TPS7H2221-SEP 抗辐射、5.5V、1.25A、115mΩ 负载开关

1 特性

- 提供供应商项目图，VID V62/22609
- 电离辐射总剂量 (TID) 为 30krad(Si)
  - 每个晶圆批次的 TID RLAT（辐射批次验收测试）：20krad (Si)
- 确定了单粒子效应 (SEE)
  - 单粒子闩锁 (SEL)、单粒子烧毁 (SEB) 和单粒子栅穿 (SEGR) 对于有效线性能量传递 (LET_{EFF}) 的抗扰度为 43MeV – cm^2/mg。
  - 单粒子瞬变 (SET) 和单粒子功能中断 (SEFI) 对于 LET_{EFF} 的额定抗扰度为 43MeV – cm^2/mg。
- 输入电压范围 (V_{IN})：1.6 至 5.5V
- 建议持续电流 (I_{MAX})：1.25A
- 导通电阻 (R_{ON})
  - V_{IN} = 5V 时典型值为 116mΩ
  - V_{IN} = 3.3V 时典型值为 115mΩ
  - V_{IN} = 1.8V 时典型值为 133mΩ
- 输出短路保护 (I_{SC})：3A（典型值）
- 低功耗：
  - 导通状态 (I_Q)：8.3μA（典型值）
  - 关闭状态 (I_{SD})：3nA（典型值）
- 可限制浪涌电流的慢速导通时序 (t_{ON})：
  - 5V 时的 t_{ON}：3.61mV/μs 下为 1.68ms
  - 3.3V 时的 t_{ON}：2.91mV/μs 下为 1.51ms
  - 1.8V 时的 t_{ON}：2.15mV/μs 下为 1.32ms
- 可调节输出放电和下降时间：
  - V_{IN} = 3.3V 时内部 QOD 电阻= 9.2Ω（典型值）
- 增强型航天塑料 (SEP)
  - 受控基线
  - 金键合线
  - NiPdAu 铅涂层
  - 一个组装和测试基地
  - 一个制造基地
  - 军用级（-55°C 到 125°C）温度范围
  - 延长了产品生命周期
  - 延长了产品变更通知 (PCN)
  - 产品可追溯性
  - 采用增强型塑封实现低释气

2 应用

- 航天卫星电源管理和配电
- 抗辐射电源树应用
- 为控制器上电和断电启用开关电源轨
- 卫星电力系统 (EPS)

3 说明

TPS7H2221-SEP 器件是一款压摆率可控的小型单通道负载开关。此器件包含一个可在 1.6V 至 5.5V 输入电压范围内运行的 N 沟道 MOSFET，并且支持 1.25A 的最大持续电流。

开关导通状态由数字输入控制，此输入可与低压控制信号直接连接。首次加电时，此器件使用智能下拉电阻来保持 ON 引脚不悬空，直到系统定序完成。按计划将该引脚驱动为高电平 (V_{ON}>V_{IH}) 之后，便会断开智能下拉电阻，以防止不必要的功率损耗。

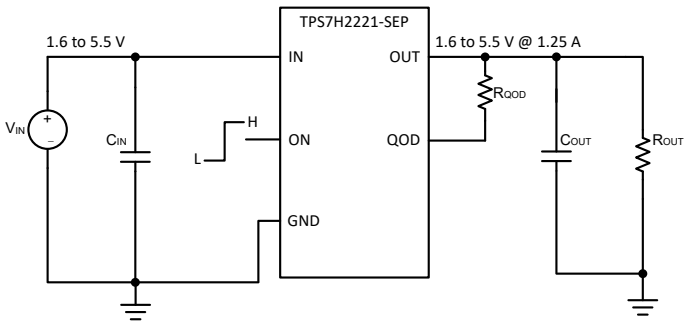
TPS7H2221-SEP 负载开关也具有自保护特性，因此可保护自己免受输出短路事件的影响。

TPS7H2221-SEP 采用标准 SC-70 封装，工作环境温度范围为 -55°C 至 125°C。

器件型号(1)	等级	封装 (2)
TPS7H2221MDCKTSEP	20krad(Si) RLAT，特征值为 30krad(Si)	SC-70 (6) 2.10mm × 2.00mm 质量 = 6.9mg
TPS7H2221EVM	评估板	EVM

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 尺寸和质量为标称值。



典型应用原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (August 2022) to Revision A (September 2022)	Page
• 将销售状态从“预告信息”更新为“初始发行版”	1
• 添加了 VID 数据表、TID、SEE 报告的链接。更新了 t_{ON} 在不同 V_{IN} 和 $R_{PD,QOD}$ 条件下的典型值	1
• Added $R_{PD,QOD}$ typical values for V_{IN}= 1.8 V, 3.3 V and 5 V	4
• Added t_{FALL} with R_{OUT}=Open, C_{OUT}=10 µF, R_{QOD}=100 Ω, R_{OUT}=Open, C_{OUT}=100 µF and R_{QOD}=0 Ω	4
• Added links to related documentation	21

5 Pin Configuration and Functions

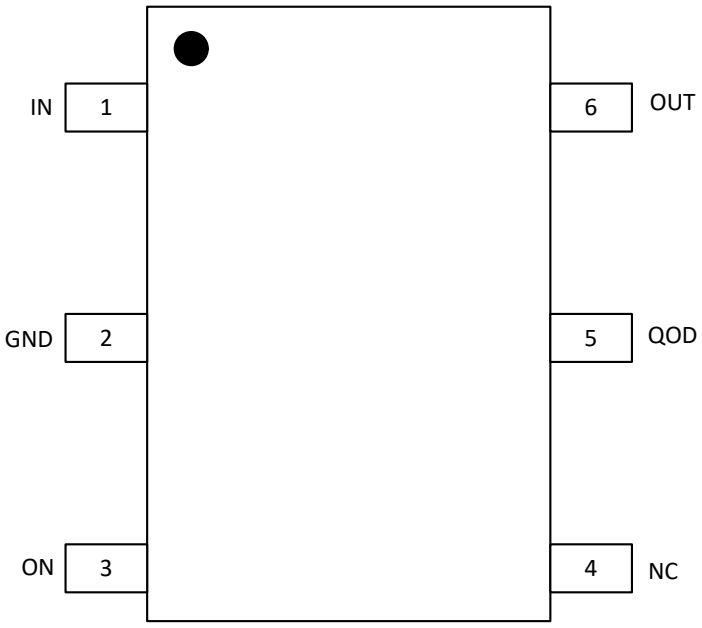


图 5-1. DCK Package
6-Pin SC-70
(Top View)

表 5-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input.
2	GND	—	Device ground.
3	ON	I	Active high switch control input. Do not leave floating.
4	NC	—	No connect. This pin is not internally connected. It is recommended to connect this pin to GND to prevent charge buildup; however, this pin can also be left open or tied to any voltage between GND and IN.
5	QOD	O	Quick Output Discharge pin. This pin can be utilized in one of three ways: • Placing an external resistor between V_{OUT} and QOD • Tying QOD directly to V_{OUT} and using the internal resistor value (R_{PD}) • Disabling QOD by leaving pin floating See the *Fall Time (t_{FALL}) and Quick Output Discharge (QOD)* section for more information.
6	OUT	O	Switch output.

(1) I = Input, O = Output, — = Other

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range (IN to GND)	– 0.3	6	V
V_{OUT}	Maximum Output Voltage Range (OUT to GND)	– 0.3	6	V
V_{ON}	Maximum ON Pin Voltage Range (ON to GND)	– 0.3	6	V
V_{QOD}	Maximum QOD Pin Voltage Range (QOD to GND)	– 0.3	6	V
I_{MAX}	Maximum Continuous Current		1.5	A
I_{PLS}	Maximum Pulsed Current (ts=2 ms, 2% Duty Cycle)		2.5	A
T_J	Junction temperature	-55	150	°C
T_{STG}	Storage temperature	– 65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range (IN to GND)	1.6		5.5	V
V_{OUT}	Output Voltage Range (OUT to GND)	0		5.5	
V_{ON}	ON Voltage Range (ON to GND)	0		5.5	
I_{MAX}	Maximum Continuous Current	0		1.25	A
T_J	Junction temperature	– 55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS7H2221-SEP DCK (SC-70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	237.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	173.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	93.9	
Ψ_{JT}	Junction-to-top characterization parameter	74.4	
Ψ_{JB}	Junction-to-board characterization parameter	93.6	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Over V_{IN} = 1.6 to 5.5 -V, $V_{ON} \geq V_{IH}$, over the temperature range (T_A=-55 ℃ to 125 ℃), unless otherwise specified. All voltage levels are reference to GND.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Supply (VIN)							
$I_{Q, VIN}$	V_{IN} Quiescent Current	V_{OUT} = Open,	25 ℃		8.3	15	μA
		V_{OUT} = Open,			8.7	20	
$I_{SD, VIN}$	V_{IN} Shutdown Current	$V_{ON} \leq V_{IL}$, V_{OUT} = GND	25 ℃		3	20	nA
		$V_{ON} \leq V_{IL}$, V_{OUT} = GND				800	
ON-Resistance (RON)							
R_{ON}	ON-State Resistance	V_{IN} = 5 V, I_{OUT} = -200 mA	-55 ℃		90	150	mΩ
			25 ℃		116	150	
			125 ℃		150	200	
		V_{IN} = 3.3 V, I_{OUT} = -200 mA	-55 ℃		89	150	mΩ
			25 ℃		115	150	
			125 ℃		150	250	
		V_{IN} = 1.8 V, I_{OUT} = -200 mA	-55 ℃		103	300	mΩ
			25 ℃		133	300	
			125 ℃		173	350	
Output Short Protection (ISC)							
I_{SC}	Short Circuit Current Limit	$V_{OUT} \leq V_{IN}$ - 1.5 V			3		A
		$V_{OUT} \leq V_{SC}$		30	512	900	mA
V_{SC}	Output Short Detection Threshold	25 ℃		0.22	0.36	0.57	V
T_{SD}	Thermal Shutdown	Rising			180		℃
		Falling			145		
Enable Pin (ON)							
I_{ON}	ON Pin Leakage	$V_{ON} \geq V_{IH}$				100	nA
$R_{PD, ON}$	Smart Pull Down Resistance	$V_{ON} \leq V_{IL}$			499		kΩ
$V_{IH,ON}$	ON Pin Input High (V_{IH} Rising)			1			V
$V_{IL,ON}$	ON Pin Input Low (V_{IL} Falling)					0.35	
Quick-output Discharge (QOD)							
$R_{PD, QOD}$	QOD Pin Internal Discharge Resistance	$V_{ON} \leq V_{IL}$	V_{IN} = 1.8-V		45.4		Ω
			V_{IN} = 3.3-V		8.5		
			V_{IN} = 5-V		6		

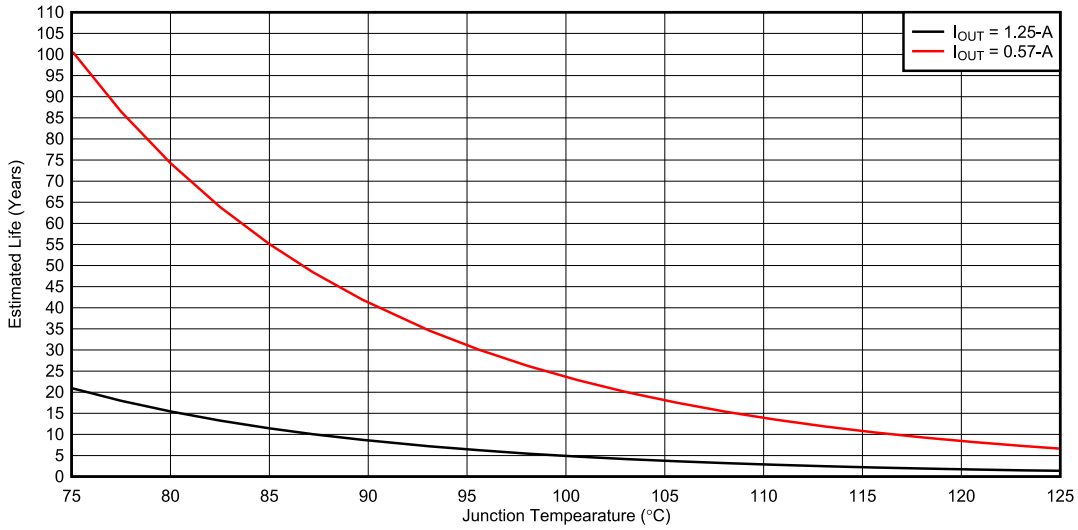
6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.3V, an ambient temperature of 25°C, R_{QOD}= 0 Ω and a load of C_{OUT}= 0.1 µF, R_{OUT} = 100 Ω. See 图 7-2

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	V_{IN} = 5.0 V			1680		µs
		V_{IN} = 3.3 V			1510		
		V_{IN} = 1.8 V			1320		
t_R	Output Rise Time	V_{IN} = 5.0 V			1120		µs
		V_{IN} = 3.3 V			915		
		V_{IN} = 1.8 V			674		
SR_{ON}	Turn ON Slew Rate	V_{IN} = 5.0 V			3.61		mV/µs
		V_{IN} = 3.3 V			2.91		
		V_{IN} = 1.8 V			2.15		
t_{OFF}	Turn OFF Time	V_{IN} = 1.8 V to 5.0V	R_{OUT} = 100 Ω, C_{OUT} = 0.1uF		5.22		µs
t_{FALL}	Output Fall Time (1)				9.6		µs
		R_{OUT} = Open (2)	C_{OUT} = 10uF, R_{QOD}=0 Ω		0.35		ms
			C_{OUT} = 10uF, R_{QOD}=100 Ω		3.12		ms
			C_{OUT} = 100uF; R_{QOD}=0 Ω		4.3		ms

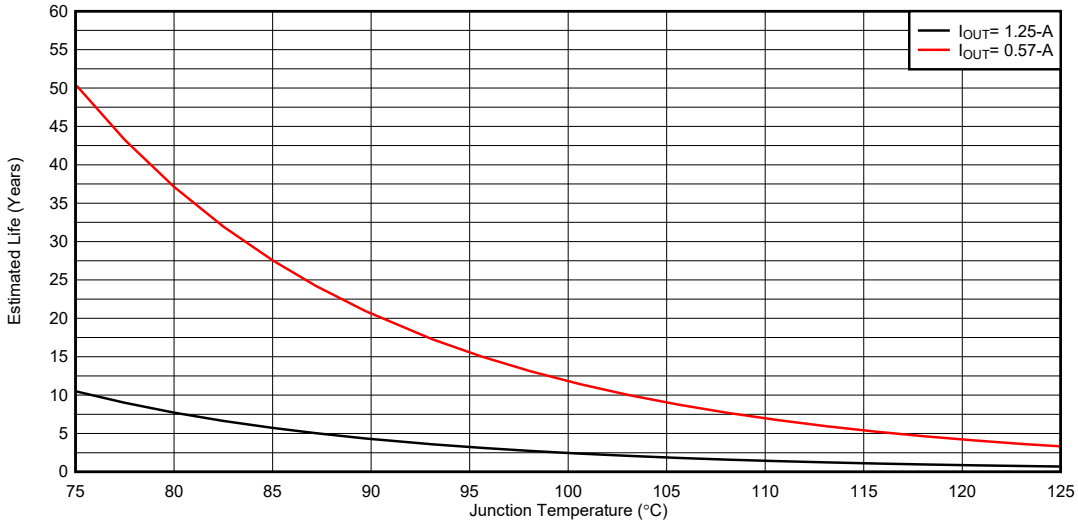
(1) Output may not discharge completely if QOD is not connected to V_{OUT}
(2) See the *Timing Application* section for information on how R_{OUT} and C_{OUT} affect Fall Time.

6.7 Derating Curves



FIT = 50

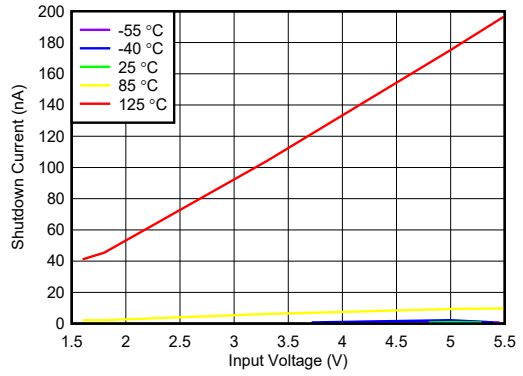
图 6-1. Estimated Life Rating Due to Electromigration vs Junction Temperature at 50% Duty Cycle



FIT=50

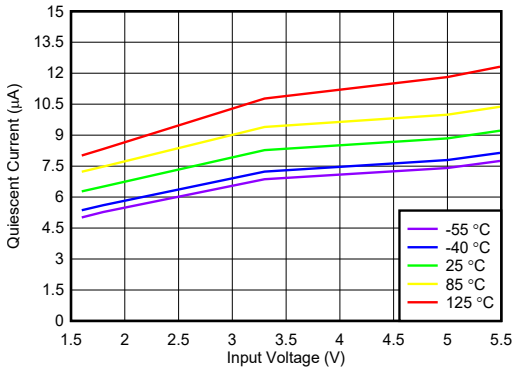
图 6-2. Estimated Life Rating Due to Electromigration vs Junction Temperature at 100% Duty Cycle

6.8 Typical Characteristics



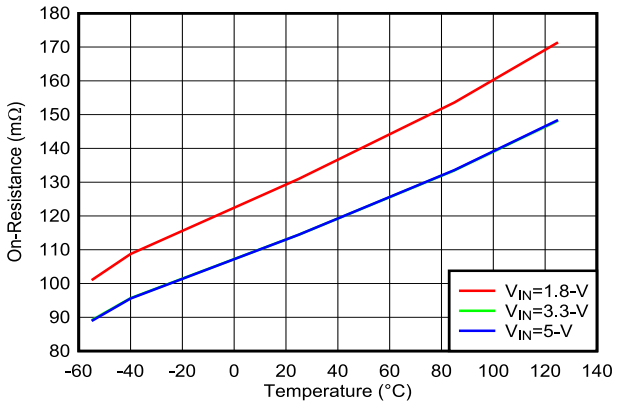
$V_{ON} \leqslant V_{IL}$

图 6-3. Shutdown Current vs Input Voltage



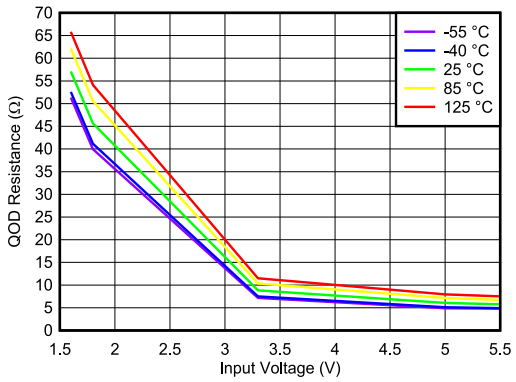
$V_{ON} \geqslant V_{IH}$

图 6-4. Quiescent Current vs Input Voltage



I_{LOAD} = – 200 mA

图 6-5. On-Resistance vs Junction Temperature



$V_{ON} \leqslant V_{IL}$

图 6-6. QOD Resistance vs Input Voltage

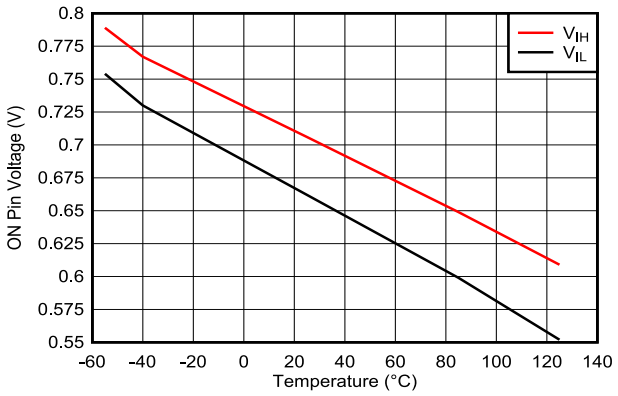
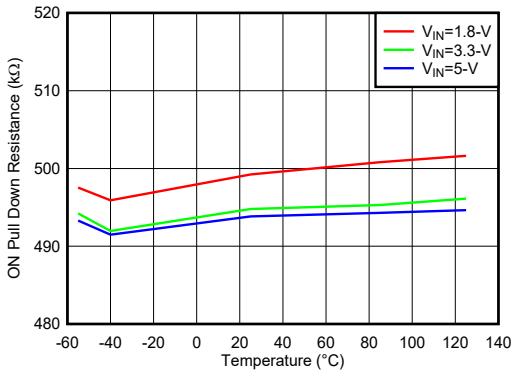
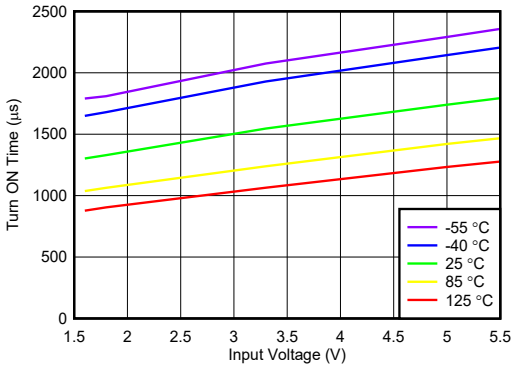


图 6-7. V_{IH}/V_{IL} vs Junction Temperature



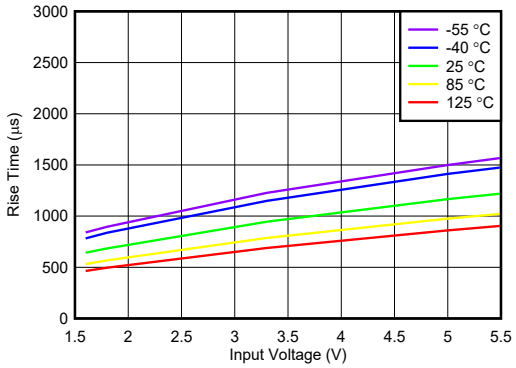
$V_{ON} \leqslant V_{IL}$

图 6-8. ON Pull Down Resistance vs Junction Temperature



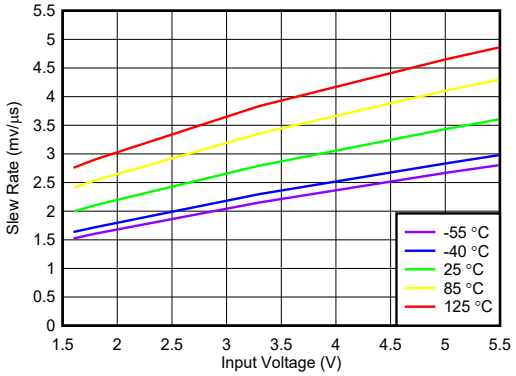
C_{OUT} = 0.1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω

图 6-9. Turn ON Time vs Input Voltage



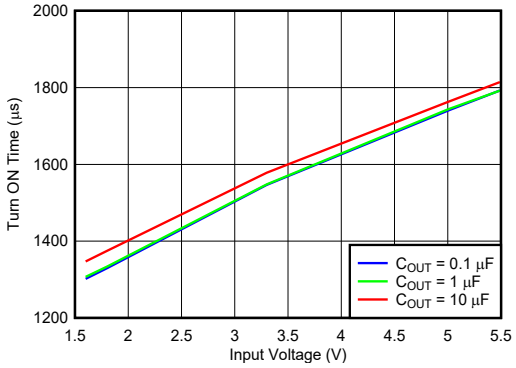
C_{OUT} = 0.1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω

图 6-10. Rise Time vs Input Voltage



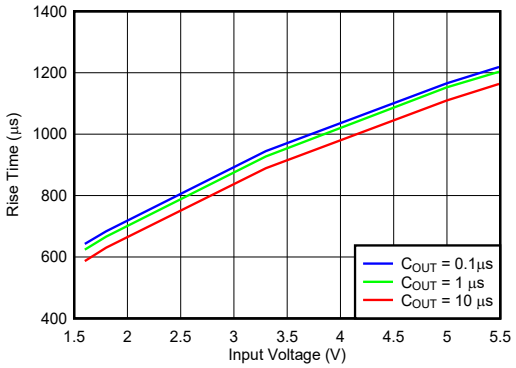
C_{OUT} = 0.1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω

图 6-11. Output Slew Rate vs Input Voltage



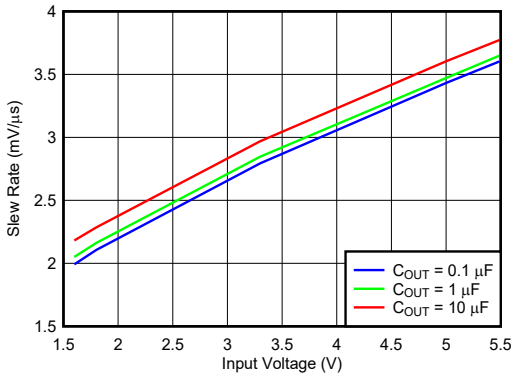
R_{OUT} = 100 Ω T_J = 25°C R_{QOD} = 0 Ω

图 6-12. Turn ON Time vs Input Voltage Across Load Capacitance



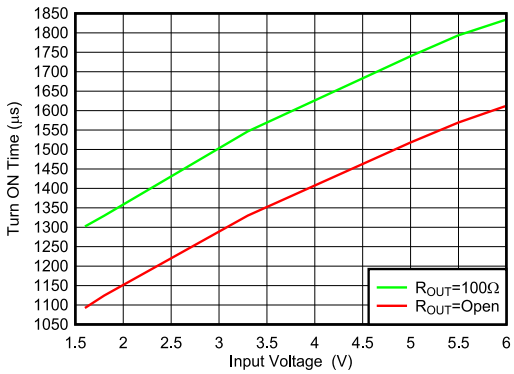
R_{OUT} = 100 Ω T_J = 25°C R_{QOD} = 0 Ω

图 6-13. Rise Time vs Input Voltage Across Load Capacitance



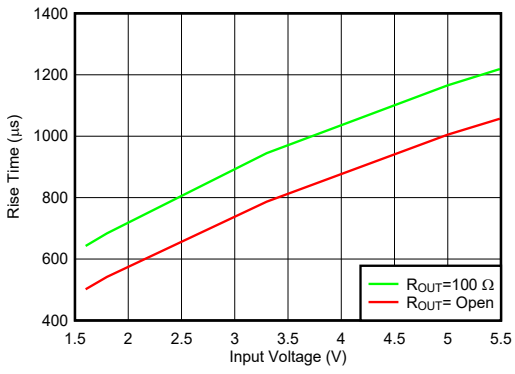
R_{OUT} = 100 Ω T_J = 25°C R_{QOD} = 0 Ω

图 6-14. Slew Rate vs Input Voltage Across Load Capacitance



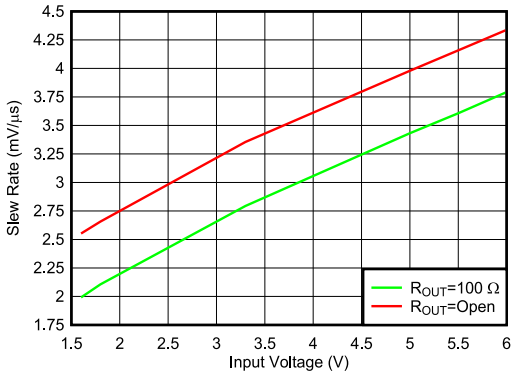
C_{OUT} = 0.1 µF T_J = 25°C R_{QOD} = 0 Ω

图 6-15. Turn ON Time vs Input Voltage Across Load Resistance



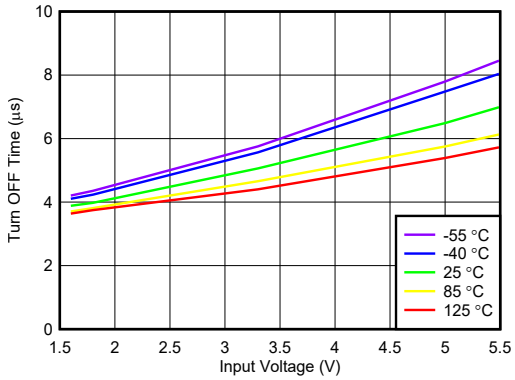
C_{OUT} = 0.1 µF T_J = 25°C R_{QOD} = 0 Ω

图 6-16. Rise Time vs Input Voltage Across Load Resistance



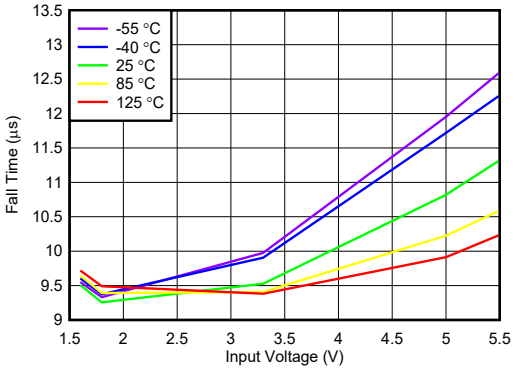
C_{OUT} = 0.1 µF T_J = 25°C R_{QOD} = 0 Ω

图 6-17. Output Slew Rate vs Input Voltage Across Load Resistance



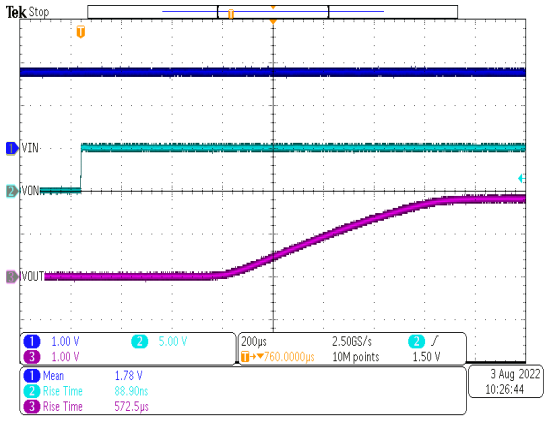
C_{OUT} = 0.1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω

图 6-18. Turn OFF Time vs Input Voltage



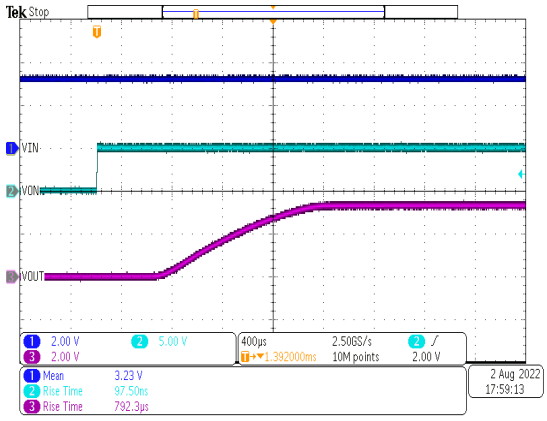
C_{OUT} = 0.1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω

图 6-19. Fall Time vs Input Voltage



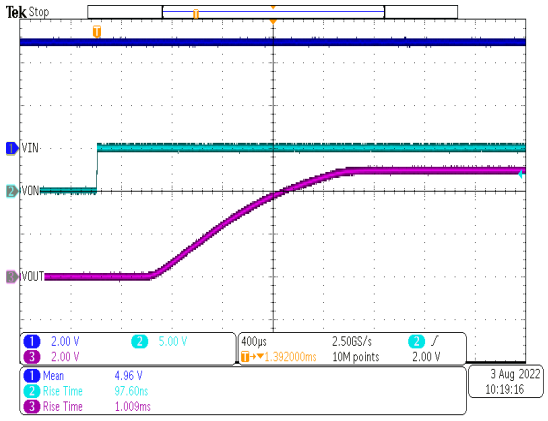
C_{IN} = 1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω
C_{OUT} = 0.1 µF

图 6-20. Rise Time with V_{IN} = 1.8 V



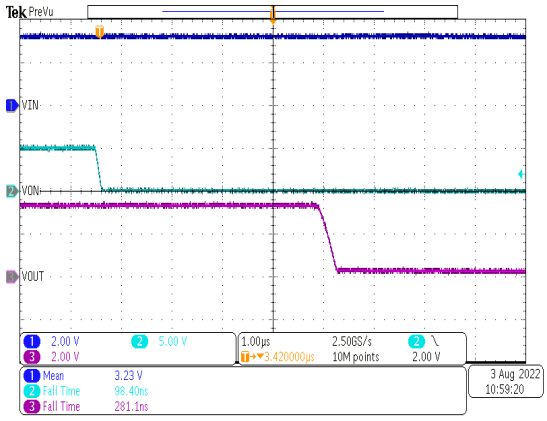
C_{IN} = 1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω
C_{OUT} = 0.1 µF

图 6-21. Rise Time with V_{IN} = 3.3 V



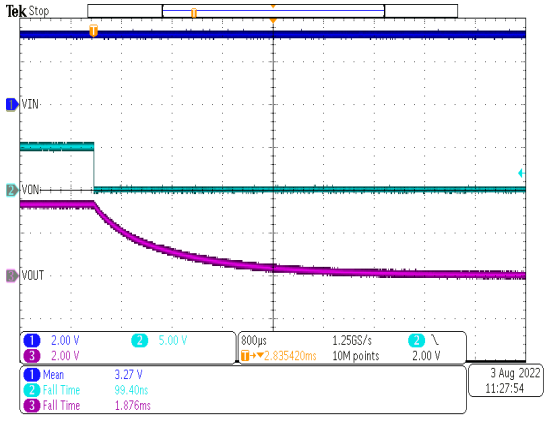
C_{IN} = 1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω
C_{OUT} = 0.1 µF

图 6-22. Rise Time with V_{IN} = 5 V



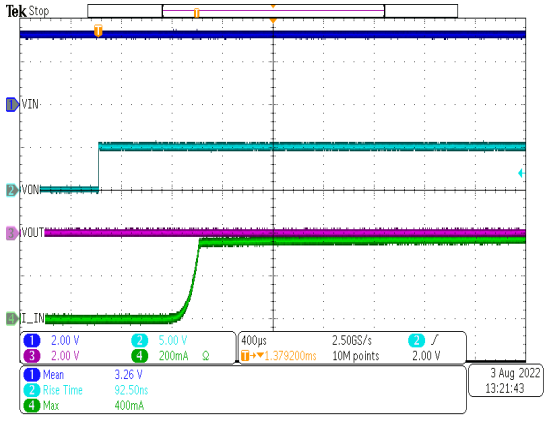
C_{IN} = 1 µF R_{OUT} = 100 Ω R_{QOD} = 2k Ω
C_{OUT} = Open

图 6-23. Turn Off with a Small Load Capacitance



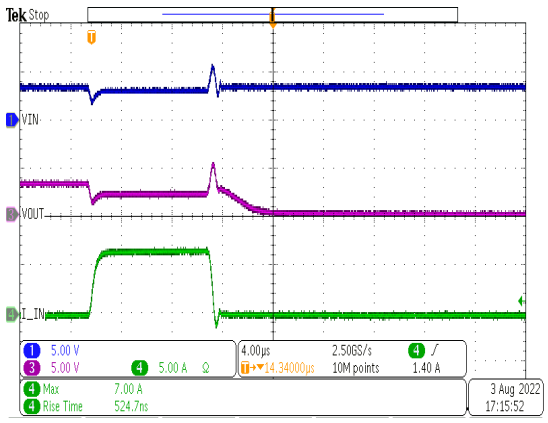
C_{IN} = 1 µF R_{OUT} = 100 Ω R_{QOD} = 2k Ω
C_{OUT} = 10 µF

图 6-24. Turn Off with a Large Load Capacitance



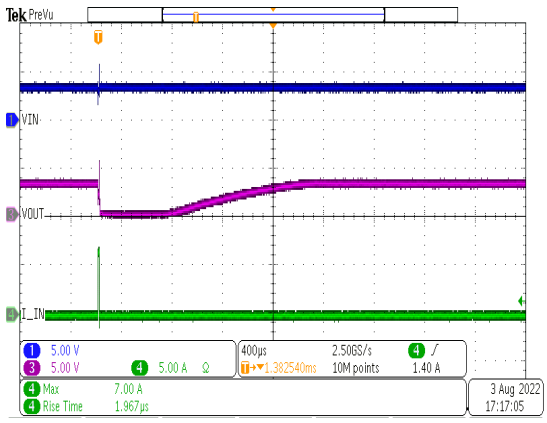
C_{IN} = 58 µF R_{OUT} = 4m Ω R_{QOD} = 0 Ω
C_{OUT} = 10 µF V_{IN} = 3.3 V

图 6-25. Turn On Into an Output Short



C_{IN} = 58 µF R_{OUT} = 300m Ω R_{QOD} = 0 Ω
C_{OUT} = 10 µF V_{IN} = 3.3 V V_{ON}=V_{IN}

图 6-26. Hot Short Event when ON

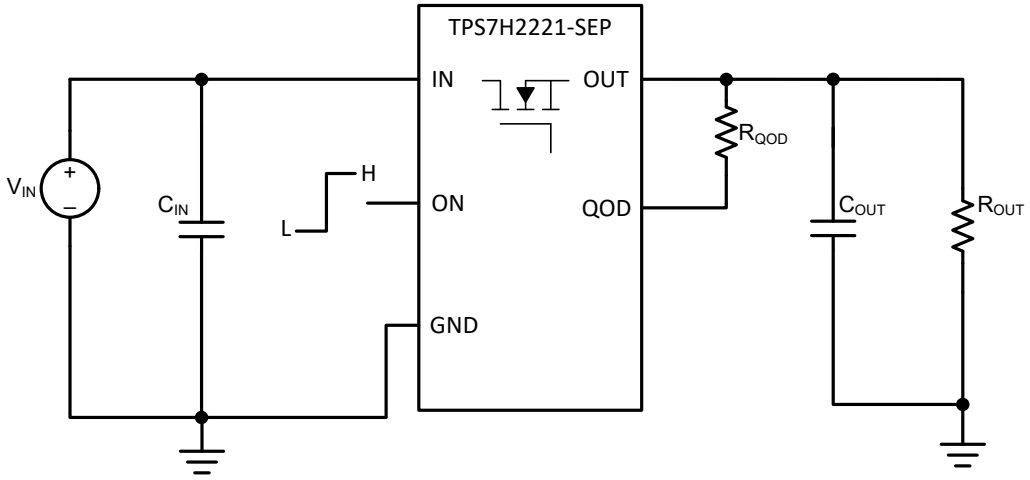


C_{IN} = 58 µF R_{OUT} = 300m Ω R_{QOD} = 0 Ω
C_{OUT} = 10 µF V_{IN} = 3.3 V V_{ON}=V_{IN}

图 6-27. Hot Short Event when ON and Recovery

7 Parameter Measurement Information

7.1 Test Circuit and Timing Waveforms Diagrams



A. Rise and fall times of the control signal are 100 ns.

B. Turn-off times and fall times are dependent on the time constant at the load. For the TPS7H2221-SEP, the internal pull-down resistance QOD is enabled when the switch is disabled. When QOD is connected to OUT using a resistor (R_{QOD}), the time constant is (R_{QOD} + $R_{PD,QOD}$ || R_{OUT}) × C_{OUT}.

图 7-1. Test Circuit

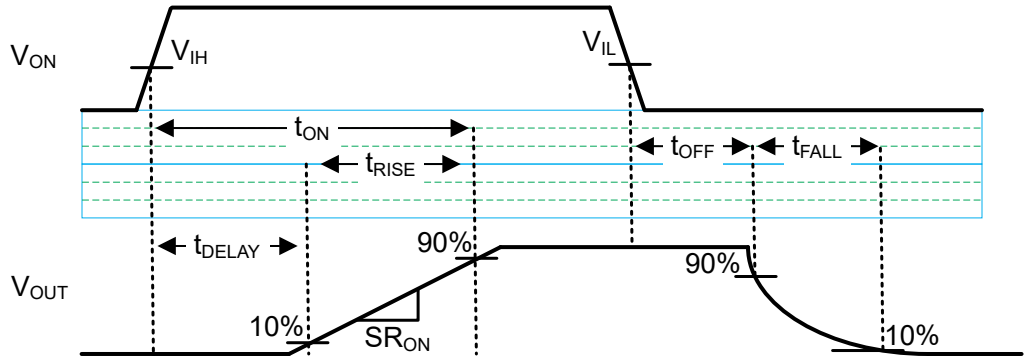


图 7-2. Timing Waveforms

8 Detailed Description

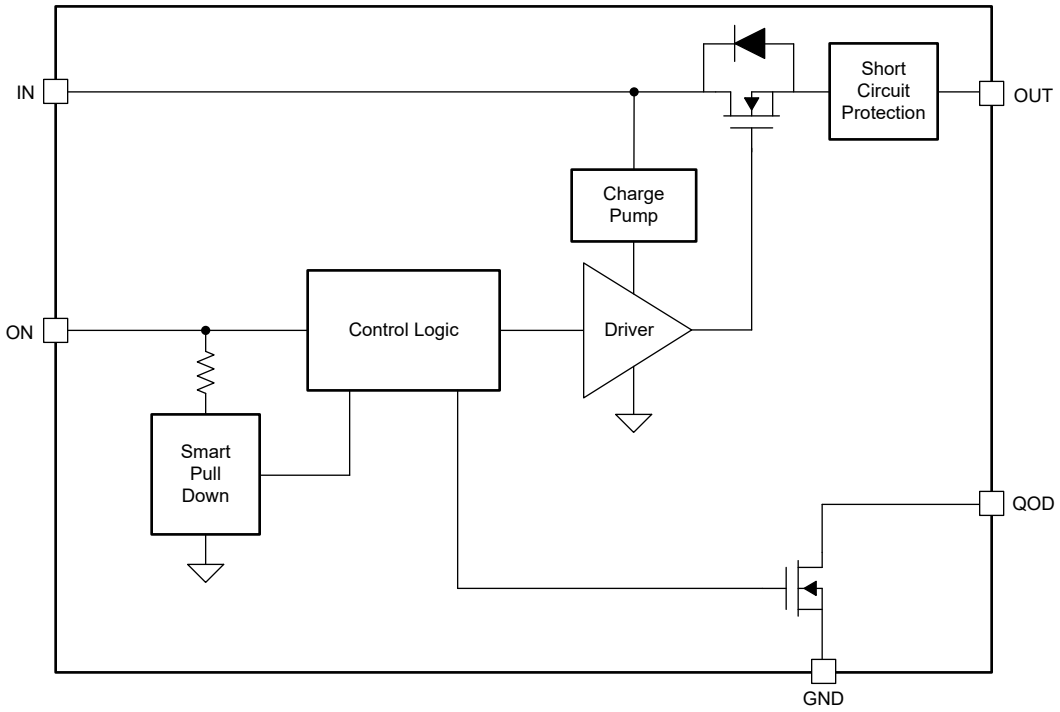
8.1 Overview

The TPS7H2221-SEP device is a 5.5-V, 1.25-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET that reduces the drop out voltage across the device.

The TPS7H2221-SEP device has a slow slew rate, which helps reduce or eliminate power supply droop because of large inrush currents during power up. Furthermore, the device features a Quick-Output-Discharge (QOD) pin, which allows the configuration of the discharge rate of V_{OUT} once the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream devices during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

The TPS7H2221-SEP load switch is also self-protected, meaning that it will protect from short circuit events on the output of the device. It also has thermal shutdown to prevent thermal runaway.

8.2 Functional Block Diagram



8.3 Feature Description

表 8-1. Smart-ON Pull Down

VON	PULL DOWN
⩽ $V_{IL,ON}$	Connected
⩾ $V_{IH,ON}$	Disconnected

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard CMOS logic threshold so it can be used in a wide variety of applications. When power is first applied to V_{IN} a Smart Pull Down is used to keep the ON pin from floating until the system sequencing is complete. Once the ON pin is deliberately driven high (⩾$V_{IH,ON}$), the Smart Pull Down is disconnected to prevent unnecessary power loss. See 表 8-1 to determine the state of the ON Pin Smart Pull Down state as function of ON pin voltage.

8.3.2 Output Short Circuit Protection (I_{SC})

The device will limit current to the output in case of output shorts. When a short occurs, the large V_{IN} to V_{OUT} voltage drop causes the switch to limit the output current (I_{SC}). When the output is below the hard short threshold (V_{SC}), a lower limit is used to minimize the power dissipation while the fault is present. The device will continue to limit the current until it reaches thermal shutdown temperature. At this time, the device will turn off until its temperature has lowered by the thermal hysteresis (35°C typical) before turning on again.

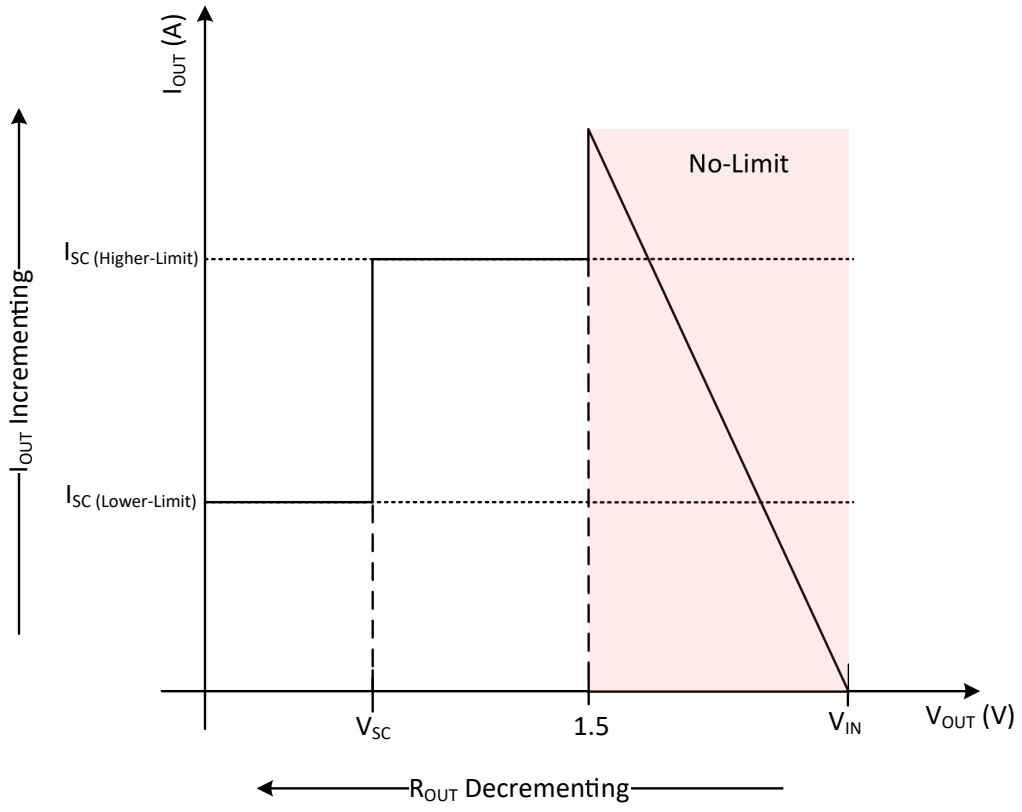


图 8-1. Output Short Circuit Current Limit

8.3.3 Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

The TPS7H2221-SEP device includes a QOD pin that can be configured in one of three ways:

- QOD pin shorted to V_{OUT} pin. Using this method, after the switch becomes disabled the discharge rate is controlled with the value of the internal resistance QOD ($R_{PD,QOD}$).
- QOD pin connected to V_{OUT} pin using an external resistor R_{QOD}. After the switch becomes disabled, the discharge rate is controlled by the value of the total discharge resistance. To adjust the total discharge resistance, 方程式 1 can be used:

$$R_{DIS} = R_{PD,QOD} + R_{QOD} \quad (1)$$

  where:

  - R_{DIS} is the total output discharge resistance (Ω)
  - $R_{PD,QOD}$ (6 Ω typ.) is the internal pulldown resistance (Ω)
  - R_{QOD} is the external resistance placed between the V_{OUT} and QOD pins (Ω)
- QOD pin is unused and left floating. Using this method, there will be no quick output discharge functionality and the output will remain floating after the switch is disabled.

The fall times of the device depend on many factors including the total discharge resistance (R_{DIS}) and the output capacitance (C_{OUT}). To calculate the approximate fall time of V_{OUT} use 方程式 2.

$$t_{FALL} = 2.2 \times (R_{DIS} \,||\, R_{OUT}) \times C_{OUT} \quad (2)$$

where:

- t_{FALL} is the output fall time from 90% to 10% (µs)
- R_{DIS} is the total QOD + R_{QOD} resistance (Ω)
- R_{OUT} is the output load resistance (Ω)
- C_{OUT} is the output load capacitance (µF)

8.3.3.1 QOD When System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor discharges at V_{IN}. Past a certain V_{IN} level, the strength of the R_{PD} will be reduced. If there is still remaining charge on the output capacitor, this will result in longer fall times. For further information regarding this condition, see the *Setting Fall Time for Shutdown Power Sequencing* section.

8.4 Device Functional Modes

表 8-2 describes the connection of the V_{OUT} pin depending on the logical state of the ON pin as well as the various QOD pin configurations.

表 8-2. V_{OUT} Connection

ON	QOD CONFIGURATION	V_{OUT}
Low	QOD pin connected to VOUT with R_{QOD}	Pull-down with ($R_{PD,\ QOD}$ + R_{QOD})
Low	QOD pin tied to VOUT directly	Pull-down with ($R_{PD,\ QOD}$)
Low	QOD pin left open	Floating
High	N/A	V_{IN}

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

9.2 Typical Application

This typical application demonstrates how the TPS7H2221-SEP devices can be used to power downstream modules.

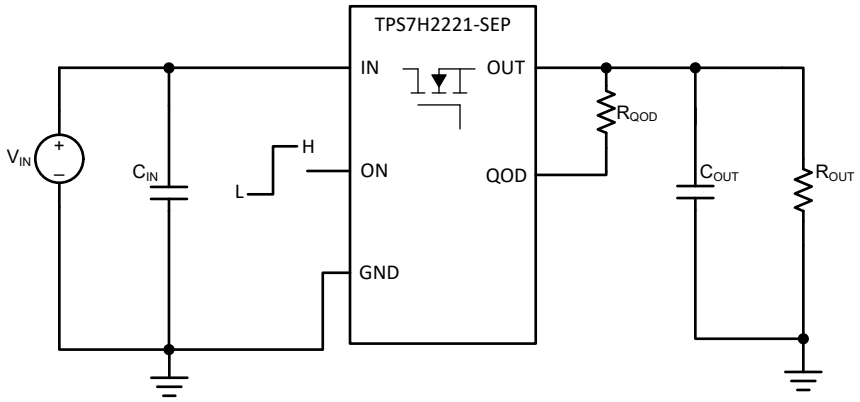


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in Design Parameters as the design parameters:

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage (V_{IN})	3.3 V
Load current resistance (R_{OUT})	1 kΩ
Load capacitance (C_{OUT})	47 µF
Minimum fall time (t_F)	40 ms
Maximum inrush current (I_{RUSH})	150 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Limiting Inrush Current

Use 方程式 3 to find the maximum slew rate value to limit inrush current for a given capacitance:

$$(\text{Slew Rate}) = I_{RUSH} \div C_{OUT} \quad (3)$$

where

- I_{INRUSH} = maximum acceptable inrush current (mA)
- C_{OUT} = capacitance on V_{OUT} (μ F)
- Slew Rate = Output Slew Rate during turn on (mV/ μ s)

Based on 方程式 3, the required slew rate to limit the inrush current to 150 mA is 3.2 mV/ μ s. The TPS7H2221-SEP has a slew rate of 2.3 mV/ μ s, so the inrush current will be below 150 mA.

9.2.2.2 Setting Fall Time for Shutdown Power Sequencing

Microcontrollers and processors often have a specific shutdown sequence in which power must be removed. Using the adjustable Quick Output Discharge function of the TPS7H2221-SEP device, adding a load switch to each power rail can be used to manage the power down sequencing. To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down.

Once the required fall time is determined, the maximum external discharge resistance (R_{DIS}) value can be found using 方程式 2:

$$t_{FALL(min)} = 2.2 \times (R_{DIS} \,||\, R_{OUT}) \times C_{OUT} \quad (4)$$

$$R_{DIS(min)} = 630\ \Omega \quad (5)$$

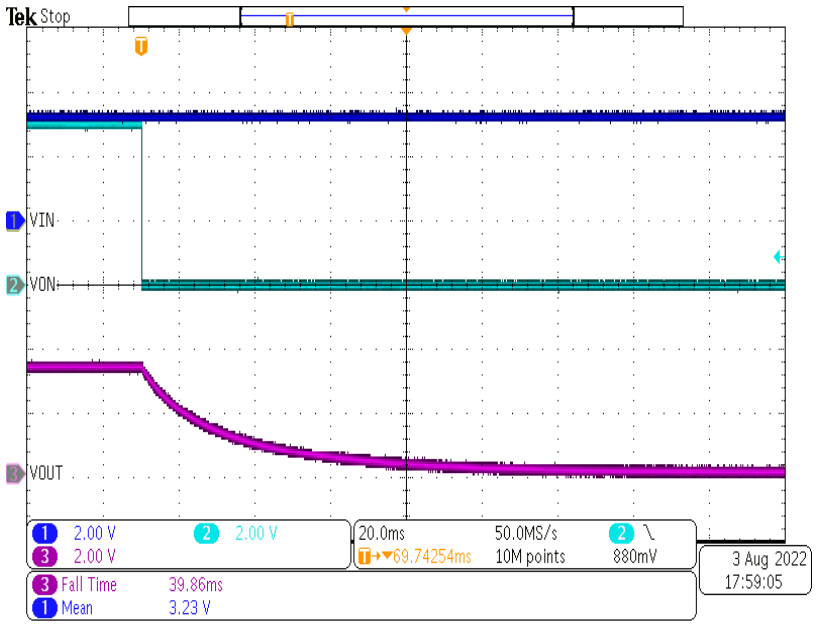
方程式 1 can then be used to calculate the R_{QOD} resistance needed to achieve a particular discharge value:

$$R_{DIS} = QOD + R_{QOD} \quad (6)$$

$$R_{QOD} = 624\ \Omega \quad (7)$$

To ensure a fall time greater than, choose an R_{QOD} value greater than 624 Ω.

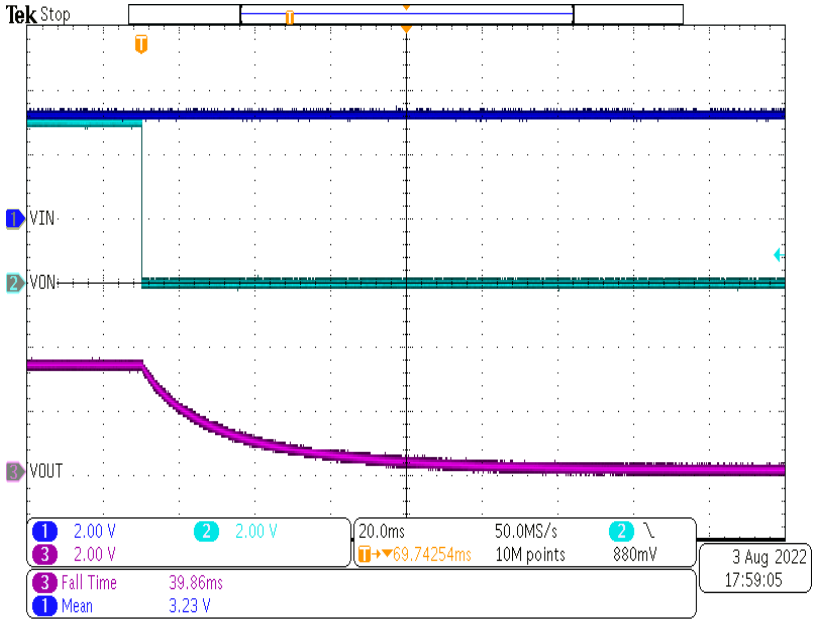
9.2.2.3 Application Curves



C_{IN} = 58.1 µF C_{OUT} = 47.1 µF R_{OUT} = 1 kΩ

图 9-2. Fall Time (R_{QOD} = 1 kΩ)

9.3 Application Curves



C_{IN} = 58.1 µF C_{OUT} = 47.1 µF R_{OUT} = 1 kΩ

图 9-3. Fall Time (R_{QOD} = 1 kΩ)

9.4 Power Supply Recommendations

The device is designed to operate with a V_{IN} range of 1.6 V to 5.5 V. The V_{IN} power supply must be well regulated. The power supply must be able to withstand all transient load current steps. In most situations, using an minimum input capacitance (C_{IN}) of 1 μF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

9.5 Layout

9.5.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for IN, OUT, and GND helps minimize the parasitic electrical effects.

9.5.2 Layout Example

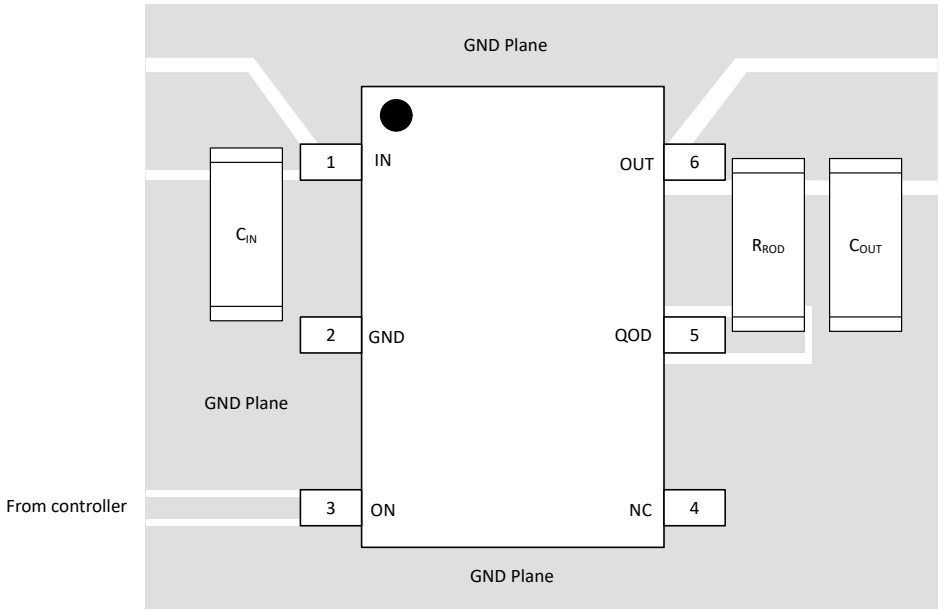


图 9-4. Recommended Board Layout

10 Device and Documentation Support

10.1 Related Documentation

For related documentation see the following:

- Texas Intruments, TPS7H2221-SEP Total Ionizing Dose (TID)
- Texas Intruments,TPS7H2221-SEP Single-Event Effects (SEE) Test Report
- Texas Intruments, TPS7H2221-SEP Neutron Displacement Damage (NDD) Characterization
- Texas Intruments, TPS7H2221-SEP Evaluation Module (EVM)
- Texas Intruments, TPS7H2221-SEP PSpice Transient Model
- Texas Intruments, Basics of Load Switches

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10.6 Export Control Notice

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7H2221MDCKTSEP	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	
TPS7H2221MDCKTSEP.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	
V62/22609-01XE	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

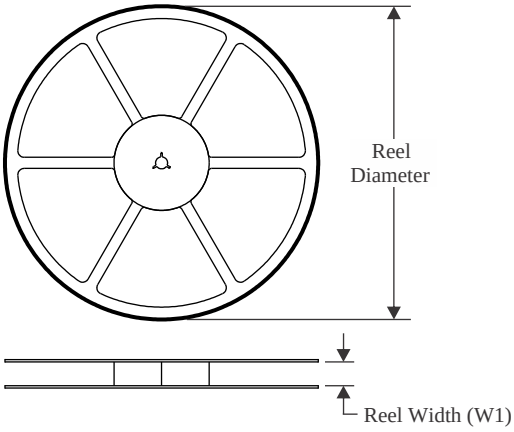
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

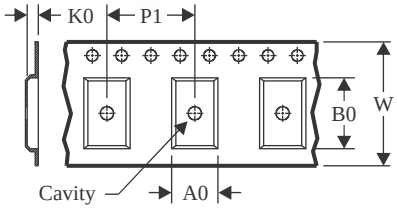
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

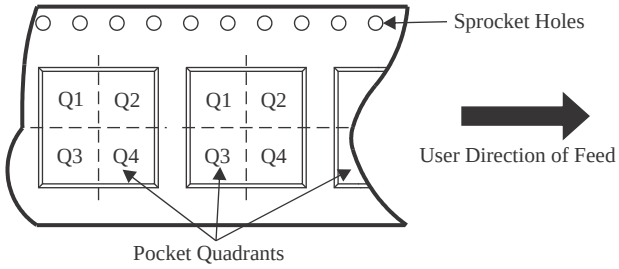


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

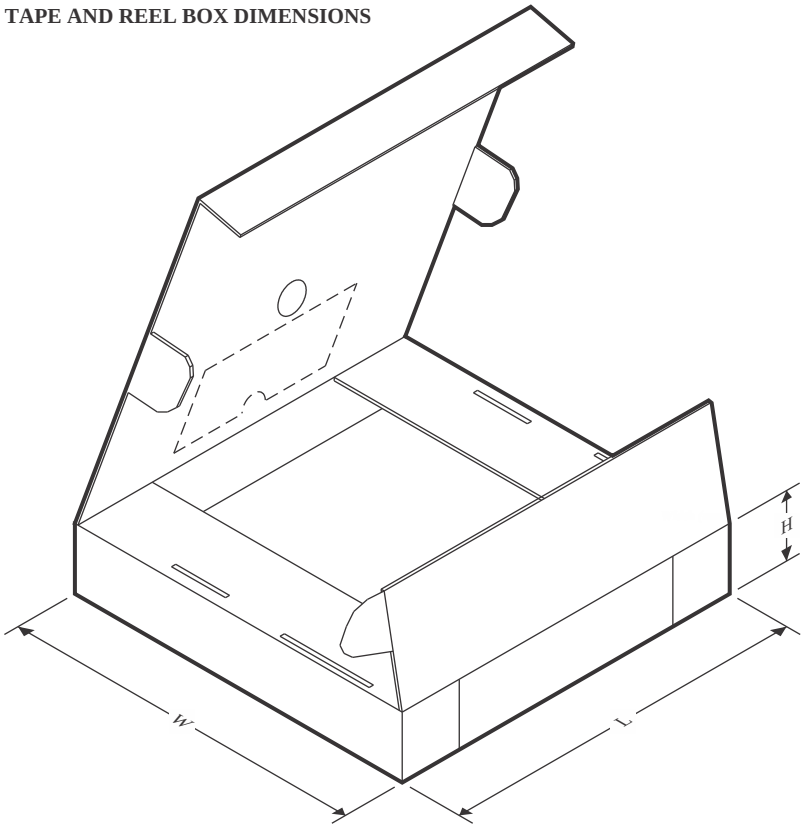
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7H2221MDCKTSEP	SC70	DCK	6	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

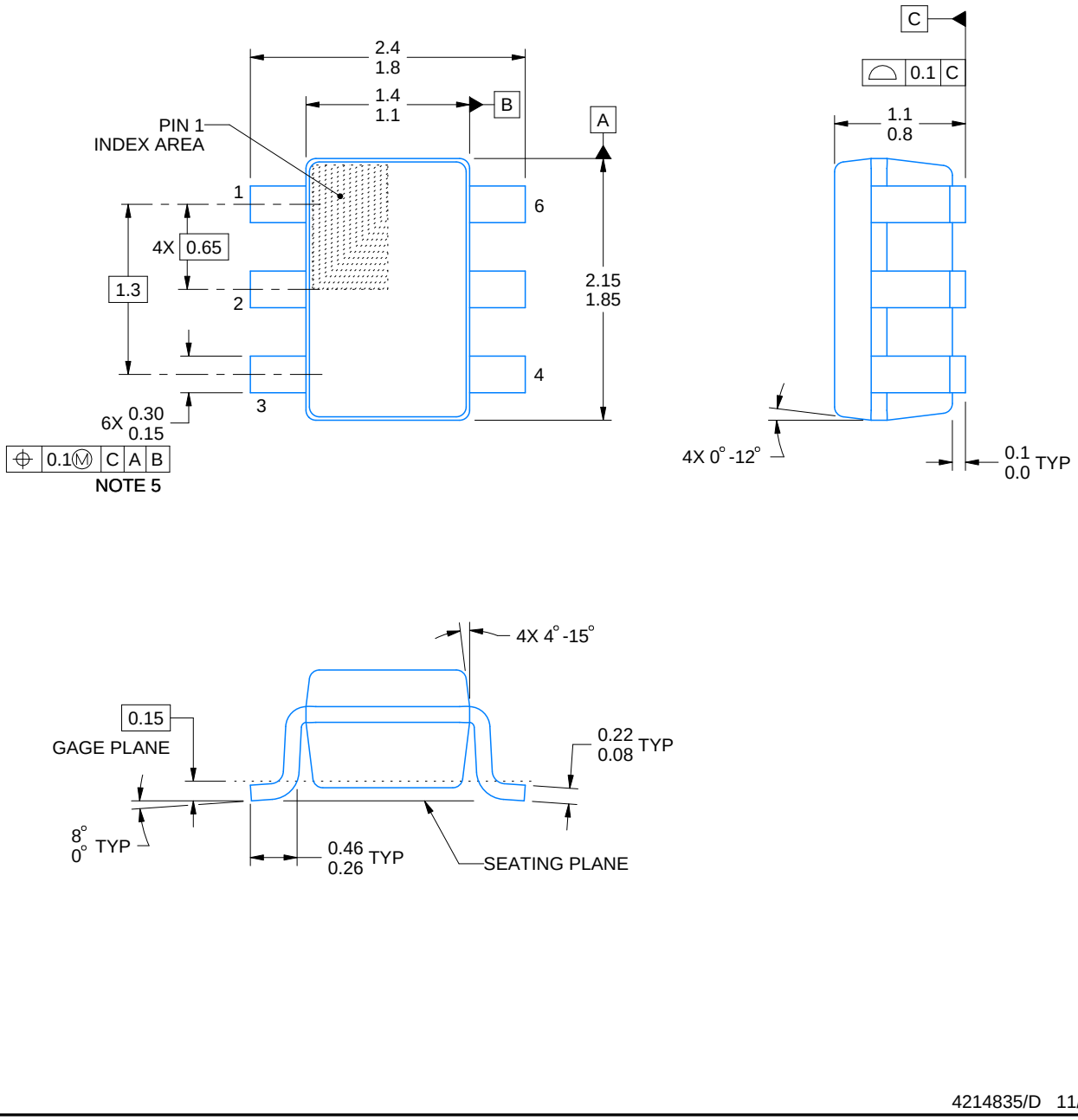
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7H2221MDCKTSEP	SC70	DCK	6	250	202.0	201.0	28.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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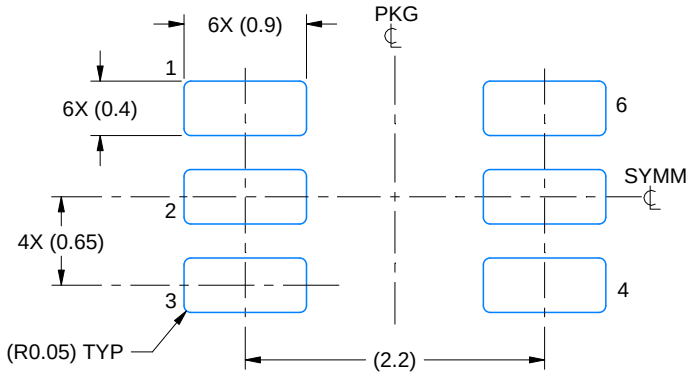
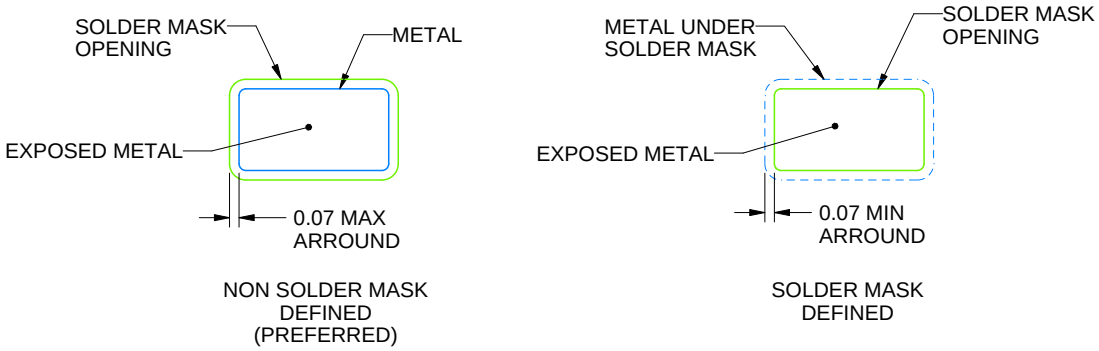
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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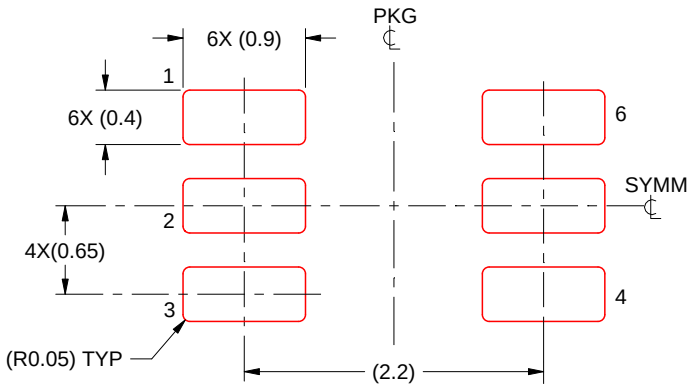
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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