TPS7H1101-SP 1.5V 至 7V 输入 3A 耐辐射、超低压差 (LDO) 稳压器

1 特性

- 5962R13202：
  - 耐辐射保障 (RHA) 高达 100krad (Si) TID
  - 总电离剂量为 100krad (Si)
  - 无低剂量率辐射损伤增强 (ELDRS) 100krad (Si)
  - 剂量率达 10mRAD (si)/s
  - 单粒子锁定 (SEL) 对于 LET 的抗扰度 = 85MeV-cm^2/mg
  - SEB 和 SEGR 对于 LET 的抗扰度 = 85MeV-cm^2/mg
  - SET/SEFI 启动阈值大于 40MeV-cm^2/mg，详情请参阅*辐射报告*
    - 专为降低干扰而设计，以避免损坏重要的下行组件
  - 有关 SET/SEFI 横截面图的详细信息，请参见*辐射报告*
- 超低输入电压范围：1.5V 至 7V
- 3A 最大输出电流
- 电流共享/并联工作可提供最高可达 6A 的输出电流
- 与陶瓷输出电容一起工作时保持稳定
- 线路、负载和温度范围内的精度为 ±2%
- 通过外部电容实现可编程软启动
- 用于电源排序的输入使能和电源正常输出
- 超低压降 LDO 电压：1A (25°C)、V_{OUT} = 1.8V 时为 62mV
- 低噪声：V_{IN} = 2V、V_{OUT} = 1.8V、电流为 3A 时为 20.33 μVRMS
- 电源抑制比 (PSRR)：1kHz 频率下超过 45dB
- 出色的负载/线路瞬态响应
- 折返电流限制
- 请参见工具和软件 (Tools & Software) 选项卡
- 耐热增强型 CFP 封装 (0.6°C/W $R_{\theta JC}$)

2 应用

- 用于 FPGA、微控制器、ASIC 和数据转换器的太空卫星负载点电源
- 太空卫星有效载荷
- 用于射频、压控振荡器、接收器和放大器的耐辐射低噪声线性稳压器
- 洁净模拟电源需求
- 可用于军用温度范围，即 -55°C 至 125°C
- 提供工程评估 (/EM) 样品 (1)

3 说明

TPS7H1101-SP 是一款采用 PMOS 导通元件配置的耐辐射 LDO 线性稳压器。此器件可在 1.5V 至 7V 的宽输入电压范围内运行，同时提供出色的 PSRR。

TPS7H1101-SP 通过 极宽的调节范围实现了精确的可编程折返电流限值功能。为了满足 FPGA、DSP 或微控制器的复杂电源要求，TPS7H1101-SP 提供使能导通和关断功能、可编程软启动、电流共享功能以及电源正常开漏输出。

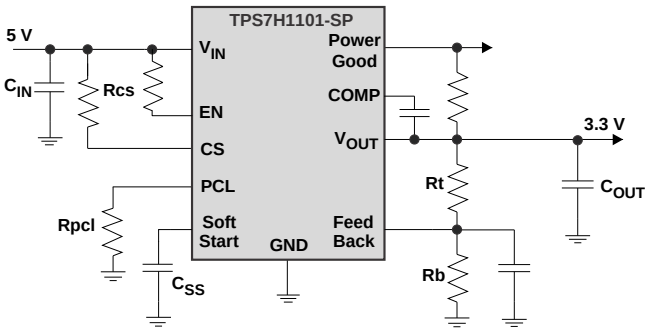
器件信息(2)

器件型号	封装	封装尺寸（标称值）
TPS7H1101-SP	CFP (16)	11.00mm x 9.60mm

(1) 这些部件仅用于工程评估。以非合规性流程对其进行了处理（即未进行老化处理等操作）并且仅在 25°C 的额定温度下进行了测试。这些部件不适用于质检、生产、辐射测试或飞行。这些零部件无法在 –55°C 至 125°C 的完整 MIL 额定温度范围内或运行寿命中保证其性能。

(2) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路



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4 修订历史记录

Changes from Original (January 2016) to Revision A **Page**

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- Changed max output voltage from V_{IN} : to 7.5 V ... 6
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- Deleted worst case dropout voltage specifications *Electrical Characteristics* table ... 7
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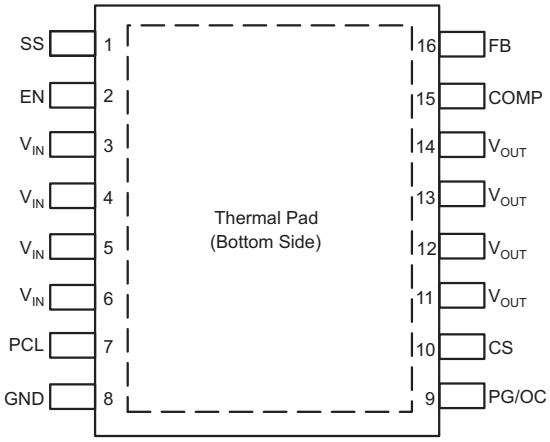
5 说明 （续）

TPS7H1101-SP 采用 16 引脚耐热增强型陶瓷扁平封装 (CFP)。

6 Pin Configuration and Functions

HKR Package
16-Pin CFP
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SS	1	O	Soft-start terminal. Connecting an external capacitor slows down the output voltage ramp rate after enable event. The soft-start terminal can be used to disable the device as described in the *Soft Start* section.
EN	2	I	Enable terminal. Driving this terminal to logic high enables the device; driving the terminal to logic low disables the device. V_{IN} voltage must be greater than 3.5 V when using the EN pin. For V_{IN} < 3.5 V, enable terminal cannot be used to disable the device. TI recommends to connect the enable terminal to V_{IN}.
V_{IN}	3	I	Unregulated supply voltage. TI recommends to connect an input capacitor as a good analog circuit practice.
	4		
	5		
	6		
PCL	7	O	Programmable current limit. A resistor to GND sets the overcurrent limit activation point. The range of resistor that can be used on the PCL terminal to GND is 8.2 kΩ to 160 kΩ.
GND	8	—	Ground/thermal pad.(1)
PG/OC	9	O	Power Good terminal. PG is an open-drain output to indicate the output voltage reaches 90% of target. PG terminal is also used as indicator when an overcurrent condition is activated. PG pin should have a pull-up resistor to the V_{OUT} pin.
CS	10	O	Current sense terminal. Resistor connected from CS to V_{IN}. CS terminal indicates voltage proportional to output current. CS terminal low: Foldback current limit disabled CS terminal high: Foldback current limit enabled
V_{OUT}	11	O	Regulated output.
	12		
	13		
	14		
COMP	15	I	Internal compensation point for error amplifier.
FB	16	I	The output voltage feedback input through voltage dividers. See *Adjustable Output Voltage (Feedback Circuit)* section.

(1) Thermal pad must be connected to GND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}, PG	–0.3	7.5	V
	FB, COMP, PCL, CS, EN	–0.3	V_{IN} + 0.3	V
Output voltage	V_{OUT}, SS	–0.3	7.5	V
PG terminal sink current		0.001	5	mA
Maximum operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature	–55		125	°C
t_R EN	Rise time (10% to 90%) for EN signal	100			µs
t_R VIN	Rise time (10% to 90%) for VIN = EN	1			ms

7.4 Thermal Information

THERMAL METRIC(1)(2)		TPS7H1101-SP HKR (CFP) 16 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) Do not allow package body temperature to exceed 265°C at any time or permanent damage may result.
(2) Maximum power dissipation may be limited by overcurrent protection.

7.5 Electrical Characteristics

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		1.5		7	V
V_{FB}	Feedback terminal voltage(1)	0 A ≤ I_{OUT} ≤ 3 A, 1.5 V ≤ V_{IN} ≤ 7 V	0.594	0.605	0.616	V
V_{OUT}	Output voltage range		0.8		V_{IN}	V
	Output voltage accuracy(1)	0 A ≤ I_{OUT} ≤ 3 A, 1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, 1.2 V, 1.8 V, 6.65 V	–2%		2%	
ΔV_{OUT}%/ ΔV_{IN}	Line regulation	1.5 V ≤ V_{IN} ≤ 7 V	-0.07	0.01	0.07	%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation	0.8 V ≤ V_{OUT} ≤ 6.65 V, 0 ≤ I_{Load} ≤ 3 A		0.08		%/A
ΔV_{OUT}	DC input line regulation	1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, 1.2 V, 1.8 V, I_{OUT} = 10 mA, T_J = –55°C(2)		0.5	3	mV
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, 1.2 V, 1.8 V, I_{OUT} = 10 mA, T_J = 25°C(2)		0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, 1.2 V, 1.8 V, I_{OUT} = 10 mA, T_J = 125°C(2)		0.2	1.0	

(1) The output voltage accuracy of condition at I_{OUT} = 2 A and I_{OUT} = 3 A is specified by characterization, but not production tested.
(2) Line and load regulations done under pulse condition for t < 10 ms.

Electrical Characteristics (continued)

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_O	DC output load regulation(3)	V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = –55°C(2)		0.4	1.0	mV
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(2)		0.6	1.1	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(2)		0.8	1.3	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = –55°C(2)		0.8	1.8	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(2)		1.3	1.8	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(2)		1.6	2.4	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = –55°C(2)		1.1	1.9	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(2)		1.9	2.6	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(2)		2.5	3.4	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 1 A, T_J = –55°C(2)		0.3	1.2	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(2)		0.5	1.3	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(2)		0.6	1.3	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 2 A, T_J = –55°C(2)		0.8	1.6	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(2)		1.1	2.1	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(2)		1.5	2.1	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 3 A, T_J = –55°C(2)		1.0	1.7	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(2)		1.1	2.4	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(2)		2.2	3.5	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = –55°C(2)		0.1	0.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(2)		0.3	0.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(2)		0.4	1.2	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = –55°C(2)		1.4	2.4	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(2)		0.7	1.4	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(2)		0.6	1.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = –55°C(2)		2.5	3.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(2)		1.2	2.1	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(2)		1.2	2.5	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 1 A, T_J = –55°C(2)		1.5	2.9	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(2)		0.4	2.6	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(2)		2.8	3.5	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 2 A, T_J = –55°C(2)		3.5	5.9	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(2)		1.1	4.7	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(2)		5.8	8.0	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 3 A, T_J = –55°C(2)		5.6	9.3	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(2)		3.7	8.0	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(2)		13.0	25	
V_{DO}	Dropout voltage(3)	I_{OUT} = 3 A, V_{OUT} = 1.3 V, V_{IN} = V_{OUT} + V_{DO}		210	335	mV
I_{CL}	Programmable output current limit range	V_{IN} = 1.5 V, V_{OUT} = 1.2 V , PCL resistance = 47 kΩ	500		750	mA
		V_{IN} = 1.5 V, V_{OUT} = 1.2 V , PCL resistance varies	200		3500(4)	
V_{CS}	Operating voltage range at CS		0.3		V_{IN}	V
CSR	Current sense ratio	I_{LOAD} / I_{CS}, V_{IN} = 2.3 V, V_{OUT} = 1.9 V	47394	47500	56000	A/A

(3) The parameter is specified to the limit in characterization, but not production tested.
(4) The maximum limit of the I_{CL}parameter is specified to the limit in characterization, but not production tested.

Electrical Characteristics (continued)

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{GND}	GND terminal current	V_{IN} = 1.5 V, V_{OUT} = 1.2 V, I_{OUT} = 2 A			10	16	mA
I_Q	Quiescent current (no load)	V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 0 A			7	10	mA
I_{SHDN}	Shutdown current	1.5 V ≤ V_{IN} ≤ 7 V			26	230	µA
		1.5 V ≤ V_{IN} ≤ 7 V, post 100 kRads (si), T_J = 25°C(5)				1400	µA
I_{SNS}, I_{FB}	FB/SNS terminal current	V_{IN} = 7 V, V_{OUT} = 6.65 V			1	5	nA
I_{EN}	EN terminal input current	V_{IN} = 7 V, V_{EN} = 7 V, V_{OUT} = 6.65 V			20	150	nA
V_{ILEN}	EN terminal input low (disable)	3.5 V < V_{IN} < 7 V			0.30 × V_{IN}		V
V_{IHEN}	EN terminal input high (enable)	3.5 V < V_{IN} < 7 V			0.75 × V_{IN}		V
Eprop Dly	Enable terminal propagation delay	V_{IN} = 2.2 V, EN rise to I_{OUT}rise			650	1000	µs
T_{EN}	Enable terminal turn-on delay	V_{IN} = 2.2 V, V_{OUT} = 1.8 V, I_{LOAD} = 1 A, C_{OUT} = 220 µF, C_{SS} = 2 nF			1.4	1.6	ms
V_{THPG}	PG threshold	No load, 0.8 V ≤ V_{OUT} ≤ 6.65 V		86%	90%		
$V_{THPGHYS}$	PG hysteresis	1.5 V ≤ V_{IN} ≤ 7 V			2%		
V_{OLPG}	PG terminal output low	I_{PG} = –1 mA to 0 mA			120	300	mV
I_{LKGPG}	PG terminal leakage current	V_{OUT} > V_{THPG}, V_{PG} = 1.2 V			0.2	1.5	µA
		V_{OUT} > V_{THPG}, V_{PG} = 7 V			0.5	2.5	
I_{SS}	SS terminal charge current	V_{IN} = 1.5 V to 7 V			2.5	3.5	µA
I_{SSdisb}	SS terminal disable current	V_{IN} = 1.5 V to 7 V			5	10	µA
V_{SS}	SS terminal voltage (device enabled)(6)	V_{IN} = 1.5 V to 7 V				1.232	V
V_{SSdisb}	SS terminal low-level input voltage to disable device	V_{IN} = 1.5 V to 7 V				0.4	V
PSRR	Power-supply rejection ratio	V_{IN} = 2.5 V, V_{OUT} = 1.8 V, C_{OUT} = 220 µF	1 kHz		48		dB
			100 kHz		25		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 3 A, V_{IN} = 2 V, V_{OUT} = 1.8 V			20.33		$µV_{RMS}$
TSD	Thermal shutdown temperature				185		°C

(5) This maximum limit applies to SMD 5962R13202 post 100 kRads (Si) test at 25°C.
(6) Any external pullup voltage should not exceed 1.188 V.

7.6 Typical Characteristics

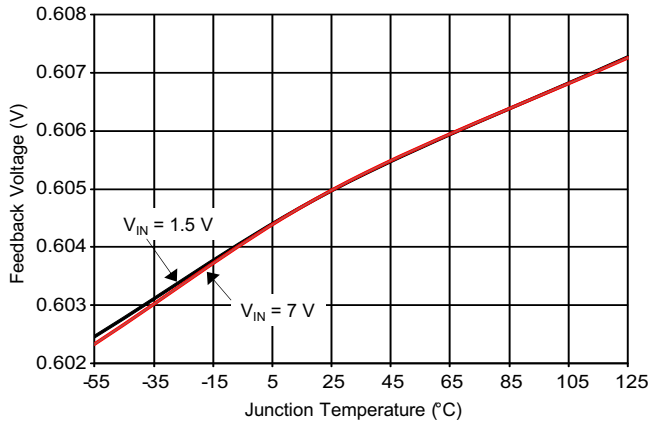


Figure 1. Feedback Voltage vs Temperature

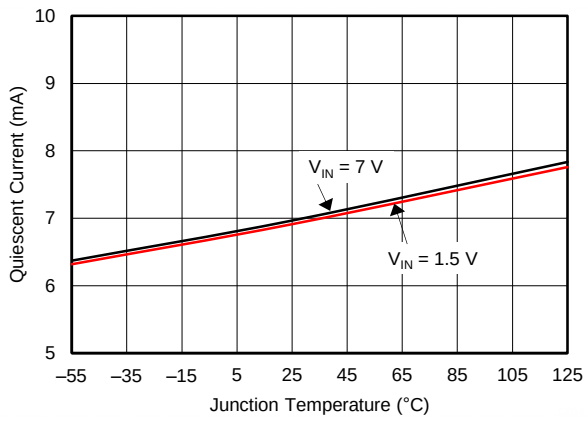


Figure 2. Quiescent Current vs Temperature

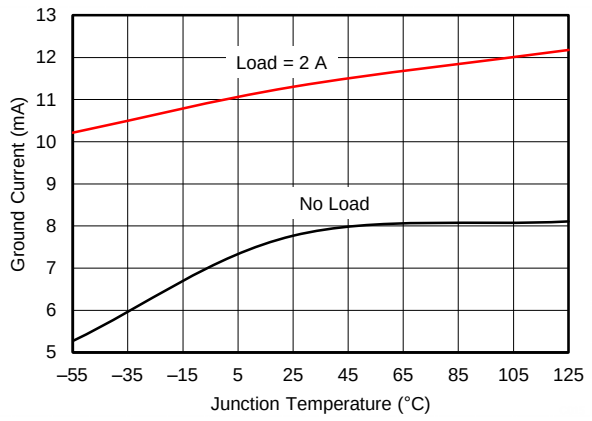


Figure 3. Ground Current vs Temperature

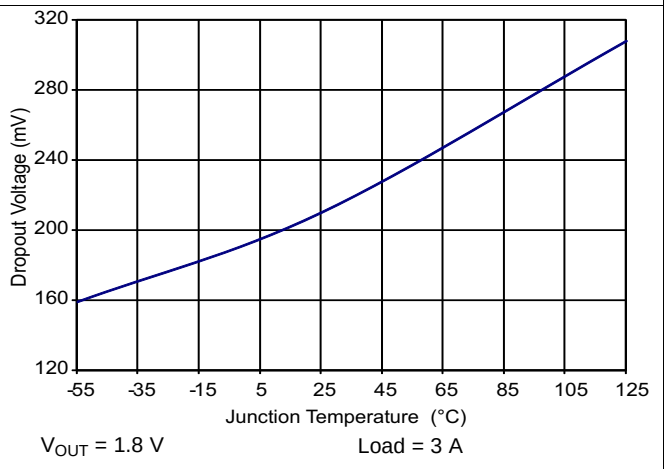


Figure 4. Dropout Voltage vs Temperature

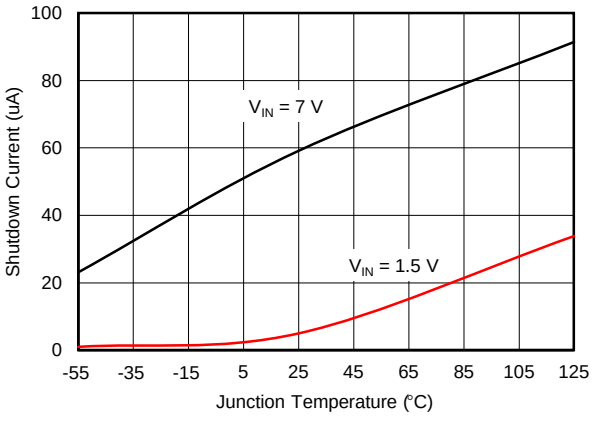


Figure 5. Shutdown Current vs Temperature

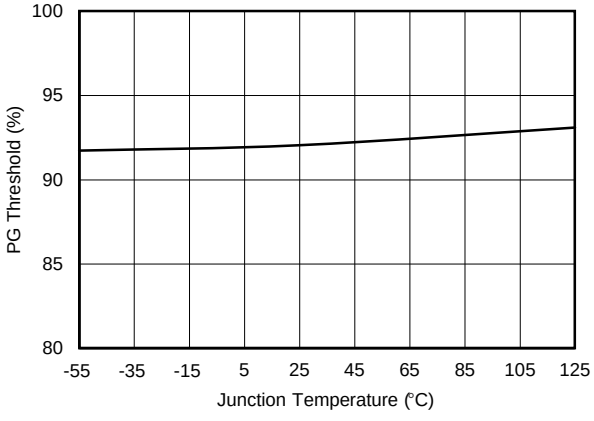
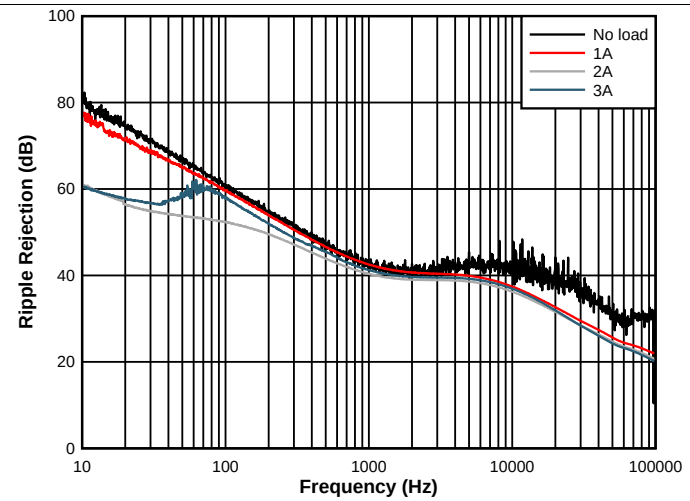


Figure 6. PG Threshold vs Temperature

Typical Characteristics (continued)



V_{IN} = 2.5 V V_{OUT} = 1.8 V

Figure 7. Power Supply Ripple Rejection vs Frequency

8 Detailed Description

8.1 Overview

The TPS7H1101-SP is 3-A, 1.5-V to 7-V LDO linear regulator that uses PMOS pass element configuration.

It uses TI's proprietary process to achieve low noise, high PSRR combined with high thermal performance in a 16-pin ceramic flatpack package (HKR).

A number of features are incorporated in the design to provide high reliability and system flexibility. Current foldback, current limit, and thermal protection are incorporated in the design to make it viable for harsh environments.

The device also has a current sense monitoring feature. A resistor connected from the current sense (CS) terminal to VIN indicates voltage proportional to the output current. When CS is held high, foldback current limit is enabled. Shorting CS low disables the foldback current limit.

A resistor connected from the programmable current limit (PCL) terminal to ground sets the over current limit activation point. When overcurrent limit activation point is reached, it results in LDO going into current foldback mode. Output current is reduced to approximately 50% of the current limit set point. *PCL* section provides a detailed description of this feature.

TPS7H1101-SP incorporates thermal protection, which disables the output when the junction temperature rises approximately 185°C, allowing the device to cool. Cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

A resistor connected from the CS terminal to VIN indicates voltage proportional to the output load current.

To provide system flexibility for demanding current needs, the LDO can be configured in parallel operation as indicated in Figure 22. *Current Sharing* section provides detailed parallel operation information.

An enable feature is incorporated in the design allowing the user to enable or disable the LDO. Power Good, an open-drain connection, indicates the status of the output voltage. These provide the customers system flexibility in monitoring and controlling the LDO operation. When using the Enable function, V_{IN} voltage must be > 3.5 V. For V_{IN} from 1.5 V to 7 V, TPS7H1101-SP can be disabled using the soft-start (SS) terminal as described in *Enable/Disable* section.

8.2 Functional Block Diagram

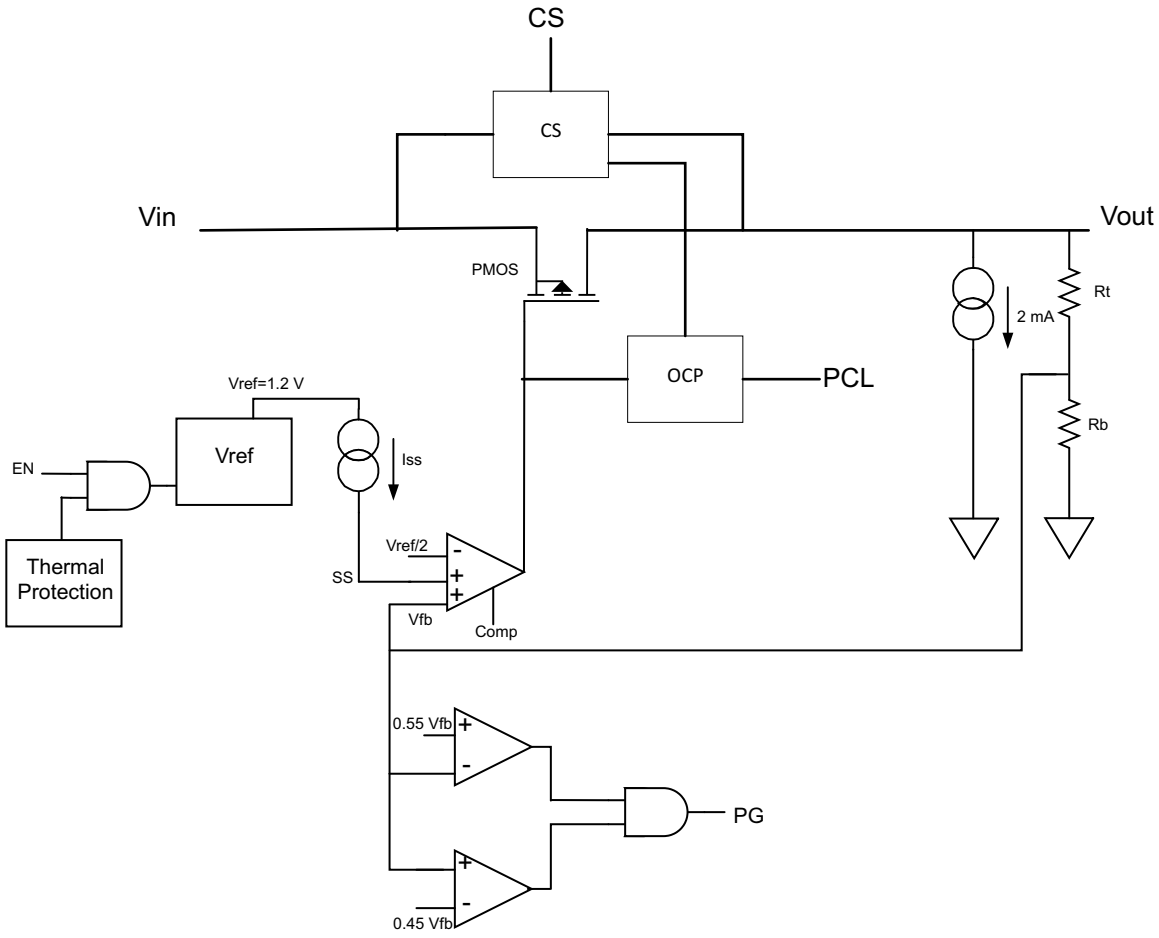


Figure 8. Block Diagram

8.3 Feature Description

8.3.1 Soft Start

Connecting a capacitor from the SS terminal to GND (C_{SS}) slows down the output voltage ramp rate. The soft-start capacitor charges up to 1.2 V.

$$C_{SS} = \frac{t_{SS} \bullet I_{SS}}{V_{FB}}$$

where

- t_{ss} = Soft-start time
- I_{ss} = 2.5 µA
- $V_{FB} = V_{REF} / 2 = 0.605$ V (1)

8.3.2 Power Good (PG)

Power Good terminal (9) is an open-drain connection and can be used to sequence multiple LDOs. Figure 9 shows typical connection for V_{IN} > 3.5 V. The PG terminal will be pulled low until the output voltage reaches 90% of its maximum level. At that point, the PG pin will be pulled up. Since the PG pin is open drain, it can be pulled up to any voltage as long as it does not exceed the absolute max of 7.5 V listed in the *Electrical Characteristics* table.

Feature Description (continued)

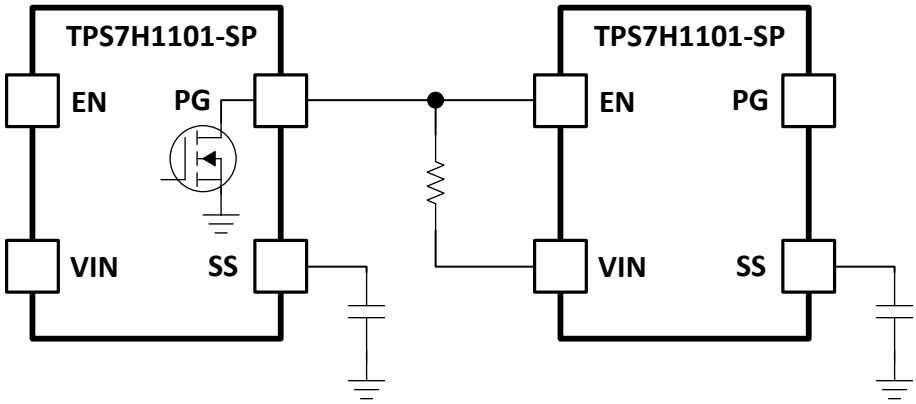


Figure 9. Sequencing LDOs with Power Good

NOTE

For PSpice models, WEBENCH, and mini-POL reference design, see the *Tools & Software* tab.

1. PSpice average model (stability – bode plot)
2. PSpice transient model (switching waveforms)
3. WEBENCH design tool (www.ti.com/product/TPS7H1101-SP/toolssoftware)

8.4 Device Functional Modes

8.4.1 Enable/Disable

For V_{IN} from 1.5 V to 7 V, TPS7H1101-SP can be disabled using the SS terminal. The minimum soft-start pulldown current is 10 μA, with soft start to ground voltage of 400 mV or lower. External voltage applied to the SS terminal must be limited to 1.2-V maximum. Removing the logic-low condition on soft start enables the device allowing the soft-start capacitor to get charged by the internal current source. Alternatively, for V_{IN} > 3.5 V, the device can be disabled by pulling the enable terminal to logic low. In all other cases, the enable terminal should be connected to VIN.

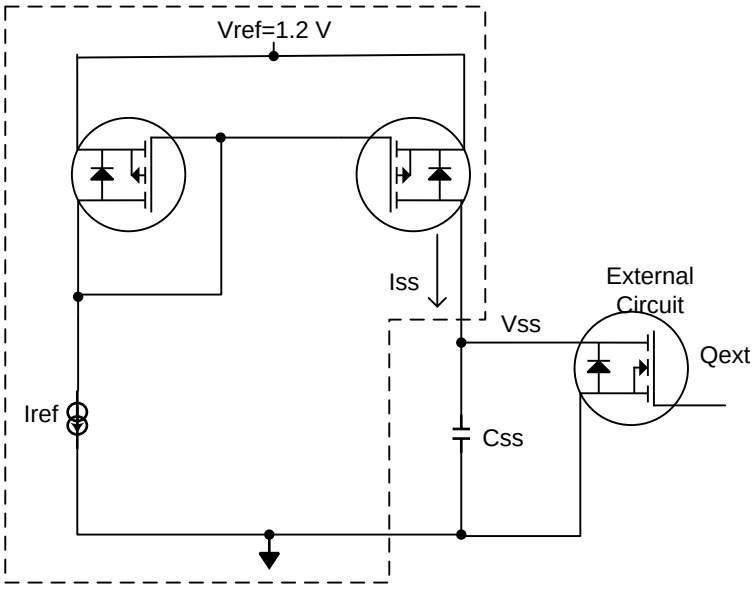


Figure 10. Enable/Disable

Device Functional Modes (continued)

The circuit shown in Figure 10 highlights the SS terminal 1 along with block diagram of internal circuitry. Circuitry in dashed outline is internal to the IC composed of PMOSFET current mirror. The PMOS current mirror sources current from the positive supply and external circuitry composed of Qext is used to sink current from SS terminal 1. As highlighted in the *Electrical Characteristics* table, typical ISS = 2.5 μA and max ISS = 3.5 μA for TPS7H1101-SP. If ISS current is exceeded, such as sinking higher current in excess of max ISS, this disables the LDO. See the *Electrical Characteristics* table for the external sink current from SS terminal necessary to disable the IC. Exceeding maximum external sink current does not damage the device.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H1101-SP LDO linear regulator is targeted to harsh environment applications. This regulator has various features such as low dropout, soft start, output current foldback, high-side current sensing (where sensing voltage at CS pin provides voltage proportional to output current), and current sharing.

9.1.1 Stability

Conventional Bode plots are a standard approach in assessing stability as shown in Figure 11. This approach requires that we have a single feedback path where an AC signal is injected across a resistor (typically 50 Ω) and measurements are taken on either side of the resistor. From this, loop gain and phase plots can be generated. Crossover frequency, f_C, is defined as the frequency where the magnitude of the loop gain is unity and phase margin is evaluated at the crossover frequency f_C.

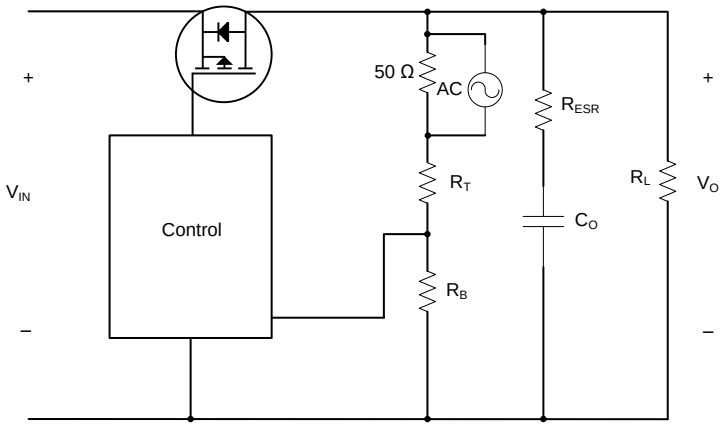


Figure 11. Conventional Bode Plot

However, there are conditions where the feedback loop is not accessible or there may be multiple feedback paths, as with the TPS7H1101-SP. When there are multiple feedback loops the conventional bode plot approach will not be representative of the device's true response. The TPS7H1101-SP uses a conventional feedback loop in addition to an inner fast loop that injects current into the error amplifier, which in turn greatly improves the transient response of the device. The Bode plot method can still be used to understand the behavior of the main loop, but this will show a lower crossover frequency and thus imply a slower transient response than the actual performance of the device. Fortunately, accurate and quantitative stability metrics can still be assessed from output impedance measurements and simulations.

There are multiple ways output impedance can be measured. One approach is to inject a small current at the output of the regulator and compare it to the resulting voltage response. The variation in the phase of the output impedance across frequency can be related to the phase margin through the group delay.

Group delay, T_g, is the rate of change of phase with respect to frequency as shown in Equation 2. Most SPICE simulation packages can plot this parameter and certain frequency analyzers boast software that supports a direct measurement. Using this software, phase margin can be extracted from the group delay plot. The phase margin and crossover frequency reported from these measurements will include the effects of both feedback loops.

$$T_g = \frac{d\phi}{d\omega} \tag{2}$$

Application Information (continued)

The stability of the device can be qualitatively validated by applying a step load to the output and observing the response. The SPICE models for the device can be found in *Tools & Software* on the product page. To simulate impedance measurements, the transient model should be used. For a more detailed explanation of this approach and how to use the model to simulate the output impedance and group delay, please see reference (1).

9.2 Typical Application

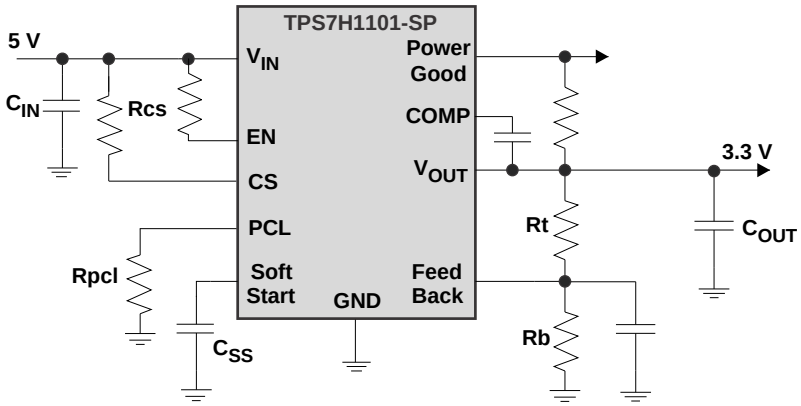


Figure 12. Typical Application Circuit

9.2.1 Design Requirements

Table 1 shows the design parameters.

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage	1.5 V to 7 V
Output voltage	User programmable
Output current	3-A max

9.2.2 Detailed Design Procedure

9.2.2.1 Adjustable Output Voltage (Feedback Circuit)

The output voltage of the TPS7H1101-SP can be set to a user-programmable level between 0.8 V and 6.65 V. Achieve this by using a resistor divider connected between V_{OUT}, FB, and GND terminals. R_{TOP} connected between V_{OUT} and V_{FB}, and R_{BOTTOM} connected between V_{FB} and GND.

Use Equation 3 to determine V_{OUT}.

$$V_{OUT} = \frac{(R_{TOP} + R_{BOTTOM}) \bullet V_{FB}}{R_{BOTTOM}} \quad (3)$$

where

- V_{FB} = 0.605 V

Table 2. Resistor Values for Typical Voltages

V_{OUT}	Standard 1% Resistors		Standard 0.1% Resistors	
	R_{TOP}	R_{BOTTOM}	R_{TOP}	R_{BOTTOM}
0.8 V	10.7 kΩ	33.2 kΩ	10.7 kΩ	33.2 kΩ
1 V	13.7 kΩ	21 kΩ	12.6 kΩ	19.3 kΩ
1.2 V	11.3 kΩ	11.5 kΩ	11.8 kΩ	12 kΩ
1.5 V	15.8 kΩ	10.7 kΩ	18.2 kΩ	12.3 kΩ
1.8 V	23.2 kΩ	11.8 kΩ	32 kΩ	16.2 kΩ
2.5 V	10.7 kΩ	3.4 kΩ	37.9 kΩ	12.1 kΩ
3.3 V	51.1 kΩ	11.5 kΩ	10.2 kΩ	2.29 kΩ
4 V	13.3 kΩ	2.37 kΩ	31.2 kΩ	5.56 kΩ
5 V	11.5 kΩ	1.58 kΩ	16.2 kΩ	2.23 kΩ
5.5 V	17.4 kΩ	2.15 kΩ	89.8 kΩ	11.1 kΩ
6 V	90.9 kΩ	10.2 kΩ	10.7 kΩ	1.2 kΩ
6.5 V	26.7 kΩ	2.74 kΩ	15.2 kΩ	1.56 kΩ
6.6 V	11.3 kΩ	1.15 kΩ	22.1 kΩ	2.23 kΩ
6.7 V	39.2 kΩ	3.92 kΩ	13.8 kΩ	1.37 kΩ

9.2.2.2 PCL

PCL resistor, R_{pcl}, sets the overcurrent limit activation point and can be calculated per Equation 4.

$$R_{pcl} = (CSR \times V_{ref}) / (I_{CL} - 0.0403) \quad (4)$$

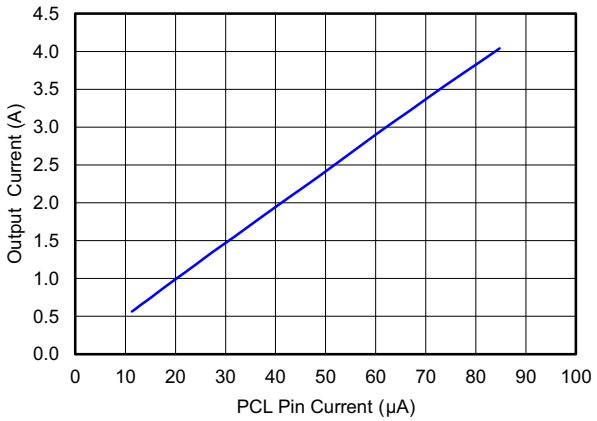
where

- V_{ref} = 0.605 V
- I_{CL} = Programmable current limit (A)
- Current sense ratio (CSR) is the ratio of output load current to I_{CS}. The typical value of the CSR is 47394.

Figure 13 shows the output load current (I_{OUT}) versus PCL terminal current (I_{CL})

A suitable resistor R_{pcl} must be chosen to ensure the CS terminal is within its operating range of 0.3 V to V_{IN}.

The maximum PCL is 3.5 A. The range of resistor that can be used on the PCL terminal to GND is 8.2 kΩ to 160 kΩ.



V_{IN} = 2.3 V V_{OUT} = 1.8 V y = 47394x + 0.0403

Figure 13. I_{OUT} (A) vs I_{PCL} (µA)

9.2.2.3 High-Side Current Sense

Figure 14 shows the cascode NMOS current mirror. V_{cs} must be in the range as specified in the *Electrical Characteristics* table. The following example shows the typical calculation of R_{cs}.

$$I_{CS} = \frac{I_{LOAD} + I_{offset}}{CSR} \quad (5)$$

$$R_{CS} = \frac{V_{IN} - V_{CS}}{I_{CS}} \quad (6)$$

where

- I_{LOAD} is the output load current.
- CSR is the current sense ratio.

When V_{IN} = 2.3 V, select V_{CS} = 2.05 V, I_{LOAD} = 3 A, CSR = 47394, and I_{offset} = 0.1899 A, then I_{CS} = 67.306 µA and R_{CS} = 3.714 kΩ.

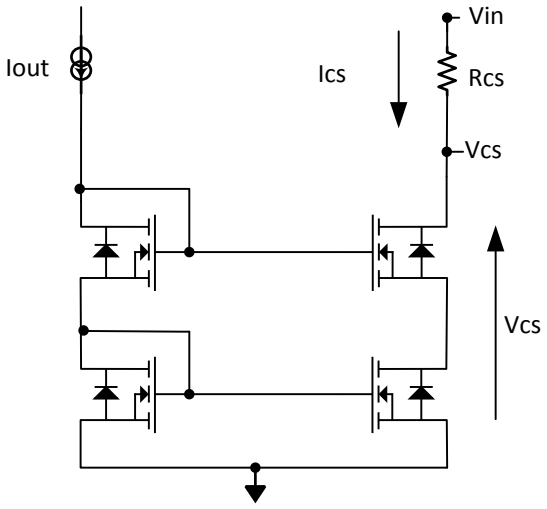
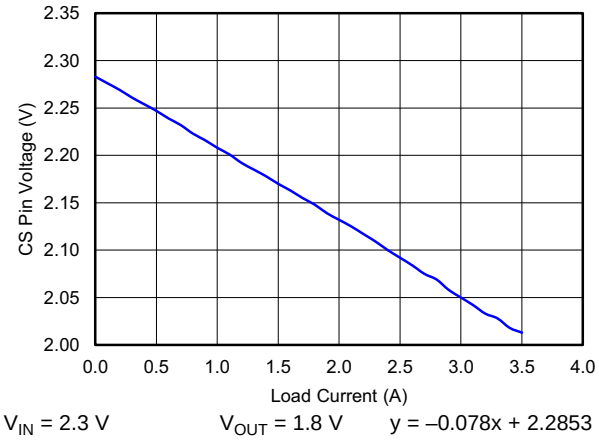


Figure 14. Cascode NMOS Current Mirror

For TPS7H1101-SP, Figure 15 shows the typical curve V_{CS} vs I_{OUT} for V_{IN} = 2.28 V and R_{CS} = 3.65 kΩ. A resistor connected from the CS terminal to V_{IN} indicates voltage proportional to the output current.

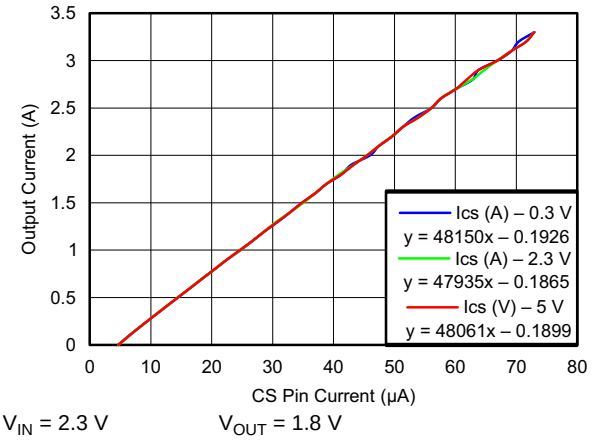
Monitoring current in the CS terminal (I_{CS} vs I_{OUT}) indicates the current sense ratio between the main PMOSFET and the current sense MOSFET as shown in Figure 16.

Figure 17 shows I_{OUT} vs I_{CS} when the voltage on CS terminal is varied from 0.3 V to 7 V.



V_{IN} = 2.3 V V_{OUT} = 1.8 V y = –0.078x + 2.2853

Figure 15. V_{CS} (V) vs I_{OUT} (A)



V_{IN} = 2.3 V V_{OUT} = 1.8 V

Figure 16. I_{OUT} (A) vs I_{CS} (A)

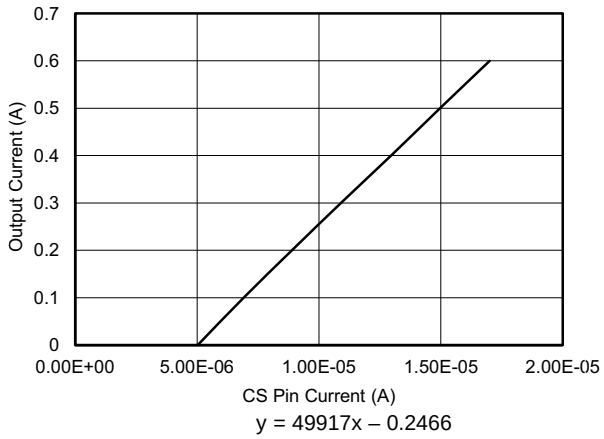


Figure 17. I_{OUT} (A) vs I_{CS} (A)

9.2.2.4 Current Foldback

1. The TPS7H1101-SP has a current foldback feature which can be enabled when the CS terminal is held high. Shorting CS low disables the foldback current limit. If the foldback current limit is disabled, then the LDO will begin regulating again as soon as the current falls below the clamp threshold.
2. With foldback current limit enabled, when current limit trip point is activated,
   a. Output voltage drops low.
   b. Output current folds back to approximately 50% of the current limit trip point.

   This results in minimizing the power loss under fault conditions. Monitoring the voltage at the CS terminal indicates voltage proportional to the output current.

9.2.2.5 Transient Response

Figure 18, Figure 19, and Figure 20 indicate the transient response behavior of the LDO for 50% step load change.

Channel 1: Input Voltage

Channel 2: Output voltage overshoot/undershoot

Channel 3: Step load in current

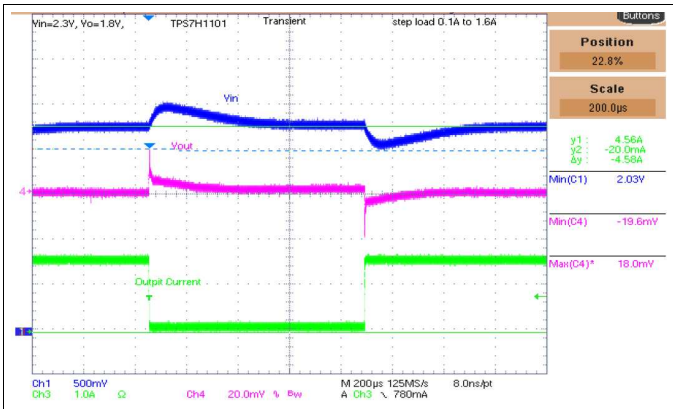


Figure 18. Load Transient Response: Step Load 0.1 A to 1.6 A, V_{IN} = 2.3 V, V_{OUT} = 1.8 V

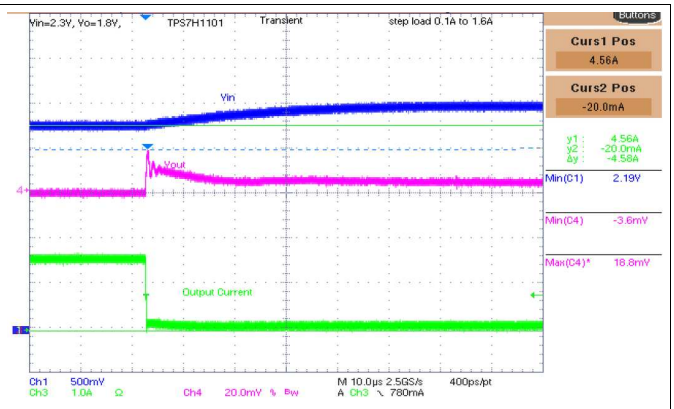


Figure 19. Expanded View Overshoot

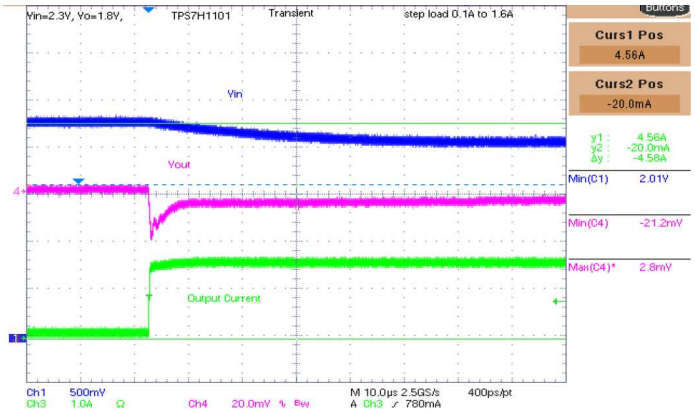


Figure 20. Expanded View Undershoot

9.2.2.6 Current Sharing

For demanding load requirements, multiple LDOs can be paralleled as indicated in Figure 22. In parallel mode, the CS terminal of LDO1 must be connected to the PCL terminal of LDO2 via a series resistor R_{CL}, and CS terminal of LDO2 must be connected to PCL terminal of LDO1 via series resistor R_{CL}. The typical value of R_{CL} in parallel operation is 3.75 kΩ for current limit > 6 A. In parallel configuration, R_{CL} (resistor from PCL to GND) and R_{CS} (resistor from CS terminal to V_{IN}) must be left open (unpopulated). The R_{CL} value must be selected so that the operating condition of the CS terminal is maintained, as specified in the *Electrical Characteristics* table. The current from PCL through RCL of LDO1 is determined by the output load current of LDO2 divided by the CSR. Hence, the voltage at CS terminal of the LDO1 is 0.605 V – ((output load current of LDO2 + 0.2458) / CSR × R_{CL}).

Alternately, it can also provide twice the output current to meet system needs. When using two LDOs in parallel operation for higher output load current, use POL TPS50601-SP as an input source.

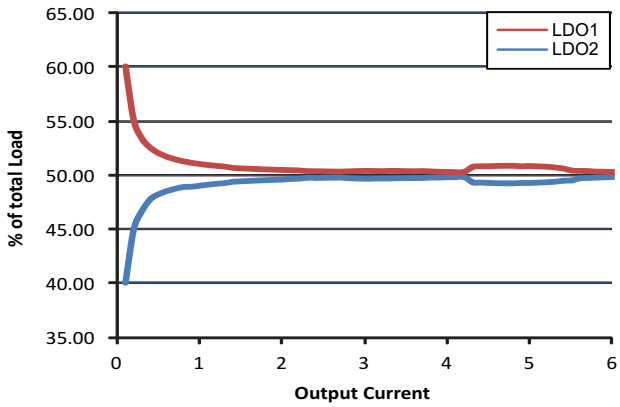


Figure 21. LDO Current Share

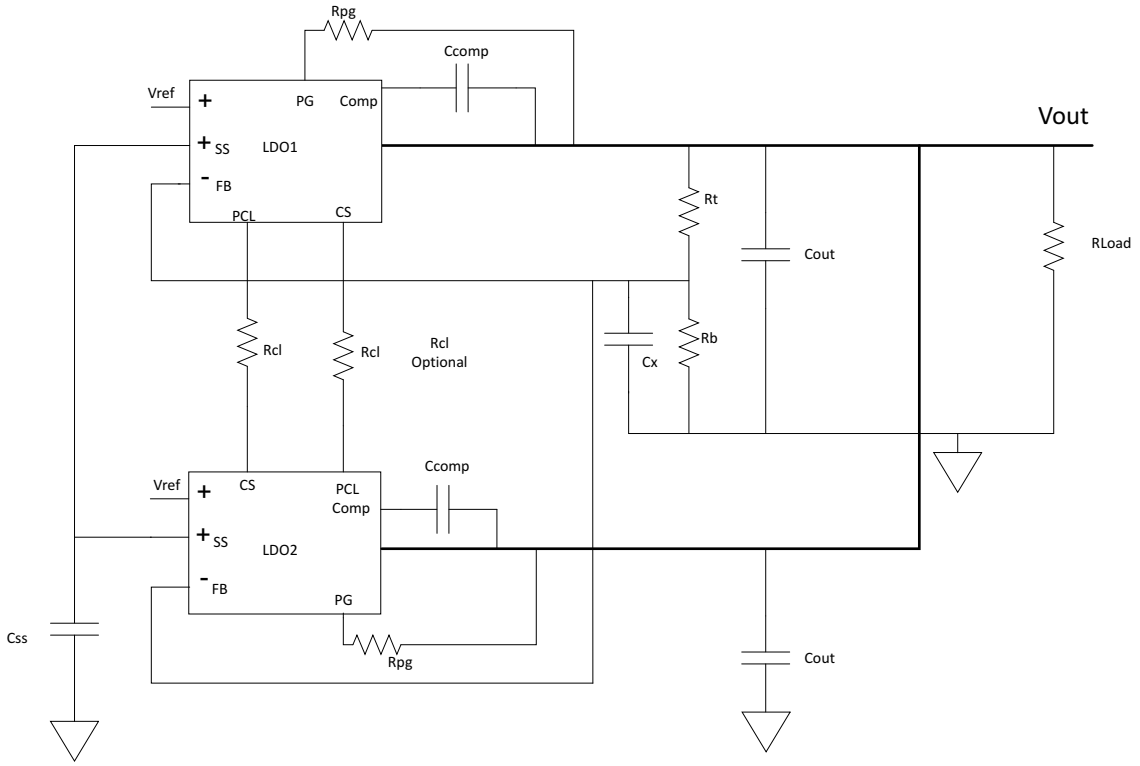


Figure 22. Block Diagram (Parallel Operation)

9.2.2.7 Compensation

Figure 23 shows a generic block diagram for TPS7H1101-SP LDO with external compensation components. LDO incorporates nested loops, thus providing the high gain necessary to meet design performance.

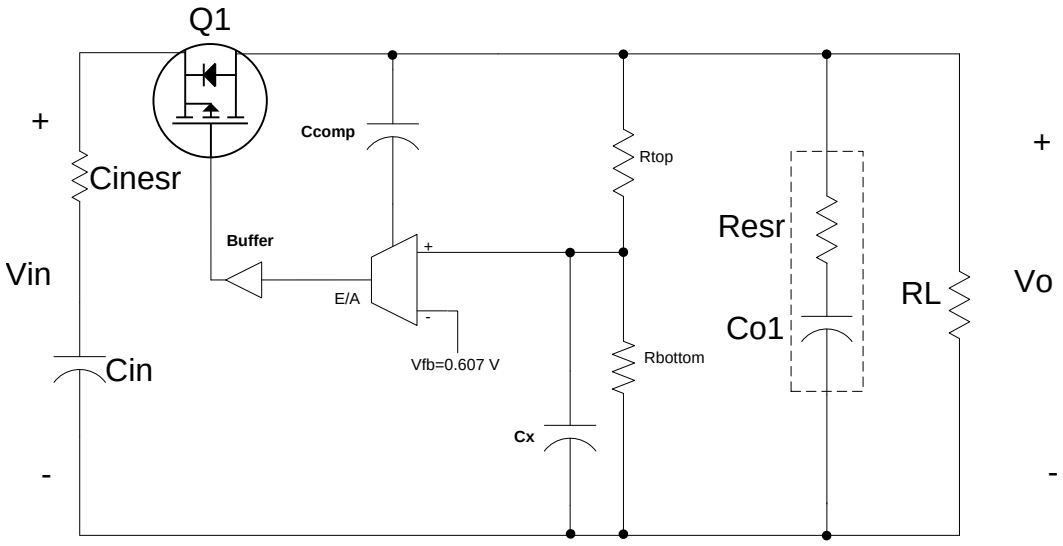


Figure 23. TPS7H1101-SP Compensation

Resistor divider composed of R_{top} and R_{bottom} determine the output voltage set points as indicated by Equation 3.

Output capacitor C_{OUT} introduces a pole and a zero as shown in the following.

$$F_{p\_co} = \frac{1}{2 \bullet \pi \bullet C_o \bullet R_L} \quad (7)$$

$$F_{z\_co} = \frac{1}{2 \bullet \pi \bullet C_o \bullet C_{esr}} \quad (8)$$

The TPS7H1101-SP was designed so that the ESR of the output capacitor will not have a strong influence on the response of the LDO. However, an optional capacitor, C_x, can be added in parallel with the bottom feedback resistor to introduce a pole to cancel F_{z_co}. Equation 9 shows how to calculate the location of the pole introduced by C_x. To cancel the zero directly, F_p should be equal to F_{z_co}.

$$F_p = \frac{1}{2 \bullet \pi \bullet C_x \bullet R_{bottom}} \quad (9)$$

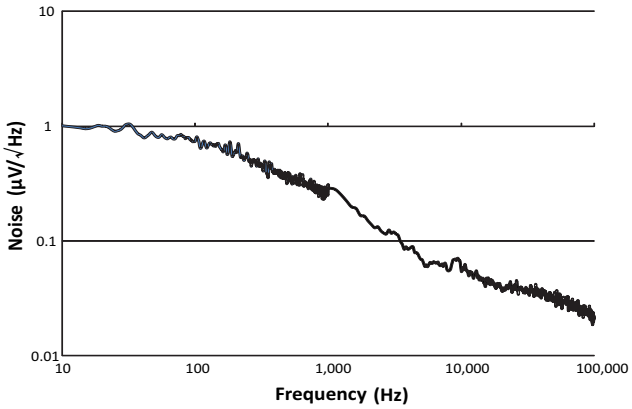
C_x is calculated to be 1000 pF for C_o = 220 µF, C_{esr} = 45 mΩ, and R_{bottom} = 10 kΩ.

Internal compensation in the LDO cancels the output capacitor pole introduced by C_{OUT} and R_L.

C_{comp} introduces a dominant pole at low frequency. TI recommends that a C_{comp} value of 10 nF.

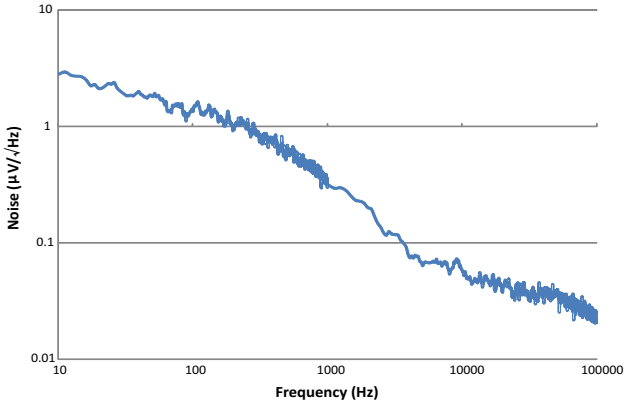
9.2.2.8 Output Noise

Output noise is measured using an HP3495A. Figure 24, Figure 25, , and show noise of the TPS7H1101-SP in µV/√Hz vs frequency.



V_{IN} = 2 V V_{OUT} = 1.8 V at 3 A
C_{IN} = 220 µF C_{LOAD} = 220 µF

Figure 24. RMS Noise (10 Hz to 100 kHz) = 20.33 µVrms



V_{IN} = 7 V V_{OUT} = 6.7 V at I_{LOAD} = 3 A
C_{IN} = 220 µF C_{LOAD} = 220 µF

Figure 25. RMS Noise (10 Hz to 100 kHz) = 31.68 µVrms

9.2.2.9 Capacitors

TPS7H1101-SP requires the use of a combination of tantalum and ceramic capacitors to achieve good volume to capacitance ratio. Table 3 highlights some of the capacitors used in the device. TI recommends to follow proper derating guidelines as recommended by the capacitor manufacturer based upon output voltage and operating temperature.

Note that polymer-based tantalum capacitors must be derated to at least 60% of rated voltage, whereas manganese oxide (MnO_2) based tantalum capacitors should be derated to 33% of rated voltage depending upon the operating temperature.

TI recommends to use a tantalum capacitor along with a 0.1-µF ceramic capacitor. The device is stable for input and output tantalum capacitor values of 10 to 220 µF with the ESR range of 10 mΩ to 2 Ω. However, the dynamic performance of the device varies based on load conditions and the capacitor values used.

TI recommends a minimum output capacitor of 22 µF with ESR of 1 Ω or less to prevent oscillations. X7R dielectrics are preferred. See Table 3 for various capacitor recommendations.

Table 3. TPS7H1101-SP Capacitors

CAPACITOR PART NUMBER	CAPACITOR DETAILS (CAPACITOR, VOLTAGE, ESR)	TYPE	VENDOR
T493X107K016CH612A(1)	100 µF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
T493X226M025AH6x20(1)	22 µF, 25 V, 35 mΩ	Tantalum - MnO2	Kemet
T525D476M016ATE035(1)	47 µF, 10 V, 35 mΩ	Tantalum - Polymer	Kemet
T540D476M016AH6520(1)	47 µF, 16 V, 20 mΩ	Tantalum - Polymer	Kemet
T525D107M010ATE025(1)	100 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T541X337M010AH6720(1)	330 µF, 10 V, 6 mΩ	Tantalum - Polymer	Kemet
T525D227M010ATE025(1)	220 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T495X107K016ATE100(1)	100 µF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
CWR29FK227JTHC(1)	220 µF, 10 V, 180 mΩ	Tantalum - MnO2	AVX
THJE107K016AJH	100 µF, 16 V, 58 mΩ	Tantalum	AVX
THJE227K010AJH	220 µF, 10 V, 40 mΩ	Tantalum	AVX
SMX33C336KAN360	33 µF, 25 V	Stacked ceramic	AVX
SR2225X7R335K1P5#M123	3.3 µF, 25 V, 10 mΩ	Ceramic	Presidio Components Inc

(1) Operating temperature is –55°C to 125°C.

9.2.3 Application Curves

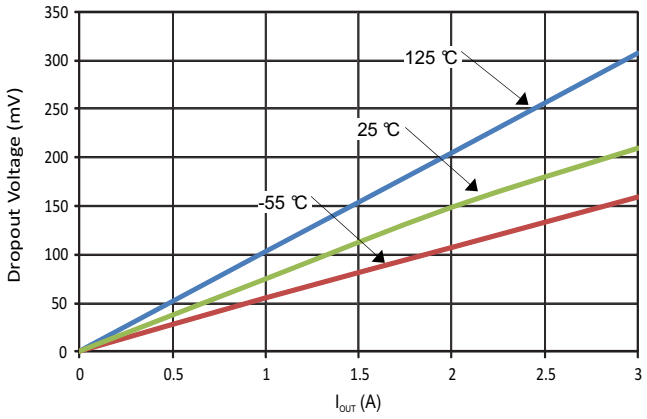


Figure 26. VDO vs I_{OUT}

10 Power Supply Recommendations

This device is designed to operate with an input voltage supply up to 7 V. The minimum input voltage should provide adequate headroom greater than the dropout voltage for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

11 Layout

11.1 Layout Guidelines

- For best performance, all traces should be as short as possible, and no longer than 5 cm.
- Use wide traces for IN, Out and GND to minimize the parasitic electrical effects.
- Place the output capacitors (COUT) as close as possible to the OUT pin of the device.

11.2 Layout Example

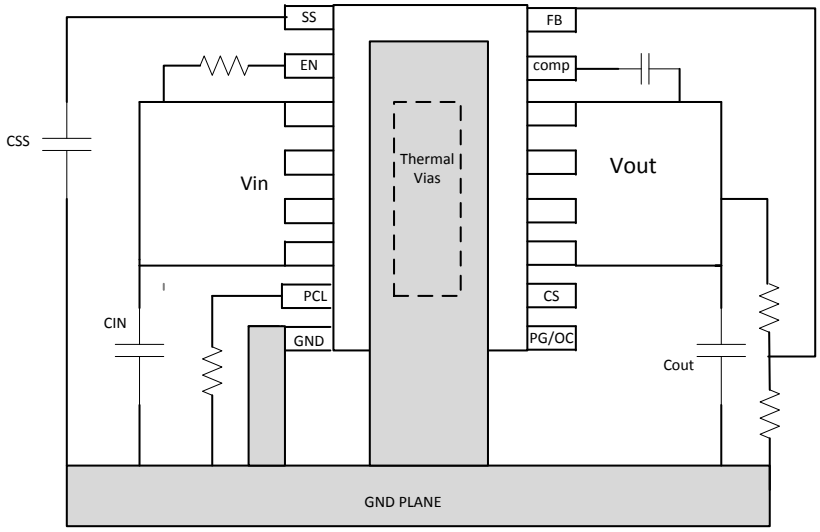


Figure 27. PCB Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.1.2 器件命名规则

KGD 已知的合格芯片

RHA 太空系统的耐辐射保障

5962R13202 与 TPS50601-SP 相同的器件，以标准微电路图 (SMD) 显示

TPS7H1101-SP 与 5962R10221 相同的器件，以 TI 封装图显示

12.2 文档支持

12.2.1 相关文档

(1) *固定稳压器的稳定性评估 - Tom Boehler、Paul Ho，AEi 系统*

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-1320201VXC	NRND	Production	CFP (HKR) | 16	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	5962-1320201VXC TPS7H1101-SP
5962R1320201VXC	NRND	Production	CFP (HKR) | 16	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	5962R1320201VXC TPS7H1101-RHA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

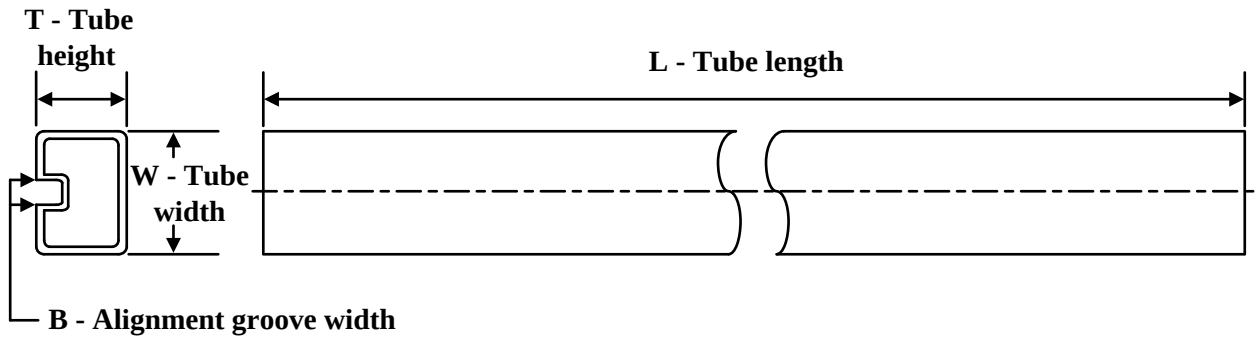
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

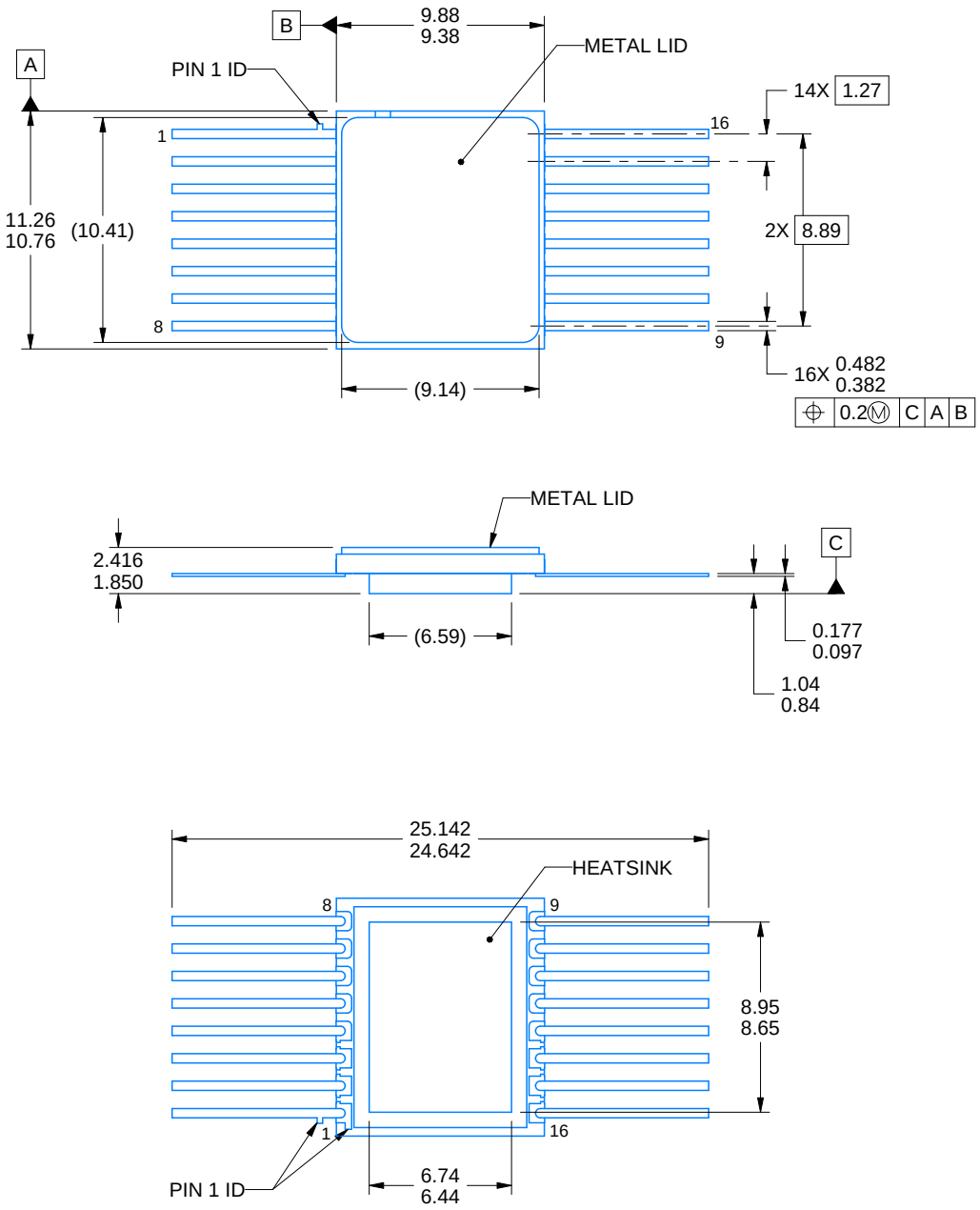
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1320201VXC	HKR	CFP	16	25	506.98	26.16	6220	NA
5962R1320201VXC	HKR	CFP	16	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

HKR0016A

CFP - 2.416 mm max height

CERAMIC DUAL FLATPACK



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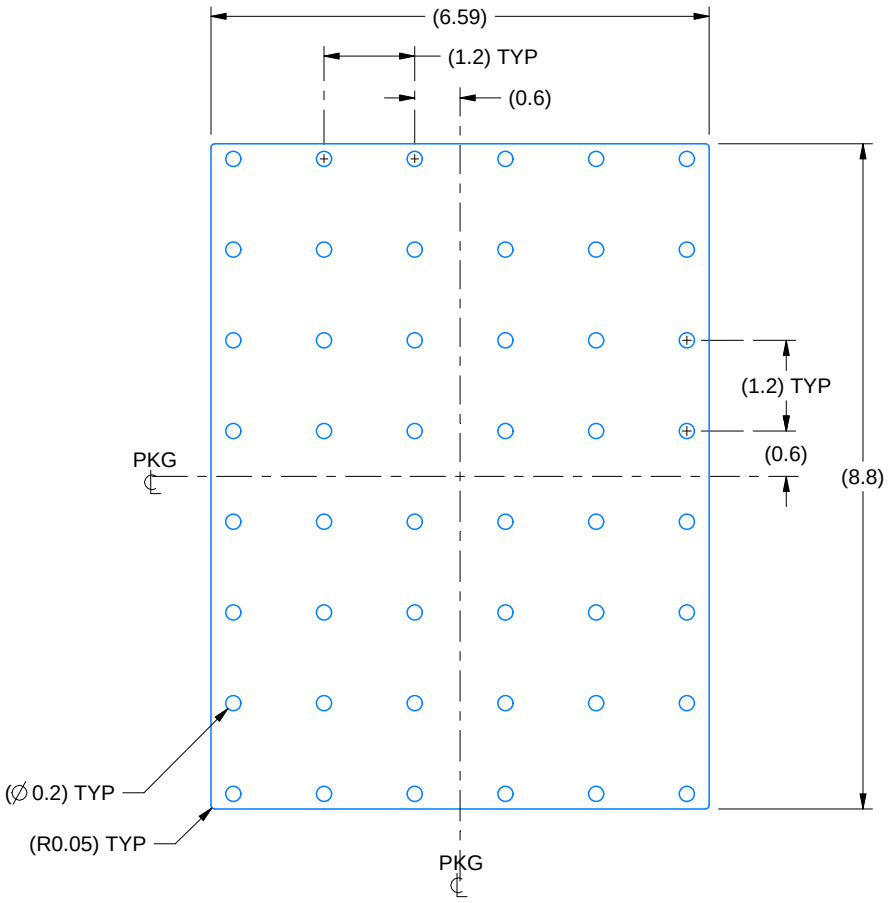
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid is connected to Heatsink.
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

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最后更新日期：2025 年 10 月