TPS7C13 300mA, Small-Size, High-PSRR, Low-Dropout Adjustable Regulator

1 Features

- High PSRR: 55dB (1MHz)
- V_{IN} range: 1.4V to 5.5V
- Adjustable output voltage range: 0.6V to 3.3V
- Output voltage accuracy: 2.5%
- Low dropout voltage:
  - 255mV at 300mA ($3.3V_{OUT}$)
- Foldback current limit with thermal shutdown
- Active output pulldown resistor
- Package:
  - 5-pin SOT-23 (DBV)

2 Applications

- Smartphones
- Tablets
- Gaming consoles
- Notebooks
- Streaming media players
- Set-top boxes
- Camera modules

3 Description

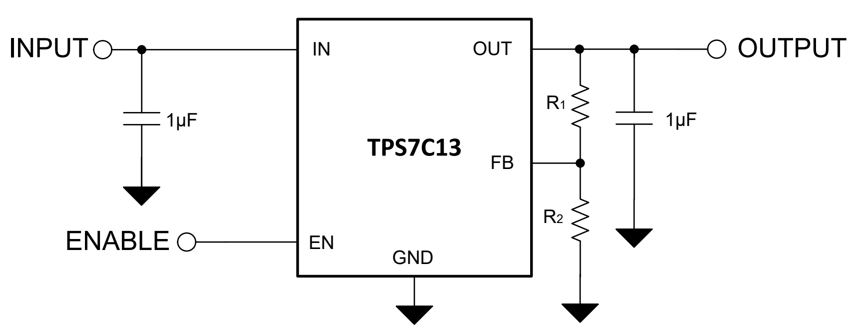
The TPS7C13 is a small, adjustable, low-dropout (LDO) linear regulator that sources 300mA of output current. This LDO provides a voltage source with high PSRR and load and line transient performance that meets the requirements of a variety of circuits. The TPS7C13 has a 1.4V to 5.5V input voltage range and a 0.6V to 3.3V output voltage range. This flexibility allows the TPS7C13 to be used in multiple applications.

The TPS7C13 features an internal soft-start circuit to avoid excessive inrush current, thus minimizing the input voltage drop during start-up. An active pulldown circuit quickly discharges the output when the LDO is disabled and provides a known start-up state. The EN input allows an external logic signal to enable or disable the regulated output. The LDO is stable with small ceramic capacitors, allowing for a small overall design size. The operating junction temperature range is from −40°C to +125°C. This LDO is available in standard SOT-23 (DBV) package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7C13	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

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4 Pin Configuration and Functions

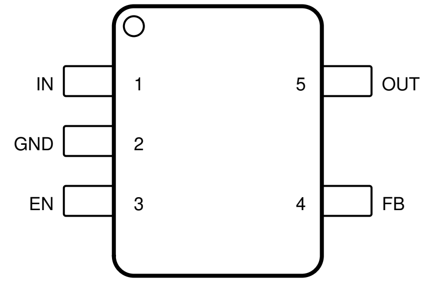


Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	SOT-23		
EN	3	I	Enable input. A low voltage (< $V_{EN(LOW)}$) on this pin turns the regulator off and discharges the output pin to GND. A high voltage (> $V_{EN(HI)}$) on this pin enables the regulator output.
FB	4	I	Feedback pin. Input to the control-loop error amplifier. This pin sets the device output voltage using external resistors.
GND	2	G	Ground pin.
IN	1	I	Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground. See the *Recommended Operating Conditions* table. Place the input capacitor as close to the device IN and GND pins as possible.
OUT	5	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the device OUT and GND pins as possible. An internal pulldown resistor prevents a charge from remaining on V_{OUT} when the regulator is in shutdown mode (V_{EN}< $V_{EN(LOW)}$).

(1) I = input, O = output, I/O = input or output, and G = ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1) (3)]

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6.5	V
	Output, V_{OUT}	–0.3	6.0 or V_{IN} + 0.3 [(2)]	
	Feedback, V_{FB}	–0.3	6.0	
	Enable, V_{EN}	–0.3	6.5	
Current	Maximum output, I_{OUT} [(4)]	Internally limited		A
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The maximum value of V_{OUT} is the lesser of 6.0V or (V_{IN} + 0.3V).
(3) All voltages are with respect to the GND pin.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.4		5.5	V
V_{EN}	Enable input voltage	0		5.5	V
V_{OUT}	Nominal output voltage range	0.6		3.3	V
I_{OUT}	Output current	0		300	mA
C_{IN}	Input capacitor[(2)]		1		µF
C_{OUT}	Output capacitance[(3)]	0.47		40	µF
ESR	Output capacitor effective series resistance			100	mΩ
C_{FF}	Feed-forward capacitor (optional)[(4)]	0	100		pF
$I_{FB\_DIVIDER}$	Feedback divider current[(5)]	2			µA
T_J	Operating junction temperature	–40		125	°C

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47µF minimum is recommended to counteract the effect of source resistance and inductance, which in some cases causes symptoms of system-level instability such as ringing or oscillation, especially in the presence of load transients. A larger input capacitance can be needed depending on the characteristics of the input voltage source.
(3) Effective output capacitance of 0.47µF minimum and 40µF maximum is required for stability. The effective output capacitance must account for tolerance, temperature, voltage, and any other factors that affect the value, and often is 50% smaller than the specified value of the capacitor.
(4) See the *Feed-Forward Capacitor (C_{FF})* section for details.
(5) Feedback divider current = V_{OUT} / (R_1 + R_2).

5.4 Thermal Information

THERMAL METRIC[(1)]		TPS7C13	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	242.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	140.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	109.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	76.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	108.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

specifications apply for T_J = 25℃, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.4V, whichever is greater, V_{EN} = V_{IN}, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1µF (unless otherwise noted); all typical values are at T_J = 25℃

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage			0.585	0.6	0.615	V
ΔV_{OUT}	Output voltage tolerance[3]	Tested at V_{OUT} = 0.6V		–2.5		2.5	%
		T_J = –40°C to 125℃, Tested at V_{OUT} = 0.6V		–3.75		3.75	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 5.5V			0.01	0.1	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	I_{OUT} = 1mA to 300mA			2	40	µV/mA
I_{FB}	Feedback pin input current	T_J = –40°C to 125°C			10	100	nA
I_{GND}	Quiescent ground current	V_{EN} = V_{IN} = 5.5V, I_{OUT} = 0mA, T_J = –40°C to 125°C			80	130	µA
I_{SHDN}	Shutdown ground current	V_{EN} < $V_{EN(LOW)}$, V_{IN} = 5.5V, T_J = –40°C to 125°C			0.01	2	µA
V_{DO}	Dropout voltage	I_{OUT} = 300mA, V_{IN} = $V_{OUT(NOM)}$ [2]	0.8V ≤ V_{OUT} < 1.8V[1]			675	mV
			1.8V ≤ V_{OUT} < 2.5V			330	
			2.5V ≤ V_{OUT} < 2.8V			260	
			2.8V ≤ V_{OUT} ≤ 3.3V			255	
		I_{OUT} = 300mA, V_{IN} = $V_{OUT(NOM)}$, T_J = –40°C to 125°C [2]	0.8V ≤ V_{OUT} < 1.8V[1]			805	
			1.8V ≤ V_{OUT} < 2.5V			435	
			2.5V ≤ V_{OUT} < 2.8V			340	
			2.8V ≤ V_{OUT} ≤ 3.3V			330	
I_{CL}	Output current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$, T_J = –40°C to 125°C		325		720	mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0V			65		mA
PSRR	Power-supply rejection ratio	I_{OUT} = 50mA, V_{IN} = V_{OUT} + 1.0V	f = 1kHz		60		dB
			f = 100kHz		56		
			f = 1MHz		55		
V_N	Output noise voltage	BW = 10Hz to 100kHz, Vout = 1.2V, I_{OUT} = 50mA			90		$µV_{RMS}$
$R_{PULLDOWN}$	Output automatic discharge pulldown resistance	V_{EN} < $V_{EN(LOW)}$ (output disabled), V_{IN} = 3.3V			135		Ω
T_{SD}	Thermal shutdown	T_J rising			160		°C
		T_J falling			140		
$V_{EN(LOW)}$	Low input threshold	V_{EN} falling until the output is disabled. T_J = –40°C to 125°C				0.3	V
$V_{EN(HI)}$	High input threshold	V_{EN} rising until the output is enabled. T_J = –40°C to 125°C		0.9			V
I_{EN}	EN input leakage current	V_{EN} = 5.5V and V_{IN} = 5.5V			0.01	1	µA

(1) For V_{OUT} < 1.4V, dropout is tested with V_{IN} = 1.4V.
(2) V_{FB} = 95% x $V_{FB(NOM)}$.
(3) Tolerance of external resistors not included in this specification.

5.6 Switching Characteristics

specifications apply for T_J = 25℃, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.4V, whichever is greater, V_{EN} = V_{IN}, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1µF (unless otherwise noted); all typical values are at T_J = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time (V_{EN})	From V_{EN} > $V_{EN(HI)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$, V_{IN} rise time = 1V/us		320		µs

5.7 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V, I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1μF (unless otherwise noted)

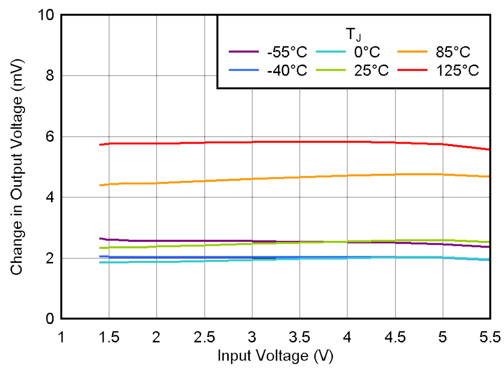


Figure 5-1. Line Regulation vs V_{IN}

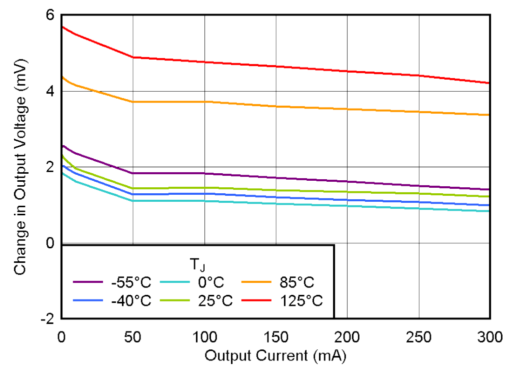


Figure 5-2. Load Regulation vs I_{OUT}

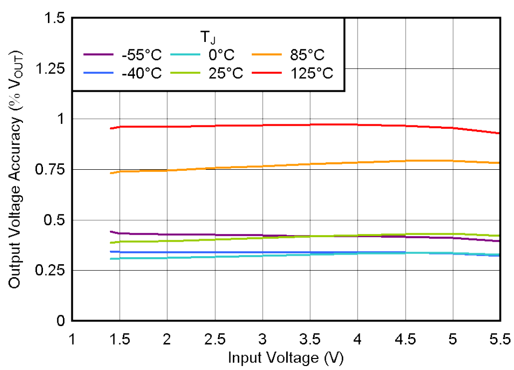


Figure 5-3. Output Voltage Accuracy vs V_{IN}

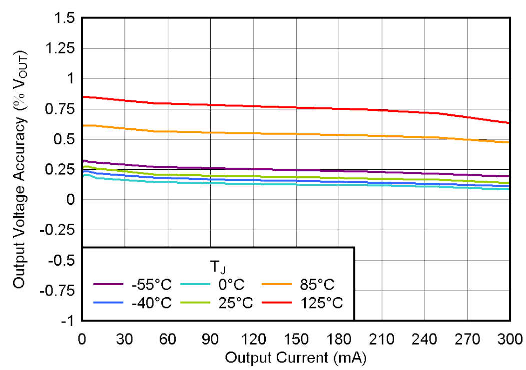
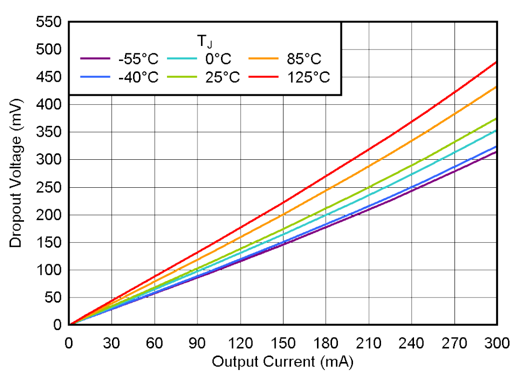


Figure 5-4. Output Voltage Accuracy vs I_{OUT}



V_{OUT} = 0.6V

Figure 5-5. Dropout Voltage vs I_{OUT}

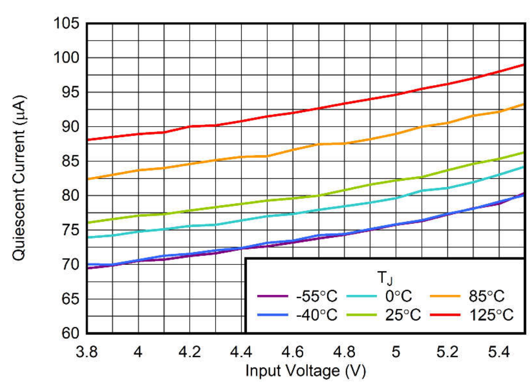


Figure 5-6. Quiescent Current vs V_{IN}

5.7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V, I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)

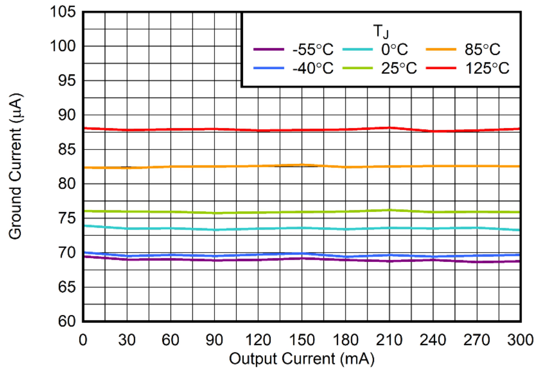
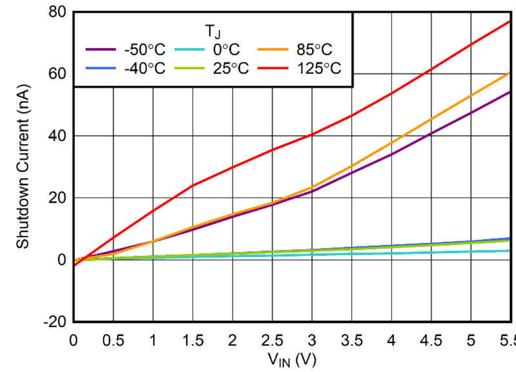


Figure 5-7. Ground Current vs I_{OUT}



V_{EN} = 0V

Figure 5-8. Shutdown Current vs V_{IN}

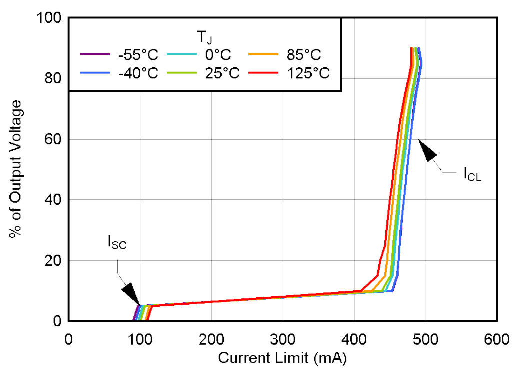


Figure 5-9. Current Limit

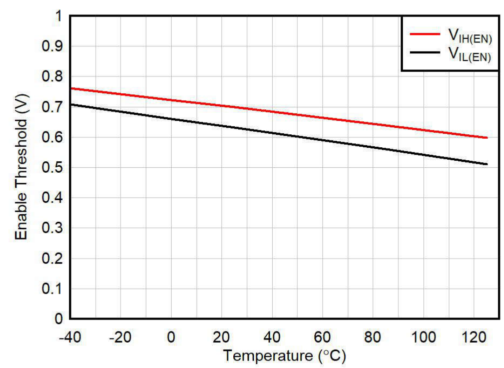
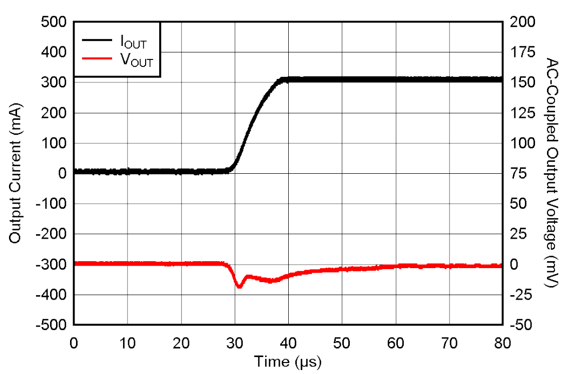
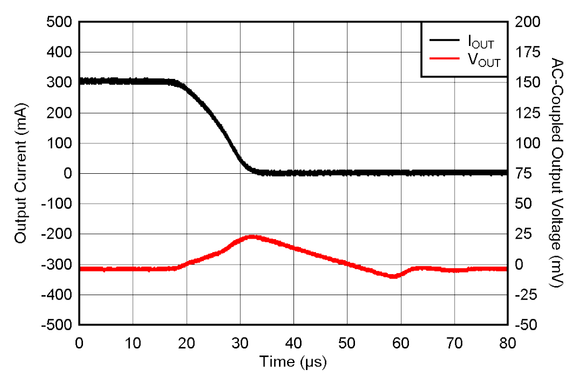


Figure 5-10. Enable Logic Threshold vs Temperature



V_{IN} = $V_{OUT(nom)}$ + 1.0V, I_{OUT} = 0mA to 300mA, T_{RISING} = 10µs

Figure 5-11. Load Transient

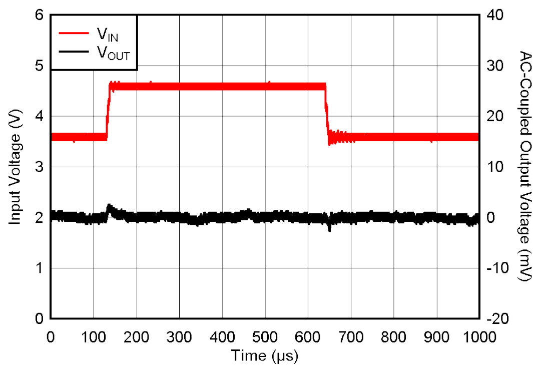


V_{IN} = $V_{OUT(nom)}$ + 1.0V, I_{OUT} = 300mA to 0mA, $T_{FALLING}$ = 10µs

Figure 5-12. Load Transient

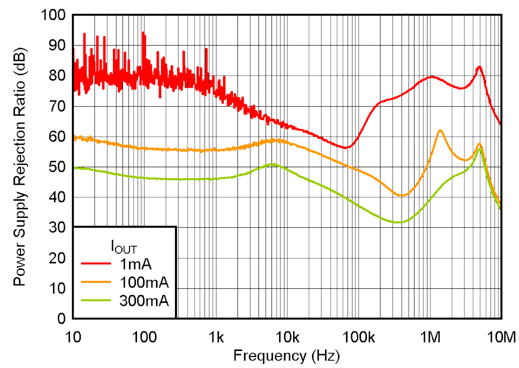
5.7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V, I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



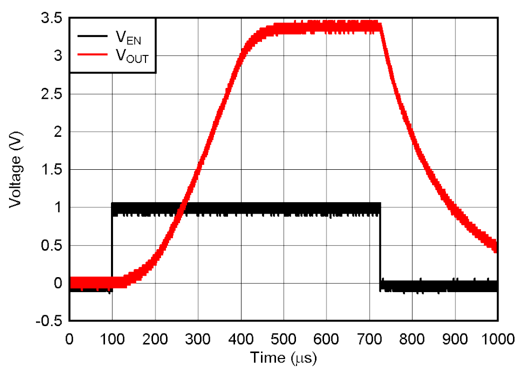
V_{IN} = V_{OUT} + 0.3V to V_{OUT} +1.3V

Figure 5-13. Line Transient



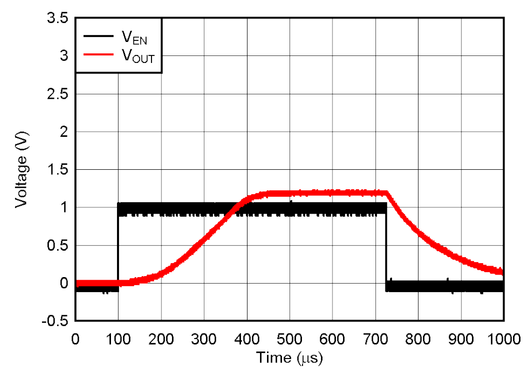
V_{IN} = $V_{OUT(nom)}$ + 1.0V

Figure 5-14. PSRR vs Frequency



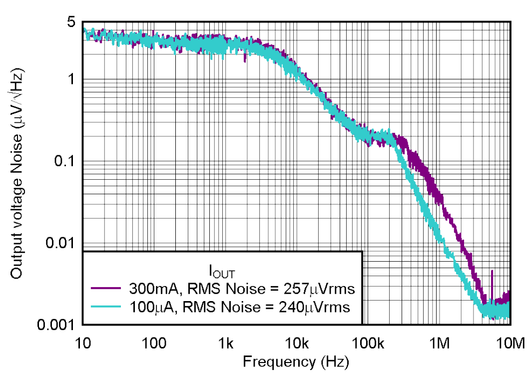
V_{OUT} = 3.3V

Figure 5-15. Start-Up



V_{OUT} = 1.2V

Figure 5-16. Start-Up



V_{IN} = 4.3V, $V_{OUT(nom)}$ = 3.3V

Figure 5-17. Noise

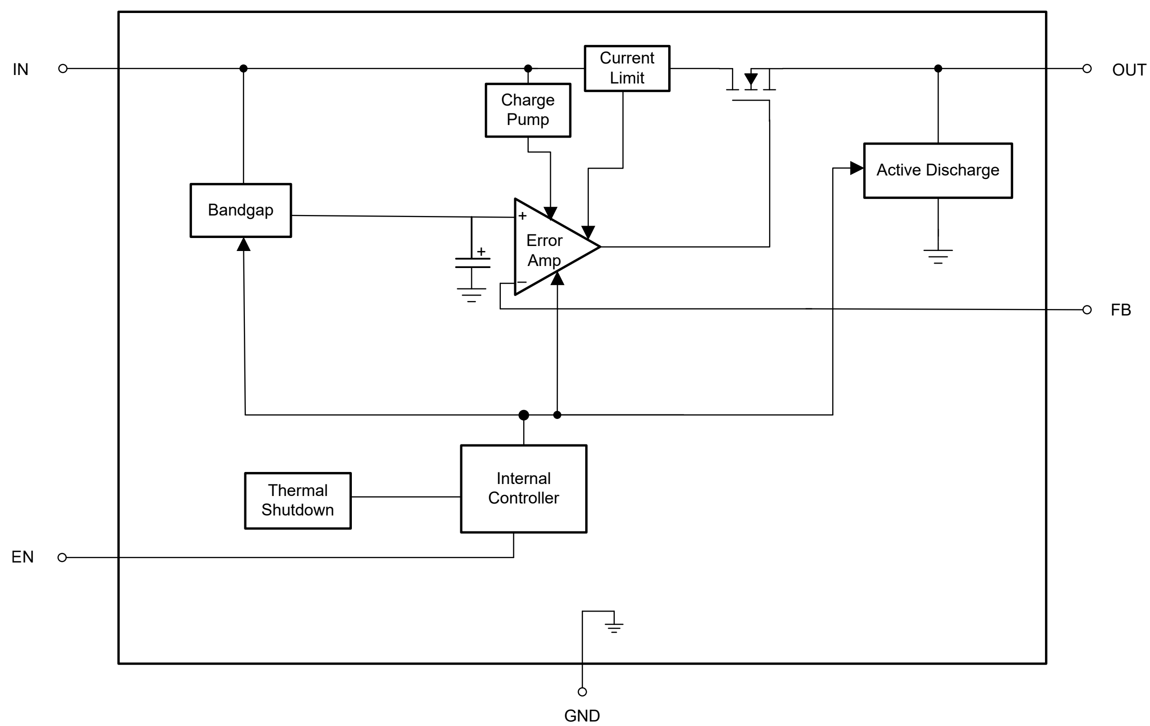
6 Detailed Description

6.1 Overview

The TPS7C13 provides high PSRR and good transient response in a small, 300mA LDO.

This LDO is designed to operate with a single 1µF input capacitor and a single 1µF ceramic output capacitor.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Dropout Voltage

Dropout voltage (V_{DO}) is defined as $V_{IN} – V_{OUT}$ at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.2 Active Discharge

The regulator has an internal MOSFET that connects a pulldown resistor between the output and ground when the device is disabled. This connection actively discharges the output voltage. The active discharge circuit is activated by the enable pin or by the voltage on IN falling below the undervoltage lockout (UVLO) threshold.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply collapses. Reverse current flow from the output to the input potentially causes damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

6.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the device supplies a typical current termed the *short-circuit current limit (I_{SC})*. I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-1 shows a diagram of the foldback current limit.

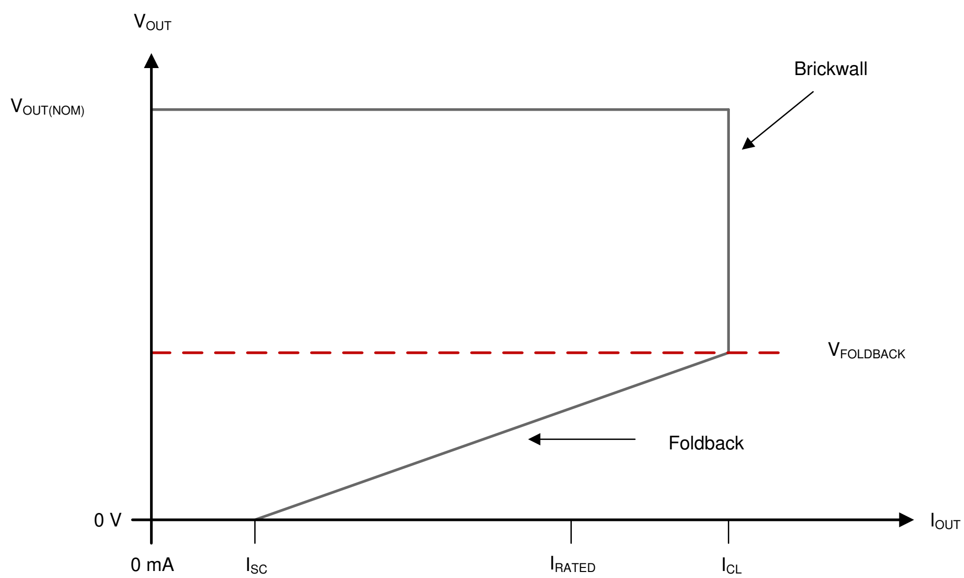


Figure 6-1. Foldback Current Limit

6.3.4 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In this mode, the transient performance of the device becomes significantly degraded. During this mode, the pass transistor is driven fully on. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven fully on. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start-up. Dropout occurs when $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the regulator exits dropout, the input voltage returns to a value $\geq V_{OUT(NOM)} + V_{DO}$. During this time, the output voltage potentially overshoots for a short period of time. $V_{OUT(NOM)}$ is the nominal output voltage and V_{DO} is the dropout voltage. During dropout exit, the device pulls the pass transistor back from being driven fully on.

6.4.3 Disabled

Shutdown the device output by forcing the enable pin voltage to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor turns off and internal circuits shut down. The output voltage is also actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. According to the following equation, V_{OUT} is set using the feedback divider resistors, R_1 and R_2.

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100 times the maximum FB pin current. This current is listed in the *Electrical Characteristics* table. As given in the following equation, this setting provides the maximum feedback divider series resistance.

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

7.1.2 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. For typical operation of the TPS7C13, connect a 1µF capacitor to the input. Use a higher value capacitor if large, fast rise-time, load, or line transients are anticipated. Additionally, use a higher-value capacitor if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability. Verify the minimum derated output capacitance is equal to or greater than 0.47µF. When the output voltage is ramping up, the inrush current depends on the size of the output capacitance. During start-up, the output current is potentially as high as the current limit value for larger output capacitors.

7.1.4 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, connect an optional feed-forward capacitor (C_{FF}) from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. Using a higher-capacitance C_{FF} is permissible but start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z. C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. The following equations calculate C_{FF} zero and pole frequencies.

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

To avoid start-up time increases from C_{FF}, limit the product $C_{FF} \times R_1 < 50\mu F \times \Omega$.

For an output voltage of 0.6V with the FB pin tied to the OUT pin, no C_{FF} is used.

7.2 Typical Application

7.2.1 Application

Figure 7-1 shows a typical application circuit for the TPS7C13.

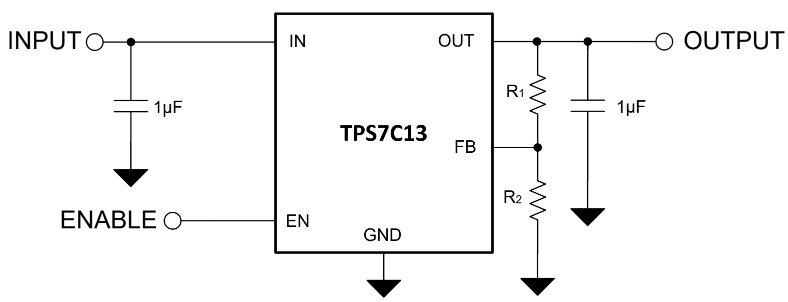


Figure 7-1. TPS7C13 Typical Application

7.2.2 Design Requirements

Table 7-1 summarizes the design requirements for Figure 7-1.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input voltage range	4.0V± 5%
Output voltage	3.3V
Output current	200mA
Maximum ambient temperature	125°C

7.2.3 Detailed Design Procedure

For this design example, a 3.3V output is set using external divider resistors R_1 and R_2. A nominal 4.0V input supply is assumed. Use a minimum 1µF input capacitor to minimize the effect of resistance and inductance between the 4.0V source and LDO input. Use a minimum 0.47µF output capacitance for stability and good load transient response. The dropout voltage (V_{DO}) is less than 255mV maximum at a 3.3V output voltage and 300mA output current. Thus, there are no dropout issues with a minimum 3.8V input voltage and a maximum 200mA output current. Minimum input voltage is calculated as 4.0V − 5%.

7.2.3.1 Choose Feedback Resistors

For this design example, V_{OUT} is set to 3.3V. The following equations set the feedback divider resistors for the desired output voltage:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (6)$$

$$R_1 + R_2 \le V_{OUT} / (I_{FB} \times 100) \quad (7)$$

For improved output accuracy, use Equation 7 and I_{FB} = 100nA as listed in the *Electrical Characteristics* table to calculate the upper limit for series feedback resistance ($R_1 + R_2 \le 330k\Omega$).

The control-loop error amplifier drives the FB pin to the same voltage as the internal reference (V_{FB} = 0.6V, as listed in the *Electrical Characteristics* table). Use Equation 6 to determine the ratio of R_1 / R_2 = 4.5. Use this ratio and solve Equation 7 for R_1. Now calculate the upper limit for $R_1 \le 270k\Omega$. Select a standard value resistor for R_1 = 267kΩ.

Reference Equation 6 and solve for R_2:

$$R_2 = R_1 / [(V_{OUT} / V_{FB}) - 1] \quad (8)$$

From Equation 8, R_2 = 59kΩ is determined. Select a standard value resistor for R_2 = 59kΩ. V_{OUT} = 3.3V (as determined by Equation 6). Verify that the feedback divider current is greater than the minimum value in the *Recommended Operating Conditions* table.

The following equation calculates the feedback divider current.

$$I_{FB\_Divider} = V_{OUT} / (R_1 + R_2) \quad (9)$$

7.2.4 Application Curves

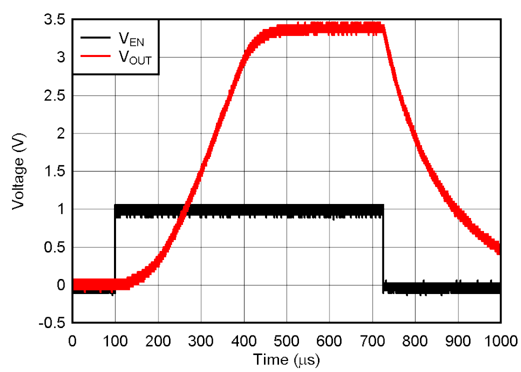


Figure 7-2. Start-Up

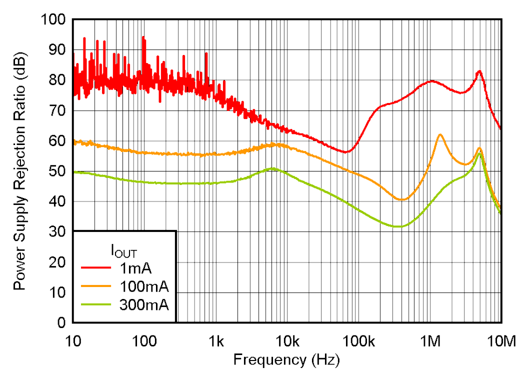


Figure 7-3. PSRR

7.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.4V to 5.5V. Verify the input supply is well regulated and free of spurious noise so the regulator provides a well regulated output with optimum dynamic performance. Set the input supply to at least $V_{OUT(nom)}$ + 0.5V or 1.4V, whichever is greater.

Use a 1µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

7.4 Layout

7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible
- Use copper planes for device connections to optimize thermal performance
- Place thermal vias around the device to distribute the heat

7.4.2 Layout Example

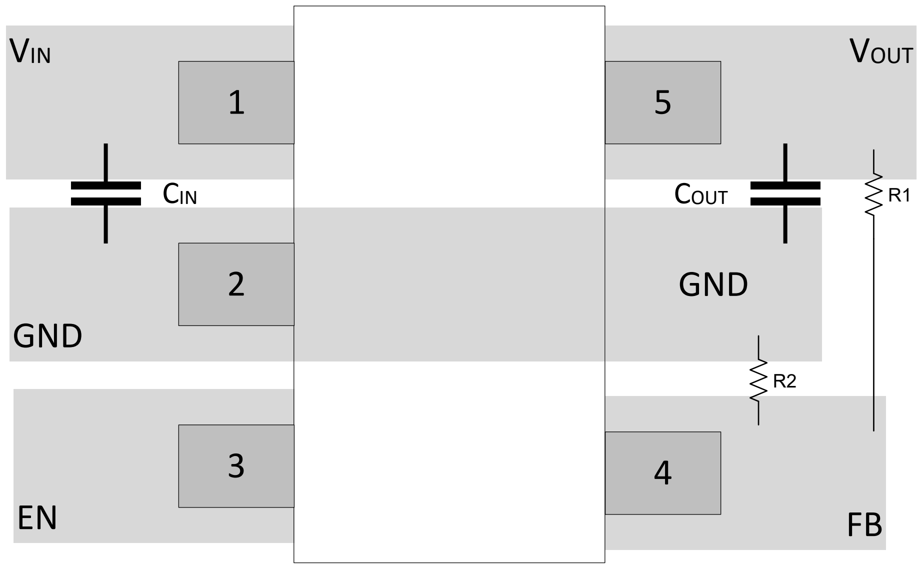


Figure 7-4. DBV Package (SOT-23) Typical Layout

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are listed in this section.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Know Your Limits* application note

8.1.2 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1)	DESCRIPTION
TPS7C1301**(P)yyyz**	**(P)** indicates an active output discharge feature. **yyy** is the package designator. **z** is the package quantity. R is for a standard reel. J is for a jumbo reel.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7C1301PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3RHH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

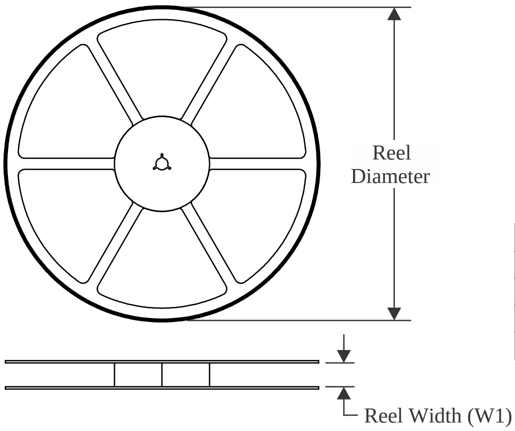
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

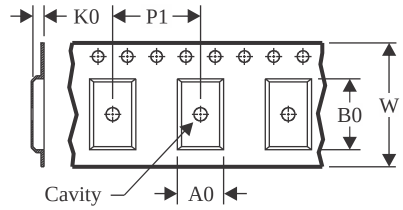
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

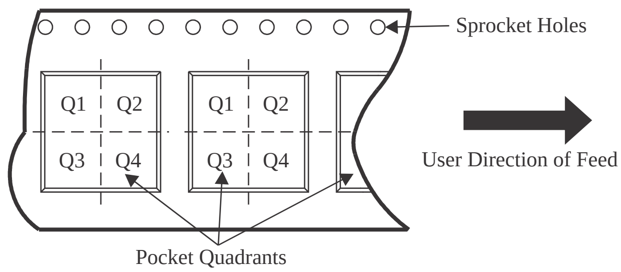


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

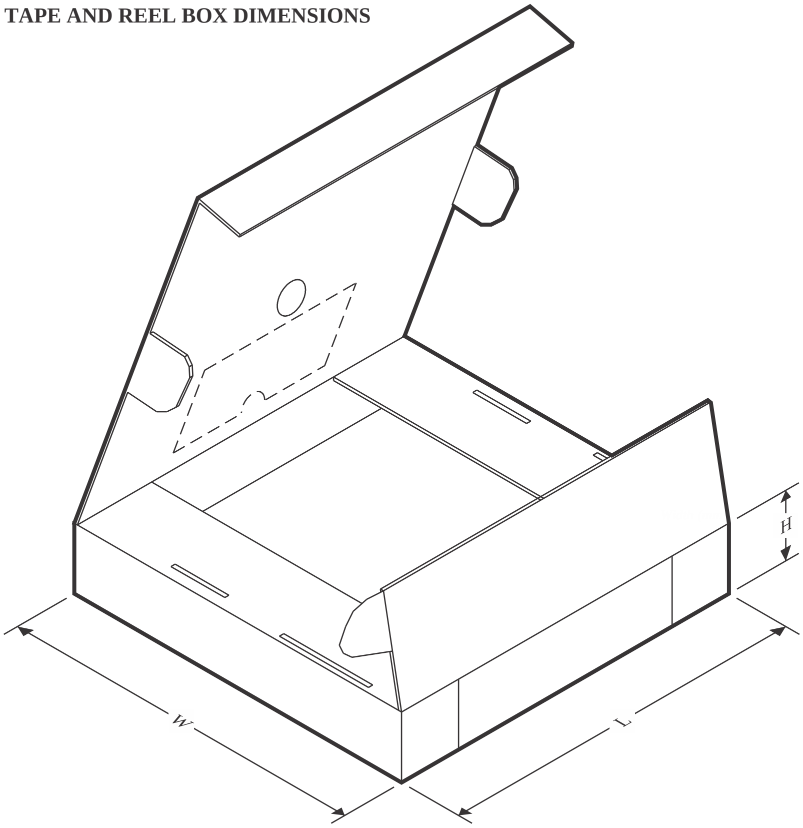
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

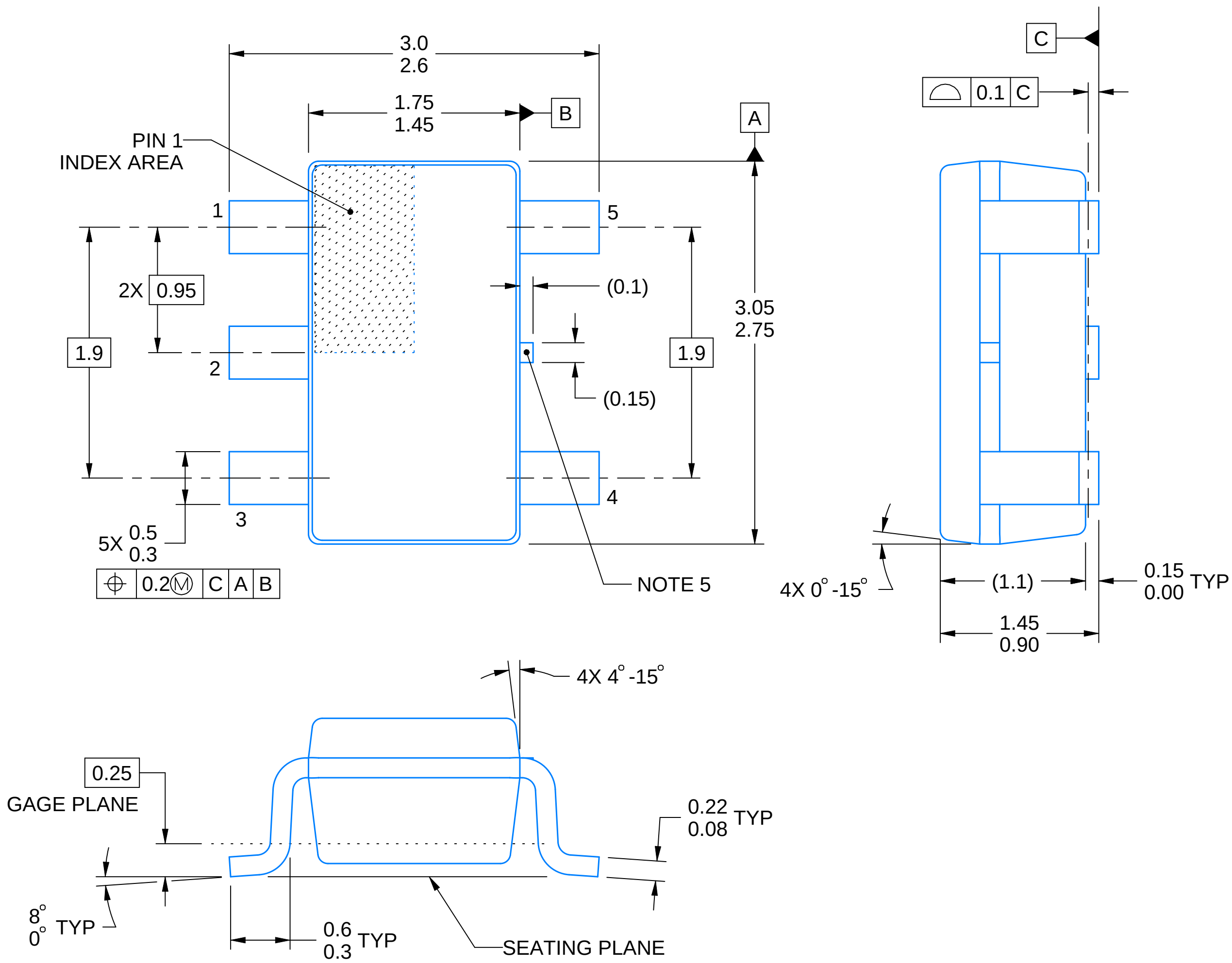
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7C1301PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7C1301PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0



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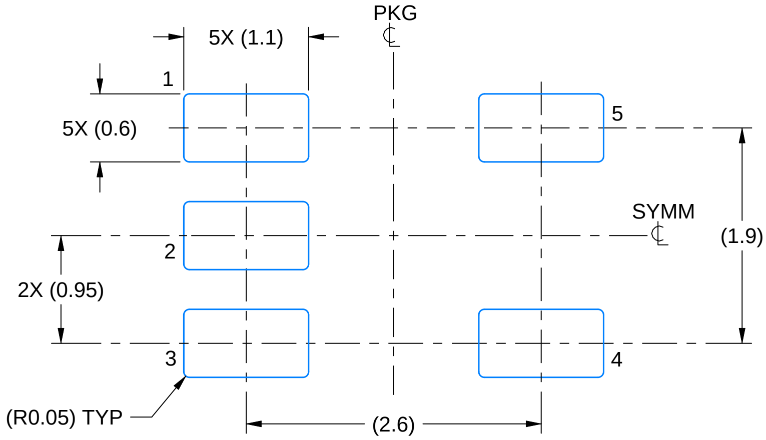
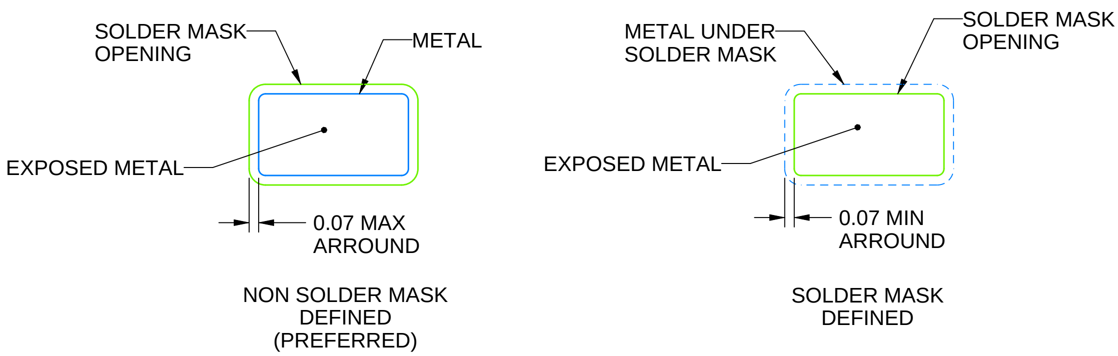
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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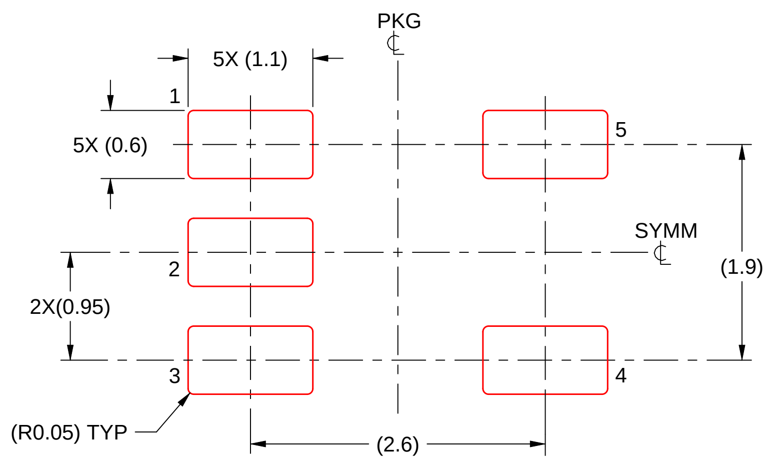
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.