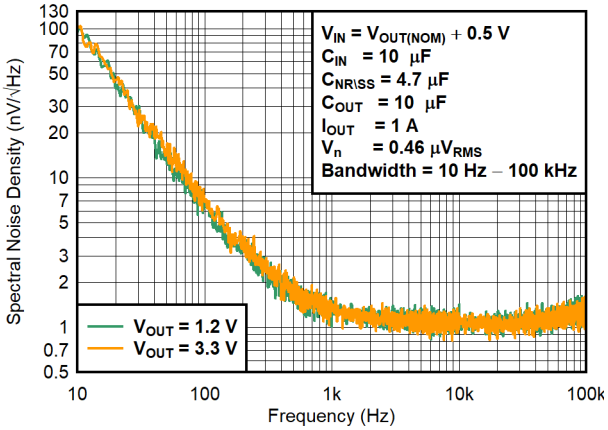
# TPS7A94 1A 超低噪声、超高 PSRR 低压降稳压器

## 1 特性

- 超低输出噪声：
  - 0.46 μ $V_{RMS}$（典型值 10Hz 至 100kHz）
- 高电源纹波抑制 (PSRR)：
  - 100Hz 时为 102dB
  - 1 kHz 时为 110 dB
  - 10 kHz 时为 95 dB
  - 100 kHz 时为 78 dB
  - 在 1MHz 时为 50dB
- 整个线路、负载和温度范围内的精度：1%
- 低压降：150 mV (1 A)
- 宽输入电压范围：1.7 V 至 5.7 V
- 宽输出电压范围：0 V 至 5.5 V
- 并行通道，可实现更低的噪声和更高的电流
- 快速瞬态响应
- 精密使能和 UVLO
- 可编程电流限制
- 可编程 PG 阈值
- 可调启动浪涌控制
- 开漏电源正常状态 (PG) 输出
- 封装：3.00mm × 3.00mm 10 引脚 WSON：
  - JEDEC $R_{\theta JA}$：46.1°C/W
  - EVM $R_{\theta JA}$：25.6°C/W

## 2 应用

- 宏远程无线电单元 (RRU)
- 室外回程单元
- 有源天线系统 mMIMO (AAS)
- 超声波扫描仪
- 实验室和现场仪表
- 传感器、成像和雷达




**与输出电压无关的超低输出噪声 (10Hz – 100kHz)**

## 3 说明

TPS7A94 是一款超低噪声 (0.46μ$V_{RMS}$)、低压降 (LDO) 稳压器，能够以仅 150mV 的压降提供 1A 电流。低压降与宽带宽误差放大器相结合，可在低工作裕量 (500mV) 和高输出电流 (750mA) 下实现非常高的 PSRR（1kHz 时为 110dB，1MHz 时为 50dB）。

该器件的输出可通过外部电阻进行调节，范围为 0V 至 5.5 V。该器件凭借宽输入电压范围，支持低至 1.7V 和高达 5.7V 的操作。该器件具有可编程电流限制、可编程 PG 阈值和精密使能功能，从而能够在应用中进行更好的控制。

该器件凭借高精度基准和宽带宽拓扑，可以轻松并联以实现更低的噪声和更高的电流。

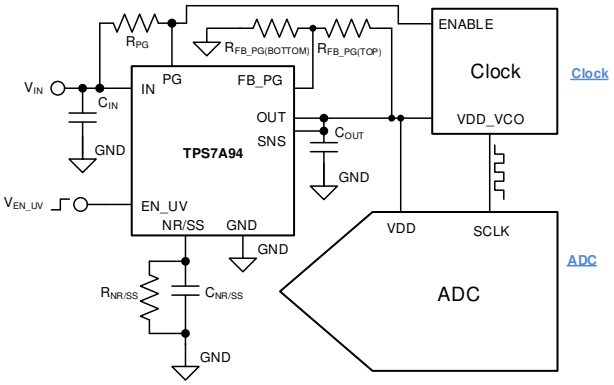
该器件具有 1% 的输出电压精度（在线路、负载和温度范围内）和软启动功能以降低浪涌电流，是为敏感模拟低压器件供电的理想选择。

**封装信息**

| 器件型号 | 封装(1) | 封装尺寸(2) |
|---|---|---|
| TPS7A94 | DSC（WSON，10） | 3.00mm × 3.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。




**典型应用电路**

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

**Changes from Revision B (February 2023) to Revision C (June 2023)** **Page**

- Deleted note regarding output current range from *Optimizing Noise and PSRR* section.....42

**Changes from Revision A (May 2022) to Revision B (February 2023)** **Page**

- Changed *GND Pin Current vs $I_{OUT}$ and Temperature for $V_{OUT}$ = 3.3 V* to *100% Current Limit vs Temperature for $V_{OUT}$ = 1.8 V* curves in *Typical Characteristics* section.....8
- Changed 方程式 1, 方程式 2, and the discussion of these equations in *Precision Enable (External UVLO)* section.....34
- Changed parallel impedance value from *10 kΩ* to *12.5 kΩ* in *Power-Good Feedback (FB_PG Pin) and Power-Good Threshold (PG Pin)* section.....36
- Added *Relationship Between Threshold Voltage, Output Voltage, $I_{FAST_SS}$, and $I_{NR/SS}$ During Start-Up* figure to *Programmable Soft-Start and Noise-Reduction (NR/SS Pin)* section.....39
- Changed discussion of $V_{ON}$ and $V_{OFF}$ in *Detailed Design Procedure* section.....52


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# 5 Pin Configuration and Functions

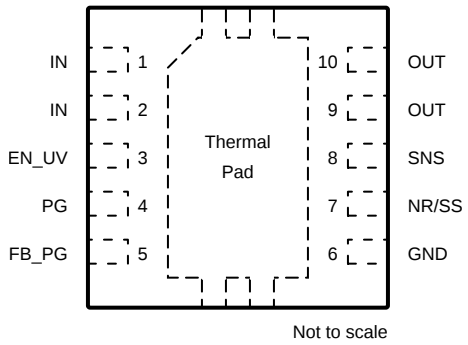


**图 5-1. DSC Package, 10-Pin WSON (Top View)**

**Pin Functions**

| PIN | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | WSON | | |
| EN_UV | 3 | I | Precision enable and undervoltage lockout pin; see the *Precision Enable (External UVLO)* section for details. |
| FB_PG | 5 | I | Power-good feedback pin. This pin has a dual function: this pin programs the PG pin output threshold and scales the factory-programmed current limit value specified in the *Electrical Characteristics* table to either 100%, 80%, or 60%. See the *Power-Good Feedback (FB_PG Pin) and Power-Good Threshold (PG Pin)* section for details. |
| GND | 6 | G | Ground pin; see the *Board Layout* section for details. |
| IN | 1, 2 | P | Input voltage supply pin; see the *Recommended Capacitor Types* section and the *Recommended Operating Conditions* table for additional information. |
| NR/SS | 7 | I | Output voltage set and noise-reduction pin; see the *Programmable Soft-Start and Noise-Reduction (NR/SS Pin)* section for details. |
| OUT | 9, 10 | O | Regulated output pin; see the *Load Transient Response* section for additional information. |
| PG | 4 | O | Open-drain, power-good indicator pin for the LDO output voltage. See the *Power-Good Feedback (FB_PG Pin) and Power-Good Threshold (PG Pin)* section for additional information. |
| SNS | 8 | I | Output sense pin. This pin is the input to the noninverting terminal of the error amplifier; see the *Board Layout* section for details. |
| Thermal pad | | G | The thermal pad is electrically connected to the GND pin; see the *Board Layout* section for details. |

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating junction temperature range and all voltages with respect to GND(unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | IN, PG, EN_UV | –0.3 | 6.0 | V |
| | FB_PG | –0.3 | 1.5 | |
| | OUT | –0.3 | $V_{IN}$ + 0.3 | |
| | NR/SS, SNS | –0.3 | 6.0 | |
| Current | OUT | Internally limited | | A |
| | PG (sink current into the device) | | 5 | mA |
| Temperature | Operating junction, $T_J$ | –55 | 150 | °C |
| | Storage, $T_{stg}$ | –55 | 150 | |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged device model (CDM), per per ANSI/ESDA/JEDEC JS-002(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.


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## 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage range | 1.7 | | 5.7 | V |
| $V_{OUT}$ | Output voltage range | 0.4 | | $V_{IN}$ - $V_{DO}$ | V |
| $I_{OUT}$ | Output current | 0 | | 1 | A |
| $C_{IN}$ | Input capacitor | 4.7 | 10 | 1000 | µF |
| $C_{OUT}$ | Output capacitor | 4.7 | 10 | 1000 | µF |
| $C_{OUT_ESR}$ | Output capacitor ESR | 1 | | 20 | mΩ |
| $Z_{OUT_ESL}$ | Total output loop impedance | | | 2 | nH |
| $C_{NR/SS}$ | Noise-reduction capacitor | 1 | 4.7 | 100 | µF |
| $R_{PG}$ | Power-good pull-up resistance | 10 | | 100 | kΩ |
| $T_J$ | Junction temperature | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPS7A94 | | UNIT |
|---|---|---|---|---|
| | | DSC (WSON)[2] | DSC (WSON)[3] | |
| | | 10 PINS | 10 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 46.1 | 25.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 35.2 | - | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 19.1 | - | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | 0.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 19 | 11.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.9 | - | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.
(2) JEDEC standard. (2s2p)
(3) EVM thermal model using JEDEC measurement methodology, see TPS7A94EVM-046 thermal analysis.

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## 6.5 Electrical Characteristics

over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN(NOM)}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{OUT(NOM)}$ = 3.3 V, $I_{OUT}$ = 1 mA, $V_{EN}$ = 1.8 V, $C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 0 nF, and PG pin pulled up to $V_{IN}$ with 100 kΩ (4) (unless otherwise noted); typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage range | | 1.7 | | 5.7 | V |
| $V_{UVLO}$ | Input supply UVLO | $V_{IN}$ rising, no load | | 1.6 | 1.7 | V |
| $V_{HYS(UVLO)}$ | Input supply UVLO hysteresis | No load | 40 | 53 | | mV |
| $I_{NR/SS}$ | NR/SS pin current | $V_{IN}$ = 1.7 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 1.2 V | | 150 | | µA |
| | | 1.7 V ≤ $V_{IN}$ ≤ 5.5 V, 0.4 V ≤ $V_{OUT}$ < 1.2 V, 1 mA ≤ $I_{OUT}$ ≤ 1A | –1.5 | | 1.5 | % |
| | | 1.7 V ≤ $V_{IN}$ ≤ 5.5 V, 1.2 V ≤ $V_{OUT}$ ≤ 5.1 V, 1 mA ≤ $I_{OUT}$ ≤ 1A | –1 | | 1 | % |
| $I_{FAST_SS}$ | NR/SS fast start-up charging current | $V_{NR/SS}$ = GND, $V_{IN}$ ≥ 2.5 V, $V_{FB_PG}$ < 0.2 V, $I_{OUT}$ = 0 mA | | 2.1 | | mA |
| | | $V_{NR/SS}$ = GND, $V_{IN}$ = 1.7 V, $V_{FB_PG}$ < 0.2 V, $I_{OUT}$ = 0 mA | | 1.5 | | |
| $V_{OUT}$ | Output voltage range | | 0 | | 5.5 | V |
| $V_{OS}$ | Output offset voltage ($V_{NR/SS}$ – $V_{OUT}$) | 1.7 V ≤ $V_{IN}$ ≤ 5.7 V, 1.2 V ≤ $V_{OUT}$ ≤ 5.1 V, 1 mA ≤ $I_{OUT}$ ≤ 1 A | –2 | ±0.1 | 2 | mV |
| | | 1.7 V ≤ $V_{IN}$ ≤ 5.7 V, 0.4 V ≤ $V_{OUT}$ < 1.2 V, 1 mA ≤ $I_{OUT}$ ≤ 1 A | –5 | ±0.2 | 5 | |
| $\Delta V_{OUT(\Delta VIN)}$ | Line regulation: $\Delta I_{NR/SS}$ | 0.4 V ≤ $V_{OUT}$ < 1.2 V, $I_{OUT}$ = 1 mA, $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 5.7 V | | –0.9 | | nA/V |
| | | $V_{OUT}$ = 1.2 V and $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1mA, $V_{IN}$ = ($V_{OUT}$ + 0.5V) to 5.7 V | | 2 | | |
| | Line regulation: $\Delta V_{OS}$ | 0.4 V ≤ $V_{OUT}$ < 1.2 V, $I_{OUT}$ = 1 mA, $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 5.7 V | | –4.5 | | µV/V |
| | | $V_{OUT}$ = 1.2 V & $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 mA, $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 5.7 V | | 2.1 | | |
| $\Delta V_{OUT(\Delta IOUT)}$ | Load regulation: $\Delta I_{NR/SS}$ (1) | $V_{IN}$ = 1.7 V, $V_{OUT}$ = 1.2 V, 1 mA ≤ $I_{OUT}$ ≤ 1 A | | 2.3 | | nA |
| | | $V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, 1 mA ≤ $I_{OUT}$ ≤ 1 A | | –3.6 | | |
| | | $V_{IN}$ = 5.6 V, $V_{OUT}$ = 5.1 V, 1 mA ≤ $I_{OUT}$ ≤ 1 A | | –21 | | |
| | Load regulation: $\Delta V_{OS}$ (1) | $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, 1.2V ≤ $V_{OUT}$ ≤ 5.1 V, 1 mA ≤ $I_{OUT}$ ≤ 1 A | | 0.03 | | mV |
| $\Delta I_{NR/SS(\Delta VNR/SS)}$ | Change in $I_{NR/SS}$ vs $V_{NR/SS}$ | 0.4 V ≤ $V_{NR/SS}$ ≤ 1.5 V, $V_{IN}$ = 5.7 V, $I_{OUT}$ = 1 mA | | 6.3 | | nA |
| | | 1.5 V ≤ $V_{NR/SS}$ ≤ 5 V, $V_{IN}$ = 5.7 V, $I_{OUT}$ = 1 mA | | –3.3 | | nA |
| $\Delta V_{OS(\Delta VNR/SS)}$ | Change in $V_{OS}$ vs $V_{NR/SS}$ | 0.4 V ≤ $V_{NR/SS}$ ≤ 1.5 V, $V_{IN}$ = 5.7 V, $I_{OUT}$ = 1 mA | | 0.033 | | mV |
| | | 1.5 V ≤ $V_{NR/SS}$ ≤ 5 V, $V_{IN}$ = 5.7 V, $I_{OUT}$ = 1 mA | | 0.013 | | mV |
| $V_{DO}$ | Dropout voltage(2) | 1.7 V ≤ $V_{IN}$ < 2.0 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 99% x $V_{OUT(NOM)}$ | | 160 | | mV |
| | | 1.7 V ≤ $V_{IN}$ < 2.0 V, $I_{OUT}$ = 1 A, $V_{OUT}$ = 99% x $V_{OUT(NOM)}$ | | 165 | 220 | |
| | | $V_{IN}$ ≥ 2.0 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 99% x $V_{OUT(NOM)}$ | | 140 | | |
| | | $V_{IN}$ ≥ 2.0 V, $I_{OUT}$ = 1 A, $V_{OUT}$ = 99% x $V_{OUT(NOM)}$ | | 150 | 240 | |
| $I_{CL}$ | Output current limit | $V_{OUT}$ forced at 90% of $V_{OUT(NOM)}$, $V_{IN}$ = $V_{OUT(NOM)}$ + 200 mV or $V_{IN}$ = 1.7 V whichever is greater, $V_{OUT(NOM)}$ ≥ 1.2 V, $R_{PGFB-to-GND}$ ≤ 12.5 kΩ (±1%) | 1.2 | 1.3 | 1.4 | A |
| | | $V_{OUT}$ forced at 90% of $V_{OUT(NOM)}$, $V_{IN}$ = $V_{OUT(NOM)}$ + 200 mV or $V_{IN}$ = 1.7 V whichever is greater, $V_{OUT(NOM)}$ ≥ 1.2 V, $R_{PGFB-to-GND}$ = 50 kΩ (±1%) | 0.96 | 1.04 | 1.12 | A |
| | | $V_{OUT}$ forced at 90% of $V_{OUT(NOM)}$, $V_{IN}$ = $V_{OUT(NOM)}$ + 200 mV or $V_{IN}$ = 1.7 V whichever is greater, $V_{OUT(NOM)}$ ≥ 1.2 V, $R_{PGFB-to-GND}$ = 100 kΩ (±1%) | 0.72 | 0.78 | 0.84 | A |
| $\Delta I_{SC}$ | Output current limit variation (3) | $V_{IN}$ = $V_{OUT(NOM)}$ + 200 mV or $V_{IN}$ = 1.7 V whichever is greater, $V_{OUT}$ = 0 V | | 5 | | % |


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## 6.5 Electrical Characteristics (continued)

over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN(NOM)}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{OUT(NOM)}$ = 3.3 V, $I_{OUT}$ = 1 mA, $V_{EN}$ = 1.8 V, $C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 0 nF, and PG pin pulled up to $V_{IN}$ with 100 kΩ (4) (unless otherwise noted); typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{GND}$ | GND pin current | $V_{IN}$ = 5.7 V, $V_{OUT}$ = 5.1 V, $I_{OUT}$ = 0.1 mA | 8 | 15 | 22 | mA |
| | | $V_{IN}$ = 1.7 V, $I_{OUT}$ = 1 A, $V_{OUT}$ = 1.2 V | 34 | 41 | 51 | |
| $I_{SDN}$ | Shutdown GND pin current | PG = (open), $V_{IN}$ = 5.7 V, $V_{EN_UV}$ = 0.4 V | | 0.1 | 30 | µA |
| $I_{EN_UV}$ | EN_UV pin current | $V_{IN}$ = 5.7 V, 0 V ≤ $V_{EN_UV}$ ≤ 5.5 V | –1 | | 1 | µA |
| $V_{IH(EN_UV)}$ | EN_UV trip point rising (turn-on) | $V_{IN}$ = 1.7 V, no load | 1.20 | 1.22 | 1.25 | V |
| $V_{HYS(EN_UV)}$ | EN_UV trip point hysteresis | $V_{IN}$ = 1.7 V, no load | | 150 | | mV |
| $t_{PGDH}$ | PG delay time rising | Time from $V_{OUT}$ crossing PG threshold% to PG reaching 20% of the value | | 1.1 | | ms |
| $t_{PGDL}$ | PG delay time falling | Time from 90% of $V_{OUT}$ to 80% of PG | | 3 | | µs |
| $V_{FB_PG}$ | FB_PG pin trip point (rising) | 1.7 V ≤ $V_{IN}$ ≤ 5.7 V | 0.19 | 0.2 | 0.21 | V |
| $V_{HYS(FB_PG)}$ | FB_PG pin hysteresis | 1.7 V ≤ $V_{IN}$ ≤ 5.7 V | | 6 | | mV |
| $V_{OL(PG)}$ | PG pin low-level output voltage | $V_{IN}$ = 1.7 V, $V_{OUT}$ < $V_{FB_PG(threshold)}$, $I_{PG}$ = –1 mA (current into device) | | | 0.4 | V |
| $I_{PG(LKG)}$ | PG pin leakage current | $V_{IN}$ = 5.7 V, $V_{OUT}$ > $V_{FB_PG(threshold)}$, $V_{PG}$ = 5.5 V | | | 1 | µA |
| $I_{FB_PG}$ | FB_PG pin leakage current | $V_{IN}$ = 5.7 V, $V_{FB_PG}$ = 0.2 V | –100 | | 100 | nA |
| PSRR | Power-supply ripple rejection | f = 1 MHz, $V_{IN}$ = 3.8 V, $V_{OUT(NOM)}$ = 3.3 V, $I_{OUT}$ = 750 mA, $C_{NR/SS}$ = 4.7 µF | | 51 | | dB |
| $V_n$ | Output noise voltage | BW = 10 Hz to 100 kHz, 1.7 V ≤ $V_{IN}$ ≤ 5.7 V, $V_{OUT(NOM)}$ = 1.2 V, $I_{OUT}$ = 1.0 A, $C_{NR/SS}$ = 4.7 µF | | 0.46 | | $\mu V_{RMS}$ |
| | | BW = 10 Hz to 100 kHz, $V_{IN}$ = 1.8 V, $V_{OUT(NOM)}$ = 0.8 V, $I_{OUT}$ = 1.0 A, $C_{NR/SS}$ = 4.7 µF | | 0.835 | | |
| | Noise spectral density | f = 100 Hz, 1.7 V ≤ $V_{IN}$ ≤ 5.7 V, $V_{OUT(NOM)}$ = 1.2 V, $I_{OUT}$ = 1.0 A, $C_{NR/SS}$ = 4.7 µF | | 6.6 | | $nV/\sqrt{Hz}$ |
| | | f = 1 kHz, 1.7 V ≤ $V_{IN}$ ≤ 5.7 V, $V_{OUT(NOM)}$ = 1.2 V, $I_{OUT}$ = 1.0 A, $C_{NR/SS}$ = 4.7 µF | | 1.3 | | |
| | | f = 10 kHz, 1.7 V ≤ $V_{IN}$ ≤ 5.7 V, $V_{OUT(NOM)}$ = 1.2 V, $I_{OUT}$ = 1.0 A, $C_{NR/SS}$ = 4.7 µF | | 1.1 | | |
| $R_{PULLDOWN_NRSS}$ | NRSS active discharge resistance | $V_{IN}$ = 1.7 V, $V_{EN_UV}$ = GND | | 15 | | Ω |
| $R_{PULLDOWN}$ | Output active discharge resistance | $V_{IN}$ = 1.7 V, $V_{EN_UV}$ = GND | | 195 | | Ω |
| TSD(shutdown) | Thermal shutdown temperature | Shutdown, temperature increasing | | 175 | | °C |
| TSD(reset) | Thermal shutdown reset temperature | Reset, temperature decreasing | | 160 | | |

(1) The device is not tested under conditions where $V_{IN}$ > $V_{OUT(NOM)}$ + 2.5 V and $I_{OUT}$ = 1 A because the junction temperature is higher than +125°C. Also, this accuracy specification does not apply on any application condition that exceeds the maximum junction temperature.
(2) Measured when output voltage drops 1% below targeted value.
(3) Brickwall current limit: $I_{CL_\%}$ = ($I_{SC}$ - $I_{CL_@0.9xVOUT}$) / $I_{CL_@0.9xVOUT}$ x 100.
(4) Additional information on setting the PG pullup resistor can be found in the application section.

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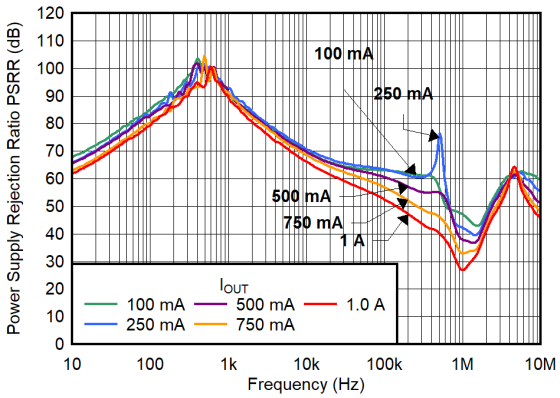
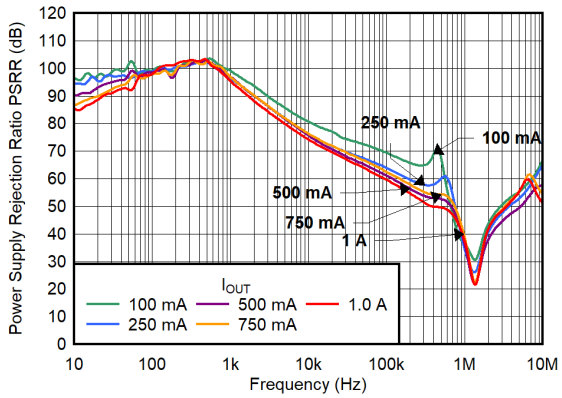
## 6.6 Typical Characteristics

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



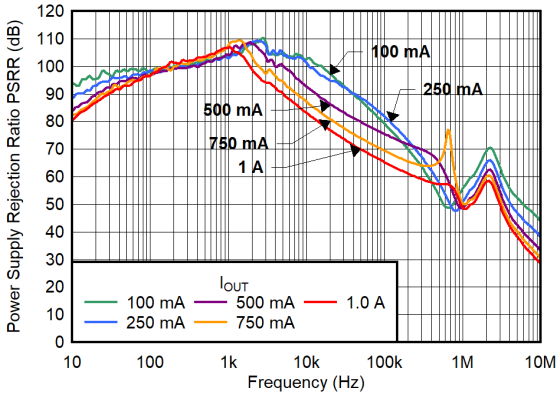

$C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, $V_{IN}$ = 1.7 V

**图 6-1. PSRR vs Frequency and $I_{OUT}$ for $V_{OUT}$ = 1.2 V**



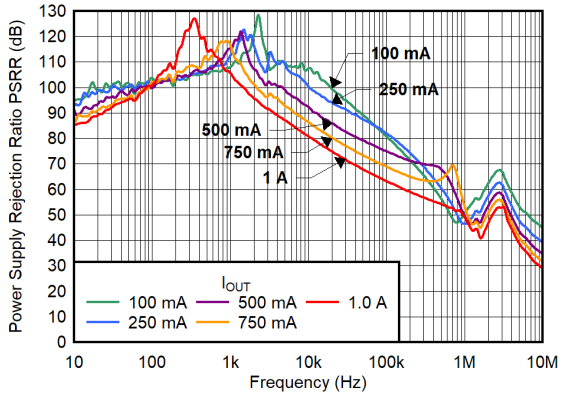

$C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, $V_{IN}$ = 2.3 V

**图 6-2. PSRR vs Frequency and $I_{OUT}$ for $V_{OUT}$ = 1.8 V**



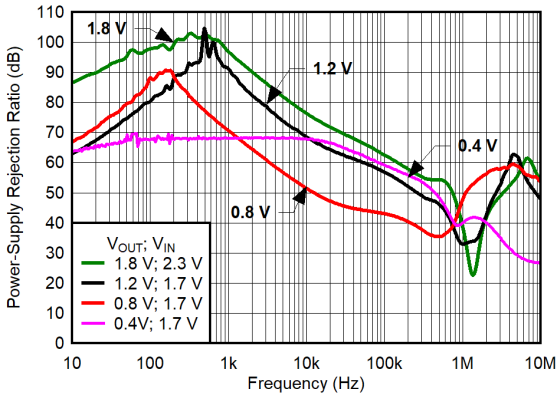

$C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, $V_{IN}$ = 3.8 V

**图 6-3. PSRR vs Frequency and $I_{OUT}$ for $V_{OUT}$ = 3.3 V**



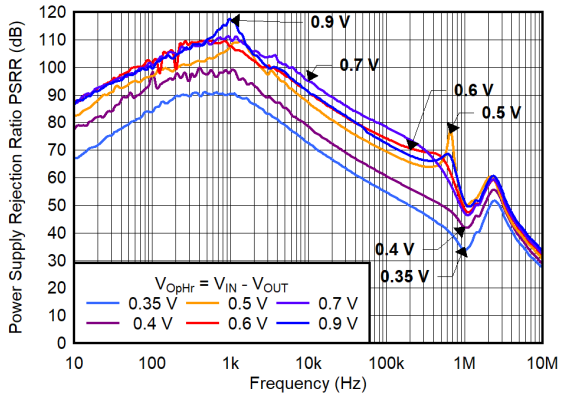

$C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, $V_{IN}$ = 5.5 V

**图 6-4. PSRR vs Frequency and $I_{OUT}$ for $V_{OUT}$ = 5.0 V**




$C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, $V_{IN}$ = $V_{OUT}$ + 0.5 V, $I_{OUT}$ = 750 mA

**图 6-5. PSRR vs Frequency and Input Pairs**




$C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, $V_{IN}$ = $V_{OUT}$ + $V_{OpHr}$, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 750 mA

**图 6-6. PSRR vs Frequency for Operating Headroom ($V_{OpHr}$)**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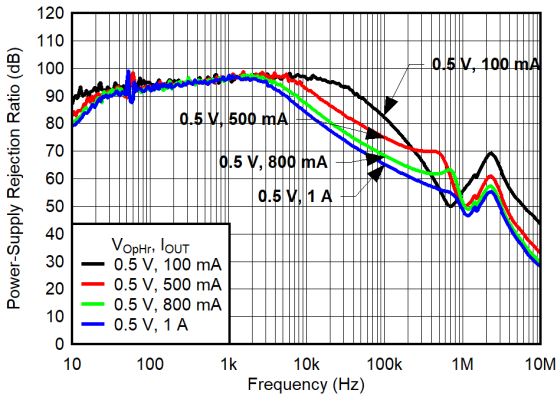
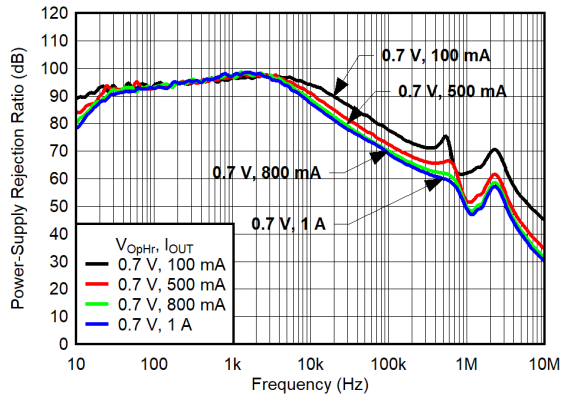
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



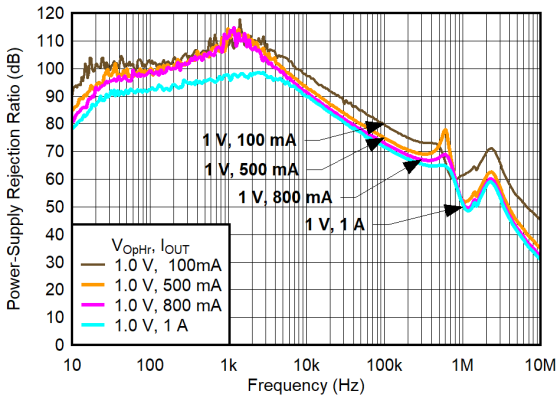

$V_{OUT}$ = 3.3 V, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF

**图 6-7. PSRR vs Frequency for Operating Headroom ($V_{OpHr}$) and $I_{OUT}$**



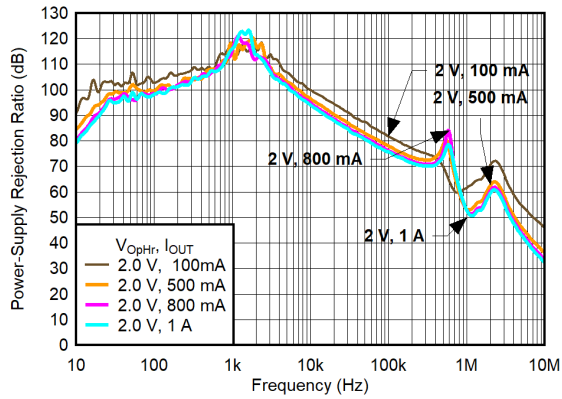

$V_{OUT}$ = 3.3 V, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF

**图 6-8. PSRR vs Frequency for Operating Headroom ($V_{OpHr}$) and $I_{OUT}$**



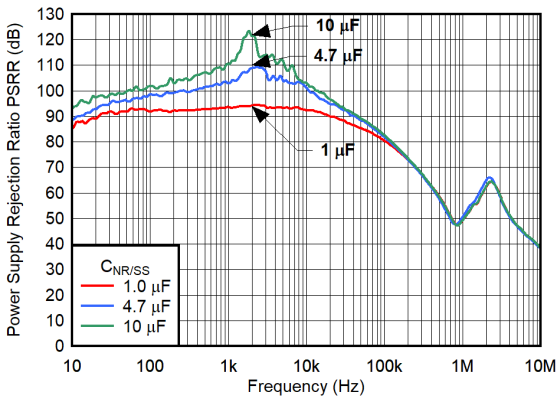

$V_{OUT}$ = 3.3 V, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF

**图 6-9. PSRR vs Frequency for Operating Headroom ($V_{OpHr}$) and $I_{OUT}$**



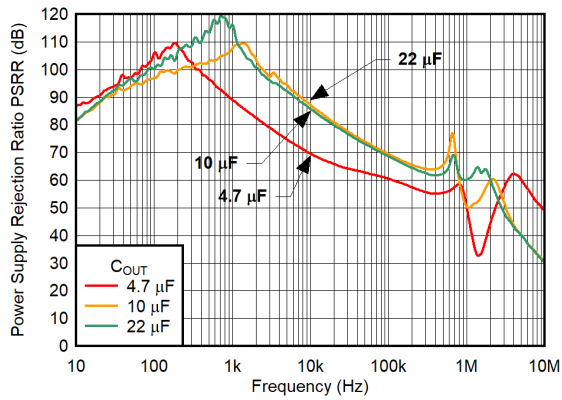

$V_{OUT}$ = 3.3 V, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF

**图 6-10. PSRR vs Frequency for Operating Headroom ($V_{OpHr}$) and $I_{OUT}$**




$C_{OUT}$ = 10 µF, $V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 250 mA

**图 6-11. PSRR vs Frequency and $C_{NR/SS}$**




$C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 750 mA

**图 6-12. PSRR vs Frequency and $C_{OUT}$**

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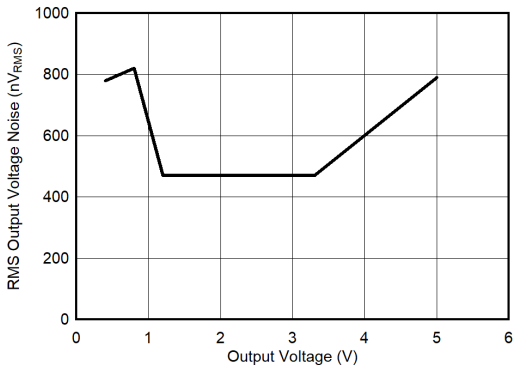
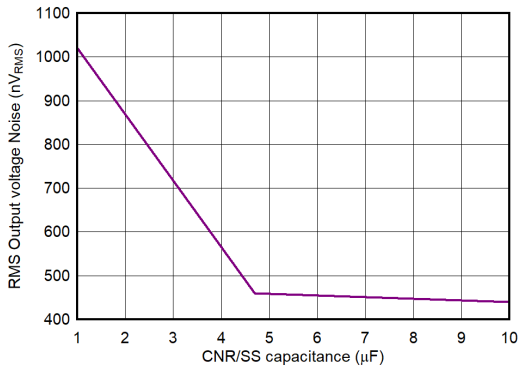
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



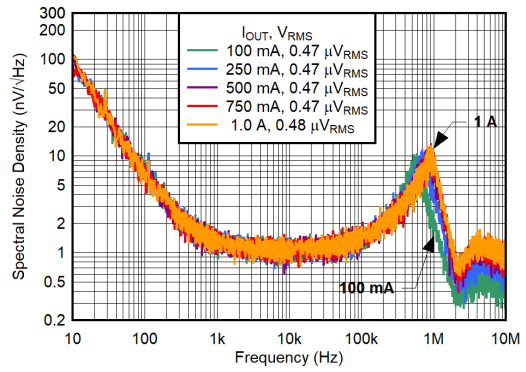

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = $V_{OUT}$ + 0.5 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 750 mA (10 Hz – 100 kHz)

**图 6-13. Output Voltage Noise (RMS) vs Output Voltage**



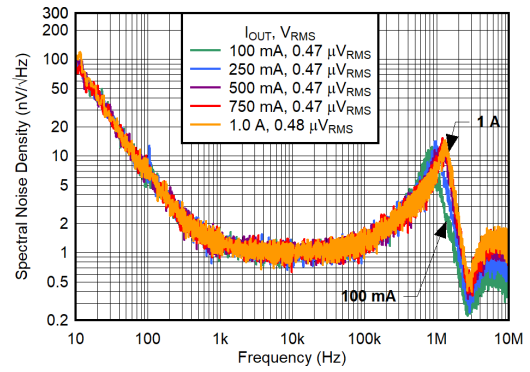

$C_{IN}$ = $C_{OUT}$ = 10 µF, $I_{OUT}$ = 750 mA (10 Hz – 100 kHz)

**图 6-14. Output Voltage Noise (RMS) vs $C_{NR/SS}$**



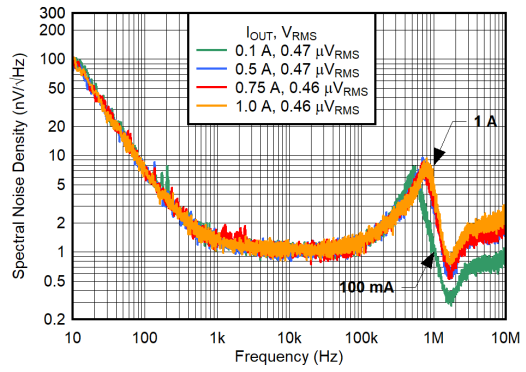

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF (10 Hz – 100 kHz)

**图 6-15. Output Voltage Noise Density vs Frequency for $I_{OUT}$ and $V_{OUT}$ = 1.2 V**



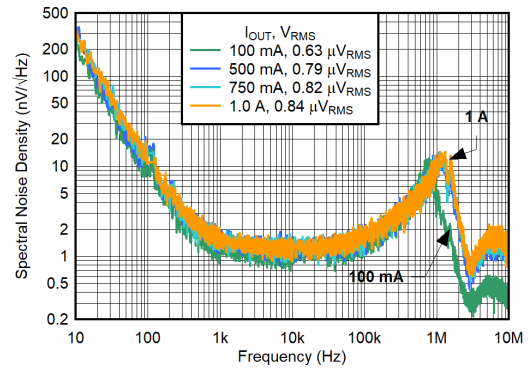

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF (10 Hz – 100 kHz)

**图 6-16. Output Voltage Noise Density vs Frequency for $I_{OUT}$ and $V_{OUT}$ = 1.8 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF (10 Hz – 100 kHz)

**图 6-17. Output Voltage Noise Density vs Frequency for $I_{OUT}$ and $V_{OUT}$ = 3.3 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF (10 Hz – 100 kHz)

**图 6-18. Output Voltage Noise Density vs Frequency for $I_{OUT}$ and $V_{OUT}$ = 5.0 V**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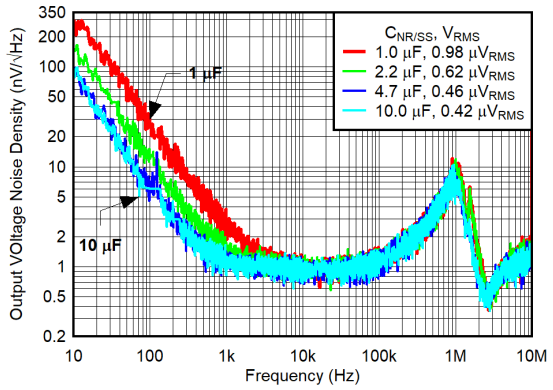
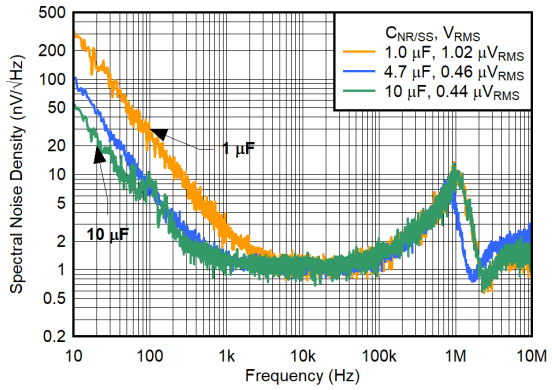
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



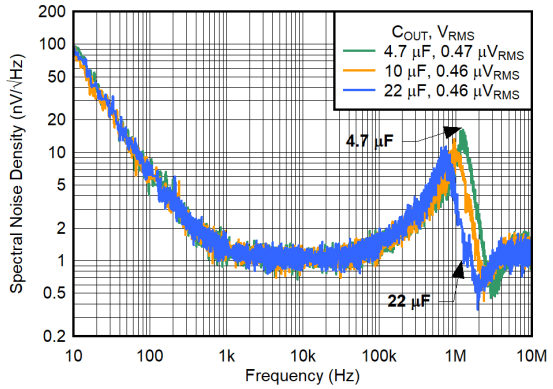

$C_{IN}$ = $C_{OUT}$ = 10 µF, $I_{OUT}$ = 500 mA (10 Hz – 100 kHz)

**图 6-19. Output Noise vs $C_{NR/SS}$ for $V_{OUT}$ = 3.3 V**



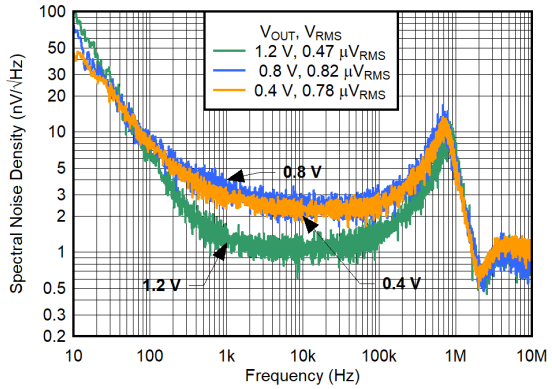

$C_{IN}$ = $C_{OUT}$ = 10 µF, $I_{OUT}$ = 750 mA (10 Hz – 100 kHz)

**图 6-20. Output Voltage Noise (RMS) vs $C_{NR/SS}$ for $V_{OUT}$ = 3.3 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA (10 Hz – 100 kHz)

**图 6-21. Output Voltage Noise Density vs Frequency and $C_{OUT}$ for $V_{OUT}$ = 3.3 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 750 mA (10 Hz – 100 kHz)

**图 6-22. Output Voltage Noise Density vs Frequency and Input Pairs**

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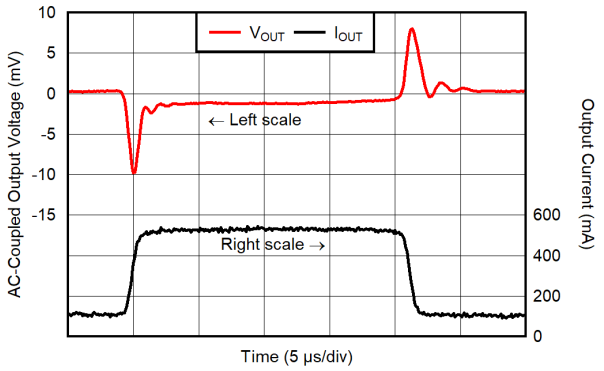
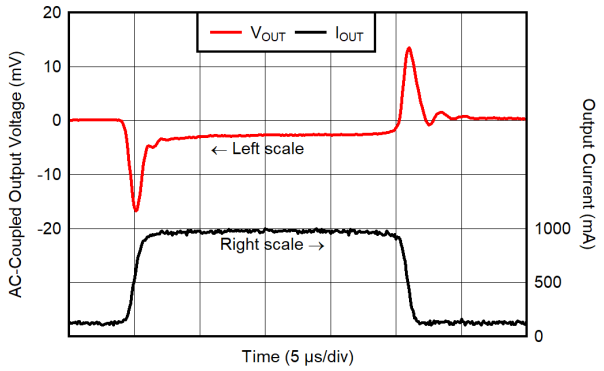
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



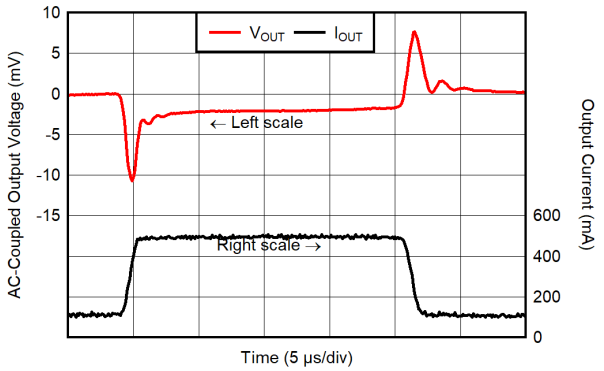

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 1.7 V, SR = 1 A/µs

**图 6-23. Load Transient Response for $V_{OUT}$ = 1.2 V, $I_{OUT}$ = 100 mA to 500 mA**



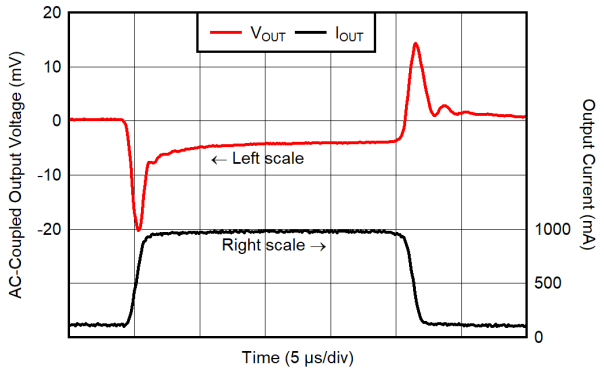

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 1.7 V, SR = 1 A/µs

**图 6-24. Load Transient Response for $V_{OUT}$ = 1.2 V, $I_{OUT}$ = 100 mA to 1 A**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 3.8 V, SR = 1 A/µs

**图 6-25. Load Transient Response for $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 100 mA to 500 mA**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 3.8 V, SR = 1 A/µs

**图 6-26. Load Transient Response for $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 100 mA to 1 A**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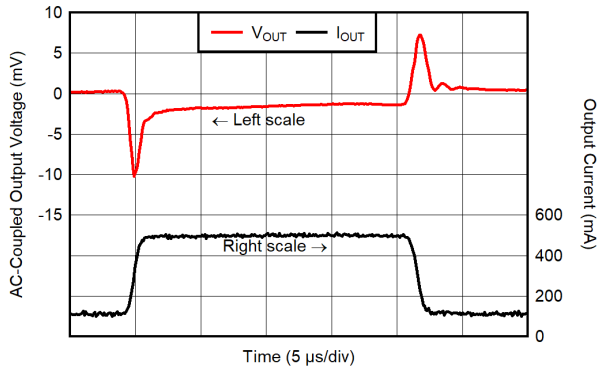
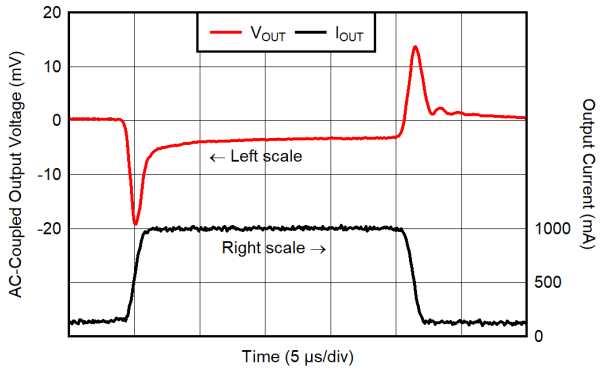
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



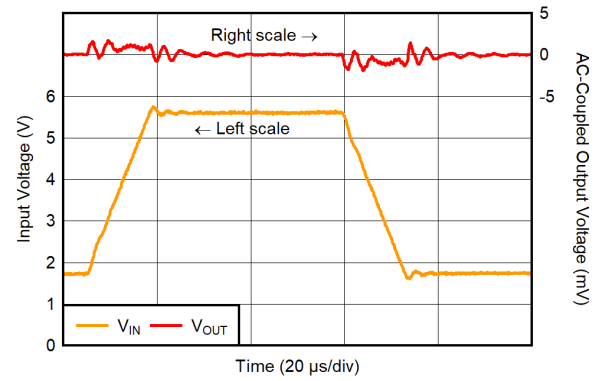

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 5.7 V, SR = 1 A/µs

**图 6-27. Load Transient Response for $V_{OUT}$ = 5.2 V, $I_{OUT}$ = 100 mA to 500 mA**



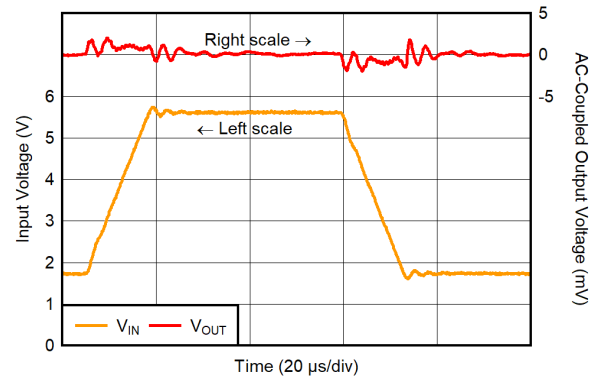

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 5.7 V, SR = 1 A/µs

**图 6-28. Load Transient Response for $V_{OUT}$ = 5.2 V, $I_{OUT}$ = 100 mA to 1 A**



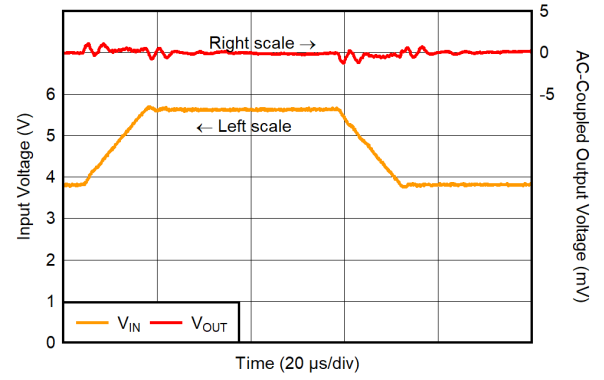

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-29. Line Transient Response for $V_{OUT}$ = 1.2 V, $I_{OUT}$ = 500 mA**



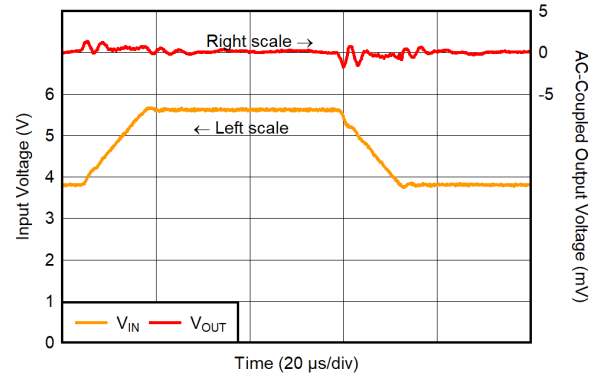

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-30. Line Transient Response for $V_{OUT}$ = 1.2 V, $I_{OUT}$ = 1 A**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-31. Line Transient Response for $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 500 mA**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-32. Line Transient Response for $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 A**

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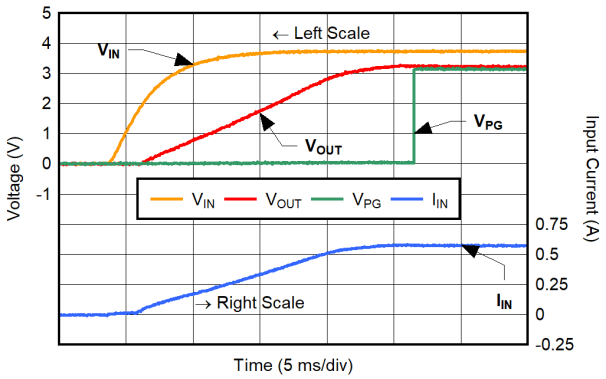
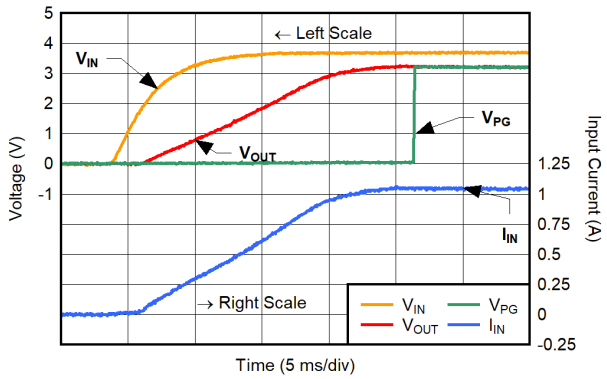
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



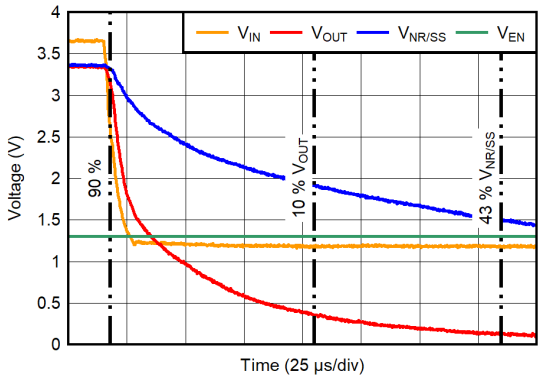

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OUT}$ = 3.3 V

**图 6-33. Start-Up Waveform for $I_{OUT}$ = 500 mA**



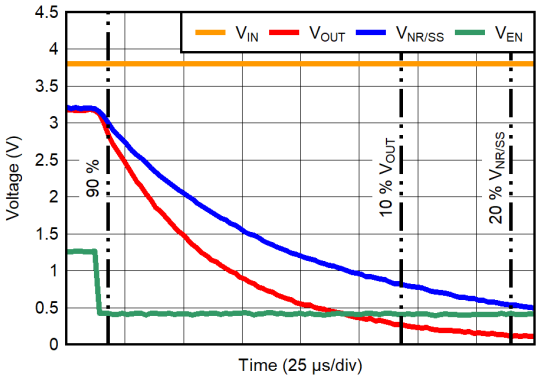

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OUT}$ = 3.3 V

**图 6-34. Start-Up Waveform for $I_{OUT}$ = 1 A**



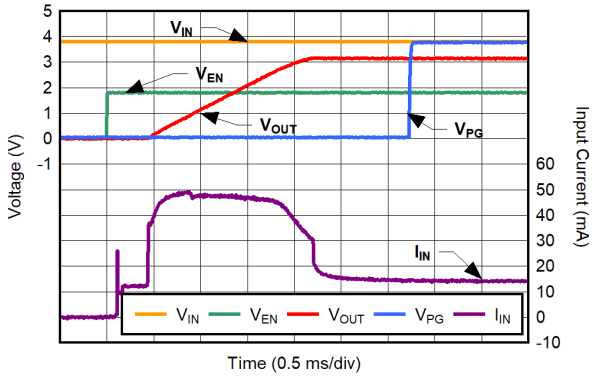

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OUT}$ = 3.3 V

**图 6-35. Shutdown Waveform for $UVLO_{(IN)}$**



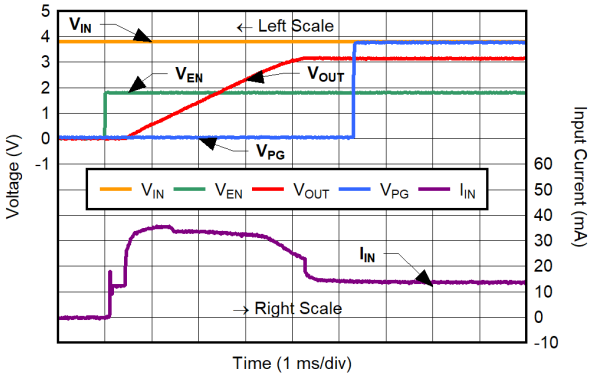

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OUT}$ = 3.3 V

**图 6-36. Shutdown Waveform With EN**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $I_{OUT}$ = 0 mA, $V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V

**图 6-37. Inrush Current for $C_{NR/SS}$ = 1.0 µF**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $I_{OUT}$ = 0 mA, $V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V

**图 6-38. Inrush Current for $C_{NR/SS}$ = 2.2 µF**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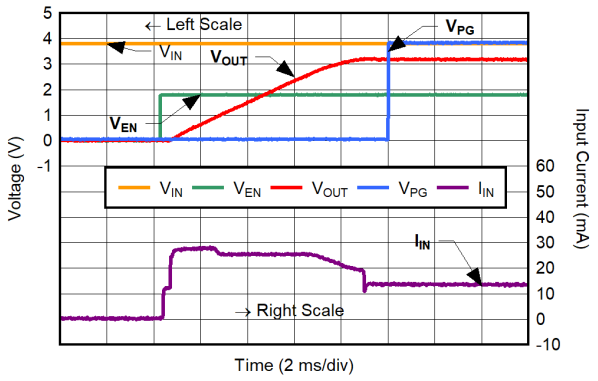
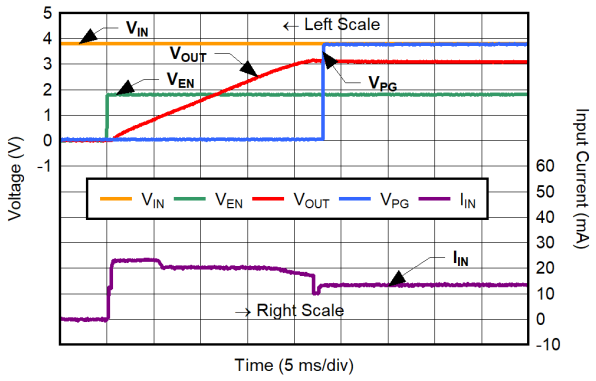
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



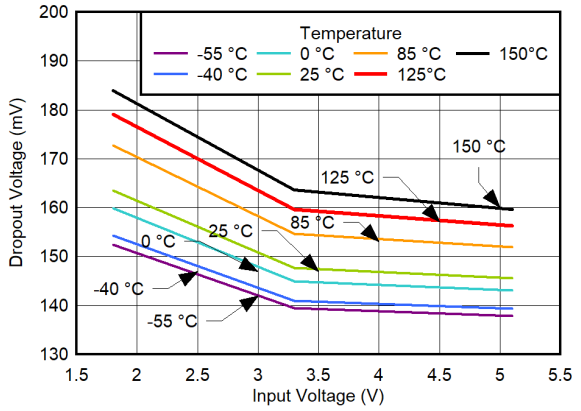

$C_{IN}$ = $C_{OUT}$ = 10 µF, $I_{OUT}$ = 0 mA, $V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V

**图 6-39. Inrush Current for $C_{NR/SS}$ = 4.7 µF**



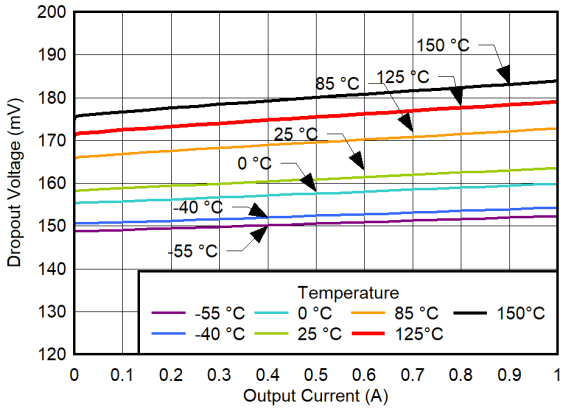

$C_{IN}$ = $C_{OUT}$ = 10 µF, $I_{OUT}$ = 0 mA, $V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V

**图 6-40. Inrush Current for $C_{NR/SS}$ = 10 µF**



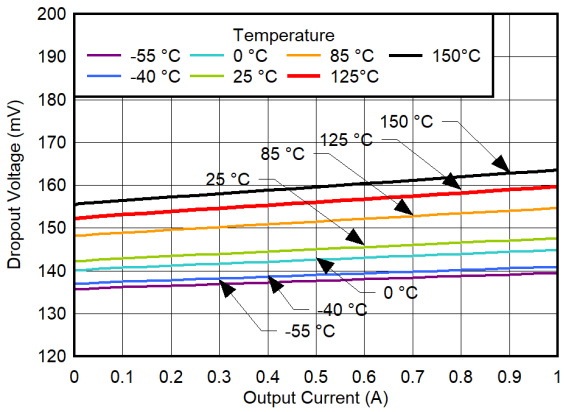

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 A

**图 6-41. Dropout Voltage vs $V_{IN}$ for $I_{OUT}$ = 1 A**



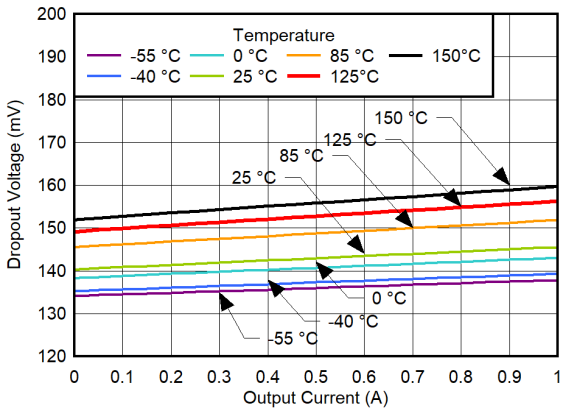

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-42. Dropout Voltage vs $I_{OUT}$ for $V_{OUT}$ = 1.8 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-43. Dropout Voltage vs $I_{OUT}$ for $V_{OUT}$ = 3.3 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-44. Dropout Voltage vs $I_{OUT}$ for $V_{OUT}$ = 5.1 V**

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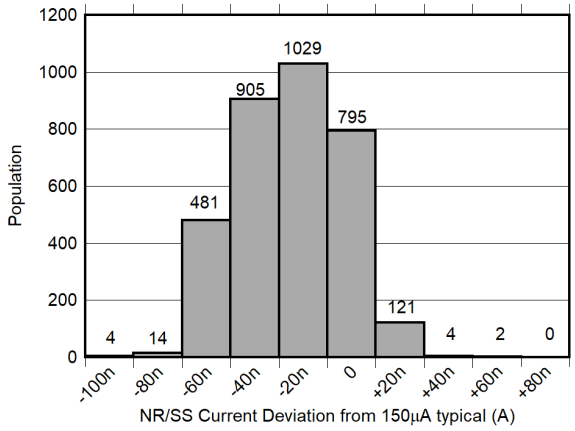
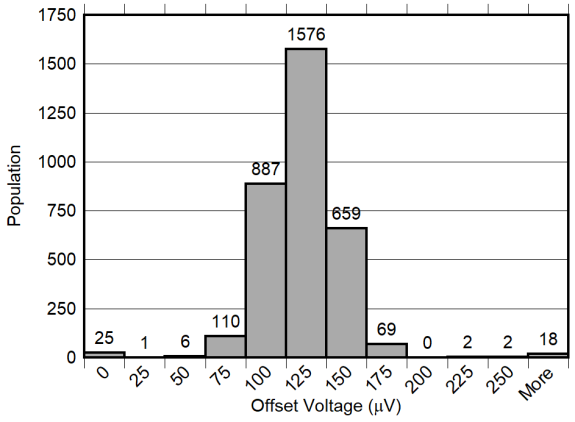
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



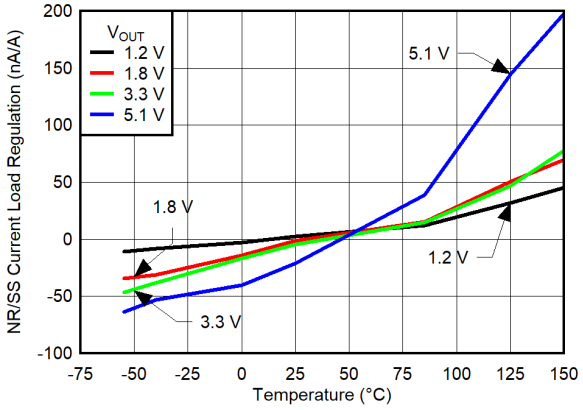

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 5.7 V, $I_{OUT}$ = 1 mA

**图 6-45. $I_{NR/SS}$ Distribution**



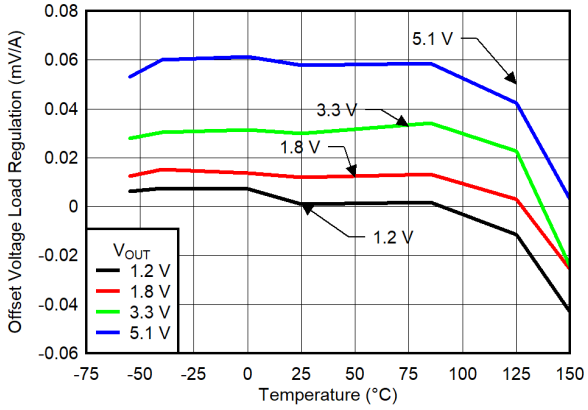

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 5.7 V, $V_{OUT}$ = 5.1 V, $I_{OUT}$ = 1 mA

**图 6-46. $V_{OS}$ Distribution**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-47. $I_{NR/SS}$ Load Regulation**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-48. $V_{OS}$ Load Regulation**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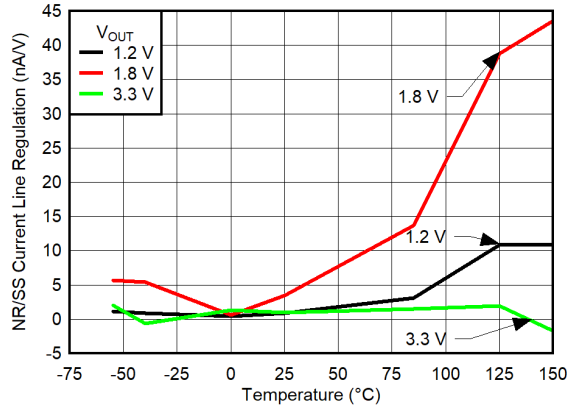
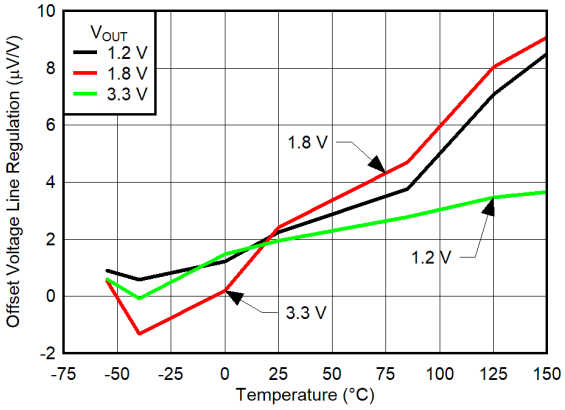
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



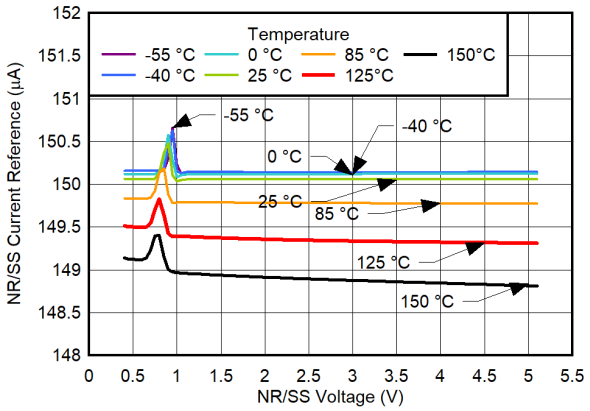

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-49. $I_{NR/SS}$ Line Regulation**



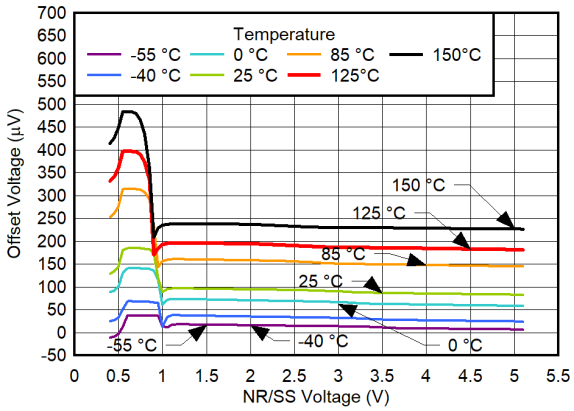

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-50. $V_{OS}$ Line Regulation**



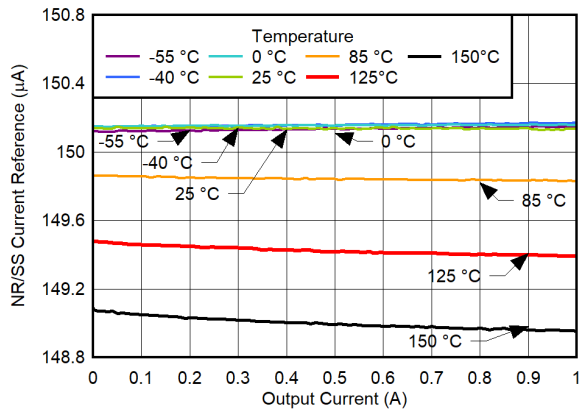

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA

**图 6-51. $I_{NR/SS}$ vs $V_{NR/SS}$ and Temperature**



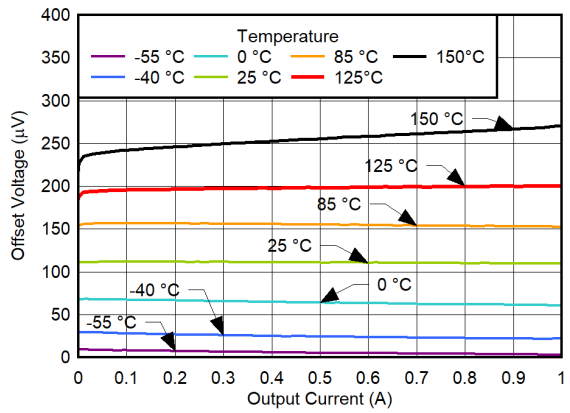

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-52. $V_{OS}$ vs $V_{NR/SS}$ and Temperature**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OUT}$ = 0.7 V

**图 6-53. $I_{NR/SS}$ vs $I_{OUT}$ and Temperature for $V_{IN}$ = 1.2 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OUT}$ = 0.7 V

**图 6-54. $V_{OS}$ vs $I_{OUT}$ and Temperature for $V_{IN}$ = 1.2 V**

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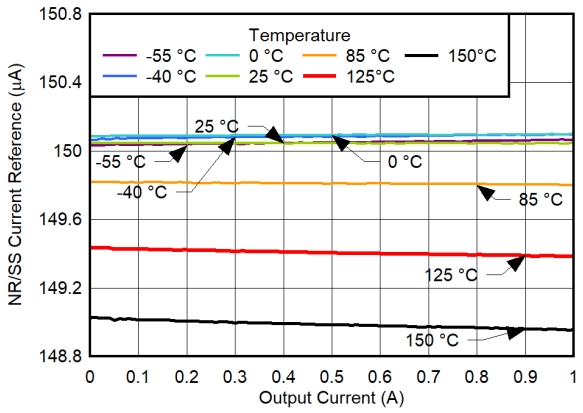
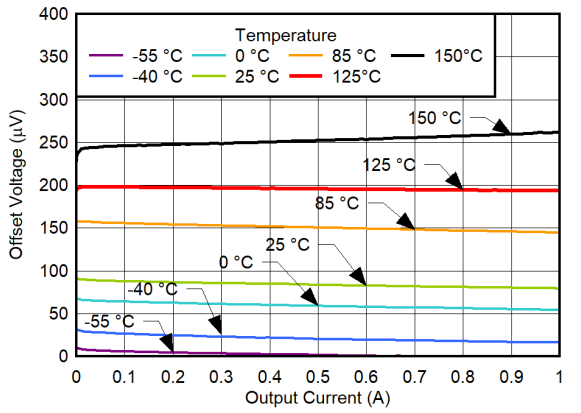
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



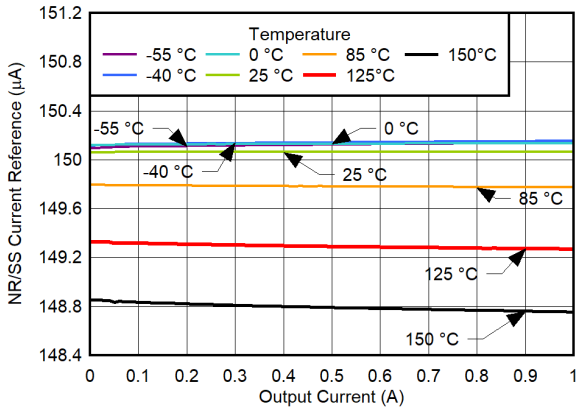

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OpHr}$ = 500 mV

**图 6-55. $I_{NR/SS}$ vs $I_{OUT}$ and Temperature for $V_{IN}$ = 1.8 V**



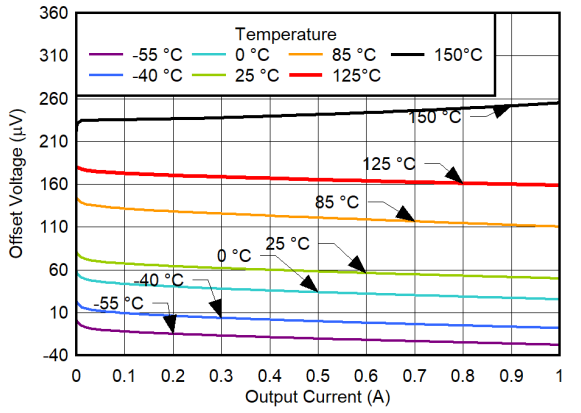

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OpHr}$ = 500 mV

**图 6-56. $V_{OS}$ vs $I_{OUT}$ and Temperature for $V_{IN}$ = 1.8 V**



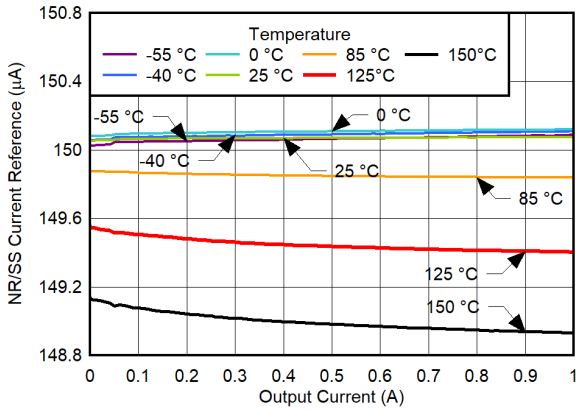

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OpHr}$ = 500 mV

**图 6-57. $I_{NR/SS}$ vs $I_{OUT}$ and Temperature for $V_{IN}$ = 3.3 V**



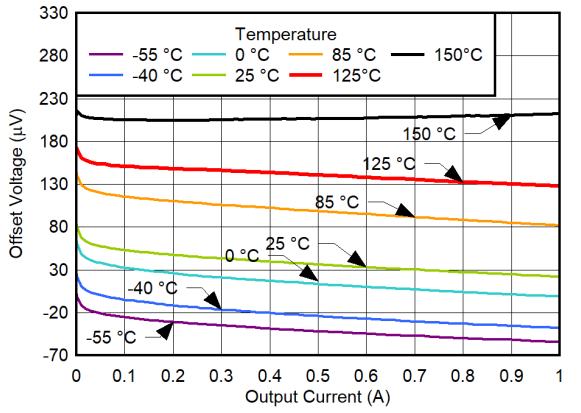

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OpHr}$ = 500 mV

**图 6-58. $V_{OS}$ vs $I_{OUT}$ and Temperature for $V_{IN}$ = 3.3 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OpHr}$ = 500 mV

**图 6-59. $I_{NR/SS}$ vs $I_{OUT}$ and Temperature for $V_{IN}$ = 5.1 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OpHr}$ = 500 mV

**图 6-60. $V_{OS}$ vs $I_{OUT}$ and Temperature for $V_{IN}$ = 5.1 V**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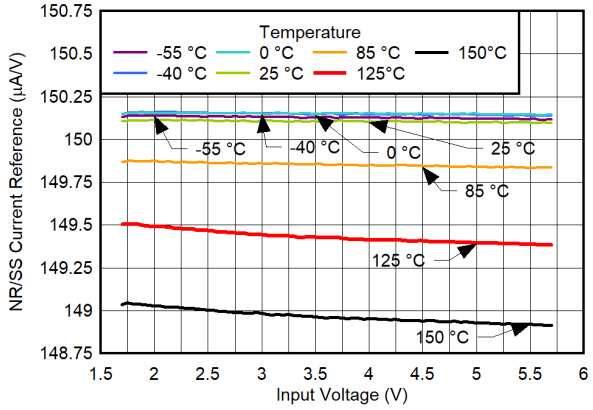
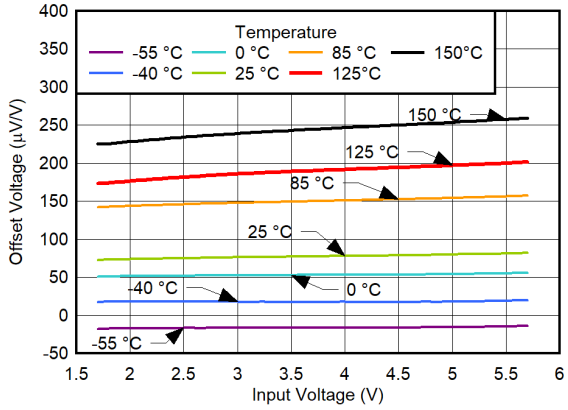
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



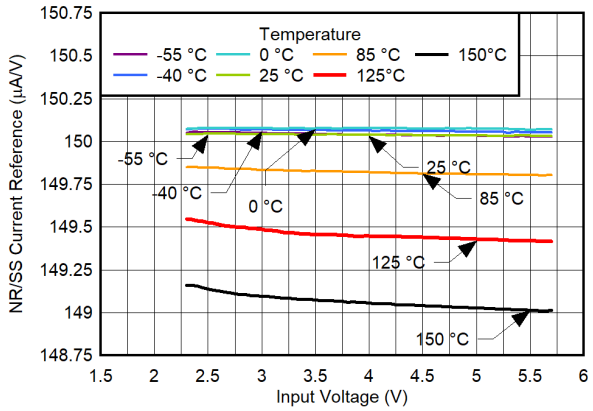

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-61. $I_{NR/SS}$ vs $V_{IN}$ and Temperature for $V_{OUT}$ = 1.2 V**



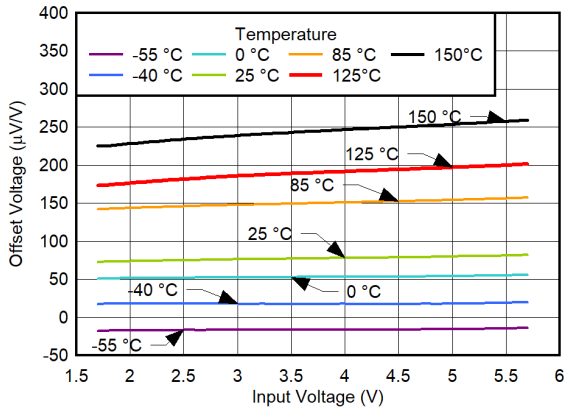

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-62. $V_{OS}$ vs $V_{IN}$ and Temperature for $V_{OUT}$ = 1.2 V**



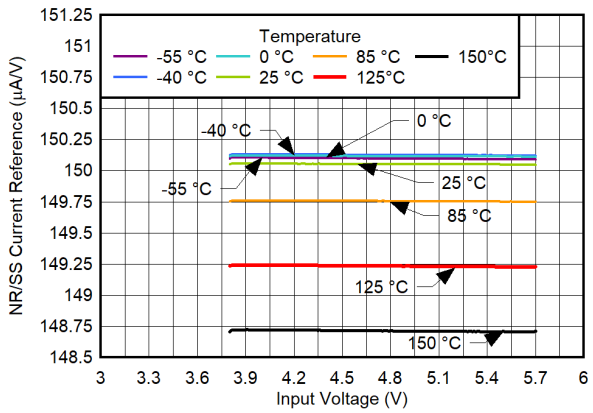

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-63. $I_{NR/SS}$ vs $V_{IN}$ and Temperature for $V_{OUT}$ = 1.8 V**



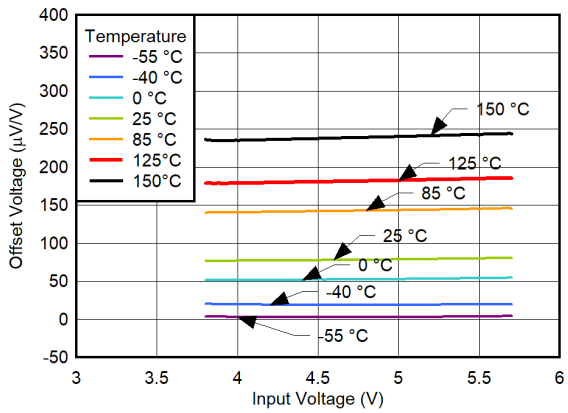

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-64. $V_{OS}$ vs $V_{IN}$ and Temperature for $V_{OUT}$ = 1.8 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-65. $I_{NR/SS}$ vs $V_{IN}$ and Temperature for $V_{OUT}$ = 3.3 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-66. $V_{OS}$ vs $V_{IN}$ and Temperature for $V_{OUT}$ = 3.3 V**

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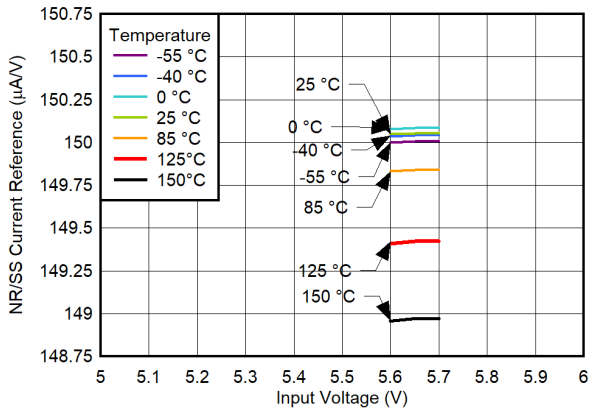
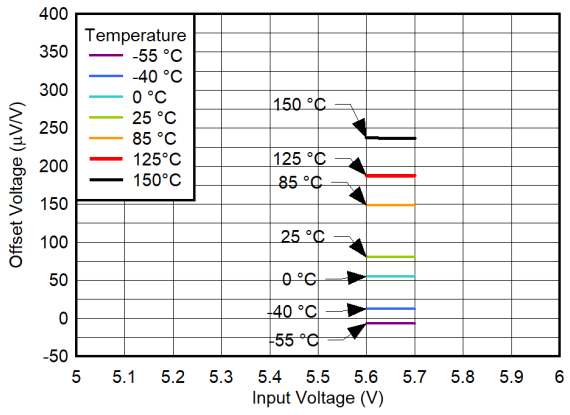
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



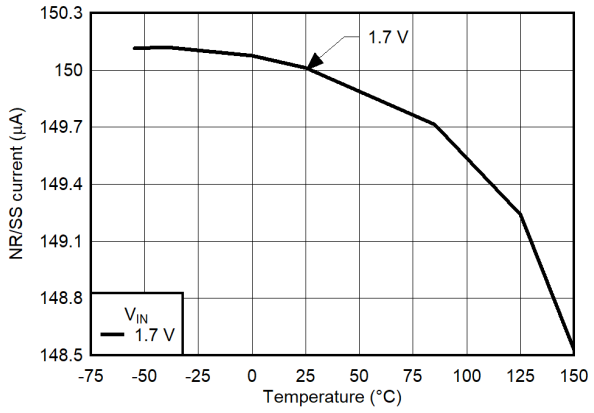

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-67. $I_{NR/SS}$ vs $V_{IN}$ and Temperature for $V_{OUT}$ = 5.1 V**



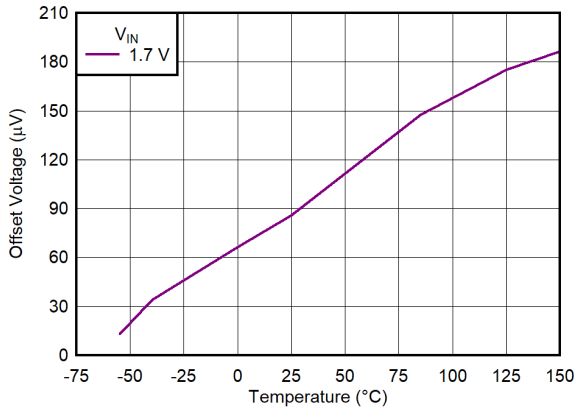

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-68. $V_{OS}$ vs $V_{IN}$ and Temperature for $V_{OUT}$ = 5.1 V**



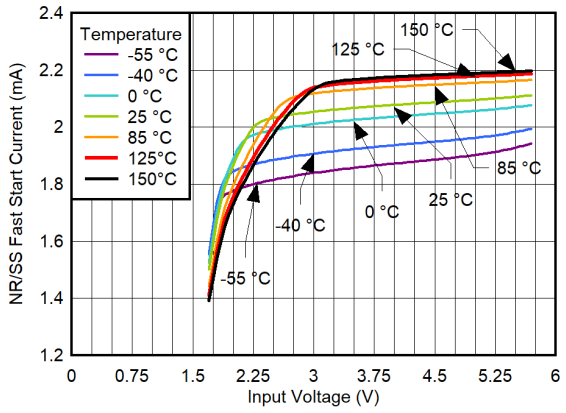

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-69. $I_{NR/SS}$ vs Temperature for $V_{IN_Min}$, $V_{OpHr}$ = 0.2 V**



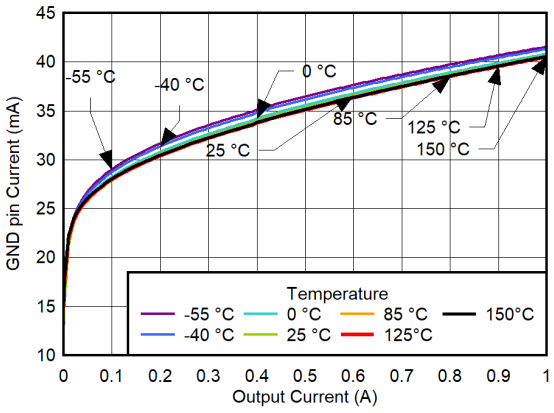

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-70. $V_{OS}$ vs Temperature for $V_{IN_Min}$, $V_{OpHr}$ = 0.2 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 1 mA

**图 6-71. $I_{NR/SS}$ Fast-Start vs $V_{IN}$ and Temperature**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 1.7 V

**图 6-72. GND Pin Current vs $I_{OUT}$ and Temperature for $V_{OUT}$ = 1.2 V**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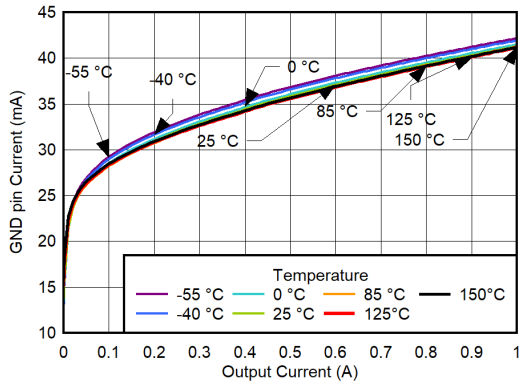
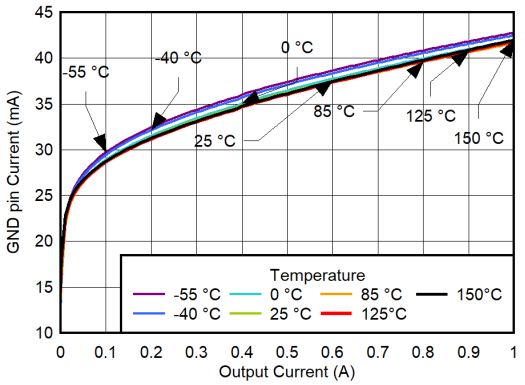
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



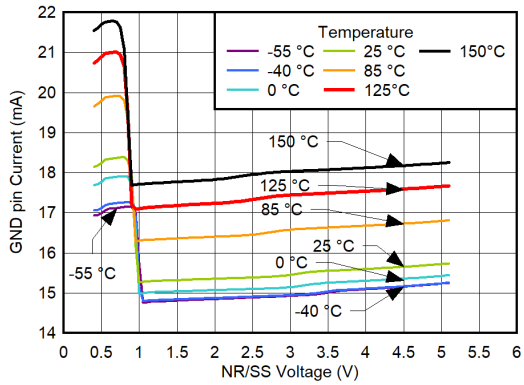

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 3.8 V

**图 6-73. GND Pin Current vs $I_{OUT}$ and Temperature for $V_{OUT}$ = 3.3 V**



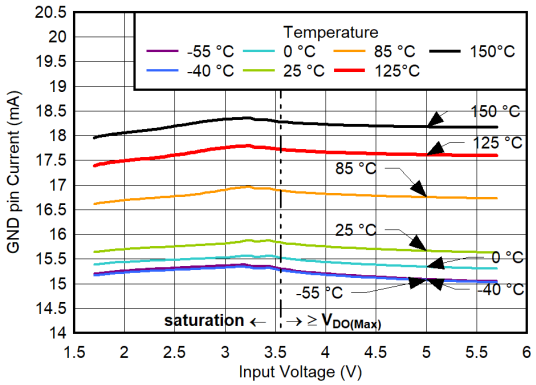

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 5.6 V

**图 6-74. GND Pin Current vs $I_{OUT}$ and Temperature for $V_{OUT}$ = 5.1 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{IN}$ = 5.7 V, $I_{OUT}$ = 1 mA

**图 6-75. GND Pin Current vs $V_{NR/SS}$ and Temperature**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OpHr}$ = 500 mV

**图 6-76. GND Pin Current vs $V_{IN}$ and Temperature for $I_{OUT}$ = 1 mA**

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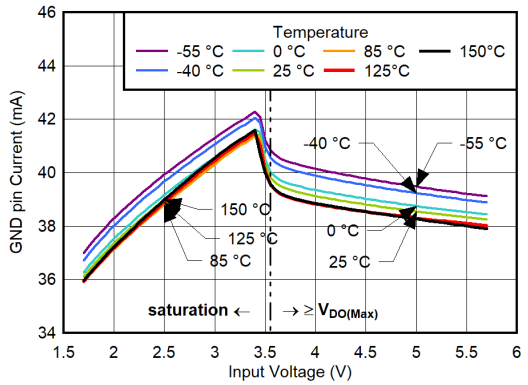
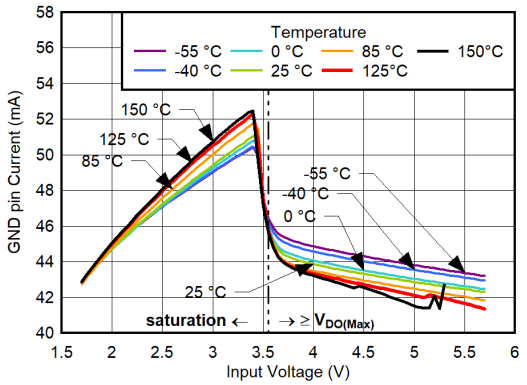
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



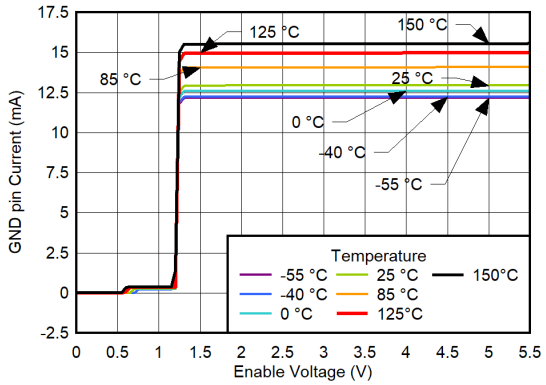

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OUT}$ = $V_{IN}$ – 0.5 V

**图 6-77. GND Pin Current vs $V_{IN}$ and Temperature for $I_{OUT}$ = 500 mA**



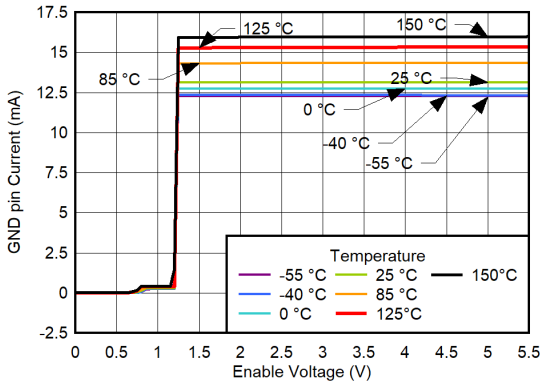

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $V_{OUT}$ = $V_{IN}$ – 0.5 V

**图 6-78. GND Pin Current vs $V_{IN}$ and Temperature for $I_{OUT}$ = 1 A**



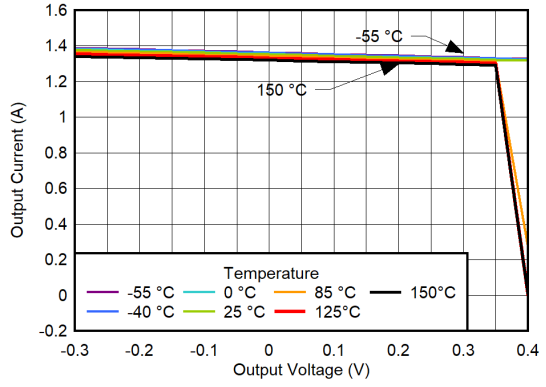

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA, $V_{OUT}$ = 3.3 V

**图 6-79. GND Pin Current vs $V_{EN}$ and Temperature for $V_{IN}$ = 1.7 V (Dropout Operation)**



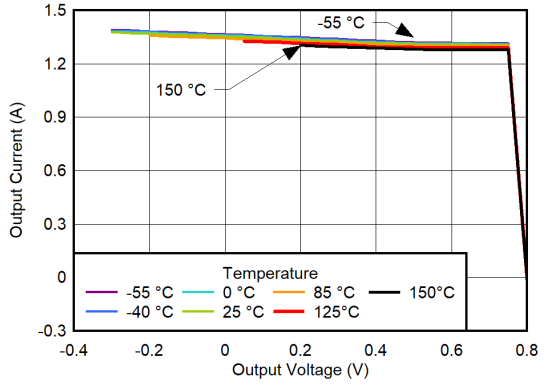

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA, $V_{OUT}$ = 3.3 V

**图 6-80. GND Pin Current vs $V_{EN}$ and Temperature for $V_{IN}$ = 5.7 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-81. 100% Current Limit vs Temperature for $V_{OUT}$ = 0.4 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-82. 100% Current Limit vs Temperature for $V_{OUT}$ = 0.8 V**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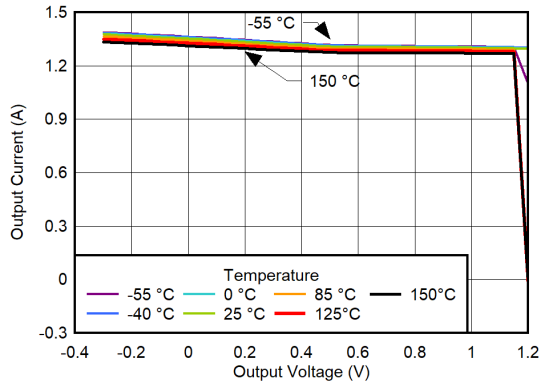
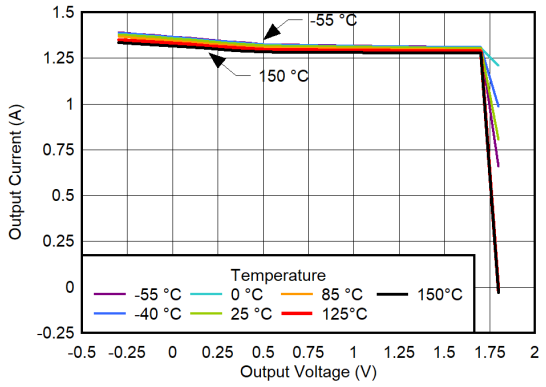
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



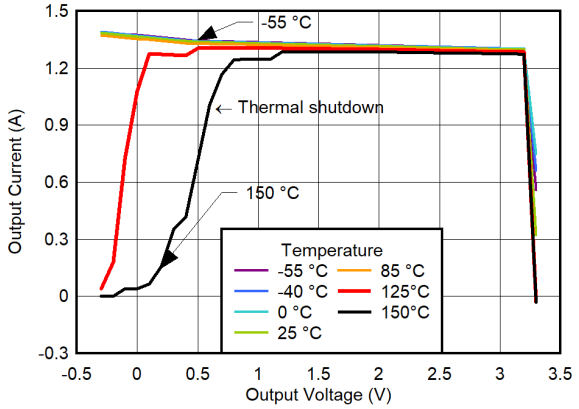

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-83. 100% Current Limit vs Temperature for $V_{OUT}$ = 1.2 V**



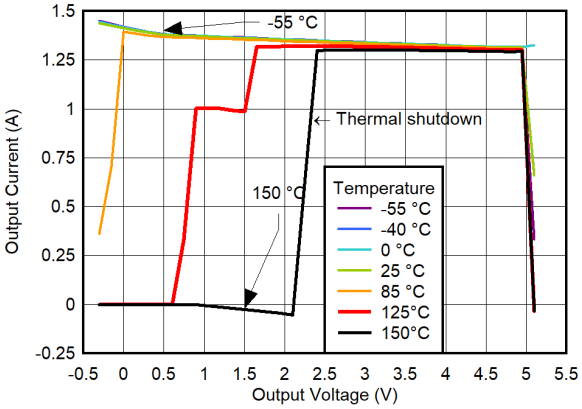

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-84. 100% Current Limit vs Temperature for $V_{OUT}$ = 1.8 V**



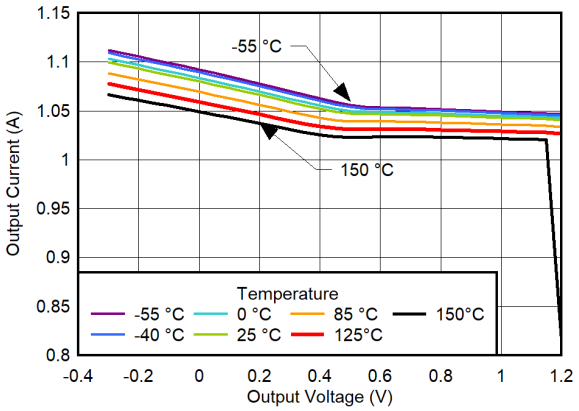

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-85. 100% Current Limit vs Temperature for $V_{OUT}$ = 3.3 V**



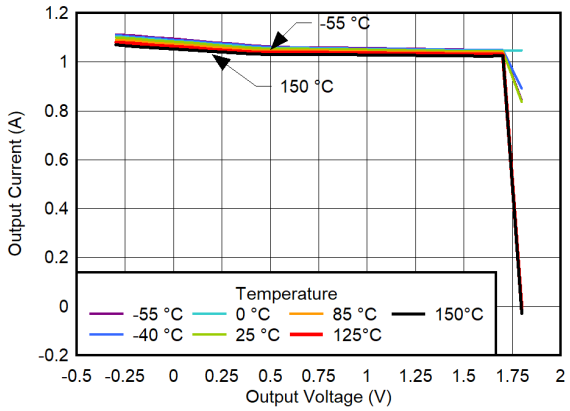

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-86. 100% Current Limit vs Temperature for $V_{OUT}$ = 5.1 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-87. 80% Current Limit vs Temperature for $V_{OUT}$ = 1.2 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-88. 80% Current Limit vs Temperature for $V_{OUT}$ = 1.8 V**

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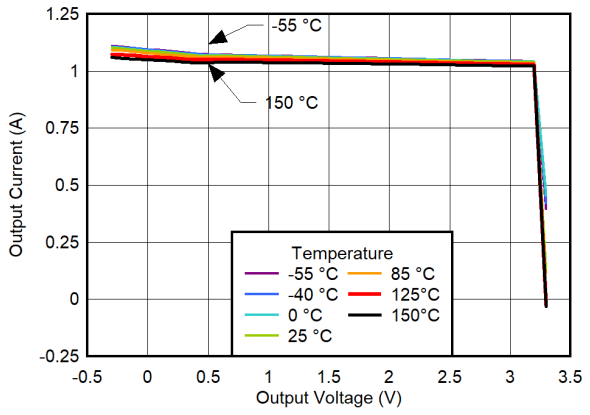
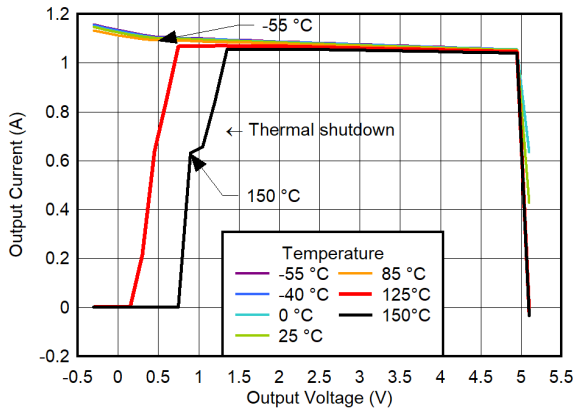
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



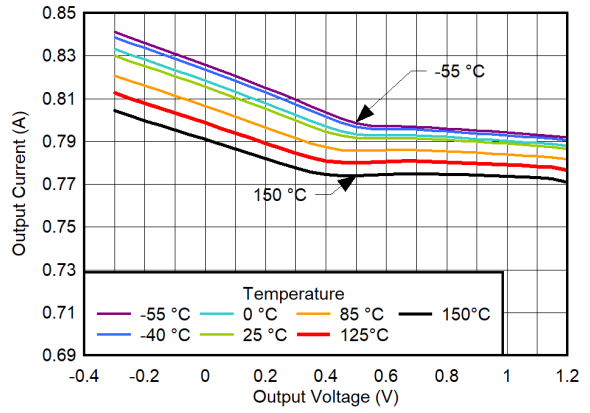

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-89. 80% Current Limit vs Temperature for $V_{OUT}$ = 3.3 V**



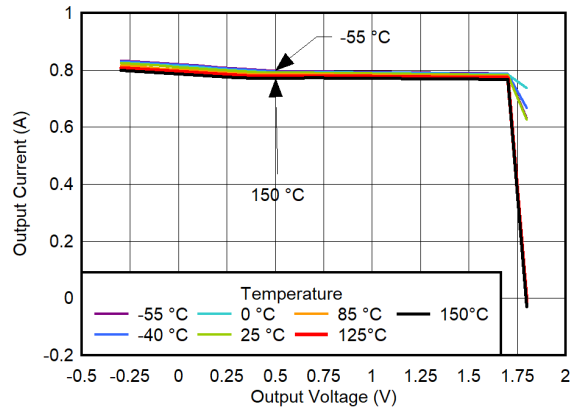

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-90. 80% Current Limit vs Temperature for $V_{OUT}$ = 5.1 V**



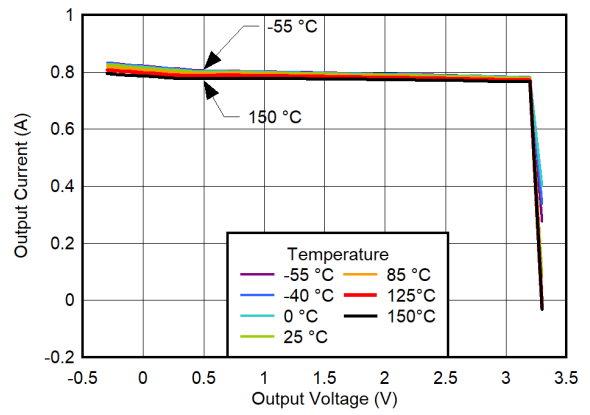

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-91. 60% Current Limit vs Temperature for $V_{OUT}$ = 1.2 V**



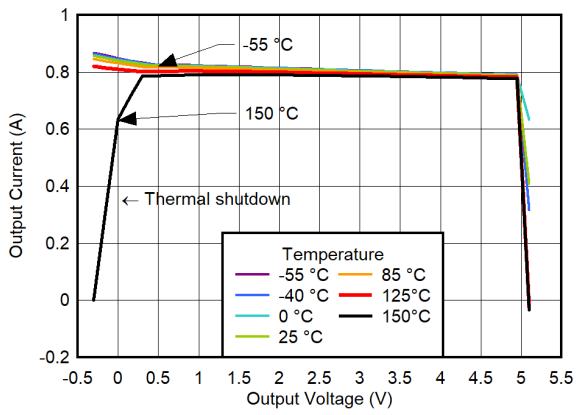

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-92. 60% Current Limit vs Temperature for $V_{OUT}$ = 1.8 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-93. 60% Current Limit vs Temperature for $V_{OUT}$ = 3.3 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF

**图 6-94. 60% Current Limit vs Temperature for $V_{OUT}$ = 5.1 V**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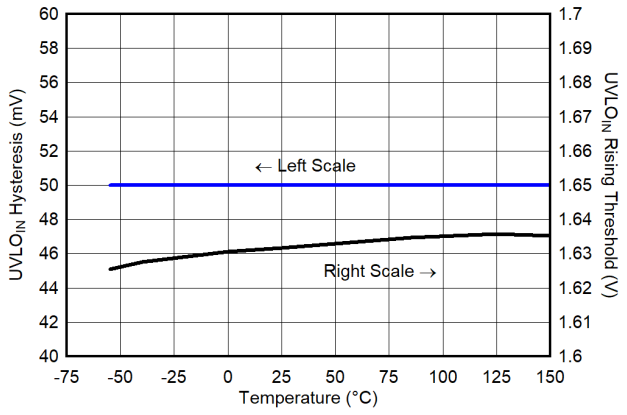
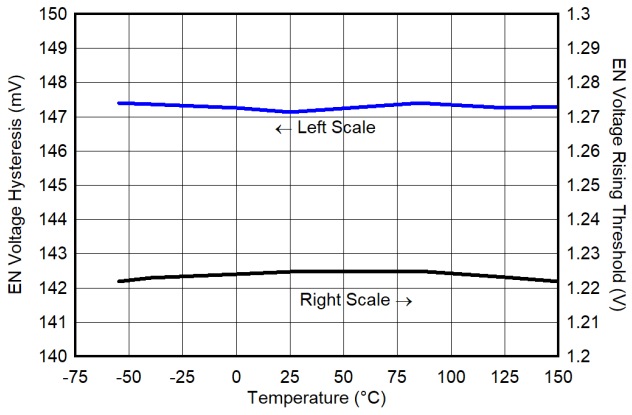
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



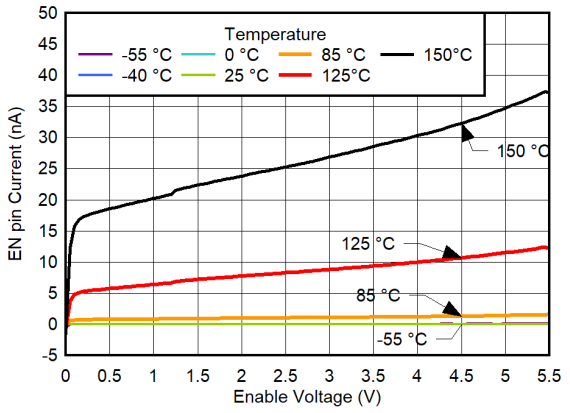

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA

**图 6-95. $UVLO_{IN}$ vs Temperature**



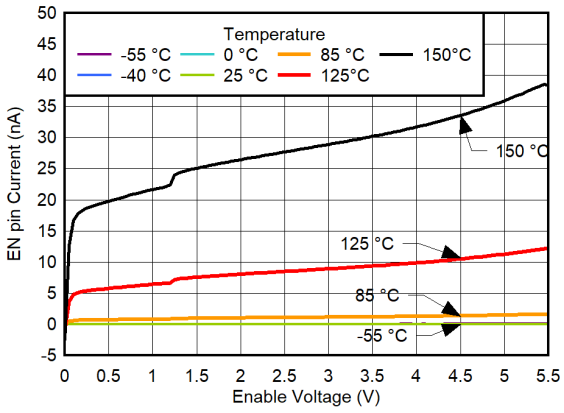

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA

**图 6-96. $V_{EN}$ Hysteresis and Threshold vs Temperature**



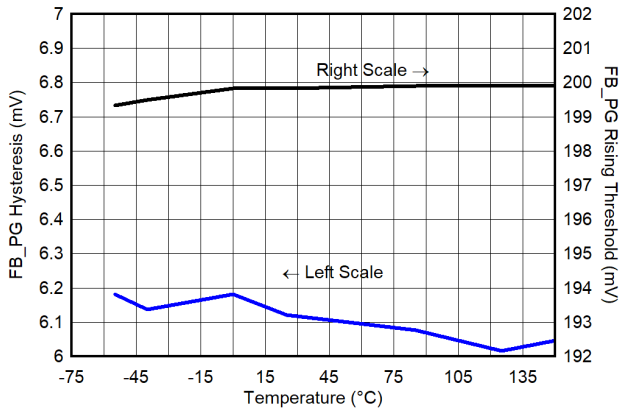

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA

**图 6-97. EN Pin Current vs Enable Voltage and Temperature for $V_{IN}$ = 1.7 V**



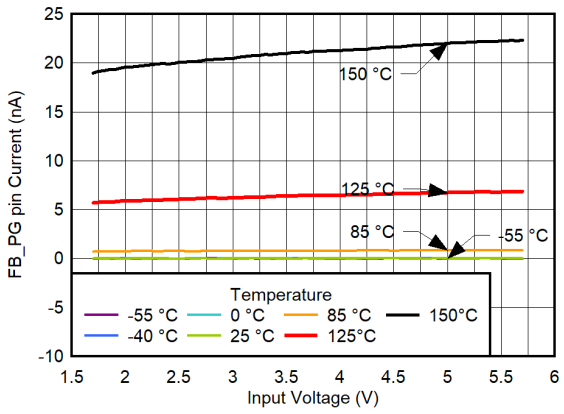

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA

**图 6-98. EN Pin Current vs Enable Voltage and Temperature for $V_{IN}$ = 5.7 V**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA

**图 6-99. $V_{FB_PG}$ Hysteresis and Threshold vs Temperature**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA

**图 6-100. FB_PG Pin Current vs $V_{IN}$ and Temperature**

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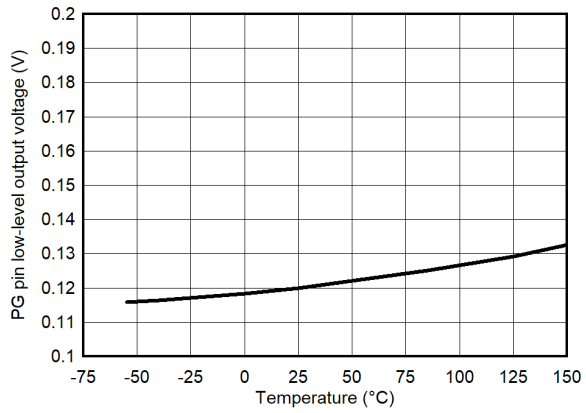
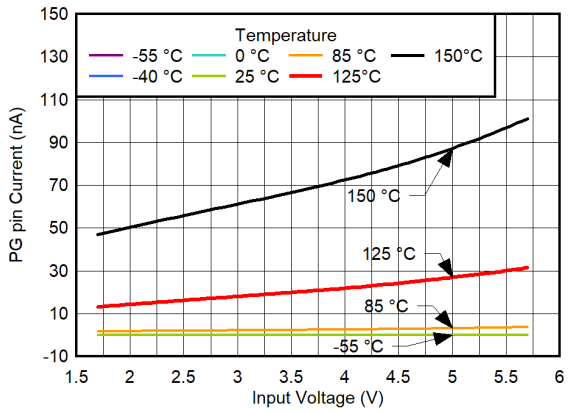
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C



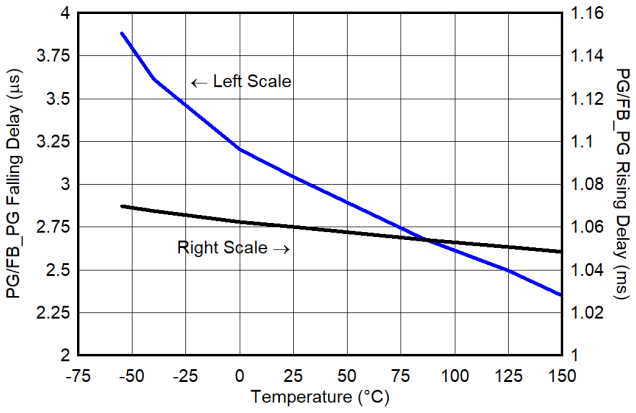

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{PG}$ = –1 mA, $V_{IN}$ = 1.7 V, $I_{OUT}$ = –1 mA

**图 6-101. $V_{PG}$ Low-Level Output Voltage vs Temperature**



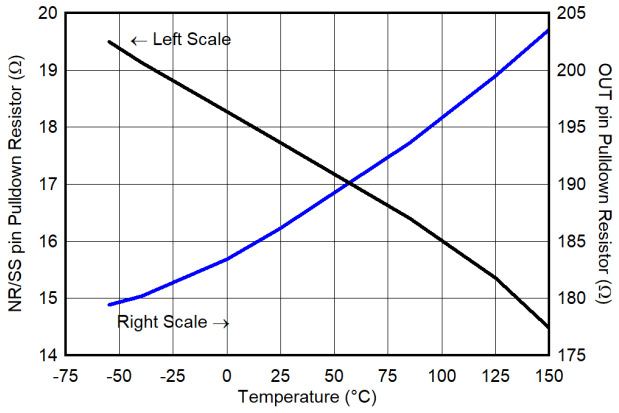

$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA

**图 6-102. PG Pin Current vs $V_{IN}$ and Temperature**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA

**图 6-103. FB_PG to PG Pin Rising and Falling Delay vs Temperature**




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA

**图 6-104. NR/SS and OUT Pulldown Resistors vs Temperature**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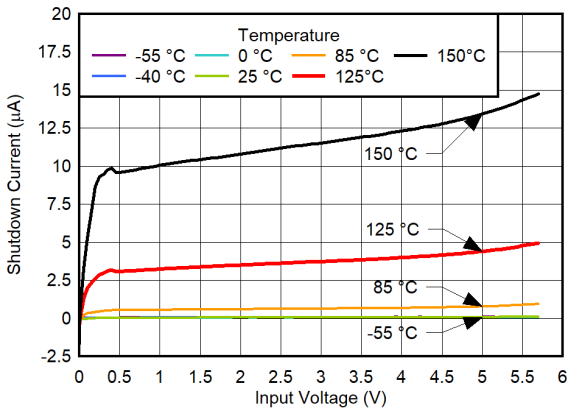
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{EN}$ = 1.8 V, $C_{IN}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $C_{OUT}$ = 10 µF, and $I_{OUT}$ = 1 mA (unless otherwise noted); typical values are at $T_J$ = 25°C




$C_{IN}$ = $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 4.7 µF, $I_{OUT}$ = 0 mA

**图 6-105. Shutdown Current vs $V_{IN}$ and Temperature**

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# 7 Detailed Description

## 7.1 Overview

The TPS7A94 is an ultra-low-noise (0.46 μ$V_{RMS}$ over 10-Hz to 100-kHz bandwidth), ultra-high PSRR (> 50 dB to 2 MHz), high-accuracy (1%), low-dropout (LDO) linear voltage regulator with an input range of 1.7 V to 5.7 V and an output voltage range from 0 V to $V_{IN}$ – $V_{DO}$ and is fully specified above 0.4 $V_{OUT}$. This LDO regulator uses innovative circuitry to achieve wide bandwidth and high loop gain, resulting in ultra-high PSRR even when operating under very low operational headroom ($V_{IN}$ – $V_{OUT}$). At a high level, the device has two main blocks (the current reference and the unity-gain LDO buffer) and a few secondary features (such as the precision enable, current limit, and PG pin).

The current reference is controlled by the NR/SS pin. This pin sets the output voltage with a single resistor, sets the start-up time, and filters the noise generated by the reference and external set resistor.

The unity-gain LDO buffer is controlled by the OUT pin. The ultra-low-noise does not increase with output voltage and provides wideband PSRR. As such, the SNS pin is only used for remote sensing of the load.

The EN_UV pin sets the precision enable feature. Select the optimal input voltage at which the LDO starts at. There are two independent UVLO voltages in this device: the internal IN rail UVLO and the EN_UV pin.

The FB_PG pin sets the current limit and power-good (PG) features. A voltage divider on this pin programs both the current limit and the PG trip point.

An ultra-low-noise current reference (150 μA, typical) is used in conjunction with an external resistor ($R_{NR/SS}$) to set the output voltage. This process allows the output voltage range to be set from 0.4 V to ($V_{IN}$ – $V_{DO}$). To achieve this ultra-low noise, an external capacitor $C_{NR/SS}$ (typically 4.7 μF) is placed in parallel to the $R_{NR/SS}$ resistor used to set the output voltage. The unity-gain architecture provides ultra-high PSRR over a wide frequency range without compromising load and line transients.

This regulator offers programmable current-limit, thermal protection, is fully specified from –40°C to +125°C above 0.4 $V_{OUT}$, and is offered in a thermally efficient 10-pin, 3-mm × 3-mm WSON package.


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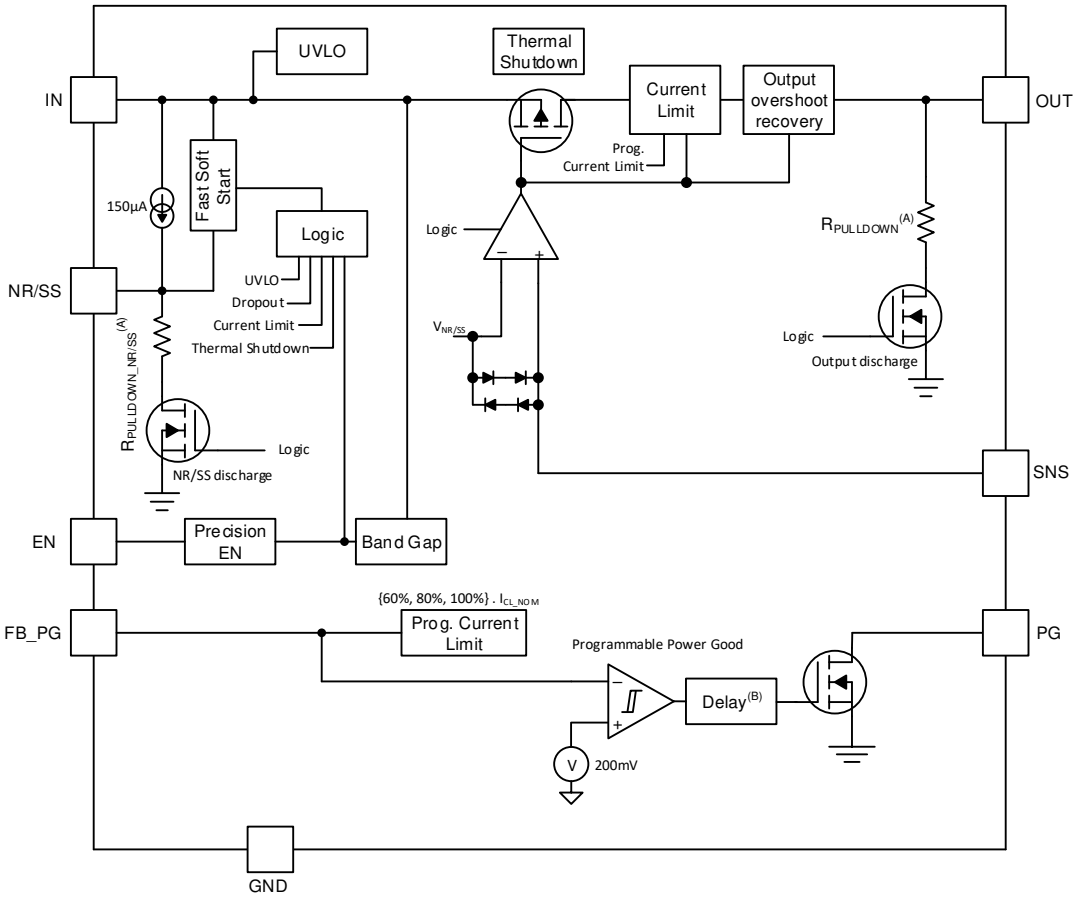
## 7.2 Functional Block Diagram

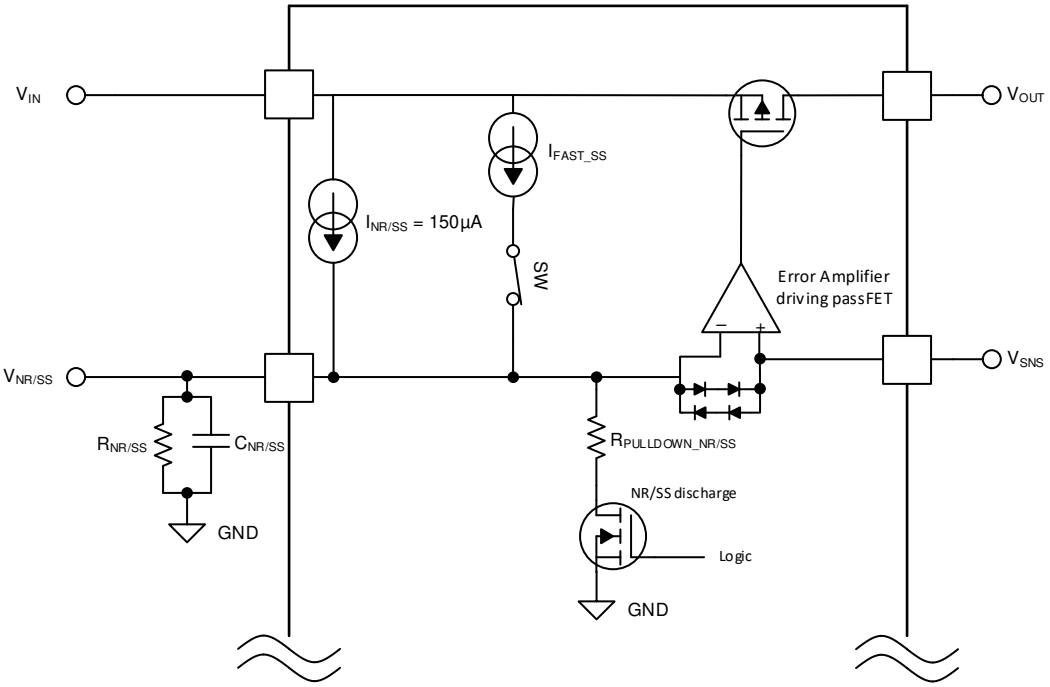



A. See the $R_{PULLDOWN}$ output active discharge resistance value in the *Electrical Characteristics* table.
B. See the delay value in the *Electrical Characteristics* table.

## 7.3 Feature Description

### 7.3.1 Output Voltage Setting and Regulation

图 7-1 shows a simplified regulation circuit, where the input signal ($V_{NR/SS}$) is generated by the internal current source ($I_{NR/SS}$) and the external resistor ($R_{NR/SS}$). Because the error amplifier is always operating in unity-gain configuration, the LDO output voltage is directly programmed by the $V_{NR/SS}$ voltage. The $V_{NR/SS}$ reference voltage is generated by an internal low-noise current source driving the $R_{NR/SS}$ resistor and is designed to have very low bandwidth at the input to the error amplifier through the use of a low-pass filter ($C_{NR/SS}$ || $R_{NR/SS}$).




$V_{OUT} = I_{NR/SS} \times R_{NR/SS}$.

**图 7-1. Simplified Regulation Circuit**

This unity-gain configuration, along with the highly accurate $I_{NR/SS}$ reference current, enables the device to achieve excellent output voltage accuracy; though, the $R_{NR/SS}$ accuracy can become the limiting factor when operating at low output voltage. The low dropout voltage ($V_{DO}$) enables reduced thermal dissipation and achieves robust performance. This combination of features makes this device an excellent voltage source for powering sensitive analog low-voltage devices.

### 7.3.2 Ultra-Low Noise and Ultra-High Power-Supply Rejection Ratio (PSRR)

The architecture features a highly accurate, high-precision, low-noise current reference followed by a state-of-the-art error amplifier (1.1 nV/ $\sqrt{\text{Hz}}$ at 10-kHz noise for $V_{OUT} \geqslant 1.2$ V) comparable to, if not better than, that of a precision amplifier. The unity-gain configuration ensures ultra-low noise over the entire output voltage range. Additional noise reduction and higher output current can be achieved by placing multiple TPS7A94 LDOs in parallel.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### 7.3.3 Programmable Current Limit and Power-Good Threshold

The brick-wall current limit can be programmed to either 100%, 80%, or 60% of the nominal factory-programmed value by setting the input impedance for the FB_PG pin. Similarly, the power-good indication threshold can also be adjusted between 85% and 95% of the nominal output voltage by changing the FB_PG resistor divider ratio; see the *Adjusting the Factory-Programmed Current Limit* section for details.

### 7.3.4 Programmable Soft Start (NR/SS Pin)

The device features a programmable, monotonic, voltage-controlled, soft-start circuit that uses the $C_{NR/SS}$ capacitor to minimize inrush current into the output capacitor and load during start up. This circuitry can also reduce the start-up time for some applications that require the output voltage to reach at least 90% of the set value for fast system start up. See the *Programmable Soft-Start and Noise-Reduction (NR/SS Pin)* section for more details.

### 7.3.5 Precision Enable and UVLO

Two independent UVLO (undervoltage lockout) voltage circuits are present. An internally set UVLO on the input supply (IN pin) automatically disables the LDO when the input voltage reaches the minimum threshold. A precision EN function (EN_UV pin) can also be used as a user-programmable UVLO.

1. The input supply voltage undervoltage lockout (UVLO) circuit prevents the regulator from turning on when the input voltage is not high enough, see the *Electrical Characteristics* table for more details.
2. The precision enable circuit allows a simple sequencing of multiple power supplies with a resistor divider from another supply. This enable circuit can be used to set an external UVLO voltage at which the device is enabled using a resistor divider on the EN_UV pin; see the *Precision Enable (External UVLO)* section for more details.

### 7.3.6 Active Discharge

The device incorporates two internal pulldown metal-oxide semiconductor field effect transistors (MOSFETs). The first pulldown MOSFET connects a resistor ($R_{PULLDOWN}$) from OUT to ground when the device is disabled to actively discharge the output capacitor. The second pulldown MOSFET connects a resistor ($R_{PULLDOWN_NR/SS}$) from NR/SS to ground when the device is disabled and discharges the NR/SS capacitor. Both pulldown MOSFETs are activated by any one or more of the following:

1. Driving the EN_UV pin below the $V_{EN(LOW)}$ threshold
2. The IN pin voltage falling below the undervoltage lockout $V_{UVLO}$ threshold
3. Having the output voltage greater than the input voltage

### 7.3.7 Thermal Shutdown Protection ($T_{SD}$)

A thermal shutdown protection circuit disables the LDO when the junction temperature ($T_J$ ) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical). The thermal time constant of the semiconductor die is fairly short, thus the device can cycle off and on when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large $V_{IN}$ – $V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors.

Under some conditions, the thermal shutdown protection can disable the device before start up completes. For reliable operation, limit the junction temperature to the maximum listed in the *Electrical Characteristics* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

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## 7.4 Device Functional Modes

表 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**表 7-1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN_UV}$ | $I_{OUT}$ | $T_J$ |
| Normal operation | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$ | $V_{EN_UV} > V_{IH(EN_UV)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < TSD_{(shutdown)}$ |
| Dropout operation | $V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN_UV} > V_{IH(EN_UV)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < TSD_{(shutdown)}$ |
| Disabled (any true condition disables the device) | $V_{IN} < V_{UVLO}$ or $V_{IN} < V_{OUT} + 90$ mV or $V_{IN} < V_{NR/SS} + 20$ mV | $V_{EN_UV} < V_{IL(EN_UV)}$ | Not applicable | $T_J > TSD_{(shutdown)}$ |
| Current-limit operation | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$ | $V_{EN_UV} > V_{IH(EN_UV)}$ | $I_{OUT} \geqslant I_{CL(min)}$ | $T_J < TSD_{(shutdown)}$ |

### 7.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < TSD_{(shutdown)}$)
- The voltage on the EN_UV pin has previously exceeded the $V_{IH(EN_UV)}$ threshold voltage and has not yet decreased to less than the $V_{IL(EN_UV)}$ falling threshold

### 7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

**备注**

While in dropout, if a heavy load transient event forces $V_{IN} < V_{OUT(NOM)} + 90$ mV or $V_{IN} < V_{NR/SS} + 20$ mV, the device restarts to prevent the output voltage from overshooting to protect the device and load.

When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

For additional information, see the *Output Voltage Restart (Overshoot Prevention Circuit)* section.

### 7.4.3 Disabled

The output of the device can be shutdown by forcing the voltage of the EN_UV pin to less than the $V_{IL(EN_UV)}$ threshold (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and both the NR/SS pin and OUT pin voltages are actively discharged to ground by internal discharge circuits to ground when the IN pin voltage is higher than or equal to a diode-drop voltage.

### 7.4.4 Current-Limit Operation

If the output current is greater than or equal to the minimum current limit, ($I_{CL(Min)}$), then the device is operating in current-limit mode. The current limit is brick-wall and is programmable with the PG_FB pin. For additional information, see the *Adjusting the Factory-Programmed Current Limit* section.


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# 8 Application and Implementation

**备注**

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## 8.1 Application Information

Successfully implementing a low-dropout regulator (LDO) in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

### 8.1.1 Output Voltage Restart (Overshoot Prevention Circuit)

Wide bandwidth linear regulators suffer from an undesirable excessive overshooting of the output voltage during restart events that occur when the $C_{NR/SS}$ and $C_{OUT}$ capacitors are not fully discharged. In this device, and as shown in 图 8-1, this undesirable behavior is mitigated by implementing low hysteresis circuitry consisting of two ORed comparators to detect when the input voltage is either 20 mV (typical) lower than the $V_{NR/SS}$ reference voltage or 300 mV (typical) lower than $V_{OUT}$.

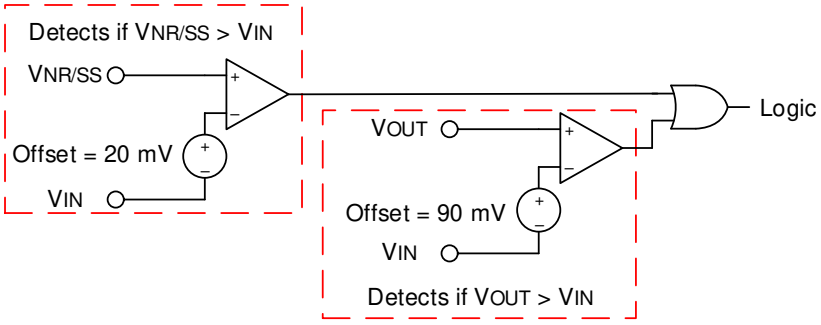


**图 8-1. Overshoot Prevention Circuit**

When the device is operating in dropout, transient events (such as an input voltage brownout, heavy load transient, or short-circuit event) can force the device in a reversed bias condition where the input voltage is either 20 mV (typical) lower than the $V_{NR/SS}$ reference voltage or 300 mV (typical) lower than $V_{OUT}$. The output overshoot prevention circuit can be triggered, as shown in 图 8-2, thus forcing the device to shutdown and restart, thereby preventing output voltage overshoot. If the device is still operating in dropout and the error condition that triggered this circuit is still present, an additional restart can occur until these conditions are removed or the device is no longer in dropout. The restart always occurs from a discharged state and always has the same characteristics as the initial LDO power-up, so the start-up time, $V_{OUT}$ ramp rate, and $V_{OUT}$ monotonicity are all predictable.

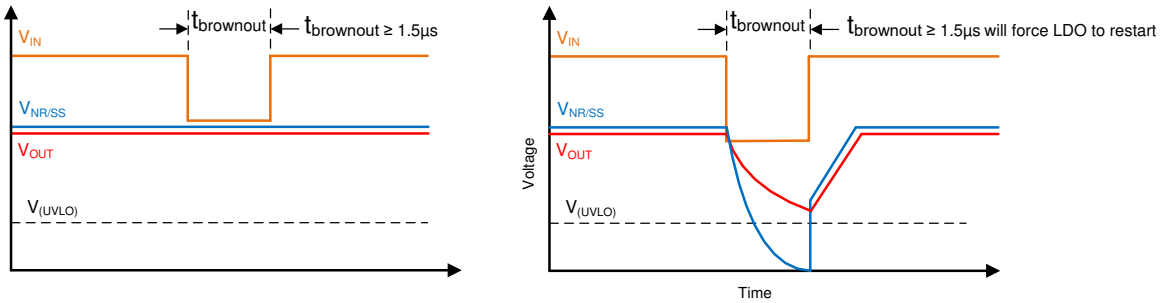


**图 8-2. Device Behavior in Dropout**

图 8-3 and 图 8-4 show examples of a soft brownout and a brownout event, respectively.

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The brownout overshoot is present with higher $V_{IN}$ slew rates. A 1-V/ μ s slew rate was used in 图 8-5.

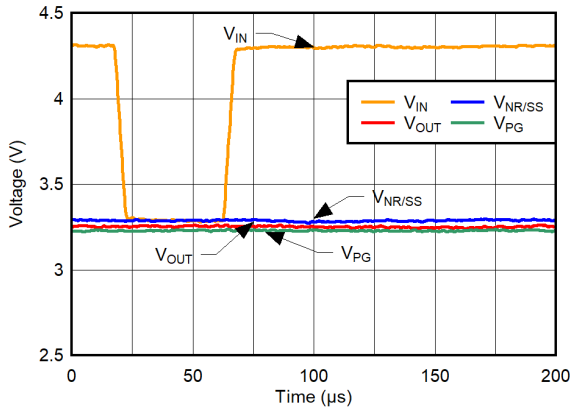


图 8-3. Example: Soft Brownout to $V_{NR/SS}$

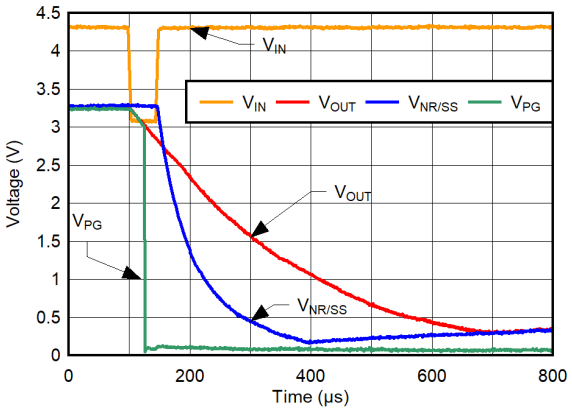


图 8-4. Example: Brownout

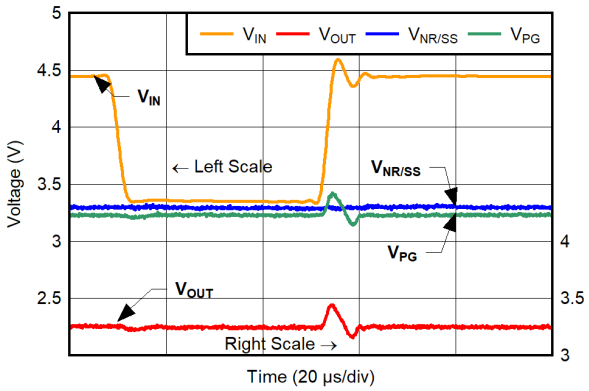


图 8-5. Example: Brownout With Overshoot Recovery

The overshoot prevention circuit is implemented to provide a predictable start-up and shutdown of the device without output overshoot if the EN_UV external UVLO is not used as described in this section. This circuit can be prevented from triggering by:

1. Using an input supply capable of handling heavy load transients or a larger value input capacitor
2. Increasing the operating headroom between $V_{IN}$ and $V_{OUT}$ (for example, when using a battery as an input supply to make sure that $V_{IN}$ stays higher than $V_{OUT}$ even when the battery is near the full discharge state)
3. Using an input supply with a ramp rate faster than the set output voltage time constant formed by $C_{NR/SS}$ || $R_{NR/SS}$
4. Discharging the input supply slower than the discharge time formed by $C_{OUT}$ || (Load || $R_{PULLDOWN}$) or by the $C_{NR/SS}$ || ($R_{NR/SS}$ || $R_{PULLDOWN_NR/SS}$)

### 8.1.2 Precision Enable (External UVLO)

The precision enable circuit is used to turn the device on and off. This circuit can be used to set an external undervoltage lockout (UVLO) voltage (see 图 8-6) to turn on and off the device using a resistor divider between IN, EN_UV, and GND.

If $V_{EN_UV} \geqslant V_{IH(EN_UV)}$, the regulator is enabled. If $V_{EN_UV} \leqslant V_{IL(EN_UV)}$, the regulator is disabled. The EN_UV pin does not incorporate an internal pulldown resistor to GND and must not be left floating. Use the precision enable circuit for this pin to set an external undervoltage lockout (UVLO) input supply voltage to turn on and off the device using a resistor divider between IN, EN_UV, and GND.


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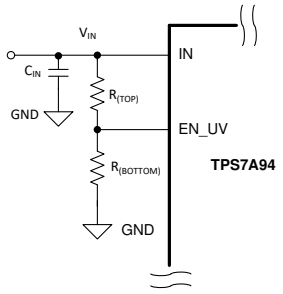


**图 8-6. Precision EN Used as External UVLO**

This external UVLO configuration prevents the LDO from turning on when the input supply voltage is insufficient and places the device in dropout operation.

Using the EN_UV pin as an externally set UVLO allows simple sequencing of cascaded power supplies. An additional benefit is that the EN_UV pin is never left floating. The EN_UV pin does not have an internal pulldown resistor. In addition to the resistor divider, a zener diode can be needed between the EN_UV pin and ground to comply with the absolute maximum ratings on this pin.

When $V_{IN}$ exceeds the targeted $V_{ON}$ voltage and the $R_{(BOTTOM)}$ resistor is set, 方程式 1 and 方程式 2 provide the $R_{(TOP)}$ resistor value and the $V_{OFF}$ voltage at which the input voltage must drop below to disable the LDO.

$$R_{(TOP)} \leqslant R_{(BOTTOM)} \times (V_{ON} / V_{IH(EN_UV)} - 1) \quad (1)$$

$$V_{OFF} < [1 + R_{(TOP)} / R_{(BOTTOM)}] \times (V_{IH(EN_UV)} - V_{HYS(EN_UV)}) \quad (2)$$

where:

- $V_{OFF}$ is the input voltage where the regulator shuts off
- $V_{ON}$ is the voltage where the regulator turns on

Consider the EN_UV current pin when selecting the $R_{(TOP)}$ and $R_{(BOTTOM)}$ values.

### 8.1.3 Undervoltage Lockout (UVLO) Operation

The UVLO circuit, present on the IN pin, ensures that the device remains disabled before the input supply reaches the minimum operational voltage range, and that the device shuts down when the input supply falls too low.

The $UVLO_{IN}$ circuit has a minimum response time of several microseconds to fully assert. During this time, a downward line transient below approximately 1.6 V causes the input supply UVLO to assert for a short time. However, the $UVLO_{IN}$ circuit can possibly not have enough stored energy to fully discharge the internal circuits inside of the device. When the $UVLO_{IN}$ circuit does not fully discharge, internal circuitry is not fully disabled.

The effect of the downward line transient can trigger the overshoot prevention circuit and can be easily mitigated by using the solution proposed in the *Precision Enable (External UVLO)* section.

图 8-7 illustrates the $UVLO_{IN}$ circuit response to various input voltage events. This diagram can be separated into the following regions:

- Region A: The device does not turn on until the input reaches the UVLO rising threshold.
- Region B: Normal operation with a regulated output.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output can fall out of regulation but the device is still enabled.
- Region D: Normal operation with a regulated output.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached by the input voltage and a normal start up then follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.

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- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

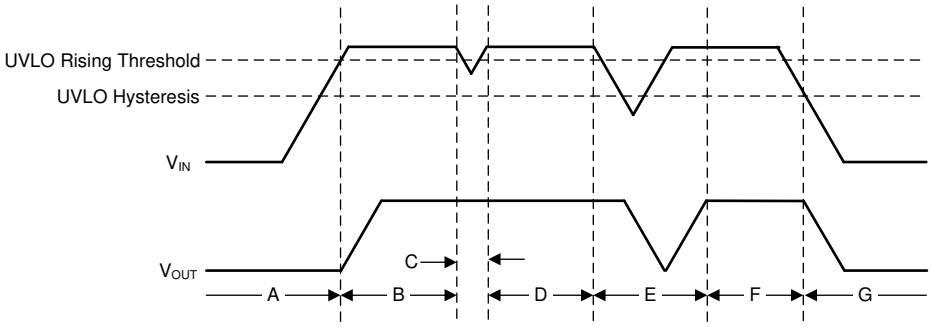


**图 8-7. Typical UVLO Operation**

### 8.1.4 Dropout Voltage ($V_{DO}$)

The dropout voltage refers to the minimum voltage difference between the input and output voltage ($V_{DO}$ = $V_{IN}$ – $V_{OUT}$) that is required for regulation. When the input voltage ($V_{IN}$) drops to or below the maximum dropout voltage ($V_{DO(Max)}$) for the given load current, see the *Electrical Characteristics* table, the device functions as a resistive switch and does not regulate the output voltage. When the device is operating in dropout, the output voltage tracks the input voltage. For high current, the dropout voltage ($V_{DO}$) is proportional to the output current because the device is operating as a resistive switch. For low current, internal nodes are saturating and the dropout plateaus to the minimum value. As mentioned in the *Output Voltage Restart (Overshoot Prevention Circuit)* section, transient events such as an input voltage brownout, heavy load transient, or short-circuit event can trigger the overshoot prevention circuit. Operating the device at or near dropout significantly degrades both transient performance and PSRR, and can also trigger the overshoot prevention circuit. Maintaining sufficient operating headroom ($V_{OpHr}$ = $V_{IN}$ – $V_{OUT}$) significantly improves the device transient performance and PSRR, and prevents triggering the overshoot prevention circuit.

**备注**

For this device, the pass element is not the limiting dropout voltage factor. Because the reference voltage is generated by a current source and the NR/SS resistor, and because the operating headroom is reducing (even at low load), the internal current source ($I_{NR/SS}$) saturates faster than the pass transistor. This behavior is described in the dropout voltage plot (图 6-43). Notice that the dropout does not go to 0 V at light loads.

### 8.1.5 Power-Good Feedback (FB_PG Pin) and Power-Good Threshold (PG Pin)

For proper device operation, the resistor divider network input to the FB_PG pin must be connected. The FB_PG pin must not be left floating because this pin represents an analog input to the device internal logic and the input impedance is sampled during device start up.

The PG pin is an output indicating whether the LDO is ready to provide power. This pin is implemented using an open-drain architecture. The FB_PG pin is used to program the PG pin and serves a dual purpose of programming the PG threshold assert voltage and adjusting the current limit, $I_{CL}$.

The PG pin must use the minimum value or larger pullup resistor from PG to IN, see 图 8-8, or the external rail as listed in the *Electrical Characteristics* table. If PG functionality is not used, leave this pin floating or connected to GND.

The FB_PG pin uses the parallel impedance formed by the resistor divider $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ to program the current limit value during LDO initialization. If this impedance is less than 12.5 kΩ, then the nominal factory-programmed, current-limit value is selected. If the input impedance is less than 50 kΩ, but greater than 12.5 kΩ, then 80% of the nominal factory-programmed current limit is selected. If the input impedance is less


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than 100 kΩ, but greater than 50 kΩ, then 60% of the nominal factory-programmed current limit is selected. Connect the $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ resistors as indicated in this section for proper operation of the LDO. Do not float this pin.

When initialization is complete, the voltage divider provides the necessary feedback to the PG pin by setting the PG assert threshold voltage.

To properly select the values of the $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ resistors, see the *Adjusting the Factory-Programmed Current Limit* section for detailed explanation and calculation.

**备注**

The $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ resistor divider ratio sets the power-good assert threshold voltage between 85% to 95% of the $V_{FB_PG}$ voltage for 60% and 80% of the nominal factory-programmed current limit.

If the current limit is set for 100% of the nominal factory-programmed current limit, the PG threshold range is not limited. A PG threshold greater than 80% is common for system where start-up inrush current must be minimized. Lower PG thresholds can be needed in systems with fast start-up time constraints.

Setting the PG threshold based off the $V_{FB_PG}$ voltage sets the PG to assert when the output voltage reaches the corresponding percentage level of $V_{FB_PG}$ because $V_{FB_PG}$ is a scaled version of the output voltage. 图 8-8 shows the internal circuitry for both the FB_PG and PG pins.

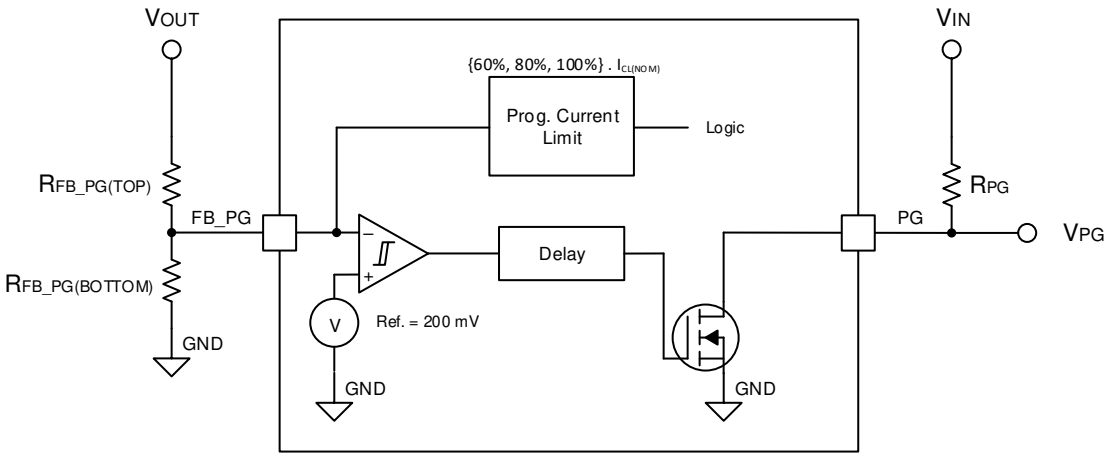


**图 8-8. Programmable Power-Good Threshold Simplified Schematic**

The PG pin pullup resistor value must be between 10 kΩ and 100 kΩ. The lower limit of 10 kΩ results from the maximum pulldown strength of the power-good transistor, and the upper limit of 100 kΩ results from the maximum leakage current at the power-good node. If the pullup resistor is outside of this range, then the power-good signal can possibly not read a valid digital logic level.

The state of the PG signal is only valid when the FB_PG pin resistor divider network is set properly and the device is in normal operating mode.

### 8.1.6 Adjusting the Factory-Programmed Current Limit

The current limit is a brick-wall scheme and the factory-programmed current limit value can be programmed to a set of discrete value (100%, 80%, or 60% of the default value), as specified in the *Electrical Characteristics* table. This adjustment can be done by changing the input impedance of the FB_PG pin represented by the parallel resistance of $R_{FB_PG(TOP)} \parallel R_{FB_PG(BOTTOM)}$. The FB_PG pin has dual functionality: adjusting the $I_{CL}$ value and setting the power-good (PG) assert threshold.

Prior to start up, the input impedance of the FB_PG pin is sampled and the $I_{CL}$ value is adjusted based on the input impedance.

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**备注**

The current limit programmability is dependent on the output voltage. For voltages below 0.4 V, the current limit cannot be programmed. For voltages between 0.4 V and 1.2 V, the current limit cannot be adjusted and is always set to 100%. Programmable Current Limit vs Output Voltage describes this behavior.

**Programmable Current Limit vs Output Voltage**

| NOMINAL OUTPUT VOLTAGE (V) | $R_{FB_PG(BOTTOM)}$ (kΩ) | $R_{FB_PG(TOP)}$ (kΩ) | $I_{CL}$ SETTING (%) |
|---|---|---|---|
| $V_{OUT(nom)} \geq 1.2$ V | $R_{FB_PG(BOTTOM)}$ = 0.2 V / 16 µA | $R_{FB_PG(TOP)} = R_{FB_PG(BOTTOM)} \times (V_{OUT(nom)} / 0.2\ V \times K - 1)$ with K = PG threshold (%$V_{OUT}$) | 100 |
| | $R_{FB_PG(BOTTOM)}$ = 0.2 V / 4 µA | | 80 |
| | $R_{FB_PG(BOTTOM)}$ = 0.2 V / 2 µA | | 60 |
| 0.4 V ≤ $V_{OUT(nom)}$ < 1.2 V | $R_{FB_PG(BOTTOM)}$ = 0.2 V / 6 µA | | 100 |
| $V_{OUT(nom)}$ < 0.4 V | N/A | N/A | N/A |

表 8-1 provides values for various output voltages using 1% resistors.

**表 8-1. Programmable Current Limit Voltage-Divider Current Settings**

| NOMINAL OUTPUT VOLTAGE (V) | $R_{FB_PG(BOTTOM)}$ (kΩ) | $R_{FB_PG(TOP)}$ (kΩ) | $I_{CL}$ SETTING (%) | PG THRESHOLD (%) |
|---|---|---|---|---|
| $V_{OUT(nom)}$ = 1.2 V | 12.4 | 51.1 | 100 | 85 |
| | 49.9 | 205 | 80 | 85 |
| | 100 | 412 | 60 | 85 |
| $V_{OUT(nom)}$ = 3.3 V | 12.4 | 187 | 100 | 95 |
| | 49.9 | 732 | 80 | 95 |
| | 100 | 1470 | 60 | 95 |
| $V_{OUT(nom)}$ = 5.1 V | 12.4 | 287 | 100 | 95 |
| | 49.9 | 1150 | 80 | 95 |
| | 100 | 2320 | 60 | 95 |

图 8-9 shows the different $I_{CL}$ settings for a nominal 3.3-V output voltage.

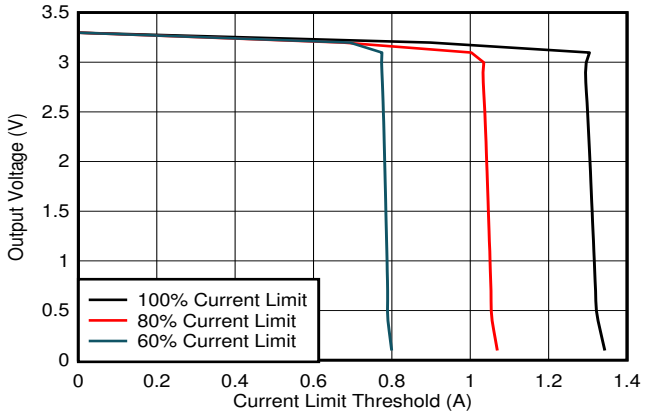


**图 8-9. Programmable Current Limit Behavior (Typical) for a 3.3-$V_{OUT(nom)}$**


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### 8.1.7 Programmable Soft-Start and Noise-Reduction (NR/SS Pin)

The NR/SS pin is the input to the inverting terminal of the error amplifier, see the *Functional Block Diagram*. A resistor connected from this pin to GND sets the output voltage by the pin internal reference current $I_{NR/SS}$, $V_{OUT}$ = $I_{NR/SS}$ × $R_{NR/SS}$ . Connecting a capacitor from this pin to GND significantly reduces the output noise, limits the input inrush-current, and soft-starts the output voltage. Use the minimum value or larger capacitor from NR/SS to ground as listed in the *Electrical Characteristics* table and place the NR/SS capacitor as close to the NR/SS and GND pins of the device as possible.

The device features a programmable, monotonic, voltage-controlled, soft-start circuit that is set to work with an external capacitor ($C_{NR/SS}$). In addition to the soft-start feature, the $C_{NR/SS}$ capacitor also lowers the output voltage noise of the LDO. The soft-start feature can be used to eliminate power-up initialization problems. The controlled output voltage ramp also reduces peak inrush current during start up, minimizing start-up transients to the input power bus.

To achieve a monotonic start up, the device output voltage tracks the $V_{NR/SS}$ reference voltage until this reference reaches the set value (the set output voltage). The $V_{NR/SS}$ reference voltage is set by the $R_{NR/SS}$ resistor and, during start up, using a fast charging current ($I_{FAST_SS}$) in addition to the $I_{NR/SS}$ current, as shown in 图 8-10, to charge the $C_{NR/SS}$ capacitor.

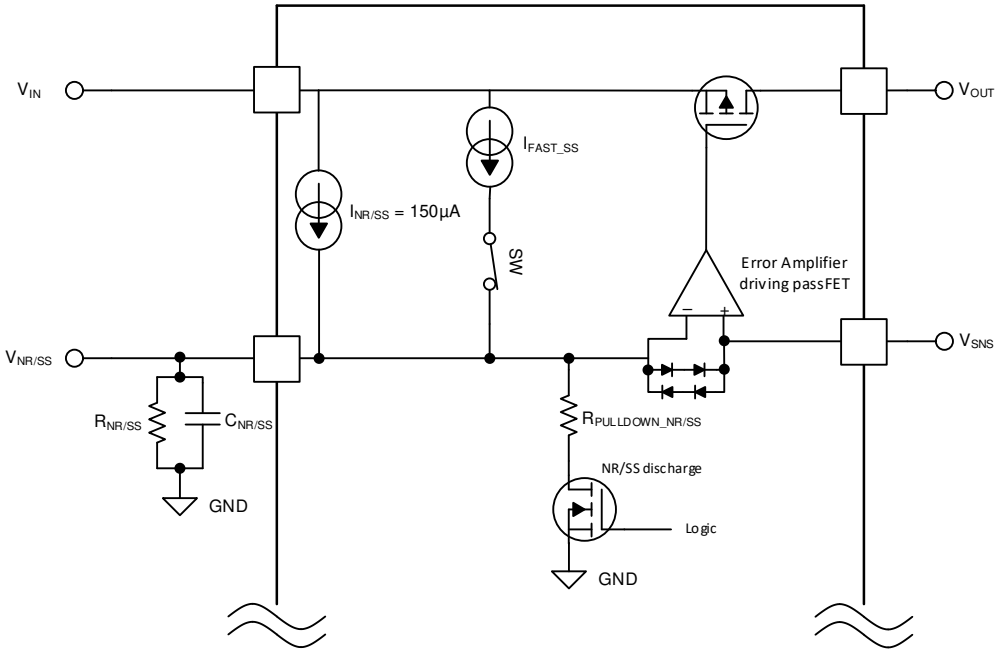


**图 8-10. Simplified Soft-Start Circuit**

The 2.1-mA (typical) $I_{FAST_SS}$ current and 150 µA (typical) $I_{NR/SS}$ current quickly charge $C_{NR/SS}$ until the voltage reaches approximately 93% of the set output voltage, then the $I_{FAST_SS}$ current disengages and only the $I_{NR/SS}$ current continues to charge $C_{NR/SS}$ to the set output voltage level. If there is any error during start up or the output overshoot prevention circuit is triggered, the NR/SS discharge FET turns on, thus discharging the $C_{NR/SS}$ capacitor to protect both the LDO and the load.

The soft-start ramp time depends on the fast start-up ($I_{FAST_SS}$) charging current, the reference current ($I_{NR/SS}$), $C_{NR/SS}$ capacitor value, and the set (targeted) output voltage ($V_{OUT(target)}$). 方程式 3 calculates the soft-start ramp time.

$$\text{Soft-Start Time } (t_{SS}) = (V_{OUT(target)} \times C_{NR/SS}) / (I_{NR/SS} + I_{FAST_SS}) \quad (3)$$

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The $I_{NR/SS}$ current is provided in the *Electrical Characteristics* table and has a value of 150 µA (typical). The $I_{FAST_SS}$ current has a value of 2 mA (typical) for $V_{IN}$ > 2.5 V. 图 8-11 and 图 8-12 depict the $I_{NR/SS}$ and $I_{FAST_SS}$ current versus $V_{IN}$ and temperature.

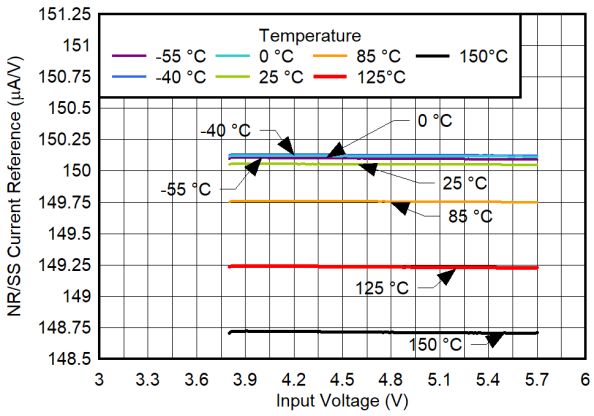


**图 8-11. $I_{NR/SS}$ Reference vs Input Voltage and Temperature for $V_{OUT}$ = 3.3 V**

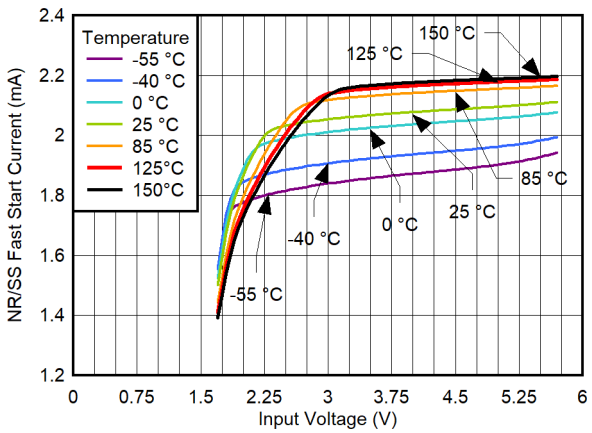


**图 8-12. $I_{FAST_SS}$ Reference vs Input Voltage and Temperature for $V_{OUT}$ = 3.3 V**

Because the error amplifier is always operating in unity-gain configuration, the output voltage noise can only be adjusted by increasing the $C_{NR/SS}$ capacitor. The $C_{NR/SS}$ capacitor and $R_{NR/SS}$ resistor form a low-pass filter (LPF) that filters out the noise from the $V_{NR/SS}$ voltage reference, thereby reducing the device noise floor. The LPF is a single-pole filter and 方程式 4 calculates the LPF cutoff frequency. Increasing the $C_{NR/SS}$ capacitor can significantly lower output voltage noise; however, doing so greatly lengthens start-up time. For low-noise applications, use a 4.7- µF $C_{NR/SS}$ for optimal noise and start-up time trade off.

$$\text{Cutoff Frequency } (f_{cutoff}) = 1 / (2 \times \pi \times R_{NR/SS} \times C_{NR/SS}) \quad (4)$$

The *Typical Characteristics* section illustrates the impact of the $C_{NR/SS}$ capacitor on the LDO output voltage noise.

图 8-13 illustrates the relationship, timing, and output voltage value during the start-up phase.


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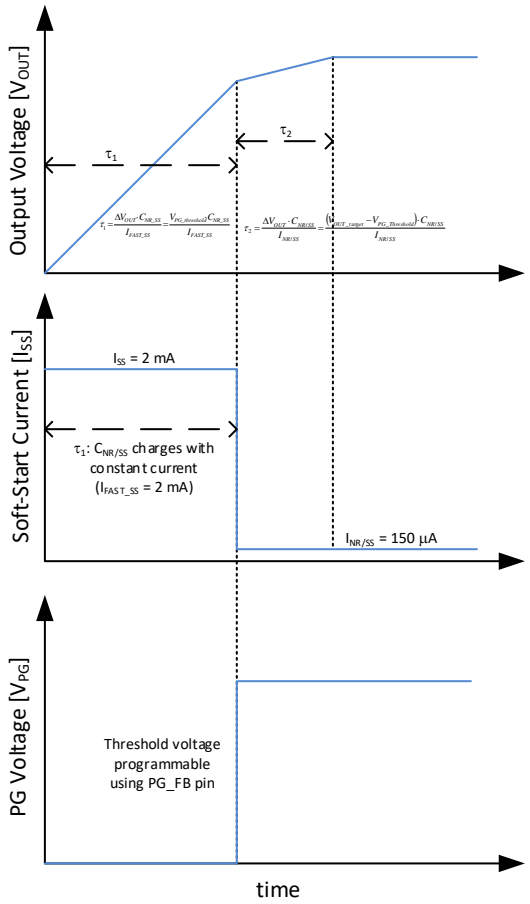


**图 8-13. Relationship Between Threshold Voltage, Output Voltage, $I_{FAST_SS}$, and $I_{NR/SS}$ During Start-Up**

### 8.1.8 Inrush Current

Inrush current is defined as the current into the LDO at the IN pin during start up. Inrush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed. Operating without an input capacitor is not recommended because this capacitor is required for stability. However, 方程式 5 can be used to estimate this current.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (5)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the $V_{OUT}$ ramp
- $R_{LOAD}$ is the resistive load impedance

As illustrated in 图 8-10, the external capacitor at the NR/SS pin ($C_{NR/SS}$) sets the output start-up time by setting the rise time of the $V_{NR/SS}$ reference voltage.

Inrush current for a no-load condition is given in 图 6-37 to 图 6-40.

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### 8.1.9 Optimizing Noise and PSRR

Noise can be generally defined as any unwanted signal combining with the desired signal (such as the regulated LDO output). Noise can easily be noticed in audio as a hissing or popping sound. Noise produced from an external circuit or the 50- to 60-hertz power-line noise (spikes), along with the harmonics, is an excellent representative of extrinsic noise. Intrinsic noise is produced by components within the device circuitry, such as resistors and transistors. The two dominating sources of intrinsic noise are the error amplifier and the internal reference voltage ($V_{NR/SS}$). Extrinsic noise, including the switching mode power-supply ac ripple voltage, coupled onto the input supply of the LDO is attenuated by the LDO power-supply rejection ratio, or PSRR. PSRR is a measurement of the noise attenuation from the input to the output of the LDO.

Optimize the intrinsic noise and PSRR by carefully selecting:

- $C_{NR/SS}$ for the low-frequency range up to the device bandwidth
- $C_{OUT}$ for the high-frequency range close to and higher than the device bandwidth
- Operating headroom, $V_{IN}$ – $V_{OUT}$ ($V_{DO}$), mainly for the low-frequency range up to the device bandwidth, but also for higher frequencies to a lesser effect

These behaviors are described in the *Typical Characteristics* curves.

图 8-14 and 图 8-15 show the measured 10-Hz to 100-kHz RMS noise for a 3.3-V device output voltage with a 0.5-V headroom for different $C_{NR/SS}$ and $C_{OUT}$ capacitors and a 1-A load current. 表 8-2 lists the typical output noise for these capacitors.

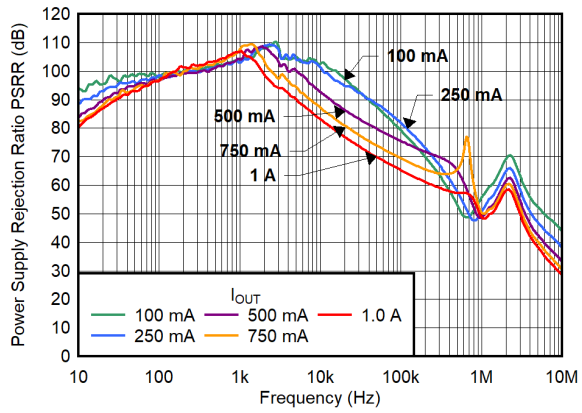


图 8-14. PSRR vs Frequency and $I_{OUT}$ for $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 10 µF

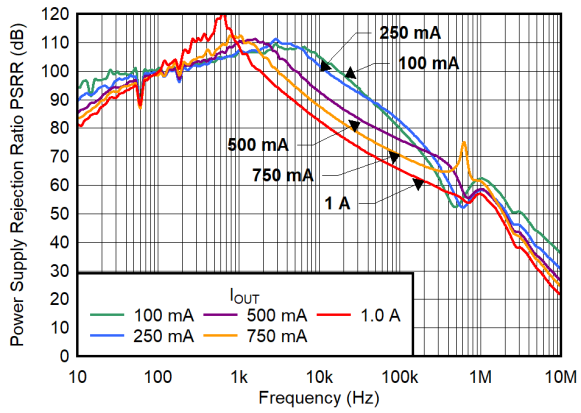


图 8-15. PSRR vs Frequency and $I_{OUT}$ for $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 4.7 µF || 4.7 µF|| 1.0 µF

表 8-2. Typical Output Noise for 3.3-$V_{OUT}$ vs $C_{NR/SS}$, $C_{OUT}$, and Typical Start-Up Time

| $V_n$ (µ$V_{RMS}$), 10-Hz to 100-kHz BW | $C_{NR/SS}$ (µF) | $C_{OUT}$ (µF) | START-UP TIME (ms) |
|---|---|---|---|
| 0.98 | 1 | 10 | 3.73 |
| 0.62 | 2.2 | 10 | 6.21 |
| 0.46 | 4.7 | 10 | 13.97 |
| 0.42 | 10 | 10 | 28.21 |

PSRR can be viewed as being simply the ratio of the output capacitor impedance by the LDO output impedance. At low frequency, the output impedance is very low whereas the output impedance of the capacitor is high, resulting in high PSRR. As the frequency increases, the output capacitor impedance reduces and reaches a minima set by the ESR.

As shown in 图 8-14 and 图 8-15, and in order to achieve high PSRR at high frequencies, ensure that the output capacitor ESR and ESL are minimal. These figures compare the use of a single 10-µF output capacitor with a


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4.7- µF || 4.7- µF || 1.0- µF implementation. Notice that below 200 kHz, there is no impact on performance but above 200 kHz, the PSRR improves by 5 dB to 7 dB.

Minimizing the ESR, ESL generated resonance point in the output capacitance allows for a smoother transition between the LDO active PSRR component to the passive PSRR of the capacitors.

### 8.1.10 Adjustable Operation

As shown in 图 8-16, the output voltage of the device can be set using a single external resistor ($R_{NR/SS}$). 方程式 6 calculates the output voltage.

$$V_{OUT} = I_{NR/SS(NOM)} \times R_{NR/SS} \quad (6)$$

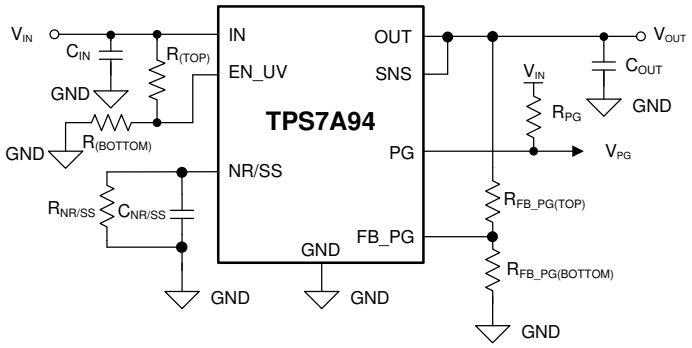


图 8-16. Typical Circuit

表 8-3 shows the recommended $R_{NR/SS}$ resistor values to achieve several common rails using a standard 1%-tolerance resistor.

表 8-3. Recommended $R_{NR/SS}$ Values

| TARGETED OUTPUT VOLTAGE (V) | $R_{NR/SS}$ (kΩ) | CALCULATED OUTPUT VOLTAGE (V) |
|---|---|---|
| 0.4 | 2.67 | 0.4005 |
| 0.5 | 3.32 | 0.498 |
| 0.6 | 4.02 | 0.603 |
| 0.7 | 4.64 | 0.696 |
| 0.8 | 5.36 | 0.804 |
| 0.9 | 6.04 | 0.906 |
| 1.0 | 6.65 | 0.9975 |
| 1.2 | 8.06 | 1.209 |
| 1.5 | 10.0 | 1.5 |
| 2.5 | 16.5 | 2.475 |
| 3.0 | 20.0 | 3.0 |
| 3.3 | 22.1 | 3.315 |
| 3.6 | 24.3 | 3.645 |
| 4.7 | 31.6 | 4.74 |
| 5.0 | 33.2 | 4.98 |

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备注

To avoid engaging the current limit during start-up with a large $C_{OUT}$ capacitor, make sure that:

1. A minimum NR/SS capacitor of 1 μF is used
2. When the output capacitor is greater than 100 μF, maintain a $C_{OUT}$ to $C_{NR/SS}$ ratio < 100

Because the set resistor is also placed on the NR/SS pin, consider using a thin-film resistor and provide enough resistor temperature drift to ensure the targeted accuracy.

### 8.1.11 Paralleling for Higher Output Current and Lower Noise

Achieving higher output current and lower noise is achievable by paralleling two or more LDOs. Implementation must be carefully planned out to optimize performance and minimize output current imbalance.

Because the TPS7A94 output voltage is set by a resistor driven by a current source, the NR/SS resistor and capacitor must be adjusted as per the following:

$$R_{NR/SS_parallel} = V_{OUT_TARGET} / (n \times I_{NR/SS}) \quad (7)$$

$$C_{NR/SS_parallel} = n \times C_{NR/SS_single} \quad (8)$$

where:

- n is the number of LDOs in parallel
- $I_{NR/SS}$ is the NR/SS current as provided in the data sheet *Electrical Characteristics* table
- $C_{NR/SS_}$single is the NR/SS capacitor for a single LDO

When connecting the input and NR/SS pin together, and with the LDO being a buffer, the current imbalance is only affected by the error offset voltage of the error amplifier. As such, the current imbalance can be expressed as:

$$\varepsilon_I = V_{OS} \times 2 \times R_{BALLAST} / (R_{BALLAST}^2 - \Delta R_{BALLAST}^2) \quad (9)$$

where:

- $\varepsilon_I$ is the current imbalance
- $V_{OS}$ is the LDO error offset voltage
- $R_{BALLAST}$ is the ballast resistor
- $\Delta R_{BALLAST}$ is the deviation of the ballast resistor value from the nominal value

With the typical offset voltage of 200 μV, considering no error from the design of the PCB ballast resistor ($\Delta R_{BALLAST}$ = 0) and a 100-mA maximum current imbalance, the ballast resistor must be 4 mΩ or greater; see 图 8-17.

Using the configuration described, the LDO output noise is reduced by:

$$e_{O_parallel} = (1 / \sqrt{n}) \times e_{O_single} \quad (10)$$

where:

- n is the numbers of LDOs in parallel
- $e_{O_single}$ is the output noise density from a single LDO
- $e_{O_parallel}$ is the output noise density for the resulting parallel LDO


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In 图 8-17, the noise is reduced by 1 / $\sqrt{2}$.

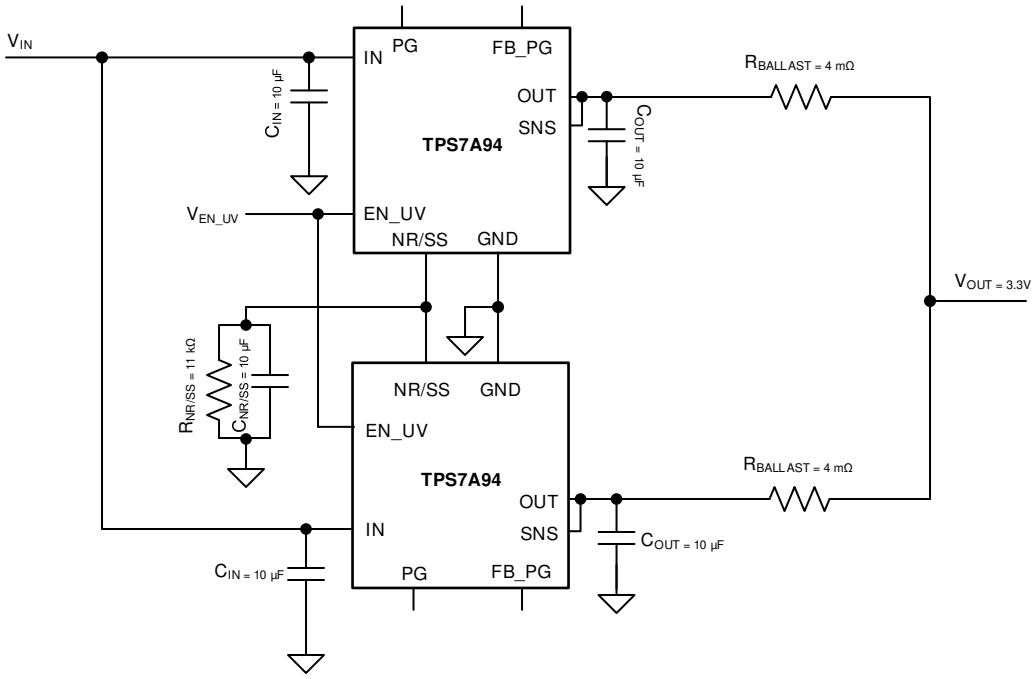


**图 8-17. Paralleling Multiple TPS7A94 Devices**

### 8.1.12 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) and low equivalent series inductance (ESL) ceramic capacitors at the input, output, and noise-reduction pin. Multilayer ceramic capacitors have become the industry standard for these applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-rated, or better dielectric materials provide relatively good capacitive stability across temperature. The use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%, but at high $V_{IN}$ and $V_{OUT}$ conditions ($V_{IN}$ = 5.5 V to $V_{OUT}$ = 5.0 V), the derating can be greater than 50%, which must be taken into consideration.

The device requires input, output, and noise-reduction capacitors for proper operation of the LDO. Use the nominal or larger than the nominal input, and output capacitors as specified in the *Recommended Operating Conditions* table. Place input and output capacitors as close as possible to the corresponding pin and make the capacitor GND connections as close as possible to the device GND pin to minimize PCB loop inductance, thus reducing transient voltage spikes during a load step.

As illustrated in 图 8-15, multiple parallel capacitors can be used to lower the impedance present on the line. This capacitor counteracts input trace inductance, improves transient response, and reduces input ripple and noise. Using an output capacitor larger than the typical value can also improve the transient response.

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### 8.1.13 Load Transient Response

**备注**

For best transient response, use the nominal value or larger capacitor from OUT to ground as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible.

For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.

The load-step transient response is the LDO output voltage response to load current changes. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions shown in 图 8-18 are broken down in this section. Regions A, E, and H are where the output voltage is in steady-state regulation.

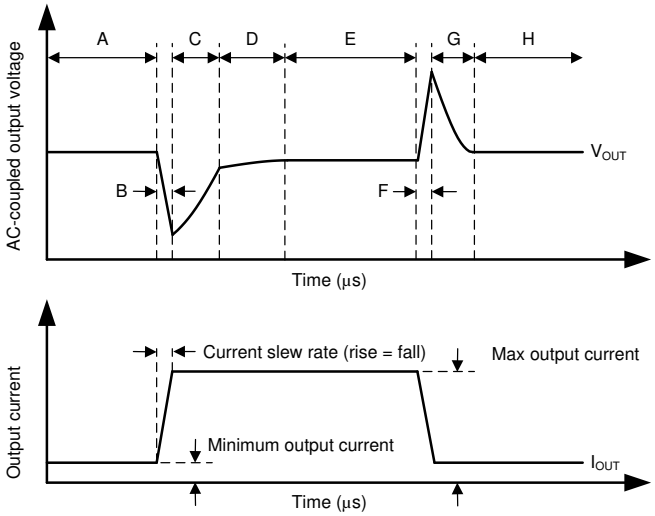


**图 8-18. Load Transient Waveform**

During transitions from a light load to a heavy load:

- The initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load:

- The initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

Transitions between current levels changes the internal power dissipation because the device is a high-current device (region D). The change in power dissipation changes the die temperature during these transitions, and leads to a slightly different voltage level. This temperature-dependent output voltage level shows up in the various load transient responses.

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.


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### 8.1.14 Power Dissipation ($P_D$)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. 方程式 11 calculates $P_D$:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \tag{11}$$

**备注**

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The power dissipation by the device determines the junction temperature ($T_J$) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air ($T_A$), according to 方程式 12. This equation is rearranged for output current in 方程式 13.

$$T_J = T_A = (R_{\theta JA} \times P_D) \tag{12}$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \tag{13}$$

This thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the DSC package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

### 8.1.15 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi ($\Psi$) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) are used in accordance with 方程式 14 and are given in the *Thermal Information* table.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \tag{14}$$

where:

- $P_D$ is the power dissipated as explained in the *Power Dissipation ($P_D$)* section
- $T_T$ is the temperature at the center-top of the device package
- $T_B$ is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

### 8.1.16 TPS7A94EVM-046 Thermal Analysis

The TPS7A94EVM-046 EVM was used to develop the TPS7A9401DRC thermal model. The DRC package is a 3-mm × 3-mm, 10-pin VQFN with 25-µm plating on each via. The EVM is a 2.85-inch × 3.35-inch (72.39 mm × 85.09 mm) PCB comprised of four layers. 表 8-4 lists the layer stackup for the EVM. 图 8-19 to 图 8-23 illustrate the various layer details for the EVM.

**表 8-4. TPS7A94EVM-046 PCB Stackup**

| LAYER | NAME | MATERIAL | THICKNESS (mil) |
|---|---|---|---|
| 1 | Top overlay | — | — |
| 2 | Top solder | Solder resist | 0.4 |
| 3 | Top layer | Copper | 2.8 |
| 4 | Dielectric 1 | FR-4 high Tg | 10 |
| 5 | Mid layer 1 | Copper | 2.8 |
| 6 | Dielectric 2 | FR-4 high Tg | 30 |
| 7 | Mid layer 2 | Copper | 2.8 |
| 8 | Dielectric 3 | FR-4 high Tg | 10 |
| 9 | Bottom layer | Copper | 2.8 |
| 10 | Bottom solder | Solder resist | 0.4 |

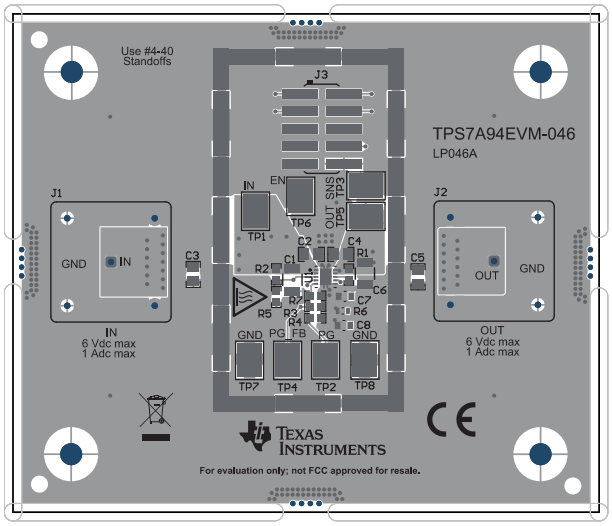


图 8-19. Top Composite View

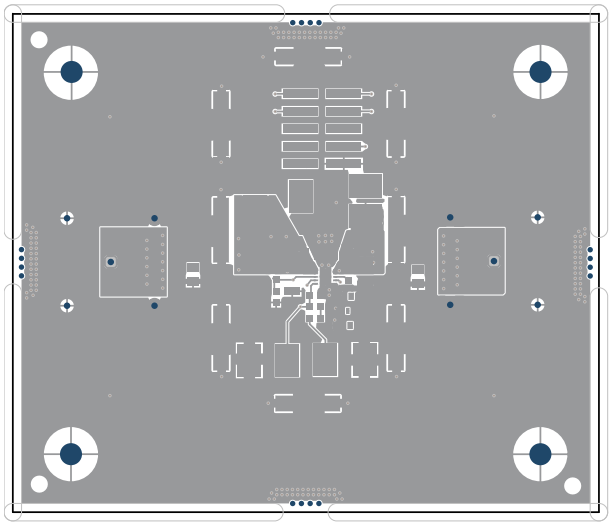

图 8-20. Top Layer Routing


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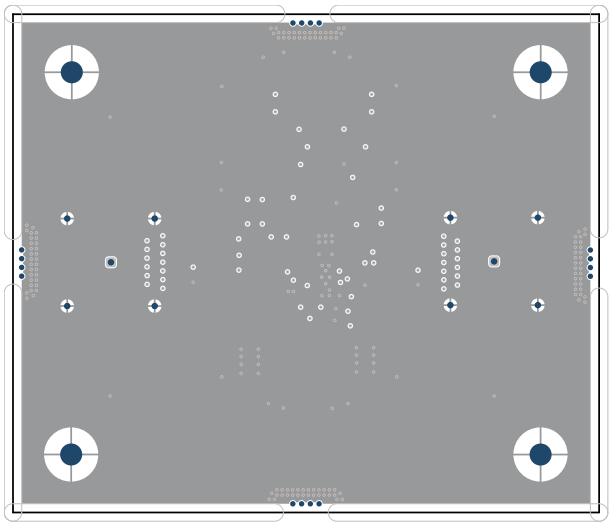


图 8-21. Mid Layer 1 Routing

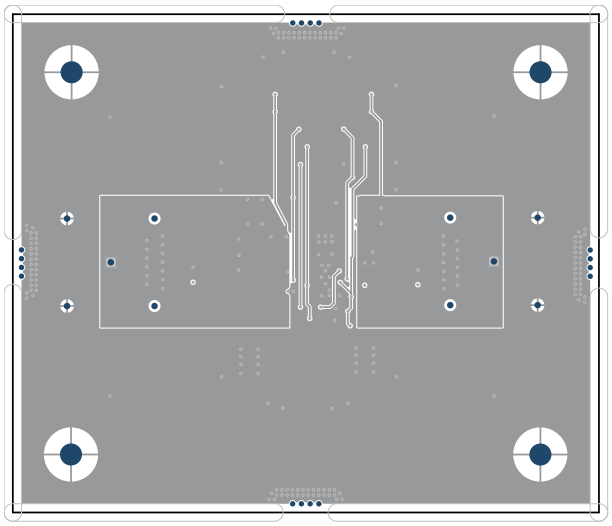


图 8-22. Mid Layer 2 Routing

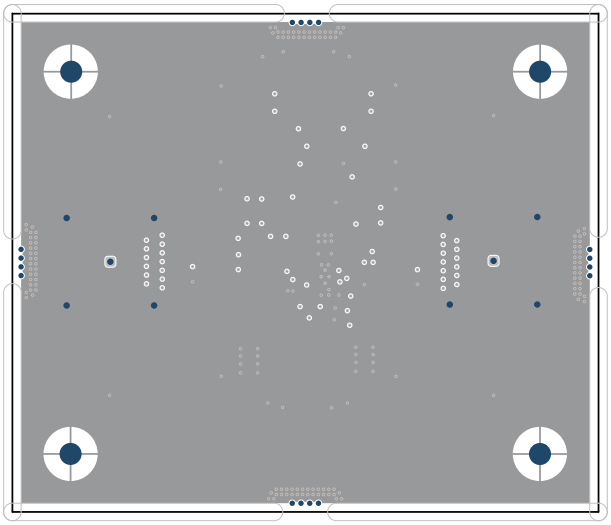


图 8-23. Bottom Layer Routing

图 8-24 to 图 8-26 show the thermal gradient on the PCB and device that results when a 1-W power dissipation is used through the pass transistor with a 25°C ambient temperature. 表 8-5 shows thermal simulation data for the TPS7A94EVM-046.

**表 8-5. TPS7A94EVM-046 Thermal Simulation Data**

| DUT | $R_{\theta JA}$ (°C/W) | $\Psi_{JB}$ (°C/W) | $\Psi_{JT}$ (°C/W) |
|---|---|---|---|
| TPS7A94EVM-046 | 25.6 | 11.5 | 0.3 |

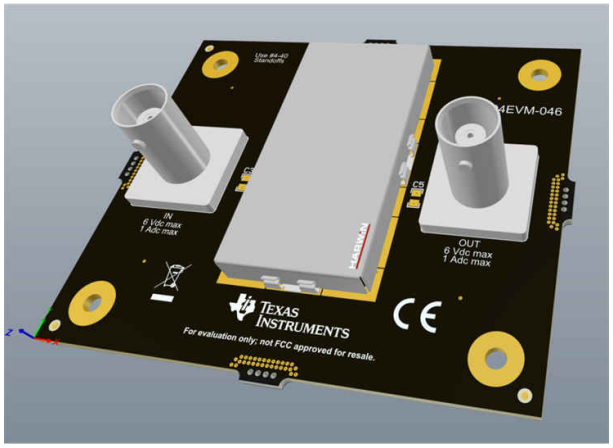
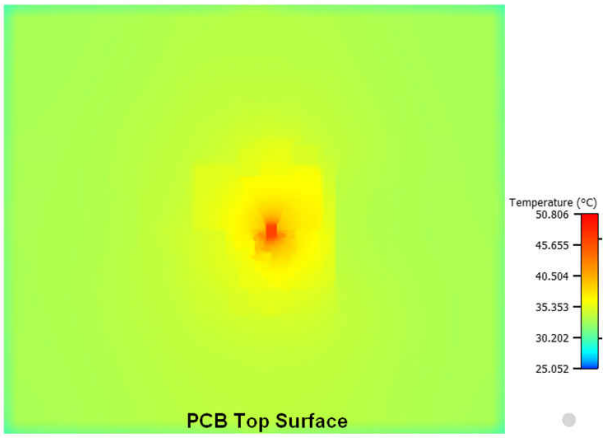



**图 8-24. TPS7A94EVM-046 3D View**




C

**图 8-25. TPS7A94EVM-046 PCB Thermal Gradient**

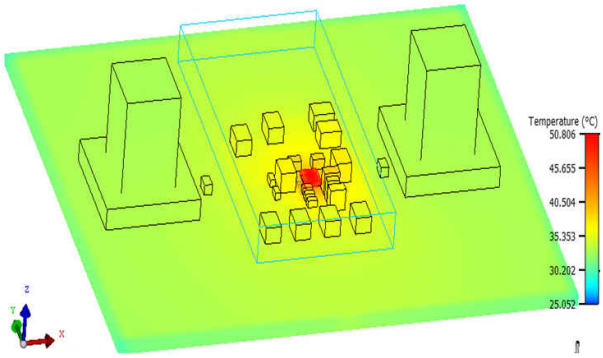



**图 8-26. TPS7A94EVM-046 Device Thermal Gradient**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## 8.2 Typical Application

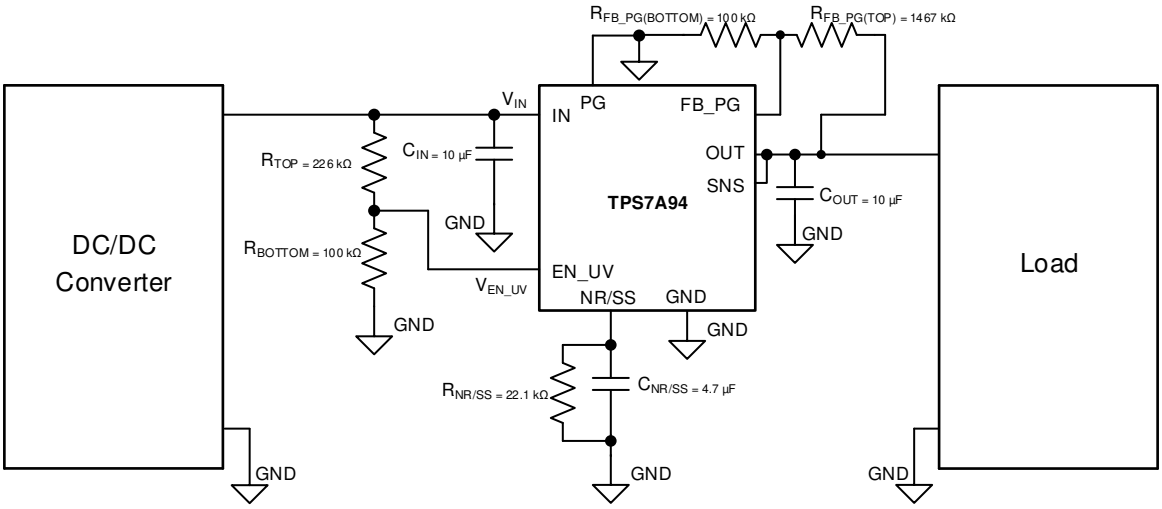


图 8-27. Typical Application Circuit

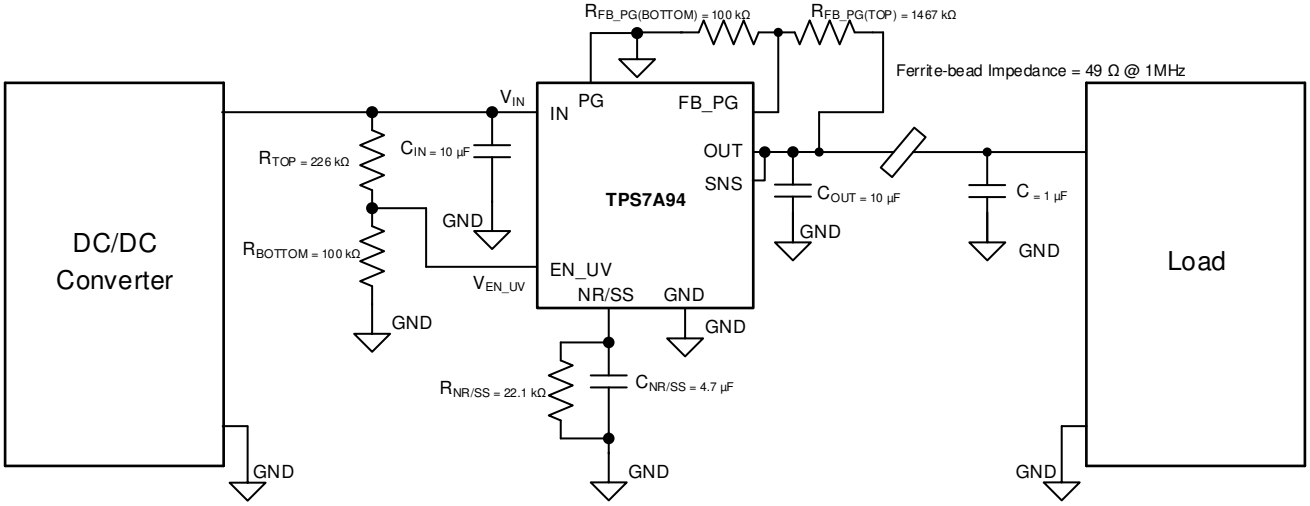


图 8-28. Typical Application Circuit With Added Pi-Filter

### 8.2.1 Design Requirements

表 8-6 lists the required application parameters for this design example.

**表 8-6. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | $V_{IN} \geqslant$ 5 V, ±3%, provided by the dc/dc converter switching at 1 MHz |
| Output voltage | 3.3 V, ±1% |
| Output current | 500 mA (maximum), 300 mA (minimum) |
| Current limit | 750 mA |
| PG threshold | 95% |
| Targeted spectral noise | Targeted noise compliance mask<br>Zone 1 (10 Hz to 100 Hz): Spectral noise $\leqslant$ 100 nV/ $\sqrt{\text{Hz}}$<br>Zone 2 (100 Hz to 1 kHz): Spectral noise $\leqslant$ 10 nV/ $\sqrt{\text{Hz}}$<br>Zone 3 (> 1 kHz): Spectral noise $\leqslant$ 3 nV/ $\sqrt{\text{Hz}}$ |
| PSRR at 1 MHz | > 50 dB at max load current |
| Start-up environment | Device to be enabled when $V_{IN} \geqslant 80\% \times V_{IN_Target}$<br>Device to be disabled when $V_{IN} < 80\% \times V_{IN_Target}$<br>Start-up time < 25 ms |

### 8.2.2 Detailed Design Procedure

In this design example, the device is powered by a dc/dc convertor switching at 1 MHz. The load requires a 3.3-V clean rail with the spectral noise mask versus frequency shown in 图 8-29 and a maximum load of 500 mA. The typical 10-µF input and output capacitors and 4.7-µF NR/SS capacitors are used to achieve a good balance between fast start-up time and excellent noise and PSRR performance.

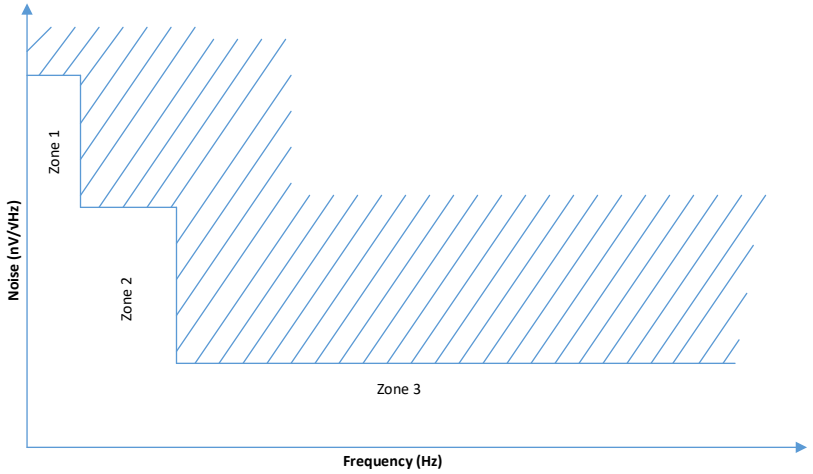


**图 8-29. Noise Compliance Mask**

The output voltage is set using a 22.1-kΩ, thin-film resistor value calculated as described in the *Adjustable Operation* section. To set the current limit to a value close to the 750 mA required by the application, and to set the PG threshold to 95%, use 表 8-1 to set the $R_{FB_PG}$ top and bottom resistors values at 1.47 MΩ and 100 kΩ, respectively.

Setting $R_B$ to 100 kΩ and using a 4-V $V_{ON}$ and 方程式 1 provide the $R_T$ value of 226 kΩ. $V_{OFF}$ is calculated with 方程式 2 to be 3.5 V.


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图 8-30 shows that the device meets all design noise requirements except for the noise peaking at 900 kHz. However, this noise peaking can be easily attenuated to the required noise level by means of a pi-filter positioned after the LDO. 图 8-31 shows that this design is very close to the PSRR level at 1 MHz and can require more margin. Fortunately, both requirements are easily achieved by inserting a pi-filter consisting of a ferrite bead and a small capacitor beyond the LDO and before the load; see 图 8-28.

The ferrite bead was selected to have a very small dc resistance of less than 50 mΩ, 1 A of current rating, and a relatively small footprint. The added pi-filter components have almost no impact on the LDO accuracy performance and no significant increase in the design total cost.

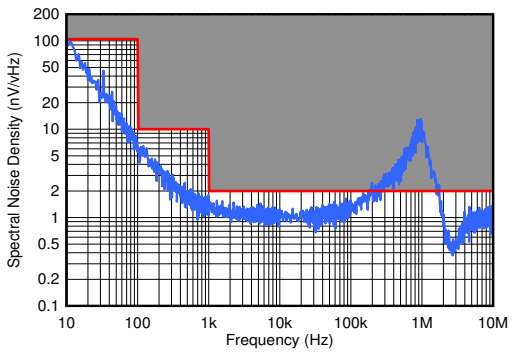


图 8-30. Output Noise vs Frequency

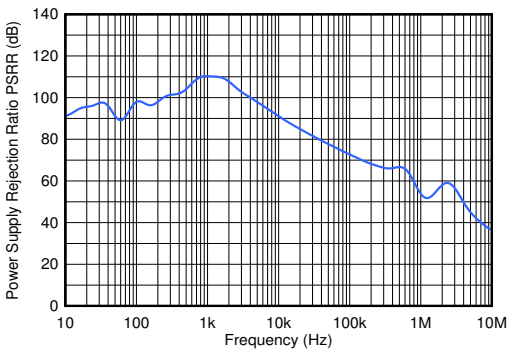


图 8-31. PSRR vs Frequency

### 8.2.3 Application Curves

图 8-32 and 图 8-33 show the design noise and PSRR performance after inserting the pi-filter.

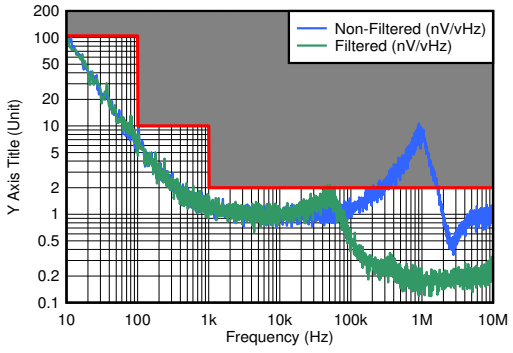


图 8-32. Noise vs Frequency

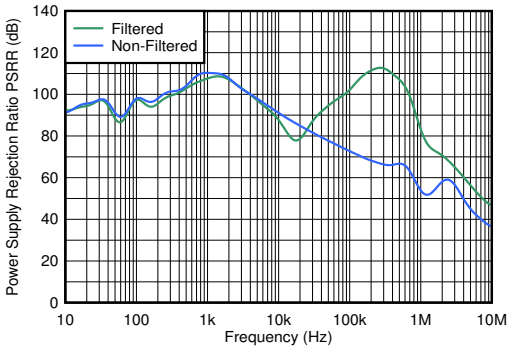


图 8-33. PSRR vs Frequency

## 8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging from 1.7 V to 5.7 V. Ensure that the input voltage range provides adequate operational headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, use additional input capacitors with low ESR and increase the operating headroom to achieve the desired output noise, PSRR, and load transient performance.

## 8.4 Layout

### 8.4.1 Layout Guidelines

#### *8.4.1.1 Board Layout*

For good thermal performance, connect the thermal pad to a large-area GND plane.

Kelvin connects the SNS pin through a low-impedance connection to the output capacitor and load for optimal transient performance. Do not float this pin.

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Connect the GND pin to the device thermal pad and connect both this pin and the thermal pad to the ground on the board through a low-impedance connection.

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. To avoid negative system performance, do not use vias or long traces to the input and output capacitors. The grounding and layout scheme described in 图 8-34 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

To improve performance, use a ground reference plane, either embedded in the printed circuit board (PCB) or placed on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

#### *8.4.1.2 Layout Example*

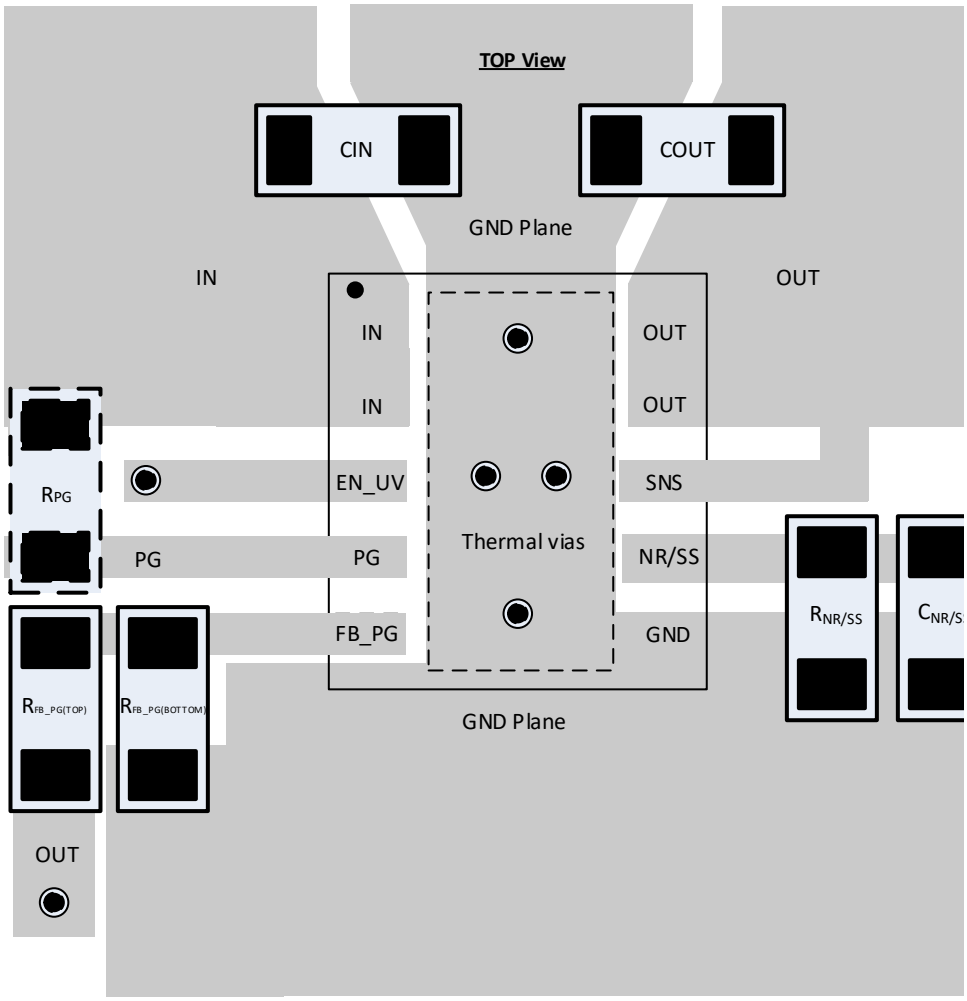


**图 8-34. Example Layout**


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# 9 Device and Documentation Support

## 9.1 Device Support

### 9.1.1 Development Support

#### *9.1.1.1 Evaluation Modules*

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A94. 表 9-1 shows the summary information for this fixture.

**表 9-1. Design Kits and Evaluation Modules**

| NAME | LITERATURE NUMBER |
|---|---|
| TPS7A94EVM-046 evaluation module | SBVU070 |

The EVM can be requested at the Texas Instruments web site through the TPS7A94 product folder.

#### *9.1.1.2 Spice Models*

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A94 is available through the TPS7A94 product folder under *simulation models*.

### 9.1.2 Device Nomenclature

**表 9-2. Ordering Information(1)**

| PRODUCT | DESCRIPTION |
|---|---|
| TPS7A9401 **yyy z** | **yyy** is the package designator.<br>**z** is the package quantity. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

## 9.2 Documentation Support

### 9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS3702 High-Accuracy, Overvoltage and Undervoltage Monitor* data sheet
- Texas Instruments, *TPS7A94EVM-046 Evaluation Module* user guide
- Texas Instruments, *High-Current, Low-Noise Parallel LDO* reference design

## 9.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 9.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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### 9.5 Trademarks

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### 9.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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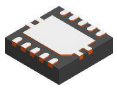
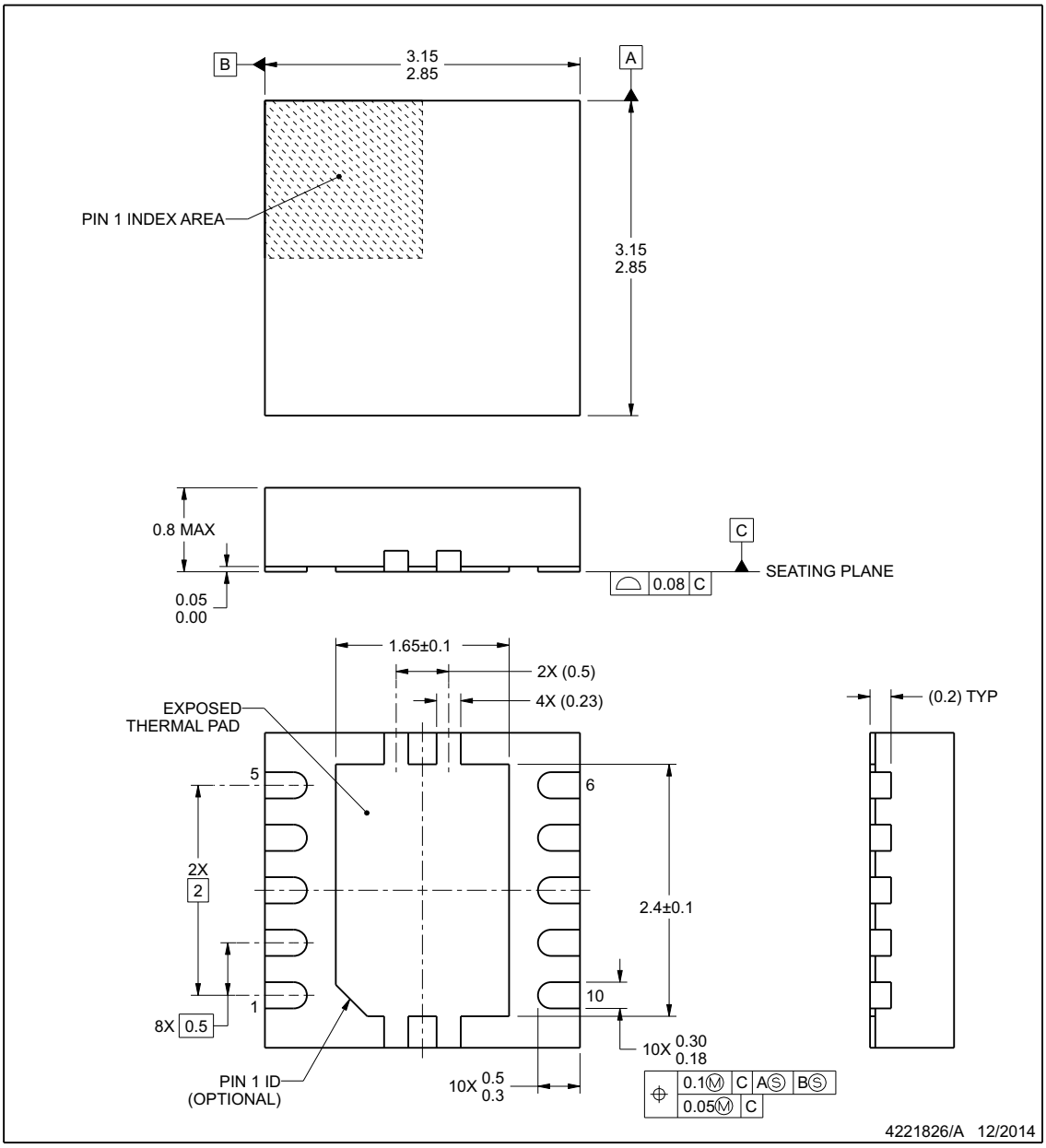
## 10.1 Mechanical Data



**PACKAGE OUTLINE**

**DSC0010J** — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



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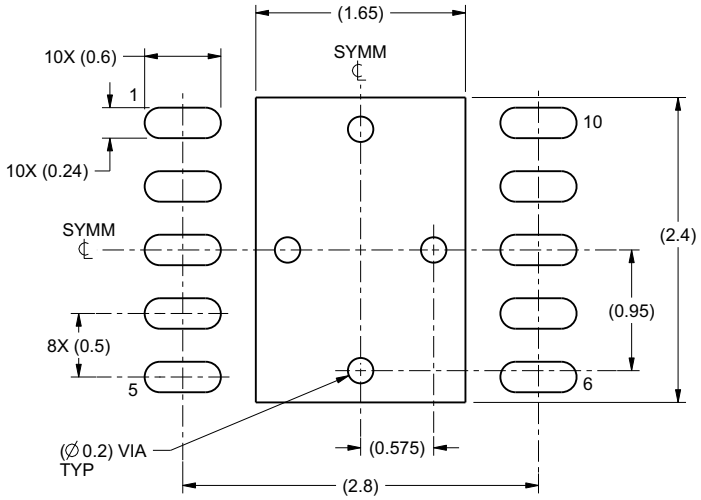
# EXAMPLE BOARD LAYOUT

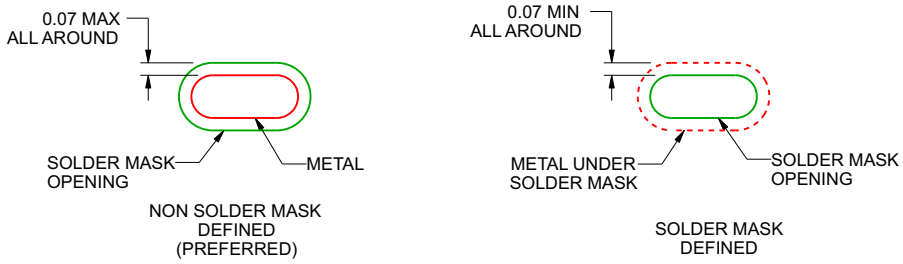
## DSC0010J

### WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
SCALE:20X




SOLDER MASK DETAILS

4221826/A 12/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).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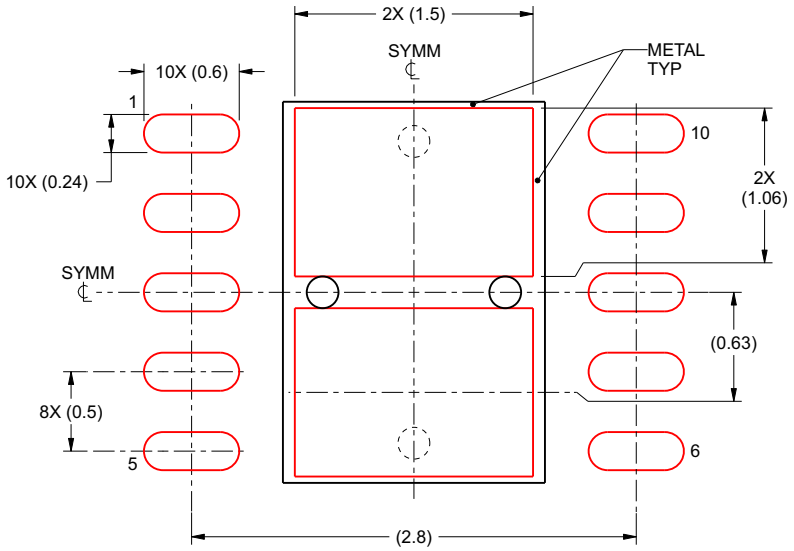
# EXAMPLE STENCIL DESIGN

## DSC0010J

### WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4221826/A 12/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7A9401DSCR | Active | Production | WSON (DSC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7A9401 |
| TPS7A9401DSCR.A | Active | Production | WSON (DSC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7A9401 |
| TPS7A9401DSCRG4 | Active | Production | WSON (DSC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7A9401 |
| TPS7A9401DSCRG4.A | Active | Production | WSON (DSC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7A9401 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

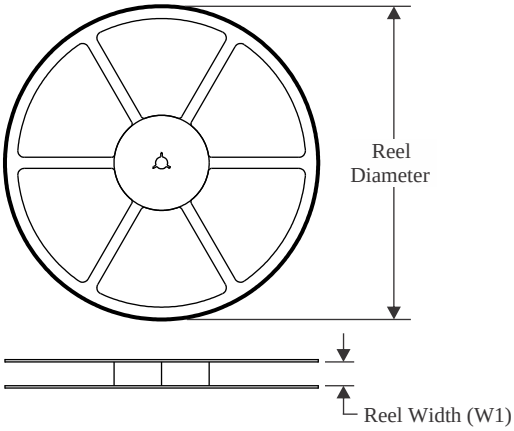
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

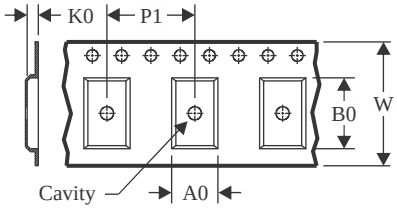
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

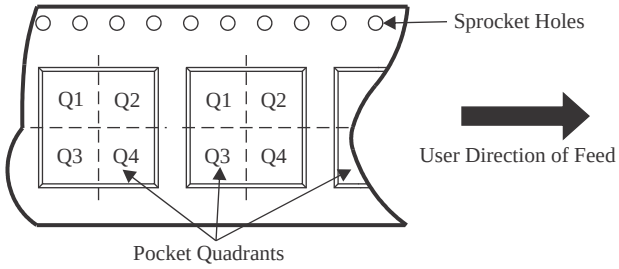



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

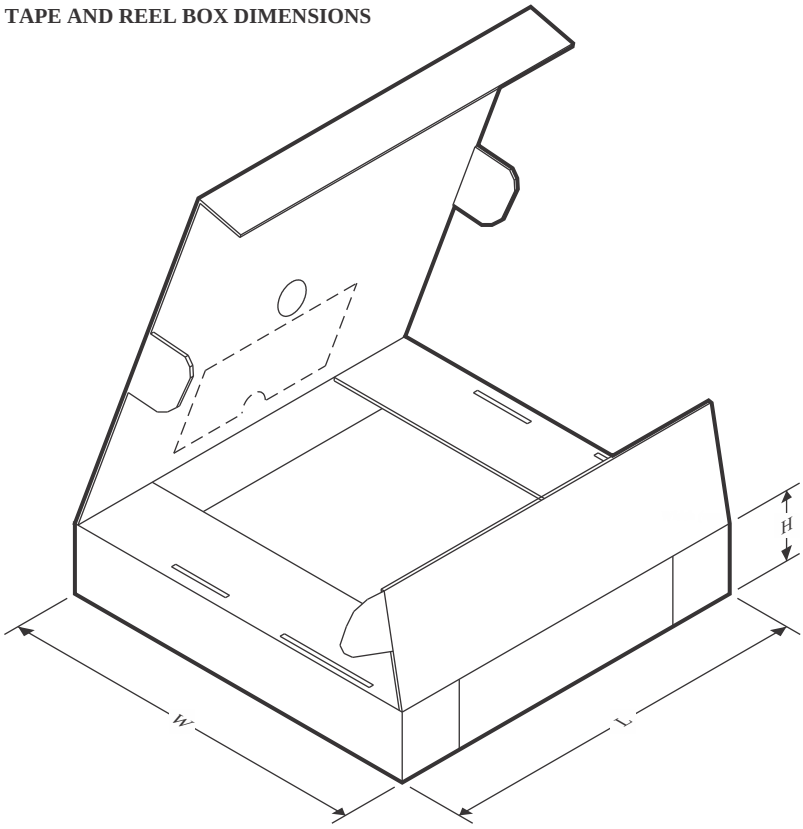
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A9401DSCR | WSON | DSC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A9401DSCRG4 | WSON | DSC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7A9401DSCR | WSON | DSC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS7A9401DSCRG4 | WSON | DSC | 10 | 3000 | 367.0 | 367.0 | 35.0 |

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