TPS7A92
2A 高精度、低噪声 LDO 稳压器

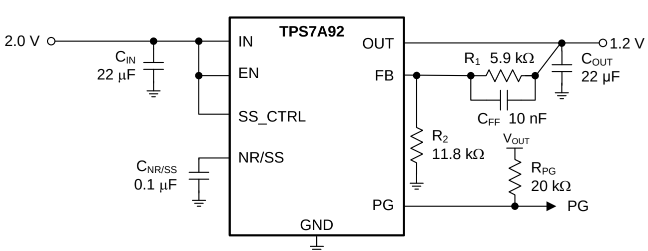
1 特性

- 整个线路、负载和温度范围内的精度达 1.0%
- 低输出噪声：4.6μV_{RMS} (10Hz–100kHz)
- 低压降：2A 时 180mV（典型值）
- 宽输入电压范围：1.4V 至 6.5V
- 宽输出电压范围：0.8V 至 5.2V
- 高电源纹波抑制 (PSRR)：
  - 直流时为 60dB
  - 100kHz 时为 40dB
  - 1MHz 时为 40dB
- 快速瞬态响应
- 通过可选软启动充电电流实现可调节的启动浪涌控制
- 开漏电源正常 (PG) 输出
- $R_{\theta JC}$ = 3.2°C/W
- 与 22μF 或更大的陶瓷输出电容器一起工作时保持稳定
- 2.5mm × 2.5mm 10 引脚 WSON 封装

2 应用

- 高速模拟电路：
  - 压控振荡器 (VCO)、模数转换器 (ADC)、数模转换器 (DAC) 以及低压差分信令 (LVDS)
- 成像：互补金属氧化物半导体 (CMOS) 传感器，视频专用集成电路 (ASIC)
- 测试和测量
- 仪器仪表、医疗和音频
- 数字负载：串化解串器 (SerDes)，现场可编程栅极阵列 (FPGA)，DSP

典型应用电路



3 说明

TPS7A92 是一款低噪声 (4.8μV_{RMS})、低压降 (LDO) 稳压器，可提供 2A 负载电流，其压降仅为 180mV。

TPS7A92 输出可通过外部电阻在 0.8V 至 5.2V 范围内进行调节。TPS7A92 的宽输入电压范围支持其在低至 1.4V 和高达 6.5V 的电压下工作。

凭借 1% 的输出电压精度（整个线路、负载和温度范围内）和用于降低浪涌电流的软启动功能，TPS7A92 非常适合为敏感类模拟低压器件 [例如压控振荡器 (VCO)、模数转换器 (ADC)、数模转换器 (DAC)、高端处理器和现场可编程门阵列 (FPGA)] 供电。

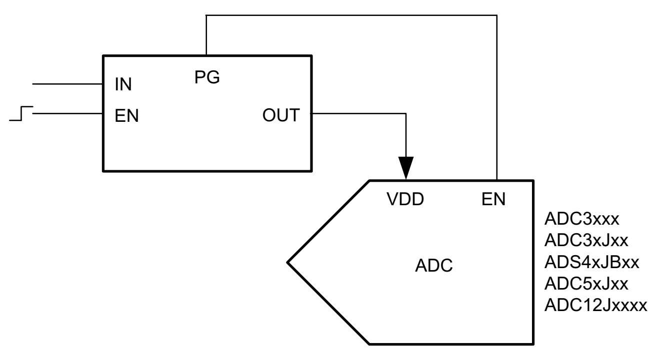
TPS7A92 旨在为高速通信、视频、医疗或测试和测量等 应用中的噪声敏感类组件供电。此器件具有极低的 4.6μV_{RMS} 输出噪声和宽带 PSRR（1MHz 时为 40dB），可最大限度地减少相位噪声和时钟抖动。这些 特性 最大限度提升了计时器件、ADC 和 DAC 的性能。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7A92	WSON (10)	2.50mm x 2.50mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用图



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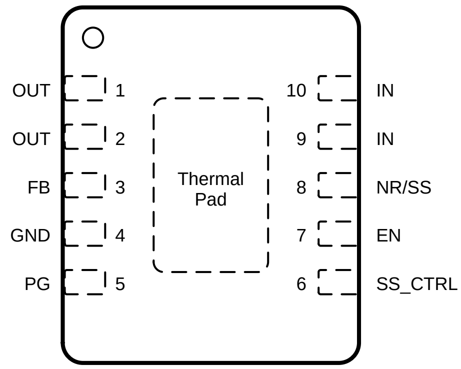
4 修订历史记录

Changes from Revision A (April 2018) to Revision B	**Page**
• Added footnotes to *Recommended Operating Conditions* table	4

Changes from Original (July 2017) to Revision A	**Page**
• 已更改 value of $C_{NR/SS}$ capacitor from 10 nF to 100 nF in *Application Example* figure	21

5 Pin Configuration and Functions

DSK Package
2.5-mm × 2.5-mm 10-Pin WSON
Top View



Not to scale

Pin Functions

PIN			DESCRIPTION
NAME	NO.	I/O	
EN	7	I	Enable pin. This pin turns the LDO on and off. If $V_{EN} \geq V_{IH(EN)}$, the regulator is enabled. If $V_{EN} \leq V_{IL(EN)}$, the regulator is disabled. The EN pin must be connected to IN if the enable function is not used.
FB	3	I	Feedback pin. This pin is the input to the control loop error amplifier and is used to set the output voltage of the device.
GND	4	—	Device GND. Connect to the device thermal pad.
IN	9, 10	I	Input pin. A 10 µF or greater input capacitor is required.
NR/SS	8	—	Noise reduction pin. Connect this pin to an external capacitor to bypass the noise generated by the internal band-gap reference. The capacitor reduces the output noise to very low levels and sets the output ramp rate to limit inrush current.
OUT	1, 2	O	Regulated output. A 22 µF or greater capacitor must be connected from this pin to GND for stability.
PG	5	O	Open-drain power-good indicator pin for the LDO output voltage. A 10-kΩ to 100-kΩ external pullup resistor is required. This pin can be left floating or connected to GND if not used.
SS_CTRL	6	I	Soft-start control pin. Connect this pin either to GND or IN to change the NR/SS capacitor charging current. If a $C_{NR/SS}$ capacitor is not used, SS_CTRL must be connected to GND to avoid output overshoot.
Thermal pad		—	Connect the thermal pad to the printed circuit board (PCB) ground plane, for an example layout see 图 42.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range and all voltages with respect to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN, PG, EN	–0.3	7.0	V
	IN, PG, EN (5% duty cycle, pulse duration = 200 µs)	–0.3	7.5	
	OUT	–0.3	V_{IN} + 0.3(2)	
	SS_CTRL	–0.3	V_{IN} + 0.3(2)	
	NR/SS, FB	–0.3	3.6	
Current	OUT	Internally limited		A
	PG (sink current into device)		5	mA
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 7.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input supply voltage range	1.4	6.5	V
V_{OUT}	Output voltage range	0.8 - 1%	5.2 + 1%	V
I_{OUT}	Output current	0	2	A
C_{IN}	Input capacitor, each input	10		µF
C_{OUT}	Output capacitor[1][2]	22		µF
$C_{NR/SS}$	Noise-reduction capacitor		1	µF
R_{PG}	Power-good pullup resistance	10	100	kΩ
T_J	Junction temperature range	–40	125	°C

(1) When I_{OUT} ≤ 1 A, the C_{OUT} minimum is 10 µF and the effective output capacitance of 5 µF (minimum) is required for stability.
(2) Effective output capacitance of 11 µF (minimum) is required for stability.

6.4 Thermal Information

THERMAL METRIC[1]		TPS7A92	UNIT
		DSK (WSON)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating temperature range (T_J = –40°C to +125°C), V_{IN} = 1.4 V, $V_{OUT(TARGET)}$ = 0.8 V, I_{OUT} = 50 mA, V_{EN} = 1.4 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, SS_CTRL = GND, PG pin pulled up to V_{INx} with 100 kΩ, and for each channel (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range		1.4		6.5	V
V_{REF}	Reference voltage			0.8		V
V_{UVLO}	Input supply UVLO	V_{IN} rising		1.31	1.39	V
V_{HYS}	V_{UVLO}			290		mV
V_{OUT}	Output voltage range		0.8 – 1.0%		5.2 + 1.0%	V
	Output voltage accuracy[1][2]	0.8 V ≤ V_{OUT} ≤ 5 V, 5 mA ≤ I_{OUT} ≤ 2 A	–1.0%		1.0%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	I_{OUT}= 5 mA, 1.4 V ≤ V_{IN} ≤ 6.5 V		0.003		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	5 mA ≤ I_{OUT} ≤ 2 A		0.03		%/A
V_{DO}	Dropout voltage	V_{IN} ≥ 1.4 V, 0.8 V ≤ V_{OUT} ≤ 5.0 V, I_{OUT} = 2 A, V_{FB} = 0.8 V – 3%			400	mV

(1) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
(2) The device is not tested under conditions where V_{IN} > V_{OUT} + 2.5 V and I_{OUT} = 2 A because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.

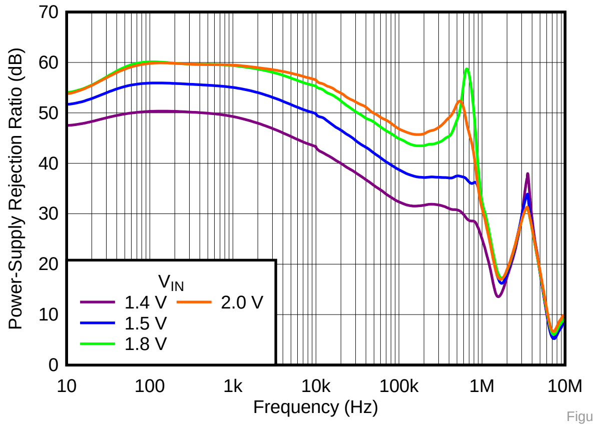
Electrical Characteristics (continued)

over operating temperature range (T_J = –40°C to +125°C), V_{IN} = 1.4 V, $V_{OUT(TARGET)}$ = 0.8 V, I_{OUT} = 50 mA, V_{EN} = 1.4 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, SS_CTRL = GND, PG pin pulled up to V_{INx} with 100 kΩ, and for each channel (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIM}	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(TARGET)}$, V_{IN} = $V_{OUT(TARGET)}$ + 300 mV	2.3	2.6	2.9	A
I_{GND}	GND pin current	Both channels enabled, per channel, V_{IN} = 6.5 V, I_{OUT} = 5 mA		2.1	3.5	mA
		Both channels enabled, per channel, V_{IN} = 1.4 V, I_{OUT} = 2 A			4	
I_{SDN}	Shutdown GND pin current	Both channels shutdown, per channel, PGx = (open), V_{IN} = 6.5 V, V_{EN} = 0.5 V		0.1	15	µA
I_{EN}	EN pin current	V_{IN} = 6.5 V, 0 V ≤ V_{EN} ≤ 6.5 V	–0.2		0.2	µA
$V_{IL(EN)}$	EN pin low-level input voltage (device disabled)		0		0.4	V
$V_{IH(EN)}$	EN pin high-level input voltage (device enabled)		1.1		6.5	V
I_{SS_CTRL}	SS_CTRL pin current	V_{IN} = 6.5 V, 0 V ≤ V_{SS_CTRL} ≤ 6.5 V	–0.2		0.2	µA
$V_{IT(PG)}$	PG pin threshold	For PG transitioning low with falling V_{OUT}, expressed as a percentage of $V_{OUT(TARGET)}$	82%	88.9%	93%	
$V_{hys(PG)}$	PG pin hysteresis	For PG transitioning high with rising V_{OUT}, expressed as a percentage of $V_{OUT(TARGET)}$		1%		
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)			0.4	V
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > $V_{IT(PG)}$, V_{PG} = 6.5 V			1	µA
$I_{NR/SS}$	NR/SS pin charging current	$V_{NR/SS}$ = GND, 1.4 V ≤ V_{IN} ≤ 6.5 V, V_{SS_CTRL} = GND	4.0	6.2	9.0	µA
		$V_{NR/SS}$ = GND, 1.4 V ≤ V_{IN} ≤ 6.5 V, V_{SS_CTRL} = V_{IN}	65	100	150	
I_{FB}	FB pin leakage current	V_{IN} = 6.5 V, V_{FB} = 0.8 V	–100		100	nA
PSRR	Power-supply ripple rejection	f = 500 kHz, V_{INx} = 2.0 V, V_{OUT} = 1.2 V, I_{OUT} = 2 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF		40		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 1.8 V, V_{OUT} = 0.8 V, I_{OUT} = 2.0 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF		4.6		μV_{RMS}
	Noise spectral density	f = 10 kHz, V_{IN} = 1.8 V, V_{OUT} = 0.8 V, I_{OUT} = 2.0 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF		15		$nV/\sqrt{Hz}$
R_{diss}	Output active discharge resistance	V_{EN} = GND		250		Ω
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		

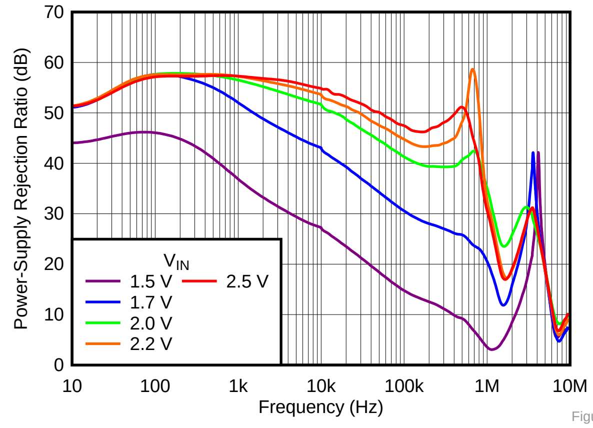
6.6 Typical Characteristics

at T_J = 25°C, 1.4 V ≤ V_{IN} ≤ 6.5 V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3 V, V_{OUT} = 0.8 V, SS_CTRL = GND, I_{OUT} = 5 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 0 nF, PG pin pulled up to V_{OUT} with 100 kΩ, and SS_CTRL = GND (unless otherwise noted)



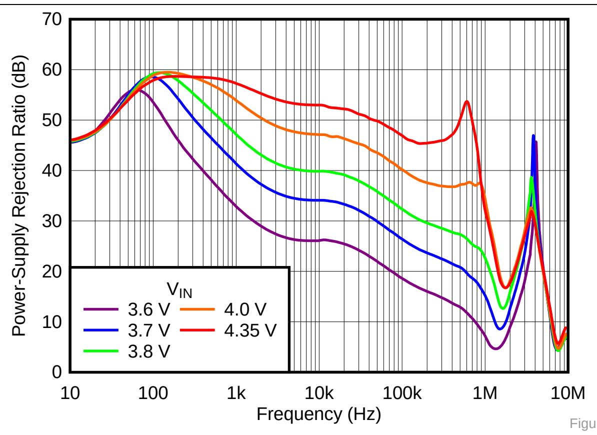
V_{OUT} = 0.8 V, I_{OUT} = 2.0 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF

图 1. PSRR vs Frequency and Input Voltage



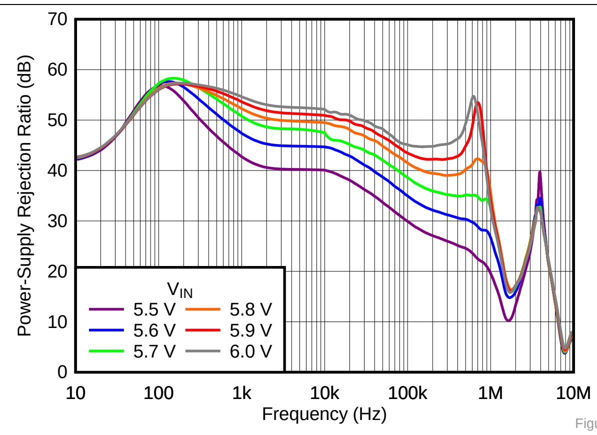
V_{OUT} = 1.2 V, I_{OUT} = 2.0 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF

图 2. PSRR vs Frequency and Input Voltage



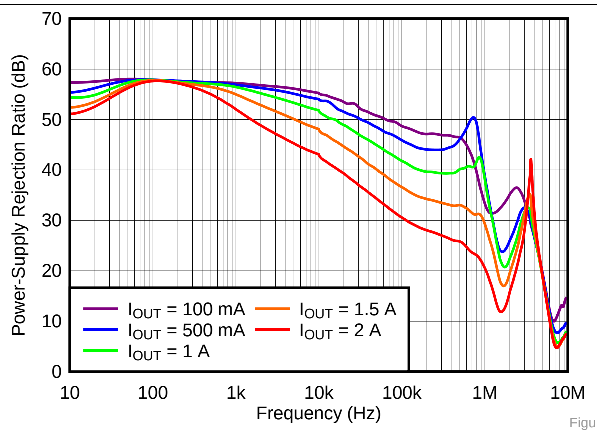
V_{OUT} = 3.3 V, I_{OUT} = 2.0 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF

图 3. PSRR vs Frequency and Input Voltage



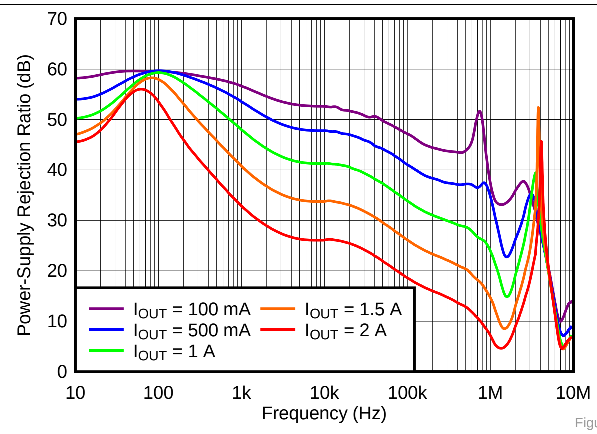
V_{OUT} = 5 V, I_{OUT} = 2.0 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF

图 4. PSRR vs Frequency and Input Voltage



V_{OUT} = 1.2 V, V_{IN} = V_{EN} = 1.7 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF

图 5. PSRR vs Frequency and Output Current

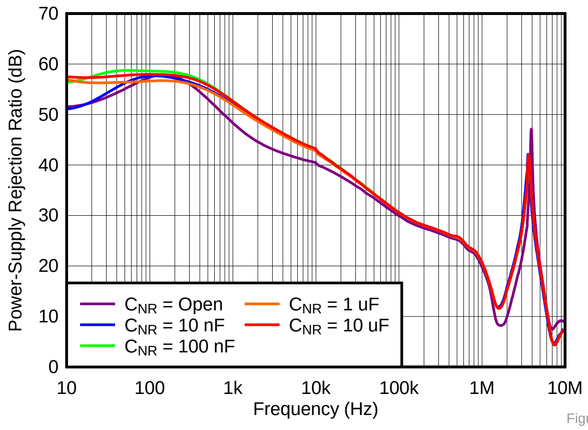


V_{OUT} = 3.3 V, V_{IN} = V_{EN} = 3.8 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF

图 6. PSRR vs Frequency and Output Current

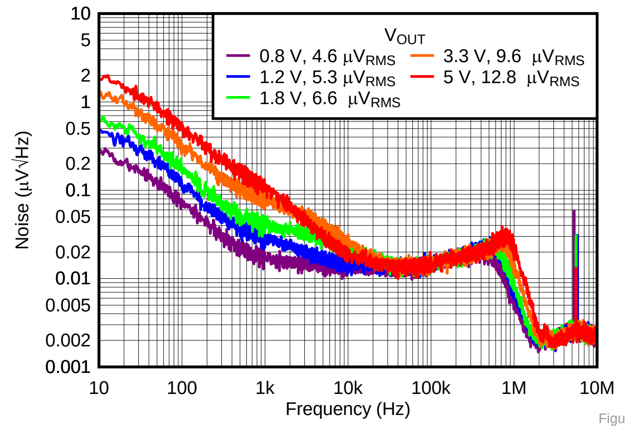
Typical Characteristics (接下页)

at T_J = 25°C, 1.4 V ≤ V_{IN} ≤ 6.5 V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3 V, V_{OUT} = 0.8 V, SS_CTRL = GND, I_{OUT} = 5 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 0 nF, PG pin pulled up to V_{OUT} with 100 kΩ, and SS_CTRL = GND (unless otherwise noted)



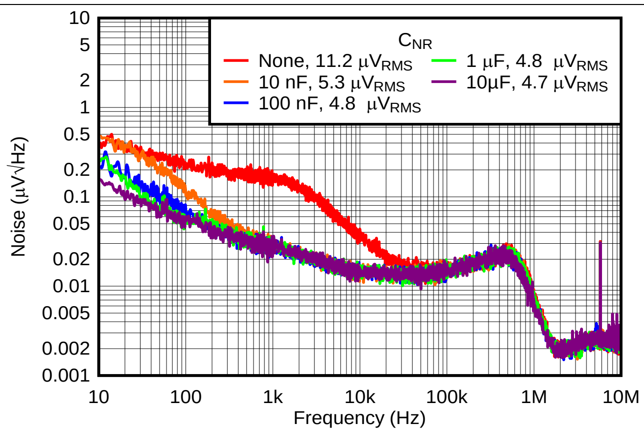
V_{OUT} = 1.2 V, V_{IN} = V_{EN} = 1.7 V, I_{OUT} = 2.0 A, C_{OUT} = 22 µF, C_{FF} = 10 nF

图 7. PSRR vs Frequency and $C_{NR/SS}$



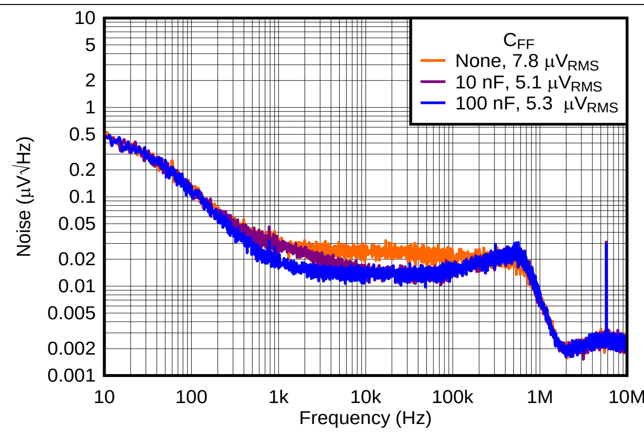
V_{IN} = V_{OUT} + 1.0 V, I_{OUT} = 2.0 A, C_{IN} = C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF, V_{RMS} BW = 10 Hz to 100 kHz

图 8. Spectral Noise Density vs Frequency and Output Voltage



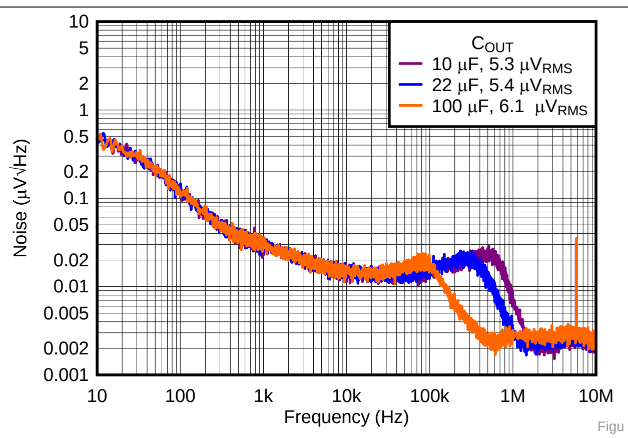
V_{IN} = 2.2 V, V_{OUT} = 1.2 V, I_{OUT} = 2.0 A, C_{IN} = C_{OUT} = 22 µF, C_{FF} = 10 nF, V_{RMS} BW = 10 Hz to 100 kHz

图 9. Spectral Noise Density vs Frequency and $C_{NR/SS}$



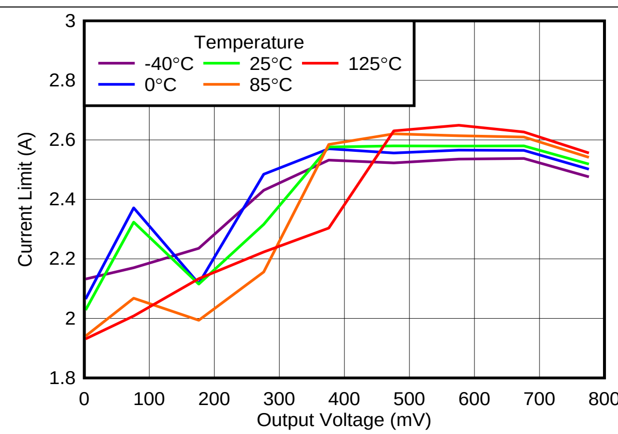
V_{IN} = 2.2 V, V_{OUT} = 1.2 V, I_{OUT} = 2.0 A, C_{IN} = C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF, V_{RMS} BW = 10 Hz to 100 kHz

图 10. Spectral Noise Density vs Frequency and C_{FF}



V_{IN} = 2.2 V, V_{OUT} = 1.2 V, I_{OUT} = 2.0 A, C_{IN} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF, V_{RMS} BW = 10 Hz to 100 kHz

图 11. Spectral Noise Density vs Frequency and C_{OUT}



V_{IN} = 1.4 V, V_{OUT} = 0.8 V

图 12. Current Limit Foldback

Typical Characteristics (接下页)

at T_J = 25°C, 1.4 V ≤ V_{IN} ≤ 6.5 V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3 V, V_{OUT} = 0.8 V, SS_CTRL = GND, I_{OUT} = 5 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 0 nF, PG pin pulled up to V_{OUT} with 100 kΩ, and SS_CTRL = GND (unless otherwise noted)

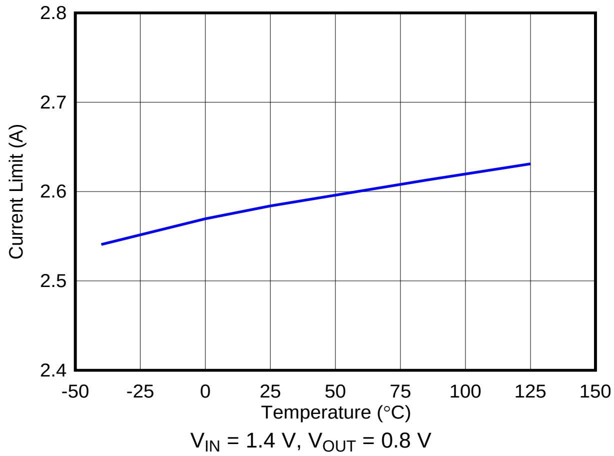


图 13. Current Limit vs Temperature

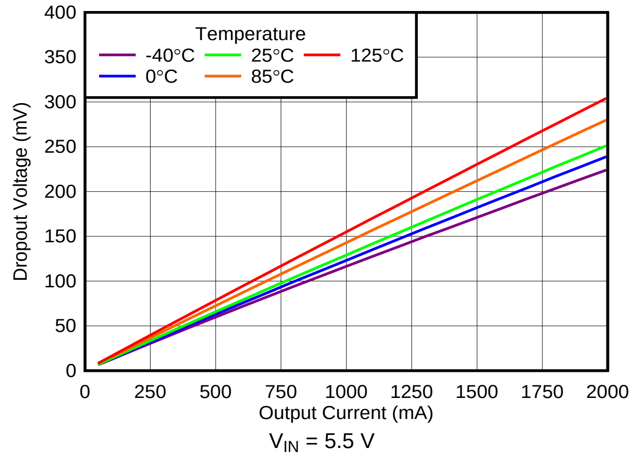


图 14. Dropout Voltage vs Output Current

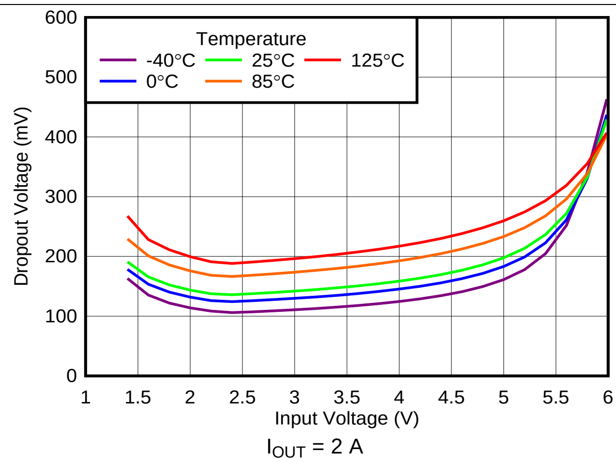


图 15. Dropout Voltage vs Input Voltage

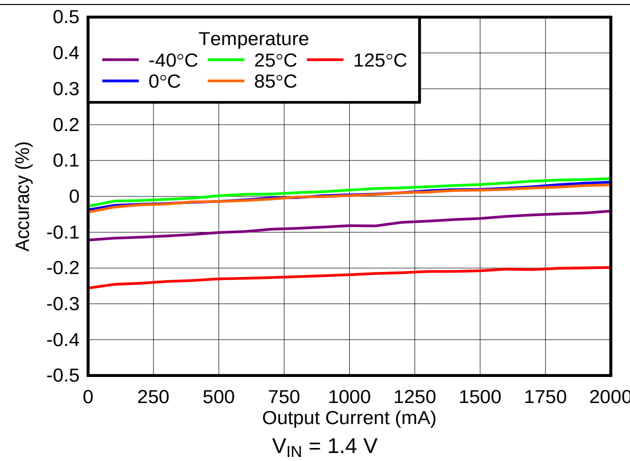


图 16. Load Regulation

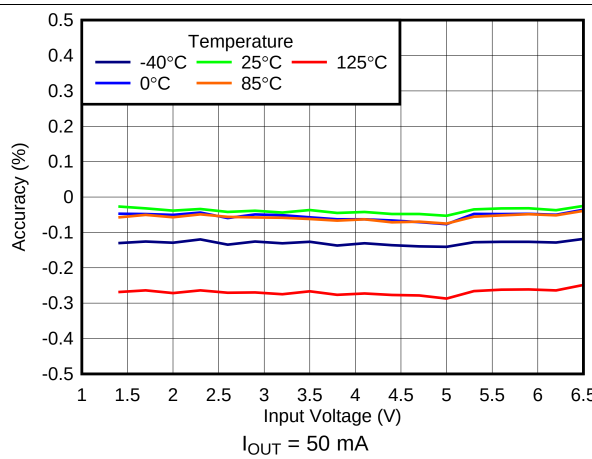


图 17. Line Regulation

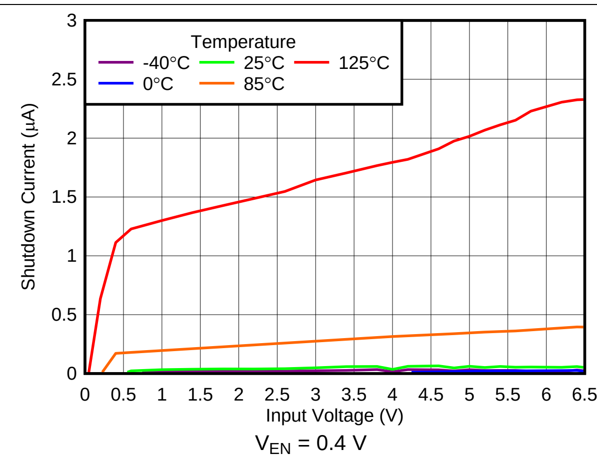


图 18. Shutdown Current vs Input Voltage

Typical Characteristics (接下页)

at T_J = 25°C, 1.4 V ≤ V_{IN} ≤ 6.5 V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3 V, V_{OUT} = 0.8 V, SS_CTRL = GND, I_{OUT} = 5 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 0 nF, PG pin pulled up to V_{OUT} with 100 kΩ, and SS_CTRL = GND (unless otherwise noted)

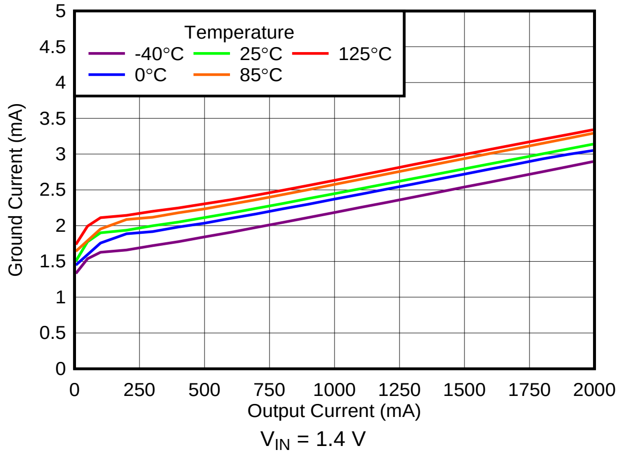


图 19. Ground Current vs Output Current

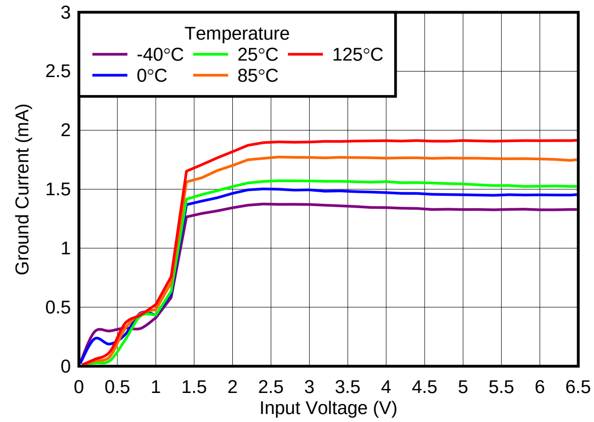


图 20. Ground Current vs Input Voltage

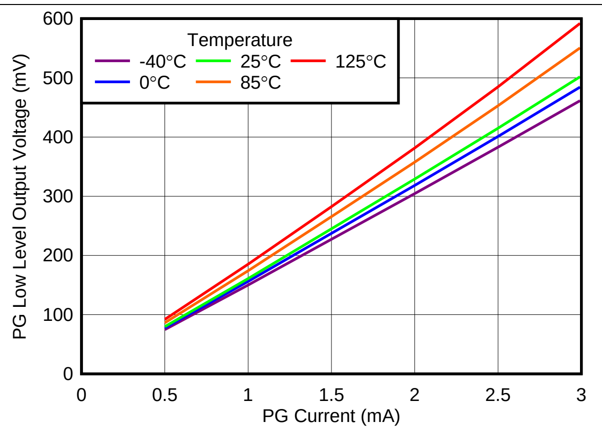


图 21. PG Low Level Voltage vs PG Current (V_{IN} = 1.4 V)

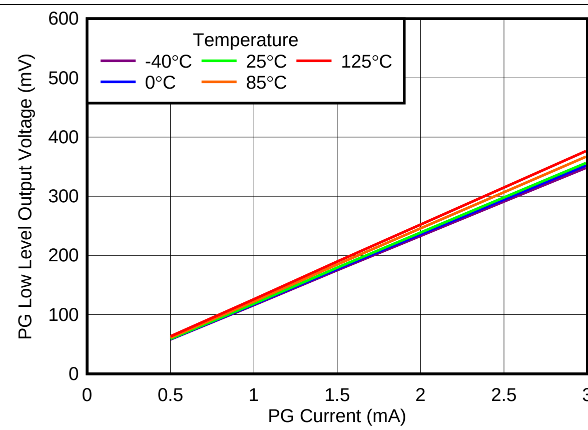


图 22. PG Low Level Voltage vs PG Current (V_{IN} = 6.5 V)

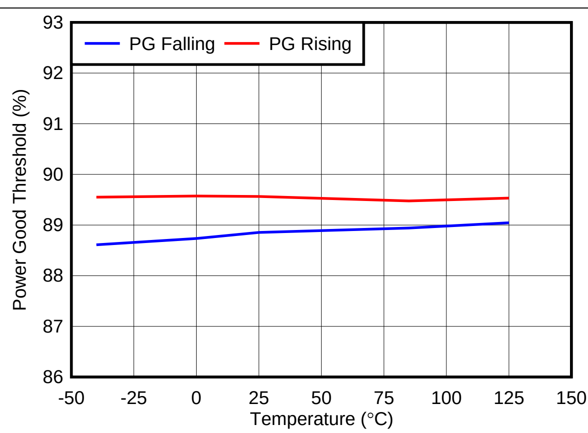


图 23. PG Threshold vs Temperature

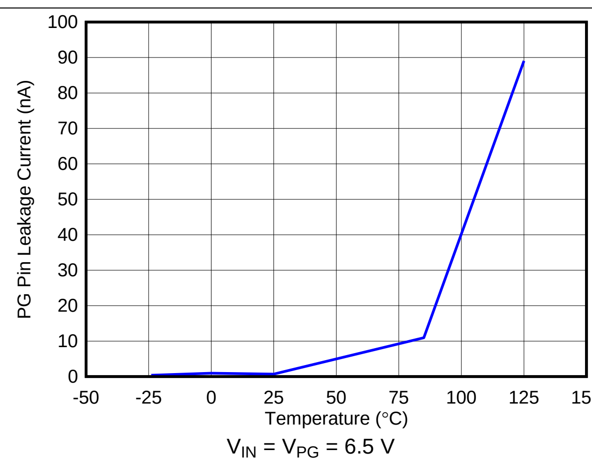


图 24. PG Leakage Current vs Temperature

Typical Characteristics (接下页)

at T_J = 25°C, 1.4 V ≤ V_{IN} ≤ 6.5 V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3 V, V_{OUT} = 0.8 V, SS_CTRL = GND, I_{OUT} = 5 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 0 nF, PG pin pulled up to V_{OUT} with 100 kΩ, and SS_CTRL = GND (unless otherwise noted)

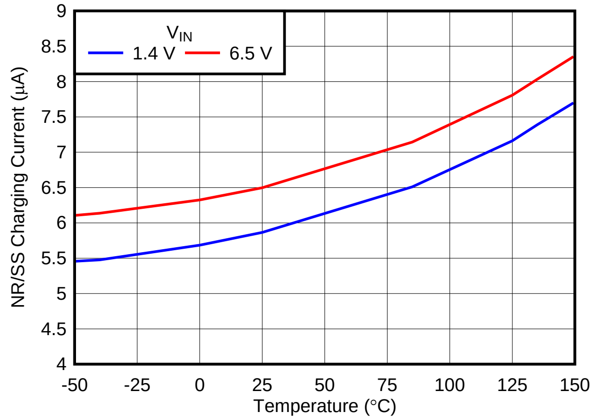


图 25. Soft-Start Current vs Temperature (SS_CTRL = GND)

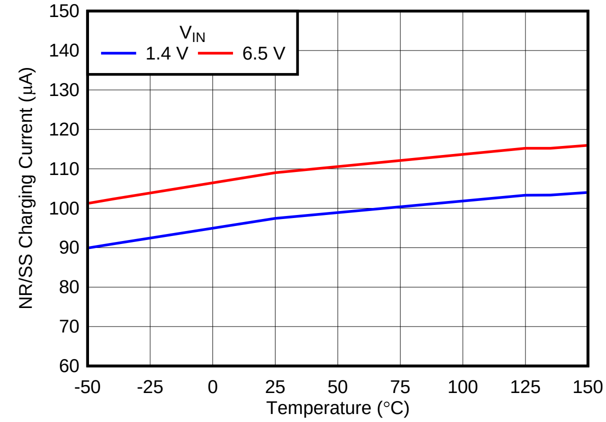


图 26. Soft-Start Current vs Temperature (SS_CTRL = V_{IN})

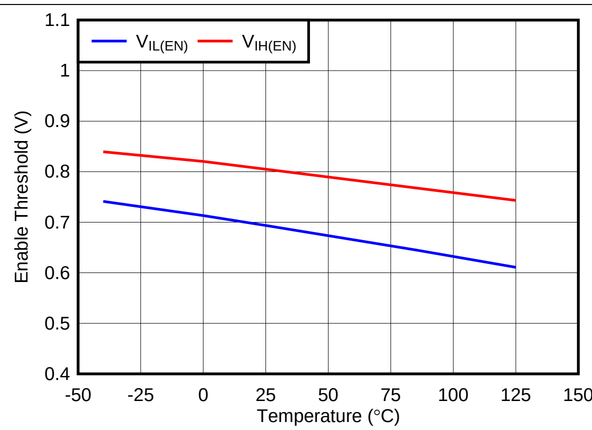


图 27. Enable Threshold vs Temperature

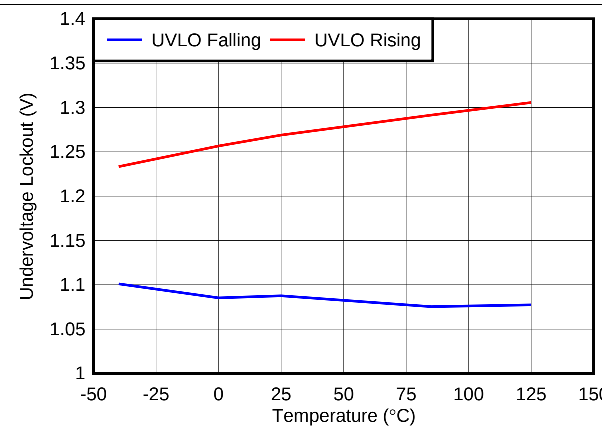
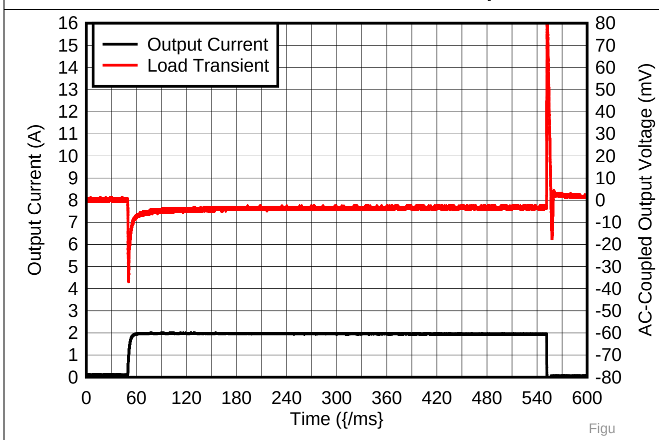
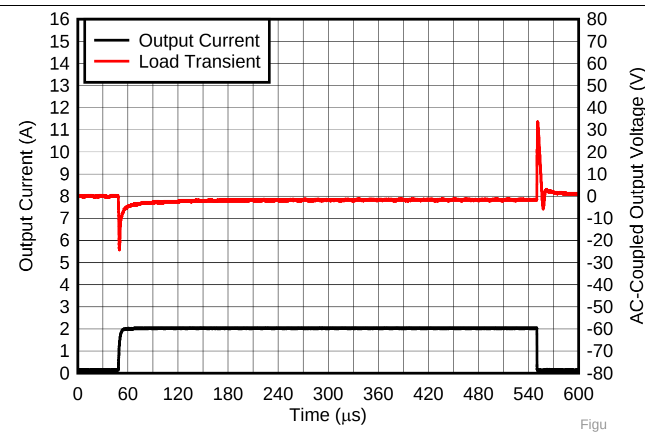


图 28. Input UVLO Threshold vs Temperature



V_{IN} = 1.5 V, I_{OUT} = 100 mA to 2 A to 100 mA at 1 A/µs, C_{OUT} = 22 µF, V_{PG} = V_{OUT}

图 29. Load Transient Response (V_{OUT} = 1.2 V)

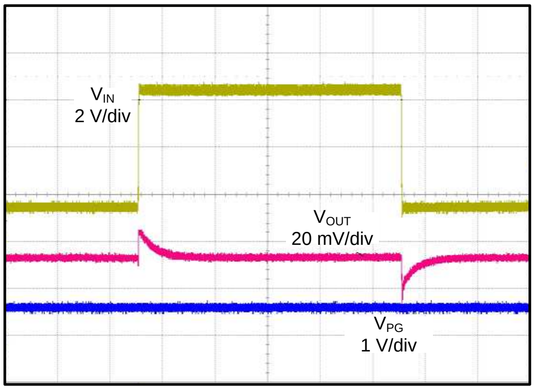


V_{IN} = 5.5 V, I_{OUT} = 100 mA to 2 A to 100 mA at 1 A/µs, C_{OUT} = 22 µF, V_{PG} = V_{OUT}

图 30. Load Transient Response (V_{OUT} = 5.0 V)

Typical Characteristics (接下页)

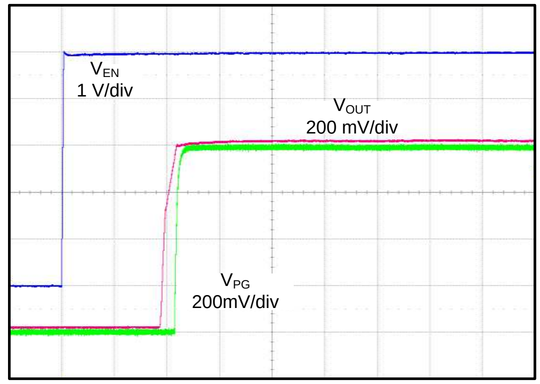
at T_J = 25°C, 1.4 V ≤ V_{IN} ≤ 6.5 V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3 V, V_{OUT} = 0.8 V, SS_CTRL = GND, I_{OUT} = 5 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 0 nF, PG pin pulled up to V_{OUT} with 100 kΩ, and SS_CTRL = GND (unless otherwise noted)



Time (200 µs/div)

V_{IN} = 1.4 V to 6.5 V to 1.4 V at 2 V/µs, V_{OUT} = 0.8 V, I_{OUT} = 2 A, $C_{NR/SS}$ = C_{FF} = 10 nF, V_{PG} = V_{OUT}

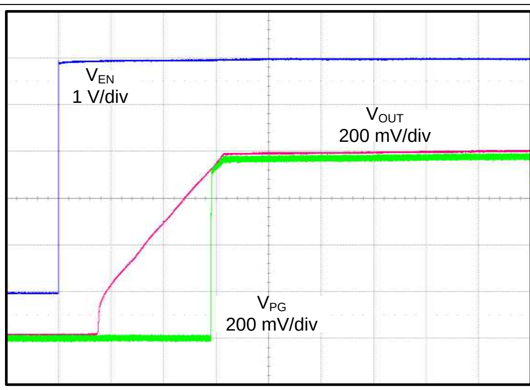
图 31. Line Transient



Time (50 µs/div)

V_{IN} = 1.4 V, V_{PG} = V_{OUT}

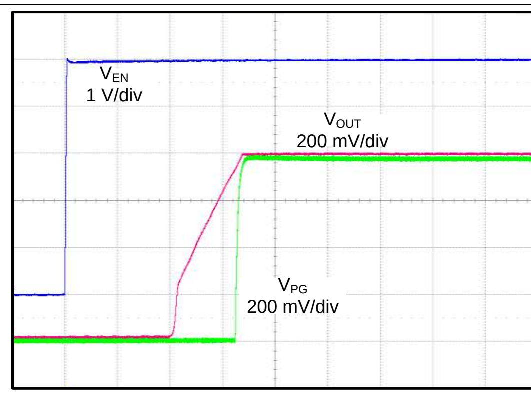
图 32. Start-Up (SS_CTRL = GND, $C_{NR/SS}$ = 0 nF)



Time (500 µs/div)

V_{IN} = 1.4 V, V_{PG} = V_{OUT}

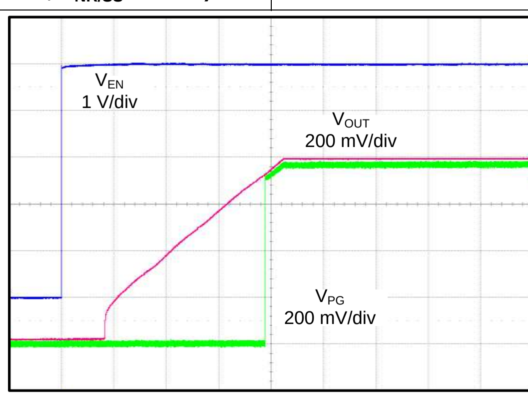
图 33. Start-Up (SS_CTRL = GND, $C_{NR/SS}$ = 10 nF)



Time (50 µs/div)

V_{IN} = 1.4 V, V_{PG} = V_{OUT}

图 34. Start-Up (SS_CTRL = V_{IN}, $C_{NR/SS}$ = 10 nF)



Time (2 ms/div)

V_{IN} = 1.4 V, V_{PG} = V_{OUT}

图 35. Start-Up (SS_CTRL = V_{IN}, $C_{NR/SS}$ = 1 µF)

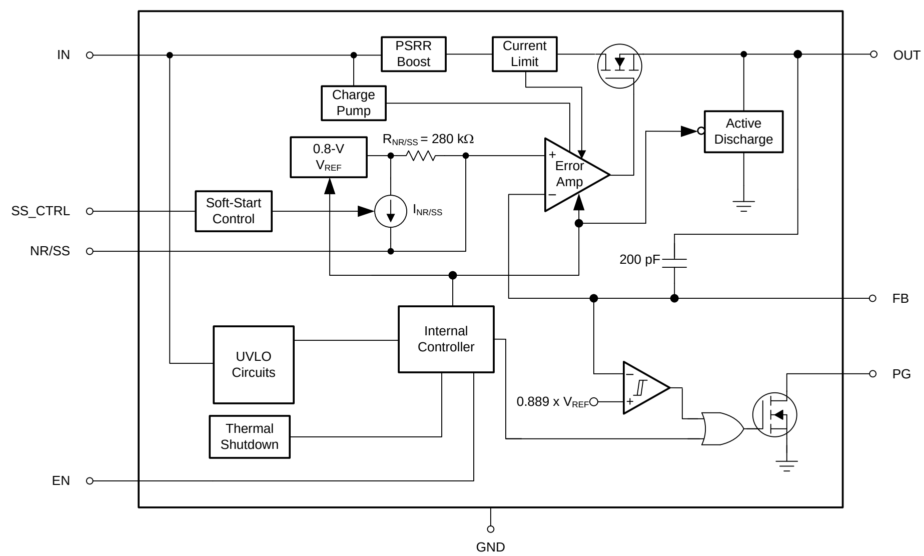
7 Detailed Description

7.1 Overview

The TPS7A92 is a low-noise, high PSRR, low dropout (LDO) regulator capable of sourcing a 2-A load with only 400 mV of maximum dropout. The TPS7A92 can operate down to a 1.4-V input voltage and a 0.8-V output voltage. This combination of low-noise, high PSRR, and low dropout voltage makes the device an ideal LDO to power a multitude of loads from noise-sensitive communication components in high-speed communications applications to high-end microprocessors or field-programmable gate arrays (FPGAs).

As shown in the *Functional Block Diagram* section, the TPS7A92 linear regulator features a low-noise, 0.8-V internal reference that can be filtered externally to obtain even lower output noise. The internal protection circuitry (such as the undervoltage lockout) prevents the device from turning on before the input is high enough to ensure accurate regulation. Foldback current limiting is also included, allowing the output to source the rated output current when the output voltage is in regulation but reduces the allowable output current during short-circuit conditions. The internal power-good detection circuit allows users to sequence down-stream supplies and be alerted if the output voltage is below a regulation threshold.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Enable

The enable pin for the TPS7A92 is active high. The output voltage is enabled when the enable pin voltage is greater than $V_{IH(EN)}$ and disabled with the enable pin voltage is less than $V_{IL(EN)}$. If independent control of the output voltage is not needed, then connect the enable pin to the input.

The TPS7A92 has an internal pulldown MOSFET that connects a discharge resistor from V_{OUT} to ground when the device is disabled to actively discharge the output voltage.

7.3.2 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as the V_{IN} – V_{OUT} voltage at the rated current (I_{RATED}) of 2 A, where the pass-FET is fully on and in the ohmic region of operation. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain in regulation. If the input falls below the nominal output regulation, then the output follows the input.

Feature Description (接下页)

Dropout voltage is determined by the $R_{DS(ON)}$ of the pass-FET. Therefore, if the LDO operates below the rated current, then the V_{DO} for that current scales accordingly. The $R_{DS(ON)}$ for the TPS7A92 can be calculated using 公式 1:

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

7.3.3 Output Voltage Accuracy

Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. The TPS7A92 features an output voltage accuracy of 1% that includes the errors introduced by the internal reference, load regulation, and line regulation variance across the full range of rated load and line operating conditions over temperature, as specified by the *Electrical Characteristics* table. Output voltage accuracy also accounts for all variations between manufacturing lots.

7.3.4 High Power-Supply Ripple Rejection (PSRR)

PSRR is a measure of how well the LDO control loop rejects noise from the input source to make the dc output voltage as noise-free as possible across the frequency spectrum (usually measured from 10 Hz to 10 MHz). Even though PSRR is a loss in noise signal amplitude, the PSRR curves in the *Typical Characteristics* section are shown as positive values in decibels (dB) for convenience. 公式 2 gives the PSRR calculation as a function of frequency where input noise voltage [$V_{IN}(f)$] and output noise voltage [$V_{OUT}(f)$] are the amplitudes of the respective sinusoidal signals.

$$\text{PSRR (dB)} = 20\ \text{Log}_{10}\left(\frac{V_{IN}(f)}{V_{OUT}(f)}\right) \quad (2)$$

Noise that couples from the input to the internal reference voltage is a primary contributor to reduced PSRR performance. Using a noise-reduction capacitor is recommended to filter unwanted noise from the input voltage, which creates a low-pass filter with an internal resistor to improve PSRR performance at lower frequencies.

LDOs are often employed not only as a step-down regulators, but also to provide exceptionally clean power rails for noise-sensitive components. This usage is especially true for the TPS7A92, which features an innovative circuit to boost the PSRR between 200 kHz and 1 MHz. This boost circuit helps further filter switching noise from switching-regulators that operate in this region; see 图 1. To achieve the maximum benefit of this PSRR boost circuit, using a capacitor with a minimum impedance in the 100-kHz to 1-MHz band is recommended.

7.3.5 Low Output Noise

LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits. The TPS7A92 is designed for system applications where minimizing noise on the power-supply rail is critical to system performance. This scenario is the case for phase-locked loop (PLL)-based clocking circuits where minimum phase noise is all important, or in test and measurement systems where even small power-supply noise fluctuations can distort instantaneous measurement accuracy.

The TPS7A92 includes a low-noise reference ensuring minimal output noise in normal operation. Further improvements can be made by adding a noise reduction capacitor ($C_{NR/SS}$), a feedforward capacitor (C_{FF}), or a combination of the two. See the *Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)* and *Feed-Forward Capacitor (C_{FF})* sections for additional design information.

For more information on noise and noise measurement, see the *How to Measure LDO Noise* white paper.

7.3.6 Output Soft-Start Control

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after the EN and UVLO thresholds are exceeded. The noise-reduction capacitor ($C_{NR/SS}$) serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on. Larger values for the noise-reduction capacitors decrease the noise but also result in a slower output turn-on ramp rate.

Feature Description (接下页)

The TPS7A92 features an SS_CTRL pin. When the SS_CTRL pin is grounded, the charging current for the NR/SS pin is 6.2 µA (typ); when this pin is connected to IN, the charging current for the NR/SS pin is increased to 100 µA (typ). The higher current allows the use of a much larger noise-reduction capacitor and maintains a reasonable startup time. 图 36 shows a simplified block diagram of the soft-start circuit. The switch SW is opened to turn off the $I_{NR/SS}$ current source after V_{FB} reaches approximately 97% of V_{REF}. The final 3% of $V_{NR/SS}$ is charged through the noise reduction resistor (R_{NR}), which creates an RC delay. R_{NR} is approximately 280 kΩ and applications that require the highest accuracy when using a large value $C_{NR/SS}$ must take this RC delay into account.

If a noise-reduction capacitor is not used on the NR/SS pin, tying the SS_CTRL pin to the IN pin can result in output voltage overshoot of approximately 10%. This overshoot is minimized by either connecting the SS_CTRL pin to GND or using a capacitor on the NR/SS pin.

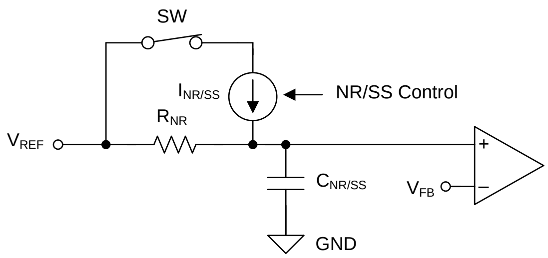


图 36. Simplified Soft-Start Circuit

7.3.7 Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the feedback pin voltage falls below the PG threshold voltage ($V_{IT(PG)}$), the PG pin open-drain output engages and pulls the PG pin close to GND. When the feedback voltage exceeds the $V_{IT(PG)}$ threshold by an amount greater than $V_{HYS(PG)}$, the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices. Using a pullup resistor from 10 kΩ to 100 kΩ is recommended. Using an external reset device such as the TPS3890 is also recommended in applications where high accuracy is needed or in applications where microprocessor induced resets are needed.

When using a feed-forward capacitor (C_{FF}), the time constant for the LDO startup is increased whereas the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue and to receive a valid PG output, make sure that the time constant of both the LDO startup and the power-good output are matching, which can be done by adding a capacitor in parallel with the power-good pullup resistor. For more information, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

The state of PG is only valid when the device is operating above the minimum input voltage of the device and power good is asserted regardless of the output voltage state when the input voltage falls below the UVLO threshold minus the UVLO hysteresis. 图 37 illustrates a simplified block diagram of the power-good circuit. When the input voltage falls below approximately 0.8 V, there is not enough gate drive voltage to keep the open-drain, power-good device turned on and the power-good output is pulled high. Connecting the power-good pullup resistor to the output voltage can help minimize this effect.

Feature Description (接下页)

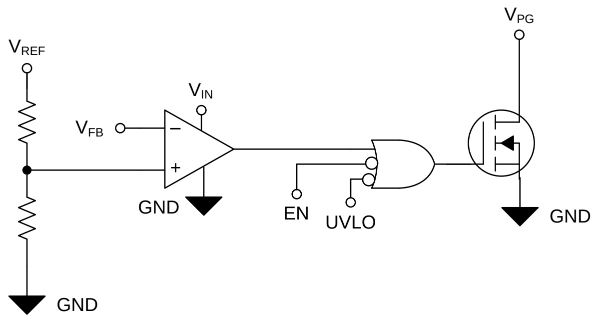


图 37. Simplified PG Circuit

7.3.8 Internal Protection Circuitry

7.3.8.1 Undervoltage Lockout (UVLO)

The TPS7A92 has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has approximately 290 mV of hysteresis.

The UVLO circuit responds quickly to glitches on V_{IN} and disables the output of the device if this rail starts to collapse too quickly. Use an input capacitor that is large enough to slow input transients to less then two volts per microsecond.

7.3.8.2 Internal Current Limit (I_{CL})

The internal current-limit circuit is used to protect the LDO against transient high-load current faults or shorting events. The LDO is not designed to operate in current limit under steady-state conditions. During an overcurrent event where the output voltage is pulled 10% below the regulated output voltage, the LDO sources a constant current as specified in the *Electrical Characteristics* table. When the output voltage falls, the amount of output current is reduced to better protect the device. During a hard short-circuit event, the current is reduced to approximately 2.2 A. See 图 12 in the *Typical Characteristics* section for more information about the current-limit foldback behavior. Note also that when a current-limit event occurs, the LDO begins to heat up because of the increase in power dissipation. The increase in heat can trigger the integrated thermal shutdown protection circuit.

7.3.8.3 Thermal Protection

The TPS7A92 contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. Thermal shutdown occurs when the thermal junction temperature (T_J) of the pass-FET exceeds 160°C (typical). Thermal shutdown hysteresis assures that the LDO again resets (turns on) when the temperature falls to 140°C (typical). The thermal time-constant of the semiconductor die is fairly short, and thus the output turns on and off at a high rate when thermal shutdown is reached until power dissipation is reduced.

The internal protection circuitry of the TPS7A92 is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A92 into thermal shutdown degrades device reliability.

For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the thermal margin in a given layout, increase the ambient temperature until the thermal protection shutdown is triggered using worst-case load and highest input voltage conditions. For good reliability, thermal shutdown must occur at least 35°C above the maximum expected ambient temperature condition for the application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

7.4 Device Functional Modes

表 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

表 1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal (1)	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Dropout (1)	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled (2)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{IL(EN)}$	—	$T_J > T_{sd}$

(1) All table conditions must be met.
(2) The device is disabled when any condition is met.

7.4.1 Normal Operation

The device regulates to the nominal output voltage when all of the following conditions are met.

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased below the enable falling threshold
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{sd}$)

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, right after being in a normal regulation state, but *not* during startup), the pass-FET is driven as hard as possible. When the input voltage returns to $V_{IN} \geq V_{OUT(NOM)} + V_{DO}$, V_{OUT} can overshoot for a short period of time if the input voltage slew rate is greater than 0.1 V/µs.

7.4.3 Disabled

The output of the TPS7A92 can be shutdown by forcing the enable pin below 0.4 V. When disabled, the pass device is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal resistor from the output to ground.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A92 is a linear voltage regulator operating from 1.4 V to 6.5 V on the input and regulates voltages between 0.8 V to 5.0 V within 1% accuracy and a 2-A maximum output current. Efficiency is defined by the ratio of output voltage to input voltage because the TPS7A92 is a linear voltage regulator. To achieve high efficiency, the dropout voltage (V_{IN} – V_{OUT}) must be as small as possible, thus requiring a very low dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

8.1.1 Adjustable Output

The output voltage of the TPS7A9201 can be adjusted from 0.8 V to 5.2 V by using a resistor divider network as shown in 图 38.

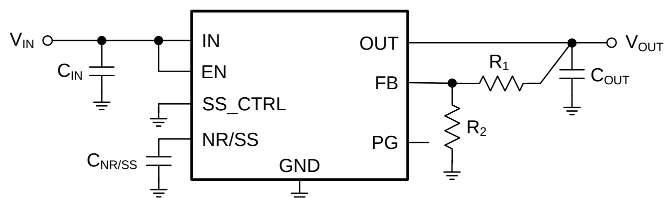


图 38. Adjustable Operation

R_1 and R_2 can be calculated for any output voltage range using 公式 3. This resistive network must provide a current greater than or equal to 5 µA for optimum noise performance.

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right), \quad \text{where } \frac{\left|V_{REF(max)}\right|}{R_2} > 5\ \mu A \tag{3}$$

If greater voltage accuracy is required, take into account the output voltage offset contribution resulting from the feedback pin current (I_{FB}) and use 0.1%-tolerance resistors.

表 2 lists the resistor combination required to achieve a few of the most common rails using commercially-available, 0.1%-tolerance resistors to maximize nominal voltage accuracy and also abiding to the formula given in 公式 3.

Application Information (接下页)

表 2. Recommended Feedback-Resistor Values

$V_{OUT(TARGET)}$ (V)	FEEDBACK RESISTOR VALUES (1)		CALCULATED OUTPUT VOLTAGE (V)
	R_1 (kΩ)	R_2 (kΩ)	
0.8	Short	Open	0.800
1.00	2.55	10.2	1.000
1.20	5.9	11.8	1.200
1.50	9.31	10.7	1.496
1.80	1.87	1.5	1.797
1.90	15.8	11.5	1.899
2.50	2.43	1.15	2.490
3.00	3.16	1.15	2.998
3.30	3.57	1.15	3.283
5.00	10.5	2	5.00

(1) R_1 is connected from OUT to FB; R_2 is connected from FB to GND; see 图 38.

8.1.2 Start-Up

8.1.2.1 Enable (EN) and Undervoltage Lockout (UVLO)

The TPS7A92 only turns on when EN and UVLO are above the respective voltage thresholds. The TPS7A92 has an independent UVLO circuit that monitors the input voltage to allow a controlled and consistent turn on and off. The UVLO has approximately 290 mV of hysteresis to prevent the device from turning off if the input drops during turn on. The EN signal allows independent logic-level turn-on and shutdown of the LDO when the input voltage is present. Connecting EN directly to IN is recommended if independent turn-on is not needed.

The TPS7A92 has an internal pulldown MOSFET that connects a discharge resistor from V_{OUT} to ground when the device is disabled to actively discharge the output voltage.

8.1.2.2 Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The $C_{NR/SS}$ capacitor serves a dual purpose of both reducing output noise and setting the soft-start ramp during turn-on.

8.1.2.2.1 Noise Reduction

For low-noise applications, the $C_{NR/SS}$ capacitor forms an RC filter for filtering output noise that is otherwise amplified by the control loop. For low-noise applications, a $C_{NR/SS}$ of between 10 nF to 10 µF is recommended. Larger values for $C_{NR/SS}$ can be used; however, above 1 µF there is little benefit in lowering the output voltage noise for frequencies above 10 Hz.

8.1.2.2.2 Soft-Start and Inrush Current

Soft-start refers to the gradual ramp-up characteristic of the output voltage after the EN and UVLO thresholds are exceeded. Reducing how quickly the output voltage increases during startup also reduces the amount of current needed to charge the output capacitor, referred to as inrush current. Inrush current is defined as the current going into the LDO during start-up. Inrush current consists of the load current, the current used to charge the output capacitor, and the ground pin current (that contributes very little to inrush current). This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, the inrush current can be estimated by 公式 4:

$$I_{OUT}(t) = \left(\frac{C_{OUT} \times dV_{OUT}(t)}{dt} \right) + \left(\frac{V_{OUT}(t)}{R_{LOAD}} \right)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t)/dt$ is the slope of the V_{OUT} ramp and
- R_{LOAD} is the resistive load impedance (4)

The TPS7A92 features a monotonic, voltage-controlled soft-start that is set by the user with an external capacitor ($C_{NR/SS}$). This soft-start helps reduce inrush current, minimizing load transients to the input power bus that can cause potential start-up initialization problems when powering FPGAs, digital signal processors (DSPs), or other high current loads.

To achieve a monotonic start-up, the TPS7A92 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds approximately 97% of the internal reference. The final 3% of $V_{NR/SS}$ is charged through the noise-reduction resistor (R_{NR}), creating an RC delay. R_{NR} is approximately 280 kΩ and applications that require the highest accuracy when using a large value $C_{NR/SS}$ must take this RC delay into account.

The soft-start ramp time depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference (V_{REF}). The approximate soft-start ramp time (t_{SS}) can be calculated with 公式 5:

$$t_{SS} = (V_{REF} \times C_{NR/SS}) / I_{NR/SS} \quad (5)$$

The value for $I_{NR/SS}$ is determined by the state of the SS_CTRL pin. When the SS_CTRL pin is connected to GND, the typical value for the $I_{NR/SS}$ current is 6.2 µA. Connecting the SS_CTRL pin to IN increases the typical soft-start charging current to 100 µA. The larger charging current for $I_{NR/SS}$ is useful if shorter start-up times are needed (such as when using a large noise-reduction capacitor).

8.1.3 Capacitor Recommendation

The TPS7A92 is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good understanding of their limitations. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged precisely because the capacitance varies so widely. In all cases, ceramic capacitors vary a great deal with operating voltage and temperature and the design engineer must be aware of these characteristics. As a rule of thumb, ceramic capacitors are recommended to be derated by 50%. The input and output capacitors recommended herein account for a capacitance derating of 50%.

8.1.3.1 Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The TPS7A92 is designed and characterized for operation with ceramic capacitors of 10 µF or greater at the input and 22 µF or greater at the output. Locate the input and output capacitors as near as practical to the input and output pins to minimize the trace inductance from the capacitor to the device.

Attention must be given to the input capacitance to minimize transient input droop during startup and load current steps. Simply using very large ceramic input capacitances can cause unwanted ringing at the output if the input capacitor (in combination with the wire-lead inductance) creates a high-Q peaking effect during transients, which is why short, well-designed interconnect traces to the upstream supply are needed to minimize ringing. Damping of unwanted ringing can be accomplished by using a tantalum capacitor, with a few hundred milliohms of ESR, in parallel with the ceramic input capacitor. The UVLO circuit responds quickly to glitches on V_{IN} and disables the output of the device if this rail starts to collapse too quickly. Use an input capacitor that is large enough to slow input transients to less then two volts per microsecond.

8.1.3.1.1 Load-Step Transient Response

The load-step transient response is the output voltage response by the LDO to a step change in load current. The depth of charge depletion immediately after the load step is directly proportional to the amount of output capacitance. However, although larger output capacitances decrease any voltage dip or peak occurring during a load step, the control-loop bandwidth is also decreased, thereby slowing the response time.

The LDO cannot sink charge, therefore when the output load is removed or greatly reduced, the control loop must turn off the pass-FET and wait for any excess charge to deplete.

8.1.3.2 Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}), from the FB pin to the OUT pin is not required to achieve stability, a 10-nF, feed-forward capacitor improves the noise and PSRR performance. A higher capacitance C_{FF} can be used; however, the startup time is longer and the power-good signal can incorrectly indicate that the output voltage has settled. For a detailed description, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

8.1.4 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. P_D can be calculated using 公式 6:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (6)$$

An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage necessary for proper output regulation.

The primary heat conduction path for the DSK package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area should contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to 公式 7.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (7)$$

Unfortunately, the thermal resistance (θ_{JA}) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area and is only used as a relative measure of package thermal performance.

8.1.5 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the *Thermal Information* table and are used in accordance with 公式 8.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in 公式 6
- T_T is the temperature at the center-top of the device package and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge (8)

For a more detailed discussion on thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.2 Typical Application

This section discusses the implementation of the TPS7A92 to regulate from a 2-V input voltage to a 1.2-V output voltages for noise-sensitive loads. The schematic for this application circuit is provided in 图 39.

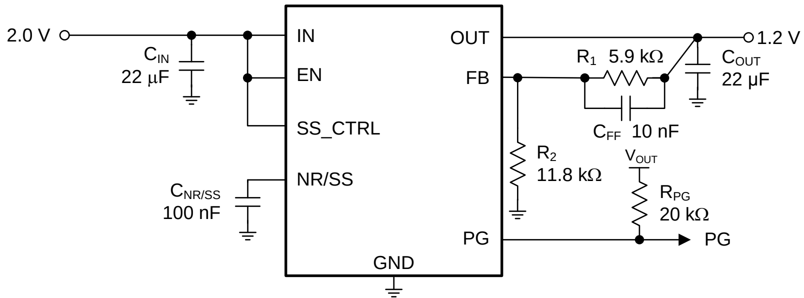


图 39. Application Example

8.2.1 Design Requirements

For the design example shown in 图 39, use the parameters listed in 表 3 as the input parameters.

表 3. Design Parameters

PARAMETER	APPLICATION REQUIREMENTS	DESIGN RESULTS
Input voltages (V_{IN})	2 V, ±3%, provided by the dc-dc converter switching at 700 kHz	1.4 V to 6.5 V
Maximum ambient operating temperature	55°C	124°C junction temperature
Output voltages (V_{OUT})	1.2 V, ±1%	1.2 V, ±1%
Output currents (I_{OUT})	1.5 A (max), 50 mA (min)	2.0 A (max), 5 mA (min)
RMS noise	< 5 μV_{RMS}, bandwidth = 10 Hz to 100 kHz	4.8 μV_{RMS}, bandwidth = 10 Hz to 100 kHz
PSRR at 700 kHz	> 40 dB	42 dB
Startup time	< 2 ms	800 µs (typ) 1.48 µs (max)

8.2.2 Detailed Design Procedure

The output voltage can be set to 1.2 V by selecting the correct values for R_1 and R_2; see 公式 3.

Input and output capacitors are selected in accordance with the *Capacitor Recommendation* section. Ceramic capacitances of 22 µF for both input and output are selected to help balance the charge needed during startup when charging the output capacitor, thus reducing the input voltage drop.

To satisfy the required startup time (t_{SS}) and still maintain low-noise performance, a 0.1-µF $C_{NR/SS}$ is selected for with SS_CTRL connected to V_{IN}. This value is calculated with 公式 9. Using the $I_{NR/SS(MAX)}$ and the smallest $C_{NR/SS}$ capacitance resulting from manufacturing variance (often ±20%) provides the fastest startup time, whereas using the $I_{NR/SS(MIN)}$ and the largest $C_{NR/SS}$ capacitance resulting from manufacturing variance provides the slowest startup time.

$$t_{SS} = (V_{REF} \times C_{NR/SS}) / I_{NR/SS} \quad (9)$$

With a 1.5-A maximum load, the internal power dissipation is 1.2 W, corresponding to a 91°C junction temperature rise. With a 55°C maximum ambient temperature, the junction temperature is at 124°C on the JEDEC standard high-K board. Connecting the thermal pad to more metal on the PCB than the standard JEDEC high-K board decreases the thermal resistance to the board and causes a decrease in the junction temperature of the device for a given power dissipation. To minimize noise, a feed-forward capacitance (C_{FF}) of 10 nF is selected.

See the *Layout* section for an example of how to layout the TPS7A92 to achieve best PSRR and noise.

8.2.3 Application Curves

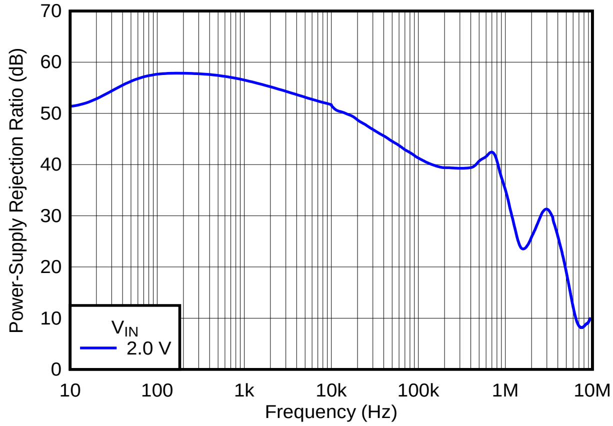


图 40. PSRR vs Frequency

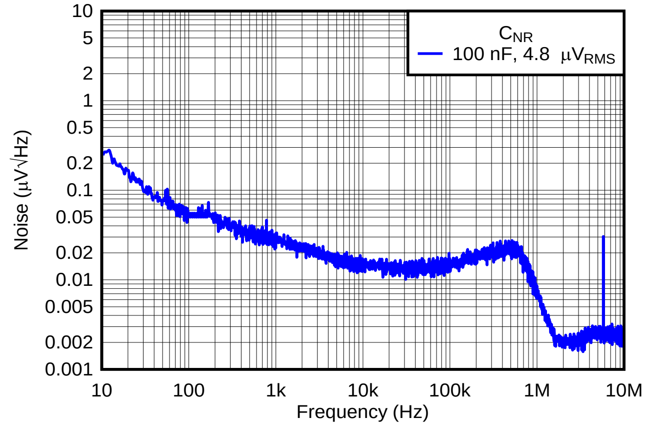


图 41. Output Noise vs Frequency

9 Power Supply Recommendations

The input of the TPS7A92 is designed to operate from an input voltage range between 1.4 V and 6.5 V and with an input capacitor of 10 µF. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors can be used to improve the output noise performance.

10 Layout

10.1 Layout Guidelines

General guidelines for linear regulator designs are to place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance.

10.1.1 Board Layout

To maximize the ac performance of the TPS7A92, following the layout example illustrated in 图 42 is recommended. This layout isolates the analog ground (AGND) from the noisy power ground. Components that must be connected to the quiet analog ground are the noise reduction capacitor ($C_{NR/SS}$) and the lower feedback resistor (R_2). These components must have a separate connection back to the power pad of the device for optimal output noise performance. Connect the GND pin directly to the thermal pad and not to any external plane.

To maximize the output voltage accuracy, the connection from the output voltage back to top output divider resistors (R_1) must be made as close as possible to the load. This method of connecting the feedback trace eliminates the voltage drop from the device output to the load.

To improve thermal performance, use an array of thermal vias to connect the thermal pad to the ground planes. Larger ground planes improve the thermal performance of the device and lowering the operating temperature of the device.

10.2 Layout Example

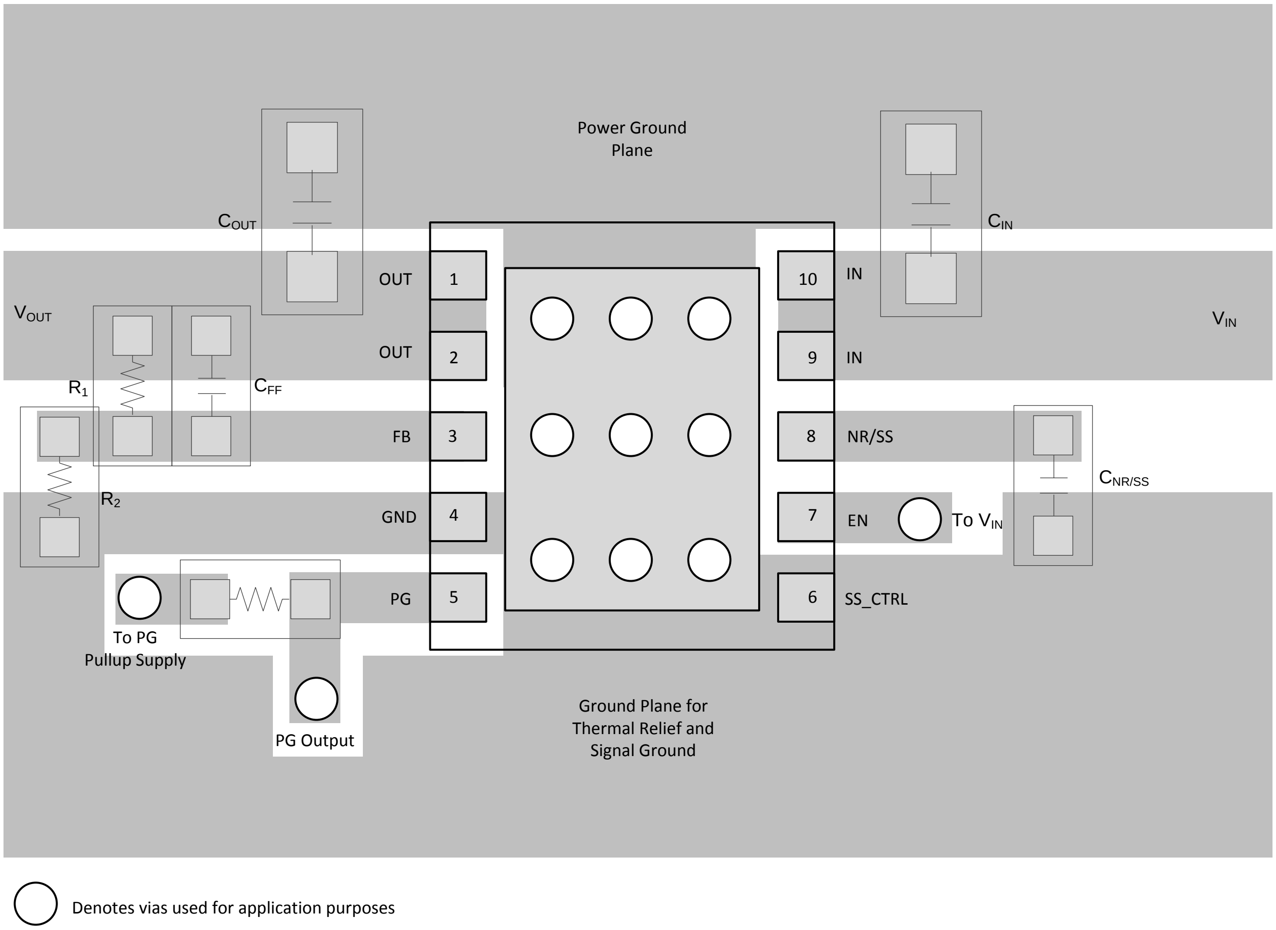


图 42. TPS7A92 Example Layout

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

我们提供了一款评估模块 (EVM)，可与 TPS7A92 配套使用，帮助评估初始电路性能。表 4 显示了此装置的摘要信息。

表 **4.** 设计套件与评估模块(1)

名称	部件号
TPS7A92 低压降稳压器评估模块	TPS7A92EVM-776

(1) 欲获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问 www.ti.com.cn 查看器件产品文件夹。

可在德州仪器 (TI) 网站 (www.ti.com.cn) 上的 TPS7A92 产品文件夹下申请获取该 EVM。

11.1.1.2 Spice 模型

分析模拟电路和系统的性能时，使用 spice 模型对电路性能进行计算机仿真非常有用。可从 TPS7A92 产品文件夹中的仿真模型下申请获取 TPS7A92 的 Spice 模型。

11.1.2 器件命名规则

表 **5.** 订购信息(1)

产品	说明
TPS7A92xx**YYYZ**	**YYY** 为封装标识符。 **XX** 表示输出电压。01 为可调输出版本。 **Z** 为封装数量。

(1) 欲获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问 www.ti.com.cn 查看器件产品文件夹。

11.2 文档支持

11.2.1 相关文档

德州仪器 (TI)，*《TPS37xx 双通道、低功耗、高精度电压检测器》*数据表

德州仪器 (TI)，*《TPS7A88 评估模块》*用户指南

德州仪器 (TI)，*《使用前馈电容器和低压降稳压器的优缺点》*应用报告

德州仪器 (TI)，*《如何测量 LDO 噪声》*白皮书

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A9201DSKR	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CFP
TPS7A9201DSKR.A	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CFP
TPS7A9201DSKRG4	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CFP
TPS7A9201DSKRG4.A	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CFP
TPS7A9201DSKT	Active	Production	SON (DSK) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CFP
TPS7A9201DSKT.A	Active	Production	SON (DSK) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CFP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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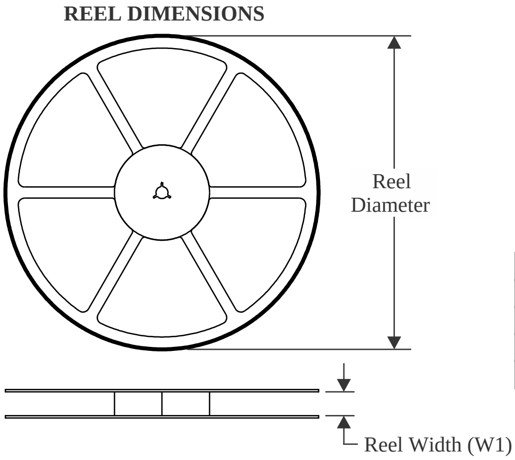
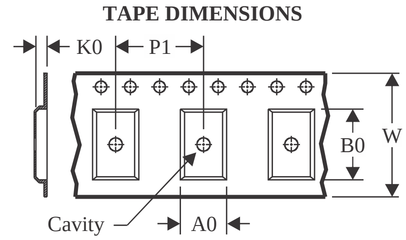
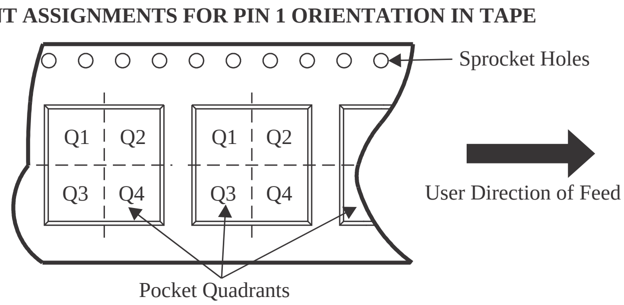
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





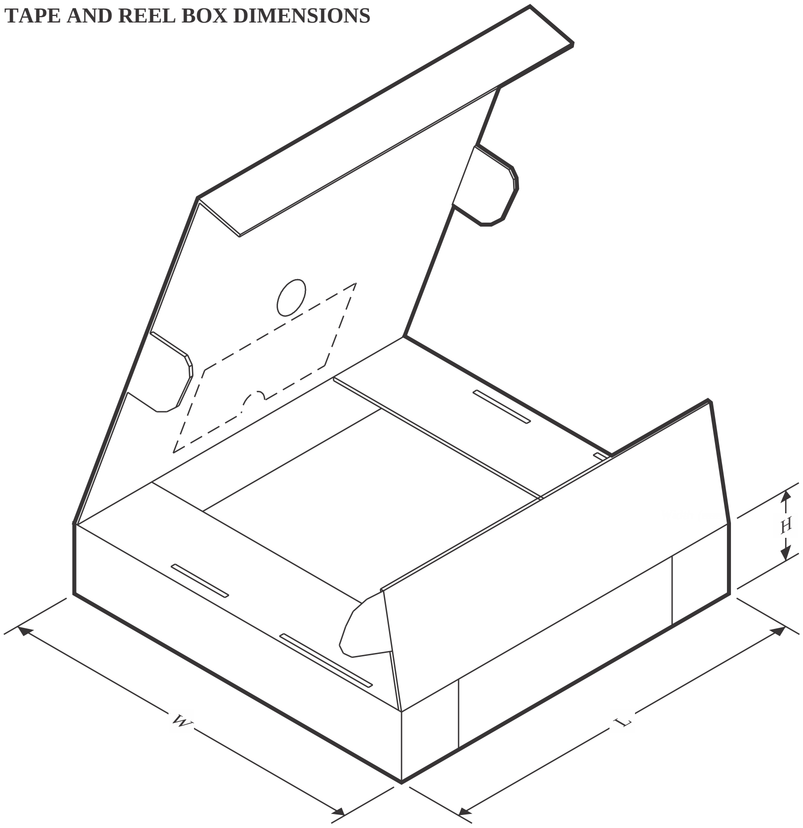
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A9201DSKR	SON	DSK	10	3000	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2
TPS7A9201DSKRG4	SON	DSK	10	3000	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2
TPS7A9201DSKT	SON	DSK	10	250	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



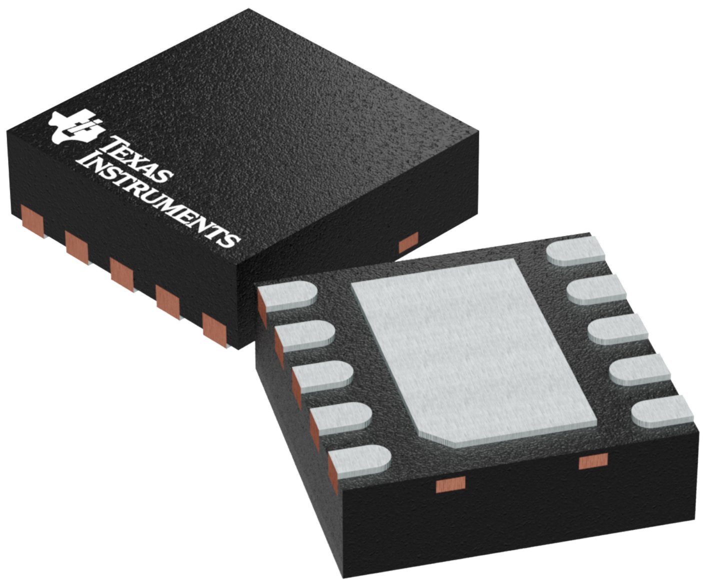
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A9201DSKR	SON	DSK	10	3000	205.0	200.0	33.0
TPS7A9201DSKRG4	SON	DSK	10	3000	205.0	200.0	33.0
TPS7A9201DSKT	SON	DSK	10	250	205.0	200.0	33.0

DSK 10 WSON - 0.8 mm max height

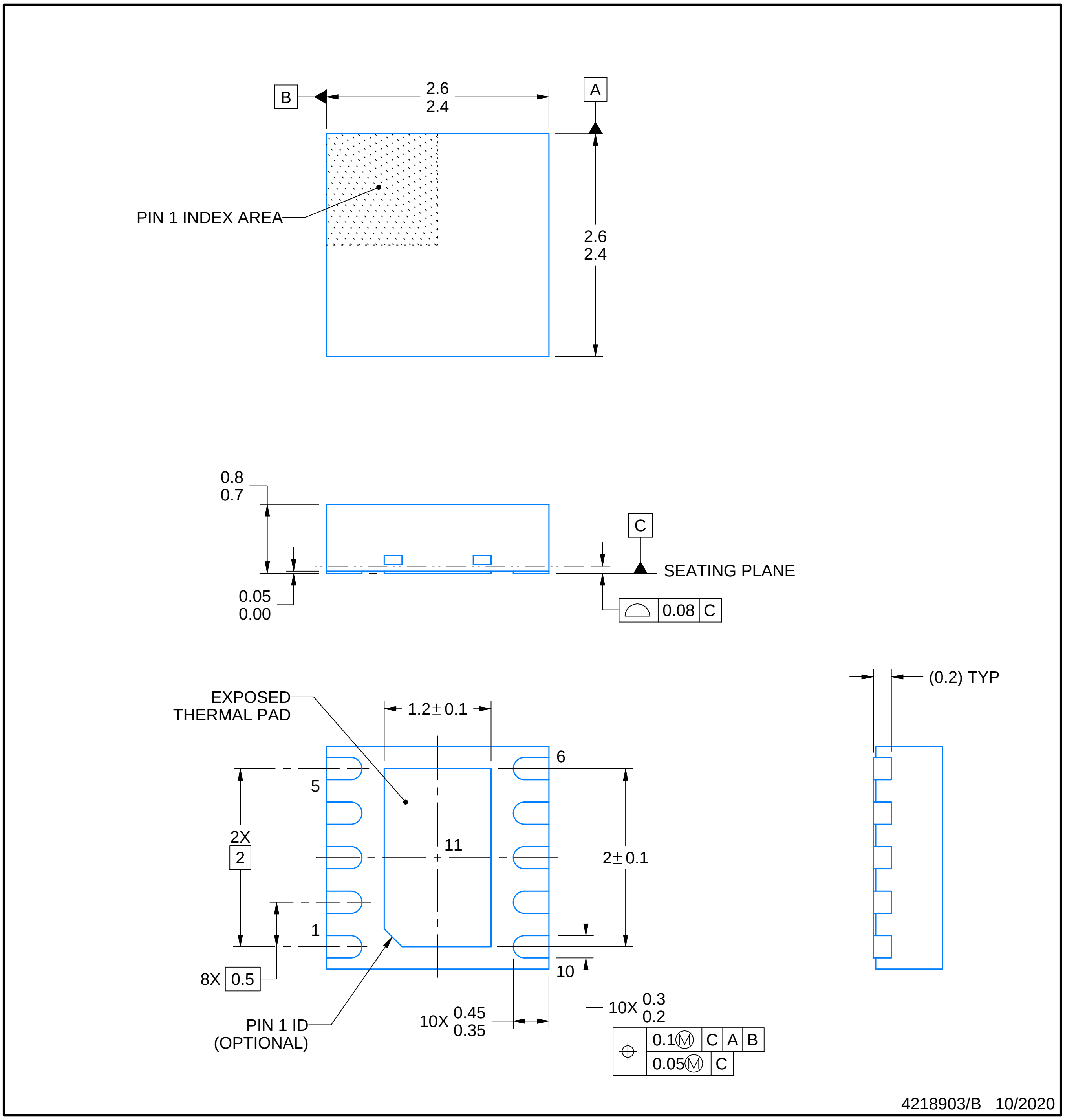
2.5 x 2.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



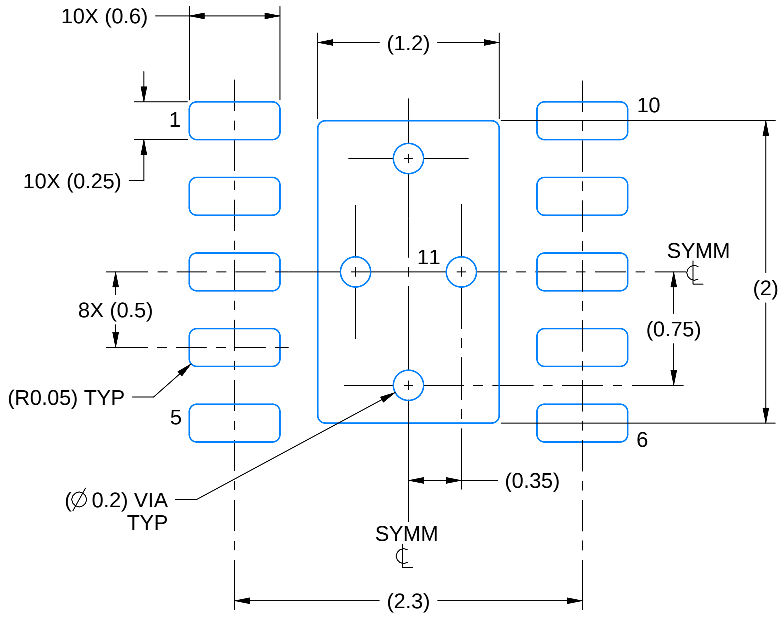
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4225304/A

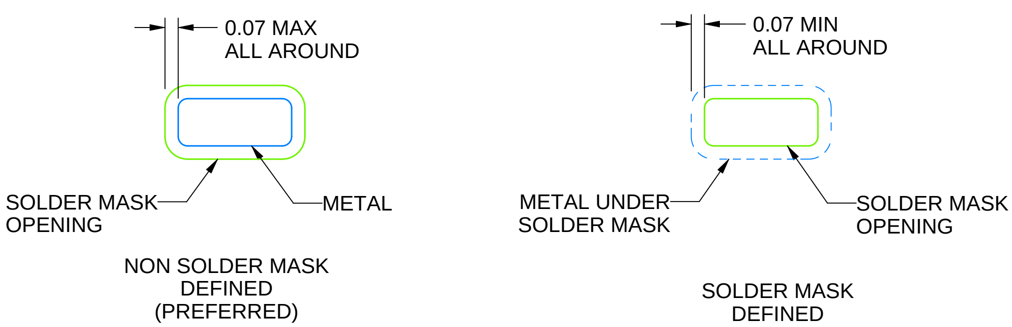


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

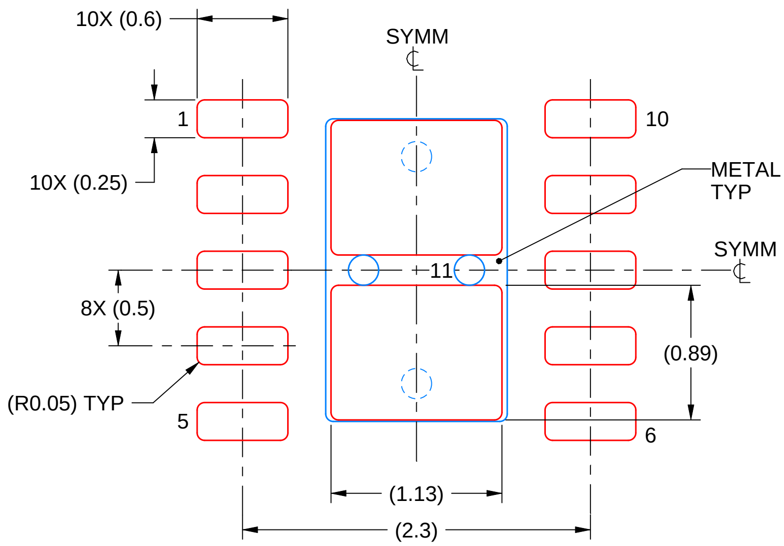


SOLDER MASK DETAILS

4218903/B 10/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218903/B 10/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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