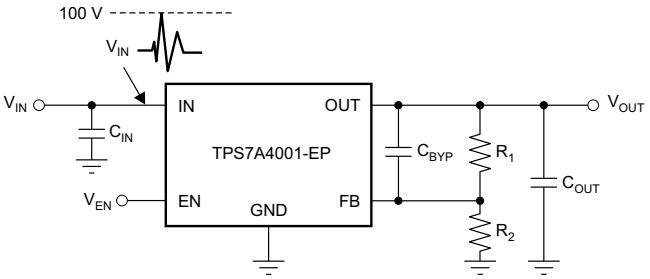
TPS7A4001-EP 100V 输入电压、50mA 超高电压线性稳压器

1 特性

- 超高最大输入电压：100V
- 宽输入电压范围：7V 至 100V
- 准确度：
  - 标称：1%
  - 整个线路、负载和温度范围内：2.7%
- 低静态电流：25µA
- 关断时的静态电流：4.1µA
- 最大输出电流：50mA
- CMOS 逻辑电平兼容的使能引脚
- 可调节输出电压范围约为 1.175V 至 90V
- 与陶瓷电容搭配使用时可保持稳定：
  - 输入电容：≥ 1µF
  - 输出电容：≥ 4.7µF
- 压降电压：290mV
- 内置限流和热关断保护
- 封装：高散热性能 HVSSOP 封装 PowerPAD™
- 支持国防、航天和医疗应用
  - 受控基线
  - 同一组装和测试场所
  - 同一制造场所
  - 支持军用（-55°C 至 125°C）温度范围
  - 延长的产品生命周期
  - 延长的产品变更通知
  - 产品可追溯性

典型应用电路原理图



2 应用

- 由工业用总线（具有高电压瞬态）供电的微处理器、微控制器
- 工业自动化
- 电信基础设施
- 车用
- 以太网供电 (PoE)
- 发光二级管 (LED) 照明
- 偏置电源

3 说明

TPS7A4001-EP 器件是一款能够耐受超高电压的线性稳压器，不仅融合了耐热增强型封装 (HVSSOP) 的优势，还能够承受持续直流电压或最高达 100V 的瞬态输入电压。

TPS7A4001-EP 器件与任何高于 4.7µF 的输出电容以及高于 1µF 的输入电容搭配使用时均可保持稳定（过热和浪涌保护）。 鉴于这款器件的封装 (HVSSOP) 小巧且可能使用的输出电容也较小，因此实现起来只需占用非常小的电路板空间。 此外，TPS7A4001-EP 器件还提供了一个与标准 CMOS 逻辑兼容的使能引脚 (EN)，用以使能低电流关断模式。

TPS7A4001-EP 器件内部具有热关断和电流限制功能，可在故障情况下保护系统。 TPS7A4001-EP 器件的工作温度范围为 T_J = –55°C 至 125°C。

此外，TPS7A4001-EP 器件非常适合在电信和工业应用中利用中间电压轨生成低压电源；该器件不但能够提供一个经充分稳压的电压轨，而且能够承受超高的快速电压瞬变并在其间保持稳压状态。 这些特性相当于一套更为简单且经济高效的电气浪涌保护电路，因此被包括 PoE、偏置电源和 LED 照明在内的多类应用广泛使用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7A4001-EP	HVSSOP (8)	3.00mm x 5.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

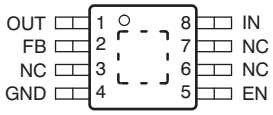
目录

4 修订历史记录

日期	修订版本	注释
2015 年 8 月	*	首次发布。

5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Regulator output. A capacitor >4.7 µF must be tied from this pin to ground to assure stability.
FB	2	O	This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device.
NC	3	—	Not internally connected. This pin must either be left open or tied to GND.
	6		
	7		
GND	4	—	Ground
EN	5	I	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_HI}$ the regulator is enabled. If $V_{EN} \leq V_{EN\_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
IN	8	I	Input supply
PowerPAD	—	—	Solder to printed-circuit-board (PCB) to enhance thermal performance. **NOTE: The PowerPAD is internally connected to GND.** Although it can be left floating, TI highly recommends connecting the PowerPAD to the GND plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–0.3	102	V
	OUT pin to GND pin	–0.3	102	
	OUT pin to IN pin	–102	0.3	
	FB pin to GND pin	–0.3	2	
	FB pin to IN pin	–102	0.3	
	EN pin to IN pin	–102	0.3	
	EN pin to GND pin	–0.3	102	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VIN	7		100	V
VOUT	1.161		90	V
VEN	0		100	V
IOUT	0		50	mA

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A4001-EP DGN (HVVSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_J = –55°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 2 V or V_{IN} = 7 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		7		100	V
V_{REF}	Internal reference	T_J = 25°C, V_{FB} = V_{REF}, V_{IN} = 9 V, I_{OUT} = 25 mA	1.161	1.173	1.185	V
V_{OUT}	Output voltage range(1)	V_{IN} ≥ $V_{OUT(NOM)}$ + 2 V	V_{REF}		90	V
	Nominal accuracy	T_J = 25°C, V_{IN} = 9 V, I_{OUT} = 25 mA	–1		1	$\%V_{OUT}$
	Overall accuracy	$V_{OUT(NOM)}$ + 2 V ≤ V_{IN} ≤ 24 V(2) 100 µA ≤ I_{OUT} ≤ 50 mA	–2.7		2.7	$\%V_{OUT}$
$\frac{\Delta\%V_{OUT}}{\Delta V_{IN}}$	Line regulation	7 V ≤ V_{IN} ≤ 100 V		0.03		$\%V_{OUT}$
$\frac{\Delta\%V_{OUT}}{\Delta I_{OUT}}$	Load regulation	100 µA ≤ I_{OUT} ≤ 50 mA		0.31		$\%V_{OUT}$
V_{DO}	Dropout voltage	V_{IN} = 17 V, $V_{OUT(NOM)}$ = 18 V, I_{OUT} = 20 mA		290		mV
		V_{IN} = 17 V, $V_{OUT(NOM)}$ = 18 V, I_{OUT} = 50mA		0.78	1.3	V
I_{LIM}	Current limit	V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 7 V, T_J ≤ 85°C	51	146	207	mA
		V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 9 V	51	165	220	mA
I_{GND}	Ground current	7 V ≤ V_{IN} ≤ 100 V, I_{OUT} = 0 mA		25	65	µA
		I_{OUT} = 50 mA		25		µA
I_{SHDN}	Shutdown supply current	V_{EN} = 0.4 V		4.1	20	µA
I_{FB}	Feedback current(3)		–0.1	0.01	0.1	µA
I_{EN}	Enable current	7 V ≤ V_{IN} ≤ 100 V, V_{IN} = V_{EN}		0.02	1	µA
V_{EN_HI}	Enable high-level voltage		1.5		V_{IN}	V
V_{EN_LO}	Enable low- level voltage		0		0.4	V
V_{NOISE}	Output noise voltage	V_{IN} = 12 V, $V_{OUT(NOM)}$ = V_{REF}, C_{OUT} = 10 µF, BW = 10 Hz to 100 kHz		58		μV_{RMS}
		V_{IN} = 12 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 10 µF, C_{BYP}(4) = 10 nF, BW = 10 Hz to 100 kHz		73		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = 12 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 10 µF, C_{BYP}(4) = 10 nF, f = 100 Hz		65		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
		Reset, temperature decreasing		150		°C
T_J	Operating junction temperature		–55		125	°C

(1) To ensure stability at no-load conditions, a current from the feedback resistive network greater than or equal to 10 µA is required.
(2) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ($P \approx (V_{IN} - V_{OUT}) \times I_{OUT}$ = (24 V – V_{REF}) × 50 mA ≈ 1.14 W). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.
(3) I_{FB} > 0 flows out of the device.
(4) C_{BYP} refers to a bypass capacitor connected to the FB and OUT pins.

6.6 Typical Characteristics

At T_J = –55°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 2 V or V_{IN} = 9 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

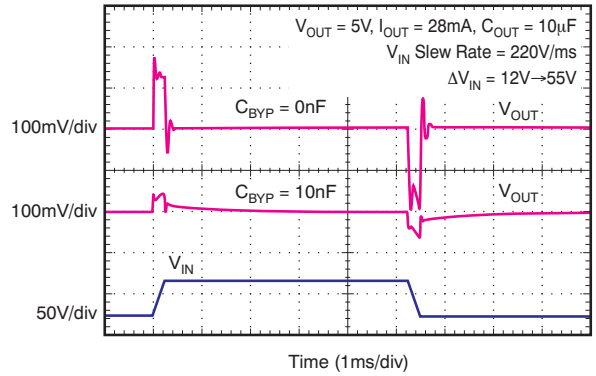


Figure 1. Line Transient Response vs C_{BYP}

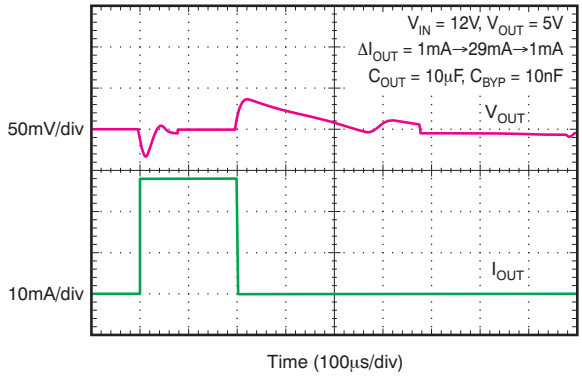


Figure 2. Load Transient Response

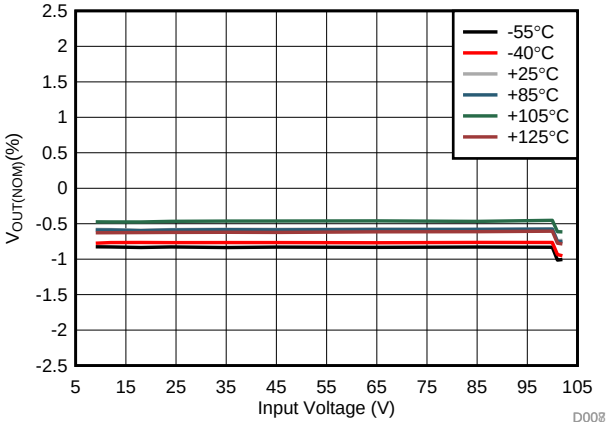


Figure 3. Line Regulation

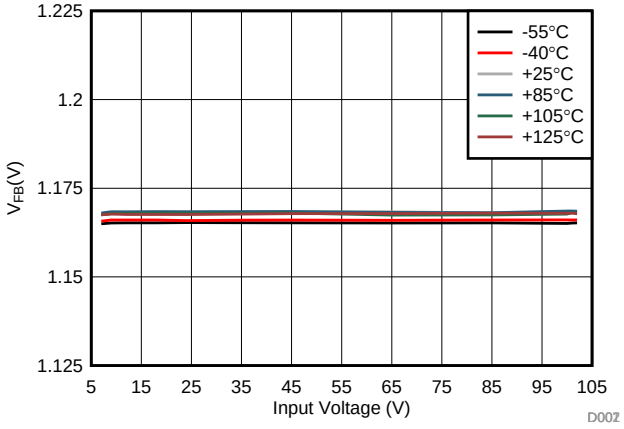


Figure 4. Feedback Voltage

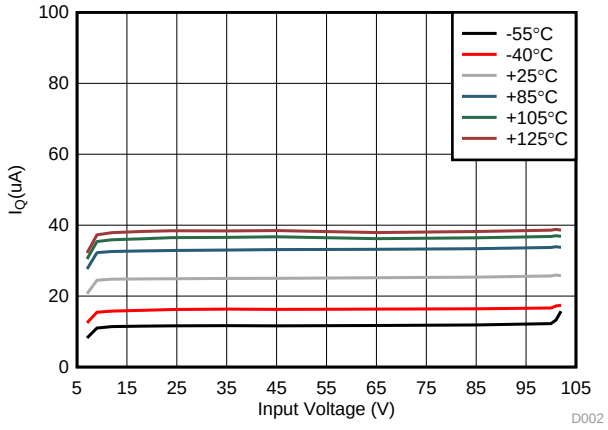


Figure 5. Ground Current vs Input Voltage

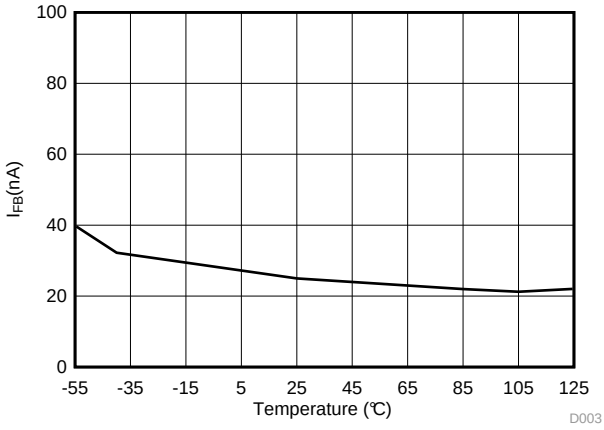


Figure 6. Feedback Current

Typical Characteristics (continued)

At T_J = –55°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 2 V or V_{IN} = 9 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

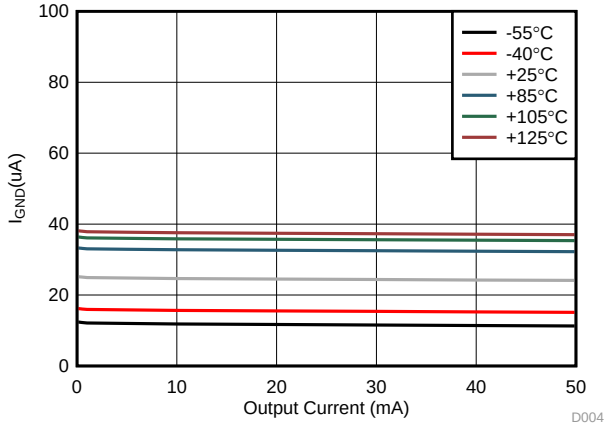


Figure 7. Ground Current vs Output Current

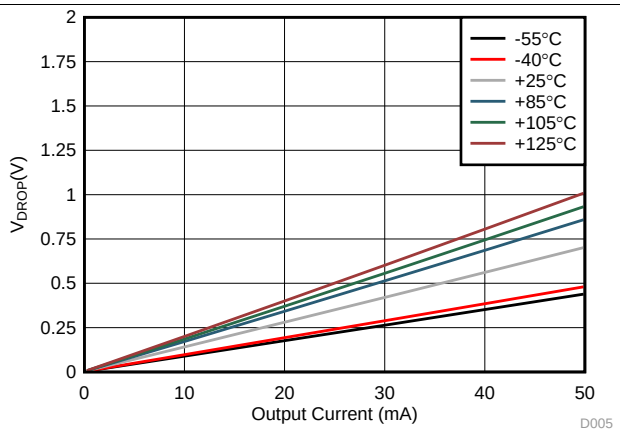


Figure 8. Dropout Voltage

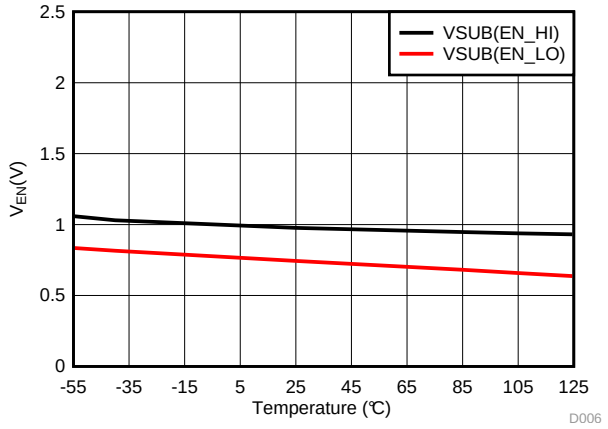


Figure 9. Enable Threshold Voltage

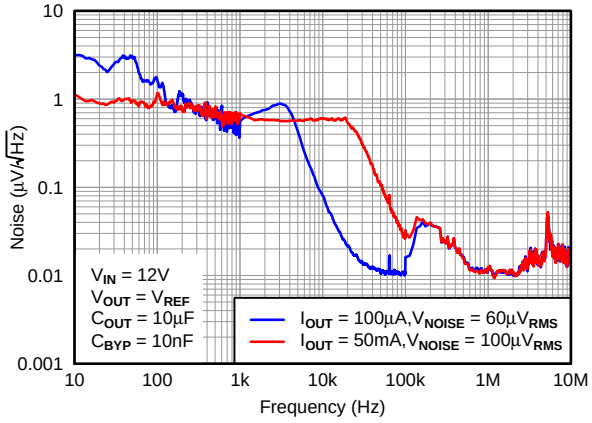


Figure 10. Output Spectral Noise Density

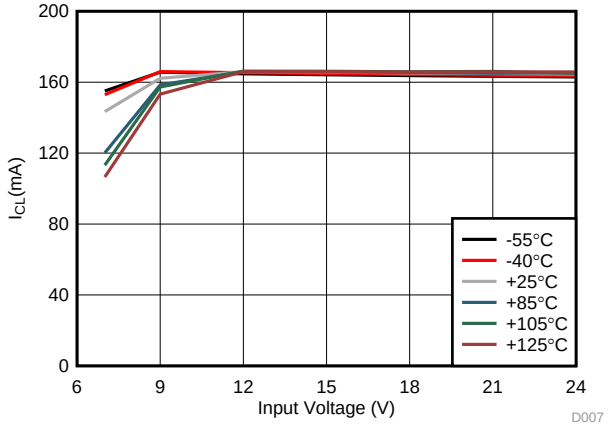


Figure 11. Current Limit

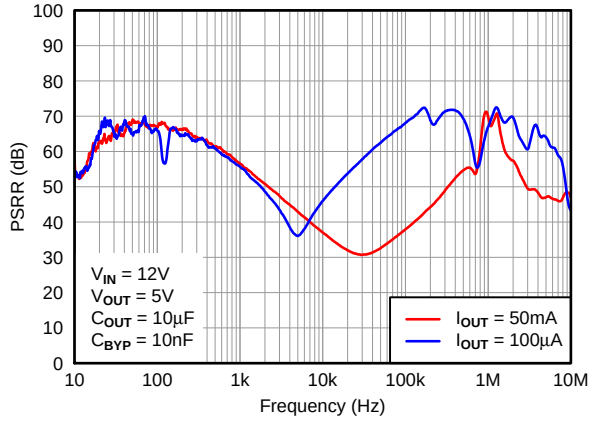


Figure 12. Power-Supply Rejection Ratio

7 Detailed Description

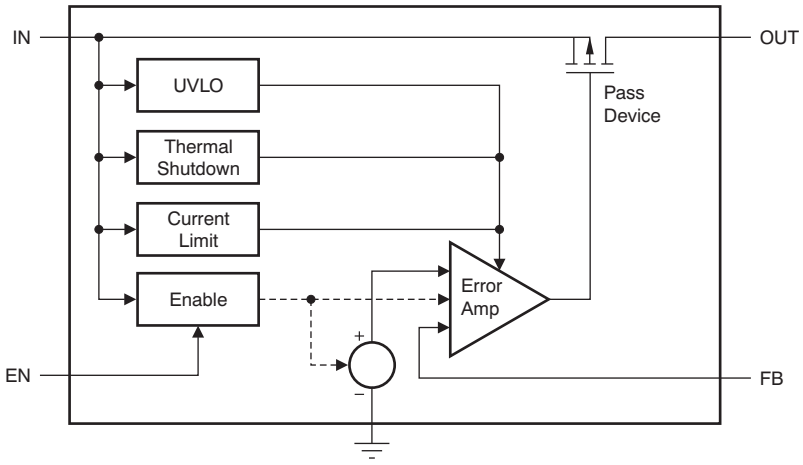
7.1 Overview

The TPS7A4001-EP device belongs to a new generation of linear regulators that use an innovative BiCMOS process technology to achieve very high maximum input and output voltages.

This process not only allows the TPS7A4001-EP device to maintain regulation during very fast high-voltage transients up to 105 V, but it also allows the TPS7A4001-EP device to regulate from a continuous high-voltage input rail. Unlike other regulators created using bipolar technology, the ground current of the TPS7A4001-EP device is also constant over its output current range, resulting in increased efficiency and lower power consumption.

These features, combined with a high thermal performance HVSSOP PowerPAD package, make this device ideal for industrial and telecom applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The fixed internal current limit of the TPS7A4001-EP device helps protect the regulator during fault conditions. The maximum amount of current the device can source is the current limit (309 mA, typical), and is largely independent of output voltage. For reliable operation, the device does not operate in current limit for extended periods of time.

7.3.2 Enable Pin Operation

The TPS7A4001-EP device provides an enable pin (EN) feature that turns on the regulator when $V_{EN} > V_{EN\_HI}$, and disables the regulator when $V_{EN} < V_{EN\_LO}$.

7.3.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

Feature Description (continued)

The internal protection circuitry of the TPS7A4001-EP device has been designed to protect against overload conditions. The protection circuitry was not intended to replace proper heatsinking. Continuously running the TPS7A4001-EP device into thermal shutdown degrades device reliability.

7.3.4 Undervoltage Lockout (UVLO)

The TPS7A4001-EP contains an UVLO comparator that ensures the error amplifier is disabled when the input voltage is below the required minimum operational voltage. The minimum recommended operational voltage is 7 V.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN\_HI}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN\_HI}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN\_LO}$	—	$T_J > 170°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

One of the primary applications of the TPS7A4001-EP device is to provide transient voltage protection to sensitive circuitry that may be damaged in the presence of high-voltage spikes.

This transient voltage protection can be more cost-effective and compact compared to topologies that use a transient voltage suppression (TVS) block.

8.1.1 Adjustable Operation

The TPS7A4001-EP device has an output voltage range of about 1.175 to 90 V. The nominal output voltage of the device is set by two external resistors, as shown in Figure 13.

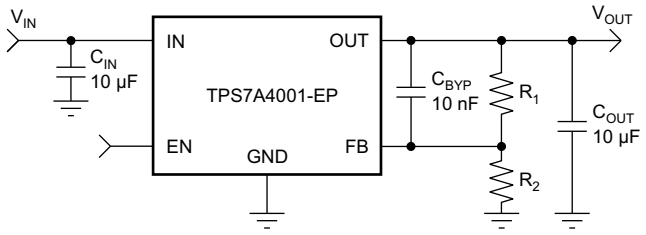


Figure 13. Adjustable Operation for Maximum AC Performance

Calculate R_1 and R_2 for any output voltage range using the formula shown in Equation 1. To ensure stability under no-load conditions, this resistive network must provide a current ≥ 10 µA.

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right), \quad \text{where } \frac{V_{OUT}}{R_1 + R_2} \geq 10\mu A \tag{1}$$

If greater voltage accuracy is required, consider the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

8.2 Typical Application

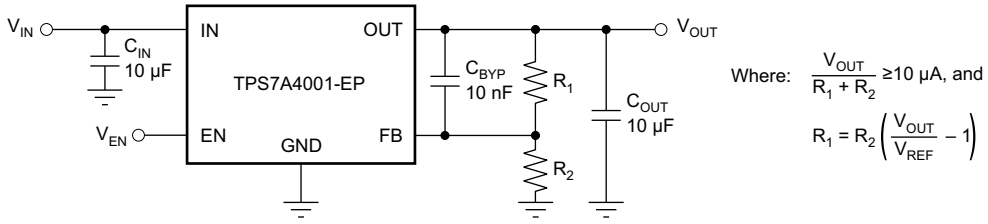


Figure 14. Example Circuit to Maximize Transient Performance

8.2.1 Design Requirements

For this design example, use the following parameters listed in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
V_{IN}	12 V, with 55 V surge tolerance
V_{OUT}	5 V (ideal), 4.981 (actual)
I_{OUT}	28 mA
Accuracy	5 %
R1, R2	162 kΩ, 49.9 kΩ

8.2.2 Detailed Design Procedure

The maximum value of total feedback resistance can be calculated to be 500 kΩ. Equation 1 was used to calculate R1 and R2, and standard 1% resistors were selected to keep the accuracy within the 5% allocation. 10-uF ceramic input and output capacitors were selected, along with a 10-nF bypass capacitor for optimal AC performance.

8.2.2.1 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors should be used for the input, output, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are required. Ceramic X7R capacitors offer improved voltage and temperature coefficients, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

NOTE

High ESR capacitors may degrade PSRR.

8.2.2.2 Input and Output Capacitor Requirements

The TPS7A4001-EP device high voltage linear regulator achieves stability with a minimum output capacitance of 4.7 µF and input capacitance of 1 µF; however, TI highly recommends to use 10-µF output and input capacitors to maximize AC performance.

8.2.2.3 Bypass Capacitor Requirements

Although a bypass capacitor (C_{BYP}) is not needed to achieve stability, TI highly recommends using a 10-nF bypass capacitor to maximize AC performance (including line transient, noise, and PSRR). For additional information regarding the performance improvements of using a bypass capacitor, see .

8.2.2.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the duration of the transient response.

The presence of the C_{BYP} capacitor may greatly improve the line transient response of the TPS7A4001-EP device, as shown in Figure 1.

8.2.3 Application Curves

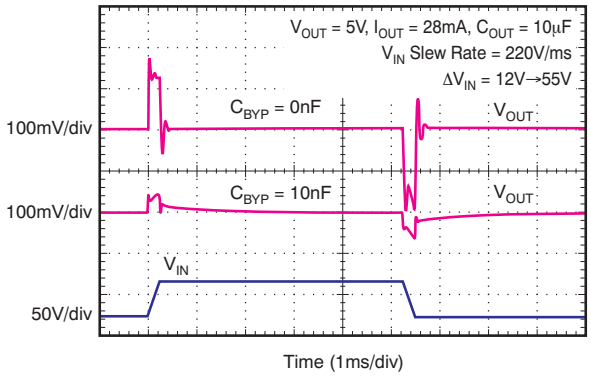


Figure 15. Line Transient Response vs C_{BYP}

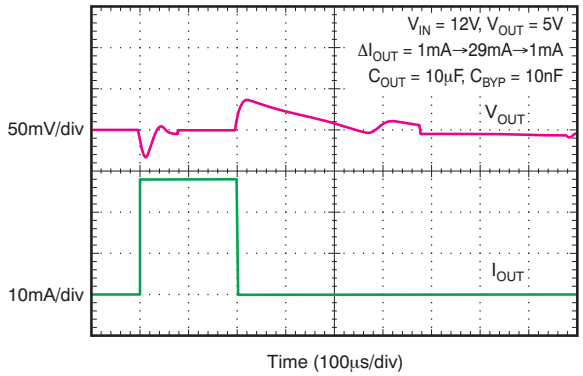


Figure 16. Load Transient Response

9 Power Supply Recommendations

The input supply for the LDO should not exceed its recommended operating conditions (7 V to 100 V). The input voltage should provide adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance. The input and output supplies should also be bypassed with 10-µF capacitors located near the input and output pins. There should be no other components located between these capacitors and the pins.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, C_{BYP}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for the TPS7A40 evaluation board, available at www.ti.com.

10.2 Layout Example

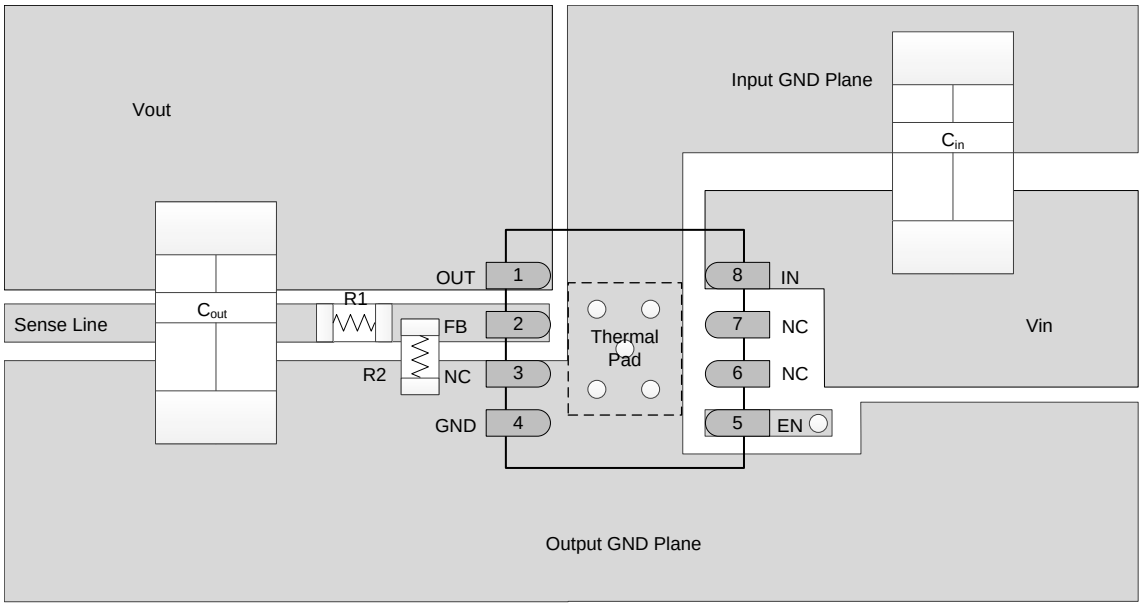


Figure 17. Recommended Layout Example

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle ON and OFF. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Thermal Considerations (接下页)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A4001-EP has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A4001-EP device into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (2)$$

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A4001MDGNREP	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	ZFY4
TPS7A4001MDGNREP.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	ZFY4
V62/15603-01XE	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	ZFY4

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS7A4001-EP :

- Catalog : TPS7A4001

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

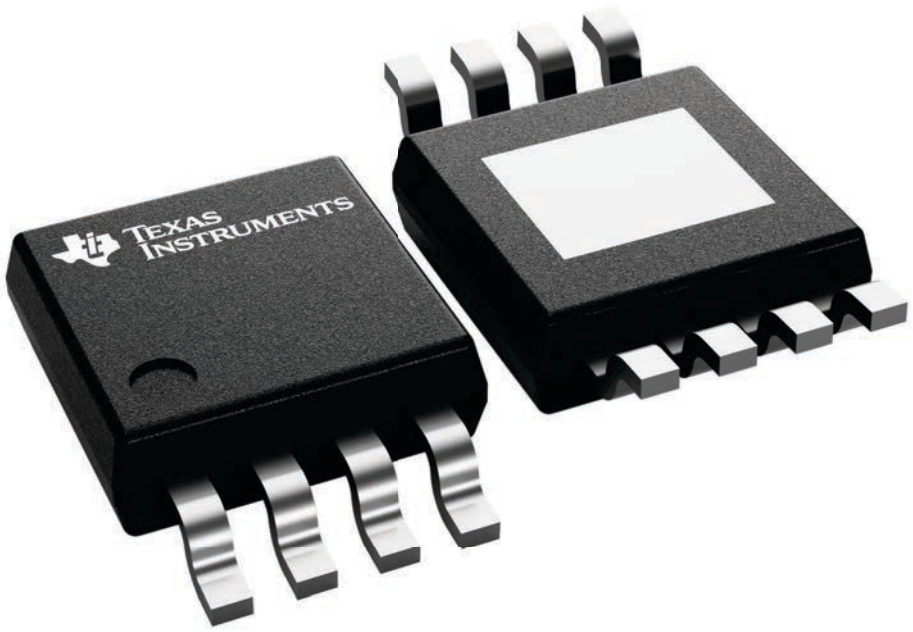
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

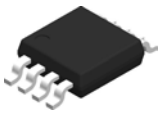
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

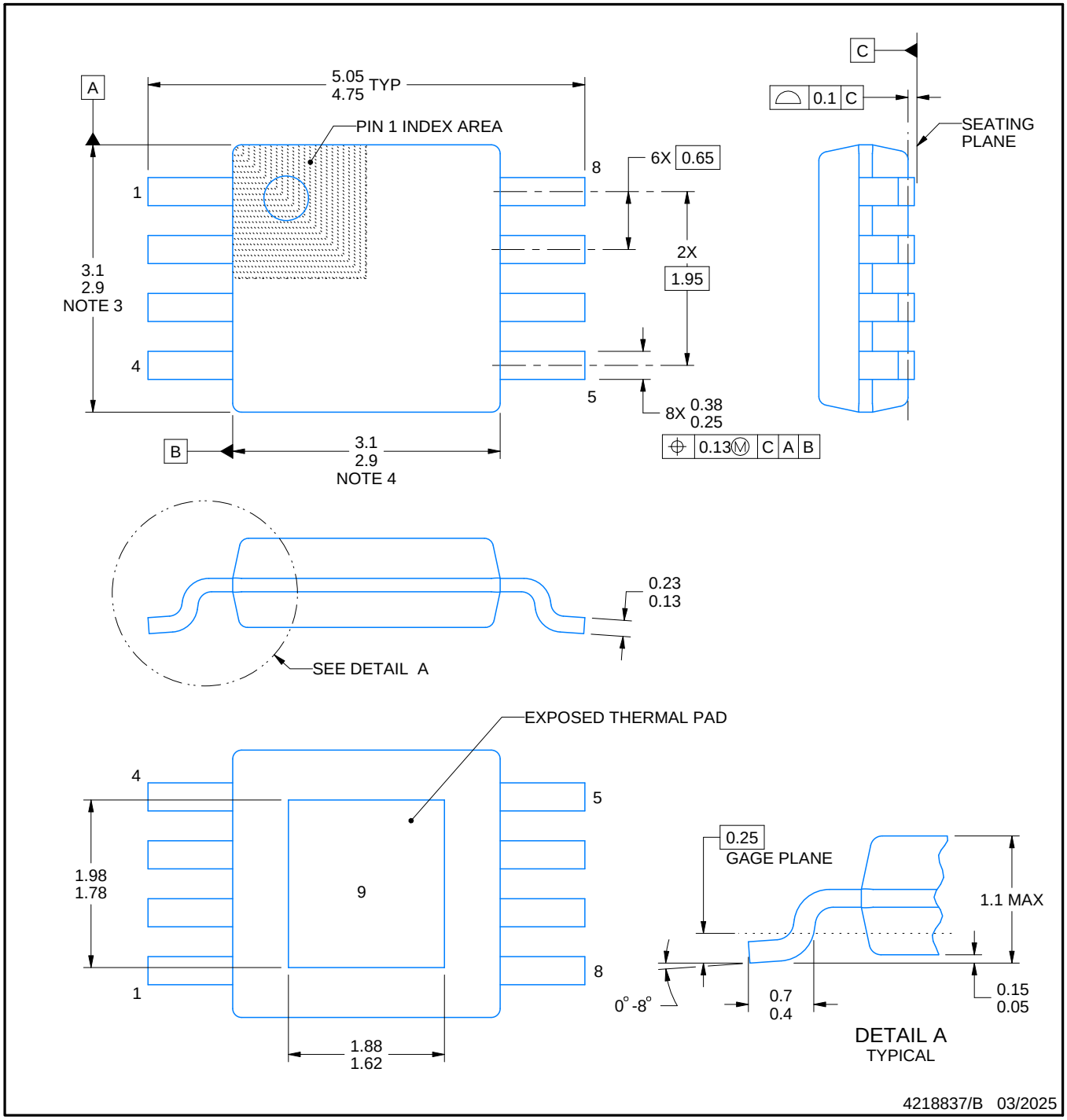
PACKAGE OUTLINE

DGN0008B



HVSSOP - 1.1 mm max height

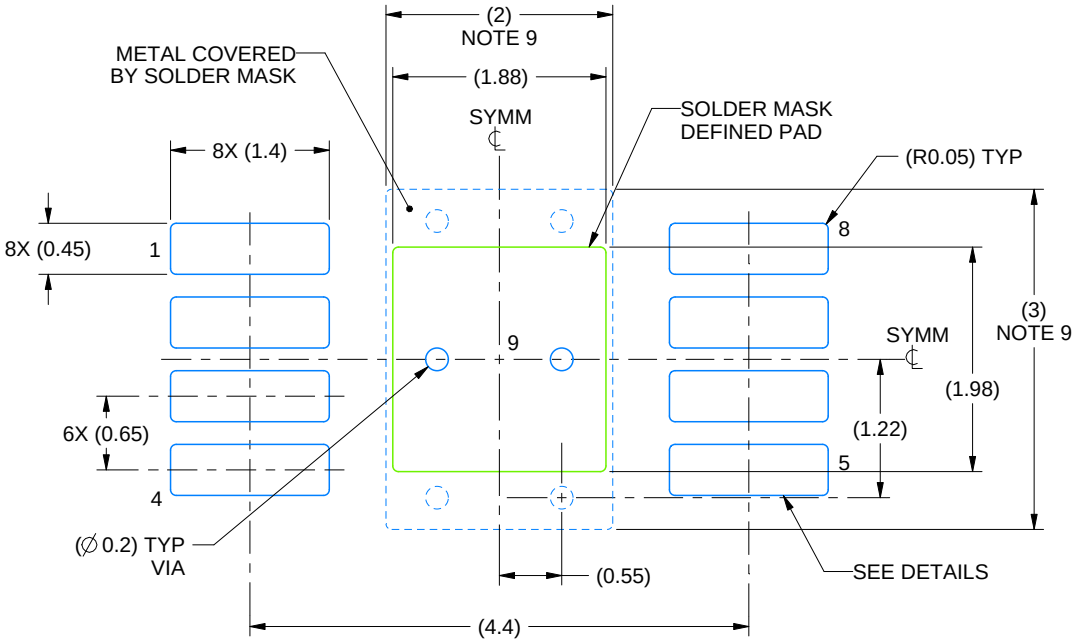
SMALL OUTLINE PACKAGE



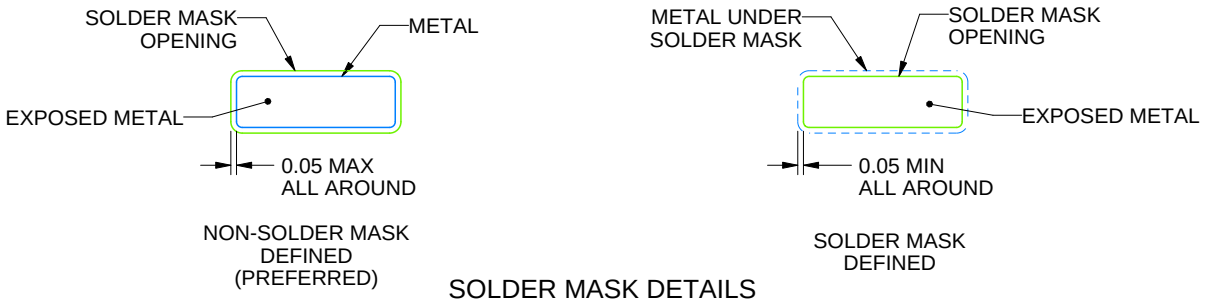
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

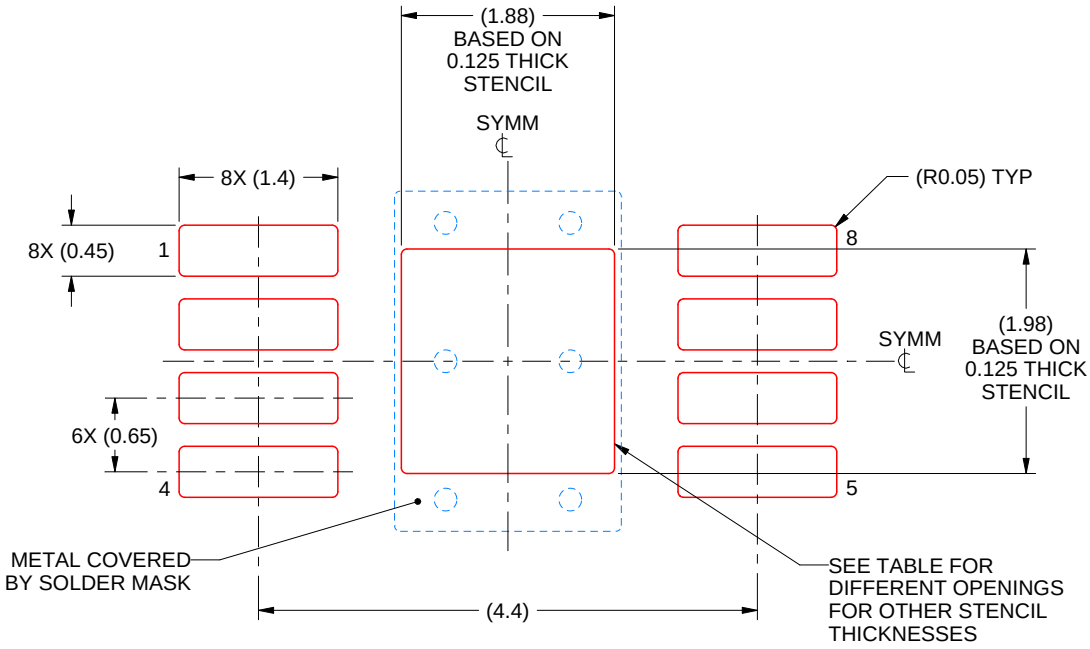


SOLDER MASK DETAILS

4218837/B 03/2025

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.21
0.125	1.88 X 1.98 (SHOWN)
0.15	1.72 X 1.81
0.175	1.59 X 1.67

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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