TPS799Lxx 内置浪涌电流保护功能的 200mA 低压降线性稳压器

1 特性

- 带有使能 (EN) 引脚的 200mA 低压降稳压器
- 提供了多个输出电压版本：
  - TPS799L：使用创新的工厂 EEPROM 编程的 5.2V 至 6.2V 固定输出电压
  - TPS799L57：5.7V 输出电压
  - TPS799L54：5.4V 输出电压
  - TPS799：输出选项少于 5.2V
- 带有 EN 切换的涌入电流保护
- 低 I_Q： 40μA
- 高电源抑制比 (PSRR)：频率 1kHz 时为 66dB
- 与一个低等效串联电阻 (ESR)，2.0μF（典型值）输出电容一起工作时保持稳定
- 出色的负载和线路瞬态响应
- 整体精度（负载、线路和温度）为 2%
- 极低压降：100 mV
- 封装：5 凸点，超薄，1mm × 1.37mm 芯片尺寸球状引脚栅格阵列 (DSBGA)

2 应用

- 手机
- 无线 LAN， 蓝牙®
- 压控振荡器 (VCO)，射频 (RF)
- 手持式管理器，掌上电脑 (PDA)

3 说明

TPS799L 低压降 (LDO)，低功耗线性稳压器系列产品能够提供出色的交流性能，同时还能保证极低的接地电流。 仅消耗 40μA（典型值）接地电流，同时具备高电源抑制比 (PSRR)，低噪声，快速启动以及出色的线路和负载瞬态响应特性。

TPS799Lxx 与陶瓷电容器搭配使用时可保持稳定，并且该器件使用先进的 BiCMOS 制造工艺，能够在输出 200mA 电流时产生 100mV 的典型压降值。 TPS799L 使用一个精度电压基准和反馈环路来实现全部负载、线路、过程、和温度变化范围上 2% 的总精度。 当 EN 切换被用于启动此器件时，TPS799L 特有涌入电流保护功能可立即钳制电流。

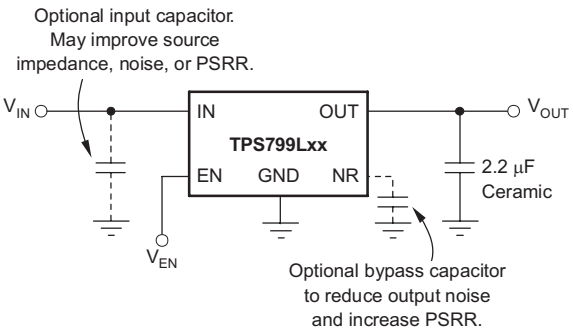
所有器件均在温度范围 T_J = -40 C 至 125°C 内全额运行，采用超薄芯片尺寸球状引脚栅格阵列 (DSBGA) 封装，适用于无线手持终端和 WLAN 卡。

器件信息(1)

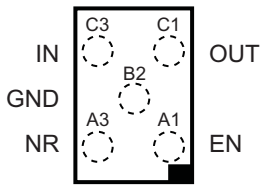
部件号	封装	封装尺寸（标称值）
TPS799Lxx	DSBGA (5)	1.57mm x 1.20mm

(1) 要了解所有可用封装，请见数据表末尾的封装选项附录。

典型应用电路



TPS799LxxYZY
WCSP
(TOP VIEW)



目录

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2012) to Revision B **Page**

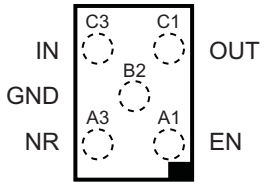
- 更改了文档格式，添加了新的部分并移动了现有部分 ... 1
- 已将 TPS799L54 器件添加到数据表 ... 1
- 已将整个数据表中的 WCSP 封装名称更改为 DSBGA ... 1
- Changed *free-air* to *junction* in Absolute Maximum Ratings table conditions ... 4
- Changed *free-air* to *junction* in Recommended Operating Conditions table conditions ... 4
- Deleted Start-up time symbol ... 5

Changes from Original (April 2012) to Revision A **Page**

- Deleted Figure 19 ... 13

5 Pin Configuration and Functions

YZY Package
DSBGA-5
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	A1	I	Driving this pin high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
GND	B2	—	Ground
IN	C3	I	Input supply
NR	A3	—	Noise reduction; connecting this pin to an external capacitor bypasses noise generated by the internal band gap. This capacitor allows output noise to be reduced to very low levels.
OUT	C1	O	Output of the regulator. To assure stability, a small ceramic capacitor (total typical capacitance ≥ 2.0 µF) is required from this pin to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	7.0	V
	EN	–0.3	V_{IN} + 0.3	V
	OUT	–0.3	V_{IN} + 0.3	V
Current	OUT	Internally limited		mA
Temperature	Operating virtual junction, T_J	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		6.5	V
I_{OUT}	Output current	0.5		200	mA
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS799Lxx YZY (DSBGA) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	143.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	84.7	
ψ_{JT}	Junction-to-top characterization parameter	3.8	
ψ_{JB}	Junction-to-board characterization parameter	84.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

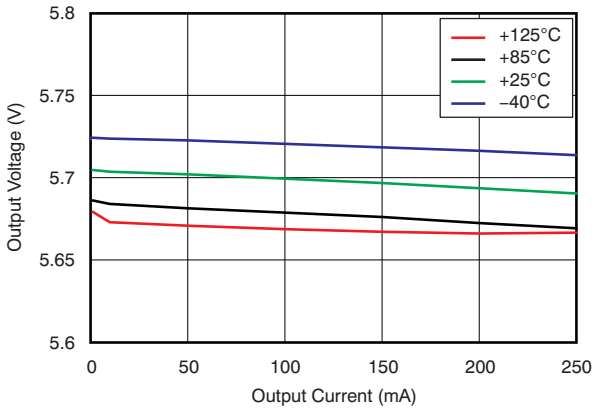
Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			2.7		6.5	V
V_{OUT}	Output voltage range			5.2		6.2	V
	Output accuracy, nominal	T_J = 25°C		–1.0%		1.0%	
	Output accuracy(1) Over V_{IN}, I_{OUT}, temperature	V_{OUT} + 0.3 V ≤ V_{IN} ≤ 6.5 V 500 µA ≤ I_{OUT} ≤ 200 mA		–2.0%	±1.0%	2.0%	
$\Delta V_{O(\Delta VI)}$	Line regulation(1)	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 6.5 V			0.02		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	500 µA ≤ I_{OUT} ≤ 200 mA			0.002		%/mA
V_{DO}	Dropout voltage (V_{IN} = $V_{OUT(NOM)}$ – 0.1 V)	V_{OUT} ≥ 3.3 V, I_{OUT} = 200 mA			90	160	mV
I_{LIM}	Output current limit(2)	V_{OUT} = 0.9 × $V_{OUT(NOM)}$		220	340	600	mA
I_{GND}	Ground pin current	500 µA ≤ I_{OUT} ≤ 200 mA			40	60	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.4 V, 2.7 V ≤ V_{IN} ≤ 6.5 V			0.15	1.0	µA
PSRR	Power-supply rejection ratio	V_{IN} = 6.5 V, V_{OUT} = 2.85 V, C_{NR} = 0.01 µF, I_{OUT} = 100 mA	f = 100 Hz		70		dB
			f = 1 kHz		66		dB
			f = 10 kHz		51		dB
			f = 100 kHz		38		dB
V_N	Output noise voltage	BW = 10 Hz to 100 kHz	C_{NR} = 0.01 µF		10.5 × V_{OUT}		μV_{RMS}
			C_{NR} = none		94 × V_{OUT}		μV_{RMS}
	Start-up time	V_{OUT} = 5.7 V, R_L = 28 Ω, C_{OUT} = 2.2 µF	C_{NR} = 0.01 µF		90		µs
			C_{NR} = none		95		µs
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	V_{EN} = V_{IN} = 6.5 V			0.03	1.0	µA
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing			165		°C
		Reset, temperature decreasing			145		°C
T_J	Operating junction temperature			–40		125	°C
UVLO	Undervoltage lockout	V_{IN} rising		1.90	2.20	2.65	V
	Hysteresis	V_{IN} falling			70		mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7 V, whichever is greater.
(2) The TPS799Lxx has a peak current clamp during EN toggle start-up.

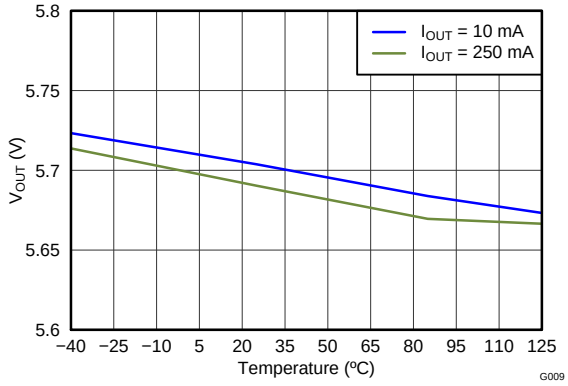
6.6 Typical Characteristics

Over operating temperature range (T_J= –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01µF, unless otherwise noted. Typical values are at T_J = 25°C.



V_{IN} = 6.5 V

Figure 1. Load Regulation



TPS799Axx

Figure 2. Output Voltage vs Junction Temperature

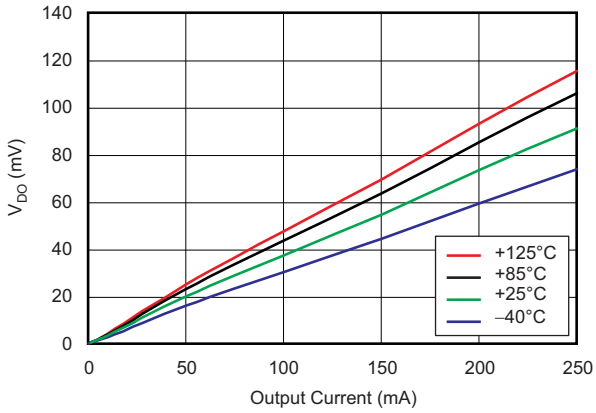
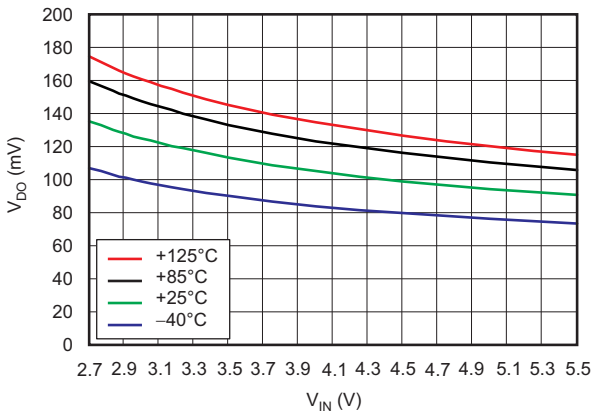


Figure 3. Dropout Voltage vs Output Current



I_{OUT} = 250 mA

Figure 4. Dropout Voltage vs Input Voltage

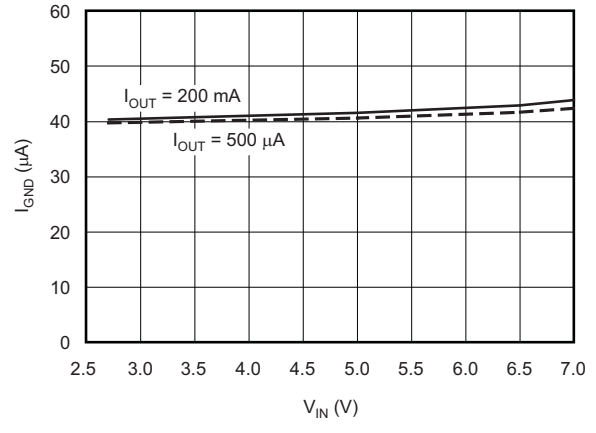
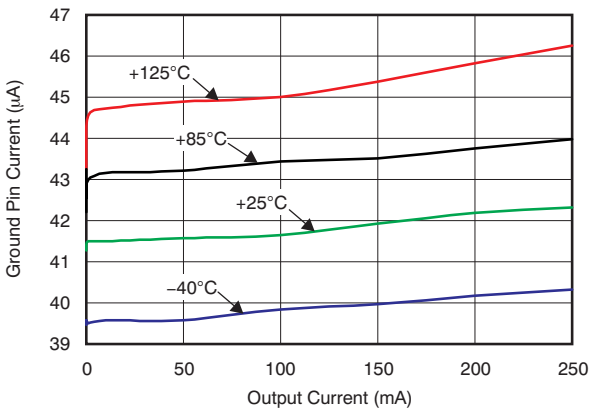


Figure 5. Ground Pin Current vs Input Voltage



V_{IN} = 6.5 V

Figure 6. Ground Pin Current vs Output Current

Typical Characteristics (continued)

Over operating temperature range (T_J= –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01µF, unless otherwise noted. Typical values are at T_J = 25°C.

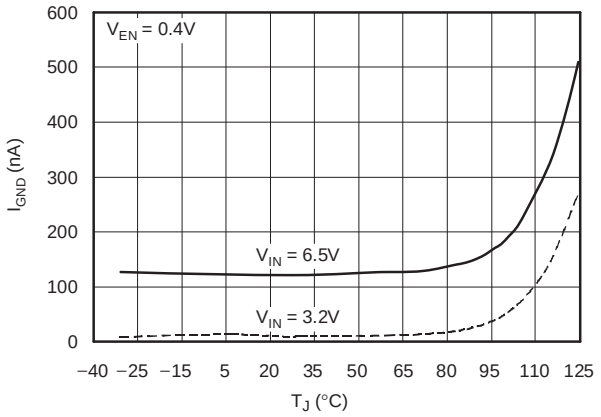
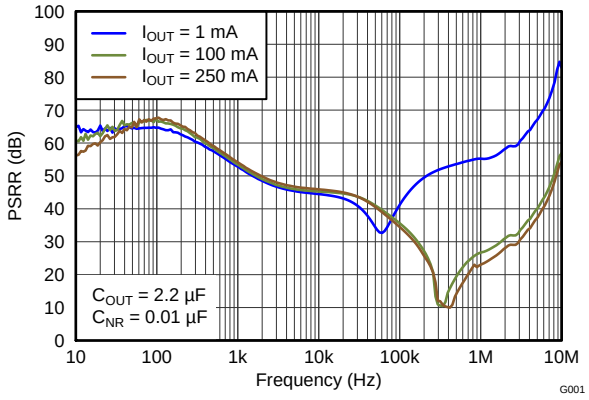
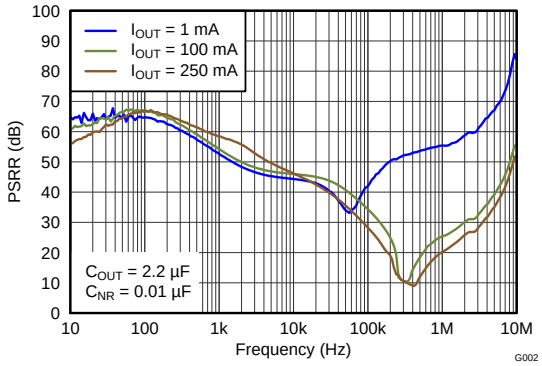


Figure 7. Ground Pin Current (Disabled) vs Junction Temperature



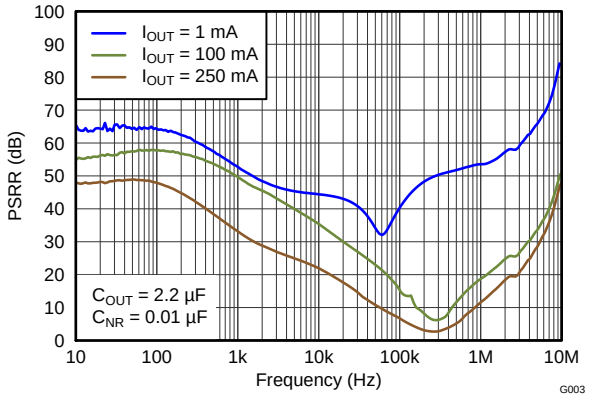
VIN = 6.5 V

Figure 8. Power-Supply Rejection Ratio vs Frequency



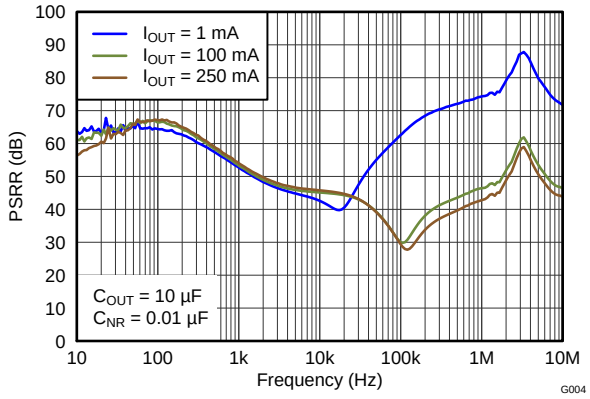
VIN = 6.2 V

Figure 9. Power-Supply Rejection Ratio vs Frequency



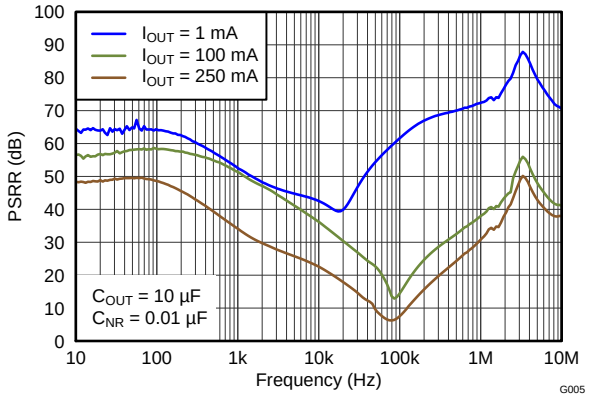
VIN = 5.95 V

Figure 10. Power-Supply Rejection Ratio vs Frequency



VIN = 6.5 V

Figure 11. Power-Supply Rejection Ratio vs Frequency

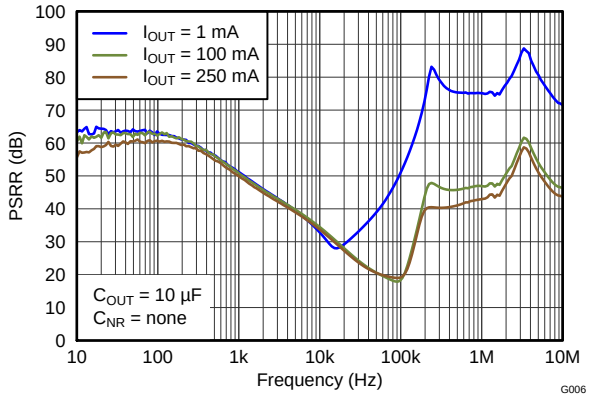


VIN = 6.2 V

Figure 12. Power-Supply Rejection Ratio vs Frequency

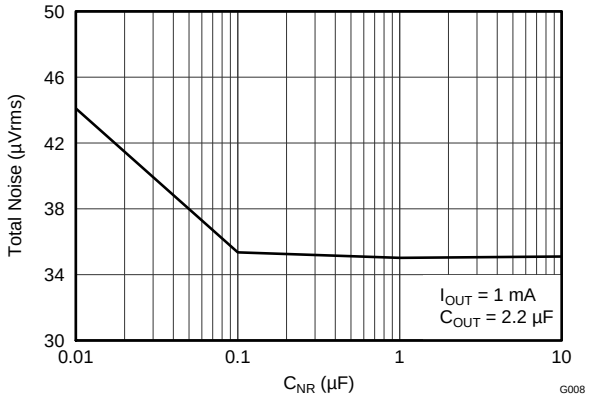
Typical Characteristics (continued)

Over operating temperature range (T_J= –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01µF, unless otherwise noted. Typical values are at T_J = 25°C.



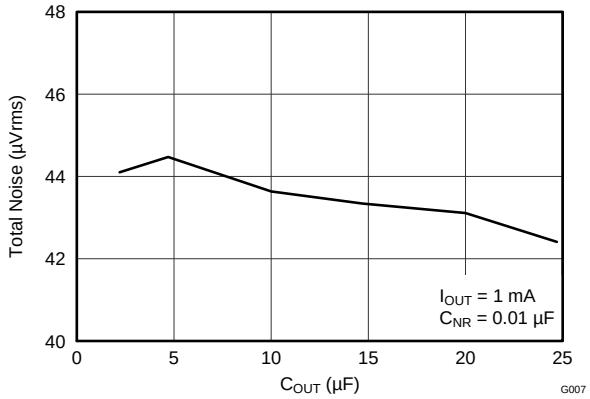
V_{IN} = 5.95 V

Figure 13. Power-Supply Rejection Ratio vs Frequency



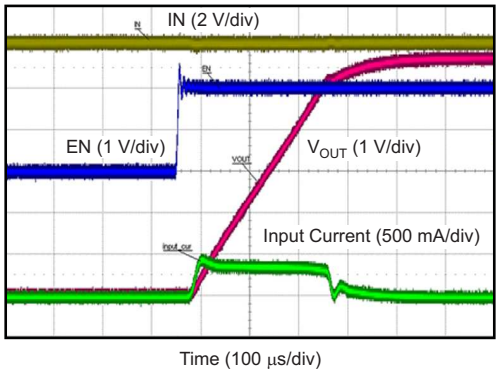
V_{IN} = 6 V

Figure 14. Total Noise vs C_{NR}



V_{IN} = 6 V

Figure 15. Total Noise vs C_{OUT}



C_{IN} = C_{OUT} = 20 µF I_{OUT} = 47 mA

Figure 16. Inrush Current at EN Turn-On

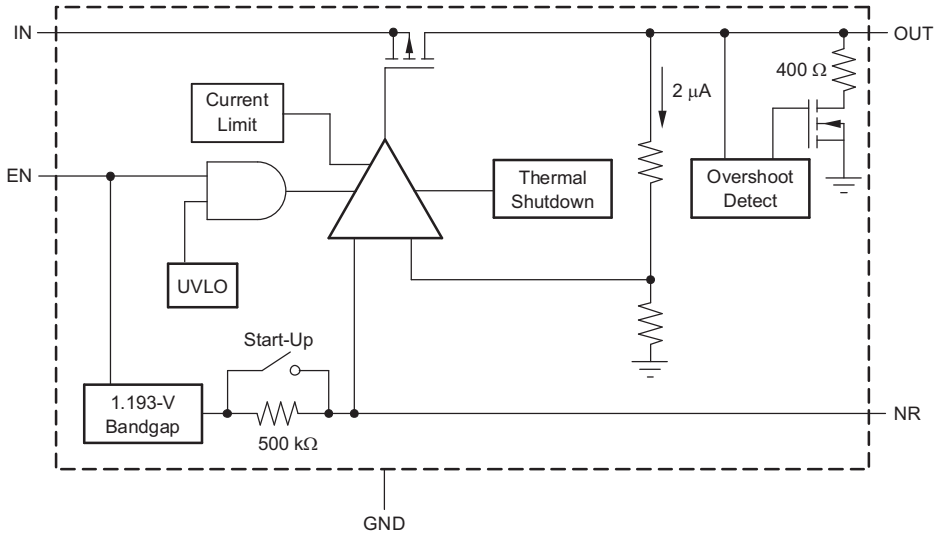
7 Detailed Description

7.1 Overview

The TPS799Lxx family of low-dropout (LDO) regulators combines the high performance required of many RF and precision analog applications with ultralow current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. The combination of high performance and low ground current also make these devices an excellent choice for portable applications. All versions have thermal and overcurrent protection, and are fully specified from –40°C to 125°C.

The TPS799Lxx family also features inrush current protection with an EN toggle start-up, and overshoot detection at the output. When the EN toggle is used to start the device, current limit protection is immediately activated, restricting the inrush current to the device (see Figure 16). If voltage at the output overshoots 5% from the nominal value, a pull-down resistor reduces the voltage to normal operating conditions, as shown in the *Functional Block Diagram*.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TPS799Lxx internal current limit helps protect the regulator during fault conditions. In current limit mode, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS799Lxx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited; therefore, if extended reverse voltage operation is anticipated, external limiting may be required.

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

7.3.3 Start Up

The TPS799Lxx uses a start-up circuit to quickly charge the noise reduction capacitor, C_{NR}, if present (see the *Functional Block Diagram*). This circuit allows for the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate for this configuration.

Note that for fastest start-up, apply V_{IN} first, and then drive the enable pin (EN) high. If EN is tied to IN, start-up is somewhat slower. The start-up switch is closed for approximately 135 µs. To ensure that C_{NR} is fully charged during start-up, use a 0.01-µF or smaller capacitor.

7.3.4 Undervoltage Lockout (UVLO)

The TPS799Lxx uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that undershoot transients are typically ignored on the input if these transients are less than 50 µs in duration.

7.4 Device Functional Modes

Driving EN over 1.2 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode, thus reducing the operating current to 150 nA, nominal.

8 Application and Implementation

8.1 Application Information

The TPS799Lxx family of LDO regulators provides high PSRR while maintaining ultralow current consumption. The family also features inrush current protection and overshoot detection at the output.

8.2 Typical Application

Figure 17 shows the basic circuit connections.

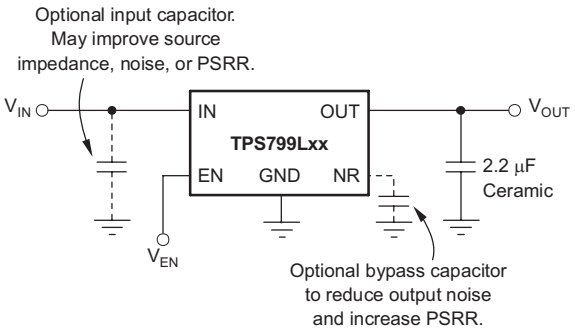


Figure 17. Typical Application Circuit

8.2.1 Design Requirements

8.2.1.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1-µF low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

The TPS799Lxx is designed to be stable with standard ceramic capacitors with values of 2.2 µF or greater. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1.0 Ω.

8.2.1.2 Output Noise

In most LDOs, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS799Lxx, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-µF noise reduction capacitor. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point; with C_{NR} = 0.01 µF total noise is approximately given by Equation 1:

$$V_N = \frac{10.5\mu V_{RMS}}{V} \times V_{OUT} \quad (1)$$

8.2.1.3 Dropout Voltage

The TPS799Lxx uses a PMOS pass transistor to achieve a low dropout voltage. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and $r_{DS(on)}$ of the PMOS pass element is the input-to-output resistance. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with the output current.

As with any linear regulator, PSRR degrades as (V_{IN} – V_{OUT}) approaches dropout. This effect is illustrated in Figure 8 through Figure 13 in the *Typical Characteristics* section.

Typical Application (continued)

8.2.1.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude, but increases the duration of the transient response. The transient response of the TPS799Lxx is enhanced by an active pull-down device that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pull-down device behaves like a 350-Ω resistor to ground.

8.2.1.5 Minimum Load

The TPS799Lxx is stable with no output load. To meet the specified accuracy, a minimum load of 500 µA is required. With loads less than 500 µA at junction temperatures near 125°C, the output can drift up enough to cause the output pull-down device to turn on. The output pull-down device limits voltage drift to 5% typically; however, ground current can increase by approximately 50 µA. In typical applications, the junction cannot reach high temperatures at light loads because there is no noticeable dissipated power. The specified ground current is then valid at no load in most applications.

8.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.3 Application Curves

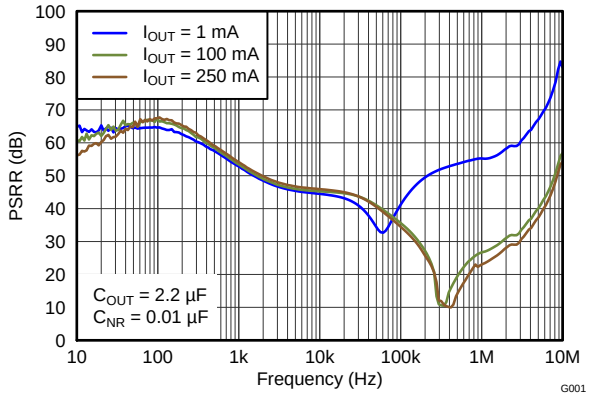


Figure 18. Power-Supply Rejection Ratio vs Frequency

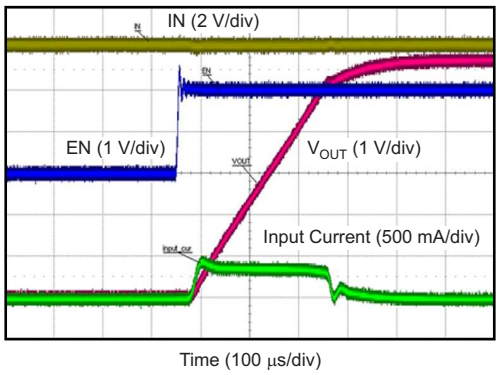


Figure 19. Inrush Current at EN Turn-On

8.3 Do's and Don'ts

Do place at least one 2.2-µF ceramic capacitor as close as possible to the OUT terminal of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do connect a 0.1-µF to 1.0-µF low equivalent series resistance (ESR) capacitor across the IN terminal and GND input of the regulator.

Do not exceed the absolute maximum ratings.

9 Power-Supply Recommendations

These devices are designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, connect the bypass capacitor directly to the GND pin of the device.

10.1.2 Thermal Information

10.1.2.1 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage resulting from overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS799Lxx is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the device into thermal shutdown degrades device reliability.

10.1.2.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the head from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table near the front of this data sheet. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = \left(V_{IN} - V_{OUT}\right) \cdot I_{OUT} \quad (2)$$

10.1.2.3 Package Mounting

Solder pad footprint recommendations for the TPS799Lxx are available from the Texas Instruments' web site at www.ti.com.

10.2 Layout Example

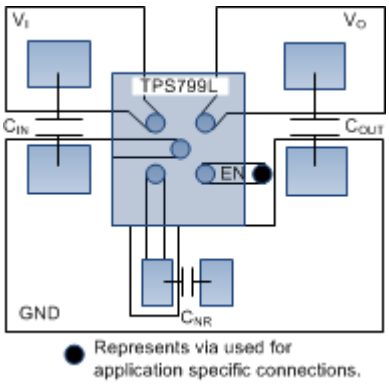


Figure 20. Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

评估模块 (EVM) 可与 TPS799Lxx 配套使用，帮助评估初始电路性能。 TPS799xx 评估模块 (EVM) 可通过德州仪器 (TI) 网站上的产品文件夹获取，也可直接从 TI 网上商店购买。

11.1.1.2 Spice 模型

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。 您可以从产品文件夹中的仿真模型下获取 TPS799Lxx 的 SPICE 模型。

11.1.2 器件命名规则

表 1. 器件命名规则(1)

产品	V_{OUT}
TPS799L**xx** ***yyy z***	**XX** 为标称输出电压（例如，57 = 5.7V）。 **YYY** 为封装标识符。 **Z** 为封装数量。

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问器件产品文件夹，此文件夹位于www.ti.com内。

11.2 文档支持

11.2.1 相关文档

更多相关文档，请参见以下用户指南：

- 《TPS799XXEVM-105 评估模块》，SLVU130

11.3 相关链接

表 2 列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 2. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS799L54	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS799L57	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 商标

蓝牙 is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS799L54YZYR	Active	Production	DSBGA (YZY) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GF
TPS799L54YZYR.B	Active	Production	DSBGA (YZY) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GF
TPS799L54YZYT	Active	Production	DSBGA (YZY) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GF
TPS799L54YZYT.B	Active	Production	DSBGA (YZY) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GF
TPS799L57YZYR	Active	Production	DSBGA (YZY) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	YF
TPS799L57YZYR.B	Active	Production	DSBGA (YZY) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	YF
TPS799L57YZYT	Active	Production	DSBGA (YZY) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	YF
TPS799L57YZYT.B	Active	Production	DSBGA (YZY) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	YF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

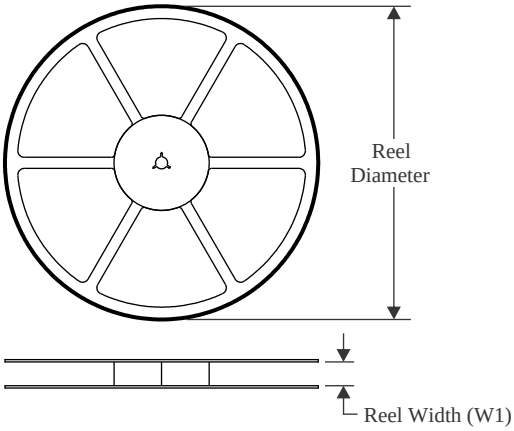
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

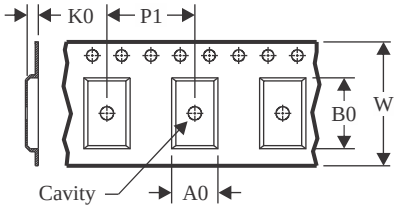
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

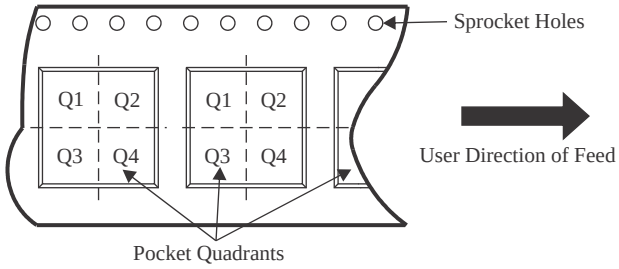


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

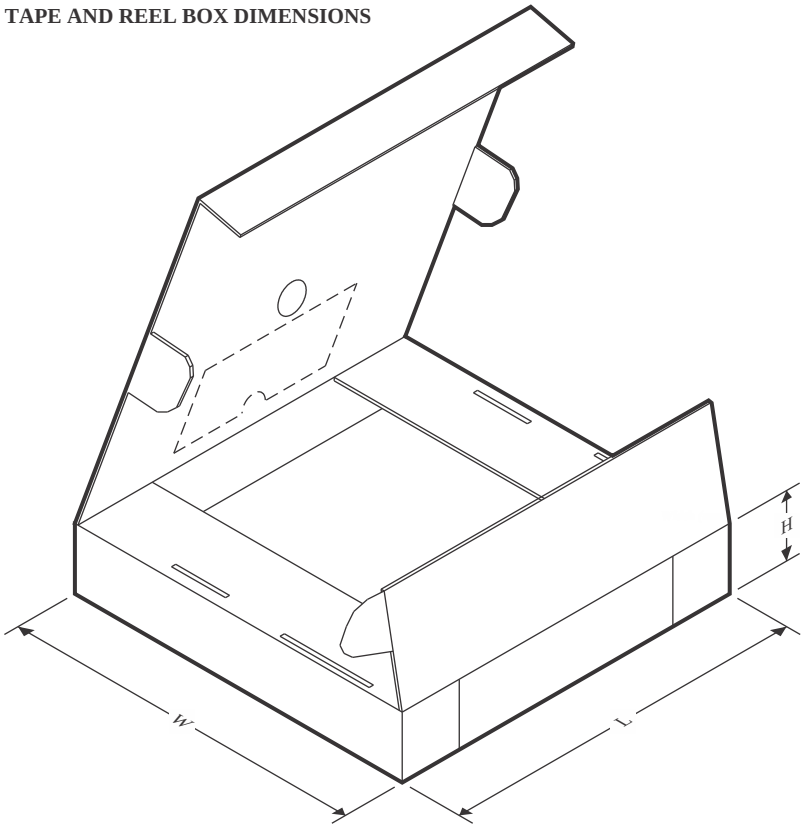
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS799L54YZYR	DSBGA	YZY	5	3000	180.0	8.4	1.08	1.45	0.61	2.0	8.0	Q1
TPS799L54YZYT	DSBGA	YZY	5	250	180.0	8.4	1.08	1.45	0.61	2.0	8.0	Q1
TPS799L57YZYR	DSBGA	YZY	5	3000	180.0	8.4	1.08	1.45	0.61	2.0	8.0	Q1
TPS799L57YZYT	DSBGA	YZY	5	250	180.0	8.4	1.08	1.45	0.61	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS799L54YZYR	DSBGA	YZY	5	3000	182.0	182.0	20.0
TPS799L54YZYT	DSBGA	YZY	5	250	182.0	182.0	20.0
TPS799L57YZYR	DSBGA	YZY	5	3000	182.0	182.0	20.0
TPS799L57YZYT	DSBGA	YZY	5	250	182.0	182.0	20.0

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