

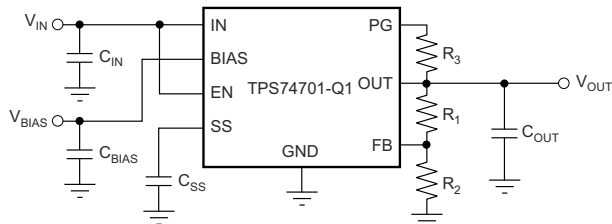
## TPS74701-Q1 具有可编程软启动功能的汽车类 500mA 低压降线性稳压器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：-40°C 至 +125°C， $T_A$
- $V_{OUT}$  范围：0.8V 至 3.6V
- $V_{IN}$  范围：0.8V 至 5.5V
- $V_{BIAS}$  范围：2.7V 至 5.5V
- 低压降：500mA 下的典型值为 20mV， $V_{BIAS} = 5V$
- 电源正常 (PG) 输出可实现电源监视或为其他电源提供时序信号
- 线路、负载和温度范围内的精度为 0.95%
- 可编程软启动可提供线性电压启动
- $V_{BIAS}$  支持低  $V_{IN}$  运行，具有良好的瞬态响应
- 与  $\geq 2.2 \mu F$  的任何输出电容器一起工作时可保持稳定
- 采用小型 3mm × 3mm 10 引脚 VSON 封装

## 2 应用

- 汽车音响主机
- 信息娱乐系统与仪表组
- 远程信息处理控制单元
- 前置摄像头和后置摄像头



典型应用电路 (可调节)

## 3 说明

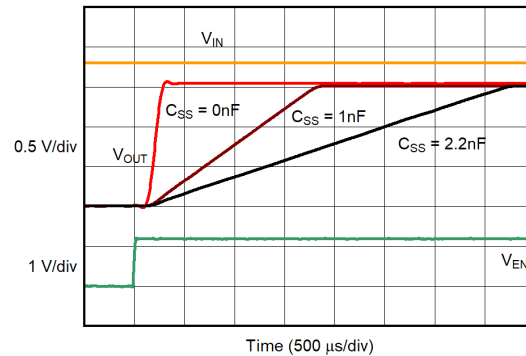
TPS74701-Q1 低压降 (LDO) 线性稳压器可面向多种应用提供易于使用的稳健型电源管理解决方案。用户可编程软启动通过减少容性浪涌电流，最大限度地减少了输入电源上的应力，并且单调启动旨在为多种不同类型的处理器和 ASIC 供电。借助使能输入和电源正常输出，可通过外部稳压器轻松进行时序控制，因此可为各种具有特殊启动要求的应用配置满足其时序要求的解决方案。

该器件还具有高精度的参考电压电路和误差放大器，可在整个负载、线路、温度和过程范围内提供 0.95% 精度。该器件在使用大于或等于 2.2μF 的任何类型的电容器时均能保持稳定，并完全符合 AEC-Q100 标准。

## 封装信息

| 器件型号        | 封装 <sup>(1)</sup> | 封装尺寸 <sup>(2)</sup> |
|-------------|-------------------|---------------------|
| TPS74701-Q1 | DRC ( VSON , 10 ) | 3mm × 3mm           |

- (1) 如需更多信息，请参阅 [机械、封装和可订购信息](#)。  
 (2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



导通响应



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## 4 Pin Configuration and Functions

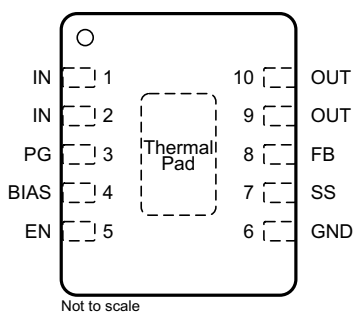


图 4-1. DRC Package, 10-Pin VSON (Top View)

表 4-1. Pin Functions

| PIN         |       | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                             |
|-------------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME        | NO.   |      |                                                                                                                                                                                                                                                                                                                                                         |
| BIAS        | 4     | I    | Bias pin. Input voltage for error amplifier, reference, and internal control circuits.                                                                                                                                                                                                                                                                  |
| EN          | 5     | I    | Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left unconnected.                                                                                                                                                                                             |
| FB          | 8     | I    | Feedback pin. The feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.                                                                                                                                                                                       |
| GND         | 6     | —    | Ground pin.                                                                                                                                                                                                                                                                                                                                             |
| IN          | 1, 2  | I    | Input pin. This pin supplies the input voltage to the device. For best transient response and to minimize input impedance, use the recommended value or larger capacitor from IN to GND, as listed in the <a href="#">Recommended Operating Conditions</a> table. Place the input capacitors as close as possible to the IN and GND pins of the device. |
| OUT         | 9, 10 | O    | Output pin. Regulated output voltage, a small capacitor (total typical capacitance $\geq 2.2 \mu\text{F}$ , ceramic) is needed from this pin to ground to assure stability. Place the output capacitors as close as possible to the OUT and GND pins of the device.                                                                                     |
| PG          | 3     | O    | Power-good pin. This pin is an open-drain, active-high output that indicates the status of $V_{\text{OUT}}$ ; see the <a href="#">Power Good</a> section for additional information.                                                                                                                                                                    |
| SS          | 7     | —    | Soft-start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left unconnected, the regulator output soft-start ramp time is typically 200 $\mu\text{s}$ ; see the <a href="#">Programmable Soft-Start</a> section for further information.                                                                        |
| Thermal Pad | —     | —    | Connect the pad to GND for the best possible thermal performance.                                                                                                                                                                                                                                                                                       |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)<sup>(1)</sup>

|                       |                                    | MIN                     | MAX                           | UNIT |
|-----------------------|------------------------------------|-------------------------|-------------------------------|------|
| $V_{IN}$ , $V_{BIAS}$ | Input voltage                      | - 0.3                   | 6                             | V    |
| $V_{EN}$              | Enable voltage                     | - 0.3                   | 6                             | V    |
| $V_{PG}$              | Power good voltage                 | - 0.3                   | 6                             | V    |
| $I_{PG}$              | PG sink current                    | 0                       | 1.5                           | mA   |
| $V_{SS}$              | Soft-start voltage                 | - 0.3                   | 6                             | V    |
| $V_{FB}$              | Feedback voltage                   | - 0.3                   | 6                             | V    |
| $V_{OUT}$             | Output voltage                     | - 0.3                   | $V_{IN} + 0.3$ <sup>(2)</sup> | V    |
| $I_{OUT}$             | Output current                     | Internally limited      |                               |      |
| $I_{CL}$              | Output short-circuit duration      | Indefinite              |                               |      |
| $P_{DISS}$            | Continuous total power dissipation | See Thermal Information |                               |      |
| $T_J$ , $T_{stg}$     | Junction temperature               | - 40                    | 150                           | °C   |
|                       | Storage temperature                | - 55                    | 150                           |      |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The absolute maximum rating is  $V_{IN} + 0.3$  V or 6.0 V, whichever is smaller.

### 5.2 ESD Ratings

|             |                         | VALUE                                                      | UNIT  |
|-------------|-------------------------|------------------------------------------------------------|-------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>    | ±2000 |
|             |                         | Charged device model (CDM), per AEC specification Q100-011 | ±500  |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                           |                                | MIN                                                 | NOM                            | MAX | UNIT |
|---------------------------|--------------------------------|-----------------------------------------------------|--------------------------------|-----|------|
| $V_{IN}$                  | Input supply voltage           | $V_{OUT} + V_{DO}$<br>( $V_{IN}$ )                  | $V_{OUT} + 0.3$                | 5.5 | V    |
| $V_{EN}$                  | Enable supply voltage          |                                                     | $V_{IN}$                       | 5.5 | V    |
| $V_{BIAS}$ <sup>(1)</sup> | Bias supply voltage            | $V_{OUT} + V_{DO}$<br>( $V_{BIAS}$ ) <sup>(2)</sup> | $V_{OUT} + 1.6$ <sup>(2)</sup> | 5.5 | V    |
| $V_{OUT}$                 | Output voltage                 | 0.8                                                 |                                | 3.3 | V    |
| $I_{OUT}$                 | Output current                 | 0                                                   |                                | 500 | mA   |
| $C_{OUT}$                 | Output capacitor               | 2.2                                                 |                                |     | μF   |
| $C_{IN}$ <sup>(3)</sup>   | Input capacitor                | 1                                                   |                                |     | μF   |
| $C_{BIAS}$                | Bias capacitor                 | 0.1                                                 | 1                              |     | μF   |
| $T_J$                     | Operating junction temperature | - 40                                                |                                | 150 | °C   |

- (1) BIAS supply is required when  $V_{IN}$  is below  $V_{OUT} + 1.62$  V.
- (2)  $V_{BIAS}$  has a minimum voltage of 2.7 V or  $V_{OUT} + V_{DO}$  ( $V_{BIAS}$ ), whichever is higher.
- (3) If  $V_{IN}$  and  $V_{BIAS}$  are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 μF.

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TPS74701-Q1 |                           | UNIT |
|-------------------------------|----------------------------------------------|-------------|---------------------------|------|
|                               |                                              | DRC (VSON)  | DRC (VSON) <sup>(2)</sup> |      |
|                               |                                              | 10 PINS     | 10 PINS                   |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 41.5        | 47.2                      | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 78          | 63.7                      | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | N/A         | 19.5                      | °C/W |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 0.7         | 4.2                       | °C/W |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 11.3        | 19.4                      | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 6.6         | 3.3                       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application note](#).
- (2) New chip.

## 5.5 Electrical Characteristics

at  $V_{EN} = 1.1\text{ V}$ ,  $V_{IN} = V_{OUT} + 0.3\text{ V}$ ,  $C_{BIAS} = 0.1\text{ }\mu\text{F}$ ,  $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{NR} = 1\text{ nF}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{BIAS} = 5.0\text{ V}$ , and  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (Legacy Chip) and  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (New Chip), (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$

| PARAMETER                         |                                                    | TEST CONDITIONS                                                                                               | MIN       | TYP                 | MAX   | UNIT              |
|-----------------------------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------|-----------|---------------------|-------|-------------------|
| $V_{REF}$                         | Internal reference (Adj.)                          | $T_A = +25^\circ\text{C}$                                                                                     | 0.796     | 0.8                 | 0.804 | V                 |
| $V_{OUT}$                         | Output voltage range                               | $V_{IN} = 5\text{ V}$ , $I_{OUT} = 0.5\text{ A}$                                                              | $V_{REF}$ |                     | 3.6   | V                 |
|                                   | Accuracy <sup>(1)</sup>                            | $2.97\text{ V} \leq V_{BIAS} \leq 5.5\text{ V}$ , $50\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$ (Legacy Chip) | -2        | $\pm 0.5$           | 2     | %                 |
|                                   |                                                    | $2.97\text{ V} \leq V_{BIAS} \leq 5.5\text{ V}$ , $50\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$ (New Chip)    | -1.25     | $\pm 0.3$           | 1.25  |                   |
| $\Delta V_{OUT} (\Delta V_{IN})$  | Line regulation                                    | $V_{OUT(nom)} + 0.3 \leq V_{IN} \leq 5.5\text{ V}$ (Legacy Chip)                                              |           | 0.03                |       | %/V               |
|                                   |                                                    | $V_{OUT(nom)} + 0.3 \leq V_{IN} \leq 5.5\text{ V}$ (New Chip)                                                 |           | 0.001               |       |                   |
| $\Delta V_{OUT} (\Delta I_{OUT})$ | Load regulation                                    | $50\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$ (Legacy Chip)                                                   |           | 0.09                |       | %/A               |
|                                   |                                                    | $50\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$ (New Chip)                                                      |           | 0.11                |       |                   |
| $V_{DO}$                          | $V_{IN}$ dropout voltage <sup>(2)</sup>            | $I_{OUT} = 0.5\text{ A}$ , $V_{BIAS} - V_{OUT(nom)} \geq 1.62\text{ V}$ (Legacy Chip) <sup>(3)</sup>          |           | 50                  | 120   | mV                |
|                                   |                                                    | $I_{OUT} = 0.5\text{ A}$ , $V_{BIAS} - V_{OUT(nom)} \geq 1.62\text{ V}$ (New Chip) <sup>(3)</sup>             |           | 20                  | 40    |                   |
|                                   | $V_{BIAS}$ dropout voltage <sup>(2)</sup>          | $I_{OUT} = 0.5\text{ A}$ , $V_{IN} = V_{BIAS}$ (Legacy Chip)                                                  |           | 1.31                | 1.39  | V                 |
|                                   |                                                    | $I_{OUT} = 0.5\text{ A}$ , $V_{IN} = V_{BIAS}$ (New Chip)                                                     |           | 1.1                 | 1.3   |                   |
| $I_{CL}$                          | Output current limit                               | $V_{OUT} = 80\% \times V_{OUT(nom)}$ (Legacy Chip)                                                            | 800       |                     | 1350  | mA                |
|                                   |                                                    | $V_{OUT} = 80\% \times V_{OUT(nom)}$ (New Chip)                                                               | 800       |                     | 1350  |                   |
| $I_{BIAS}$                        | BIAS pin current                                   | (Legacy Chip)                                                                                                 |           | 1                   | 2     | mA                |
|                                   |                                                    | (New Chip)                                                                                                    |           | 1                   | 1.2   |                   |
| $I_{SHDN}$                        | Shutdown supply current ( $I_{GND}$ )              | $V_{EN} \leq 0.4\text{ V}$ (Legacy Chip)                                                                      |           | 1                   | 50    | $\mu\text{A}$     |
|                                   |                                                    | $V_{EN} \leq 0.4\text{ V}$ (New Chip)                                                                         |           | 1                   | 10    |                   |
| $I_{FB}$                          | Feedback pin current                               | (Legacy Chip)                                                                                                 | -1        | 0.15                | 1     | $\mu\text{A}$     |
|                                   |                                                    | (New Chip)                                                                                                    | -30       | 0.15                | 30    | nA                |
| PSRR                              | Power-supply rejection ( $V_{IN}$ to $V_{OUT}$ )   | 1 kHz, $I_{OUT} = 0.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (Legacy Chip)            |           | 60                  |       | dB                |
|                                   |                                                    | 1 kHz, $I_{OUT} = 0.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (New Chip)               |           | 76                  |       |                   |
|                                   |                                                    | 300 kHz, $I_{OUT} = 0.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (Legacy Chip)          |           | 30                  |       |                   |
|                                   |                                                    | 300 kHz, $I_{OUT} = 0.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (New Chip)             |           | 50                  |       |                   |
|                                   | Power-supply rejection ( $V_{BIAS}$ to $V_{OUT}$ ) | 1 kHz, $I_{OUT} = 0.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (Legacy Chip)            |           | 50                  |       |                   |
|                                   |                                                    | 1 kHz, $I_{OUT} = 0.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (New Chip)               |           | 59                  |       |                   |
|                                   |                                                    | 300 kHz, $I_{OUT} = 0.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (Legacy Chip)          |           | 30                  |       |                   |
|                                   |                                                    | 300 kHz, $I_{OUT} = 0.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (New Chip)             |           | 49                  |       |                   |
| $V_n$                             | Output noise voltage                               | BW = 100 Hz to 100 kHz, $I_{OUT} = 0.5\text{ A}$ , $C_{SS} = 1\text{ nF}$ (Legacy Device)                     |           | $25 \times V_{OUT}$ |       | $\mu\text{ Vrms}$ |
|                                   |                                                    | BW = 100 Hz to 100 kHz, $I_{OUT} = 0.5\text{ A}$ , $C_{SS} = 1\text{ nF}$ (New Chip)                          |           | $20 \times V_{OUT}$ |       |                   |

## 5.5 Electrical Characteristics (续)

at  $V_{EN} = 1.1\text{ V}$ ,  $V_{IN} = V_{OUT} + 0.3\text{ V}$ ,  $C_{BIAS} = 0.1\text{ }\mu\text{F}$ ,  $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{NR} = 1\text{ nF}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{BIAS} = 5.0\text{ V}$ , and  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (Legacy Chip) and  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (New Chip), (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$

| PARAMETER            |                              | TEST CONDITIONS                                                                        | MIN | TYP | MAX   | UNIT              |
|----------------------|------------------------------|----------------------------------------------------------------------------------------|-----|-----|-------|-------------------|
| t <sub>STR</sub>     | Minimum startup time         | R <sub>LOAD</sub> for I <sub>OUT</sub> = 0.5 A, C <sub>SS</sub> = open (Legacy Device) | 200 |     |       | μs                |
|                      |                              | R <sub>LOAD</sub> for I <sub>OUT</sub> = 0.5 A, C <sub>SS</sub> = open (New Chip)      | 250 |     |       |                   |
| I <sub>SS</sub>      | Soft-start charging current  | V <sub>SS</sub> = 0.4 V (Legacy Chip)                                                  | 440 |     |       | nA                |
|                      |                              | V <sub>SS</sub> = 0.4 V (New Chip)                                                     | 530 |     |       |                   |
| V <sub>EN(hi)</sub>  | Enable input high level      |                                                                                        | 1.1 |     | 5.5   | V                 |
| V <sub>EN(lo)</sub>  | Enable input low level       |                                                                                        | 0   |     | 0.4   | V                 |
| V <sub>EN(hys)</sub> | Enable pin hysteresis        | (Legacy Chip)                                                                          | 50  |     |       | mV                |
|                      |                              | (New Chip)                                                                             | 55  |     |       |                   |
| V <sub>EN(dg)</sub>  | Enable pin deglitch time     |                                                                                        | 20  |     |       | μs                |
| I <sub>EN</sub>      | Enable pin current           | V <sub>EN</sub> = 5 V (Legacy Chip)                                                    | 0.1 |     | 1     | μA                |
|                      |                              | V <sub>EN</sub> = 5 V (New Chip)                                                       | 0.1 |     | 0.3   |                   |
| V <sub>IT</sub>      | PG trip threshold            | V <sub>OUT</sub> decreasing                                                            | 85  | 90  | 94    | %V <sub>OUT</sub> |
| V <sub>HYS</sub>     | PG trip hysteresis           |                                                                                        | 3   |     |       | %V <sub>OUT</sub> |
| V <sub>PG(lo)</sub>  | PG output low voltage        | I <sub>PG</sub> = 1 mA (sinking), V <sub>OUT</sub> < V <sub>IT</sub> (Legacy Chip)     |     |     | 0.3   | V                 |
|                      |                              | I <sub>PG</sub> = 1 mA (sinking), V <sub>OUT</sub> < V <sub>IT</sub> (New Chip)        |     |     | 0.125 |                   |
| I <sub>PG(lkg)</sub> | PG leakage current           | V <sub>PG</sub> = 5.25 V, V <sub>OUT</sub> > V <sub>IT</sub> (Legacy Chip)             | 0.1 |     | 1     | μA                |
|                      |                              | V <sub>PG</sub> = 5.25 V, V <sub>OUT</sub> > V <sub>IT</sub> (New Chip)                | 0.1 |     | 0.05  |                   |
| T <sub>SD</sub>      | Thermal shutdown temperature | Shutdown, temperature increasing                                                       | 165 |     |       | °C                |
|                      |                              | Reset, temperature decreasing                                                          | 140 |     |       |                   |

- (1) Adjustable devices tested at  $0.8\text{ V}$ ; resistor tolerance is not taken into account.
- (2) Dropout is defined as the voltage from  $V_{IN}$  to  $V_{OUT}$  when  $V_{OUT}$  is 3% below nominal.
- (3)  $1.62\text{ V}$  is a test condition of this device and can be adjusted by referring to Figure 5-29.

## 5.6 Typical Characteristics: $I_{OUT} = 50\text{ mA}$

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$  (unless otherwise noted)

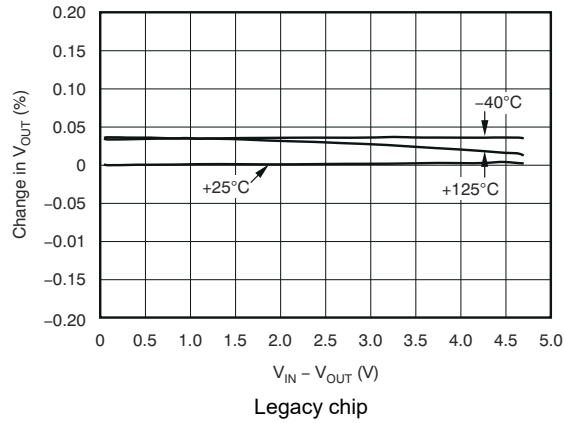
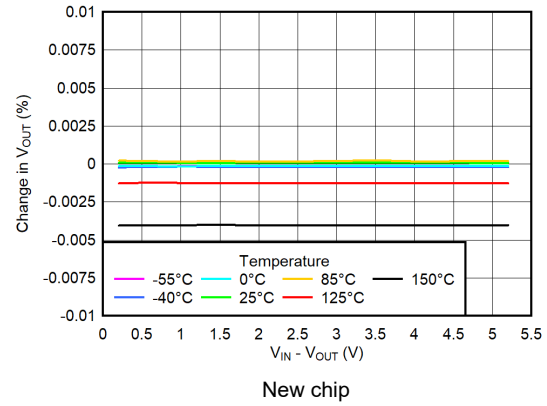
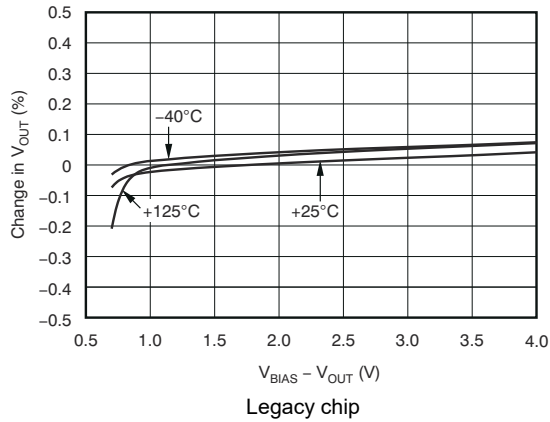
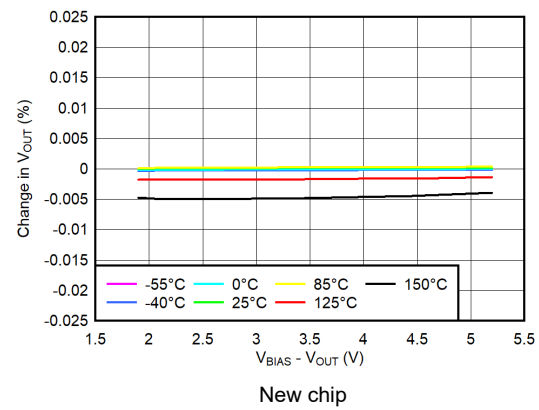
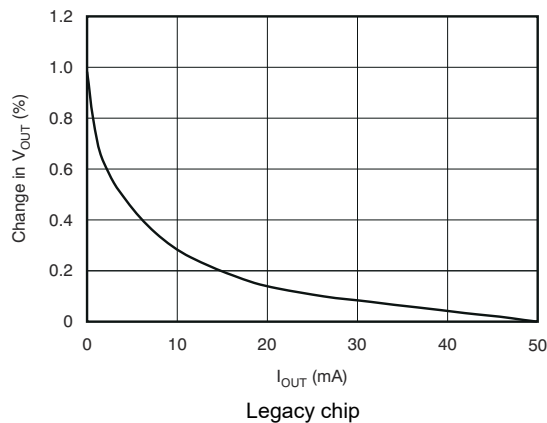
图 5-1.  $V_{IN}$  Line Regulation图 5-2.  $V_{IN}$  Line Regulation图 5-3.  $V_{BIAS}$  Line Regulation图 5-4.  $V_{BIAS}$  Line Regulation

图 5-5. Load Regulation at Light Load

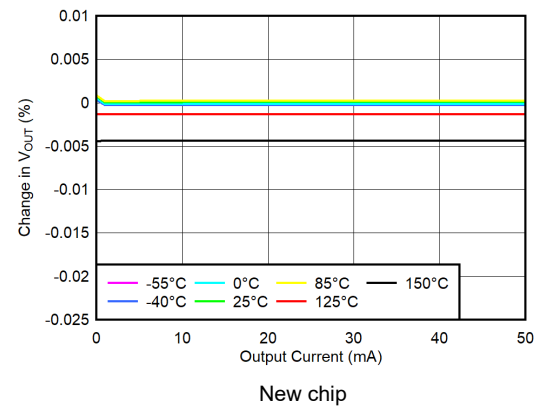


图 5-6. Load Regulation at Light Load



## 5.6 Typical Characteristics: $I_{OUT} = 50 \text{ mA}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3 \text{ V}$ ,  $V_{BIAS} = 5 \text{ V}$ ,  $I_{OUT} = 50 \text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1 \mu\text{F}$ ,  $C_{BIAS} = 4.7 \mu\text{F}$ , and  $C_{OUT} = 10 \mu\text{F}$  (unless otherwise noted)

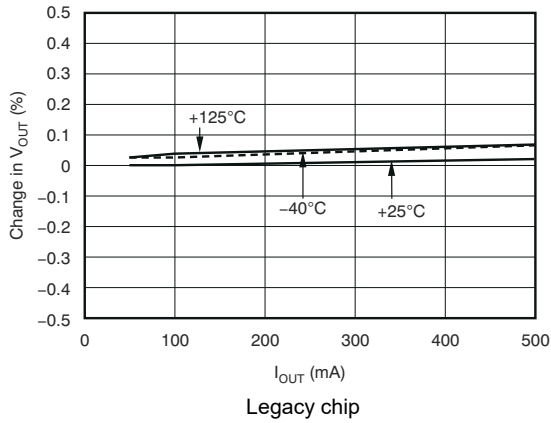


图 5-7. Load Regulation

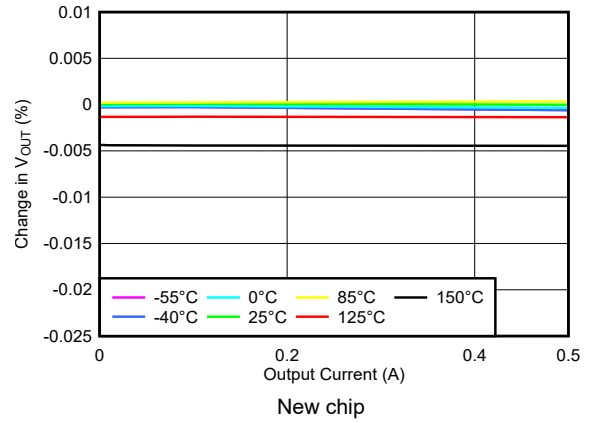


图 5-8. Load Regulation

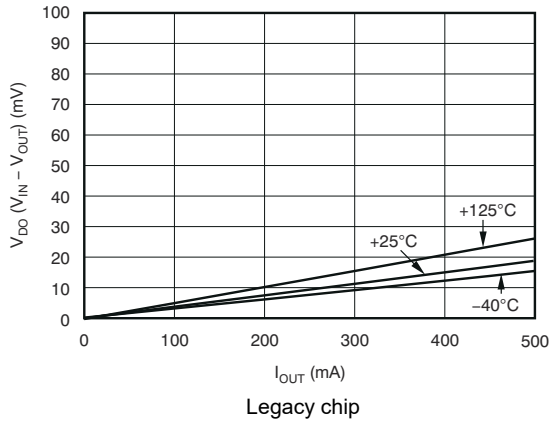


图 5-9. Dropout Voltage vs  $I_{OUT}$  and Temperature ( $T_J$ )

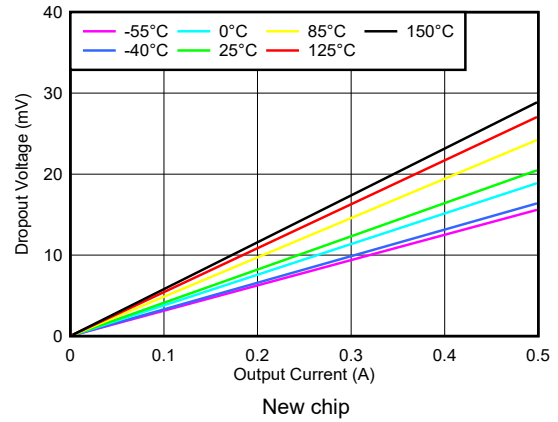


图 5-10.  $V_{IN}$  Dropout Voltage vs  $I_{OUT}$  and Temperature ( $T_J$ )

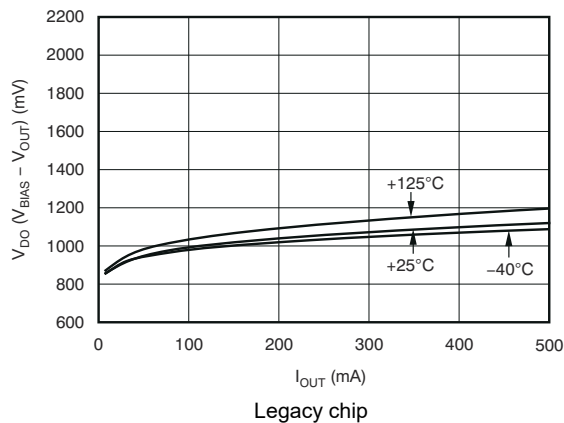


图 5-11.  $V_{BIAS}$  Dropout Voltage vs  $I_{OUT}$  and Temperature ( $T_J$ )

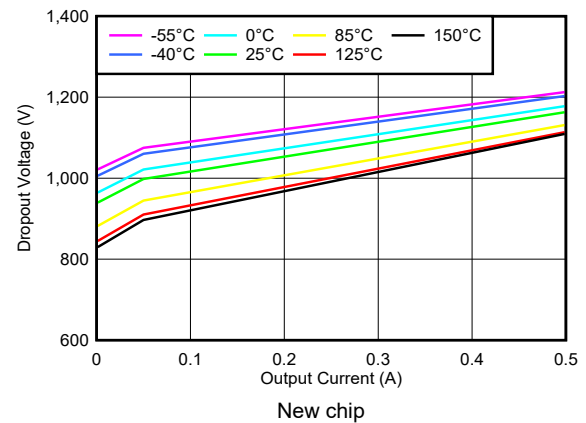


图 5-12.  $V_{BIAS}$  Dropout Voltage vs  $I_{OUT}$  and Temperature ( $T_J$ )

## 5.6 Typical Characteristics: $I_{OUT} = 50\text{ mA}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$  (unless otherwise noted)

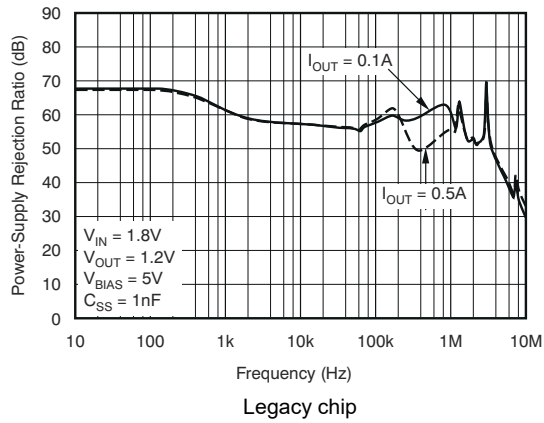


图 5-13.  $V_{BIAS}$  PSRR vs Frequency

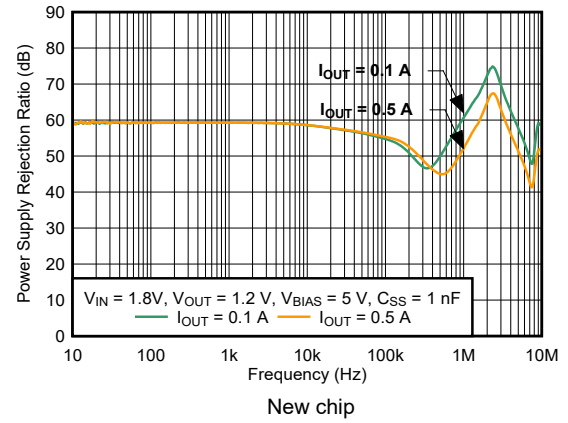


图 5-14.  $V_{BIAS}$  PSRR vs Frequency

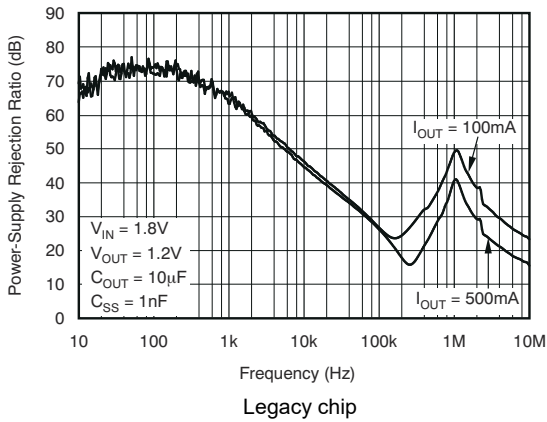


图 5-15.  $V_{IN}$  PSRR vs Frequency

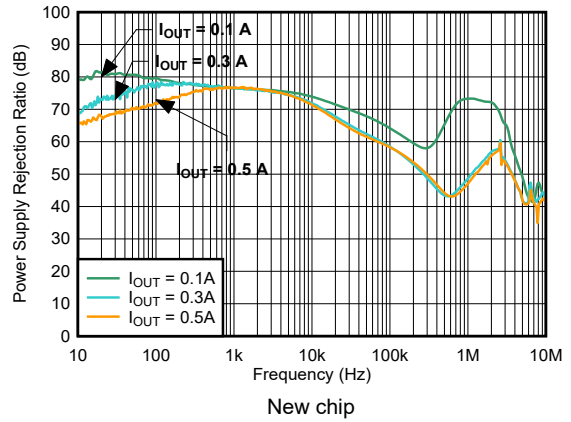


图 5-16.  $V_{IN}$  PSRR vs Frequency

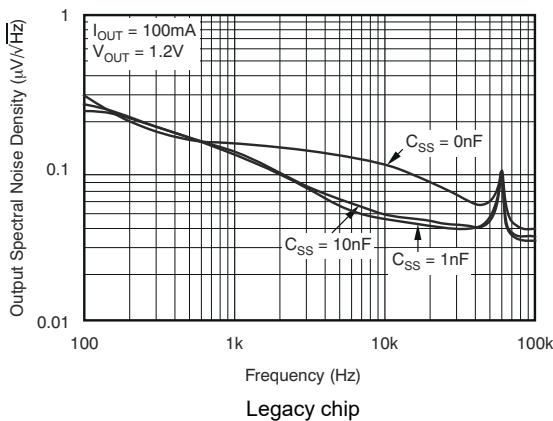


图 5-17. Noise Spectral Density

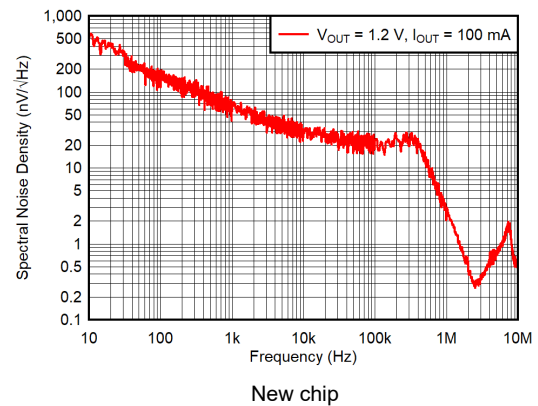


图 5-18. Noise Spectral Density

## 5.6 Typical Characteristics: $I_{OUT} = 50\text{ mA}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$  (unless otherwise noted)

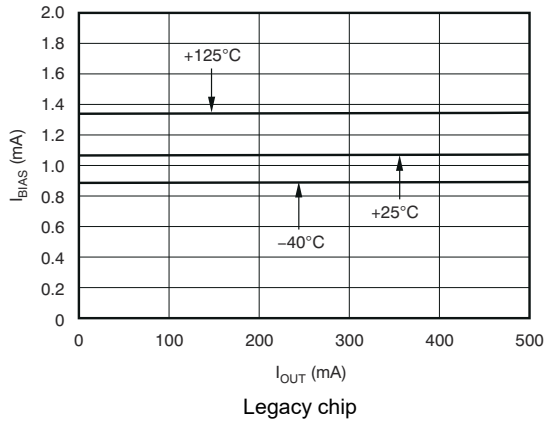


图 5-19. BIAS Pin Current vs  $I_{OUT}$  and Temperature ( $T_J$ )

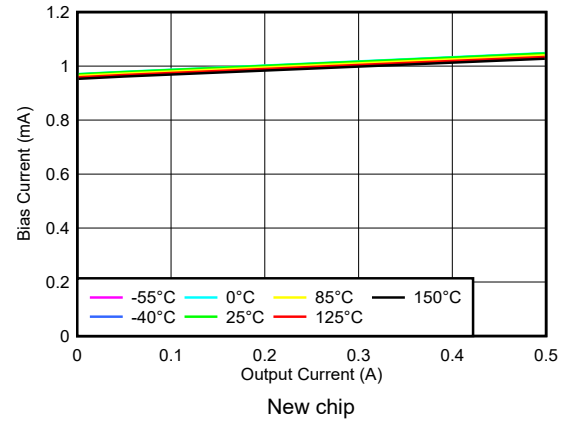


图 5-20. BIAS Pin Current vs Output Current and Temperature ( $T_J$ )

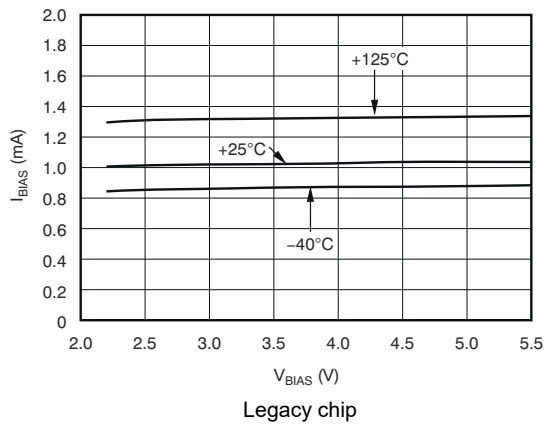


图 5-21. BIAS Pin Current vs  $V_{BIAS}$  and Temperature ( $T_J$ )

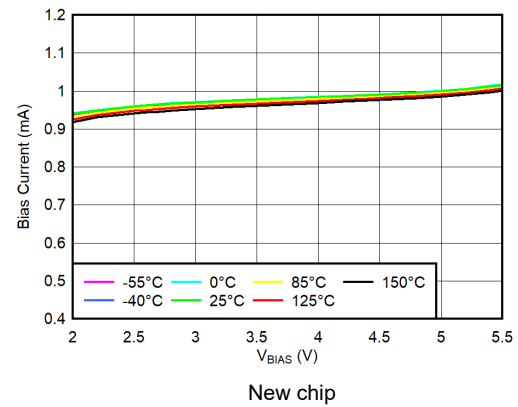


图 5-22. BIAS Pin Current vs  $V_{BIAS}$  and Temperature ( $T_J$ )

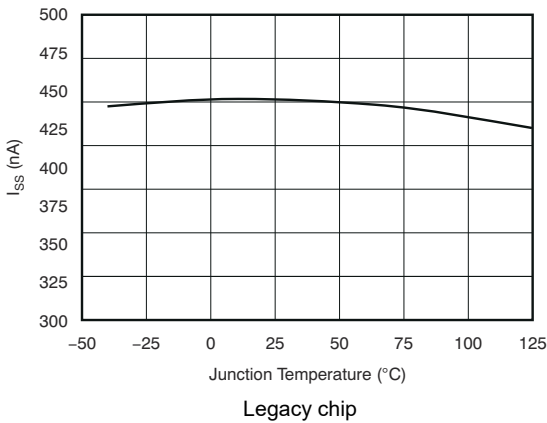


图 5-23. Soft-Start Charging Current ( $I_{SS}$ ) vs Temperature ( $T_J$ )

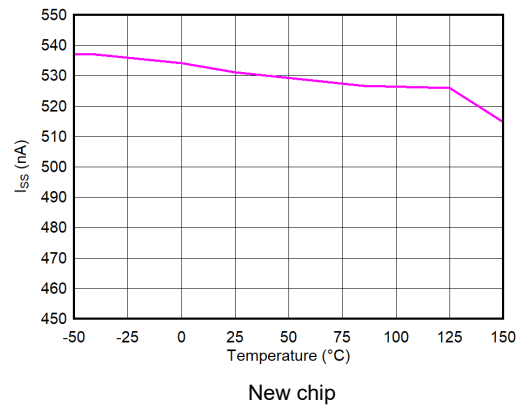


图 5-24. Soft-Start Charging Current ( $I_{SS}$ ) vs Temperature ( $T_J$ )

## 5.6 Typical Characteristics: $I_{OUT} = 50 \text{ mA}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3 \text{ V}$ ,  $V_{BIAS} = 5 \text{ V}$ ,  $I_{OUT} = 50 \text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1 \mu\text{F}$ ,  $C_{BIAS} = 4.7 \mu\text{F}$ , and  $C_{OUT} = 10 \mu\text{F}$  (unless otherwise noted)

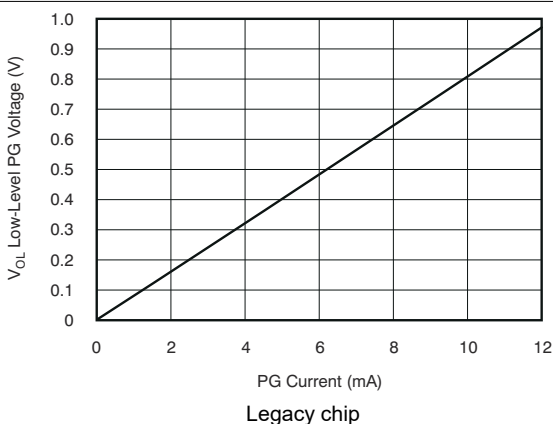


图 5-25. Low-Level PG Voltage vs Current

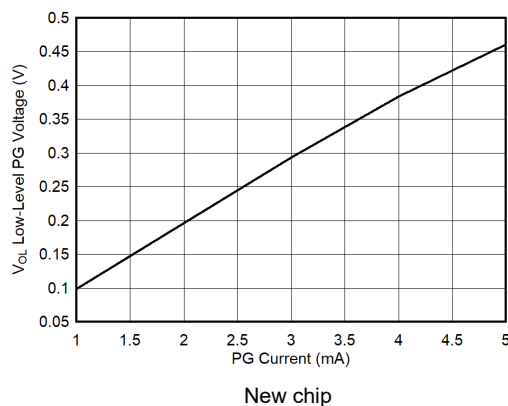


图 5-26. Low-Level PG Voltage vs Current

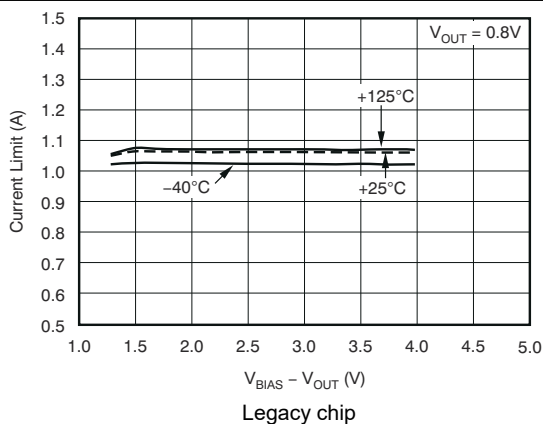


图 5-27. Current Limit vs ( $V_{BIAS} - V_{OUT}$ )

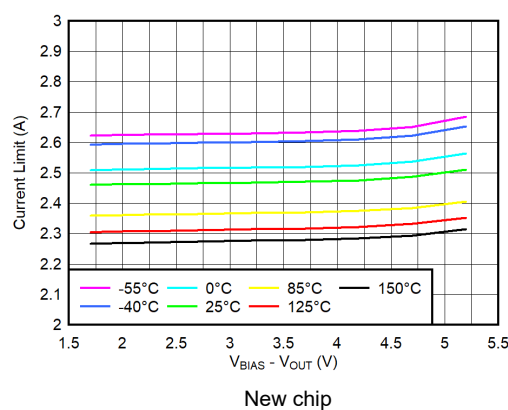


图 5-28. Current Limit vs ( $V_{BIAS} - V_{OUT}$ )

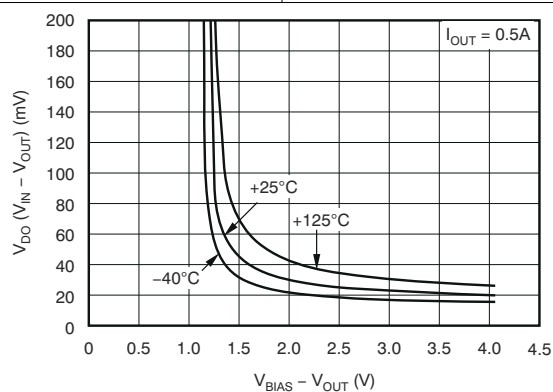


图 5-29. Dropout Voltage vs ( $V_{BIAS} - V_{OUT}$ ) and Temperature ( $T_J$ )

## 5.7 Typical Characteristics: $V_{EN} = V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN} = 1.8\text{ V}$ ,  $V_{OUT} = 1.5\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$  (unless otherwise noted)

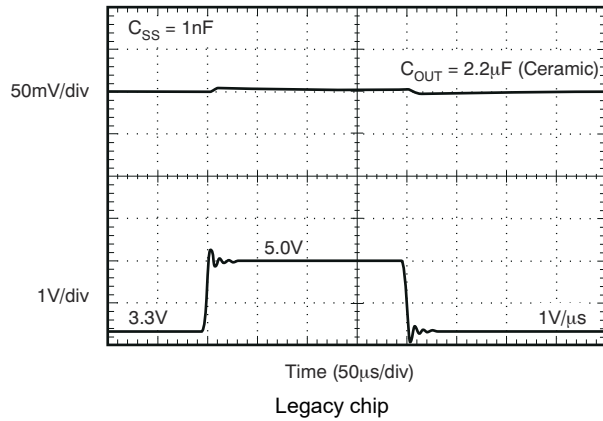


图 5-30.  $V_{BIAS}$  Line Transient

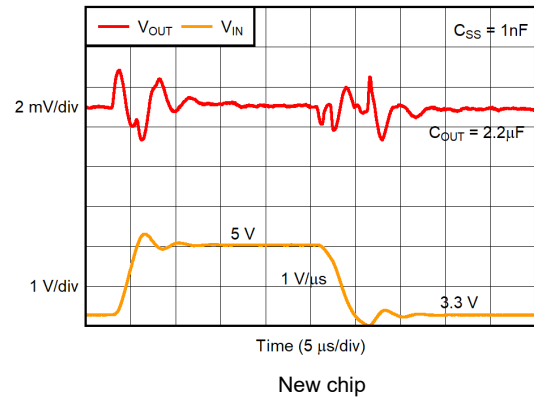


图 5-31.  $V_{BIAS}$  Line Transient

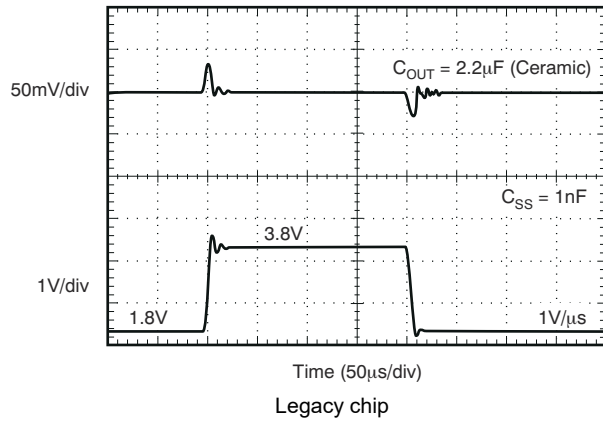


图 5-32.  $V_{IN}$  Line Transient

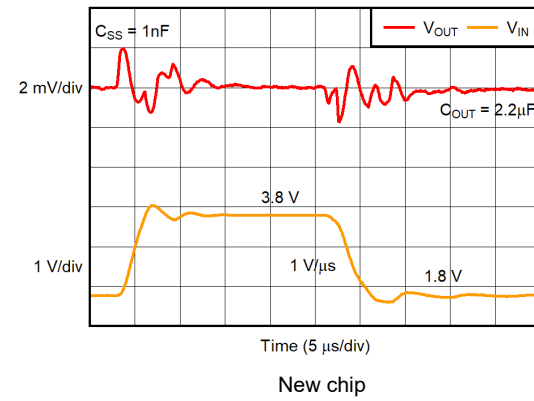


图 5-33.  $V_{IN}$  Line Transient

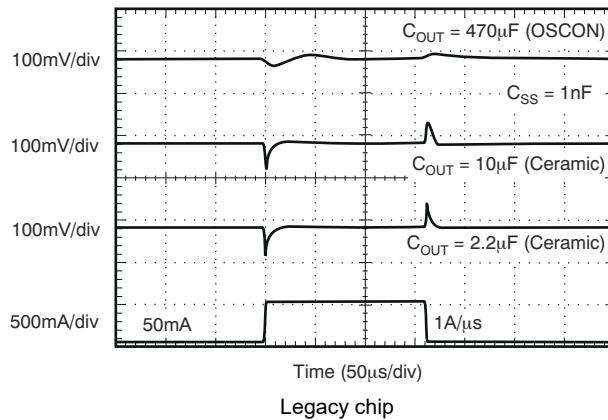


图 5-34. Output Load Transient Response

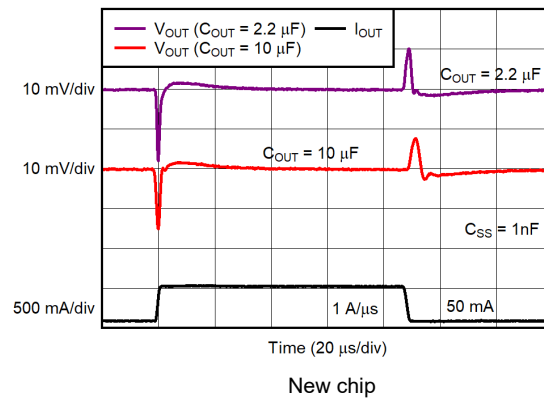


图 5-35. Output Load Transient Response

## 5.7 Typical Characteristics: $V_{EN} = V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN} = 1.8\text{ V}$ ,  $V_{OUT} = 1.5\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$  (unless otherwise noted)

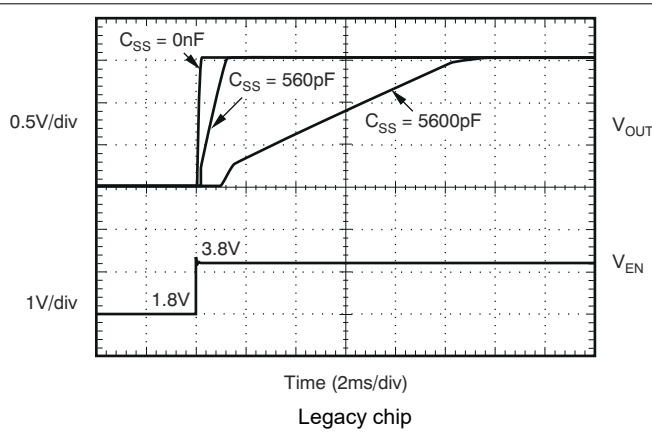


图 5-36. Turn-On Response

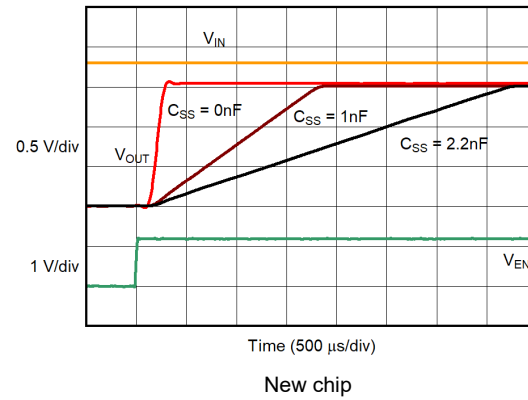


图 5-37. Turn-On Response

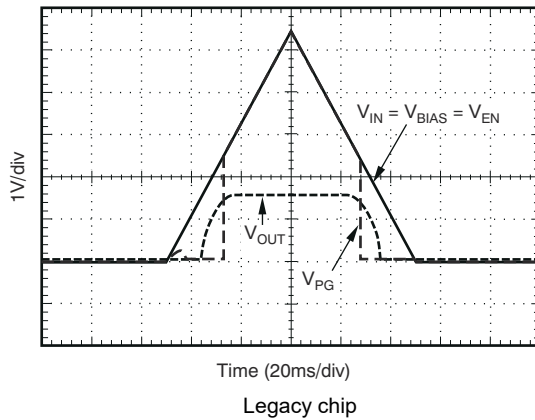


图 5-38. Power-Up and Power-Down

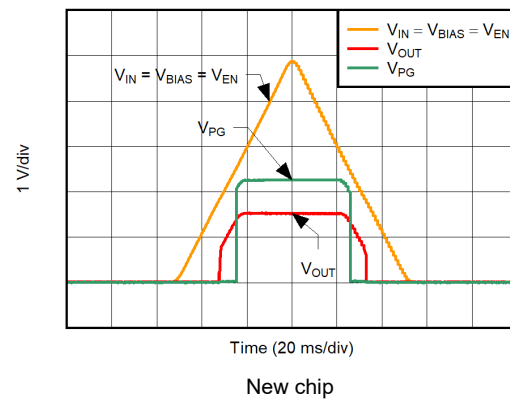


图 5-39. Power-Up and Power-Down

## 6 Detailed Description

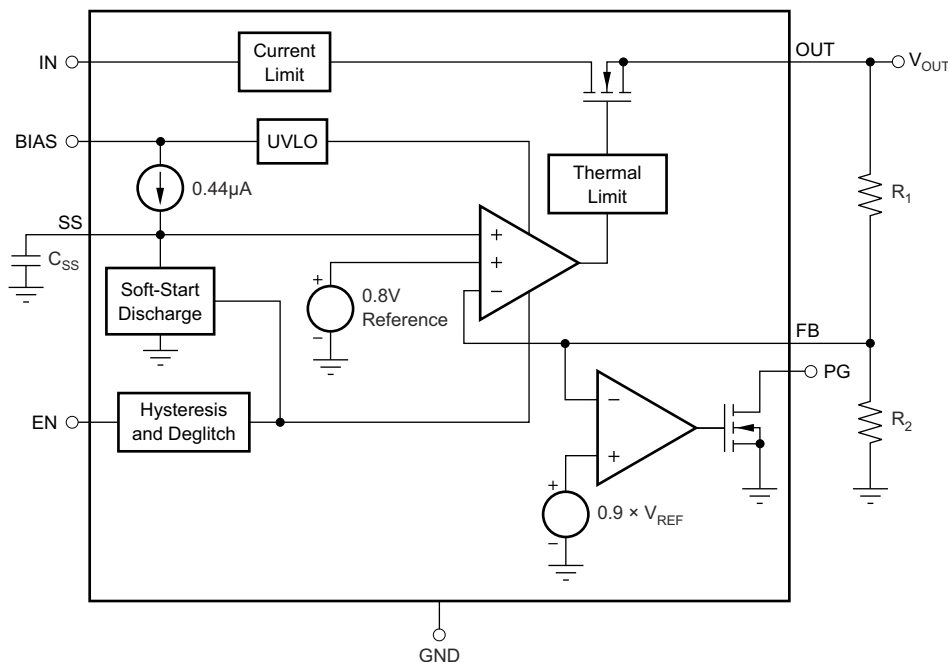
### 6.1 Overview

The TPS74701-Q1 is a low-dropout regulator that features soft-start capability. This regulator use a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74701 to be stable with any capacitor type of value 2.2  $\mu\text{F}$  or greater. Transient response is also superior to PMOS topologies, particularly for low VIN applications.

The TPS74701-Q1 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that may be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low VIN and VOUT capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor-intensive systems.

### 6.2 Functional Block Diagram



### 6.3 Feature Description

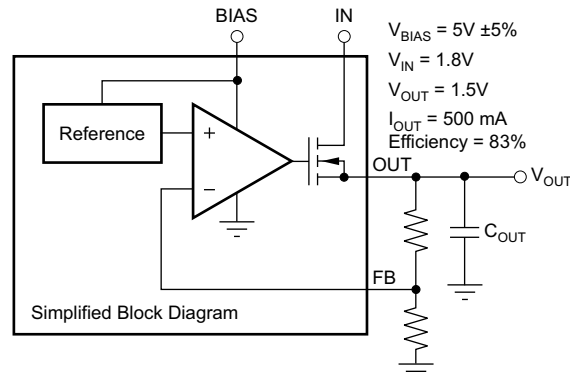
#### 6.3.1 Transient Response

The TPS74701-Q1 is designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response can be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance does. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; see 图 5-34 and 图 5-34. Because the TPS74701-Q1 is stable with output capacitors as low as 2.2  $\mu\text{F}$ , many applications can then need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device can be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

### 6.3.2 Dropout Voltage

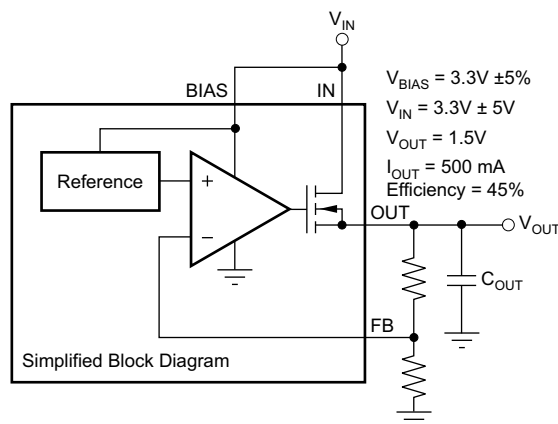
The TPS74701-Q1 offers very low dropout performance, making the device designed for high-current, low  $V_{IN}$ , low  $V_{OUT}$  applications. The low dropout of the TPS74701-Q1 allows the device to be used in place of a DC/DC converter and still achieve good efficiency. This feature provides designers with the power architecture for their applications to achieve the smallest, simplest, and lowest cost solution.

There are two different specifications for dropout voltage with the TPS74701-Q1. The first specification (shown in [图 6-1](#)) is referred to as  $V_{IN}$  dropout and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that  $V_{BIAS}$  is at least 1.62 V above  $V_{OUT}$ , which is the case for  $V_{BIAS}$  when powered by a 3.3-V rail with 5% tolerance and with  $V_{OUT} = 1.5$  V. If  $V_{BIAS}$  is higher than  $V_{OUT} + 1.62$  V,  $V_{IN}$  dropout is less than specified.



**图 6-1. Typical Application of the TPS74701-Q1 Using an Auxiliary Bias Rail**

The second specification (shown in [图 6-2](#)) is referred to as  $V_{BIAS}$  dropout and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because  $V_{BIAS}$  provides the gate drive to the pass transistor; therefore,  $V_{BIAS}$  must be 1.39 V above  $V_{OUT}$  for the legacy chip or 1.3 V for the new chip<sup>1</sup>. Because of this usage, IN and BIAS tied together easily consume huge power. Pay attention not to exceed the power rating of the device package.



**图 6-2. Typical Application of the TPS74701-Q1 Without an Auxiliary Bias Rail**

<sup>1</sup> See the [Device Nomenclature](#) and [Electrical Characteristics](#) for more information regarding the legacy chip and new chip



### 6.3.3 Output Noise

The TPS74701-Q1 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001-μF soft-start capacitor, the output noise is reduced by half and is typically 30 μV<sub>RMS</sub> for a 1.2-V output (10 Hz to 100 kHz) for the legacy chip and 24 μV<sub>RMS</sub> for a 1.2-V output (10 Hz to 100 kHz) with the new chip. Further increasing C<sub>SS</sub> has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 0.001-μF soft-start capacitor is given in the following equations:

$$V_N = 25 \left( \frac{\mu V_{RMS}}{V} \right) \times V_{OUT} (V) \text{ (Legacy Chip)} \quad (1)$$

$$V_N = 20 \left( \frac{\mu V_{RMS}}{V} \right) \times V_{OUT} (V) \text{ (New Chip)} \quad (2)$$

The low output noise of the TPS74701-Q1 makes the device a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

### 6.3.4 Enable and Shutdown

The enable (EN) pin is active high and is compatible with standard digital signaling levels. V<sub>EN</sub> below 0.4 V turns the regulator off, while V<sub>EN</sub> above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the TPS74701-Q1 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on and off cycling as a result of small glitches in the V<sub>EN</sub> signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately – 1 mV/°C; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turn-on timing is required, a fast rise-time signal must be used to enable the TPS74701-Q1.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, connect this pin as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

### 6.3.5 Power Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5 V or lower rail through an external pullup resistor. This pin requires at least 1.1 V on V<sub>BIAS</sub> to have a valid output. The PG output is high-impedance when V<sub>OUT</sub> is greater than V<sub>IT</sub> + V<sub>HYS</sub>. If V<sub>OUT</sub> drops below V<sub>IT</sub> or if V<sub>BIAS</sub> drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of the PG pin sink current is up to 1 mA, so the pullup resistor for PG must be in the range of 10 kΩ to 1 MΩ. If output voltage monitoring is not needed, the PG pin can be left floating.

### 6.3.6 Internal Current Limit

The TPS74701-Q1 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 1 A and maintain regulation. The current limit responds in approximately 10 μs to reduce the current during a short-circuit fault.

The internal current limit protection circuitry of the TPS74701-Q1 is designed to protect against overload conditions. This circuitry is not intended to allow operation above the rated current of the device. Continuously running the TPS74701-Q1 above the rated current degrades device reliability.

### 6.3.7 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heat sinking. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS74701-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS74701-Q1 into thermal shutdown degrades device reliability.

## 6.4 Device Functional Modes

### 6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold
- The output current is less than the current limit
- The device junction temperature is less than the maximum specified junction temperature

### 6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass transistor is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

### 6.4.3 Disabled

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

表 6-1 shows the conditions that lead to the different modes of operation.

表 6-1. Device Functional Mode Comparison

| OPERATING MODE                                | PARAMETER                             |                       |                                         |                    |                           |
|-----------------------------------------------|---------------------------------------|-----------------------|-----------------------------------------|--------------------|---------------------------|
|                                               | $V_{IN}$                              | $V_{EN}$              | $V_{BIAS}$                              | $I_{OUT}$          | $T_J$                     |
| Normal mode                                   | $V_{IN} > V_{OUT(nom)} + V_{DO}(VIN)$ | $V_{EN} > V_{EN, HI}$ | $V_{BIAS} \geq V_{OUT} + 1.39\text{ V}$ | $I_{OUT} < I_{CL}$ | $T_J < 125^\circ\text{C}$ |
| Dropout mode                                  | $V_{IN} < V_{OUT(nom)} + V_{DO}(VIN)$ | $V_{EN} > V_{EN, HI}$ | $V_{BIAS} < V_{OUT} + 1.39\text{ V}$    | —                  | $T_J < 125^\circ\text{C}$ |
| Disabled mode (any true condition the device) | $V_{IN} < V_{IN(min)}$                | $V_{EN} < V_{EN, LO}$ | $V_{BIAS} < V_{BIAS(min)}$              | —                  | $T_J > 165^\circ\text{C}$ |

## 7 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 7.1 Application Information

The TPS74701-Q1 is a 500-mA low-dropout regulator with soft-start function integrated. Based on the end-application, different output voltage could be achieved with different values of external components.

### 7.2 Typical Application

图 7-1 shows the typical application circuit for the TPS74701-Q1 adjustable output device.

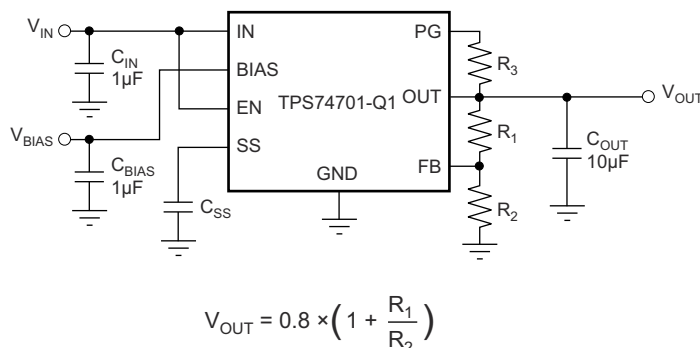


图 7-1. Typical Application Circuit for the TPS74701-Q1

$R_1$  and  $R_2$  can be calculated for any output voltage using the formula shown in 图 7-1. See 表 7-2 for sample resistor values of common output voltages. To achieve the maximum accuracy specifications,  $R_2$  must be less than or equal to 4.99 k $\Omega$ .

#### 7.2.1 Design Requirements

For this design example, use the parameters in 表 7-1.

表 7-1. Design Parameters

| PARAMETER        | EXAMPLE VALUE   |
|------------------|-----------------|
| Input voltage    | 1.8 V $\pm$ 10% |
| Output voltage   | 1.5 V $\pm$ 3%  |
| Enable voltage   | 1.8 V $\pm$ 10% |
| BIAS voltage     | 3.3 V $\pm$ 10% |
| Output current   | 500 mA          |
| Output capacitor | 10 $\mu$ F      |
| Start-up time    | <2 ms           |

#### 7.2.2 Detailed Design Procedure

1. Select  $R_1$  and  $R_2$  based on the required output voltage. 表 7-2 gives example calculations for many common output voltages.
2. Select  $C_{SS}$  to be the highest capacitance while still achieving the desired start-up time. 表 7-3 gives examples of this calculation. 图 7-3 gives examples of turn-on response with different  $C_{SS}$  capacitor value.

3. Select a minimum of a 2.2-μF ceramic output capacitor. Increased output capacitance helps the output load transient response. 图 7-4 gives examples of the load transient response with different output capacitor values and types.

#### 7.2.2.1 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for all available types and values of output capacitors greater than or equal to 2.2 μF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for  $V_{IN}$  and  $V_{BIAS}$  is 1 μF. If  $V_{IN}$  and  $V_{BIAS}$  are connected to the same supply, the recommended minimum capacitor for  $V_{BIAS}$  is 4.7 μF. Good-quality, low-ESR capacitors must be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors must be placed as close the pins as possible for optimum performance.

**表 7-2. Standard 1% Resistor Values for Programming the Output Voltage<sup>(1)</sup>**

| $R_1$ (kΩ) | $R_2$ (kΩ) | $V_{OUT}$ (V) |
|------------|------------|---------------|
| Short      | Open       | 0.8           |
| 0.619      | 4.99       | 0.9           |
| 1.13       | 4.53       | 1             |
| 1.37       | 4.42       | 1.05          |
| 1.87       | 4.99       | 1.1           |
| 2.49       | 4.99       | 1.2           |
| 4.12       | 4.75       | 1.5           |
| 3.57       | 2.87       | 1.8           |
| 3.57       | 1.69       | 2.5           |
| 3.57       | 1.15       | 3.3           |

$$(1) \quad V_{OUT} = 0.8 \times \left( 1 + \frac{R_1}{R_2} \right).$$

**表 7-3. Standard Capacitor Values for Programming the Soft-Start Time<sup>(1)</sup>**

| $C_{SS}$ | SOFT-START TIME (Legacy Chip) | SOFT-START TIME (New Chip) |
|----------|-------------------------------|----------------------------|
| Open     | 0.1 ms                        | 0.25 ms                    |
| 270 pF   | 0.5 ms                        | 0.4 ms                     |
| 560 pF   | 1 ms                          | 0.8 ms                     |
| 2.7 nF   | 5 ms                          | 4.1 ms                     |
| 5.6 nF   | 10 ms                         | 8.5 ms                     |
| 0.01 μF  | 18 ms                         | 15 ms                      |

$$(1) \quad t_{SS}(s) = \frac{0.8 \times C_{SS}(F)}{I_{SS}(A)}$$

#### 7.2.2.2 Programmable Soft-Start

The TPS74701-Q1 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ( $C_{SS}$ ). This feature is important for many applications because this capacitor eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft start, the TPS74701-Q1 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current ( $I_{SS}$ ), soft-start capacitance ( $C_{SS}$ ), and the internal reference voltage ( $V_{REF}$ ), and can be calculated using 方程式 3:

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \quad (3)$$

If large output capacitors are used, the device current limit ( $I_{CL}$ ) and the output capacitor can set the start-up time. In this case, the start-up time is given by 方程式 4:

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}} \quad (4)$$

where:

- $V_{OUT(NOM)}$  is the nominal output voltage
- $C_{OUT}$  is the output capacitance
- $I_{CL(MIN)}$  is the minimum current limit for the device

In applications where monotonic start-up is required, the soft-start time given by 方程式 3 must be set greater than 方程式 4.

The maximum recommended soft-start capacitor is 0.015  $\mu$ F. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit can possibly be unable to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 0.015  $\mu$ F can be a problem in applications where the enable pin must be rapidly pulsed and still require the device to soft-start from ground.  $C_{SS}$  must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. See 表 7-3 for suggested soft-start capacitor values.

### 7.2.2.3 Sequencing Requirements

$V_{IN}$ ,  $V_{BIAS}$ , and  $V_{EN}$  can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications, as long as  $V_{IN}$  is greater than 1.1 V and the ramp rate of  $V_{IN}$  and  $V_{BIAS}$  is faster than the set soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until reaching the set output voltage. If EN is connected to BIAS, the device soft-starts as programmed, provided that  $V_{IN}$  is present before  $V_{BIAS}$ . If  $V_{BIAS}$  and  $V_{EN}$  are present before  $V_{IN}$  is applied and the set soft-start time has expired, then  $V_{OUT}$  tracks  $V_{IN}$ . If the soft-start time has not expired, the output tracks  $V_{IN}$  until  $V_{OUT}$  reaches the value set by the charging soft-start capacitor. 图 7-2 shows the use of an RC delay circuit to hold off  $V_{EN}$  until  $V_{BIAS}$  has ramped. This technique can also be used to drive EN from  $V_{IN}$ . An external control signal can also be used to enable the device after  $V_{IN}$  and  $V_{BIAS}$  are present.

#### 备注

When  $V_{BIAS}$  and  $V_{EN}$  are present and  $V_{IN}$  is not supplied, this device outputs approximately 50  $\mu$ A of current from OUT. Although this condition does not cause any damage to the device, the output current can charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 k $\Omega$ .

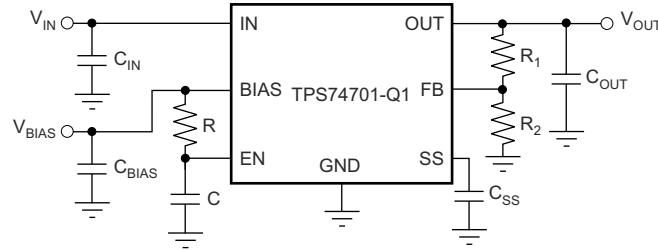


图 7-2. Soft-Start Delay Using an RC Circuit to Enable the Device

### 7.2.3 Application Curves

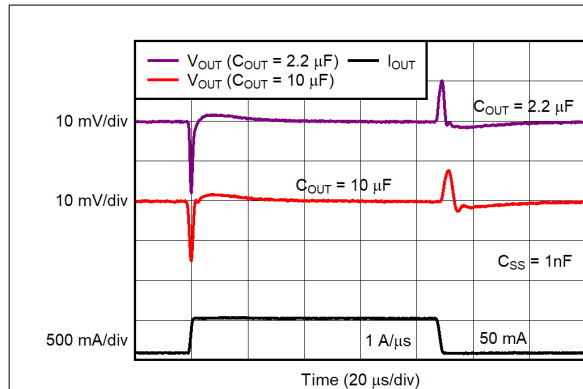


图 7-3. Output Load Transient Response

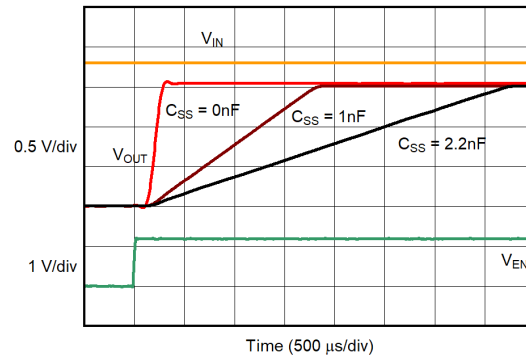


图 7-4. Turn-On Response

## 7.3 Power Supply Recommendations

The TPS74701-Q1 is designed to operate from an input voltage up to 5.5 V, provided the bias rail is at least 1.39 V higher than the input supply and dropout requirements are met. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally.

Connect a low-output impedance power supply directly to the IN pin of the TPS74701. This supply must have at least 1  $\mu\text{F}$  of capacitance near the IN pin for optimal performance. A supply with similar requirements must also be connected directly to the bias rail with a separate 1  $\mu\text{F}$  or larger capacitor. If the IN pin is tied to the bias pin, a minimum 4.7  $\mu\text{F}$  of capacitance is needed for performance. To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

## 7.4 Layout

### 7.4.1 Layout Guidelines

#### 7.4.1.1 Layout Recommendations and Power Dissipation

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS must be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can, therefore, improve stability. To achieve optimal transient performance and accuracy, the top side of  $R_1$  in 图 7-1 must be connected as close as possible to the load. If BIAS is connected to IN, connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and to provide reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated using 方程式 5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

The primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, the pad must be attached to an appropriate amount of copper PCB area to make sure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using [方程式 6](#):

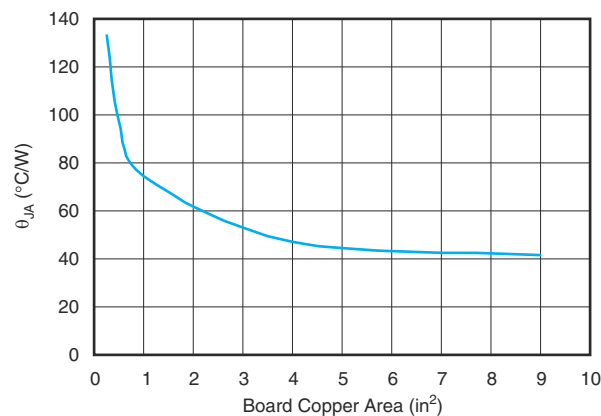
$$R_{\theta JA} = \frac{(150^{\circ}\text{C} - T_A)}{P_D} \quad (6)$$

Knowing the maximum  $R_{\theta JA}$ , the minimum amount of PCB copper area needed for appropriate heat sinking can be estimated using [图 7-5](#).

[图 7-5](#) shows the variation of  $R_{\theta JA}$  as a function of ground plane copper area in the board. This figure is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and is not intended to be used to estimate actual thermal performance in real application environments.

#### 备注

When the device is mounted on an application PCB, use  $\Psi_{JT}$  and  $\Psi_{JB}$ , as explained in the [Estimating Junction Temperature](#) section.



$R_{\theta JA}$  value at board size of 9 in<sup>2</sup> (that is, 3-in × 3-in) is a JEDEC standard.

**图 7-5.  $R_{\theta JA}$  vs Board Size**

#### 7.4.1.2 Estimating Junction Temperature

Using the thermal metrics  $\Psi_{JT}$  and  $\Psi_{JB}$ , as shown in the [Thermal Information](#) table, the junction temperature can be estimated with corresponding formulas (given in [方程式 7](#)). For backwards compatibility, an older  $R_{\theta JC, Top}$  parameter is listed as well.

$$\begin{aligned} \Psi_{JT}: T_J &= T_T + \Psi_{JT} \cdot P_D \\ \Psi_{JB}: T_J &= T_B + \Psi_{JB} \cdot P_D \end{aligned} \quad (7)$$

Where  $P_D$  is the power dissipation shown by 方程式 7,  $T_T$  is the temperature at the center-top of the device package, and  $T_B$  is the PCB temperature measured 1 mm away from the device package *on the PCB surface* (see 图 7-7).

#### 备注

Both  $T_T$  and  $T_B$  can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring  $T_T$  and  $T_B$ , see the [Using New Thermal Metrics application note](#), available for download at [www.ti.com](http://www.ti.com).

In reference to 图 7-6, the new thermal metrics ( $\Psi_{JT}$  and  $\Psi_{JB}$ ) have very little dependency on board size. That is, using  $\Psi_{JT}$  or  $\Psi_{JB}$  with 方程式 7 is a good way to estimate  $T_J$  by simply measuring  $T_T$  or  $T_B$ , regardless of the application board size.

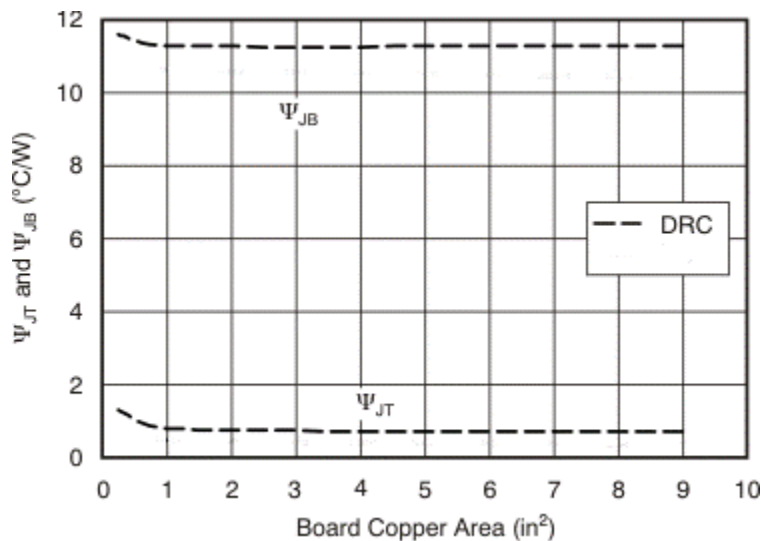
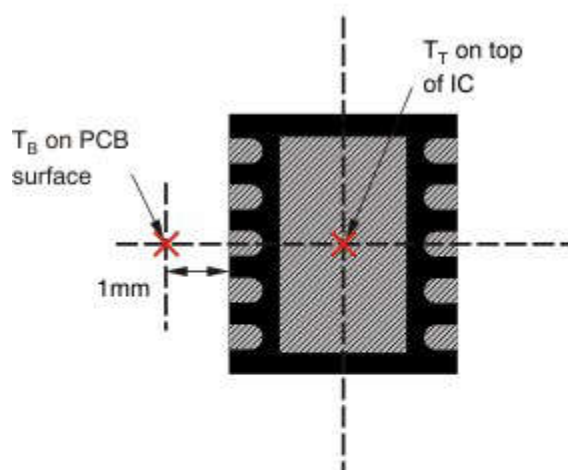


图 7-6.  $\Psi_{JT}$  and  $\Psi_{JB}$  vs Board Size

For a more detailed discussion of why TI does not recommend using  $R_{\theta JC(top)}$  to determine thermal characteristics, see the [Using New Thermal Metrics application note](#), available for download at [www.ti.com](http://www.ti.com). For further information, see the [Semiconductor and IC Package Thermal Metrics application note](#), also available on the TI website.



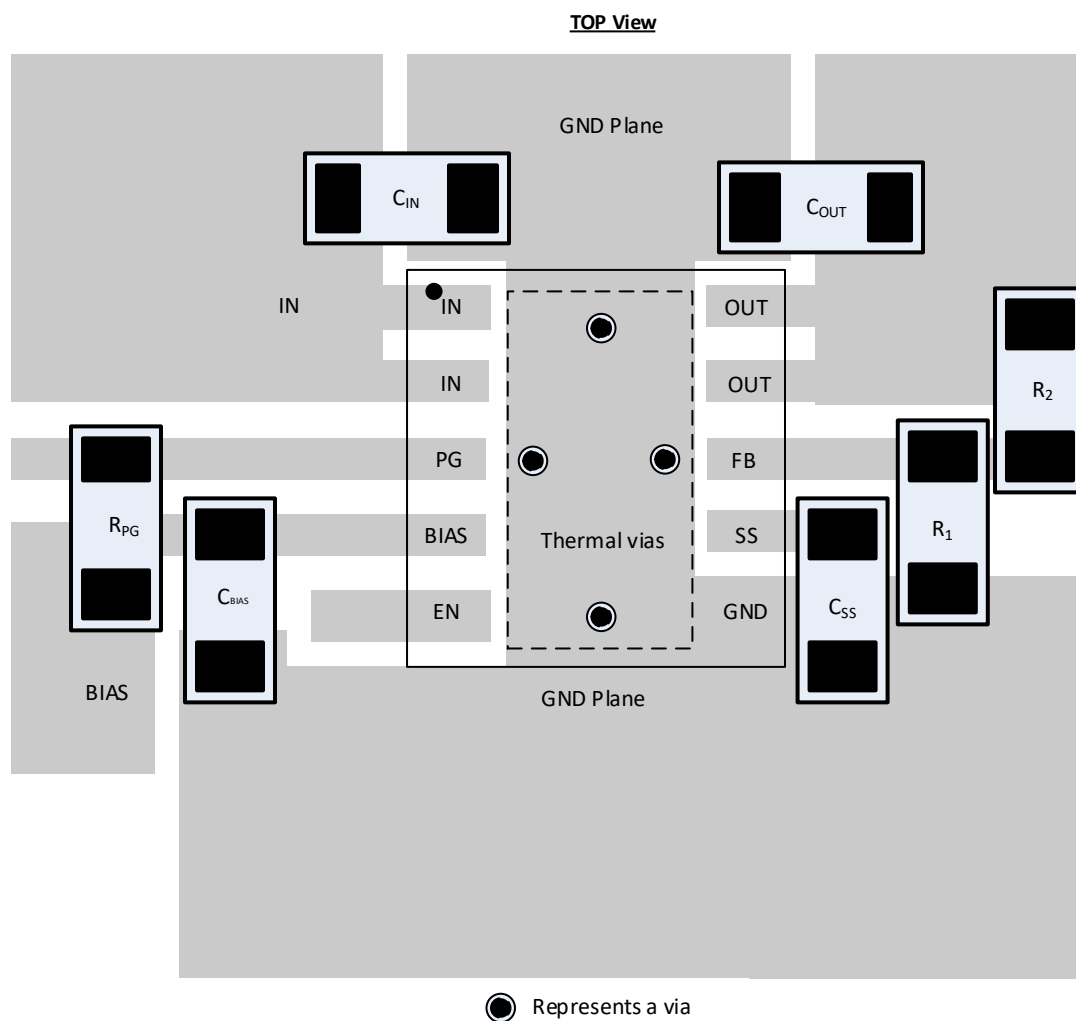


**(a) Example DRC (SON) Package Measurement**

- A.  $T_T$  is measured at the center of both the X- and Y-dimensional axes.
- B.  $T_B$  is measured *below* the package lead on the PCB surface.

**图 7-7. Measuring Points for  $T_T$  and  $T_B$**

## 7.4.2 Layout Example



**图 7-8. Layout Example: DRC Package**

## 8 Device and Documentation Support

### 8.1 Device Support

#### 8.1.1 Development Support

For development support, see the following:

- Texas Instruments, [TPS74801-Q1 1.5 A Low-Dropout Linear Regulator with Programmable Soft-Start data sheet](#)
- Texas Instruments, [TI PCB Thermal Calculator](#)

#### 8.1.2 Device Nomenclature

表 8-1. Device Nomenclature

| PRODUCT <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TPS74701QyyyzM3Q1      | <p><b>Q</b> indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard.</p> <p><b>yyy</b> is the package designator.</p> <p><b>z</b> is the package quantity.</p> <p><b>M3</b> is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix can ship with the legacy chip (CSO: DLN) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is used. Device performance for new and legacy chips is denoted throughout the document.</p> <p><b>Q1</b> indicates that this device is an automotive grade (AEC-Q100) device.</p> |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on [www.ti.com](http://www.ti.com).

### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 8.4 Trademarks

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### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision C (October 2023) to Revision D (December 2023)                                                                                                        | Page |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • 通篇添加了器件措辞以区分旧芯片和新芯片信息.....                                                                                                                                                | 1    |
| • 更新了导通响应图以显示新芯片性能.....                                                                                                                                                     | 1    |
| • Changed <i>Typical Characteristics</i> sections to show legacy chip and new chip data side by side and deleted $V_{IN}$ Dropout Voltage vs $V_{BIAS}-V_{OUT}$ curves..... | 8    |
| • Added soft-start time for new chip in <i>Standard Capacitor Values for Programming the Soft-Start Time</i> table.....                                                     | 20   |
| • Changed <i>Device Nomenclature</i> section.....                                                                                                                           | 27   |

| Changes from Revision B (September 2016) to Revision C (October 2023)                                                              | Page |
|------------------------------------------------------------------------------------------------------------------------------------|------|
| • 更新了整个文档中的表格、图和交叉参考的编号格式.....                                                                                                     | 1    |
| • 向文档添加了 M3 器件.....                                                                                                                | 1    |
| • 更改了特定于汽车的特性要点.....                                                                                                               | 1    |
| • 更改了 $V_{IN}$ 范围、低压降、精度和封装 特性要点：删除了 $V_{IN}$ 范围要点中的超低，将低压降要点中的“50mV”更改为“20mV”，将精度要点中的“2%”更改为“0.95%”，并删除了封装要点中的 $\times 1mm$ ..... | 1    |
| • 更改了应用 部分.....                                                                                                                    | 1    |
| • 更改了说明 部分.....                                                                                                                    | 1    |
| • Changed <i>Description</i> column of <i>Pin Functions</i> table.....                                                             | 3    |
| • Changed <i>Typical Characteristics</i> and added new <i>Typical Characteristics</i> sections.....                                | 8    |
| • Changed footnote for <i>Standard Capacitor Values for Programming the Soft-Start Time</i> table.....                             | 20   |
| • Changed <i>Layout</i> section.....                                                                                               | 22   |
| • Added <i>Device Nomenclature</i> section.....                                                                                    | 27   |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS74701QDRCRM3Q1</a> | Active        | Production           | VSON (DRC)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 150   | PAE                 |
| TPS74701QDRCRM3Q1.A               | Active        | Production           | VSON (DRC)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 150   | PAE                 |
| <a href="#">TPS74701QDRCRQ1</a>   | Active        | Production           | VSON (DRC)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | PAE                 |
| TPS74701QDRCRQ1.A                 | Active        | Production           | VSON (DRC)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 150   | PAE                 |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS74701-Q1 :**

- Catalog : [TPS74701](#)

NOTE: Qualified Version Definitions:

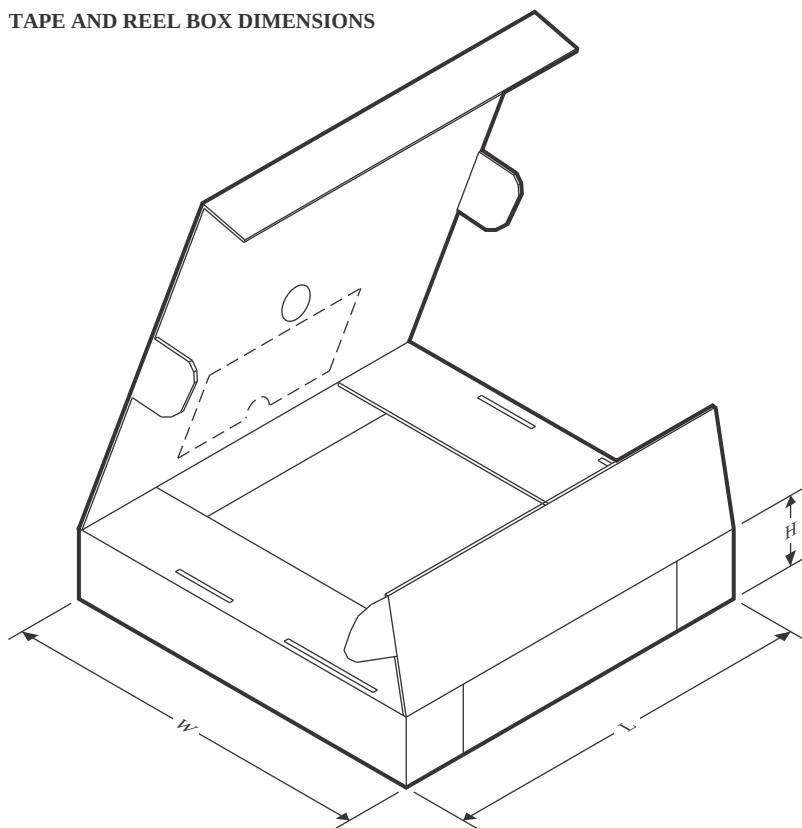
- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS74701QDRCRM3Q1 | VSON         | DRC             | 10   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS74701QDRCRQ1   | VSON         | DRC             | 10   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS74701QDRCRM3Q1 | VSON         | DRC             | 10   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS74701QDRCRQ1   | VSON         | DRC             | 10   | 3000 | 367.0       | 367.0      | 35.0        |



## GENERIC PACKAGE VIEW

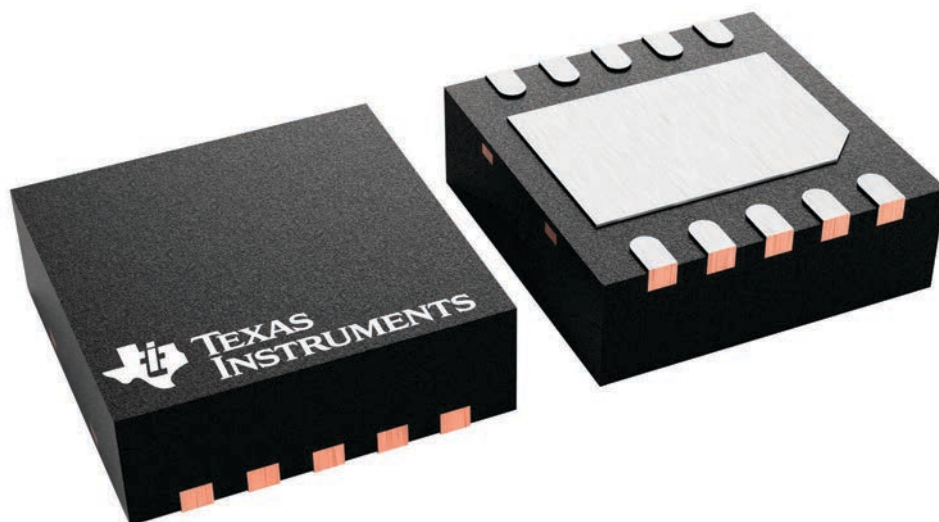
**DRC 10**

**VSON - 1 mm max height**

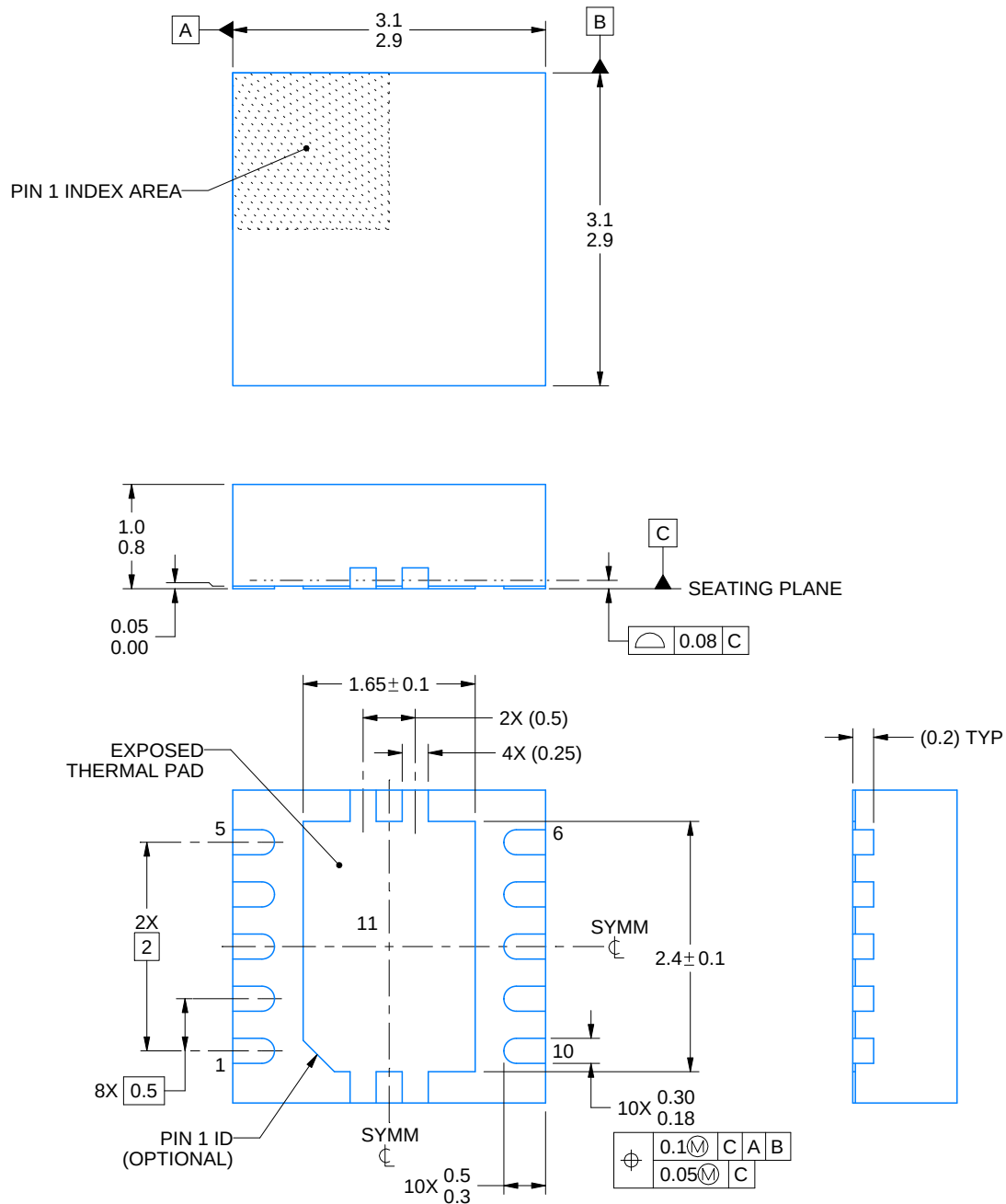
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



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## NOTES:

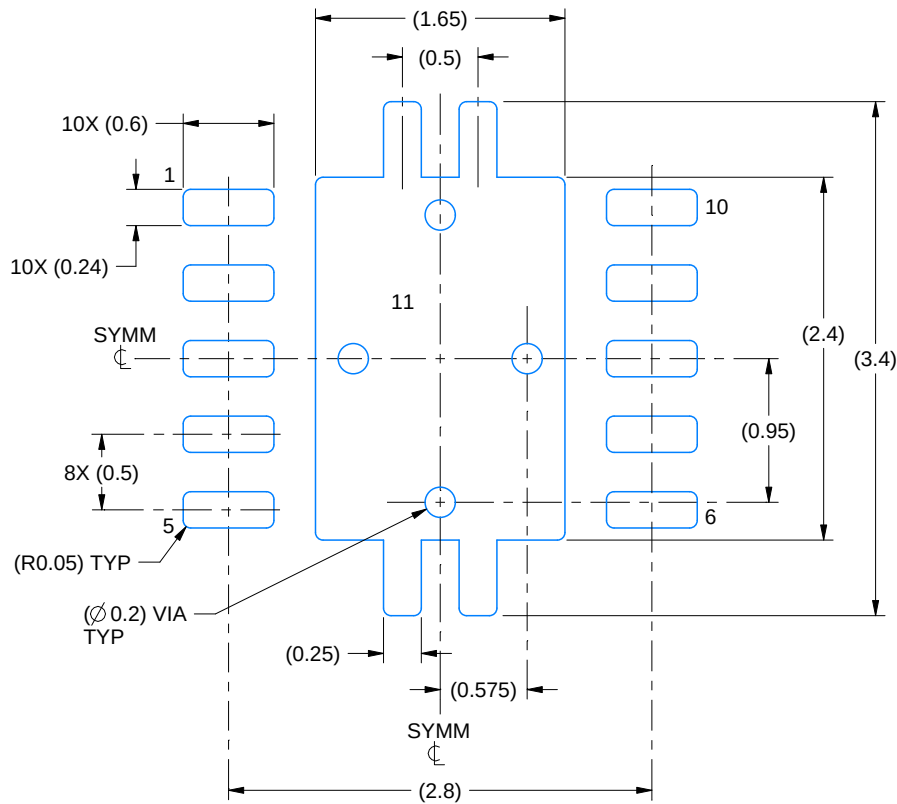
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

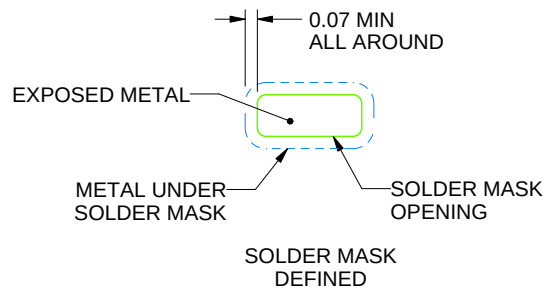
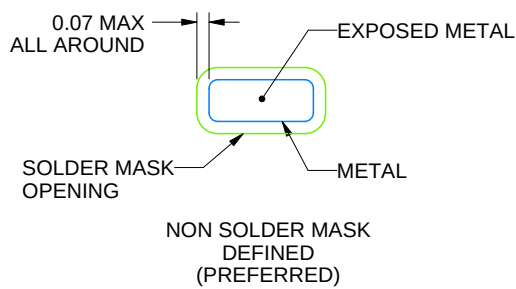
DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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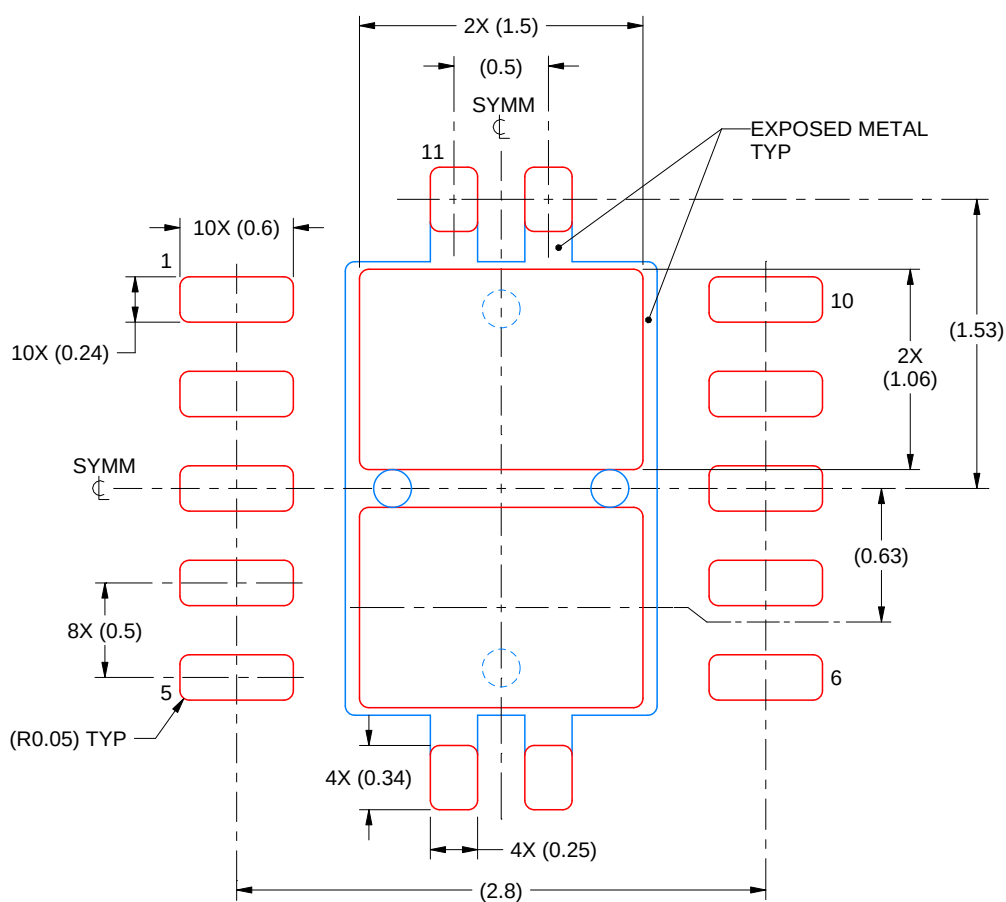
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**DRC0010J**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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