具有电源正常状态指示功能且采用小型封装的 TPS745 500mA 高精度可调节 LDO

1 特性

- 输入电压范围：1.5V 至 6.0V
- 可调节输出电压：
  - 0.55V 至 5.5V
- 极低压降：
  - 500mA 时为 130mV（最大值）($3.3V_{OUT}$)
- 高输出精度：0.7%（典型值）和 1%（过温条件下的最大值）
- 开漏电源正常状态输出
- I_Q：25µA（典型值）
- 内置软启动功能，具有单调 V_{OUT} 上升
- 封装：
  - 2mm × 2mm WSON-6 (DRV)
- 有源输出放电

2 应用

- 机顶盒和游戏机
- 家庭影院和娱乐
- 台式机、笔记本电脑、超极本
- 打印机
- 服务器
- 恒温器和照明控制
- 电子销售点 (EPOS)

3 说明

TPS745 是一款具有电源状态良好指示功能的可调 500A 低压降 (LDO) 稳压器。该器件采用小型 6 引脚 2mm × 2mm WSON 封装并具有极低的静态电流，可提供快速的线路和负载瞬态性能。TPS745 具有 130mV 的超低压降（500mA 电流情况下），这有助于提高系统的功效。

TPS745 针对各种 应用 进行了优化：支持 1.5V 至 6.0V 的输入电压范围以及 0.55V 至 5.5V 的外部可调输出范围。这种低输出电压使得该 LDO 能够为具有较低内核电压的现代微控制供电。

TPS745 具有监测反馈引脚电压的电源正常状态 (PG) 输出，用于指示输出电压的状态。EN 输入和 PG 输出可用于对系统中的多个电源进行定序。

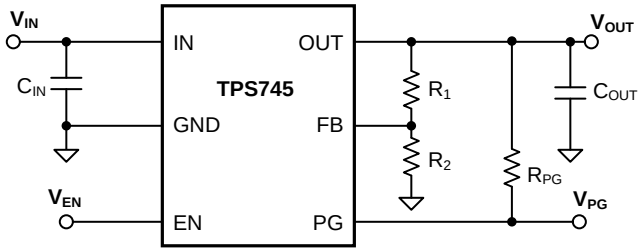
TPS745 在与支持小尺寸总体解决方案的小型陶瓷输出电容器搭配使用时，可保持稳定。一个精密带隙和误差放大器具有高精度特性，在 25°C 时提供 0.7%（最大值）的精度，在过温 (85ºC) 条件下提供 1%（最大值）的精度。该器件包括集成的热关断、电流限制和欠压锁定 (UVLO) 功能的刷式直流电机。TPS745 包含一个内部折返电流限制，有助于在短路事件中减少热耗散。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS745	WSON (6)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用



目录

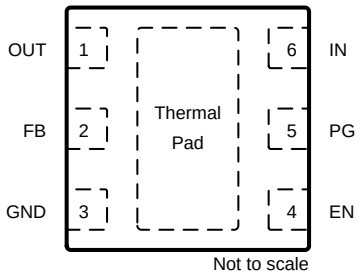
4 修订历史记录

Changes from Original (April 2018) to Revision A **Page**

- 已更改 文档状态从“预告信息”改为“生产数据” 1

5 Pin Configuration and Functions

DRV Package
6-Pin Adjustable WSON
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	4	Input	Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the LDO into shutdown mode.
FB	2	—	This pin is used as an input to the control loop error amplifier and is used to set the output voltage of the LDO.
GND	3	—	Ground pin
IN	6	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the input capacitor as close to the output of the device as possible.
OUT	1	Output	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the output capacitor as close to output of the device as possible.
PG	5	Output	Power-good output
Thermal pad	Pad	—	Connect the thermal pad to a large area GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, V_{IN}	–0.3	6.5	V
	Enable, V_{EN}	–0.3	6.5	
	Feedback, V_{FB}	–0.3	2	
	Power-good, V_{PG}	–0.3	6.5	
	Output, V_{OUT}	–0.3	V_{IN} + 0.3(2)	
Current	Power-good current		±10	mA
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3V or 6.5 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM ispossible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM ispossible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.5		6.0	V
V_{OUT}	Output voltage	0.55		5.5	V
I_{OUT}	Output current	0		500	mA
C_{IN}	Input capacitor	1			µF
C_{OUT}	Output capacitor(1)	1		220	µF
V_{EN}	Enable voltage	0		6.0	V
f_{EN}	Enable toggle frequency			10	kHz
V_{PG}	PG voltage	0		6.0	V
T_J	Junction temperature	–40		125	°C

(1) Minimum derated capacitance of 0.47 µF is required for stability

6.4 Thermal Information

THERMAL METRIC[1]		TPS745 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	20.8	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.

6.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to +125°C),V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever isgreater), I_{OUT} = 1 mA, V_{EN} =V_{IN}, and C_{IN} = C_{OUT} = 1 uF(unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage	T_J = 25°C			0.55		V
	Output accuracy[1]	T_J = 25°C		–0.7%		0.7%	
		–40°C ≤ T_J ≤ +85°C		–1%		1%	
		–40°C ≤ T_J ≤ +125°C		–1.5%		1.5%	
	Line regulation	$V_{OUT(NOM)}$ + 0.5 V[2] ≤ $V_{I N}$ ≤ 6.0 V			2	7.5	mV
	Load regulation	0.1 mA ≤ I_{OUT} ≤ 500 mA, V_{IN} ≥ 2.0 V			0.030		V/A
I_{GND}	Ground current	I_{OUT} = 0 mA	T_J = 25°C	10	25	31	µA
I_{GND}	Ground current		–40°C ≤ T_J ≤ +125°C			35	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.3 V, 1.5 V ≤ V_{IN} ≤ 6.0 V			0.1	1	µA
I_{FB}	Feedback pin current				0.01	0.1	µA
I_{CL}	Output current limit	V_{IN} = $V_{OUT(NOM)}$ + 1.0 V	V_{OUT} = $V_{OUT(NOM)}$ – 0.2 V, V_{OUT} < 1.5 V	530	720	865	mA
			V_{OUT} = 0.9 V × $V_{OUT(NOM)}$, V_{OUT} ≥ 1.5 V	530	720	865	
I_{SC}	Short-circuit current limit	V_{IN} = $V_{OUT(NOM)}$ + 1.0 V	V_{OUT} = 0 V		350		mA
V_{DO}	Dropout voltage	I_{OUT} = 500 mA, –40°C ≤ T_J ≤ +125°C, V_{OUT} = 0.95 × $V_{OUT(NOM)}$	0.65 V ≤ V_{OUT} < 0.8 V		720	880	mV
			0.8 V ≤ V_{OUT} < 1.0 V		585	750	
			1.0 V ≤ V_{OUT} < 1.2 V		420	570	
			1.2 V ≤ V_{OUT} < 1.5 V		285	400	
			1.5 V ≤ V_{OUT} < 1.8 V		180	235	
			1.8 V ≤ V_{OUT} < 2.5 V		140	185	
			2.5 V ≤ V_{OUT} < 3.3 V		102	140	
			3.3 V ≤ V_{OUT} ≤ 5.5 V		95	130	
PSRR	Power-supply rejection ratio	V_{IN} = $V_{OUT(NOM)}$ + 1.0 V, I_{OUT} = 50 mA	f = 1 kHz		50		dB
			f = 100 kHz		45		
			f = 1 MHz		30		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 0.9 V			53		μV_{RMS}
V_{UVLO}	Undervoltage lockout	V_{IN} rising		1.21	1.33	1.47	V
		V_{IN} falling		1.17	1.29	1.42	V
$V_{UVLO, HYST}$	Undervoltage lockout hysteresis	V_{IN} Hysteresis			40		mV
t_{STR}	Startup time	From EN low-to-high transition to V_{OUT} = $V_{OUT(NOM)}$ × 95%			500		µs

(1) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included
(2) V_{IN} = 1.5V for V_{OUT} < 1.0 V

Electrical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C),V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever isgreater), I_{OUT} = 1 mA, V_{EN} =V_{IN}, and C_{IN} = C_{OUT} = 1 uF(unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{EN(HI)}$	EN pin high voltage		1.0			V
$V_{EN(LO)}$	EN pin low voltage				0.3	V
I_{EN}	Enable pin current	V_{IN} = EN = 6.0 V		10		nA
$R_{PULL\ DOWN}$	Pulldown resistance	V_{IN} = 6.0 V		95		Ω
PG_{HTH}	PG high threshold	V_{OUT} increasing	89	94	95	%V_{OUT}
PG_{LTH}	PG low threshold	V_{OUT} decreasing	87	92	93	%V_{OUT}
$V_{OL(PG)}$	PG pin low-level output voltage	V_{IN} ≥ 1.5 V, I_{SINK} = 1 mA			300	mV
$V_{OL(PG)}$	PG pin low-level output voltage	V_{IN} ≥ 2.75 V, I_{SINK} = 2 mA			300	
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > PG_{HTH}, V_{PG} = 6.0 V			300	nA
T_{SD}	Thermal shutdown	Shutdown, temperature increasing		170		°C
		Reset, temperature decreasing		155		

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{PGDH}	PG delay time rising(1)	Time from 92% VOUT to 20% of PG	135	165	178	µs
t_{PGDL}	PG delay time falling(1)	Time from 90% V_{OUT} to 80% of PG	1.5	7	10	µs

(1) Output overdrive = 10%

6.7 Typical Characteristics

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

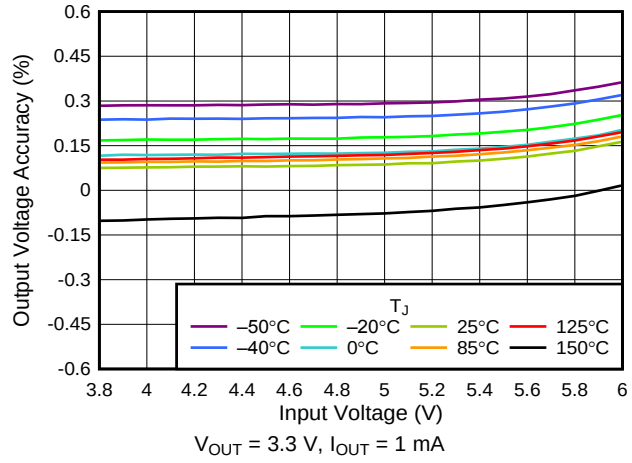


图 1. 3.3-V Line Regulation vs V_{IN}

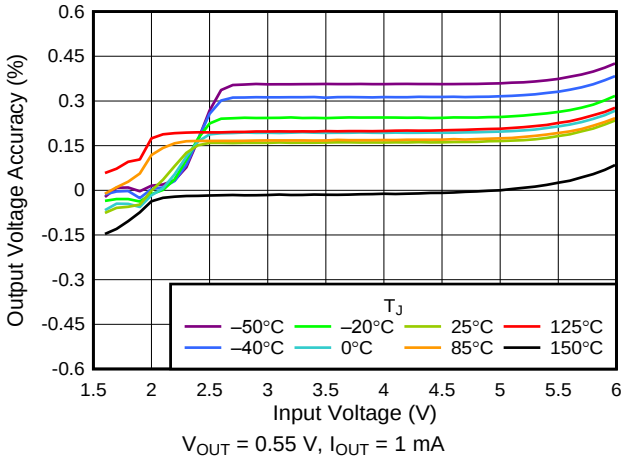


图 2. 0.55-V Line Regulation vs V_{IN}

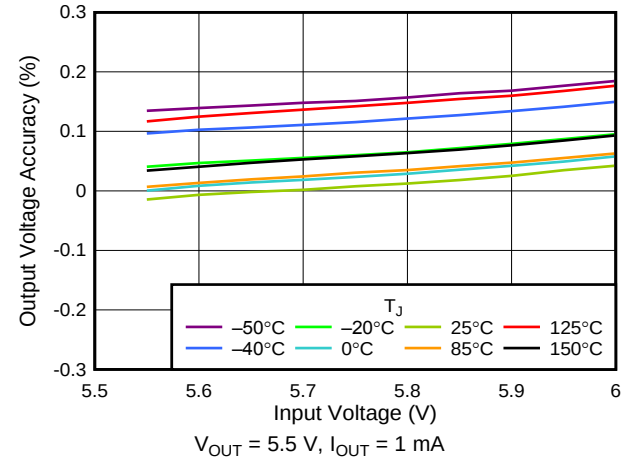


图 3. 5.5-V Line Regulation vs V_{IN}

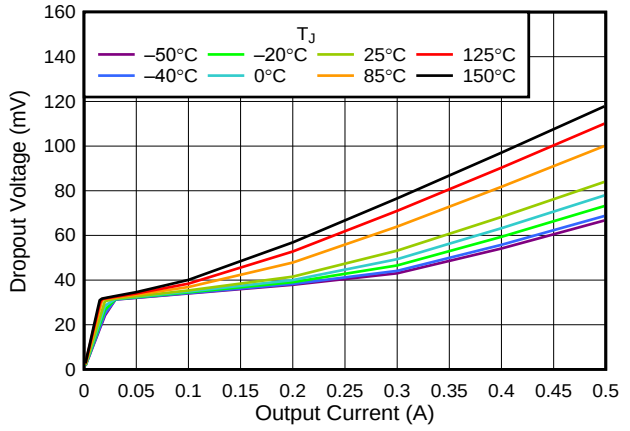


图 4. 3.3-V Dropout Voltage vs I_{OUT}

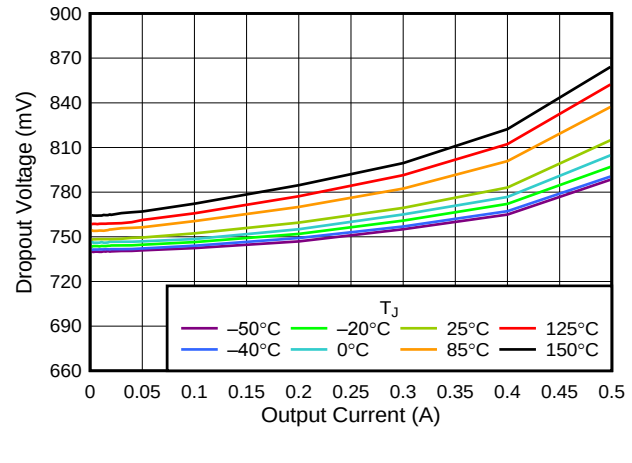


图 5. 0.55-V Dropout Voltage vs I_{OUT}

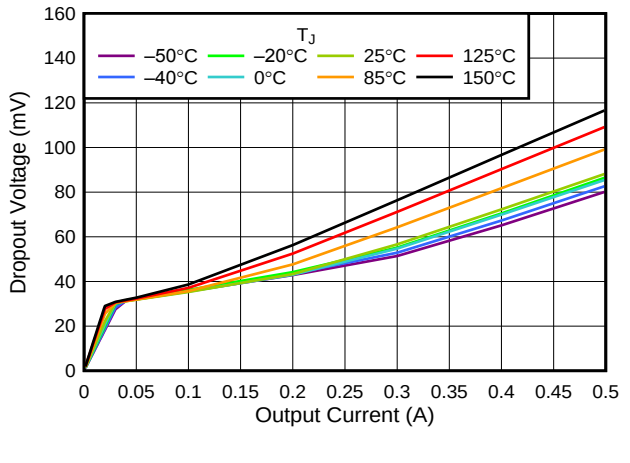
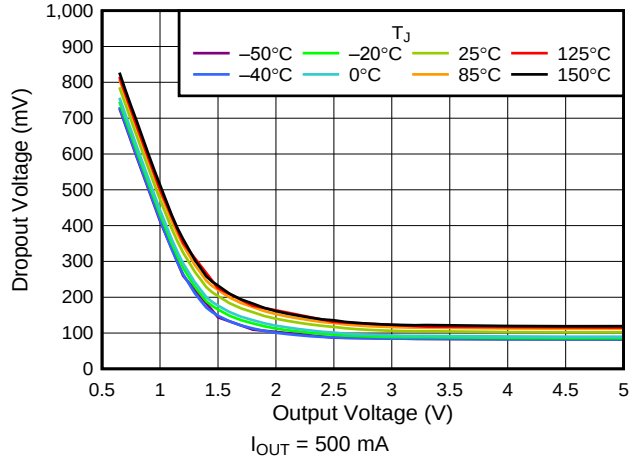


图 6. 5.5-V Dropout Voltage vs I_{OUT}

Typical Characteristics (接下页)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



I_{OUT} = 500 mA

图 7. V_{DO} vs V_{OUT}

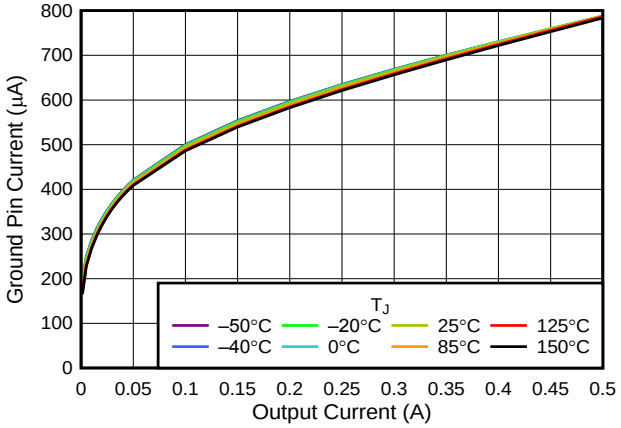
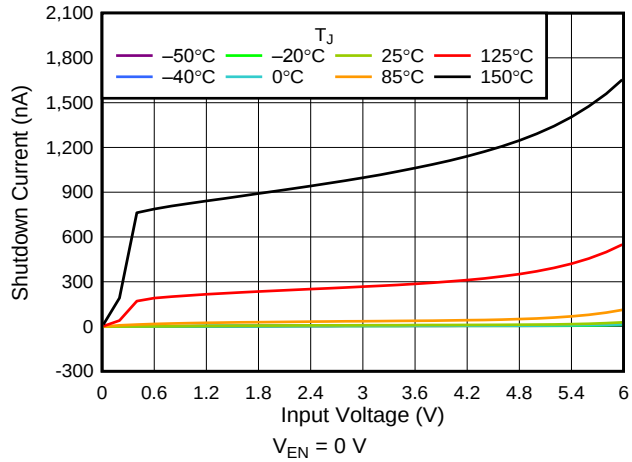
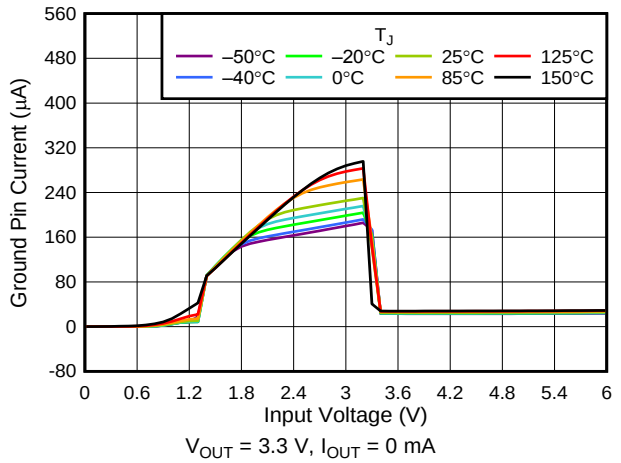


图 8. I_{GND} vs I_{OUT}



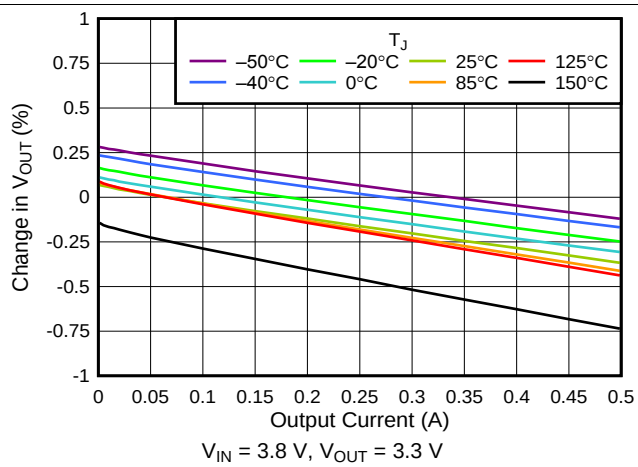
V_{EN} = 0 V

图 9. I_{SHDN} vs V_{IN}



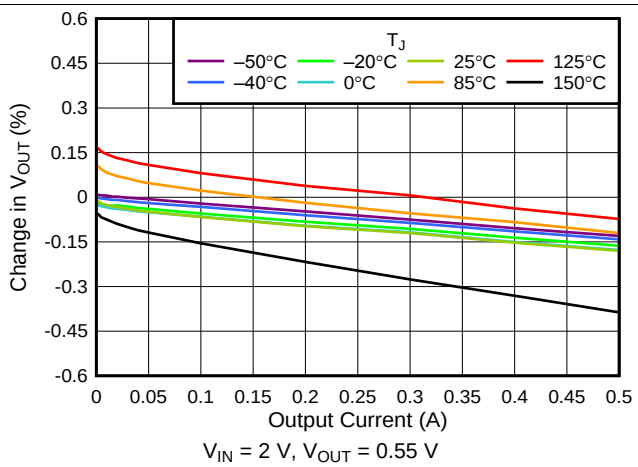
V_{OUT} = 3.3 V, I_{OUT} = 0 mA

图 10. I_Q vs V_{IN}



V_{IN} = 3.8 V, V_{OUT} = 3.3 V

图 11. 3.3-V Load Regulation vs I_{OUT}



V_{IN} = 2 V, V_{OUT} = 0.55 V

图 12. 0.55-V Load Regulation vs I_{OUT}

Typical Characteristics (接下页)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

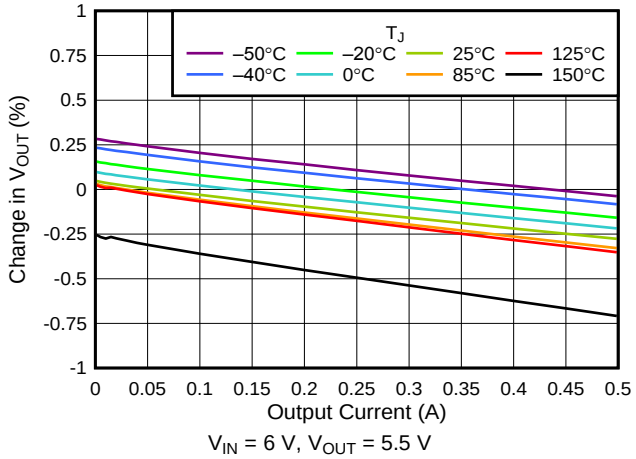


图 13. 5-V Load Regulation vs I_{OUT}

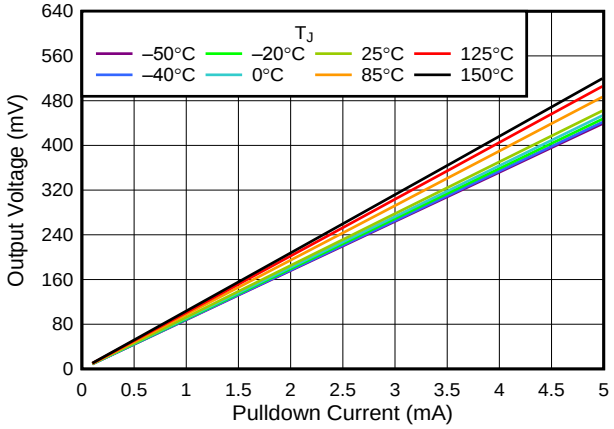


图 14. V_{OUT} vs I_{OUT} Pulldown Resistor

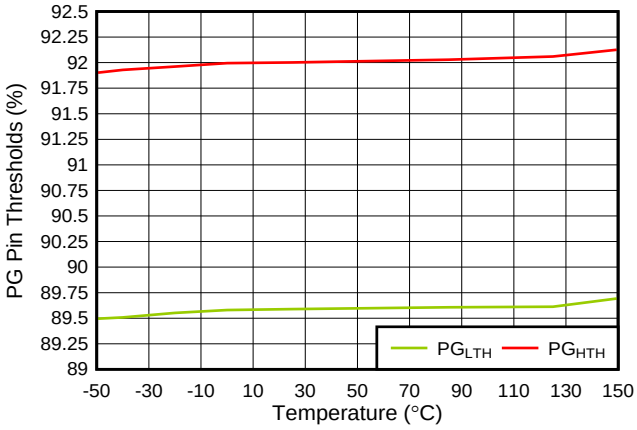


图 15. PG_{LTH} and PG_{HTH} vs Temperature

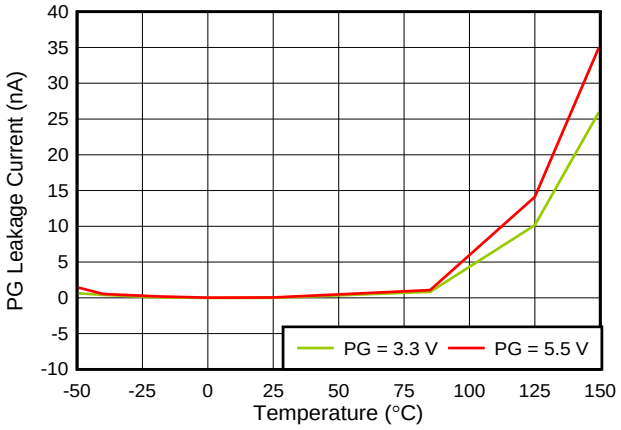


图 16. $I_{lkg(PG)}$ vs Temperature and PG Pin Voltage

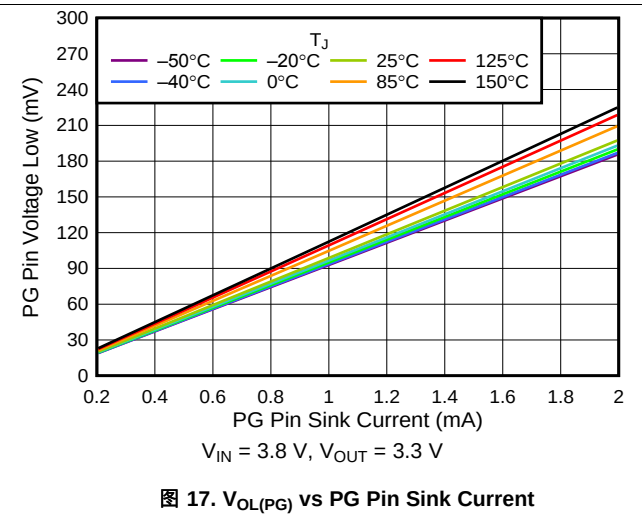


图 17. $V_{OL(PG)}$ vs PG Pin Sink Current

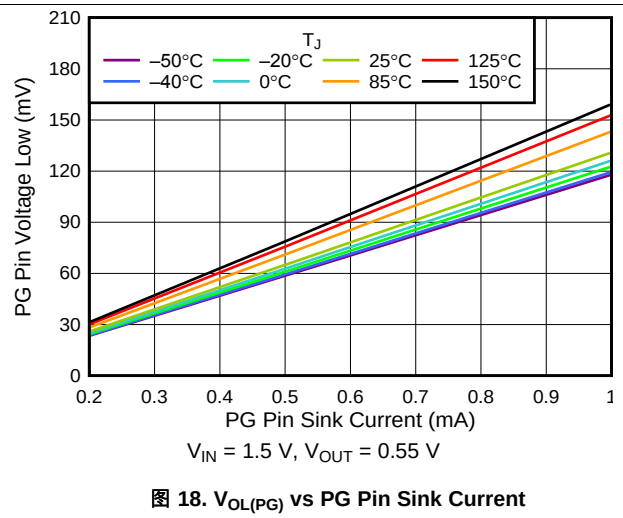


图 18. $V_{OL(PG)}$ vs PG Pin Sink Current

Typical Characteristics (接下页)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

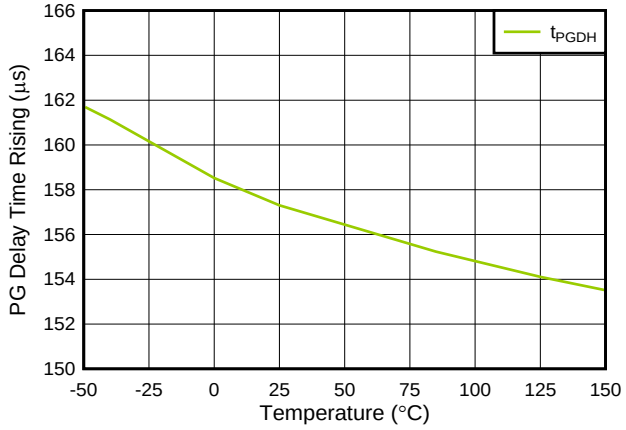


图 19. t_{PGDH} vs Temperature

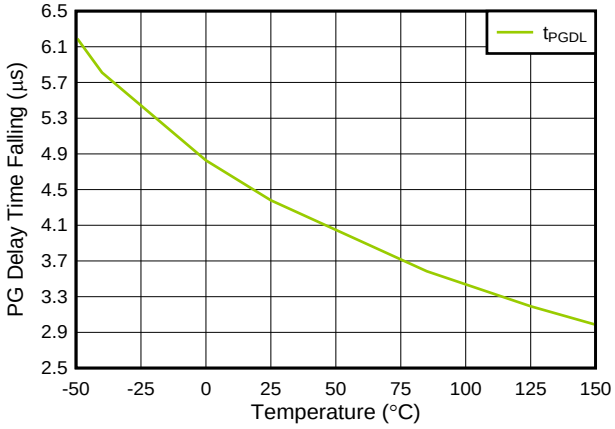


图 20. t_{PGDL} vs Temperature

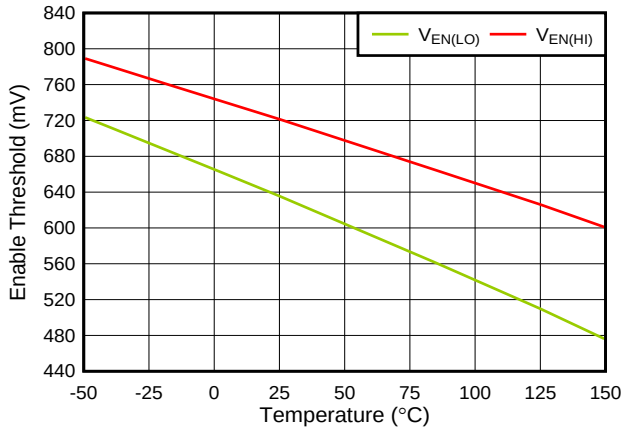


图 21. $V_{EN(HI)}$ and $V_{EN(LO)}$ vs Temperature

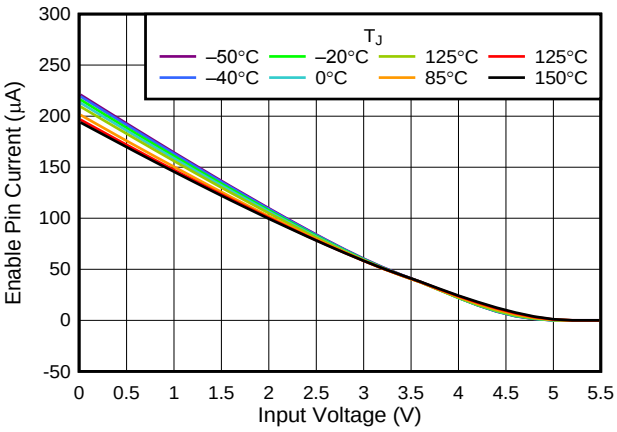


图 22. I_{EN} vs V_{IN}

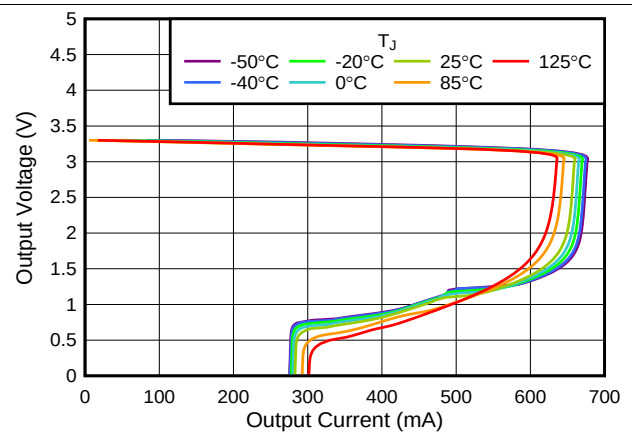


图 23. 3.3-V Foldback Current Limit vs I_{OUT}

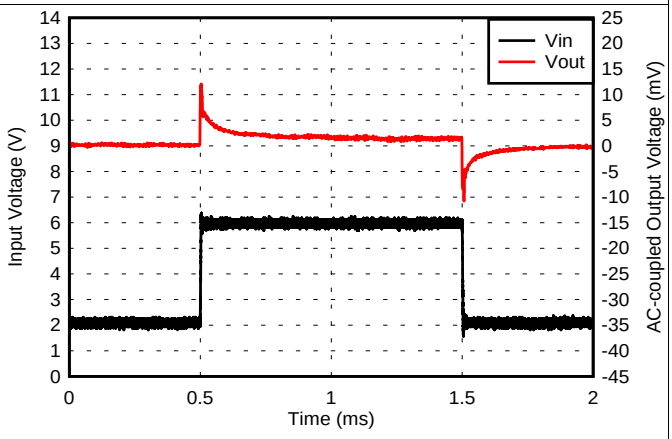
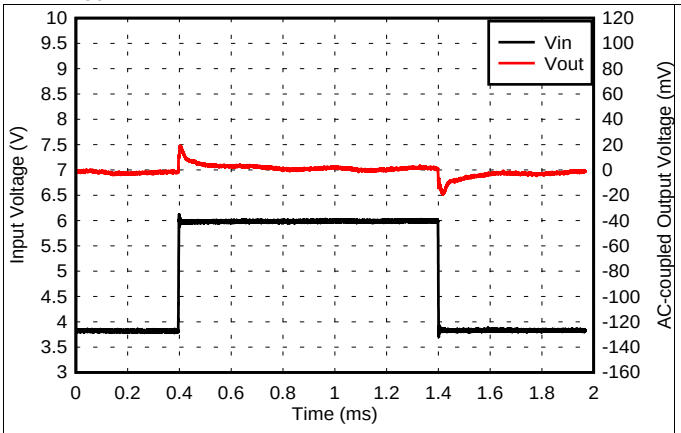


图 24. 0.55-V Line Transient

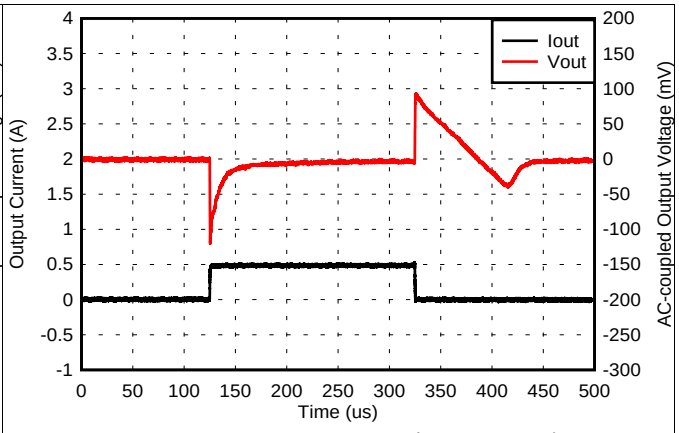
Typical Characteristics (接下页)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



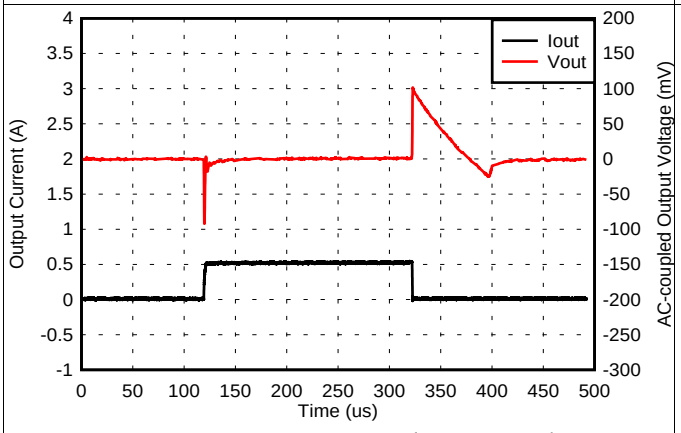
V_{OUT} = 3.3 V, I_{OUT} = 1 mA, V_{IN} slew rate = 1 V/µs

图 25. 3.3-V Line Transient



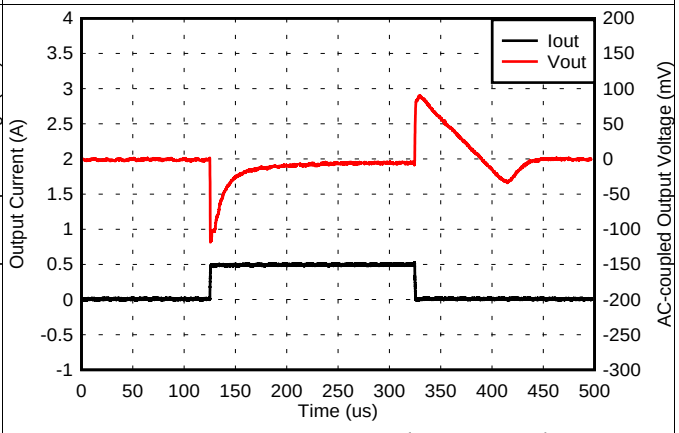
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} slew rate = 1 A/µs

图 26. 3.3-V, 1-mA to 500-mA Load Transient



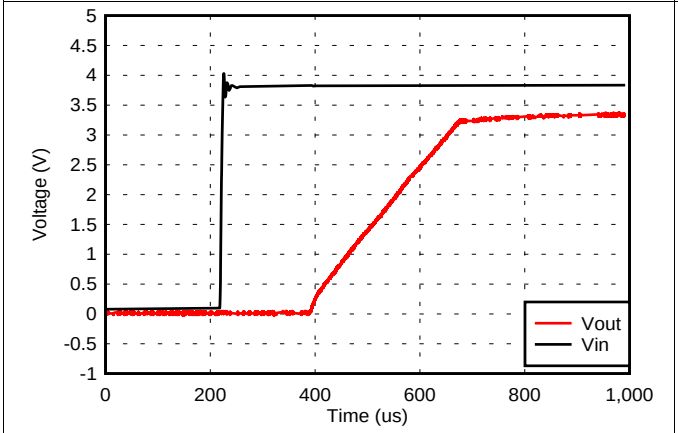
V_{IN} = 2 V, V_{OUT} = 0.55 V, I_{OUT} slew rate = 1 A/µs

图 27. 0.55-V, 1-mA to 500-mA Load Transient



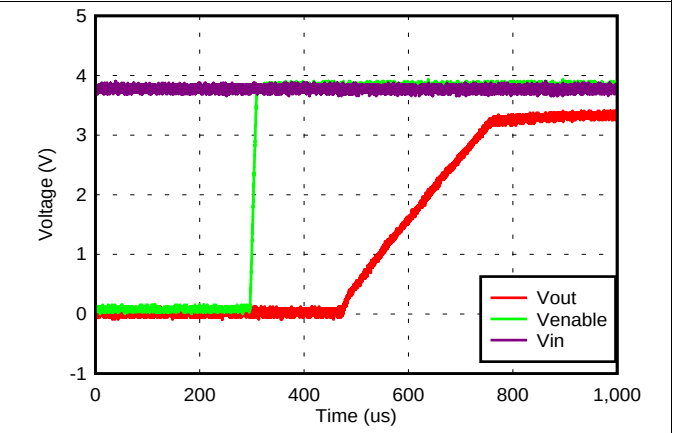
V_{IN} = 5.5 V, V_{OUT} = 5 V, I_{OUT} slew rate = 1 A/µs

图 28. 5-V, 1-mA to 500-mA Load Transient



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA

图 29. V_{IN} Power-Up

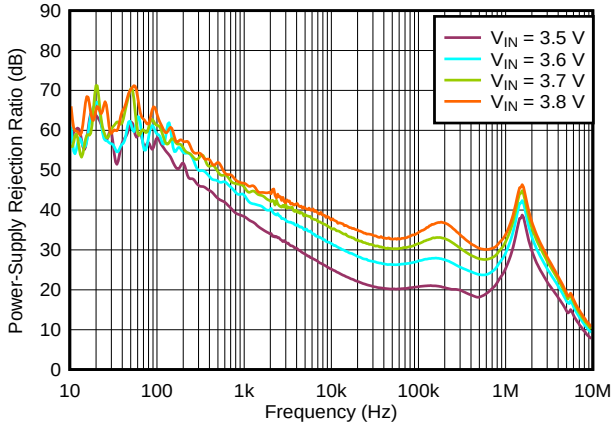


V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA

图 30. Startup With EN

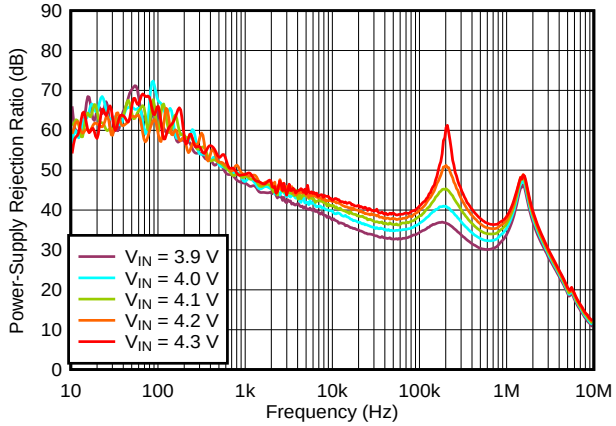
Typical Characteristics (接下页)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



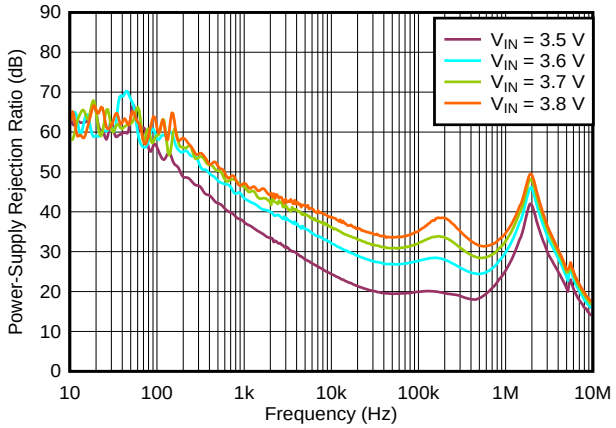
V_{OUT} = 3.3 V, I_{OUT} = 500 mA, C_{OUT} = 2.2 µF

图 31. PSRR vs Frequency and V_{IN}



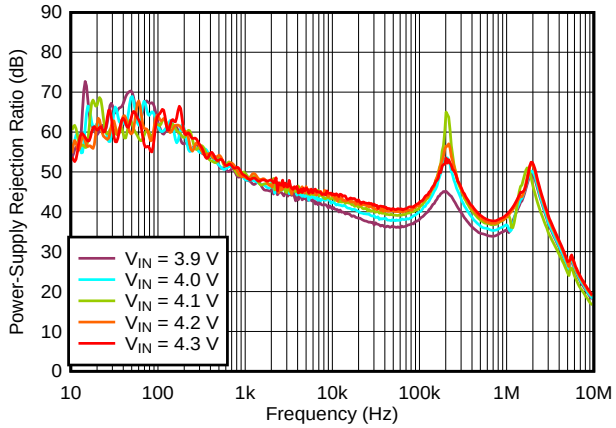
V_{OUT} = 3.3 V, I_{OUT} = 500 mA, C_{OUT} = 2.2 µF

图 32. PSRR vs Frequency and V_{IN}



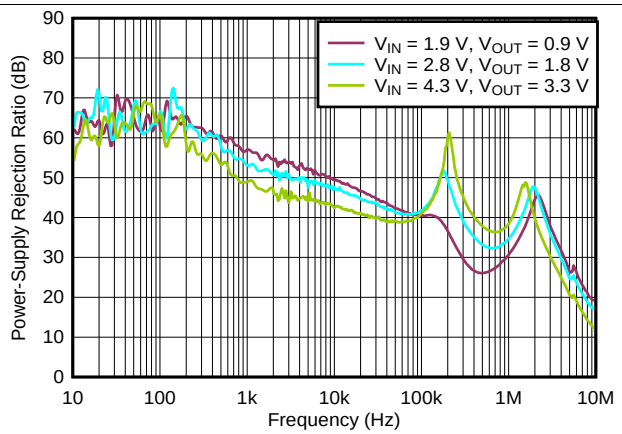
V_{OUT} = 3.3 V, I_{OUT} = 250 mA, C_{OUT} = 2.2 µF

图 33. PSRR vs Frequency and V_{IN}



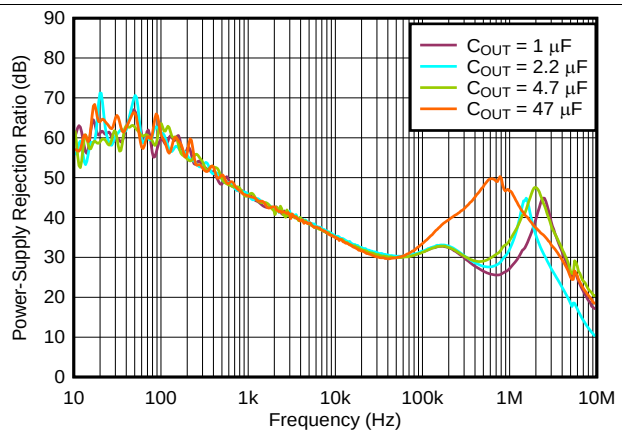
V_{OUT} = 3.3 V, I_{OUT} = 250 mA, C_{OUT} = 2.2 µF

图 34. PSRR vs Frequency and V_{IN}



I_{OUT} = 500 mA, C_{OUT} = 2.2 µF

图 35. PSRR vs Frequency

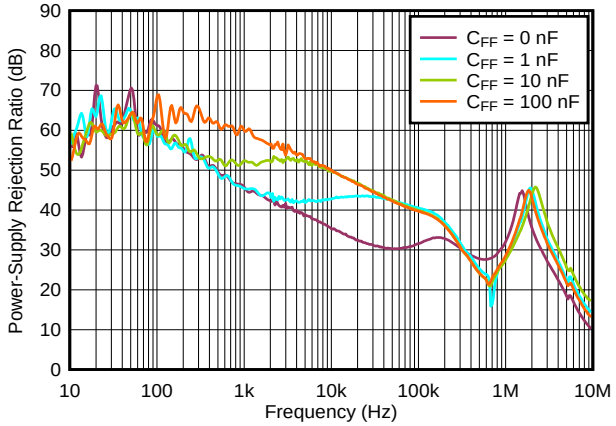


V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

图 36. PSRR vs Frequency and C_{OUT}

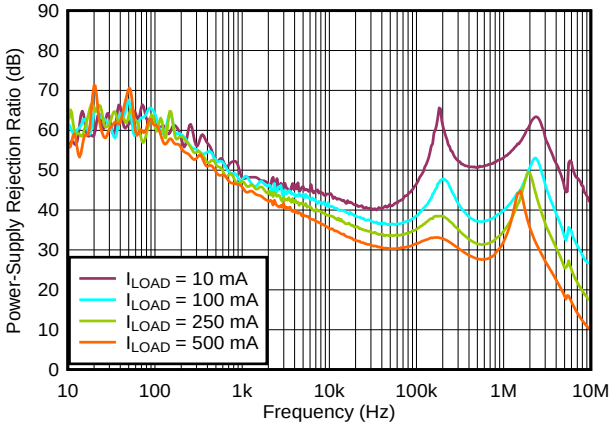
Typical Characteristics (接下页)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



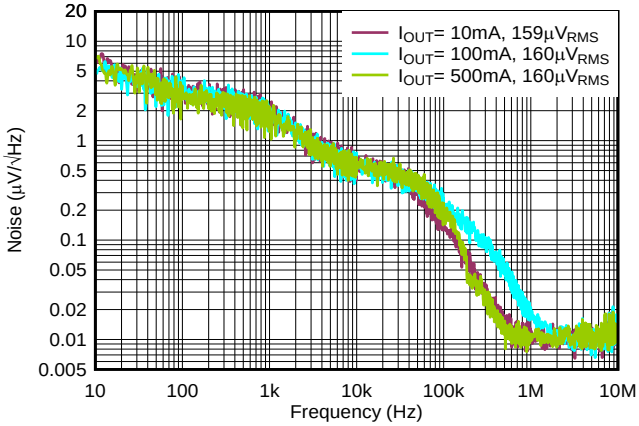
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

图 37. PSRR vs Frequency and C_{FF}



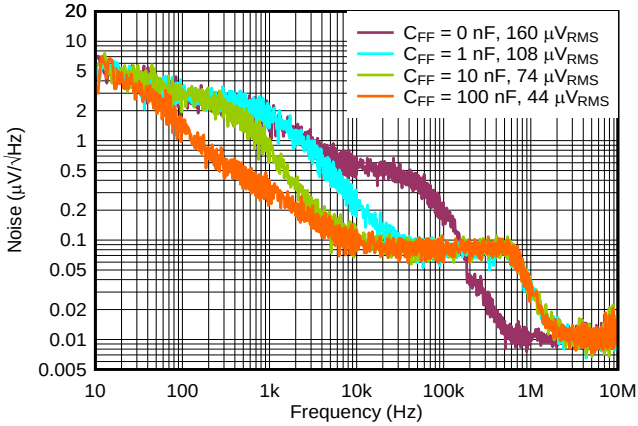
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF

图 38. PSRR vs Frequency and I_{LOAD}



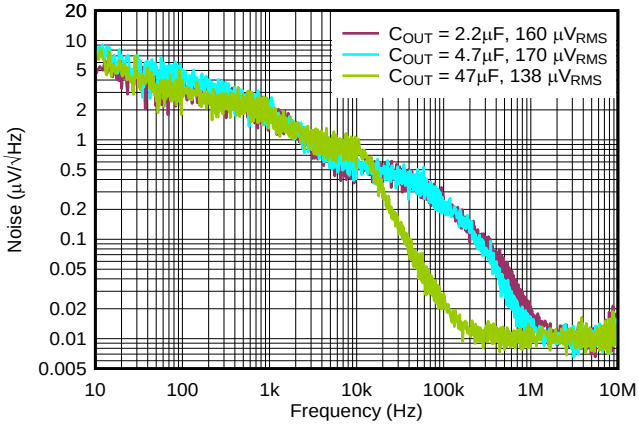
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF,
V_{RMS} BW = 10 Hz to 100 kHz

图 39. Output Spectral Noise Density



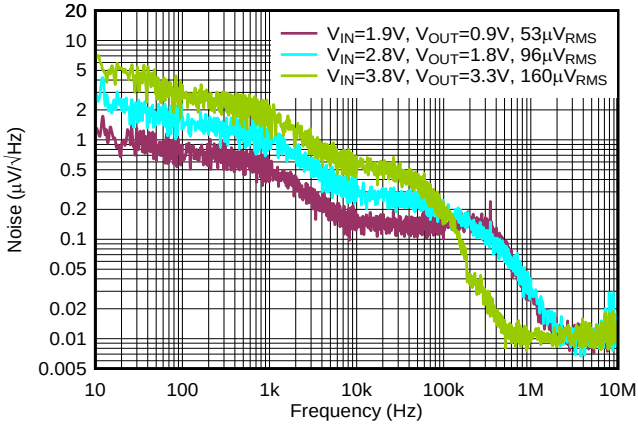
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA, C_{OUT} = 2.2 µF,
V_{RMS} BW = 10 Hz to 100 kHz

图 40. Output Spectral Noise Density vs Frequency and C_{FF}



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 100 mA, C_{FF} = 0 µF,
V_{RMS} BW = 10 Hz to 100 kHz

图 41. Output Spectral Noise Density vs Frequency and C_{OUT}



I_{OUT} = 500 mA, C_{OUT} = 2.2 µF, V_{RMS} BW = 10 Hz to 100 kHz

图 42. Output Spectral Noise Density vs Frequency

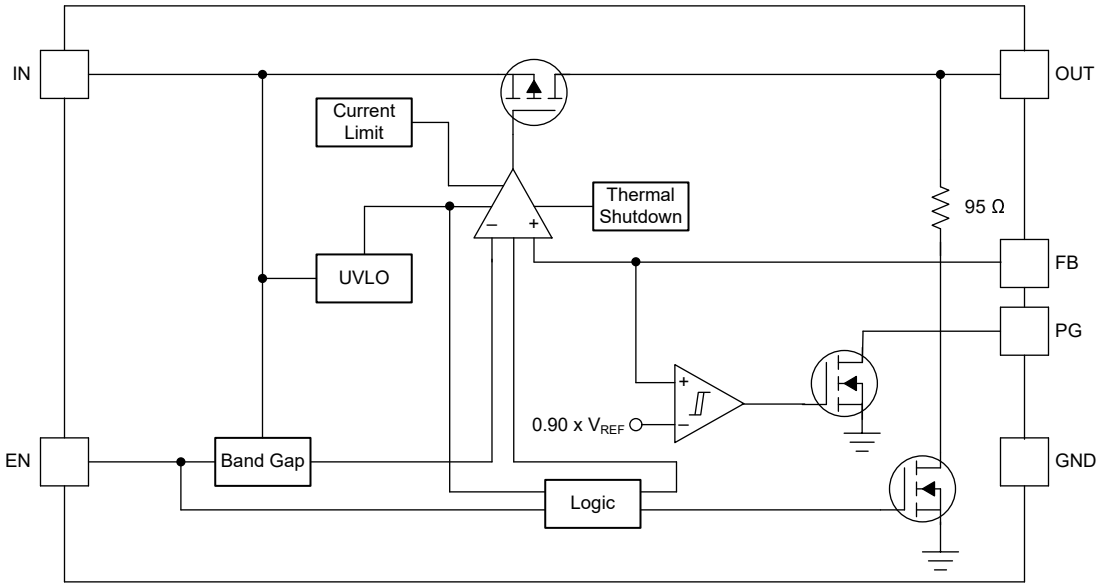
7 Detailed Description

7.1 Overview

The TPS745 low-dropout regulators (LDO) consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise and good PSRR with low dropout voltage, make this device ideal for portable consumer applications. The internal power-good detection circuit allows the down-stream supplies to be sequenced and alerts if the output voltage is below a regulation threshold.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TPS745 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage (V_{UVLO}). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When V_{IN} is less than V_{UVLO}, the output is connected to ground with a pulldown resistor ($R_{PULLDOWN}$). When the device enters UVLO, the PG output is pulled low.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$. Turn off the device by forcing the EN pin to drop below $V_{EN(LO)}$. If shutdown capability is not required, connect EN to IN.When the device is disabled, the PG output pin is pulled low.

The TPS745 has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor ($R_{PULLDOWN}$). 公式 1 calculates the time constant:

$$\tau = (R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L) \quad (1)$$

Feature Description (continued)

7.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4\ V \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

Figure 43 shows a diagram of the foldback current limit.

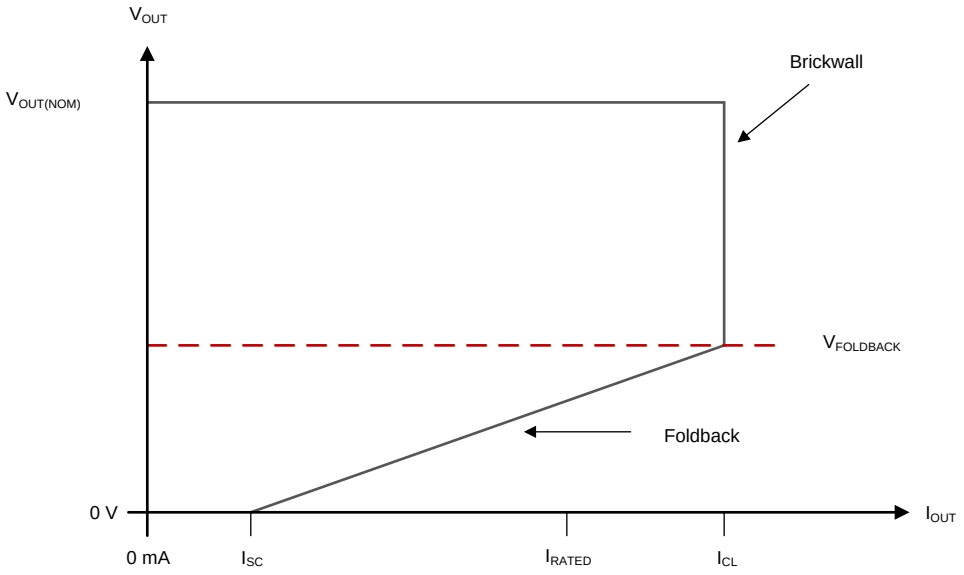


Figure 43. Foldback Current Limit

7.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 170°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the ($V_{IN} – V_{OUT}$) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

Feature Description (continued)

The TPS745 internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TPS745 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Device Feedback Resistors

图 44 shows that the output voltage of the TPS745 can be adjusted from 0.55 V to 5.5 V by using a resistor divider network.

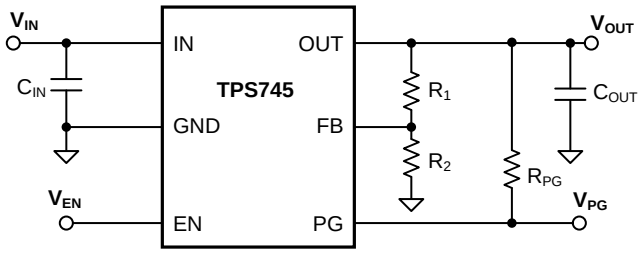


图 44. Adjustable Operation

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

For this device, V_{FB} = 0.55 V.

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

For this device, I_{FB} = 10 nA.

8.1.2 Input and Output Capacitor Selection

The TPS745 requires an output capacitance of 0.47 µF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application, pay attention to the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

Application Information (接下页)

8.1.3 Dropout Voltage

The TPS745 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation.

8.1.4 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output may overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in 图 45, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

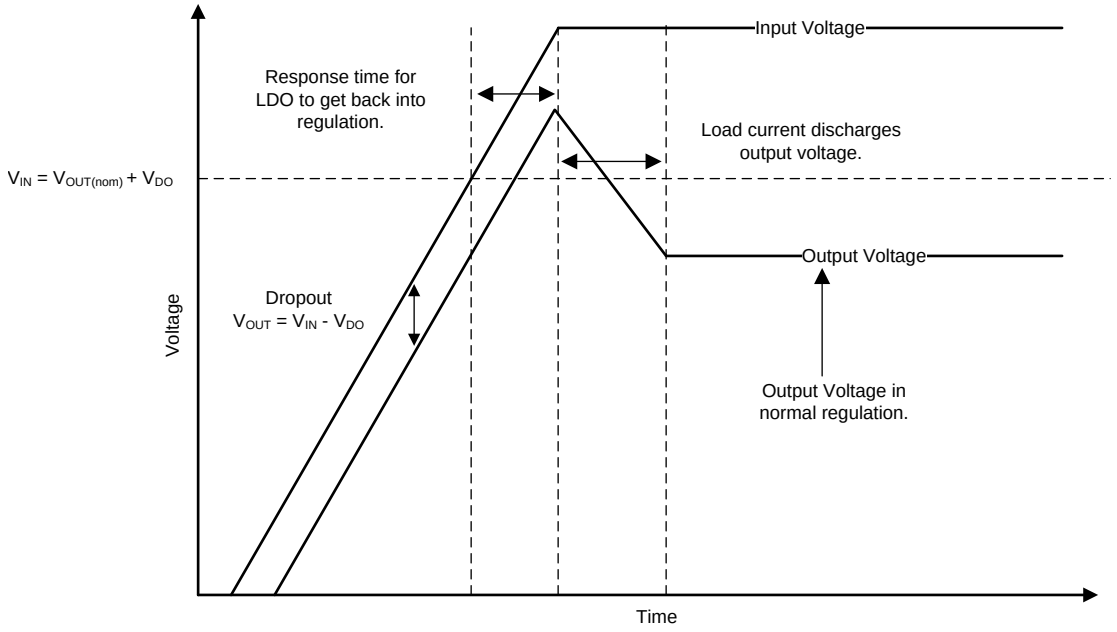


图 45. Startup Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. 图 46 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (VGS) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

Application Information (接下页)

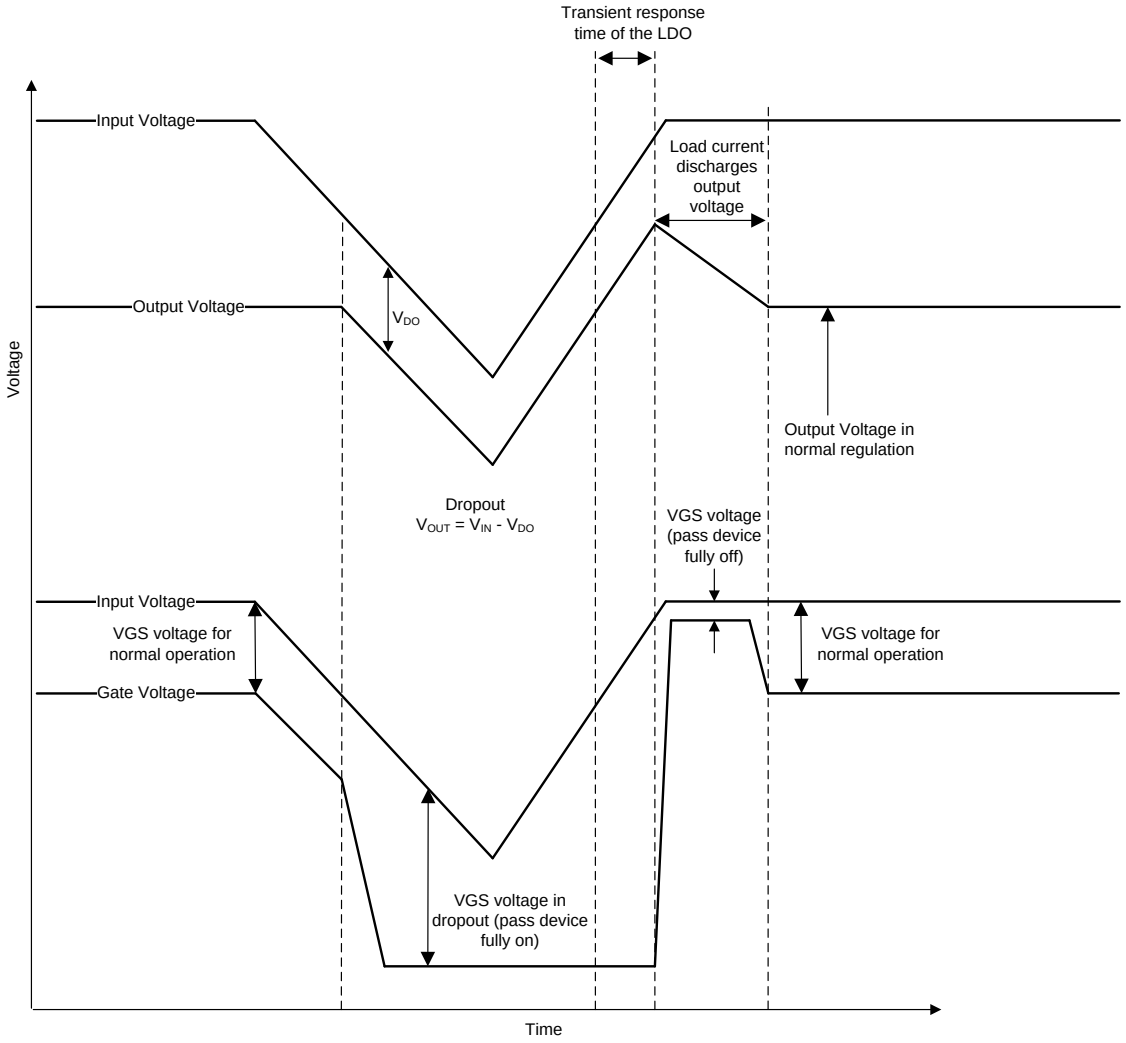


图 46. Line Transients From Dropout

8.1.5 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

Application Information (接下页)

If reverse current flow is expected in the application, external protection must be used to protect the device. 图 47 shows one approach of protecting the device.

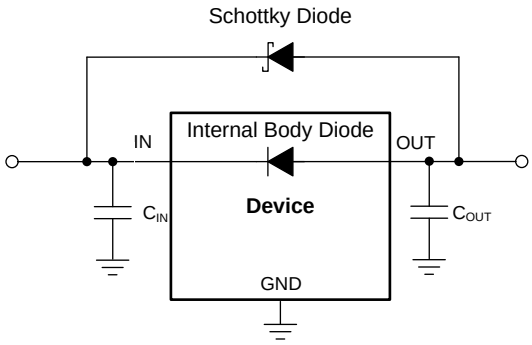


图 47. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 4 calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (4)$$

NOTE

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to Equation 5, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.1.7 Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the output voltage falls below the PG threshold voltage (PG_{LTH}), the PG pin open-drain output engages and pulls the PG pin close to GND. When the output voltage exceeds PG_{HTH}, the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device. Using a pullup resistor from 10 kΩ to 100 kΩ is recommended.

Application Information (接下页)

When using a feed-forward capacitor (C_{FF}), the time constant for the LDO startup is increased whereas the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue, and to receive a valid PG output, make sure that the time constant of both the LDO startup and the power-good output match, which can be done by adding a capacitor in parallel with the power-good pullup resistor. For more information, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

The state of PG is only valid when the device operates above the minimum input voltage of the device and power-good is asserted, regardless of the output voltage state when the input voltage falls below the UVLO threshold minus the UVLO hysteresis. When the input voltage falls below approximately 0.8 V, there is not enough gate drive voltage to keep the open-drain, power-good device turned on and the power-good output pulled high. Connecting the power-good pullup resistor to the output voltage can help minimize this effect.

8.1.8 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the startup time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

8.2 Typical Application

图 48 shows the typical application circuit for the TPS745. Input and output capacitances must be at least 1 µF.

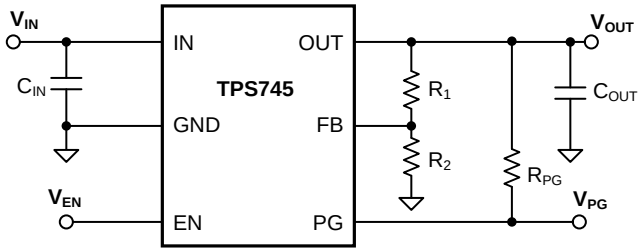


图 48. TPS745 Typical Application

8.2.1 Design Requirements

Use the parameters listed in 表 2 for typical linear regulator applications.

表 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.8 V
Output voltage	3.3 V, ±1%
Input current	500 mA (maximum)
Output load	500-mA DC
Maximum ambient temperature	70°C

8.2.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 2.2 µF are selected to give the maximum output capacitance in a small, low-cost package; see the *Input and Output Capacitor Selection* section for details.

图 44 illustrates the output voltage of the TPS745. Set the output voltage using the resistor divider; see the section for details.

8.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During startup, the input current is higher as a result of the inrush current charging the output capacitor. Use 公式 6 to calculate the current through the input.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (6)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

8.2.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use 公式 7 to calculate the power dissipation. Multiply P_D by $R_{\theta JA}$ as 公式 8 shows and add the ambient temperature (T_A) to calculate the junction temperature (T_J).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (7)$$

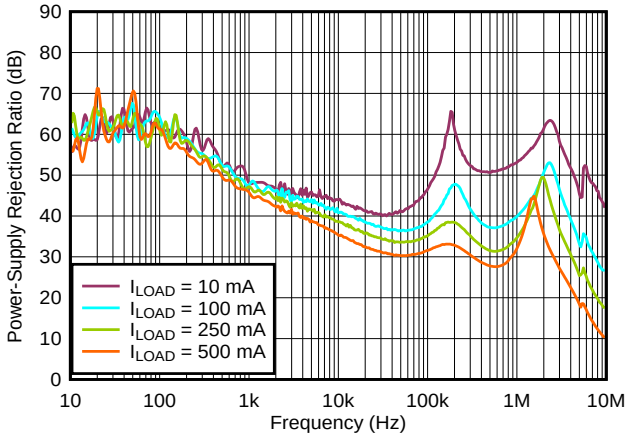
$$T_J = R_{\theta JA} \times P_D + T_A \quad (8)$$

Calculate the maximum ambient temperature as 公式 9 shows if the ($T_{J(MAX)}$) value does not exceed 125°C. 公式 10 calculates the maximum ambient temperature with a value of 104.93°C.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (9)$$

$$T_{A(MAX)} = 125°C - 80.3°C/W \times (3.8\ V - 3.3\ V) \times (0.5\ A) = 104.93°C \quad (10)$$

8.2.3 Application Curve



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF

图 49. PSRR vs Frequency and I_{LOAD}

9 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TPS745.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections, in order to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Example

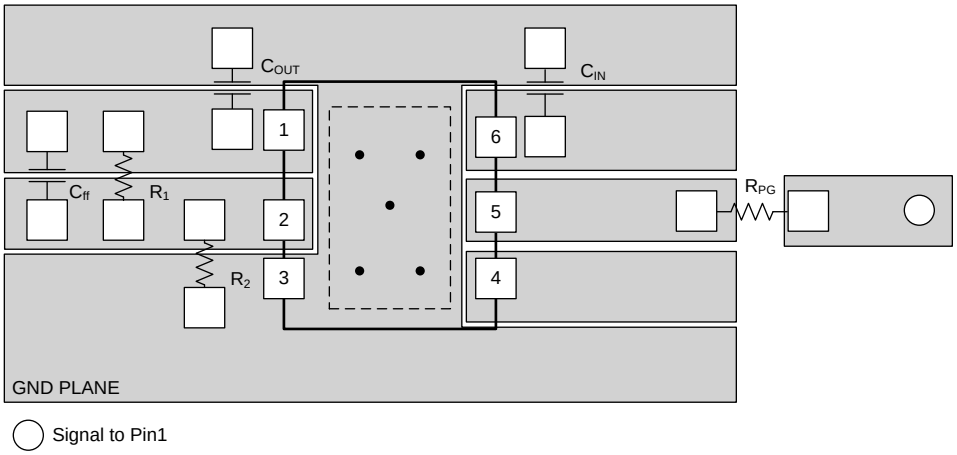


图 50. DRV Package Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

德州仪器 (TI)，*《使用前馈电容器和低压降稳压器的优缺点》*应用报告

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS74501PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MEH
TPS74501PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MEH
TPS74501PDRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MEH
TPS74501PDRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MEH
TPS74501PDRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MEH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS745 :

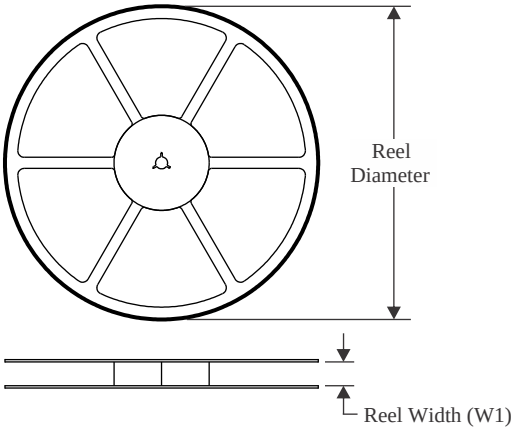
- Automotive : TPS745-Q1

NOTE: Qualified Version Definitions:

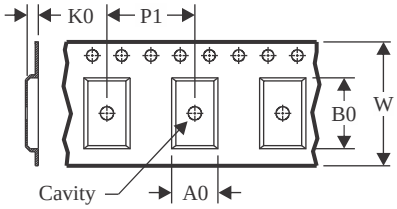
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

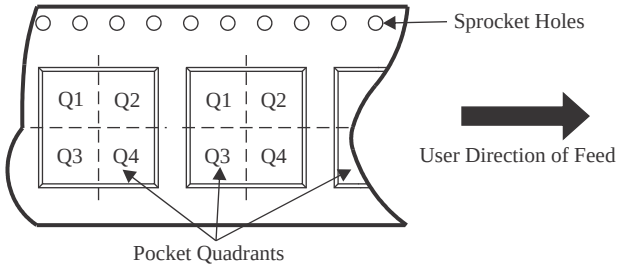


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

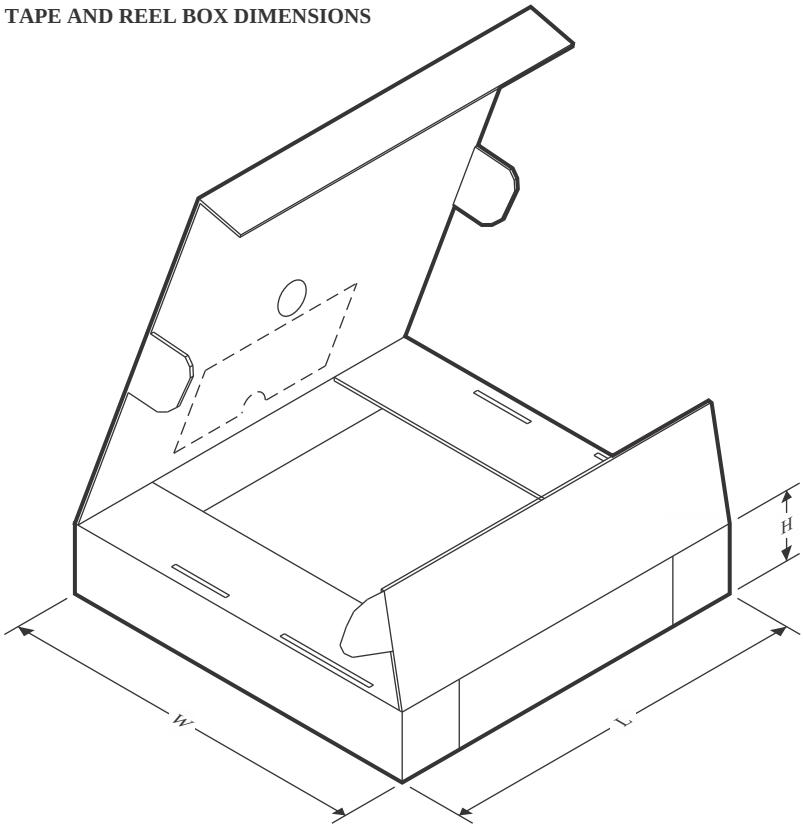
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74501PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS74501PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

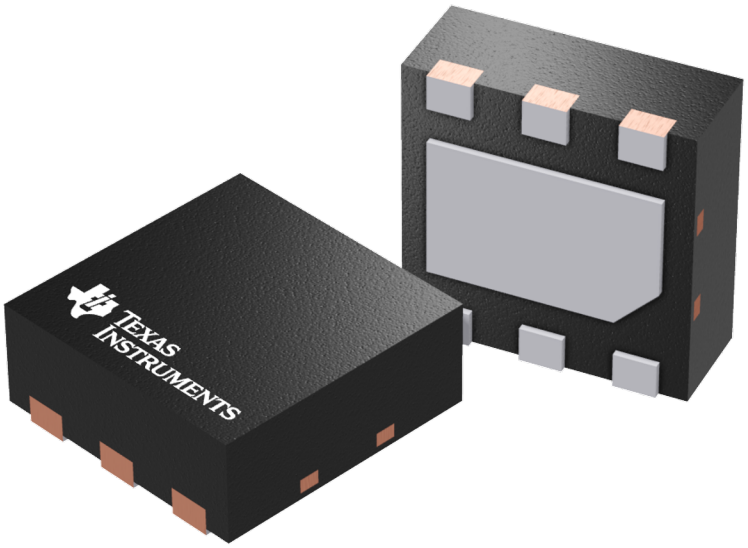


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74501PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS74501PDRVT	WSON	DRV	6	250	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



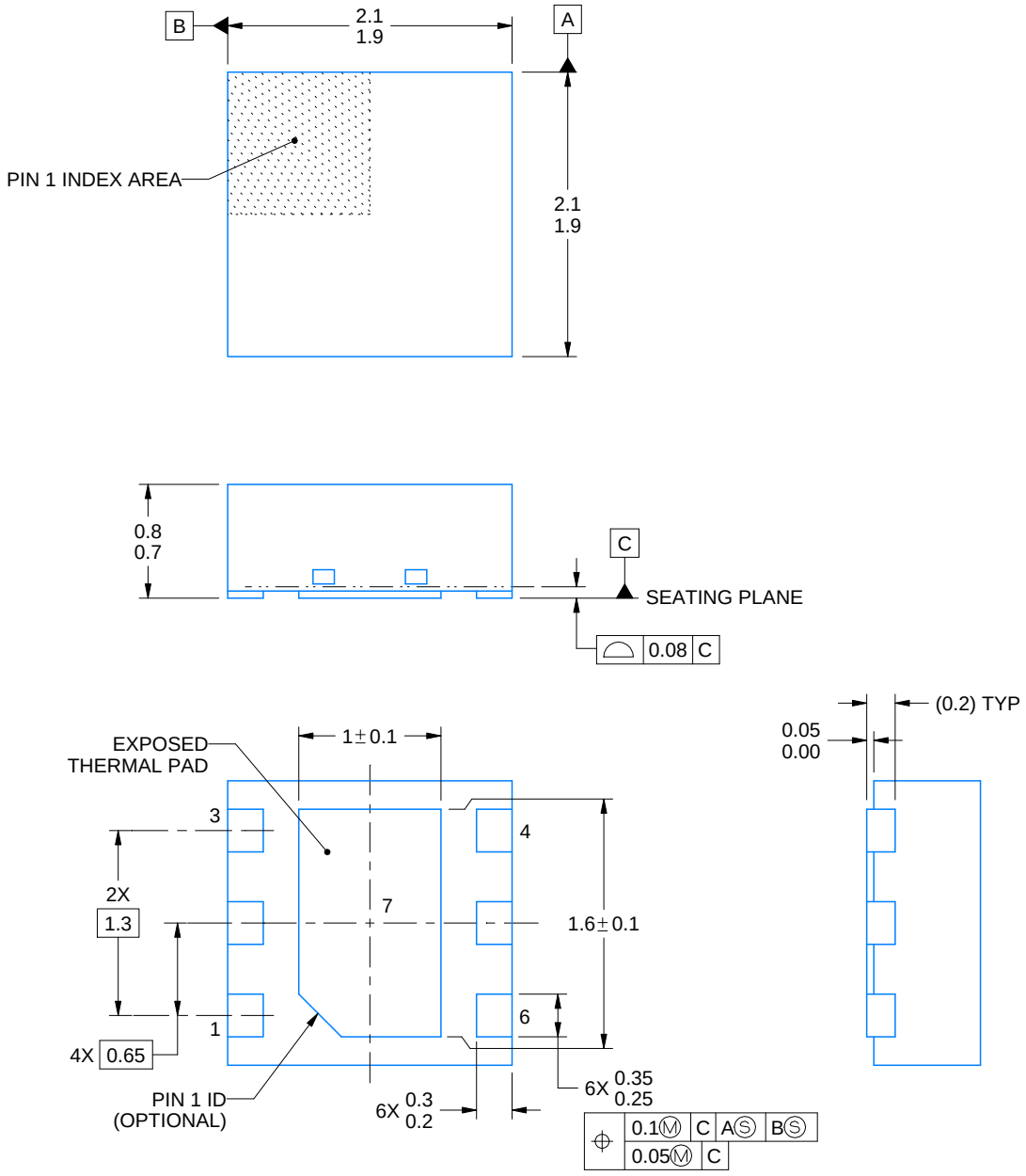
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

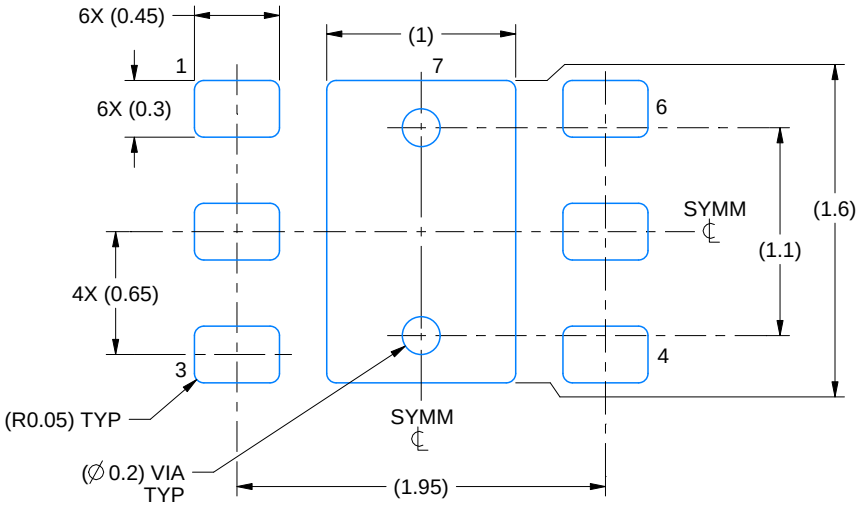
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

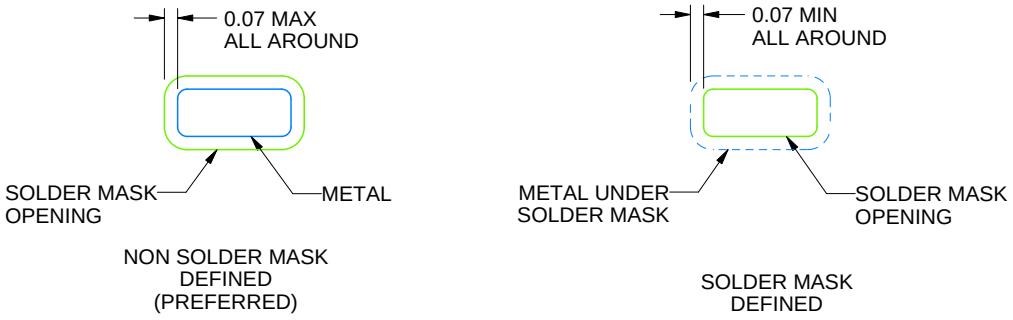


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

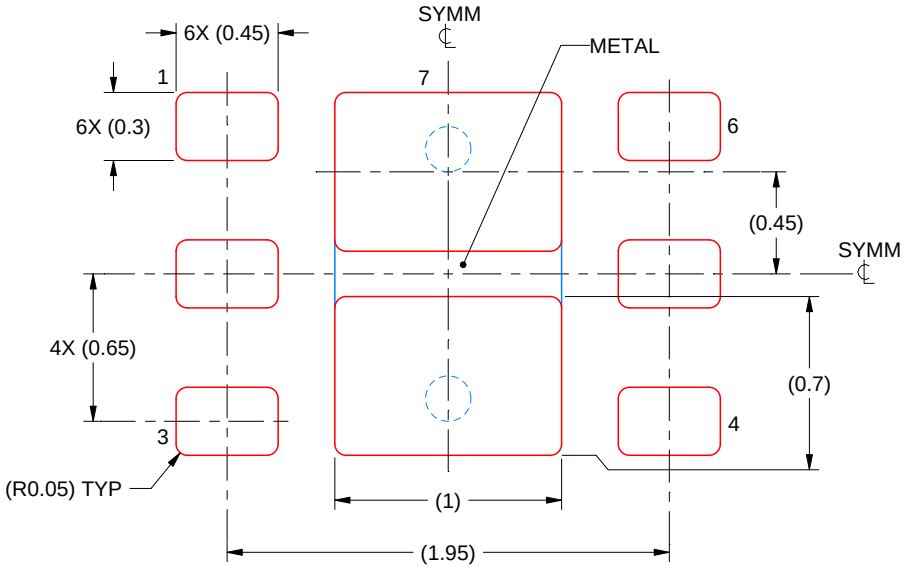
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265