Fully Programmable LCD Bias IC for TV with 6-Channel Gamma Buffer, Vcom Reference and Dynamic Gain

Check for Samples: TPS65178, TPS65178A

FEATURES

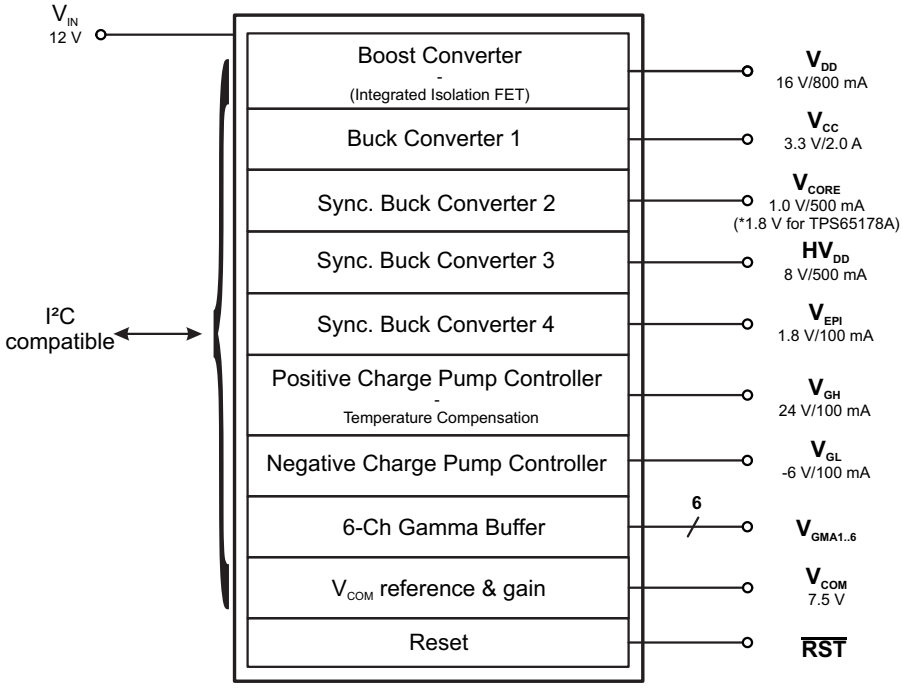
- 8.6V to 14.7V Input Voltage Range
- Boost Converter V_{DD}: 12.8V…19V (6-Bit)
- Integrated Input-to-Output Isolation Switch
- Buck Converter HV_{DD}: V_{DD} tracking
- Buck Converter V_{CC}: 3.0V…3.7V (3-Bit)
- Buck Converter V_{CORE}: 0.9V…2.4V (4-Bit)
- Buck Converter V_{EPI}: 0.9V…2.4V (4-Bit)
- Positive Charge Pump V_{GH}:
  - 19V…34V for Low Temperature (4-Bit)
  - 17V…32V for High Temperature (4-Bit)
- Temperature Compensation for V_{GH}
- Negative Charge Pump V_{GL}: –1.8V…–8.1V (6-Bit)
- 6-Ch Gamma Buffer:
  - 3-Ch: V_{DD}…HV_{DD} (9-Bit)
  - 3-Ch: HV_{DD}...GND (9-Bit)
- 9-Bit V_{COM} Reference
- 2-Bit V_{COM} Gain
- Selectable Dynamic Gain
- Reset Signal With Programmable Delay Time
- Programmable Sequencing Delays (3 × 3-Bit)
- Thermal Shutdown
- 48-Pin 6-mm × 6-mm QFN Package

APPLICATIONS

- LCD TVs
- LCD Monitors

DESCRIPTION

The TPS65178/A provides a simple and economic power supply solution for a wide variety of LCD bias applications. The device provides all supply rails needed by a TFT-LCD panel but also 6 gamma references, a supply rail for LVDS support, as well as a Vcom reference and its programmable dynamic gain. The solution is delivered in a small 6x6mm QFN package.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The TPS65178/A provides a simple and economic power supply solution for a wide variety of LCD bias applications. The device provides all supply rails needed by a TFT-LCD panel. V_{CC}, V_{CORE} and $\overline{RST}$ for the T-Con. V_{DD} and HV_{DD} for the Source Driver. V_{GH} and V_{GL} for the Gate Driver or the Level Shifter. The V_{GH} voltage can be compensated for low and high temperatures, if GIP (Gate In Panel) technology is used.The transition from one programmed V_{GH} value to another is made using an external thermistor connected to the IC. In addition, a 6-channel Gamma Buffer is integrated as well as the V_{COM} reference and programmable gain (fixed or dynamic). A V_{EPI} supply rail is also integrated. All output rails and delay times are programmable by a two-wire interface: a single BOM (Bill of Material) can cover several panel types and sizes whose desired output levels can be programmed in production and stored in a non-volatile memory embedded into the TPS65178/A. V_{CORE}, V_{EPI} and HV_{DD} are generated by synchronous buck converters which support chip inductors for an optimized solution size. The solution is delivered in a small 6x6mm QFN package.

ORDERING INFORMATION(1)

T_A	ORDERING	PACKAGE	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY	V_{CORE} DEFAULT VALUE
–40°C to 85°C	TPS65178RSLR	48-Pin 6x6 QFN	TPS65178	Tape and reel , 3000	1.0 V
	TPS65178ARSLR		TPS65178A		1.8 V

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	VALUE		UNIT
	MIN	MAX	
Input voltage range AVIN, PVINB1, PVINB3(2)	–0.3	20	V
Voltage range on pin CTRLP, TCOMP, VGH(2)	–0.3	40	V
Voltage range on pins DYN, GMA1–GMA6, NEG, OUT3, POS, SW, SWB1, SWB3, SWI, SWN, SWO, SWP, VCOM, VCOMFB(2)	–0.3	20	V
Voltage on pin COMP, CTRLN, OUT1, OUT2, OUT4, $\overline{RST}$, SCL, SDA, SS, SWB2, SWB4, VL(2)	–0.3	7	V
Voltage on pin VGL(2)	–10	0.3	V
ESD rating HBM (Human Body Model)		2	kV
ESD rating MM (Machine Model)		200	V
ESD rating CDM (Charged Device Model)		700	V
Continuous power dissipation	See the Thermal Table		
Operating junction temperature range	–40	150	°C
Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) With respect to the GND pin.

THERMAL INFORMATION

THERMAL METRIC[1]		TPS65178/A RSL 48 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	29.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	17.2	
θ_{JB}	Junction-to-board thermal resistance	5.3	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	5.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
AV_{IN}	Input voltage range	8.6	12	14.7	V
C_{VL}	Input capacitor on internal regulator input pin VL		1		µF
BOOST CONVERTER					
V_{DD}	Boost output voltage range	12.8		19	V
L	Boost converter inductor	10		22	µH
C_{IN_BOOST}	Input capacitor on boost converter input	20			µF
C_{OUT_BOOST}	Output capacitor on boost converter output on SWI pin	10	20		µF
C_{OUT_ISO}	Output capacitor on isolation MosFET output on SWO pin	30	40		µF
BUCK 1 CONVERTER					
V_{CC}	Buck 1 converter output voltage range	3.0		3.7	V
L1	Buck 1 converter inductor	10		22	µH
C_{IN_BUCK1}	Input capacitor on buck 1 converter input pin PVINB1	10			µF
C_{OUT_BUCK1}	Output capacitor on buck 1 converter output	30	40		µF
BUCK 2 CONVERTER					
V_{CORE}	Buck 2 converter output voltage range	0.9		2.4	V
L2	Buck 2 converter inductor	1.0		2.2	µH
C_{IN_BUCK2}	Input capacitor on buck 2 converter input pin OUT1	1.0	4.7		µF
C_{OUT_BUCK2}	Output capacitor on buck 2 converter output	2.2	4.7	20	µF
BUCK 3 CONVERTER					
HV_{DD}	Buck 3 converter output voltage range		$V_{DD}/2$		V
L3	Buck 3 converter inductor	4.7		6.8	µH
C_{IN_BUCK3}	Input capacitor on buck 3 converter input pin PVINB3		10		µF
C_{OUT_BUCK3}	Output capacitor on buck 3 converter output	4.7	10	20	µF
BUCK 4 CONVERTER					
V_{EPI}	Buck 4 converter output voltage range	0.9		2.4	V
L4	Buck 4 converter inductor	1.0		2.2	µH
C_{IN_BUCK4}	Input capacitor on buck 4 converter input pin OUT1	1.0	4.7		µF
C_{OUT_BUCK4}	Output capacitor on buck 4 converter output	2.2	4.7	20	µF
POSITIVE CHARGE PUMP CONTROLLER					
V_{GH_LT}	Positive charge pump output voltage range Low Temperature	19		34	V
V_{GH_HT}	Positive charge pump output voltage range High Temperature	17		32	V
C_{FLY_CP}	Charge pump flying capacitor		220		nF

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
C_{STOR_CP}	Charge pump storage capacitor		100		nF
C_{OUT_CP}	Charge pump output capacitor		4.7		µF
NEGATIVE CHARGE PUMP CONTROLLER					
V_{GL}	Negative charge pump output voltage range	–1.8		–8.1	V
C_{FLY_CP}	Charge pump flying capacitor		220		nF
C_{STOR_CP}	Charge pump storage capacitor		100		nF
C_{OUT_CP}	Charge pump output capacitor		4.7		µF
TEMPERATURE					
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

AV_{IN} = PV_{INB1} = PV_{INB3} = 12V, V_{DD} = 16V, HV_{DD} = 8V , V_{CC} = 3.3V, V_{CORE} = 1V, V_{EPI} = 1.8V, V_{GH_LT} = 28V, V_{GH_HT} = 26V
V_{GL} = –5V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		8.6		14.7	V
I_{Q_AVIN}	Supply quiescent current AVIN	Device not switching		3.2		mA
I_{Q_PVINB1}	Supply quiescent current PVINB1	Device not switching		0.1		mA
I_{Q_PVINB3}	Supply quiescent current PVINB3	Device not switching		1.6		mA
I_{Q_OUT1}	Supply quiescent current OUT1	Device not switching		50		µA
I_{Q_SWI}	Supply quiescent current SWI	Device not switching		5		mA
V_{UVLO}	Undervoltage lockout	V_{IN} rising	8.3	8.6	8.9	V
	Undervoltage lockout hysteresis		0.3	0.8	1.3	V
T_{SD}	Thermal shutdown	T_J rising		138		°C
T_{HYS}	Thermal shutdown hysteresis	T_J falling		8		°C
LOGIC SIGNAL DYN, SCL, SDA						
V_{IH1}	High level input voltage DYN	AV_{IN} = 8.6 V to 14.7 V	1.5			V
V_{IL1}	Low level input voltage DYN	AV_{IN} = 8.6 V to 14.7 V			0.5	V
V_{IH2}	High level input voltage SCL, SDA	AV_{IN} = 8.6 V to 14.7 V	2			V
V_{IL2}	Low level input voltage SCL, SDA	AV_{IN} = 8.6 V to 14.7 V			0.8	V
INTERNAL OSCILLATOR						
f_{OSC}	Switching frequency for the boost, buck1 converters and the charge pumps		480	600	720	kHz
INTERNAL REGULATOR						
V_L	Internal regulator	No load	4.8	5.0	5.2	V
BOOST CONVERTER [V_{DD}]						
V_{DD_ACC}	Output voltage accuracy	V_{DD} default value	–2%	16.05	2%	V
$r_{DS(on)}$	N-MOSFET on-resistance	I_{SW} = current limit		90	165	mΩ
I_{LIM}	N-MOSFET current limit		3.5	4.2	5	A
I_{SS}	Soft-start current	V_{SS} = 1.230 V		10		µA
	Line regulation	AV_{IN} = 8.6 V to 14.7 V, I_{OUT} = 700 mA		0.002		%/V
	Load regulation	I_{OUT} = 0 A to 1 A		0.066		%/A
ISOLATION SWITCH						
$r_{DS(on)ISO}$	Isolation MOSFET on-resistance	I_{SWI} = 1 A		100	180	mΩ
I_{SC_ISO}	Short circuit current limit	V_{SWI} = 12 V, V_{SWO} = 0 V		200		mA
BUCK 1 CONVERTER [V_{CC}]						

ELECTRICAL CHARACTERISTICS (continued)

AV_{IN} = PV_{INB1} = PV_{INB3} = 12V, V_{DD} = 16V, HV_{DD} = 8V , V_{CC} = 3.3V, V_{CORE} = 1V, V_{EPI} = 1.8V, V_{GH_LT} = 28V, V_{GH_HT} = 26V
V_{GL} = –5V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC_ACC}	Output voltage accuracy	V_{CC} default value	–3%	3.3	3%	V
$r_{DS(on)}$	Switch on-resistance	I_{SWB1} = current limit		180	300	mΩ
I_{LIM}	Switch current limit		2.6	3.4	4.2	A
	Line regulation	V_{IN} = AV_{IN} = PV_{INB1} = 8.6 V to 14.7 V I_{CC} = 400 mA		0.001		%/V
	Load regulation	I_{CC} = 0 A to 1 A		0.033		%/A
BUCK 2 CONVERTER [V_{CORE}]						
V_{CORE_ACC}	Output voltage accuracy	V_{CORE} default value TPS65178	–3%	1.0	3%	V
		V_{CORE} default value TPS65178A	–3%	1.8	3%	
$r_{DS(on)}$	MOSFET on-resistance	I_{SBW2} = current limit		220	400	mΩ
I_{LIM}	Switch current limit		1.1	1.4	1.8	A
f_{SWB2}	Switching frequency buck 2 converter		1.1	1.7	2.3	MHz
	Line regulation	OUT1 = 3.0 V to 3.7 V I_{CORE} = 300 mA		0.008		%/V
	Load regulation	I_{CORE} = 0 A to 500 mA		0.114		%/A
BUCK 3 CONVERTER [HV_{DD}]						
HV_{DD_ACC}	Output voltage accuracy	HV_{DD} default value	–3%	8.03	3%	V
$r_{DS(on)}$	MOSFET on-resistance	I_{SBW3} = current limit		320	480	mΩ
I_{LIM}	Switch current limit – source		0.9	1.3	1.7	A
	Switch current limit – sink		-0.9	-1.3	-1.7	
f_{SWB3}	Switching frequency buck 3 converter		1.4	1.6	1.8	MHz
	Line regulation	AV_{IN} = PV_{INB3} = 8.6 V to 14.7 V I_{OUT} = ±300 mA		0.003		%/V
	Load regulation	I_{OUT} = –500 mA to 500 mA		0.007		%/A
BUCK 4 CONVERTER [V_{EPI}]						
V_{EPI_ACC}	Output voltage accuracy	V_{EPI} default value	–3%	1.8	3%	V
$r_{DS(on)}$	MOSFET on-resistance	I_{SBW4} = current limit		250	450	mΩ
I_{LIM}	Switch current limit		0.5	0.7	1.0	A
f_{SWB4}	Switching frequency buck 4 converter		1.2	1.9	2.6	MHz
	Line regulation	OUT1 = 3.0 V to 3.7 V I_{EPI} = 100 mA		0.029		%/V
	Load regulation	I_{EPI} = 0 A to 100 mA		0.190		%/A
POSITIVE CHARGE PUMP CONTROLLER [V_{GH}]						
$V_{GH\_LT\_ACC}$	Output voltage accuracy	V_{GH_LT} default value	–3.5%	28	3.5%	V
$V_{GH\_HT\_ACC}$		V_{GH_HT} default value	–3.5%	26	3.5%	V
I_{CTRLP_SC}	Base current during short circuit	VGH = GND	40		75	µA
I_{CTRLP_max}	Maximum base current		1		2	mA
	Line regulation	AV_{IN} = 8.6 V to 14.7 V, I_{GH} = 50 mA		0.004		%/V
	Load regulation	I_{GH} = 0 A to 100 mA		0.414		%/A
NEGATIVE CHARGE PUMP CONTROLLER [V_{GL}]						
V_{GL}	Output voltage accuracy	V_{GL} default value	-3.5%	-5	3.5%	V
I_{CTRLN_SC}	Base current during short circuit	VGL = GND	200		440	µA
I_{CTRLN_max}	Maximum base current		1		3	mA
	Line regulation	AV_{IN} = 8.6 V to 14.7 V, I_{GL} = 50 mA		0.001		%/V
	Load regulation	I_{GL} = 0 A to 100 mA		0.817		%/A
GAMMA BUFFER [GMA]						
I_O	Continuous output current		10	30		mA

ELECTRICAL CHARACTERISTICS (continued)

AV_{IN} = PV_{INB1} = PV_{INB3} = 12V, V_{DD} = 16V, HV_{DD} = 8V , V_{CC} = 3.3V, V_{CORE} = 1V, V_{EPI} = 1.8V, V_{GH_LT} = 28V, V_{GH_HT} = 26V
V_{GL} = –5V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH1}	Output voltage swing high GMA1,2,3	I_{OUT} = 10mA	V_{DD}-0.7	V_{DD}-0.5		V
V_{OL1}	Output voltage swing low GMA1,2,3	I_{OUT} = 10mA		HV_{DD}+0.5	HV_{DD}+0.7	V
V_{OH2}	Output voltage swing high GMA4,5,6	I_{OUT} = 10mA	HV_{DD}-0.7	HV_{DD}-0.5		V
V_{OL2}	Output voltage swing low GMA4,5,6	I_{OUT} = 10mA		0.5	0.7	V
INL_max	Maximum integral nonlinearity			±0.6		LSB
DNL_max	Maximum differential nonlinearity			±0.3		LSB
P-VCOM [VPOS]						
V_{POS}	Output voltage accuracy	V_{POS} default value	-1.5%	6.5	1.5%	V
RESET GENERATOR [$\overline{RST}$](1)						
$V_{\overline{RST}(ON)}$	Low voltage level	$I_{\overline{RST}(ON)}$ = 1 mA			0.5	V
$I_{LEAK\_\overline{RST}}$	Leakage current	$V_{\overline{RST}(ON)}$ = V_{CC} = 3.3 V			2	µA

(1) External pull-up resistor to be chosen so that the current flowing into $\overline{RST}$ pin when active ($V_{\overline{RST}}$ = 0 V) is below $I_{\overline{RST}(ON)}$ = 1 mA.

I^2C INTERFACE TIMING CHARACTERISTICS (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			µs
		Fast mode	600			ns
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
$t_{hd;STA}$	Hold time for a repeated START condition	Standard mode	4.0			µs
		Fast mode	600			ns
$t_{su;STA}$	Setup time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	600			ns
$t_{su;DAT}$	Data setup time	Standard mode	250			ns
		Fast mode	100			ns
$t_{hd;DAT}$	Data hold time	Standard mode	0.05		3.45	µs
		Fast mode	0.05		0.9	µs
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard mode	20 + 0.1C_B		1000	ns
		Fast mode	20 + 0.1C_B		1000	ns
t_{RCL}	Rise time of SCL signal	Standard mode	20 + 0.1C_B		1000	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{FCL}	Fall time of SCL signal	Standard mode	20 + 0.1C_B		300	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{RDA}	Rise time of SDA signal	Standard mode	20 + 0.1C_B		1000	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{FDA}	Fall time of SDA signal	Standard mode	20 + 0.1C_B		300	ns
		Fast mode	20 + 0.1C_B		300	ns

(1) Industry standard I^2C timing characteristics. Not tested in production.

I²C INTERFACE TIMING CHARACTERISTICS (1) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su;STO}$	Setup time for STOP condition	Standard mode	4.0			µs
		Fast mode	600			ns
C_B	Capacitive load for SDA and SCL				0.4	nF

I²C TIMING DIAGRAMS

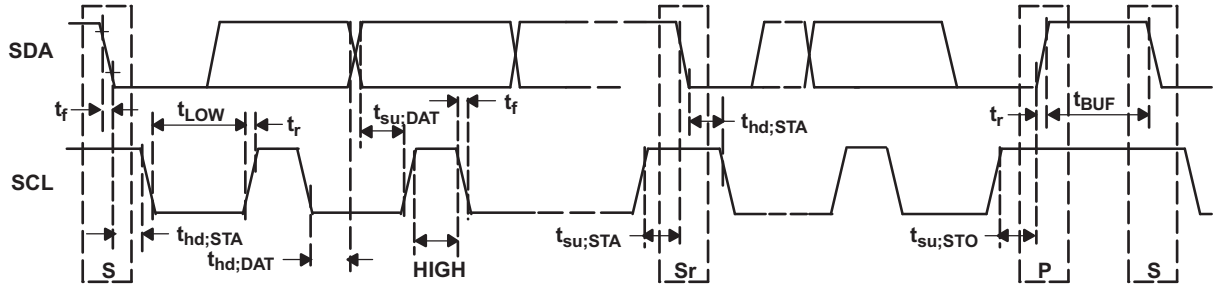
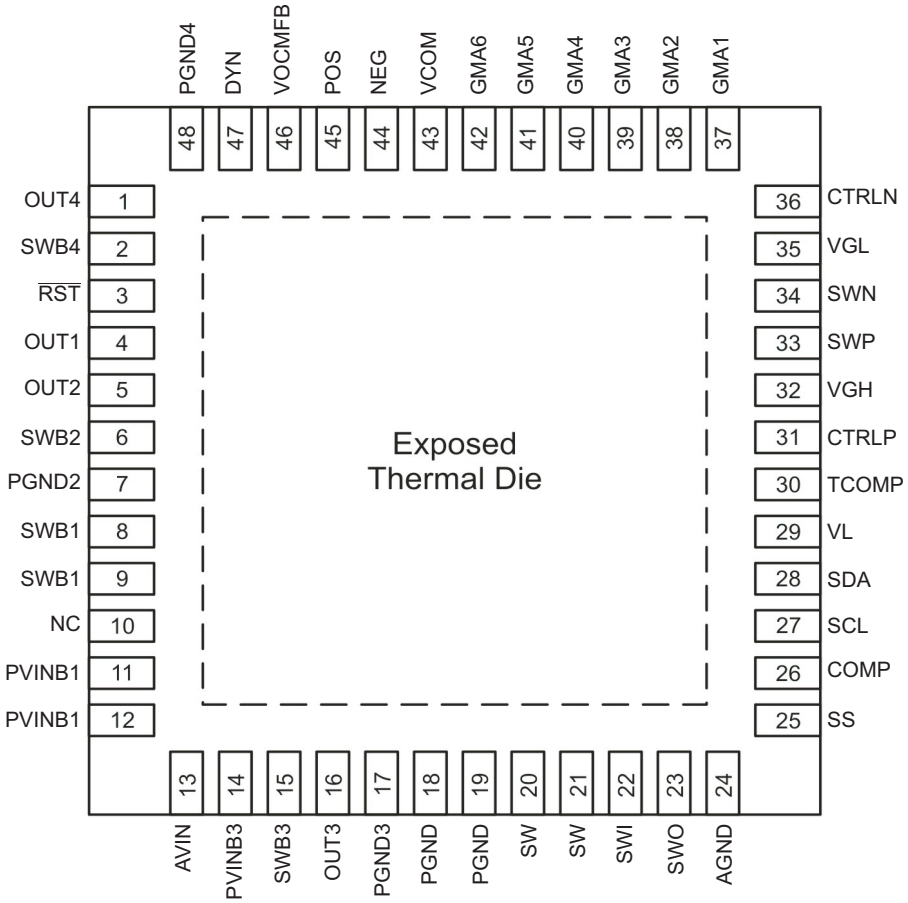


Figure 1. Serial Interface Timing for F/S-Mode

DEVICE INFORMATION



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT4	1	I	Buck 4 converter (V_{EPI}) output voltage sense pin
SWB4	2	I/O	Buck 4 converter (V_{EPI}) switch pin
$\overline{RST}$	3	O	Reset generator open drain output pin
OUT1	4	I	Buck 1 converter ($V_{CC)}$ output voltage sense pin. Buck 2 and buck 4 converters input pin
OUT2	5	I	Buck 2 converter (V_{CORE}) output voltage sense pin
SWB2	6	I/O	Buck 2 converter (V_{CORE}) switch pin
PGND2	7		Buck 2 converter ($V_{CORE)}$ power ground pin
SWB1	8, 9	I/O	Buck 1 converter (V_{CC}) switch pin
NC	10		Not connected
PVINB1	11, 12	I	Buck 1 converter (V_{CC}) input supply pin
AVIN	13	I	Internal regulator supply pin
PVINB3	14	I	Buck 3 converter (HV_{DD}) power input pin
SWB3	15	I/O	Buck 3 converter (HV_{DD}) switch pin
OUT3	16	I	Buck 3 converter (HV_{DD}) output voltage sense pin
PGND3	17		Buck 3 converter (HV_{DD}) power ground pin
PGND	18, 19		Boost converter (V_{DD}) power ground pin
SW	20, 21	I/O	Boost converter (V_{DD}) switch pin
SWI	22	I	Isolation switch input pin. The SWI pin is connected to the internal overvoltage protection comparator of the boost converter
SWO	23	O	Isolation switch output pin (V_{DD})
AGND	24, exposed pad		Analog ground pin. Connect this pin to the PowerPAD™.
SS	25	O	Boost converter (V_{DD}) soft-start pin. Connect a capacitor to this pin if a soft-start is needed. Open = no soft-start.
COMP	26	I/O	Boost converter (V_{DD}) compensation pin
SCL	27	I/O	I^2C clock pin
SDA	28	I/O	I^2C data pin
VL	29	O	Internal regulator output pin. Connect an output capacitor to this pin
TCOMP	30	I	Temperature compensation input pin. Connect the thermistor / pull-up resistor network to this pin
CTRLP	31	O	Positive charge pump (V_{GH}) base drive signal pin
VGH	32	I	Positive charge pump (V_{GH}) output voltage sense pin
SWP	33	I/O	Positive charge pump (V_{GH}) switch pin
SWN	34	I/O	Negative charge pump (V_{GL}) switch pin
VGL	35	I	Negative charge pump (V_{GL}) output voltage sense pin
CTRLN	36	O	Negative charge pump (V_{GL}) base drive signal pin
GMA1	37	O	Gamma buffer 1 output pin. DAC output
GMA2	38	O	Gamma buffer 2 output pin. DAC output
GMA3	39	O	Gamma buffer 3 output pin. DAC output
GMA4	40	O	Gamma buffer 4 output pin. DAC output
GMA5	41	O	Gamma buffer 5 output pin. DAC output
GMA6	42	O	Gamma buffer 6 output pin. DAC output
VCOM	43	I	V_{COM} output sense pin
NEG	44	O	V_{COM} inverting pin
POS	45	O	V_{COM} non-inverting pin. DAC output for the V_{COM} reference
VCOMFB	46	I	V_{COM} panel feedback pin
DYN	47	I	Dynamic V_{COM} gain select pin
PGND4	48		Buck 4 converter (V_{EPI}) power ground pin

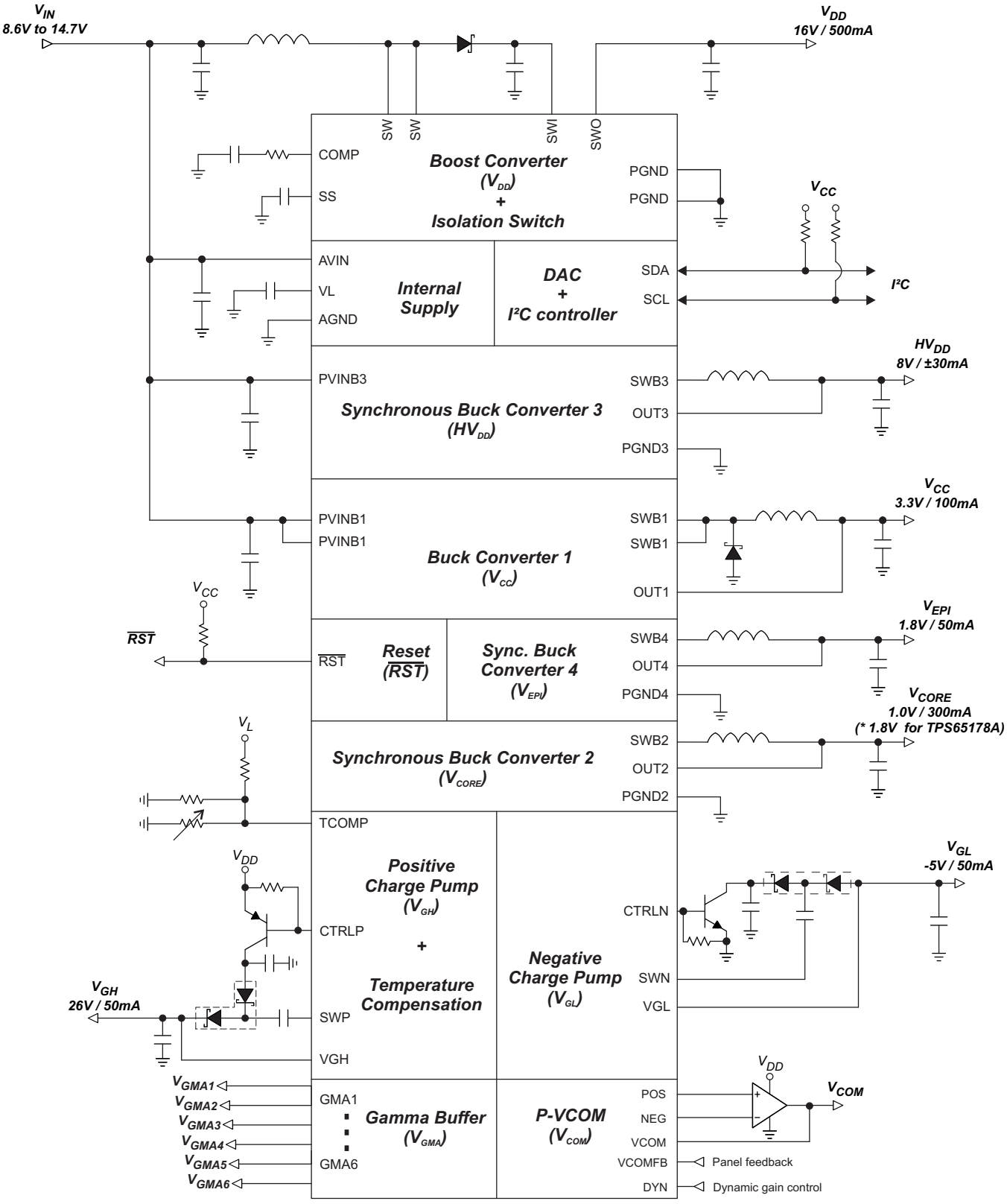


Figure 2. Simple Application Schematic

TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

PARAMETER	Conditions	Figure
Buck 1 Converter - (V_{IN} = 12 V, L = 10 µH, C_{OUT} = 40 µF)		
Efficiency vs. Load Current	V_{CC} = 3.3 V	Figure 3
PWM Switching – Light Load	V_{CC} = 3.3 V/50 mA	Figure 4
PWM Switching – Heavy Load	V_{CC} = 3.3 V/ 500 mA	Figure 5
Load Transient Response	V_{CC} = 3.3 V/100 ~ 300 mA	Figure 6
Buck 2/4 Converters - (V_{IN} = 12 V, L = 2.2 µH, C_{OUT} = 10 µF)		
Efficiency vs. Load Current	$V_{CORE/EPI}$ = 1.0 V, 1.2 V, 1.5 V, 1.8 V	Figure 7
PWM Switching – Light Load	$V_{CORE/EPI}$ = 1.0 V/0 A	Figure 8
PWM Switching – Heavy Load	$V_{CORE/EPI}$ = 1.0 V/500 mA	Figure 9
Load Transient Response	$V_{CORE/EPI}$ = 3.3 V/100~ 400 mA	Figure 10
Buck 3 Converter - (V_{IN} = 12 V, L = 6.8 µH, C_{OUT} = 10 µF)		
Efficiency vs. Load Current	HV_{DD} = 8 V	Figure 11
PWM Switching – Light Load	HV_{DD} = 8 V/0 A	Figure 12
PWM Switching – Heavy Load (Source)	HV_{DD} = 8 V/500 mA	Figure 13
PWM Switching – Heavy Load (Sink)	HV_{DD} = 8 V/–500 mA	Figure 14
Load Transient Response	HV_{DD} = 3.3 V/–200 ~ +200 mA	Figure 15
Boost Converter - (V_{IN} = 12 V, L = 10 µH, C_{OUT} = 40 µF)		
Efficiency vs. Load Current	V_{DD} = 16 V	Figure 16
PWM Switching – Light Load	V_{DD} = 16 V/0 A	Figure 17
PWM Switching – Heavy Load	V_{DD} = 16 V/ 700 mA	Figure 18
Load Transient Response	V_{DD} = 16 V/ 200 ~ 550 mA	Figure 19
Positive Charge Pump - (V_{IN} = 12 V, C_{OUT} = 10 µF)		
Load Transient Response	V_{GH} = 26 V/ 10 ~ 60 mA	Figure 20
Negative Charge Pump - (V_{IN} = 12 V, C_{OUT} = 10 µF)		
Load Transient Response	V_{IN} = 12 V, V_{GL} = –5 V/ 10 ~ 50 mA	Figure 21
Temperature Compensation		
Voltage Adjustment - [–2°C ~ 25°C)	V_{GH_LT1} = 34 V, V_{GH_HT1} = 17 V V_{GH_LT2} = 27 V, V_{GH_HT2} = 24 V	Figure 22
Temperature Adjustment V_{GH_LT} = 28 V, V_{GH_HT} = 22 V	T°C Variation1: 2 °C ~ 18 °C T°C Variation2: 16 °C ~ 32 °C	Figure 23
Sequencing		
Power On Sequencing	V_{IN} = 12 V, V_{LOGIC} = 3.3 V, V_{GL}= –5 V V_{DD}= 16 V, HV_{DD} = 8 V, V_{GH} = 26 V	Figure 24
Power On Sequencing V_{LOGIC}	V_{IN} = 12 V, V_{CC} = 3.3 V, V_{CORE} = 1.8 V, V_{CORE} = 1.0 V	Figure 25
Power On Sequencing V_{DD} dependency	V_{IN} = 12 V, V_{DD} = 16 V, V_{GMA1} = 14 V HV_{DD} = 8 V, V_{POS} = 6.5 V, V_{GMA6} = 2 V	Figure 26

BUCK 1 (V_{CC}) EFFICIENCY vs LOAD CURRENT

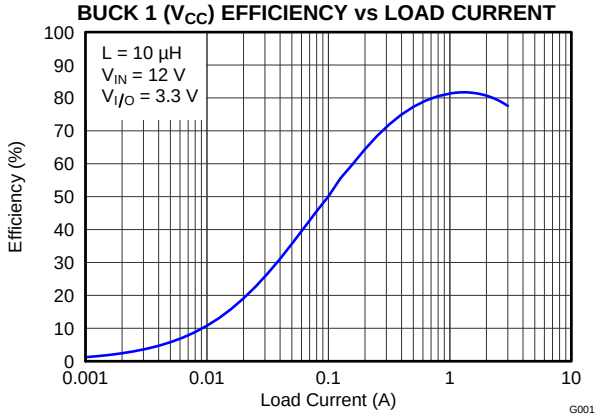


Figure 3.

BUCK 1 (V_{CC}) PWM SWITCHING – LIGHT LOAD

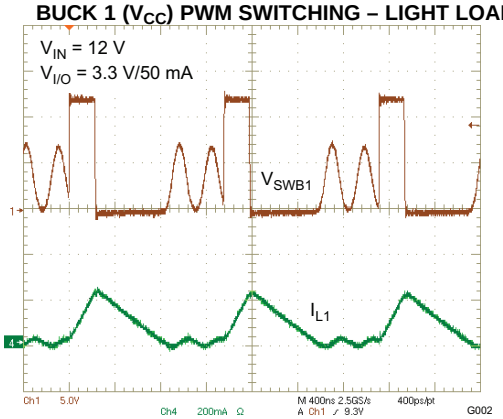


Figure 4.

BUCK 1 (V_{CC}) PWM SWITCHING – HEAVY LOAD

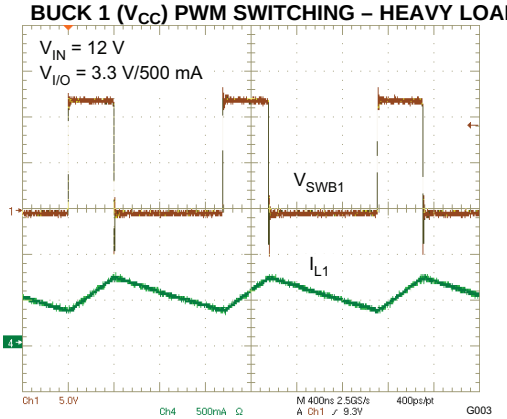


Figure 5.

BUCK 1 (V_{CC}) LOAD TRANSIENT RESPONSE

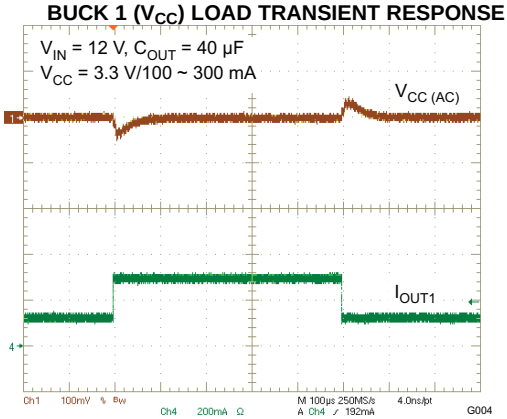


Figure 6.

BUCK 2 (V_{CORE}) EFFICIENCY vs LOAD CURRENT

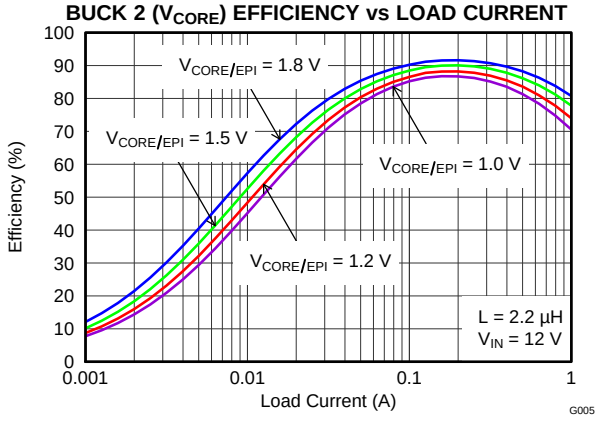


Figure 7.

BUCK 2 (V_{CORE}) PWM SWITCHING – LIGHT LOAD

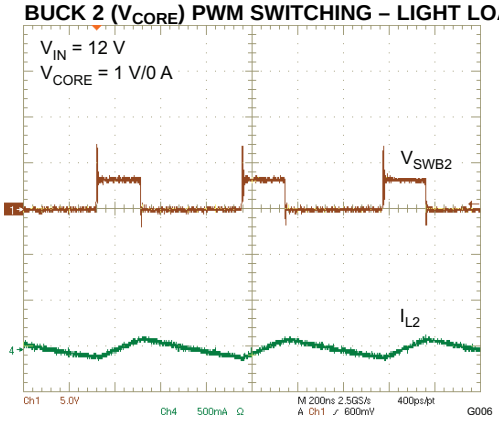


Figure 8.

BUCK 2 (V_{CORE}) PWM SWITCHING – HEAVY LOAD

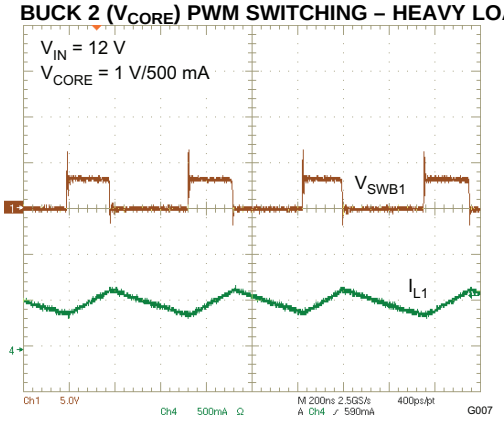


Figure 9.

BUCK 2 (V_{CORE}) LOAD TRANSIENT RESPONSE

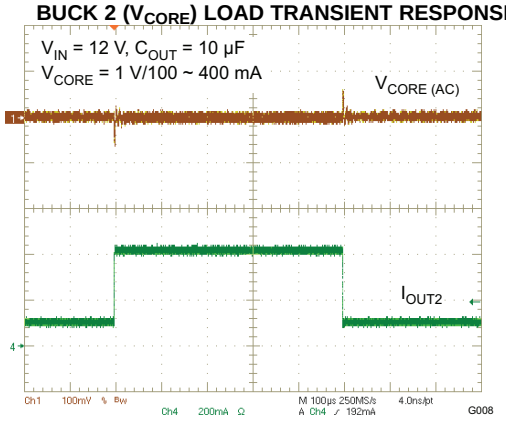


Figure 10.

BUCK 3 (HV_{DD}) EFFICIENCY vs LOAD CURRENT

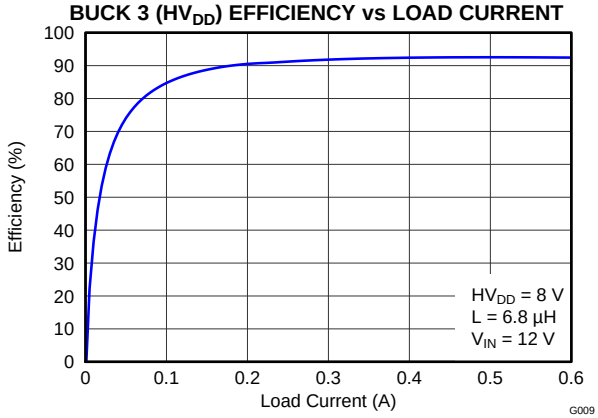


Figure 11.

BUCK 3 (HV_{DD}) PWM SWITCHING - LIGHT LOAD

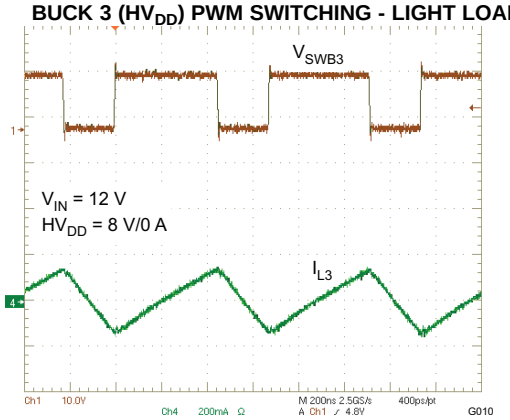


Figure 12.

BUCK 3 (HV_{DD}) PWM SWITCHING – HEAVY LOAD (SOURCE)

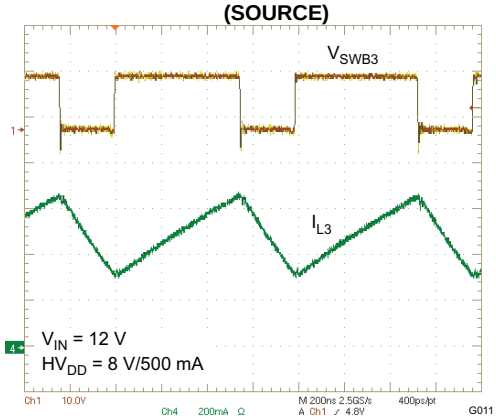


Figure 13.

BUCK 3 (HV_{DD}) PWM SWITCHING – HEAVY LOAD (SINK)

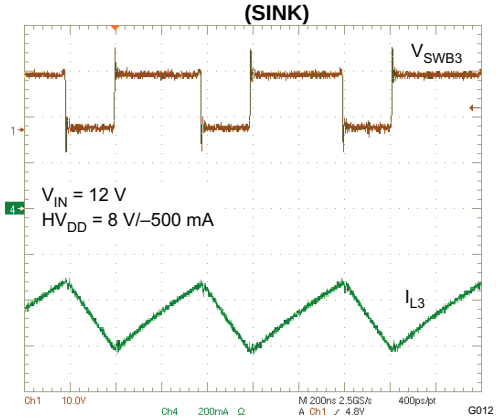


Figure 14.

BUCK 3 (HV_{DD}) LOAD TRANSIENT RESPONSE

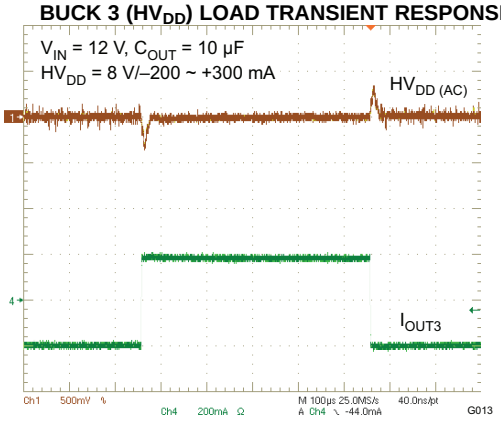


Figure 15.

BOOST (V_{DD}) EFFICIENCY vs LOAD CURRENT

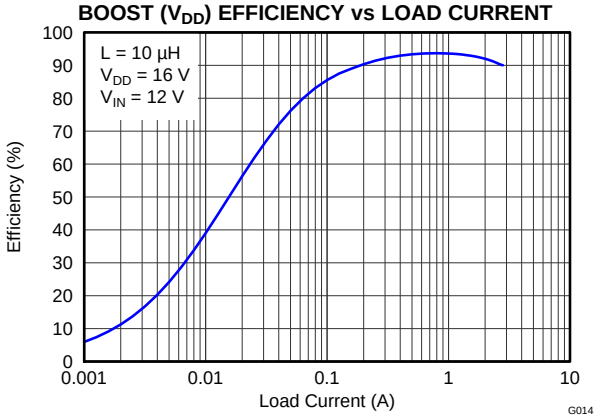


Figure 16.

BOOST (V_{DD}) PWM SWITCHING – LIGHT LOAD

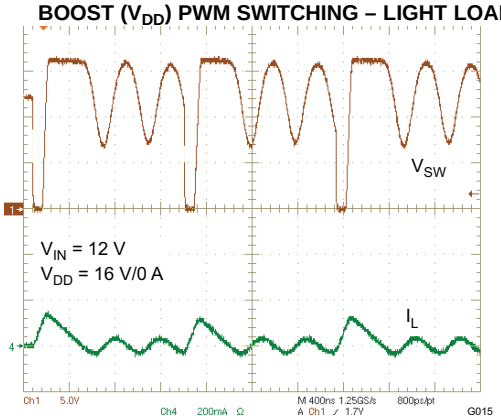


Figure 17.

BOOST (V_{DD}) PWM SWITCHING – HEAVY LOAD

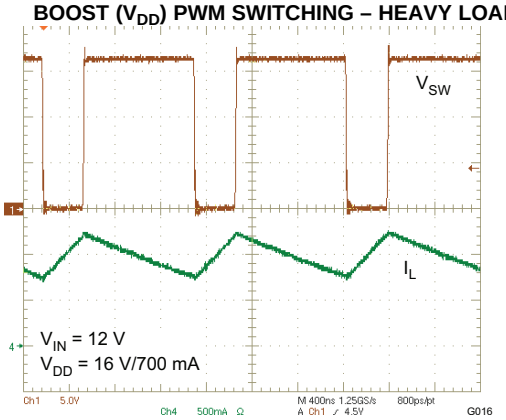


Figure 18.

BOOST (V_{DD}) LOAD TRANSIENT RESPONSE

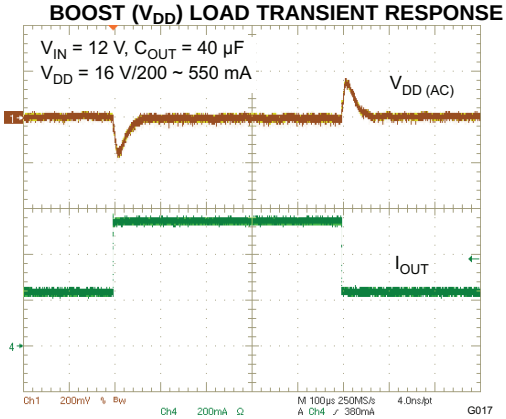


Figure 19.

CPP (V_{GH}) LOAD TRANSIENT RESPONSE

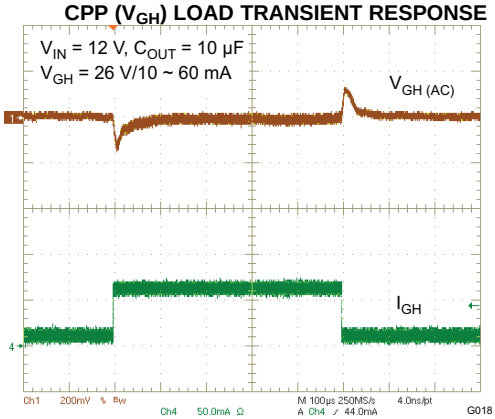


Figure 20.

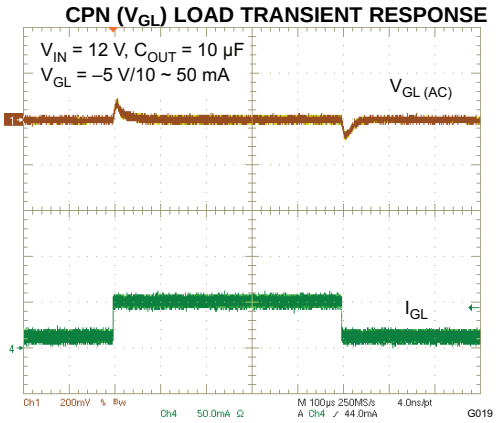


Figure 21.

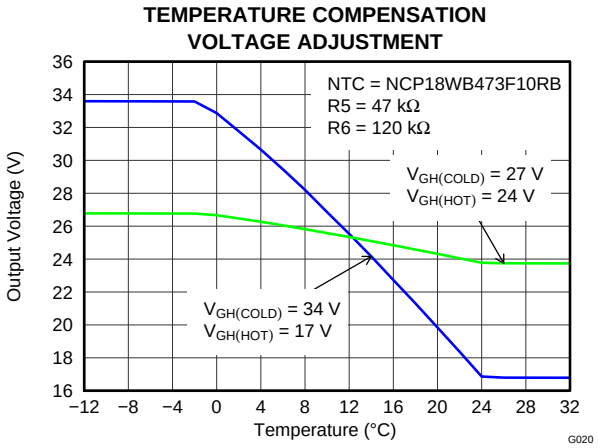


Figure 22.

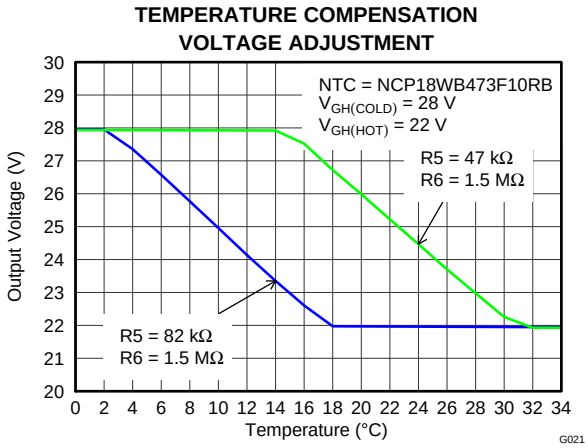


Figure 23.

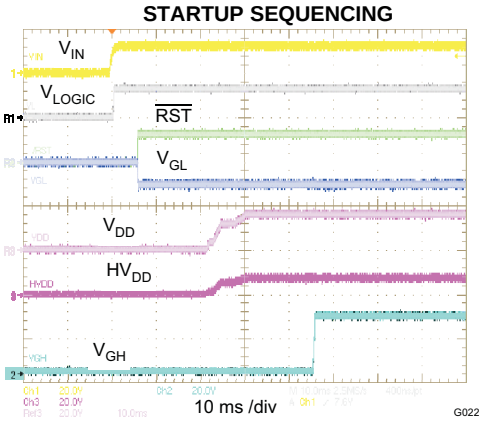


Figure 24.

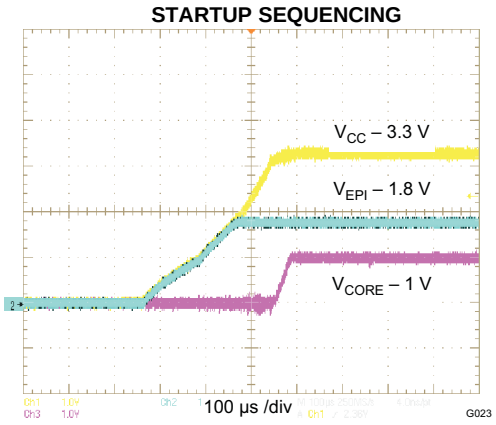


Figure 25.

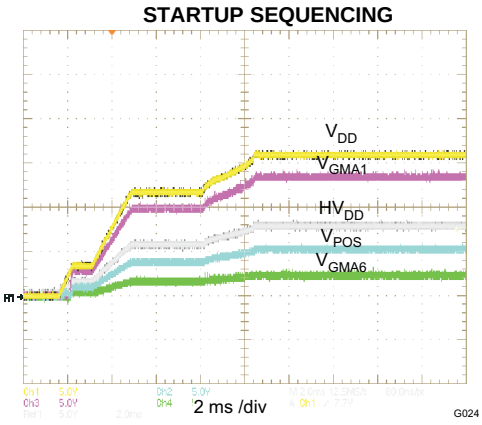


Figure 26.

DAC RANGE SUMMARY

All outputs are programmable using a two-wire interface.

Boost Converter (V_{DD})

Output voltage selection: programmable with I^2C
Number of bits: 6
Output voltage range: 12.8V…19V
Step size: 100 mV

Buck 1 Converter (V_{CC})

Output voltage selection: programmable with I^2C
Number of bits: 3
Output voltage range: 3.0V…3.7V
Step size: 100 mV

Buck 2 Converter (V_{CORE})

Output voltage selection: programmable with I^2C
Number of bits: 4
Output voltage range: 0.9V…2.4V
Step size: 100 mV

Buck 3 Converter (HV_{DD})

Output voltage selection: not possible (V_{DD} tracking)
Number of bits: -
Output voltage range: $V_{DD}/2$
Step size: 50 mV

Buck 4 Converter (V_{EPI})

Output voltage selection: programmable with I^2C
Number of bits: 4
Output voltage range: 0.9V…2.4V
Step size: 100 mV

Positive Charge Pump Controller (V_{GH_LT} – low temperature)

Output voltage selection: programmable with I^2C
Number of bits: 4
Output voltage range: 19V…34V
Step size: 1 V

Positive Charge Pump Controller (V_{GL_HT} - high temperature)

Output voltage selection: programmable with I^2C
Number of bits: 4
Output voltage range: 17V…32V
Step size: 1 V

Negative Charge Pump (V_{GL})

Output voltage selection: programmable with I^2C
Number of bits: 4
Output voltage range: –1.8V…–8.1V
Step size: 100 mV

Gamma Buffer ($V_{GMA1,2,3}$) - (V_{DD} dependency)

Output voltage selection: programmable with I^2C
Number of bits: 9
Output voltage range: $V_{DD}/2 \ldots V_{DD}$ (512 steps)
Step size: $V_{DD}/1023$

Gamma Buffer ($V_{GMA4,5,6}$) - (V_{DD} dependency)

Output voltage selection: programmable with I^2C
Number of bits: 9
Output voltage range: $0V \ldots V_{DD}/2$ (512 steps)
Step size: $V_{DD}/1\text{-}23$

Vcom Reference (V_{POS}) - (V_{DD} dependency)

Output voltage selection: programmable with I^2C
Number of bits: 9
Output voltage range: $(V_{DD}/1023)*250V \ldots (V_{DD}/1023)*640V$ (391 steps)
Step size: $V_{DD}/1023$

Vcom Fixed Gain

Gain voltage selection: programmable with I^2C
Number of bits: 2
Gain levels: Buffer, –1x,–2x,–3x

Vcom Dynamic Gain

Gain voltage selection: logic levels on DYN pin (driven by T-CON)
Number of bits: 1
Gain levels: –2x, –4x
DYN = high: –2x
DYN = low: –4x

SEQUENCING

The power-up sequence delays are programmable with a I^2C. DLY1, DLY2 and DLY3 can be set per steps of 5 ms, up to 35 ms.

DLY1, 2, 3

Number of bits: 3

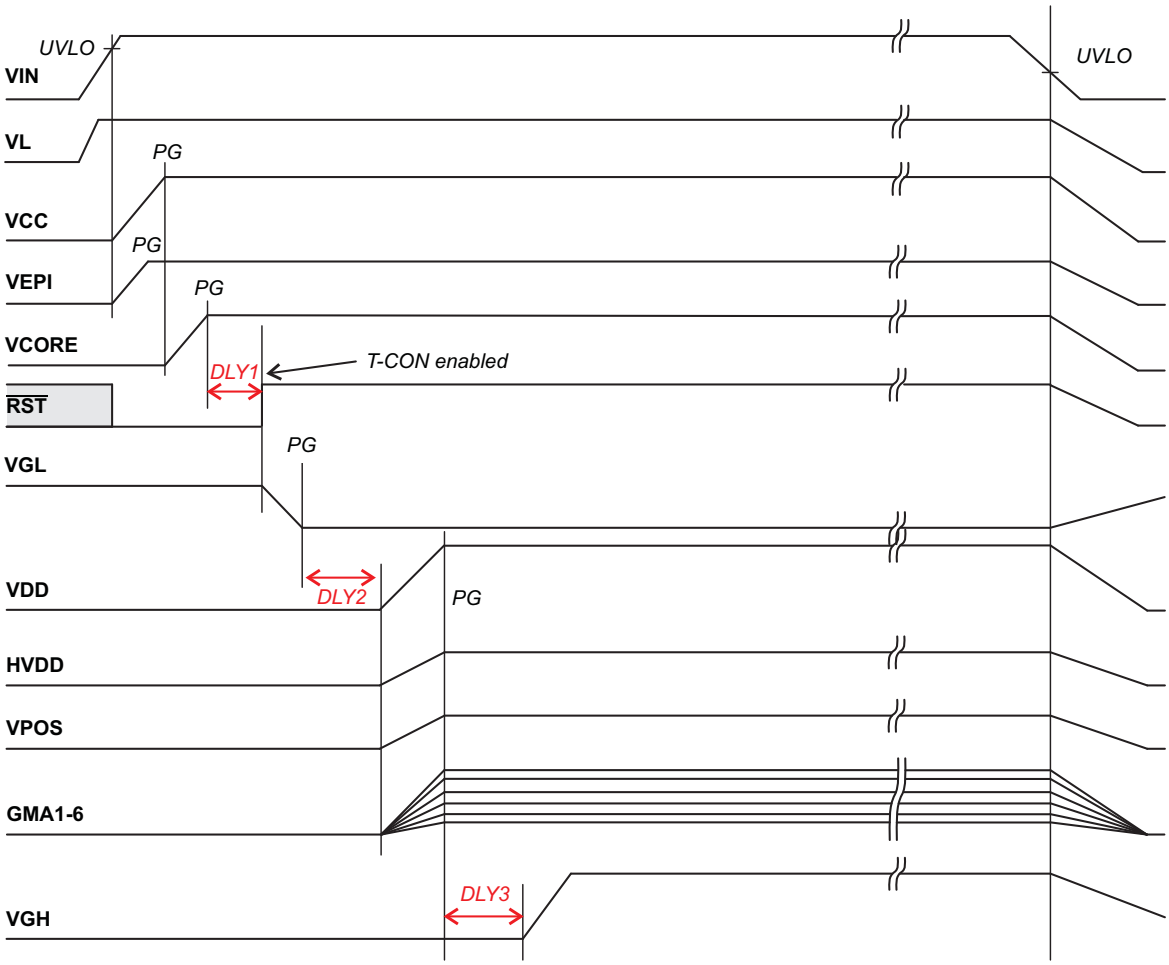
Timing delay range: 0ms…35ms (± 20% accuracy)

POWER-UP

1. When AV_{IN} > 8.6 V the device is enabled, V_L goes into regulation and the $\overline{RST}$ signal is set 'low'. The buck 1 (V_{CC}) **and** buck 4 (V_{EPI}) converters start up.
2. When PG1 and PG4 are reached, buck 2 (V_{CORE}) strarts up.
3. When PG2 is reached **and** DLY1 has passed, $\overline{RST}$ is released **and** the negative charge pump controller (V_{GL}) starts.
4. When PGN is reached **and** DLY2 has passed, the boost converter (V_{DD}) **and** the buck 3 converter (HV_{DD}) start. The Gamma Buffer outputs as well as the V_{POS} rise at a ratio metric rate of V_{DD}.
5. When PG is reached **and** DLY3 has passed, the positive charge pump controller (V_{GH}) starts.

POWER-DOWN

1. When V_{IN} falls down below the UVLO threshold, all blocks are disabled and discharge at a rate driven by the output load and the output capacitors.



DETAILED DESCRIPTION

BOOST CONVERTER (V_{DD})

The non-synchronous boost converter uses a current mode topology and operates at a fixed frequency of 600 kHz. A typical application circuit is shown in Figure 30. The external compensation allows designers to optimize the performance for individual applications, and is easily implemented by connecting a suitable capacitor/resistor network between the COMP pin and AGND (see design procedure section for more details).

Enable Signal (DLY2)

The boost converter is enabled when the power good signal from the negative charge pump controller (V_{GL}) is asserted and the programmed DLY2 has passed (see the *Appendix* section to set DLY2 timing).

Boost Converter Operation

The boost operates either in continuous conduction mode (CCM) or discontinuous conduction mode (DCM), depending on the load current. The switch node waveforms for CCM and DCM operation are shown in Figure 4 and Figure 5. Note that the ringing seen during DCM operation (at light load) occurs because of parasitic capacitance in the PCB layout and is normal for DCM operation. There is very little energy contained in the ringing waveform and it does not significantly affect EMI performance.

Startup (Boost Converter)

The startup of the boost converter block operates in two steps:

1. **Input-to-output isolation switch (IsoFET)**

   As soon as the internal enable signal of the boost converter is activated, the isolation switch is slowly turned on, ramping up smoothly the current flowing from V_{IN} into the output capacitors. The startup current is limited to 200 mA typically until V_{SWO} > 3.5 V (short-circuit condition), and increases linearly with the output voltage. Once V_{SWO} gets close to V_{SWI}, the isolation switch is fully turned on and the boost converter starts switching. The soft-start function is also enabled.

2. **Soft-start (SS)**

   To minimize the inrush current during start-up an external capacitor connected to the soft-start pin SS is used to slowly ramp up the internal current limit of the boost converter. It is charged with a constant current of typically 10 µA. The inductor peak current limit is proportional to the SS voltage and the maximum load current is available after the soft-start is completed (V_{SS} = 0.8 V) or V_{DD} has reached its Power Good value (90% of its nominal voltage). The larger the SS capacitor, the slower the ramp of the current limit and the longer the soft-start time. A 100-nF capacitor is usually sufficient for most applications. When V_{IN} decreases below the undervoltage lockout threshold, the soft-start capacitor is discharged to ground.

Protections (Boost Converter)

The boost converter is protected against potentially damaging conditions such as overvoltage and short circuits.

1. **Short-Circuit Protection**

   The boost converter integrates a short-circuit protection circuit to prevent the inductor or the rectifier diode from overheating when the output rail is shorted to GND. If the boost output is shorted to GND and the voltage on SWO drops below V_{IN} - 0.5 V, the boost converter shuts down and the input-to-output isolation is turned-off. Only when the SWO voltage drops below 2 V typically, the switch turns on again and limits the current to 200 mA typically (start-up behavior). The soft-start capacitor is also discharged to ground.

2. **Overvoltage Protection**

   The boost converter integrates an overvoltage protection. If the output voltage V_{DD} exceeds the OVP threshold of 20.3 V typically , the boost converter stops switching. The output voltage will drop down by the hysteresis and the boost converter will autonomously recover and switch again.

NOTE

The boost converter stops switching while the positive charge pump is in a short circuit condition. This condition is not latched and the boost converter autonomously resumes normal operation once the short circuit condition has been removed from the positive charge pump.

Setting the Output Voltage V_{DD}

The output voltage of the boost converter is programmable via a two-wire interface between 12.8 V and 19 V with a 6-bit resolution. See the *Appendix* section to set the V_{DD} voltage.

Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency number from the provided efficiency curves at the application's maximum load or to use a worst case assumption for the expected efficiency, e.g., 85%.

1. Duty Cycle: $D = 1 - \frac{V_{IN\_min} \times \eta}{V_S}$
2. Inductor ripple current: $\Delta I_L = \frac{V_{IN\_min} \times D}{f_{OSC} \times L}$
3. Maximum output current: $I_{OUT\_max} = \left(I_{LIM\_min} - \frac{\Delta I_L}{2} \right) \times (1 - D)$
4. Peak switch current of the application: $I_{SWPEAK} = \frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2}$

η = Estimated boost converter efficiency (use the number from the efficiency plots or 85% as an estimation)
f_{OSC} = Boost converter switching frequency (600 kHz)
L = Selected inductor value for the boost converter (see the Inductor Selection section)
I_{SWPEAK} = Boost converter switch current at the desired output current (must be < I_{LIM_min} = 3.5 A)
ΔI_L = Inductor peak-to-peak ripple current

The peak switch current is the current that the integrated switch, the inductor and the external Schottky diode have to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest.

Inductor Selection (Boost Converter)

Saturation current: the inductor must handle the maximum peak current ($I_{L\_SAT} > I_{SWPEAK}$, or $I_{L\_SAT} > I_{LIM\_max}$ as conservative approach)

DC Resistance: the lower the DCR, the lower the losses

Inductor value: with a fixed frequency of 600 kHz, the recommended values are 10 µH ≤ L ≤ 22 µH. The boost converter is optimized to work with 10 µH. The higher the inductor value, the lower the inductor ripple and output voltage ripple but the slower the transient response.

Table 2. Inductor Selection Boost / Buck 1

L (µH)	SUPPLIER	COMPONENT CODE	SIZE (L x W x H mm)	DCR TYP (mΩ)	I_{SAT} (A)
10	Sumida	CDRH8D43NP-100N	8.3 x 8.3 x 4.5	29	4
10	Murata	LQH6PPN100M43K	6.0 x 6.0 x 4.3	53	2.6
22	Sumida	CD105NP-100M	10.4 x 9.4 x 5.8	60	2.6
22	Sumida	CDRH129-220M	12.5 x 12.5 x 10	23	5

Rectifier Diode Selection (Boost Converter)

Diode type: Schottky type for better efficiency

Reverse voltage: V_R of the diode must block V_{OVP} voltage (20 V recommended)

Forward current: the diode's averaged rectified forward current I_F must handle the output current since $I_F = I_{OUT}$ (2A recommended as conservative approach, 1A sufficient for lower output current).

Thermal characteristics: the diode must be chosen so that it can dissipate the power ($P_D = I_F \times V_F$, 500 mW should be sufficient for most of the applications)

Table 3. Rectifier Diode Selection Boost / Buck 1

PART NUMBER	V_R / I_{AVG}	V_F	$R_{\theta JA}$	SIZE	COMPONENT SUPPLIER
MBRS320	20V / 3A	0.44V at 3A	46°C/W	SMC	International Rectifier
SL22	20V / 2A	0.44V at 2A	75°C/W	SMB	Vishay Semiconductor
SS22	20V / 2A	0.50V at 2A	75°C/W	SMB	Fairchild Semiconductor

Compensation (COMP)

The regulation loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. The compensation capacitor will adjust the low frequency gain and the resistor value will adjust the high frequency gain. Lower output voltages require a higher gain and therefore a lower compensation capacitor value. A good start, that will work for the majority of the applications is R_{COMP} = 33 kΩ and C_{COMP} = 1 nF. In the case where a 22 uH inductor is used, R_{COMP} = 22 kΩ and C_{COMP} = 1 nF are recommended.

Input Capacitor Selection

For good input voltage filtering low ESR ceramic capacitors are recommended. TPS65178/A has an analog input AVIN. A 1-µF bypass capacitor is required as close as possible from AVIN to GND.

Two 10-µF (or one 22-µF) ceramic input capacitors are sufficient for most applications. For better input voltage filtering this value can be increased. Refer to the *Recommended Operation Conditions* table, Table 4 and the *Typical Application* section for input capacitor recommendations.

Output Capacitor Selection

For best output voltage filtering a low ESR output capacitor is recommended. Typically, four 10-µF (or two 22-µF) ceramic output capacitors work for most of the applications. Higher capacitor values can be used to improve the load transient response. *A 10 µF capacitor is also required between the rectifier diode and the SWI pin* (Refer to the *Recommended Operation Conditions* table, Table 4 and the *Typical Application* section for output capacitor recommendations).

Table 4. Input and Output Capacitor Selection Boost / Buck 1

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMPONENT CODE	COMMENTS
1µF/0603	16V	Taiyo Yuden	EMK107BJ105KA	AVIN bypass
10µF/1206	16V	Taiyo Yuden	EMK212BJ106KG	C_{IN}
10µF/1206	25V	Taiyo Yuden	TMK316BJ106KL	C_{OUT}
22µF/1210	25V	Murata	GRM32ER61E226KE15	C_{IN} / C_{OUT}

To calculate the output voltage ripple, the following equations can be used:

$$\Delta V_C = \frac{V_{DD} - V_{IN}}{V_{DD} \times f_{OSC}} \times \frac{I_{OUT}}{C_{OUT}} \qquad \Delta V_{C\_ESR} = I_{SWPEAK} \times R_{C\_ESR} \tag{1}$$

ΔV_{C_ESR} can be neglected in many cases since ceramic capacitors provide very low ESR.

BUCK 1 CONVERTER (V_{CC})

The buck 1 converter (step-down) used in TPS65178/A is a non-synchronous type current mode control that runs at a fixed frequency of 600kHz. The converter features integrated soft-start, bootstrap, and compensation circuits to minimize external component count.

Enable Signal (UVLO)

The buck 1 converter is enabled when the VIN voltage exceeds the UVLO threshold of 8.3 V typically.

Buck 1 Converter Operation

The buck 1 operates in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM), depending on the load current. The switch node waveforms for CCM and DCM operation are shown in Figure 4 and Figure 5. Note that the ringing seen during DCM operation (at light load) occurs because of parasitic capacitance in the PCB layout and is normal for DCM operation. There is very little energy contained in the ringing waveform and it does not significantly affect EMI performance.

The buck 1 converter uses a *skip* mode to regulate V_{CC} at very low load currents. This mode allows the converter to maintain its output at the required voltage while still meeting the requirement of a *minimum on time*. During skip mode, the buck 1 converter switches for a few cycles, then stops switching for a few cycles, and then starts switching again and so on, for as long as the output current is below the skip mode threshold. Output voltage ripple can be a little higher during skip mode.

Startup and Short Circuit Protection (Buck 1 Converter)

The buck 1 converter is limiting its switching frequency when its output voltage V_{CC} is below a certain threshold (f_{SWB1} = 1/4 × fosc for $V_{FB\_internal}$ < 400mV and f_{SWB1} = ½ × fosc for $V_{FB\_internal}$ < 800mV - with V_{REF} = 1.24 V). This feature avoids run away of the inductor in case of short circuit and helps smoothing the buck converter startup as well.

Setting the Output Voltage V_{CC}

The output voltage of the buck 1 converter is programmable via a two-wire interface between 3.0 V and 3.7 V with a 3-bit resolution. See the *Appendix* section to set the V_{CC} voltage.

Buck 1 Converter Design Procedure

1. Duty Cycle: $D = \frac{V_{CC}}{V_{IN} \times \eta}$
2. Inductor ripple current: $\Delta I_L = \frac{(V_{IN\_max} - V_{CC}) \times D}{f_{OSC} \times L}$
3. Maximum output current: $I_{CC\_max} = I_{LIM\_min} - \frac{\Delta I_L}{2}$
4. Peak switch current: $I_{SWPEAK} = I_{CC\_max} + \frac{\Delta I_L}{2}$

   η = Estimated buck 1 converter efficiency (use the number from the efficiency plots or 85% as an estimation)
   f_{OSC} = Buck 1 converter switching frequency (600 kHz)
   L = Selected inductor value for the boost converter (see the Inductor Selection section)
   I_{SWPEAK} = Buck 1 converter switch current (must be < I_{LIM_min} = 2.6 A)
   ΔI_L = Inductor peak-to-peak ripple current

Inductor Selection (Buck 1 Converter)

Refer to the boost converter *Inductor Selection*.

Inductor value: as for the boost converter, the buck 1 converter is designed to work with an inductor range as 10 µH ≤ L ≤ 22 µH. The buck 1 converter is optimized to work with 10 µH.

Rectifier Diode Selection (Buck 1 Converter)

Refer to the boost converter rectifier *Diode Rectifier Selection*.

Input Capacitor Selection (Buck 1 Converter)

Two 10-µF (or one 22-µF) ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering this value can be increased. Refer to the *Recommended Operation Conditions* table, Table 4 and the *Typical Application* section for input capacitor recommendations.

Output Capacitor Selection (Buck 1 Converter)

For best output voltage filtering a low ESR output capacitor is recommended. Typically, four 10-µF (or two 22-µF) ceramic output capacitors work for most of the applications. Higher capacitor values can be used to improve the load transient response. Refer to the *Recommended Operation Conditions* table, Table 4 and the *Typical Application* section for input capacitor recommendations.

BUCK 2 & 4 CONVERTER (V_{CORE} & V_{EPI})

The TPS65178/A integrates two synchronous buck converters (step-down) 2 and 4 that include a unique hysteric PWM controller scheme which enables switching frequencies over 3MHz, excellent transient and ac load regulation as well as operation with tiny and cost competitive external components like chip inductors. The TPS65178/A's buck 2 and 4 converters offer adjustable output voltage down to 0.9 V, ideal to support the most recent timing controllers and panel interfaces. The internal switch current limit of 1.1 A minimum supports output currents of up to 1 A for the buck 2 and a lower limit to support current up to 400 mA for the buck 4. .

Enable Signal (UVLO & Power Good)

The buck 4 converter is enabled together with the buck 1 converter when the VIN voltage exceeds the UVLO threshold of 8.3 V typically. The buck 2 converter is enabled with the power good signals of the buck 2 and 4.

Buck 2 & 4 Converter Operation

The converters operate in a hysteretic mode. The high side transistor (PMOS) remains turned on until a minimum on time of $t_{ON\ min}$ expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high side switch current limit. Once the high side switch turns off, the low side switch rectifier is turned on and the inductor current ramps down. As the output voltage falls below the threshold of the error comparator, a switch pulse is initiated and the high side switch is turned on again. If the inductor current falls down to zero, will continue operating with $t_{ON\ min}$ and $t_{OFF\ min}$ in order to maintain the proper output voltage.

Startup and Short Circuit Protection (Buck 2 & 4 Converters)

The buck 4 converter tracks the buck 1 converter output voltage during startup until it has reached its programmed value. The buck 2 converter starts operation after the Power Good signals of buck 1 and 4 converters have been asserted. In the event of a short circuit, the converters will operate with maximum duty cycle and the output current will be limited by the internal current limit.

Startup Sequence (Buck 1, 2 & 4)

As the buck 1 supplies the inputs of buck 2 and buck 4 via the OUT1 pin, it is not possible to have V_{CORE} or V_{EPI} exceeding their input voltage V_{CC}. Buck 4 and buck 1 start simultaneously and buck 4 operates with maximum duty cycle during startup (it behaves as a LDO) until V_{EPI} has reached its programmed value. Buck 2 will only start when buck 1 and buck 4 Power Good signals have been asserted by reaching their target values.

The startup durations depending on output load, output capacitance, inductor value, input voltage and output voltage, a typical example can be seen on Figure 25 (refer to the typical application conditions on Figure 30 for the external components used - no output load on this measurement).

Buck 2 or Buck 4 Not used

In the case where buck 2/4 are not used (one or both of them), the following connections need to be made: OUT2/4 = OUT1 and SWB2/4 = PGND2/4 = N.C. This will ensure that both converters will generate their Power Good signal allowing the rest of the sequencing to happen ($\overline{RST}$ and Negative Charge Pump).

Setting the Output Voltage V_{CORE} & V_{EPI}

The output voltages of the buck 2 and 4 converters are programmable via a two-wire interface between 0.9 V and 2.4 V with a 4-bit resolution. See the *Appendix* section to set the V_{CORE} voltage.

Buck 2 and 4 Converter Design Procedure

V_{EPI} output voltage can be calculated using the following equations by replacing V_{CORE} values.

1. Duty Cycle: $D = \frac{V_{CORE}}{V_{CC} \times \eta}$
2. Inductor ripple current: $\Delta I_L = \frac{V_{CC} - V_{CORE}}{L} \times t_{ON} = \frac{V_{CC} - V_{CORE}}{L \times f} \times D$
3. Maximum output current: $I_{CORE\_max} = I_{LIM\_min} - \frac{\Delta I_L}{2}$
4. Peak switch current: $I_{SWPEAK} = I_{CORE\_max} + \frac{\Delta I_L}{2}$

η = Estimated buck 2 converter efficiency (use the number from the efficiency plots or 80% as an estimation)

f = Buck 2 converter switching frequency $f_{SW2} = \frac{V_{CORE} \times (1\text{-}D)}{0.37e^{-6}}$

L = Selected inductor value for the buck 2 converter (see the Inductor Selection section)

I_{SWPEAK} = Buck 2 converter switch current (must be < I_{LIM_min} = 1.1 A)

ΔI_L = Inductor peak-to-peak ripple current

The peak switch current is the steady state current that the integrated switches and the inductor have to be able to handle.

Inductor Selection (Buck 2 & 4 Converter)

Refer to the boost converter inductor selection.

Inductor value: the buck 2 and 4 converters are designed to work with small inductors in the following range: 1.0 µH ≤ L ≤ 2.2 µH. The buck 2 and 4 converters are optimized to work with 2.2 µH.

Table 5. Inductor Selection Buck 2 and 4 (Chip Inductors)

L (µH)	SUPPLIER	COMPONENT CODE	SIZE (LxWxH mm)	DCR TYP (mΩ)	I_{SAT} (A)
2.2	Murata	LQM21PN2R2	2 x 1.2 x 0.55	340	0.6
2.2	FDK	MPSZ2012D2R2	2 x 1.2 x 1	230	0.7
1.0	FDK	MIPSZ2012D1R0	2 x 1.2 x 1	90	1.1
2.2	Murata	LQM2HPN2R2MG0	2.5 x 2 x 1	80	1.3
1.0	Murata	LQM2HPN1R0MG0	2.5 x 2 x 1	90	1.5

Input Capacitor Selection

Because of the nature of the buck 2 and 4 converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications a minimum of 1 µF ceramic capacitor is recommended. The input capacitor connected as close as possible to the IC on OUT1 pin can be increased without any limit for better input voltage filtering. Refer to Table 6 for the selection of the filtering capacitors.

Output Capacitor Selection

The unique hysteric PWM control scheme of the TPS65178/A's buck 2 converter allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. Refer to Table 6 for the selection of the output capacitors.

Table 6. Input and Output Capacitor Selection Buck 2 and 4

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMPONENT CODE	COMMENTS
1µF/0603	16V	Taiyo Yuden	EMK107 BJ 105KA	C_{IN}
4.7µF/0603	10V	Taiyo Yuden	LMK107 BJ 475KA	C_{IN}
4.7µF/0603	6.3V	Taiyo Yuden	JMK107 BJ 475_A	C_{OUT}

Note: If the buck 2 or 4 are not used, OUT2 (pin 5) or OUT4 (pin 1) must be connected to OUT1 (pin 4) for proper startup.

BUCK 3 CONVERTER (HV_{DD})

The TPS65178/A integrates also a synchronous buck 3 (step-down) converter that uses a PWM able to sink and source current up to 500 mA.

Enable Signal (DLY2)

The buck 3 converter is enabled together with the boost converter when the power good of the negative charge pump (VGL) is asserted and that the DLY2 has passed. See the *Appendix* section to set the DLY2 timing.

Startup and Short Circuit Protection (Buck 3 Converter)

The buck 3 converter output voltage tracks the boost converter output voltage at a ratio metric pace during startup. To prevent Source Driver damages, the TPS65178/A implements a protection feature that disables both the boost (V_{DD}) and the buck 3 (HV_{DD}) converters when short-circuits or over voltages occur on one of the two converters. The converters will autonomously recover after the failure has gone.

Setting the output voltage HVDD

The output voltage of the buck 3 converter is programmable via a two-wire interface between 6.4 V and 9.55 V with a 6-bit resolution. See the *Appendix* section to set the HV_{DD} voltage.

Buck 3 Converter Design Procedure

1. Duty Cycle: $D = \frac{HV_{DD}}{V_{IN} \times \eta}$
2. Inductor ripple current: $\Delta I_L = \frac{1.85e^{-6}}{L}$
3. Maximum output current: $I_{HVDD\_max} = I_{LIM\_min} - \frac{\Delta I_L}{2}$
4. Peak switch current: $I_{SWPEAK} = I_{HVDD\_max} + \frac{\Delta I_L}{2}$

   η = Estimated buck 3 converter efficiency (use the number from the efficiency plots or 80% as an estimation)

   f = Buck 3 converter switching frequency $f_{SW3} = \frac{HV_{DD} \times (1\text{-}D)}{1.85e^{-6}}$

   L = Selected inductor value for the buck 3 converter (in µH – for value see the *Inductor Selection* section)

   I_{SWPEAK} = Buck 3 converter switch current (must be < I_{LIM_min} = 0.8 A)

   ΔI_L = Inductor peak-to-peak ripple current

The peak switch current is the steady state current that the integrated switches and the inductor have to be able to handle.

Inductor Selection (Buck 3 Converter)

Refer to the boost converter *Inductor Selection* section, for more details.

Inductor value: the buck 3 converter is designed to work with small inductors in the following range: 4.7µH ≤ L ≤ 10 µH. The buck 3 converter is optimized to work with 6.8 µH.

Table 7. Inductor Selection Buck 3 (Chip Inductors)

L (µH)	SUPPLIER	COMPONENT CODE	SIZE (LxWxH mm)	DCR TYP (mΩ)	I_{SAT} (A)
4.7, 6.8, 10	Taiyo Yuden	CBC2518T series	2.5 x 1.8 x 1.8	260 ~ 460	480 ~ 680
4.7, 6.8, 10	Taiyo Yuden	CBC3225T series	3.2 x 2.5 x 2.5	100 ~ 133	900 ~ 1250

Input Capacitor Selection

Typically, one 10-µF ceramic capacitor on PVINB3 pin is recommended. For better input voltage filtering this value can be increased. Refer to the *Recommended Operation Conditions* table, Table 4 and the *Typical Application* section for input capacitor recommendations.

Output Capacitor Selection

Typically, one 10-µF ceramic output capacitor works for most of the applications. Refer to the *Recommended Operation Conditions* table, Table 4 and the *Typical Application* section for output capacitor recommendations.

POSITIVE CHARGE PUMP CONTROLLER (V_{GH}) and TEMPERATURE COMPENSATION

The positive charge pump (CPP) flying capacitor is driven from SWP pin with an intergated 50% duty cycle push-pull stage. The regulation is achieved using an external PNP transistor controlled by the CTRLP pin. The TPS65178/A also includes a temperature compensation feature that controls the output voltage depending on the temperature sense by an external Negative Thermistor (NTC).

Enable Signal (DLY3)

The positive charge pump controller as well as the push-pull stage on SWP pin are enabled when the boost and buck 3 converters' power good signals are asserted and that the DLY3 has passed. See the *Appendix* section to set the DLY3 timing.

Positive Charge Pump Controller Operation

During normal operation, the TPS65178/A is able to provide up to 1.5 mA of base current typically and is designed to work best with transistors whose DC gain (hFE) is between 100 and 300. The charge pump is protected against short-circuits on its output, which are detected for voltages below 1 V. During short-circuit mode, the base current available from the CTRLP pin is limited to 60 µA typically. Note that if a short-circuit is detected during normal operation, the boost converter switching activity is also halted until V_{GH} is above 1 V. Typical application circuits are shown in Figure 27.

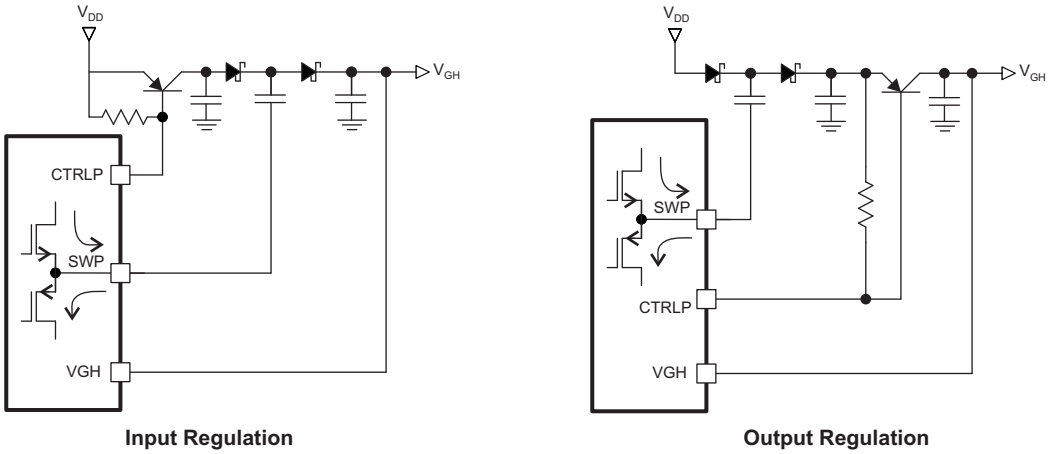


Figure 27. Positive Charge Pump Application Circuits

Positive Charge Pump Design Procedure

The regulation of the positive charge pump (CPP) can be done either on the input (transistor placed between V_{DD} and the diode) or on the output. For better regulation and fewer interactions between the boost converter and the CPP controller, it is recommended to place the transistor on the output. During startup, the inrush current is limited by the SWP push-pull stage that limits the current to 300 mA typically. For proper operation, it is recommended to have a headroom ($2xV_{DD}$-$2xV_{DIODE}$-V_{GH}) of 1 V minimum.

Diodes selection (CPP)

Small-signal diodes can be used for most low current applications (<50mA) and higher rated diodes for higher power applications. The average current through the diode is equal to the output current, so that the power dissipated in the diode is given by: $P_D = I_{GH} \times V_F$

The peak current through the diode occurs during start-up for a few cycles may reach the current limit of the push-pull stage (500 mA max.). However, this condition typically lasts for < 1 ms and can be tolerated by many diodes whose repetitive current rating is much lower. The diodes' reverse voltage rating should be equal to $2 \times V_{DD}$.

Table 8. Positive Charge Pump Diode Selection

PART NUMBER	I_{AVG}	I_{PK}	V_R	V_F	COMPONENT SUPPLIER
BAV99W	150mA	1A for 1ms	75V	1V at 50mA	NXP
BAT54S	200mA	600mA for 1s	30V	0.8V at 100mA	Fairchild Semiconductor
MBR0540	500mA	5.5A for 8ms	40V	0.51 at 500mA	Fairchild Semiconductor

Capacitors Selection (CPP)

Flying capacitors

A flying capacitor in the range 100 nF to 1 µF is suitable for most applications. Larger values experience a smaller voltage drop by the end of each switching cycle, and allow higher output voltages and/or currents to be achieved. Smaller values tend to be physically smaller and a bit cheaper. For best performance, it is recommended to include a resistor of a few ohms (1 Ω is a good value to start with) in series with the flying capacitor to limited peak currents occurring at the instant of switching.

Storage capacitors

For lowest output voltage ripple, low-ESR ceramic capacitors are recommended. The actual value is not critical and 1 µF to 10 µF is suitable for most applications. Larger capacitors provide better performance in applications where large load transient currents are present.

Transistor placed on the input (Figure 27)

A collector capacitor is required. A range of 100 nF to 1µF is suitable for most applications. Larger values are more suitable for high current applications but can affect stability if they are too big.

Transistor placed on the output (Figure 27)

An emitter capacitor is required. A range of 1µF to 10 µF is suitable for most applications. A smaller ratio between the emitter capacitor and the output capacitor is better for startup reason. A combination of C_{OUT} = 4.7 µF, C_{FLY} = 220 nF, (and $C_{EMITTER}$ = 4.7 µF) is a good starting point for most applications (the final values can be optimized on a case-by-case basis if necessary).

Selecting the PNP Transistor (CPP)

The PNP transistor used to regulate VGH should have a DC gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump's output current. The transistor should also be able to withstand voltages up to $2 \times V_{DD}$ across its collector-emitter (V_{CE}) – in the case where the CPP operates in doubler mode.

The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design. The power dissipated in the transistor is given by the following equation:

The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design. The power dissipated in the transistor is given by the following equation:

$$P_Q = \left[(2 \times V_{DD}) - (2 \times V_F) - V_{GH} \right] \times I_{GH} \quad (2)$$

I_{GH} = Mean output current on V_{GH}
V_F = Diode forward voltage

A pull-up resistor is also required between the transistor's base and emitter. The value of this resistor is not critical, but it should be large enough not to divert significant current away from the base of the transistor. A value of 100 kΩ is suitable for most applications.

Positive Charge Pump Protection

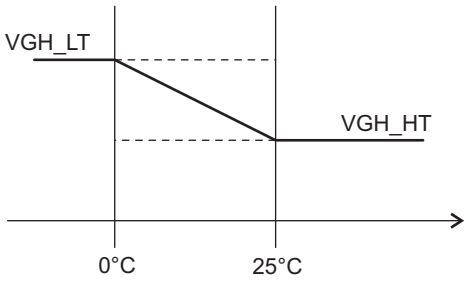
The TPS65178/A contains a circuit to protect the CPP against short circuits on its output. A short circuit condition is detected as long as the VGH voltage is below 1 V. The base current is then limited to 55 µA typically.

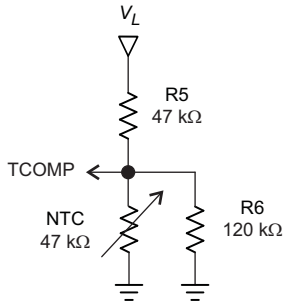
Temperature Compensation

By connecting a fixed-value thermistor between [TCOMP and GND] and a fixed-value pull-up resistor between [VL and TCOMP], the V_{GH} voltage will vary from a given V_{GH_LT} voltage below a pre-defined (by external resistors) 'low' temperature to a lower voltage defined by V_{GH_HT} for 'high' temperatures (also set by the same external resistors). The user has to provide V_{GH_LT} and V_{GH_HT}. The temperatures can be adjusted using the external resistors.

NOTE

The internal temperature compensation system is made to work only with 47 kΩ NTC part number **NCP18WB473F10RB** only (see the *Appendix* section).





Setting the output voltage V_{GH_LT} and V_{GH_HT}

The output voltage of the positive charge pump is programmable via a two-wire interface between 19 V and 34 V with a 4-bit resolution for V_{GH_LT}, and between 17 V and 32 V with a 4-bit resolution for V_{GH_HT}. See the *Appendix* section to set the V_{GH_LT} and V_{GH_HT} voltage.

NOTE

In the case where $V_{GH\_LT} \leq V_{GH\_HT}$, whatever the temperature is, the output voltage will be V_{GH_HT}.

NEGATIVE CHARGE PUMP (V_{GL})

The negative charge pump (CPN) flying capacitor is driven from SWN pin with an intergated 50% duty cycle push-pull stage. The regulation is achieved using an external NPN transistor controlled by the CTRLN pin. The IC is optimized for use with transistors having a DC gain (h_{FE}) in the range 100 to 300; however, it is possible to use transistors outside this range, depending on the application requirements. A typical application circuit is shown in Figure 28.

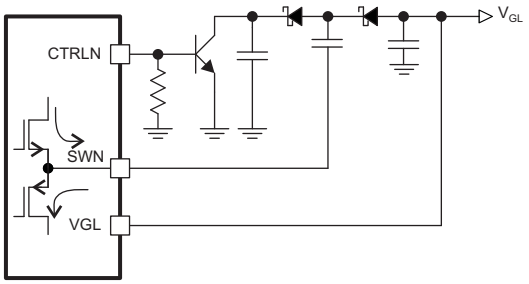


Figure 28. Negative Charge Pump Application Circuit

Enable Signal (DLY1)

The negative charge pump controller as well as the push-pull stage on SWN pin are enabled when the buck 2 converters' power good signal is asserted and that the DLY1 has passed. See the *Appendix* section to set the DLY1 timing.

Setting the output voltage V_{GL}

The output voltage of the negative charge pump is programmable via a two-wire interface between –1.8 V and –8.1 V with a 6-bit resolution. See the *Appendix* section to set the V_{GL} voltage.

Negative Charge Pump Design Procedure

Diodes Selection (CPN)

As for the CPP, the CPN's diodes need to handle the following power: $P_D = I_{GL} \times V_F$. See Table 3 for diode selection.

Capacitors selection (CPN)

See the *Capacitors selection (CPP)* section for more detail.

A combination of C_{OUT} = 4.7 µF, C_{FLY} = 100 nF, and $C_{COLLECTOR}$ = 100 nF is a good starting point for most applications (the final values can be optimized on a case-by-case basis if necessary).

Selecting the NPN Transistor (CPN)

The NPN transistor used to regulate V_{GL} should have a DC gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump's output current. The transistor should also be able to withstand voltages up to V_{IN} across its collector-emitter (V_{CE}).

The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design. The power dissipated in the transistor is given by the following equation:

$$P_Q = \left[V_{IN} - (2 \times V_F) - |V_{GL}| \right] \times I_{GL} \quad (3)$$

I_{GL} = Mean output current on V_{GL}
V_F = Diode forward voltage

A pull-down resistor is also required between the transistor's base and emitter. The value of this resistor is not critical, but it should be large enough not to divert significant current away from the base of the transistor. A value of 100 kΩ is suitable for most applications

Negative Charge Pump Protection

The TPS65178/A contains a circuit to protect the CPN against short circuits on its output. A short circuit condition is detected as long as V_{GL} remains above -0.7 V. The base current is then limited to 320 µA typically.

P-VCOM VOLTAGE AND GAIN (V_{POS})

The TPS65178/A integrates a P-Vcom block that allows to set the non-inverting input voltage reference as well as the gain of an external operational amplifier (Op-Amp).

Enable Signal (DLY2)

The P-Vcom is powered by the boost converter and starts operating after the DLY2 has passed. See the *Appendix* section to set the DLY2 timing.

Setting the non-inverting Vcom voltage V_{POS}

The V_{POS} voltage generated on POS pin (45) is programmable via a two-wire interface with a 9-bit resolution between 250*V_{DD}/1023 and 640*V_{DD}/1023. See the *Appendix* section to set the V_{POS} voltage.

Setting the Vcom gain

A fixed gain option is selectable between via a two-wire interface between Buffer Mode, -1x amplification, -2x and -3x (addresses 00h - 03h). With the use of a fixed gain, the DYN pin can be left floating or connected to GND.

A dynamic gain option is selectable via a two-wire interface on address 04h (or higher). The user has the possibility to select the gain (-2x or -4x) using the logic input pin DYN (47): V_{DYN} = 'high' for -2x amplification and V_{DYN} = 'low' for -4x amplification. See the *Appendix* section to set the Vcom gain.

P-Vcom Design Procedure

The TPS65178/A P-Vcom block needs to be connected to an external Op-Amp as shown in Figure 29.

For better stability, the Op-Amp shall be placed as close as possible to the TPS65178/A device.

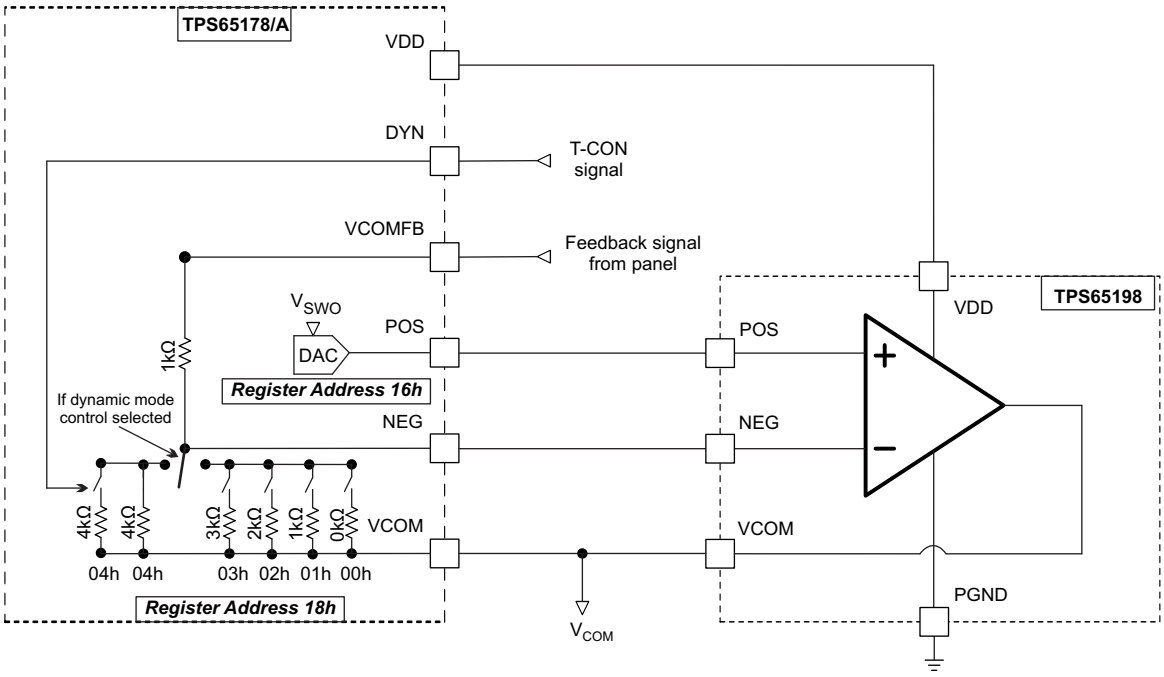


Figure 29. Interconnections VCOM TPS65178/A - TPS65198

NOTE

It is highly recommended in the case the panel features GIP (Gate In Panel) techonology to use the TPS65198 Level Shifter, which integrates an OpAmp in addition to its 13 Level Shifter output channels.

GAMMA BUFFER (GMA1-GMA6)

The TPS65178/A integrates 6-channel gamma buffer used as voltage references for the Source Driver IC.

Enable Signal (DLY2)

As the gamma buffer channels are supplied by the boost converter output rail, they are following ratio-metrically the V_{DD} voltage from power-on till power-down and start together with the boost converter after the DLY2 has passed. See the *Appendix* section to set the DLY2 timing.

Setting the output voltage of GMA1-GMA6

The output voltage of each of the 6 channels is programmable via a two-wire interface with a 9-bit resolution between V_{DD} and $V_{DD}/2$ for GMA1-GMA3, and between $V_{DD}/2$ and 0 V and for GMA4-GMA6 . See the *Appendix* section to set the V_{GMAX} voltage.

Output Load (Gamma Buffer)

The gamma buffer channels are able to sink and source DC output current of 10 mA (minimum guaranteed).

The output channels are not designed to support high capacitive loads bigger than 150 pF and shall be connected directly to the Source Driver IC without output capacitor.

TYPICAL APPLICATIONS

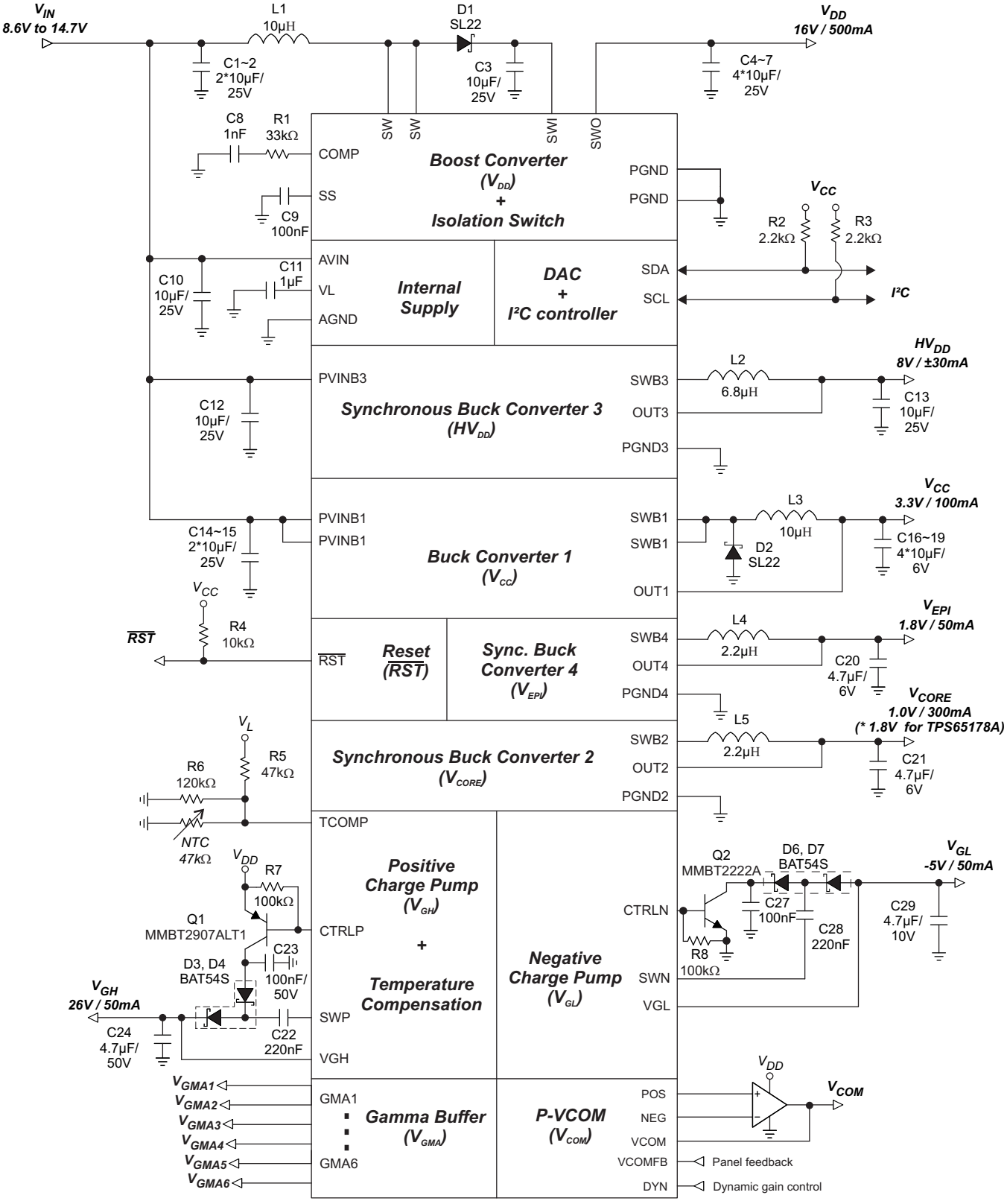


Figure 30.

PCB Layout Recommendations

NOTE

Special care must be taken for the Buck 2 and Buck 4 converters. Placing a decoupling capacitor of 1 µF miminum on OUT1 pin (4) as close as possible to the IC will help stabilize the switching waveforms of the hysteretic converters.

- For **high dv/dt** signals (switch pin traces): keep copper to a minimum to prevent making unintentional parallel plate capacitors with other traces or to a ground plane. Best to route signal and return on same layer.
- For **high di/dt** signals: keep traces short, wide and closely spaced. This will reduce stray inductance and decrease the current loop area to help prevent EMI.
- Always avoid vias when possible. They have high inductance and resistance. **If vias are necessary always use more than one in parallel to decrease parasitics especially for power lines.**
- Keep input capacitor close to the IC with low inductance traces.
- **Keep the copper trace between a switch node and a diode as short and wide as possible.**
- **Use single point grounding.**
- **All AGND and PGND pins must be connected to the Power Pad.**
- Isolate analog signal paths from power paths.
- Keep trace from switching node pin to inductor short: **it reduces EMI emissions and noise that may couple into other portions of the converter.**
- Output voltage feedback sampling must be taken right at output capacitor and shielded.

APPENDIX – I²C INTERFACE

I²C Serial Interface Description

The TPS65178/A communicates through an industry standard two-wire interface, I²C, to receive data in slave mode.

The TPS65178/A integrates a non-volatile memory (EEPROM) that allows the storage of the DAC values into the registers with a capability of 1000 programming cycles maximum.

I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS65178/A works as a slave and supports the following data transfer modes, as defined in the I²C-Bus specification: standard mode (100 kbps) and fast mode (400 kbps). The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The TPS65178/A supports 7-bit addressing. The device 7-bit address is defined as '010000X' (see Figure 31), where the LSB enables the write or read function.

(MSB)	TPS65178/A Address						(LSB)
0	1	0	0	0	0	0	R/$\overline{W}$

NOTE: R/$\overline{W}$ = R/(W)

Figure 31. TPS65178/A Slave Address Byte

The device that initiates the communication is called a master, and the devices controlled by the master are slaves. The master generates the serial clock on SCL, controls the bus access, and generates START and STOP conditions (see Figure 32). A START initiates a new data transfer to slave. Transitioning SDA from high to low while SCL remains high generates a START condition. A STOP condition ends a data transfer to slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

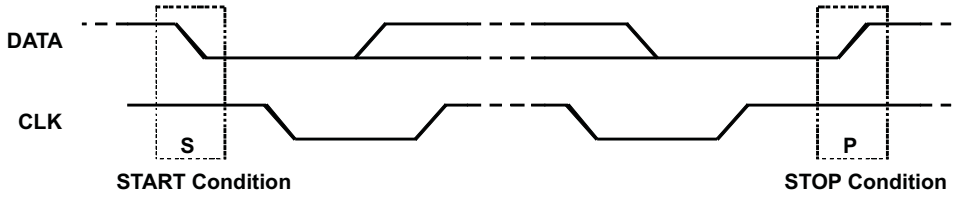


Figure 32. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/(W) on the SDA line. During all transmissions, the master ensures that the data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 33). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an Acknowledgment, ACK, (see Figure 34) by pulling the SDA line low during the entire high period of the SCL cycle. Upon detecting this Acknowledgment, the master knows that communication link with a slave has been established.

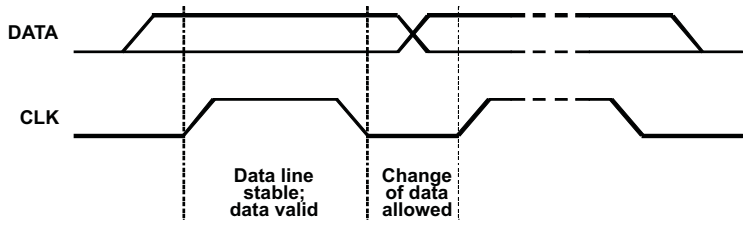


Figure 33. Bit Transfer on the Serial Interface

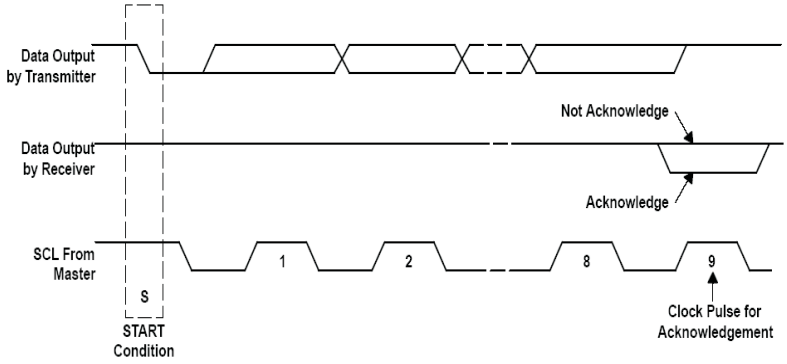


Figure 34. Acknowledge on the I²C Bus

The master generates further SCL cycles to either transmit data to the slave (R/(W) bit = 0) or receive data from the slave (R/(W) bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To terminate the data transfer, the master generates STOP condition by pulling the SDA line from low to high while the SCL line is high (see Figure 35). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

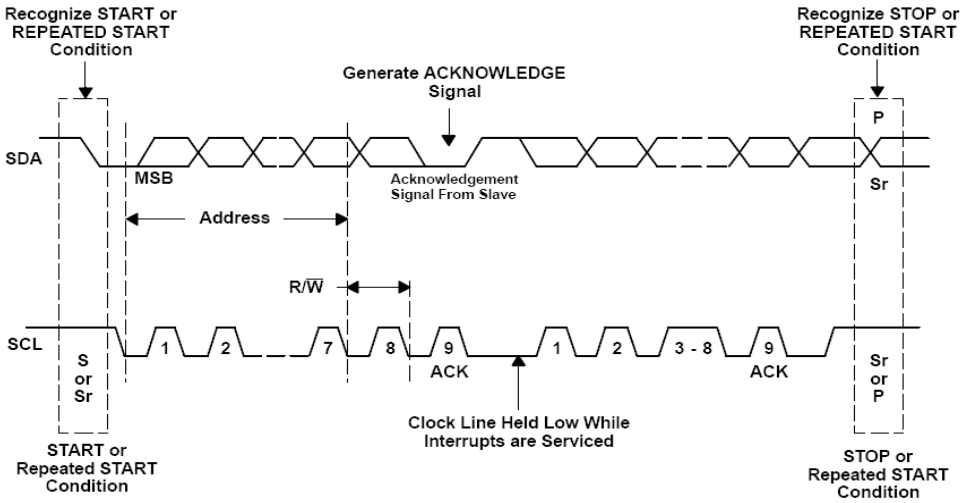


Figure 35. Bus Protocol

Attempting to read data from register addresses not listed in the following section will result in 00h being read out.

DETAILED DESCRIPTION

REGISTER MAP

Slave address: 0100000X

X = R/W R/W = 1 → read mode

R/W = 0 → write mode

Table 9. Register Map

REGISTER	NAME	ADDRESS	FACTORY VALUE	BIT COUNT	STEPS COUNT
VDD	Boost	00h	21h	6	64
VEPI	Buck 4	01h	09h	4	16
VCC	Buck 1	02h	03h	3	8
VCORE	Buck 2	03h	01h for TPS65178	4	16
		03h	09h for TPS65178A	4	16
VGH_LT	Positive charge pump - Low Temperature	04h	09h	4	16
VGH_HT	Positive charge pump - High Temperature	05h	09h	4	16
VGL	Negative charge pump	06h	20h	6	64
DLY1	V_{GL} delay	07h	01h	3	8
DLY2	V_{DD} delay	08h	03h	3	8
DLY3	V_{GH} delay	09h	03h	3	8
GMA1	Gamma buffer 1	0Ah	01h	1	512
			5Fh	8	
GMA2	Gamma buffer 2	0Ch	01h	1	512
			06h	8	
GMA3	Gamma buffer 3	0Eh	00h	1	512
			86h	8	
GMA4	Gamma buffer 4	10h	01h	1	512
			86h	8	
GMA5	Gamma buffer 5	12h	01h	1	512
			0Ch	8	
GMA6	Gamma buffer 6	14h	00h	1	512
			9Fh	8	
VPOS	VCOM reference	16h	00h	1	391
			DFh	8	
VCOM GAIN	VCOM gain selection	18h	00h	3	5
CR	Control Register	FFh	–	8	1

DAC REGISTERS

VDD Register (with factory value) – 00h (21h):

MSB			Address 001				LSB
Reserved	Reserved	1	0	0	0	0	1

VEPI Register (with factory value) – 01h (09h):

MSB			Address 01h				LSB
Reserved	Reserved	Reserved	Reserved	1	0	0	1

VCC Register (with factory value) – 02h (03h):

MSB			Address 02h				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	1	1

VCORE Register (with factory value) – 03h (01h): for TPS65178

MSB			Address 03h				LSB
Reserved	Reserved	Reserved	Reserved	0	0	0	1

VCORE Register (with factory value) – 03h (09h): for TPS65178A

MSB			Address 03h				LSB
Reserved	Reserved	Reserved	Reserved	1	0	0	1

VGH_LT Register (with factory value) – 04h (09h):

MSB			Address 04h				LSB
Reserved	Reserved	Reserved	Reserved	1	0	0	1

VGH_HT Register (with factory value) – 05h (09h):

MSB			Address 05h				LSB
Reserved	Reserved	Reserved	Reserved	1	0	0	1

VGL Register (with factory value) – 06h (20h):

MSB			Address 06h				LSB
Reserved	Reserved	1	0	0	0	0	0

DLY1 Register (with factory value) – 07h (01h):

MSB			Address 07h				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	0	1

DLY2 Register (with factory value) – 08h (03h):

MSB			Address 08h				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	1	1

DLY3 Register (with factory value) – 09h (03h):

MSB			Address 09h				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	1	1

GMA1 Register (with factory value) – 0Ah (01 – 5Fh):

MSB			Address 0Ah (MSB byte)				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1

MSB			Address 0Ah (LSB byte)				LSB
0	1	0	1	1	1	1	1

GMA2 Register (with factory value) – 0Ch (01 – 6Fh):

MSB			Address 0Ch (MSB byte)				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1

MSB			Address 0Ch (LSB byte)				LSB
0	0	0	0	0	1	1	0

GMA3 Register (with factory value) – 0Eh (00 – 86h):

MSB			Address 0Eh (MSB byte)				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0

MSB			Address 0Eh (LSB byte)				LSB
1	0	0	0	0	1	1	0

GMA4 Register (with factory value) – 10h (01 – 86h):

MSB			Address 10h (MSB byte)				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1

MSB			Address 10h (LSB byte)				LSB
1	0	0	0	0	1	1	0

GMA5 Register (with factory value) – 12h (01 – 0Ch):

MSB			Address 12h (MSB byte)				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1

MSB			Address 12h (LSB byte)				LSB
0	0	0	0	1	1	0	0

GMA6 Register (with factory value) – 14h (00 – 9Fh):

MSB			Address 14h (MSB byte)				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0

MSB			Address 14h (LSB byte)				LSB
1	0	0	1	1	1	1	1

VPOS Register (with factory value) – 16h (00 – DFh):

MSB			Address 16h (MSB byte)				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0

MSB			Address 16h (LSB byte)				LSB
1	1	0	1	1	1	1	1

VCOM Register (with factory value) – 18h (00h):

MSB			Address 18h (MSB byte)				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	0	0

Control Register – FFh:

MSB			Address FFh				LSB
WED	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EE/(DR)

DAC SETTINGS

The following tables show the DAC values and the corresponding voltages of each block address.

VDD (00h)

DAC value	VDD
00h	12.82 V
01h	12.92 V
02h	13.02 V
03h	13.11 V
04h	13.21 V
05h	13.31 V
06h	13.41 V
07h	13.50 V
08h	13.60 V
09h	13.70 V
0Ah	13.80 V
0Bh	13.90 V
0Ch	13.99 V
0Dh	14.09 V
0Eh	14.19 V
0Fh	14.29 V
10h	14.38 V
11h	14.48 V
12h	14.58 V
13h	14.68 V
14h	14.78 V
15h	14.87 V
16h	14.97 V
17h	15.07 V
18h	15.17 V
19h	15.26 V
1Ah	15.36 V
1Bh	15.46 V
1Ch	15.56 V
1Dh	15.66 V
1Eh	15.75 V
1Fh	15.85 V

DAC value	VDD
20h	15.95 V
21h	16.05 V
22h	16.14 V
23h	16.24 V
24h	16.34 V
25h	16.44 V
26h	16.54 V
27h	16.63 V
28h	16.73 V
29h	16.83 V
2Ah	16.93 V
2Bh	17.02 V
2Ch	17.12 V
2Dh	17.22 V
2Eh	17.32 V
2Fh	17.42 V
30h	17.51 V
31h	17.61 V
32h	17.71 V
33h	17.81 V
34h	17.90 V
35h	18.00 V
36h	18.10 V
37h	18.20 V
38h	18.30 V
39h	18.39 V
3Ah	18.49 V
3Bh	18.59 V
3Ch	18.69 V
3Dh	18.78 V
3Eh	18.88 V
3Fh	18.98 V

VGL (06h)

DAC value	VGL
00h	-1.8 V
01h	-1.9 V
02h	-2.0 V
03h	-2.1 V
04h	-2.2 V
05h	-2.3 V
06h	-2.4 V
07h	-2.5 V
08h	-2.6 V
09h	-2.7 V
0Ah	-2.8 V
0Bh	-2.9 V
0Ch	-3.0 V
0Dh	-3.1 V
0Eh	-3.2 V
0Fh	-3.3 V
10h	-3.4 V
11h	-3.5 V
12h	-3.6 V
13h	-3.7 V
14h	-3.8 V
15h	-3.9 V
16h	-4.0 V
17h	-4.1 V
18h	-4.2 V
19h	-4.3 V
1Ah	-4.4 V
1Bh	-4.5 V
1Ch	-4.6 V
1Dh	-4.7 V
1Eh	-4.8 V
1Fh	-4.9 V

DAC value	VGL
20h	-5.0 V
21h	-5.1 V
22h	-5.2 V
23h	-5.3 V
24h	-5.4 V
25h	-5.5 V
26h	-5.6 V
27h	-5.7 V
28h	-5.8 V
29h	-5.9 V
2Ah	-6.0 V
2Bh	-6.1 V
2Ch	-6.2 V
2Dh	-6.3 V
2Eh	-6.4 V
2Fh	-6.5 V
30h	-6.6 V
31h	-6.7 V
32h	-6.8 V
33h	-6.9 V
34h	-7.0 V
35h	-7.1 V
36h	-7.2 V
37h	-7.3 V
38h	-7.4 V
39h	-7.5 V
3Ah	-7.6 V
3Bh	-7.7 V
3Ch	-7.8 V
3Dh	-7.9 V
3Eh	-8.0 V
3Fh	-8.1 V

VCC (02h)

DAC value	VCC
00h	3.0 V
01h	3.1 V
02h	3.2 V
03h	3.3 V
04h	3.4 V
05h	3.5 V
06h	3.6 V
07h	3.7 V

VCORE (03h)

DAC value	VCORE
00h	0.9 V
01h	1.0 V
02h	1.1 V
03h	1.2 V
04h	1.3 V
05h	1.4 V
06h	1.5 V
07h	1.6 V
08h	1.7 V
09h(1)	1.8 V
0Ah	1.9 V
0Bh	2.0 V
0Ch	2.1 V
0Dh	2.2 V
0Eh	2.3 V
0Fh	2.4 V

VGH LT,HT (04h - 05h)

DAC value	VGH_LT
00h	19 V
01h	20 V
02h	21 V
03h	22 V
04h	23 V
05h	24 V
06h	25 V
07h	26 V
08h	27 V
09h	28 V
0Ah	29 V
0Bh	30 V
0Ch	31 V
0Dh	32 V
0Eh	33 V
0Fh	34 V

DAC value	VGH_HT
00h	17 V
01h	18 V
02h	19 V
03h	20 V
04h	21 V
05h	22 V
06h	23 V
07h	24 V
08h	25 V
09h	26 V
0Ah	27 V
0Bh	28 V
0Ch	29 V
0Dh	30 V
0Eh	31 V
0Fh	32 V

(1) Default value for TPS65178A

VEPI (01h)

DAC value	VEPI
00h	0.9 V
01h	1.0 V
02h	1.1 V
03h	1.2 V
04h	1.3 V
05h	1.4 V
06h	1.5 V
07h	1.6 V
08h	1.7 V
09h	1.8 V
0Ah	1.9 V
0Bh	2.0 V
0Ch	2.1 V
0Dh	2.2 V
0Eh	2.3 V
0Fh	2.4 V

VGMA1, 2, 3 (0Ah ~ 0Fh)

DAC value	VGMA1,2,3
00-00h	512*(V_{DD}/1023)
00-01h	513*(V_{DD}/1023)
00-02h	514*(V_{DD}/1023)
00-03h	515*(V_{DD}/1023)
00-04h	516*(V_{DD}/1023)
00-05h	517*(V_{DD}/1023)
00-06h	518*(V_{DD}/1023)
…	…
01-F9h	1017*(V_{DD}/1023)
01-FAh	1018*(V_{DD}/1023)
01-FBh	1019*(V_{DD}/1023)
01-FCh	1020*(V_{DD}/1023)
01-FDh	1021*(V_{DD}/1023)
01-FEh	1022*(V_{DD}/1023)
01-FFh	1023*(V_{DD}/1023)

DLY1, 2, 3 (07h - 08h - 09h)

DAC value	DLY1
00h	0 ms
01h	5 ms
02h	10 ms
03h	15 ms
04h	20 ms
05h	25 ms
06h	30 ms
07h	35 ms

DAC value	DLY2
00h	0 ms
01h	5 ms
02h	10 ms
03h	15 ms
04h	20 ms
05h	25 ms
06h	30 ms
07h	35 ms

DAC value	DLY3
00h	0 ms
01h	5 ms
02h	10 ms
03h	15 ms
04h	20 ms
05h	25 ms
06h	30 ms
07h	35 ms

VPOS (16h - 17h)

DAC value	VPOS
00-00h	250*(V_{DD}/1023)
00-01h	251*(V_{DD}/1023)
00-02h	252*(V_{DD}/1023)
00-03h	253*(V_{DD}/1023)
00-04h	254*(V_{DD}/1023)
00-05h	255*(V_{DD}/1023)
00-06h	256*(V_{DD}/1023)
…	…
01-80h	634*(V_{DD}/1023)
01-81h	635*(V_{DD}/1023)
01-82h	636*(V_{DD}/1023)
01-83h	637*(V_{DD}/1023)
01-84h	638*(V_{DD}/1023)
01-85h	639*(V_{DD}/1023)
01-86h	640*(V_{DD}/1023)

VGMA4, 5, 6 (10h - 15h)

DAC value	VGMA4,5,6
00-00h	0*(V_{DD}/1023)
00-01h	1*(V_{DD}/1023)
00-02h	2*(V_{DD}/1023)
00-03h	3*(V_{DD}/1023)
00-04h	4*(V_{DD}/1023)
00-05h	5*(V_{DD}/1023)
00-06h	6*(V_{DD}/1023)
…	…
01-F9h	505*(V_{DD}/1023)
01-FAh	506*(V_{DD}/1023)
01-FBh	507*(V_{DD}/1023)
01-FCh	508*(V_{DD}/1023)
01-FDh	509*(V_{DD}/1023)
01-FEh	510*(V_{DD}/1023)
01-FFh	511*(V_{DD}/1023)

VCOM Gain (18h)

DAC value	Gain
00h	Buffer
01h	-1x
02h	-2x
03h	-3x
04h	DYN
…	…
07h	DYN

I²C INTERFACE PROTOCOL

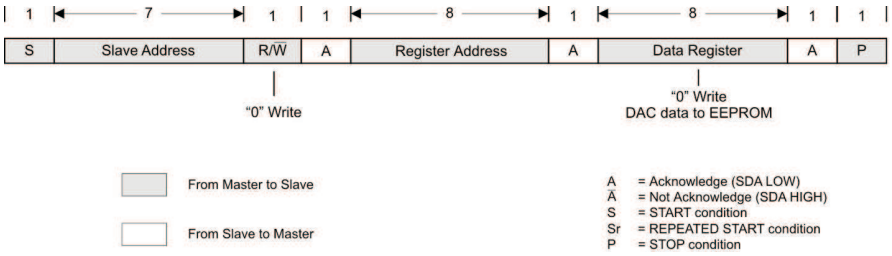


Figure 36. "Write" Data to DAC – Transfer Format in F/S-Mode

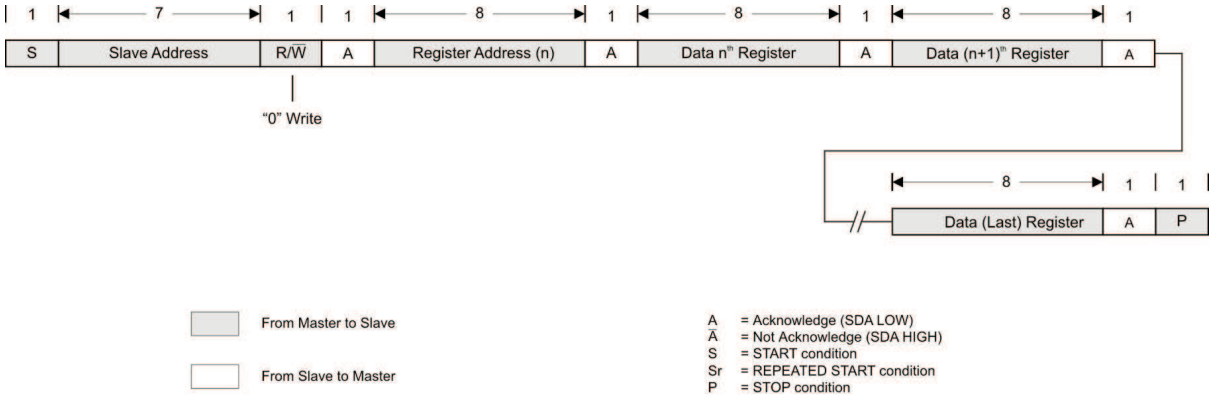


Figure 37. "Write" Data to DAC – Transfer Format in F/S-Mode Featuring Register Address Auto-Increment

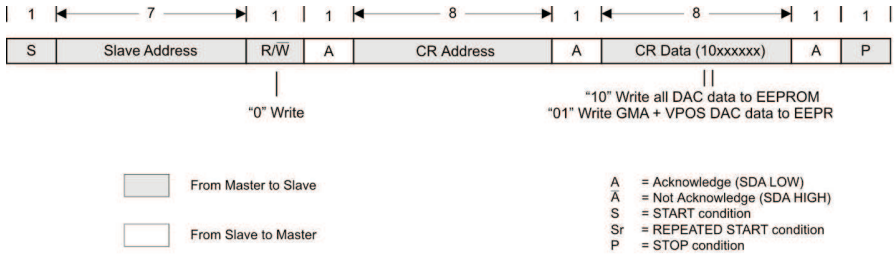


Figure 38. "Write" Data to EEPROM – Transfer Format in F/S-Mode Featuring Register Address Auto-Increment

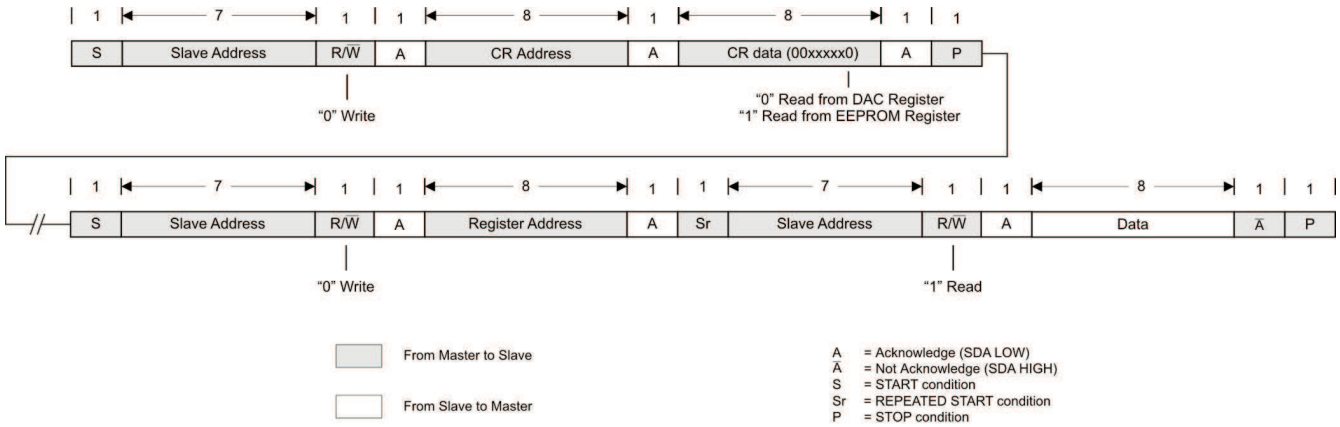


Figure 39. "Read" Data From DAC/EEPROM – Transfer Format in F/S-Mode

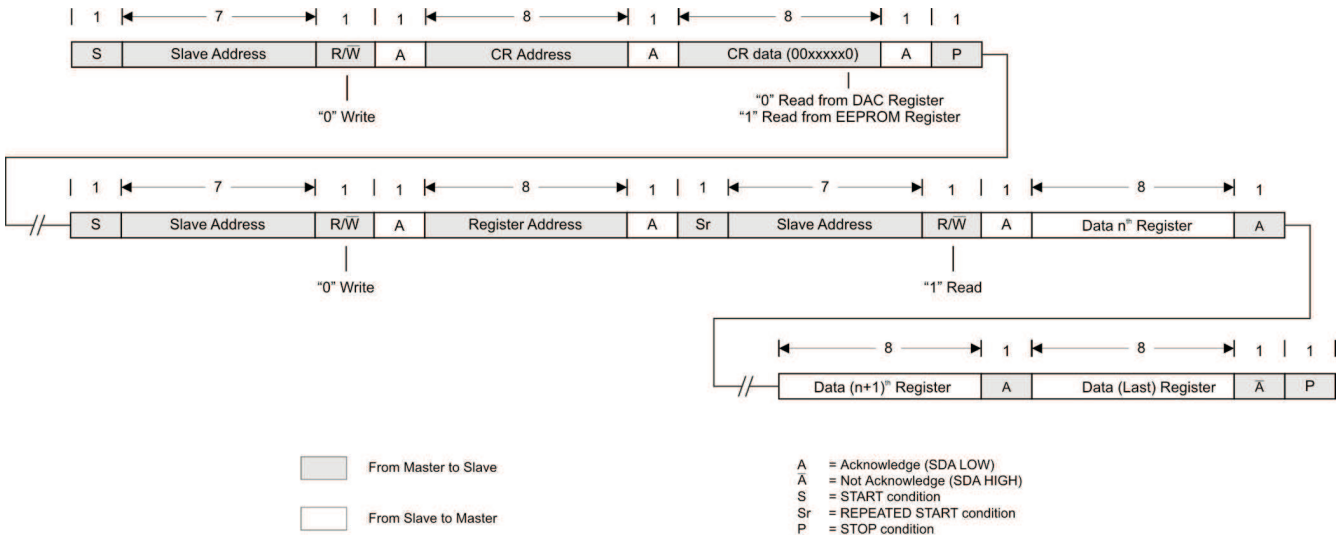
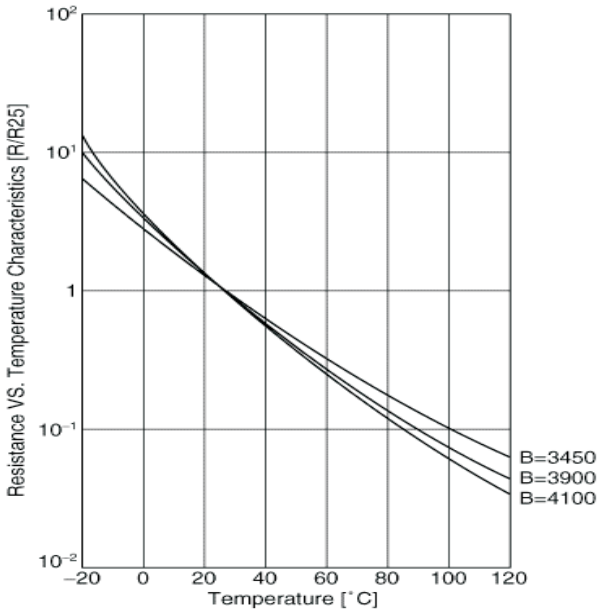


Figure 40. "Read" Data From DAC/EEPROM – Transfer Format in F/S-Mode Featuring Register Address Auto-Increment

TEMPERATURE COMPENSATION

Table 10. NTC 47 kΩ – NCP18WB473F10RB – Characteristics

Global Part Number	NCP18WB473F10RB
Resistance (25°C)	47 kΩ ±1%
B-Constant (25/50°C)	4050K ±1.5%
B-Constant (25/80°C)(Reference Value)	4101K
B-Constant (25/85°C)(Reference Value)	4108K
B-Constant (25/100°C)(Reference Value)	4131K
Permissive Operating Current (25°C)	0.14mA
Rated Electric Power (25°C)	100mW
Typical Dissipation Constant (25°C)	1mW/°C
Min. Operating Temp. Range	–40°C
Max. Operating Temp. Range	125°C



REVISION HISTORY

Changes from Original (July 2011) to Revision A	Page
• Changed Figure 2	9
• Changed Figure 30	31
• Changed VEPI; VGMA1 ,2 ,3; DLY1, 2, 3; VPOS; VGMA4, 5, 6; and VCOM Gain	40

Changes from Revision A (November 2011) to Revision B	Page
• Added TPS65178A device to data sheet	1

Changes from Revision B (January 2012) to Revision C	Page
• Added TEMPERATURE COMPENSATION section	43

Changes from Revision C (February 2012) to Revision D	Page
• Added "With the use of a fixed gain, the DYN pin can be left floating or connected to GND." to Setting the Vcom gain section	29

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65178ARSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178A	Samples
TPS65178ARSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178A	Samples
TPS65178RSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178	Samples
TPS65178RSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

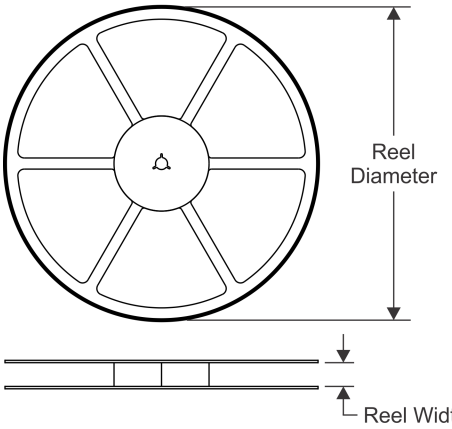
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

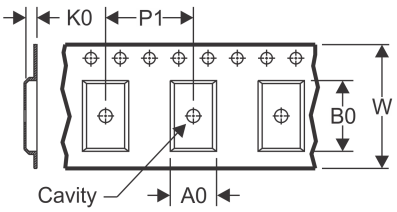
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

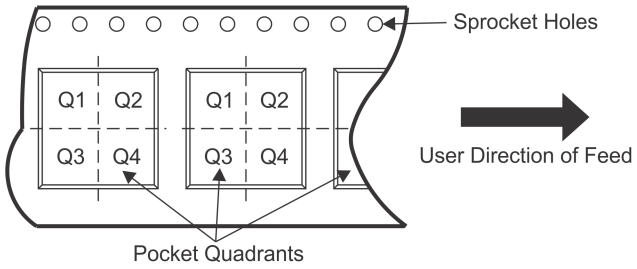


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

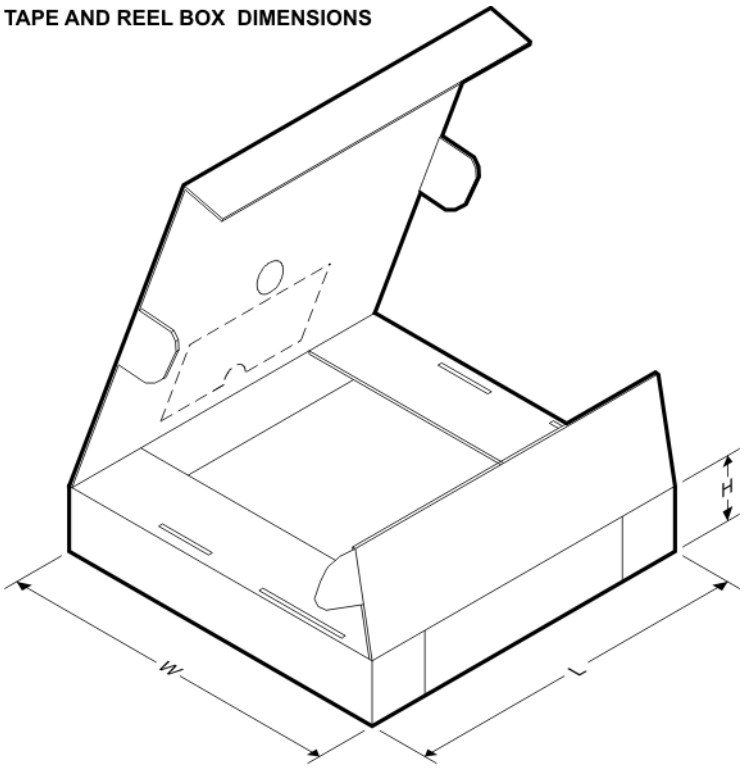
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65178ARSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65178ARSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65178RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

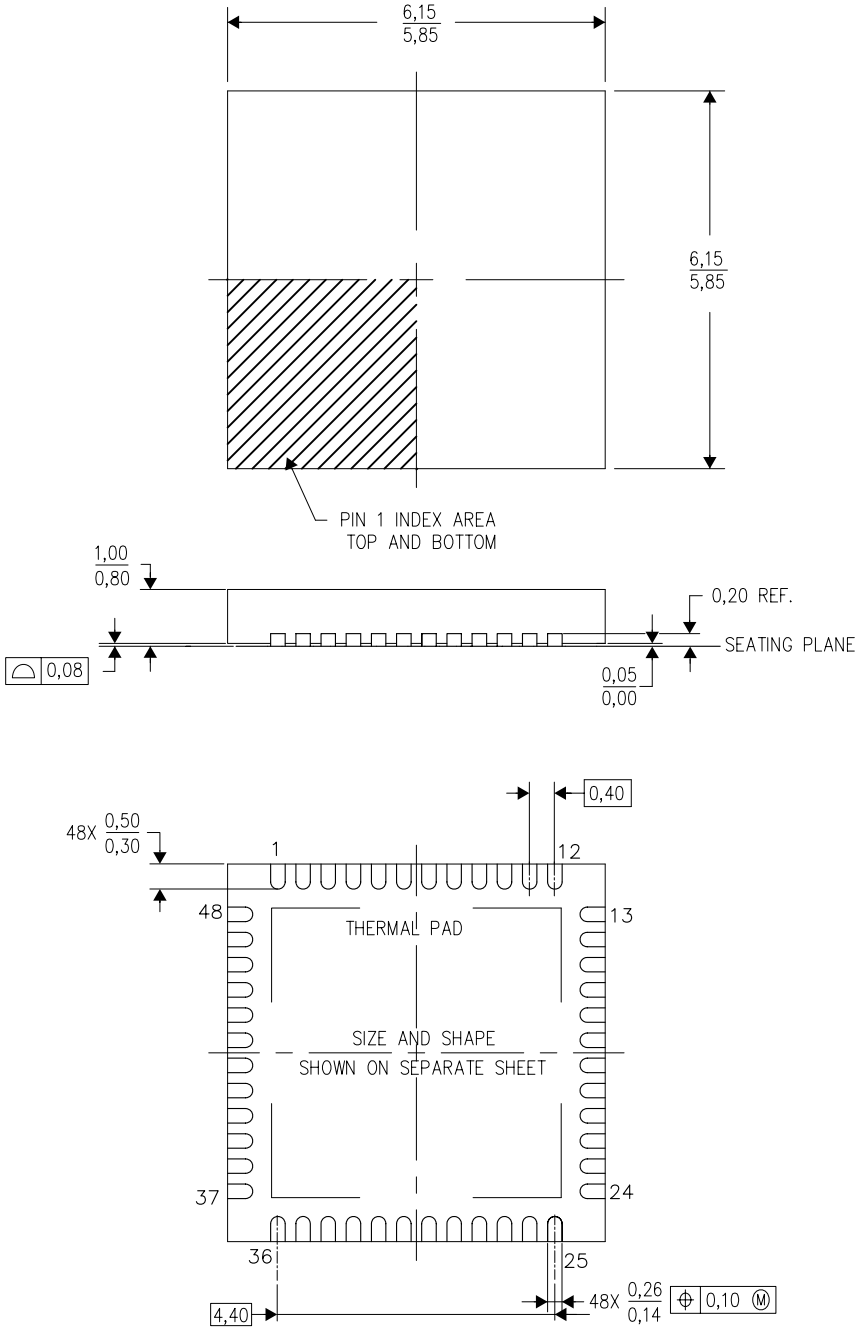
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65178ARSLR	VQFN	RSL	48	2500	552.0	367.0	38.0
TPS65178ARSLT	VQFN	RSL	48	250	552.0	185.0	36.0
TPS65178RSLR	VQFN	RSL	48	2500	552.0	367.0	38.0

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

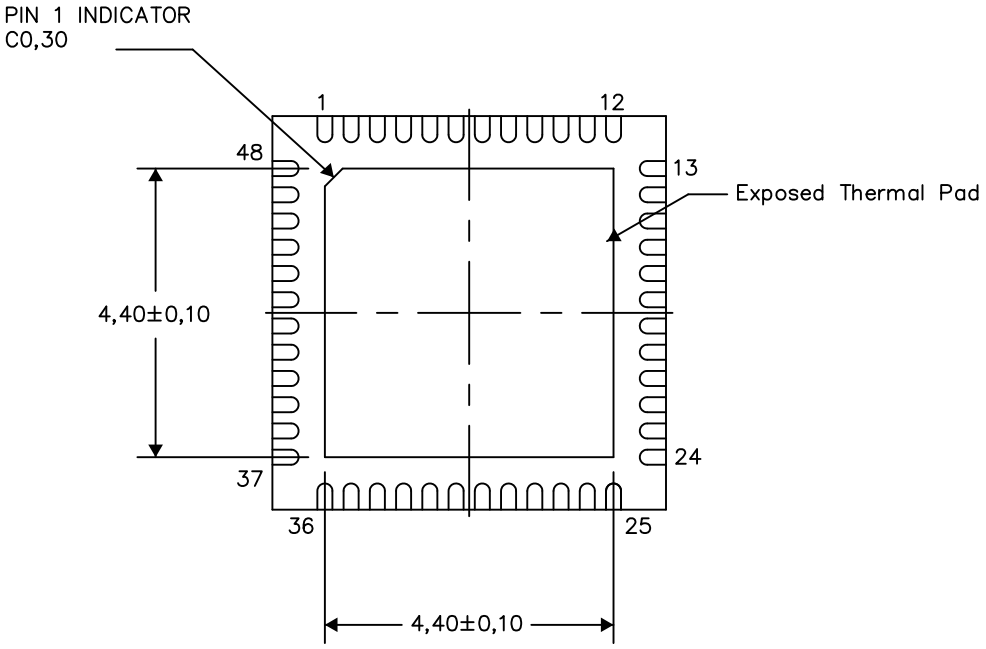
RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



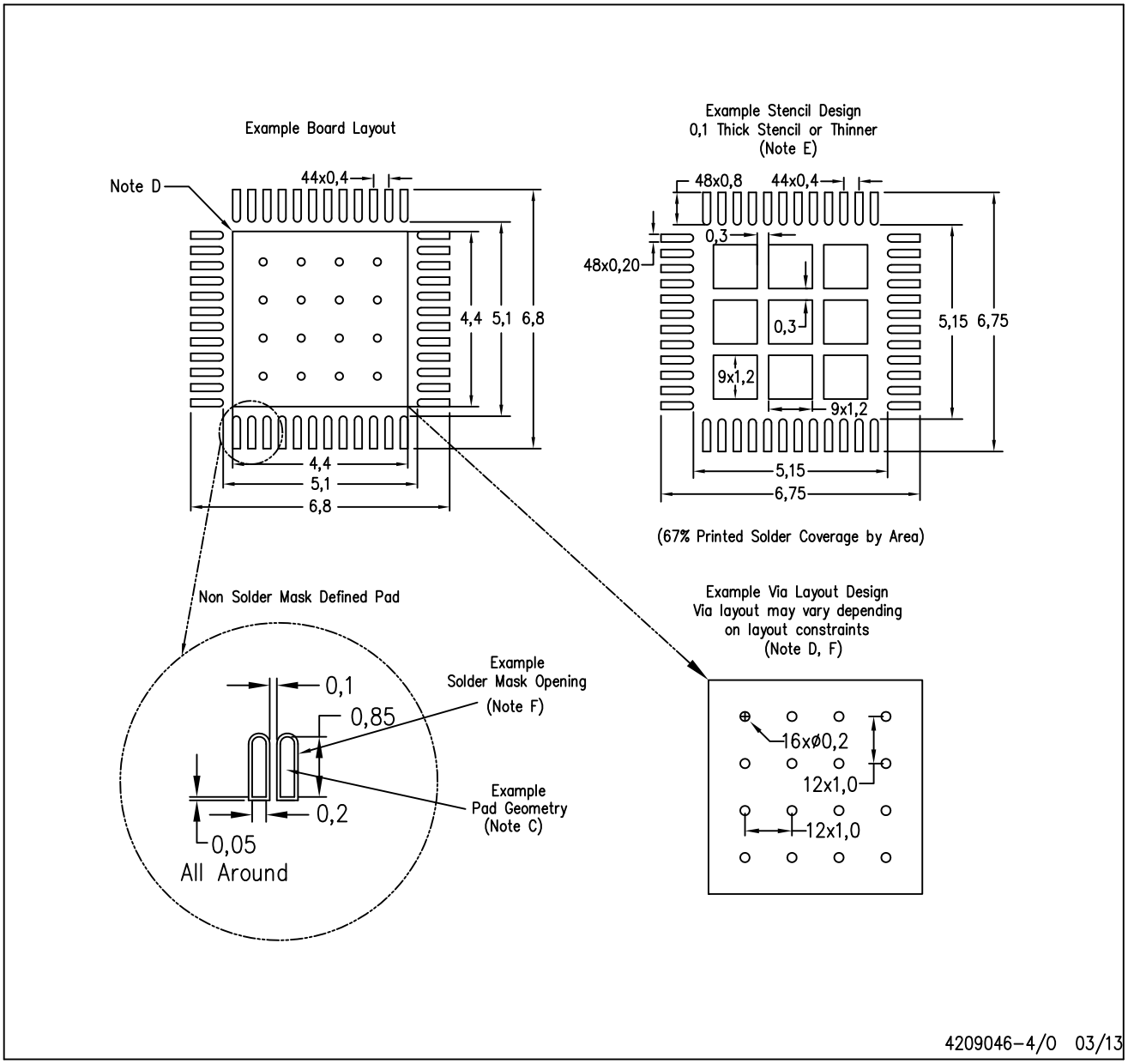
Bottom View

Exposed Thermal Pad Dimensions

4207841–2/P 03/13

NOTE: All linear dimensions are in millimeters

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65178ARSLR	Active	Production	VQFN (RSL) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178A
TPS65178ARSLR.A	Active	Production	VQFN (RSL) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178A
TPS65178ARSLR.B	Active	Production	VQFN (RSL) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178A
TPS65178ARSLT	Active	Production	VQFN (RSL) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178A
TPS65178ARSLT.A	Active	Production	VQFN (RSL) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178A
TPS65178ARSLT.B	Active	Production	VQFN (RSL) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178A
TPS65178RSLR	Active	Production	VQFN (RSL) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178
TPS65178RSLR.A	Active	Production	VQFN (RSL) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178
TPS65178RSLR.B	Active	Production	VQFN (RSL) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178
TPS65178RSLT	Active	Production	VQFN (RSL) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178
TPS65178RSLT.A	Active	Production	VQFN (RSL) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178
TPS65178RSLT.B	Active	Production	VQFN (RSL) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65178

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

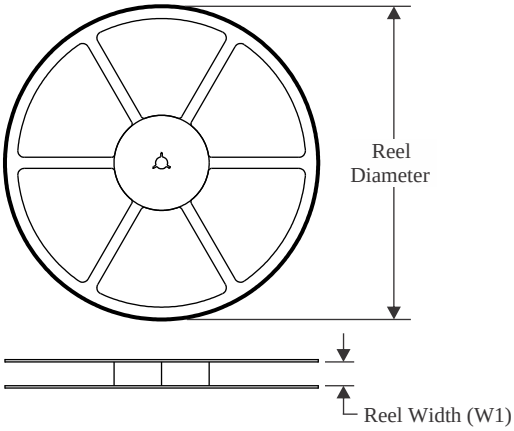
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

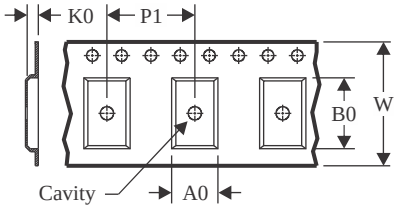
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

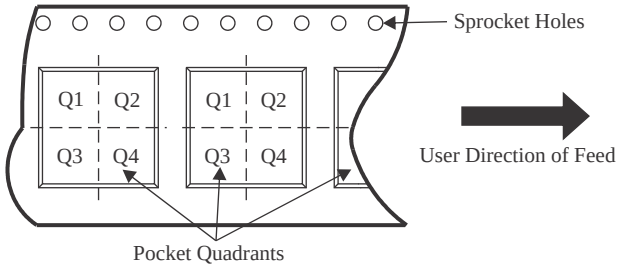


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

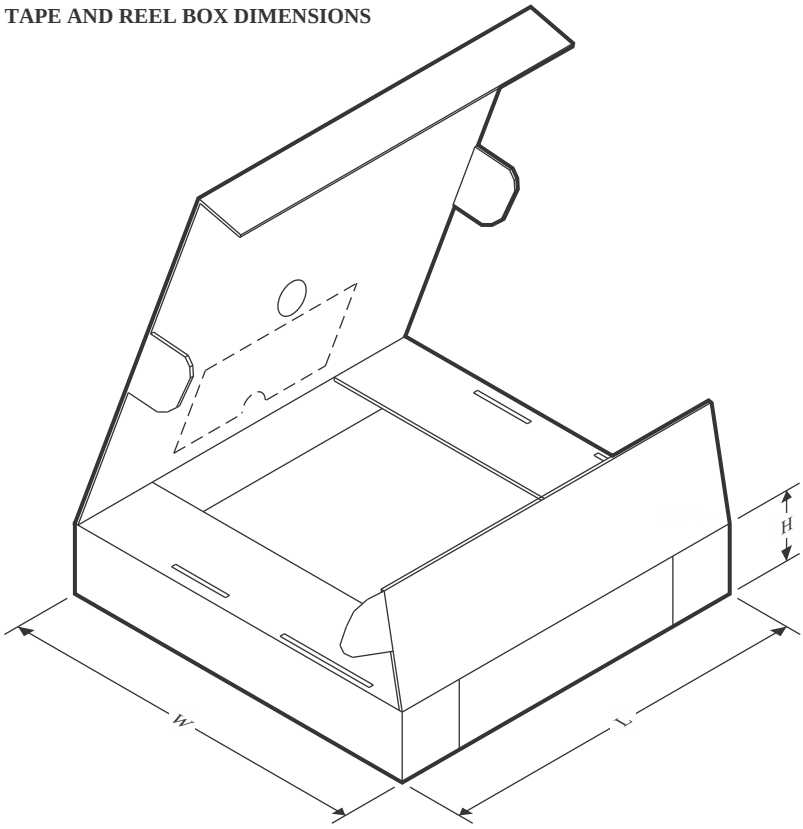
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65178ARSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65178ARSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65178RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65178RSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

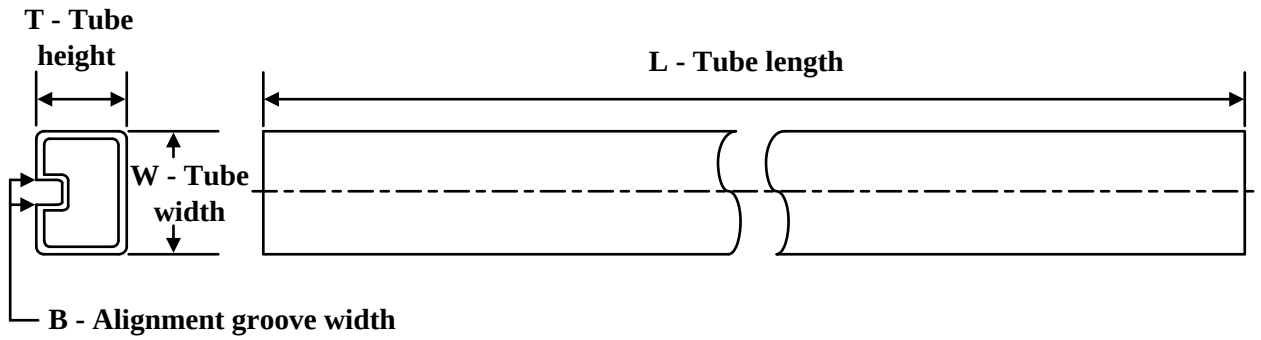
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65178ARSLR	VQFN	RSL	48	2500	552.0	367.0	38.0
TPS65178ARSLT	VQFN	RSL	48	250	552.0	185.0	36.0
TPS65178RSLR	VQFN	RSL	48	2500	552.0	367.0	38.0
TPS65178RSLT	VQFN	RSL	48	250	552.0	185.0	36.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS65178ARSLR	RSL	VQFN	48	2500	381.5	7.92	2286	0
TPS65178ARSLR.A	RSL	VQFN	48	2500	381.5	7.92	2286	0
TPS65178ARSLR.B	RSL	VQFN	48	2500	381.5	7.92	2286	0
TPS65178ARSLT	RSL	VQFN	48	250	381.5	7.92	2286	0
TPS65178ARSLT.A	RSL	VQFN	48	250	381.5	7.92	2286	0
TPS65178ARSLT.B	RSL	VQFN	48	250	381.5	7.92	2286	0
TPS65178RSLR	RSL	VQFN	48	2500	381.5	7.92	2286	0
TPS65178RSLR.A	RSL	VQFN	48	2500	381.5	7.92	2286	0
TPS65178RSLR.B	RSL	VQFN	48	2500	381.5	7.92	2286	0
TPS65178RSLT	RSL	VQFN	48	250	381.5	7.92	2286	0
TPS65178RSLT.A	RSL	VQFN	48	250	381.5	7.92	2286	0
TPS65178RSLT.B	RSL	VQFN	48	250	381.5	7.92	2286	0

GENERIC PACKAGE VIEW

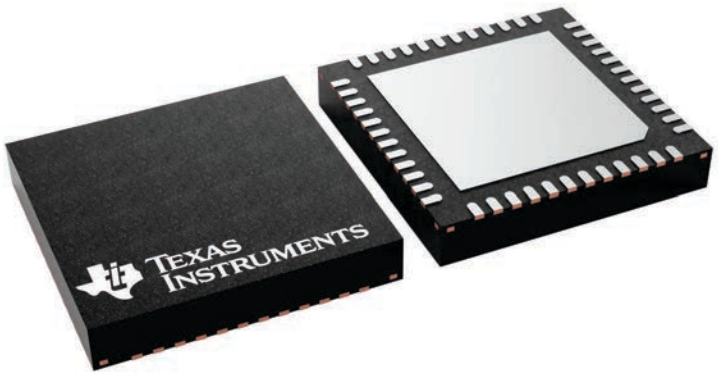
RSL 48

VQFN - 1 mm max height

6 x 6, 0.4 mm pitch

QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



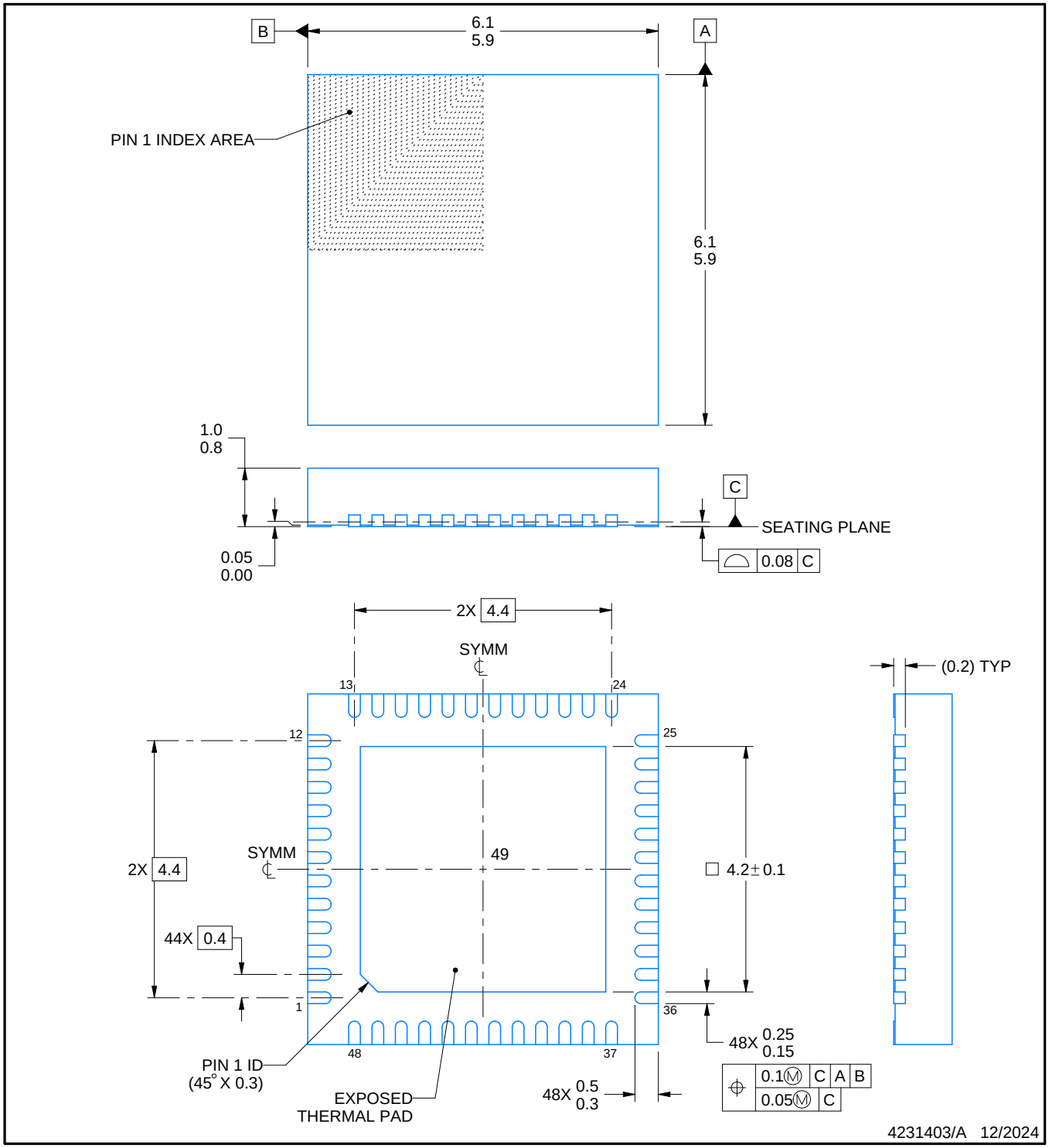
4225749/A

RSL0048G

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

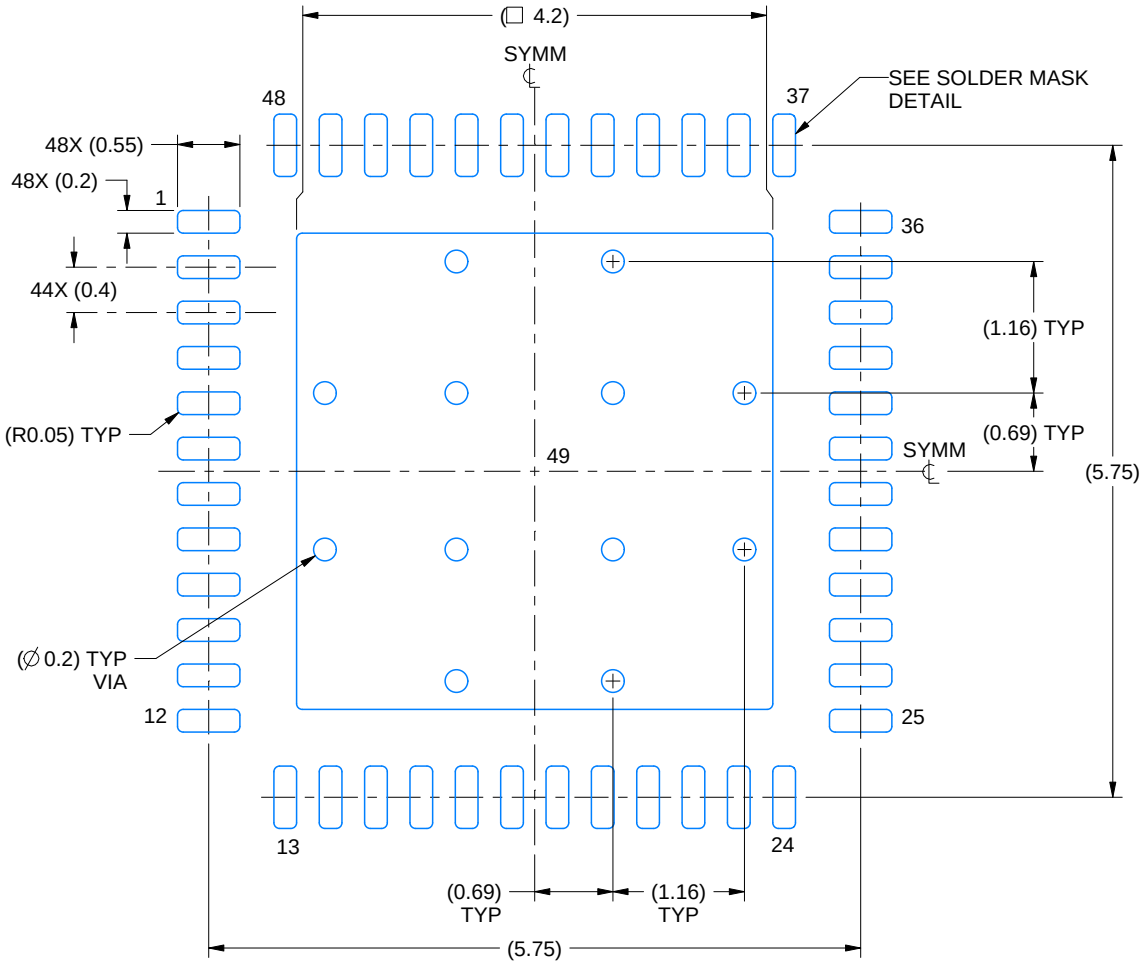
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

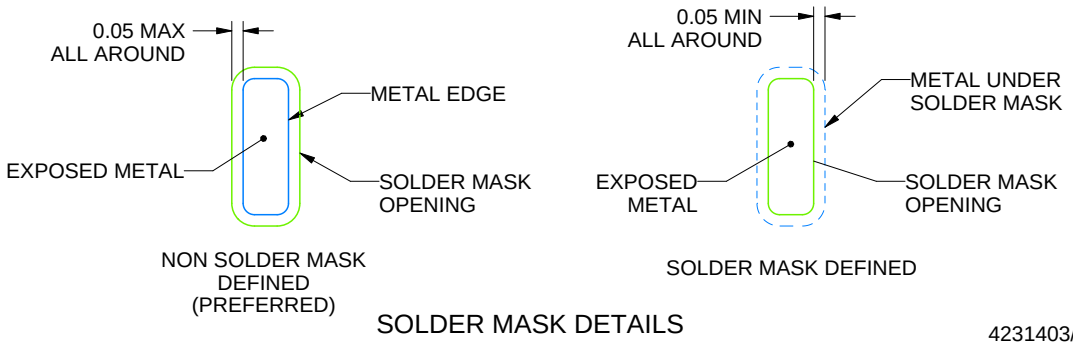
RSL0048G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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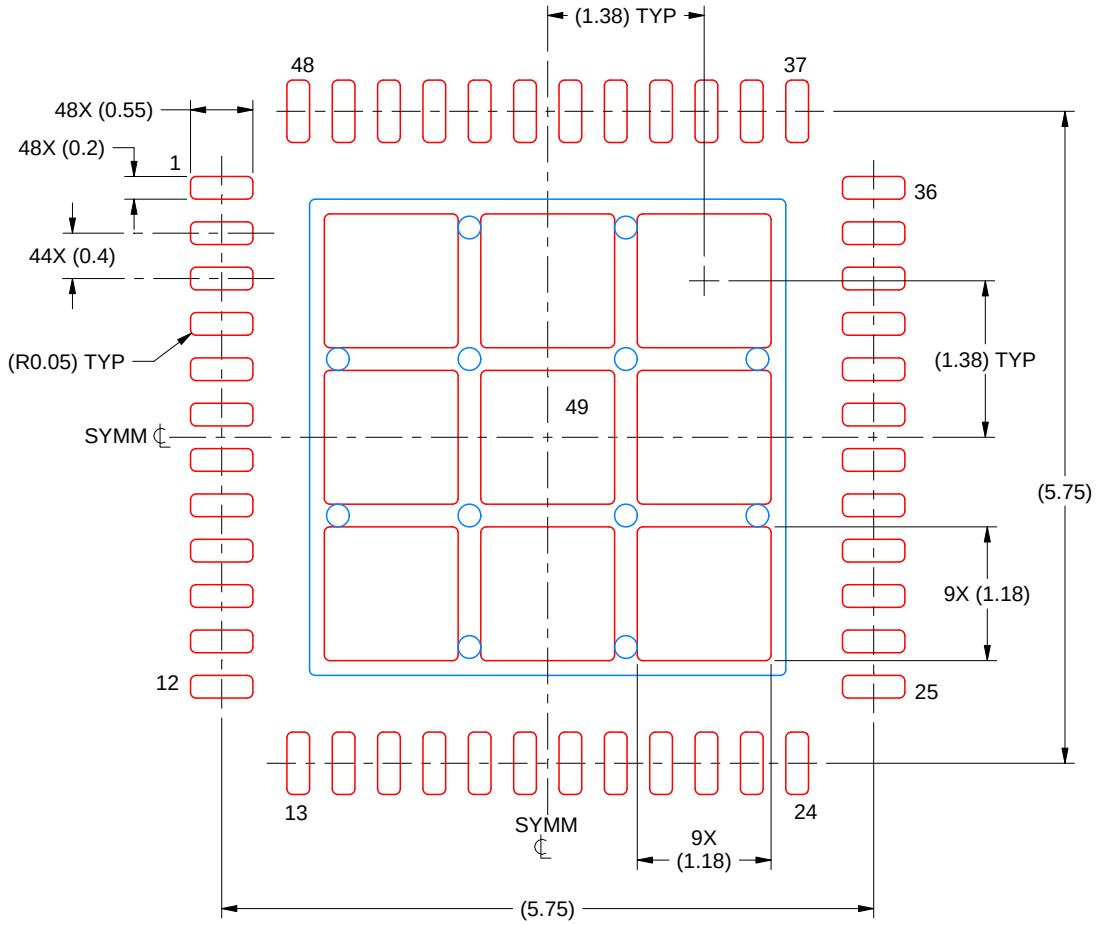
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 49
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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