TPS65090

具有开关模式充电器（用于 2-3 节串联电池）的前端电源管理单元 (PMU)

Data Manual

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具有开关模式充电器（用于 2-3 节串联电池）的前端电源管理单元 (PMU)

1 介绍

1.1 特性

- 宽输入电压充电器/电源路径管理：
  - 6V 至 17V 的 $V_{输入}$范围
  - 电源路径上高达 4A 的输出电流
  - 开关模式充电器；高达 4A 的最大充电电流
  - 与日本电子情报技术产业协会 (JEITA) 标准兼容的充电控制
  - 热调节、安全定时器
  - 2 个温度感测输入
- 3 个降压转换器：
  - 宽输出电流范围上的高效率
  - 6V 至 17V 的 $V_{输入}$范围
  - 2 个固定输出电压（5.0V 和 3.3V）
    - 高达 5A 的持续输出电流
  - 1 个可调输出电压（在 1.0V 和 5.0V 之间）
    - 高达 4A 的持续输出电流
  - 输出电压精度 ±1%
  - 每个转换器的静态电流典型值为 30μA
- 2 个常开低压降稳压器 (LDO) 的：
  - 2 个固定输出电压（5V 和 3.3V）
  - 输出电压精度 ±1%
  - 每 LDO 典型值为 10μA 的静态电流
- 7 个限流负载开关：
  - 一个具有 1A 电流限值的系统电压开关
  - 一个具有 200mA 电流限值的 5V 开关，受到反向电压保护
  - 一个具有 3A 电流限值的 3.3V 开关
  - 四个具有 1A 电流限值的 3.3V 开关
  - 所有开关由 I^2C 接口控制
- I^2C 接口
  - 所支持的标准模式 (100kHz)
  - 所支持的快速模式 (400kHz)
  - 所支持的快速模式增强型 (1000kHz)
  - 所支持的高速模式 (3.4MHz)
- 16 通道，10 位 A/D 转换器
- 采用 9mm x 9mm，超薄型四方扁平无引线 (VQFN)-100 封装

1.2 应用范围

- 使用 2-3 节串联锂电池的电池供电产品
- 笔记本电脑
- 移动个人电脑 (PC) 和移动互联网器件
- 工业计量设备
- 个人医疗产品

1.3 说明

TPS65090 是一款用于便携式应用的单芯片电源管理集成电路 (IC)，此器件包含一个支持双重或三重锂离子或锂聚合物电池组电源路径管理的电池充电器。 此充电器可直接连接至一个外部墙上适配器。 三个高效降压转换器专门用来提供一个固定 5V 系统电压、一个固定 3.3V 系统电压和一个可调电压轨。 为了在最大可能的负载电流范围内实现最大效率，这些降压转换器在轻负载时进入低功率模式。 这些降压转换器允许使用小型电感器和电容器以实现一个小型解决方案尺寸。 TPS65090还集成了两个通用常开 LDO，这两个 LDO 在关断时为控制系统的电路区块供电。 每个 LDO 的运行输入电压范围介于 6V 和 17V 之间，从而使得它们能够由墙上适配器或直接由主电池组供电。

此器件还内置了 7 个负载开关。 它们可被用来针对应用电路中的特定电路区块来对电源进行单独控制。 流经负载开关的电流，以及降压转换器的输出电流，来自交流适配器的输入电流和充电电流受到监控并可使用数字接口读出。

这些装置包含有限的内置 ESD 保护。

存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

2 DEVICE SPECIFICATION

2.1 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
POWER PATH CONTROL				
Voltage range(2)	VAC, VACS	-0.3	30	V
	ACP, ACN, ACS, BATG	–0.3	20	V
Differential Voltage	between ACP and ACN	-0.5	0.5	V
	between ACG and ACS	–0.3	7	V
CHARGER				
Voltage range(2)	VSYSC, VBAT, LC, SRP, SRN, STAT	–0.3	20	V
	FBC, TS1, TS2, VREFT	–0.3	7	V
	ENC	–0.3	3.6	V
Differential Voltage	between SRP and SRN	-0.5	0.5	V
	between CBC and LC	-0.3	7	V
DC-DC1				
Voltage range(2)	VSYS1, L1	–0.3	20	V
	FB1, VDCDC1	–0.3	7	V
	EN1	–0.3	3.6	V
Differential Voltage	between CB1 and L1	-0.3	7	V
DC-DC2				
Voltage range(2)	VSYS2, L2	–0.3	20	V
	FB2, VDCDC2	–0.3	3.6	V
	EN2	–0.3	3.6	V
Differential Voltage	between CB2 and L2	-0.3	7	V
DC-DC3				
Voltage range(2)	VSYS3, L3	–0.3	20	V
	FB3, VDCDC3	–0.3	7	V
	EN3	–0.3	3.6	V
Differential Voltage	between CB3 and L3	-0.3	7	V
LDO1				
Voltage range(2)	VSYS_L1	–0.3	20	V
	VLDO1, FB_L1	–0.3	7	V
LDO2				
Voltage range(2)	VSYS_L2	–0.3	20	V
	VLDO2, FB_L2	–0.3	3.6	V
FET1				
Voltage range(2)	INFET1, VFET1	–0.3	20	V
FET2				
Voltage range(2)	INFET2, VFET2	–0.3	6	V
FET3				
Voltage range(2)	INFET3, VFET3	–0.3	6	V
FET4				
Voltage range(2)	INFET4, VFET4	–0.3	6	V
FET5				

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.

ABSOLUTE MAXIMUM RATINGS *(continued)*

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage range[2]	INFET5, VFET5	–0.3	6	V
FET6				
Voltage range[2]	INFET6, VFET6	–0.3	6	V
FET7				
Voltage range[2]	INFET7, VFET7	–0.3	6	V
Digital Interface / Control				
Voltage range[2]	SDAT, SCLK, IRQ, VCTRL, VCTRL2, VACG, VSYSG, VBATG	–0.3	7	V
	VREFADC, VREF	–0.3	3.6	V
GENERAL				
Temperature range	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C
ESD rating[3]	Human Body Model - (HBM)		2	kV
	Charge Device Model - (CDM)		0.5	kV

(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

2.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
POWER PATH CONTROL				
Supply voltage at VAC	6.0		17	V
Differential voltage between ACP and ACN	-0.2		0.2	V
CHARGER				
Supply voltage at VSYSC, VBAT	6.0		17	V
Differential voltage between SRP and SRN	-0.2		0.2	V
DCDC1				
Supply voltage at VSYS1	6.0		17	V
DCDC2				
Supply voltage at VSYS2	6.0		17	V
DCDC3				
Supply voltage at VSYS3	6.0		17	V
LDO1				
Supply voltage at VSYS_L1	6.0		17	V
LDO2				
Supply voltage at VSYS_L2	6.0		17	V
FET1				
Supply voltage at INFET1	5.0		17	V
FET2				
Supply voltage at INFET2	4.5		5.5	V
FET3				
Supply voltage at INFET3	3.0		5.5	V
FET4				
Supply voltage at INFET4	3.0		5.5	V
FET5				
Supply voltage at INFET5	3.0		5.5	V
FET6				
Supply voltage at INFET6	3.0		5.5	V

RECOMMENDED OPERATING CONDITIONS *(continued)*

	MIN	NOM	MAX	UNIT
FET7				
Supply voltage at INFET7	3.0		5.5	V
CONTROL				
Supply voltage at VCTRL2	3.0		5.5	V
GENERAL				
Operating free air temperature range, T_A	–40		85	°C
Operating junction temperature range, T_J	–40		125	°C

2.3 THERMAL INFORMATION

THERMAL METRIC[(1)]		TPS65090 RVN 100 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	24.8	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	5.6	
θ_{JB}	Junction-to-board thermal resistance	3.9	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	3.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	0.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

2.4 ELECTRICAL CHARACTERISTICS - POWER PATH CONTROL

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VAC overvoltage disconnect		17	17.6	18.2	V
	VAC overvoltage hysteresis			550		mV
	VAC undervoltage lockout	V_{AC} voltage decreasing	5.0	5.5	6.0	V
	VAC undervoltage lockout hysteresis			550		mV
	Maximum input DPM current programming range		1000		4000	mA
	(V_{ACP} - V_{ACN}) voltage to maximum input DPM current gain			100		A / V
	Input DPM current regulation	V_{ACP} - V_{ACN}, IACSET = 0	40	44	48	mV
		V_{ACP} - V_{ACN}, IACSET = 1	36	40	44	mV
	Maximum battery discharge current comparator threshold	V_{BAT} - V_{SRN}, IBATSET = 0, T_A = 25 °C	17.5	20	21	mV
		V_{BAT} - V_{SRN}, IBATSET = 1, T_A = 25 °C	15	17.5	18.5	mV
	VACS input impedance			1000		kΩ
	VAC input impedance			25		kΩ
	Gate drive current on ACG		12			µA
	Gate drive current on BATG	turn on	500			µA
	Gate drive current on BATG	turn off	25			mA
	BATG turn off delay time after adapter is detected			30		ms
	Quiescent current into VAC	charging enabled, V_{AC} = 11.5 V		2.5	5	mA
		charging disabled, V_{AC} = 11.5 V		1	1.5	mA
	Leakage current into ACP and ACN	charging disabled			80	µA
V_{SUPPL}	Supplement threshold to turn on battery switch	V_{SRN} - V_{ACN} rising	13	45	84	mV

ELECTRICAL CHARACTERISTICS - POWER PATH CONTROL *(continued)*

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SUPPL_HYS}	Supplement mode hysteresis to turn off battery switch	V_{SRN} - V_{ACN} falling		20		mV
I_{ACRC}	Reverse adapter current threshold	V_{ACN} - V_{ACP} rising		45		mV
V_{SLEEP}	SLEEP mode threshold	V_{AC} – V_{SRN} falling	20	90	150	mV
V_{SLEEP_HYS}	SLEEP mode hysteresis	V_{AC} – V_{SRN} rising		200		mV

2.5 ELECTRICAL CHARACTERISTICS - CHARGER

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGER - POWER						
V_{FBC}	Charger feedback voltage	VSET = 00, default for T_{01} and T_{40}	1.98	2.0	2.02	V
		VSET = 01, default for T_{12}	2.03	2.05	2.07	
		VSET = 10, default for T_{34}	2.055	2.075	2.095	
		VSET = 11, default for T_{23}	2.08	2.1	2.12	
	Leakage current into FBC				0.1	μA
V_{FBCR}	Charger feedback voltage for automatic charge restart	VSET = 00, ENRECG = 1	1.925	1.950	1.975	V
		VSET = 01, ENRECG = 1	1.975	2.0	2.025	
		VSET = 10, ENRECG = 1	2.0	2.025	2.05	
		VSET = 11, ENRECG = 1	2.025	2.05	2.075	
I_{CHARGE}	Maximum charge current programming range		1000		4000	mA
	(V_{SRP} - V_{SRN}) voltage to maximum charge current gain			100		A / V
	I2C programmable charge current	ISET = 000		0		%
		ISET = 001		25		%
		ISET = 010		37.5		%
		ISET = 011, default for T_{12} and T_{34} battery temperature range		50		%
		ISET = 100		62.5		%
		ISET = 101		75		%
		ISET = 110		87.5		%
		ISET = 111, default for T_{23} battery temperature range		100		%
	Charge current sense regulation voltage	V_{SRP} - V_{SRN} = 40 mV typical, T_J < 100 °C	38.5	40	42.5	mV
		V_{SRP} - V_{SRN} = 20 mV typical, T_J < 100 °C	18.5	20	22.0	
		V_{SRP} - V_{SRN} = 4 mV typical, T_J < 100 °C	2.3	4	5.9	
	minimum programmable charge current			100		mA
	Precharge current			0.1 * I_{CHARGE}		
	Termination current			0.1 * I_{CHARGE}		
	Leakage current into SRN and SRP	V_{BAT} < 12 V			45	μA
	Switching frequency		1360	1600	1840	kHz
R_{DSON}	High side switch on resistance			25		mΩ

ELECTRICAL CHARACTERISTICS - CHARGER *(continued)*

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DSON}	Low side switch on resistance			60		mΩ
CHARGER - CONTROL						
	Precharge timer		1600	1800	2000	s
	Fastcharge safety timer programming range		2		10	h
	Fastcharge safety timer accuracy				10%	
	I2C programmable values for fastcharge safety timer	FASTTIME = 000, default setting		2		h
		FASTTIME = 001		3		h
		FASTTIME = 010		4		h
		FASTTIME = 011		5		h
		FASTTIME = 100		6		h
		FASTTIME = 101		7		h
		FASTTIME = 110		8		h
		FASTTIME = 111		10		h
	Battery detection discharge timer			1		s
	Battery detection discharge current		5		20	mA
	Battery detection discharge current after timer fault			2		mA
V_{FBCL}	Battery detection discharge feedback voltage threshold for battery ok		1.43	1.45	1.47	V
	Battery feedback voltage threshold for precharge to fastcharge transition		1.43	1.45	1.47	V
	Battery detection charge timer			0.5		s
	Battery detection charge current sense regulation voltage	V_{SRP} - V_{SRN} = 2 mV typical, T_J < 100 °C	0.5	2	3.8	mV
	Battery detection charge feedback voltage threshold for battery ok	VSET = 00	1.925	1.95	1.975	V
		VSET = 01	1.975	2.0	2.025	
		VSET = 10	2.0	2.025	2.05	
		VSET = 11	2.025	2.05	2.075	
	Minimum battery feedback voltage for battery good detection	voltage at FBC increasing	1.44	1.5	1.54	V
	Maximum battery feedback voltage for battery good detection	voltage at FBC increasing	2.18	2.25	2.28	V
	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS}, I2C programming option for T_1	sensor temperature is -10°C, T_SET = 000	71.9	72.4	72.9	%
	Voltage ratio threshold hysteresis	sensor temperature is -10°C, voltage decreasing		0.2		%
T_1	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS}	default value, Sensor temperature is 0°C, T_SET = 001	70.4	71.0	71.5	%
	Voltage ratio threshold hysteresis	sensor temperature is 0°C, voltage decreasing		0.2		%
T_2	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS}	default value, Sensor temperature is 10°C, T_SET = 010	68.1	68.7	69.2	%
	Voltage ratio threshold hysteresis	sensor temperature is 10°C, voltage decreasing		0.4		%
	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS}, I2C programming option for T_2	sensor temperature is 15°C, T_SET = 011	67.0	67.4	67.9	%
	Voltage ratio threshold hysteresis	sensor temperature is 15°C, voltage decreasing		0.4		%

ELECTRICAL CHARACTERISTICS - CHARGER *(continued)*

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS}, I2C programming option for T_3	sensor temperature is 40°C, T_SET = 100	59.3	59.7	60.1	%
	Voltage ratio threshold hysteresis	sensor temperature is 40°C, voltage increasing		0.9		%
T_3	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS}	default value, Sensor temperature is 45°C, T_SET = 101	57.1	57.6	57.9	%
	Voltage ratio threshold hysteresis	sensor temperature is 45°C, voltage increasing		0.9		%
	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS}, I2C programming option for T_3 or T_4	sensor temperature is 50°C, T_SET = 110	54.7	55.2	55.8	%
	Voltage ratio threshold hysteresis	sensor temperature is 50°C, voltage increasing		1.1		%
T_4	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS}	default value, Sensor temperature is 60°C, T_SET = 111	49.6	50.1	50.5	%
	Voltage ratio threshold hysteresis	sensor temperature is 60°C, voltage increasing		1.1		%
	Output voltage at VREFT	internally connected to VLDO2		3.3		V
	Output impedance of VREFT			4		kΩ
	Quiescent current into VBAT	charging active			25	µA
	Quiescent current into VBAT	charging suspended			150	µA
V_{IL}	ENC input low voltage				0.4	V
V_{IH}	ENC input high voltage		1.2			V
	ENC input current	Clamped on GND or 3.3V		0.01	0.1	µA
	Charge current derating starting temperature	junction temperature increasing		100		°C
	Charge current derating starting voltage	V_{SYSC} decreasing	6.7	7.3	7.6	V
	Overtemperature protection		125	140	150	°C
	Overtemperature hysteresis			20		°C

2.6 ELECTRICAL CHARACTERISTICS - DCDC CONVERTERS

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DCDC1 - POWER						
	Output voltage	Power save mode disabled	5.0	5.05	5.125	V
	Switch valley current limit	T_A = 25°C	5500			mA
	High side switch on resistance			20		mΩ
	Low side switch on resistance			20		mΩ
	Maximum line regulation			0.5		%
	Maximum load regulation			0.5		%
	Output auto discharge resistance			300	400	Ω
	FB1 input impedance	V_{EN1} = 1		1		MΩ
	Shutdown current into VSYS1	V_{SYS1} = 7.2 V, EN1 = 0			1	µA
DCDC1 - CONTROL						
V_{IL}	EN1 input low voltage				0.4	V
V_{IH}	EN1 input high voltage		1.2			V
	EN1 input current	Clamped on GND or 3.3 V		0.01	0.1	µA

ELECTRICAL CHARACTERISTICS - DCDC CONVERTERS *(continued)*

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C
DCDC2 - POWER						
	Output voltage	Power save mode disabled	3.3	3.333	3.383	V
	Switch valley current limit	T_A = 25°C	5500			mA
	High side switch on resistance			20		mΩ
	Low side switch on resistance			20		mΩ
	Maximum line regulation			0.5		%
	Maximum load regulation			0.5		%
	Output auto discharge resistance			300	400	Ω
	FB2 input impedance	V_{EN2} = 1		1		MΩ
	Shutdown current into VSYS2	V_{SYS2} = 7.2 V, EN2 = 0			1	µA
DCDC2 - CONTROL						
V_{IL}	EN2 input low voltage				0.4	V
V_{IH}	EN2 input high voltage		1.2			V
	EN2 input current	Clamped on GND or 3.3 V		0.01	0.1	µA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C
DCDC3 - POWER						
	Feedback voltage		792	800	808	mV
	Switch valley current limit	T_A = 25°C	4200			mA
	High side switch on resistance			20		mΩ
	Low side switch on resistance			20		mΩ
	Maximum line regulation			0.5		%
	Maximum load regulation			0.5		%
	Output auto discharge resistance			300	400	Ω
	Leakage current into FB3				0.1	µA
	Shutdown current into VSYS3	V_{SYS3} = 7.2 V, EN3 = 0			1	µA
DCDC3 - CONTROL						
V_{IL}	EN3 input low voltage				0.4	V
V_{IH}	EN3 input high voltage		1.2			V
	EN3 input current	Clamped on GND or 3.3 V		0.01	0.1	µA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C

2.7 ELECTRICAL CHARACTERISTICS - LINEAR REGULATORS

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO1						
	Output voltage	$I_{OUTLDO1}$ = 1 mA	4.90	4.95	5.0	V
	LDO1 current limit	T_A = 25°C	30	50	120	mA
	LDO1 maximum output current	DCDC1 active (bypass switch turned on), V_{SYS} = 7.5 V		120		mA
	Maximum line regulation			0.5		%

ELECTRICAL CHARACTERISTICS - LINEAR REGULATORS *(continued)*

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum load regulation			0.5		%
FB_L1 input impedance			1		MΩ
Quiescent current into VSYS_L1 and VSYS_L2	DCDC1 and DCDC2 are enabled			35	µA
Overtemperature protection			140		°C
Overtemperature hysteresis			20		°C
LDO2					
Output voltage	$I_{OUTLDO2}$ = 1 mA	3.233	3.267	3.3	V
LDO2 current limit	T_A = 25°C	30	50	120	mA
LDO2 maximum output current	DCDC2 active (bypass switch turned on), V_{SYS} = 7.5 V		120		mA
Maximum line regulation			0.5		%
Maximum load regulation			0.5		%
FB_L2 input impedance			1		MΩ
Quiescent current into VSYS_L2 and VSYS_L1	DCDC1 and DCDC2 are enabled			35	µA
Overtemperature protection			140		°C
Overtemperature hysteresis			20		°C

2.8 ELECTRICAL CHARACTERISTICS - LOAD SWITCHES

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FET1					
Overcurrent detect threshold	T_A = 25°C	1000		1200	mA
Switch on resistance				120	mΩ
Output auto discharge resistance			800		Ω
Maximum output voltage slew rate after turn on		0.1	0.5	1	V / µs
Switch current limit - timeout	multiplier set to 1, WTFET1 = 00	200		250	µs
Switch current limit - timeout	multiplier set to 4, WTFET1 = 01	800		1000	µs
Switch current limit - timeout	multiplier set to 8, WTFET1 = 10	1600		2000	µs
Switch current limit - timeout	multiplier set to 16, WTFET1 = 11	3200		4000	µs
Leakage current into INFET1	FET1 disabled, V_{FET1} = 0 V		1		µA
FET2					
Overcurrent detect threshold	T_A = 25°C	200		240	mA
Switch on resistance				500	mΩ
Output auto discharge resistance			300		Ω
Maximum output voltage slew rate after turn on		0.1	0.5	1	V / µs
Switch current limit - timeout	multiplier set to 1, WTFET2 = 00	200		250	µs
Switch current limit - timeout	multiplier set to 4, WTFET2 = 01	800		1000	µs
Switch current limit - timeout	multiplier set to 8, WTFET2 = 10	1600		2000	µs
Switch current limit - timeout	multiplier set to 16, WTFET2 = 11	3200		4000	µs
Shutdown current into INFET2	FET2 disabled, V_{FET2} = 0 V		5		µA
Reverse leakage current	FET disabled, VFET2 > INFET2		10		µA
FET3					
Overcurrent detect threshold	T_A = 25°C	3000		3600	mA
Switch on resistance				45	mΩ

ELECTRICAL CHARACTERISTICS - LOAD SWITCHES *(continued)*

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output auto discharge resistance			300		Ω
Maximum output voltage slew rate after turn on		0.1	0.5	1	V / µs
Switch current limit - timeout	multiplier set to 1, WTFET3 = 00	200		250	µs
Switch current limit - timeout	multiplier set to 4, WTFET3 = 01	800		1000	µs
Switch current limit - timeout	multiplier set to 8, WTFET3 = 10	1600		2000	µs
Switch current limit - timeout	multiplier set to 16, WTFET3 = 11	3200		4000	µs
Leakage current into INFET3	FET3 disabled, V_{FET3} = 0 V		3		µA
FET4					
Overcurrent detect threshold	T_A = 25°C	1000		1200	mA
Switch on resistance				80	mΩ
Output auto discharge resistance			300		Ω
Maximum output voltage slew rate after turn on		0.1	0.5	1	V / µs
Switch current limit - timeout	multiplier set to 1, WTFET4 = 00	200		250	µs
Switch current limit - timeout	multiplier set to 4, WTFET4 = 01	800		1000	µs
Switch current limit - timeout	multiplier set to 8, WTFET4 = 10	1600		2000	µs
Switch current limit - timeout	multiplier set to 16, WTFET4 = 11	3200		4000	µs
Leakage current into INFET4	FET4 disabled, V_{FET4} = 0 V		1		µA
FET5					
Overcurrent detect threshold	T_A = 25°C	1000		1200	mA
Switch on resistance				80	mΩ
Output auto discharge resistance			300		Ω
Maximum output voltage slew rate after turn on		0.1	0.5	1	V / µs
Switch current limit - timeout	multiplier set to 1, WTFET5 = 00	200		250	µs
Switch current limit - timeout	multiplier set to 4, WTFET5 = 01	800		1000	µs
Switch current limit - timeout	multiplier set to 8, WTFET5 = 10	1600		2000	µs
Switch current limit - timeout	multiplier set to 16, WTFET5 = 11	3200		4000	µs
Leakage current into INFET5	FET5 disabled, V_{FET5} = 0 V		1		µA
FET6					
Overcurrent detect threshold	T_A = 25°C	1000		1200	mA
Switch on resistance				80	mΩ
Output auto discharge resistance			300		Ω
Maximum output voltage slew rate after turn on		0.1	0.5	1	V / µs
Switch current limit - timeout	multiplier set to 1, WTFET6 = 00	200		250	µs
Switch current limit - timeout	multiplier set to 4, WTFET6 = 01	800		1000	µs
Switch current limit - timeout	multiplier set to 8, WTFET6 = 10	1600		2000	µs
Switch current limit - timeout	multiplier set to 16, WTFET6 = 11	3200		4000	µs
Leakage current into INFET6	FET6 disabled, V_{FET6} = 0 V		1		µA
FET7					
Overcurrent detect threshold	T_A = 25°C	1000		1200	mA
Switch on resistance				80	mΩ
Output auto discharge resistance			300		Ω
Maximum output voltage slew rate after turn on		0.1	0.5	1	V / µs
Switch current limit - timeout	multiplier set to 1, WTFET7 = 00	200		250	µs
Switch current limit - timeout	multiplier set to 4, WTFET7 = 01	800		1000	µs
Switch current limit - timeout	multiplier set to 8, WTFET7 = 10	1600		2000	µs

ELECTRICAL CHARACTERISTICS - LOAD SWITCHES *(continued)*

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Switch current limit - timeout	multiplier set to 16, WTFET7 = 11	3200		4000	µs
	Leakage current into INFET7	FET7 disabled, V_{FET7} = 0 V		1		µA

2.9 ELECTRICAL CHARACTERISTICS - CONTROL

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM - CONTROL						
	VBATG, VACG, VSYSG, IRQ output low voltage	I_{VxxxGL} = 1 mA		0.04	0.4	V
	VBATG, VACG, VSYSG, IRQ output leakage current			0.01	0.4	µA
	STAT output low voltage	I_{STAT} = 1 mA		0.04	0.4	V
	STAT output low voltage	I_{STAT} = 5 mA			0.6	V
	STAT output leakage current			0.01	0.1	µA
	System under voltage lockout threshold	V_{SYS} voltage decreasing	5.5	5.6	5.7	V
	System under voltage lockout threshold hysteresis			300		mV
	LDO under voltage lockout threshold	V_{SYS} voltage decreasing	4.4	4.6	4.7	V
	LDO under voltage lockout threshold hysteresis			300		mV
V_{IL}	SDA, SCL input low voltage				0.4	V
V_{IH}	SDA, SCL input high voltage		1.2			V
	SDA, SCL input current	Clamped on GND or 3.3 V		0.01	0.3	µA
	SDA output low voltage	I_{SDA} = 5 mA		0.04	0.4	V
AD - CONVERTER						
	ADC resolution			10		Bits
	Differential linearity error			±1		LSB
	Offset error			1	5	LSB
	Offset error, voltage				12.7	mV
	Gain error			±8		LSB
	Sampling time			150		µs
	Conversion time			20		µs
	Wait time after enable	Time needed to stabilize the internal voltages			10	ms
	Quiescent current, ADC enabled by I^2C	includes current needed for I2C block		500		µA
AD - CONVERTER - MEASUREMENT RANGES						
	Voltage on VAC		0		17	V
	Battery voltage VBAT		0		17	V
	Input current IAC	V_{ACP} - V_{ACN} is measured	0		33	mV
	Battery charge current IBAT	V_{SRP} - V_{SRN} is measured	0		40	mV
	DCDC1 output current IDCDC1		0		4	A
	DCDC2 output current IDCDC2		0		4	A
	DCDC3 output current IDCDC3		0		4	A
	FET1 output current IFET1		0		1.1	A
	FET2 output current IFET2		0		220	mA
	FET3 output current IFET3		0		3.3	A
	FET4 output current IFET4		0		1.1	A

ELECTRICAL CHARACTERISTICS - CONTROL *(continued)*

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FET5 output current IFET5		0		1.1	A
FET6 output current IFET6		0		1.1	A
FET7 output current IFET7		0		1.1	A
AD - CONVERTER - SIGNAL CONDITIONING					
Voltage sense error referenced to maximum value				2	%
Current sense error referenced to maximum value for IAC and IBAT				20	%
Current sense error referenced to maximum value for DCDC converter currents	measurements at VSYS > 7.2 V, low side switch duty cycle at DCDC1-3 > 30%			15	%
Current sense error referenced to maximum value for Load switch currents				10	%

2.10 ELECTRICAL CHARACTERISTICS - I²C INTERFACE TIMING(1)

over recommended free-air temperature range and over recommended input voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency	Standard-mode		100	kHz
		Fast-mode		400	kHz
		Fast-mode Plus		1000	kHz
		High-speed mode, C_b – 100 pF max		3.4	MHz
		High-speed mode, C_b – 400 pF max(2)		1.7	MHz
t_{BUF}	Bus free time between a STOP and START condition	Standard-mode	4.7		µs
		Fast-mode	1.3		µs
		Fast-mode Plus	0.5		µs
$t_{HD;\ STA}$	Hold time (repeated) START condition	Standard-mode	4		µs
		Fast-mode	600		ns
		Fast-mode Plus	260		ns
		High-speed mode	160		ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7		µs
		Fast-mode	1.3		µs
		Fast-mode Plus	0.5		µs
		High-speed mode, C_b – 100 pF max	160		ns
		High-speed mode, C_b – 400 pF max(2)	320		ns
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4		µs
		Fast-mode	600		ns
		Fast-mode Plus	260		ns
		High-speed mode, C_b – 100 pF max	60		ns
		High-speed mode, C_b – 400 pF max(2)	120		ns
$t_{SU;\ STA}$	Setup time for a repeated START condition	Standard-mode	4.7		µs
		Fast-mode	600		ns
		Fast-mode Plus	260		ns
		High-speed mode	160		ns

(1) All values referred to V_{IH} min and V_{IH} max levels.
(2) For bus line loads C_b between 100 pF and 400 pF, the timing parameters must be linearly interpolated.

ELECTRICAL CHARACTERISTICS - I²C INTERFACE TIMING(1) *(continued)*

over recommended free-air temperature range and over recommended input voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{SU;\,DAT}$	Data setup time	Standard-mode	250		ns
		Fast-mode	100		ns
		Fast-mode Plus	50		ns
		High-speed mode	10		ns
$t_{HD;\,DAT}$	Data hold time	Standard-mode	1	3450	ns
		Fast-mode	1	900	ns
		Fast-mode Plus	1		ns
		High-speed mode, C_b – 100 pF max	1 (3)	70	ns
		High-speed mode, C_b – 400 pF max (2)	1 (3)	150	ns
t_{rCL}	Rise time of SCL signal	Standard-mode		1000	ns
		Fast-mode	20	300	ns
		Fast-mode Plus		120	ns
		High-speed mode, C_b – 100 pF max	10	40	ns
		High-speed mode, C_b – 400 pF max (2)	20	80	ns
t_{rCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard-mode		1000	ns
		Fast-mode	20	300	ns
		Fast-mode Plus		120	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max (2)	20	160	ns
t_{fCL}	Fall time of SCL signal	Standard-mode		300	ns
		Fast-mode	20 x (V_{DD} / 5.5 V)	300	ns
		Fast-mode Plus	20 x (V_{DD} / 5.5 V)	120	ns
		High-speed mode, C_b – 100 pF max	10	40	ns
		High-speed mode, C_b – 400 pF max (4)	20	80	ns
t_{rDA}	Rise time of SDA signal	Standard-mode		1000	ns
		Fast-mode	20	300	ns
		Fast-mode Plus		120	ns
		High-speed mode, C_b – 100 pF max	10	80	ns
		High-speed mode, C_b – 400 pF max (4)	20	160	ns
t_{fDA}	Fall time of SDA signal	Standard-mode		300	ns
		Fast-mode	20 x (V_{DD} / 5.5 V)	300	ns
		Fast-mode Plus	20 x (V_{DD} / 5.5 V)	120	ns
		High-speed mode, C_b – 100 pF max	10	80	ns
		High-speed mode, C_b – 400 pF max (4)	20	160	ns
$t_{SU;\,STO}$	Setup time for STOP condition	Standard-mode	4		μs
		Fast-mode	600		ns
		Fast-mode Plus	260		ns
		High-speed mode	160		ns
C_b	Capacitive load for SDA and SCL			400	pF

(3) A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.
(4) For bus line loads C_b between 100 pF and 400 pF, the timing parameters must be linearly interpolated.

2.11 PIN ASSIGNMENTS

RVN PACKAGE
(TOP VIEW)

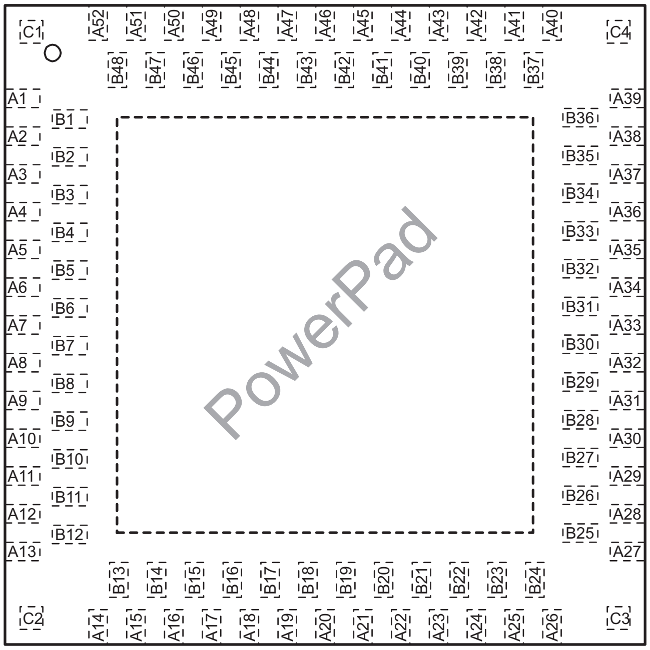


Table 2-1. Pin Functions

Pin NAME	Pin NO.	I/O	DESCRIPTION
POWER PATH CONTROL			
VAC	A13	I	AC adaptor supply input for charger control
VACS	A14	I	AC adaptor sense input for the charger
ACG	A51	O	Gate connection for AC adaptor input switches
ACS	B48		Source connection for AC adaptor input switches
ACP	B47	I	Shunt resistor sense connection for input current sensing
ACN	A50	I	Shunt resistor sense connection for input current sensing
BATG	A2	O	Gate connection for the battery switch
CHARGER			
VSYSC	A3, A4, B3	I	Switchmode battery charger step down converter supply voltage
LC	A5, B4, B5		Inductor connection for switchmode battery charger step down converter
PGNDC	A6, B6		
CBC	B2		Bootstrap capacitor connection for charger step down converter
FBC	A52	I	Voltage feedback input for charger step down converter. Must be connected to an external feedback divider to program charge voltage.
VBAT	A15	I	Battery sense connection
SRP	A1	I	Shunt resistor connection for battery charge current sensing
SRN	B1	I	Shunt resistor connection for battery charge current sensing
ENC	A41	I	Enable input for charger (1: enabled, 0: disabled), must be connected to a valid logic signal
VREFT	A25	I	Reference voltage output for temperature measurements
TS1	A24	I	Temperature sensor input for temperature sensor 1
TS2	B23	I	Temperature sensor input for temperature sensor 2
VACG	A39	O	VAC good pin, open drain (1, high impedance : voltage good; 0 : voltage not available)
VSYSG	B36	O	VSYS good pin, open drain (1, high impedance : voltage good; 0 : voltage not available)

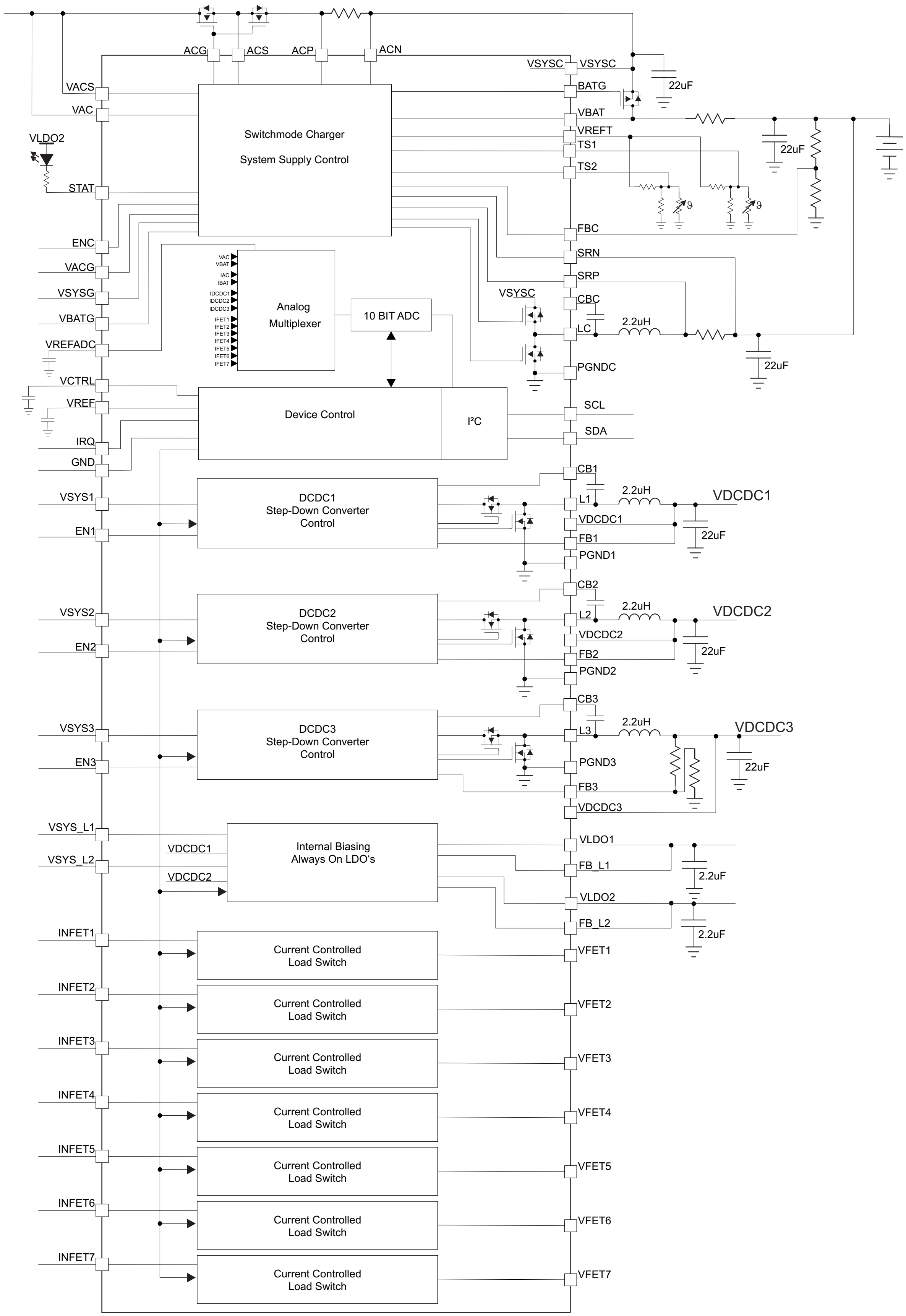
Table 2-1. Pin Functions (continued)

Pin NAME	Pin NO.	I/O	DESCRIPTION
VBATG	A38	O	VBAT good pin, open drain (1, high impedance : voltage good; 0 : voltage not available), pull up voltage should not be higher than voltage connected to
STAT	B13	O	Charge status pin, open drain (charge in progress, charge complete, sleep mode, fault)
DCDC1			
VSYS1	A46, A47, B43	I	Supply voltage input for DCDC1 step down converter
L1	A45, B41, B42		Inductor connection for DCDC1 step down converter
PGND1	A43, A44, B40		
CB1	B44		Bootstrap capacitor connection for DCDC1
FB1	B37	I	Output voltage sense input for DCDC1
VDCDC1	A48	I	Output voltage connection of DCDC1
EN1	B38	I	Enable input for DCDC1 (1: enabled, 0: disabled), must be connected to a valid logic signal
DCDC2			
VSYS2	A19, A20, B18	I	Supply voltage input for DCDC2 step down converter
L2	A21, B19, B20		Inductor connection for DCDC2 step down converter
PGND2	A22, A23, B21, B22		
CB2	B17		Bootstrap capacitor connection for DCDC2
FB2	B24	I	Output voltage sense input for DCDC2
VDCDC2	A18	I	Output voltage connection of DCDC2
EN2	A42	I	Enable input for DCDC2 (1: enabled, 0: disabled), must be connected to a valid logic signal
DCDC3			
VSYS3	A10, A11, B10, B11	I	Supply voltage input for DCDC3 step down converter
L3	A9, B8, B9		Inductor connection for DCDC3 step down converter
PGND3	A7, A8, B7		
CB3	A12		Bootstrap capacitor connection for DCDC3
FB3	B14	I	Output voltage feedback input for DCDC3, a resistive feedback divider must be connected
VDCDC3	A16	I	Output voltage sense input for DCDC3
EN3	A26	I	Enable input for DCDC3 (1: enabled, 0: disabled), must be connected to a valid logic signal
LDO1			
VSYS_L1	A49	I	Supply voltage input for LDO1 linear regulator
VLDO1	B45	O	Output of the LDO1 linear regulator
FB_L1	B46	I	Output voltage sense input for LDO1
LDO2			
VSYS_L2	A17	I	Supply voltage input for LDO2 linear regulator
VLDO2	B16	O	Output of the LDO2 linear regulator
FB_L2	B15	I	Output voltage sense input for LDO2
FET1			
INFET1	B28	I	Supply voltage input for load switch FET1, connect to GND, if not used
VFET1	A30	O	Output of load switch FET1, leave unconnected if not used
FET2			
INFET2	B29	I	Supply voltage input for load switch FET2, connect to GND, if not used
VFET2	A31	O	Output of load switch FET2, leave unconnected if not used

Table 2-1. Pin Functions (continued)

Pin NAME	Pin NO.	I/O	DESCRIPTION
FET3			
INFET3	A34, B31	I	Supply voltage input for load switch FET3, connect to GND, if not used
VFET3	A32, B30	O	Output of load switch FET3, leave unconnected if not used
FET4			
INFET4	B34	I	Supply voltage input for load switch FET4, connect to GND, if not used
VFET4	A37	O	Output of load switch FET4, leave unconnected if not used
FET5			
INFET5	B33	I	Supply voltage input for load switch FET5, connect to GND, if not used
VFET5	A36	O	Output of load switch FET5, leave unconnected if not used
FET6			
INFET6	B32	I	Supply voltage input for load switch FET6, connect to GND, if not used
VFET6	A35	O	Output of load switch FET6, leave unconnected if not used
FET7			
INFET7	B27	I	Supply voltage input for load switch FET7, connect to GND, if not used
VFET7	A29	O	Output of load switch FET7, leave unconnected if not used
Digital Interface / Control			
SDA	A27	I/O	Data line for the I2C interface
SCL	B25	I/O	Clock input for the I2C interface
IRQ	B12	O	Interrupt output, open drain, (1, high impedance : no interrupt; 0 : interrupt) details on events available via I2C
AGND	A33		Analog ground
VCTRL	B39	O	Internal control supply decoupling capacitor connection
VREF	B35	O	Reference voltage decoupling capacitor connection
VREFADC	B26	O	ADC reference voltage decoupling capacitor connection
VCTRL2	A28		Not used, must be connected to either VLDO2 or VCTRL
GND	A40		Logic ground
PGND	C1, C2, C3, C4		internally connected to PowerPAD™
PowerPAD™			Must be soldered to achieve appropriate power dissipation. Must be connected to PGND.

FUNCTIONAL BLOCK DIAGRAM (TPS65090)



2.12 TYPICAL CHARACTERISTICS

Table 2-2. TABLE OF GRAPHS

DESCRIPTION		REFERENCE
Efficiency	vs Output current, DCDC1, V_{OUT} = 5 V	Figure 2-1
	vs Output current, DCDC2, V_{OUT} = 3.3 V	Figure 2-1
	vs Output current, DCDC3, V_{OUT} = 1.0 V	Figure 2-3
	vs Output current, DCDC3, V_{OUT} = 1.35 V	Figure 2-4
	vs Output current, DCDC3, V_{OUT} = 1.8 V	Figure 2-5
	vs Output current, DCDC3, V_{OUT} = 3.3 V	Figure 2-6
	vs Output current, DCDC3, V_{OUT} = 4.0 V	Figure 2-7
	vs Output current, DCDC3, V_{OUT} = 5.0 V	Figure 2-8
Efficiency	vs Output current, Charger, V_{OUT} = 8.4 V	Figure 2-9
	vs Output current, Charger, V_{OUT} = 12.6 V	Figure 2-10
Efficiency	vs Input voltage, DCDC1, V_{OUT} = 5 V	Figure 2-11
	vs Input voltage, DCDC2, V_{OUT} = 3.3 V	Figure 2-12
	vs Input voltage, DCDC3, V_{OUT} = 1.0 V	Figure 2-13
	vs Input voltage, DCDC3, V_{OUT} = 1.35 V	Figure 2-14
	vs Input voltage, DCDC3, V_{OUT} = 1.8 V	Figure 2-15
	vs Input voltage, DCDC3, V_{OUT} = 3.3 V	Figure 2-16
	vs Input voltage, DCDC3, V_{OUT} = 4.0 V	Figure 2-17
	vs Input voltage, DCDC3, V_{OUT} = 5.0 V	Figure 2-18
Efficiency	vs Battery voltage, Charger, I_{OUT} = 1.0 A	Figure 2-19
	vs Battery voltage, Charger, I_{OUT} = 2.0 A	Figure 2-20
	vs Battery voltage, Charger, I_{OUT} = 3.0 A	Figure 2-21
	vs Battery voltage, Charger, I_{OUT} = 4.0 A	Figure 2-22
Switching frequency	vs Output current, DCDC1, V_{OUT} = 5 V	Figure 2-23
	vs Output current, DCDC2, V_{OUT} = 3.3 V	Figure 2-24
	vs Output current, DCDC3, V_{OUT} = 1.35 V	Figure 2-25
	vs Input voltage, DCDC1, V_{OUT} = 5 V	Figure 2-26
	vs Input voltage, DCDC2, V_{OUT} = 3.3 V	Figure 2-27
	vs Input voltage, DCDC3, V_{OUT} = 1.35 V	Figure 2-28
Inductor current ripple	vs Output current, DCDC1, V_{OUT} = 5 V	Figure 2-29
	vs Output current, DCDC2, V_{OUT} = 3.3 V	Figure 2-30
	vs Output current, DCDC3, V_{OUT} = 1.35 V	Figure 2-31
	vs Input voltage, DCDC1, V_{OUT} = 5 V	Figure 2-32
	vs Input voltage, DCDC2, V_{OUT} = 3.3 V	Figure 2-33
	vs Input voltage, DCDC3, V_{OUT} = 1.35 V	Figure 2-34

Table 2-2. TABLE OF GRAPHS (continued)

DESCRIPTION		REFERENCE
Waveforms	Load transient response, DCDC1, V_{IN} = 11.5 V, load change from 400 mA to 5 A	Figure 2-35
	Load transient response, DCDC1, V_{IN} = 15 V, load change from 400 mA to 5 A	Figure 2-36
	Load transient response, DCDC2, V_{IN} = 11.5 V, load change from 400 mA to 5 A	Figure 2-37
	Load transient response, DCDC2, V_{IN} = 15V, load change from 400 mA to 5 A	Figure 2-38
	Load transient response, DCDC3, V_{OUT} = 1.35 V, V_{IN} = 11.5 V, load change from 400 mA to 4.4 A	Figure 2-39
	Load transient response, DCDC3, V_{OUT} = 1.35 V, V_{IN} = 15V, load change from 400 mA to 4.4 A	Figure 2-40
	Line transient response, DCDC1, V_{IN} change from 6 V to 8.4 V, I_{OUT} = 4 A	Figure 2-41
	Line transient response, DCDC2, V_{IN} change from 6 V to 8.4 V, I_{OUT} = 4 A	Figure 2-42
	Line transient response, DCDC3, V_{OUT} = 1.35 V, V_{IN} change from 6 V to 8.4 V, I_{OUT} = 4 A	Figure 2-43
	Startup after enable, DCDC1, V_{IN} = 7.5 V, I_{OUT} = 4 A	Figure 2-44
	Startup after enable, DCDC2, V_{IN} = 7.5 V, I_{OUT} = 4 A	Figure 2-45
	Startup after enable, DCDC3, V_{OUT} = 1.35 V, V_{IN} = 7.5 V, I_{OUT} = 4 A	Figure 2-46
	Startup after enable, Charger, V_{IN} = 12 V, I_{OUT} = 4 A	Figure 2-47
	Softstart, Charger, V_{IN} = 12 V, I_{OUT} = 4 A	Figure 2-48
	Shutdown after disable, Charger, V_{IN} = 12 V, I_{OUT} = 4 A	Figure 2-49
	Continuous current mode operation, Charger, V_{IN} = 12 V	Figure 2-50
	Discontinuous current mode operation, Charger, V_{IN} = 12 V	Figure 2-51
	Adapter input power up and power down, Charger, V_{IN} = 12 V	Figure 2-52
	Supplement mode operation, Charger, V_{IN} = 12 V	Figure 2-53
	Input DPM operation, Charger, V_{IN} = 12 V	Figure 2-54
	Battery removal and insertion, Charger, V_{IN} = 12 V	Figure 2-55
	Battery short, Charger, V_{IN} = 12 V	Figure 2-56

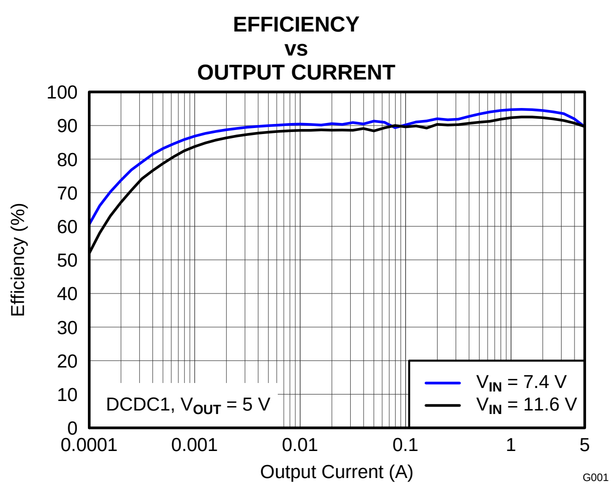


Figure 2-1.

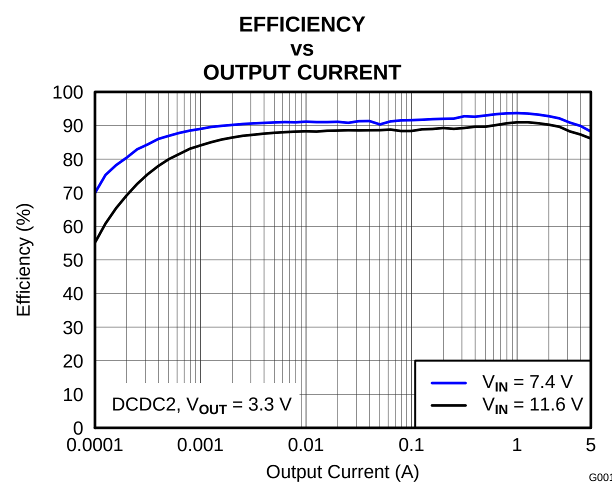


Figure 2-2.

**EFFICIENCY
vs
OUTPUT CURRENT**

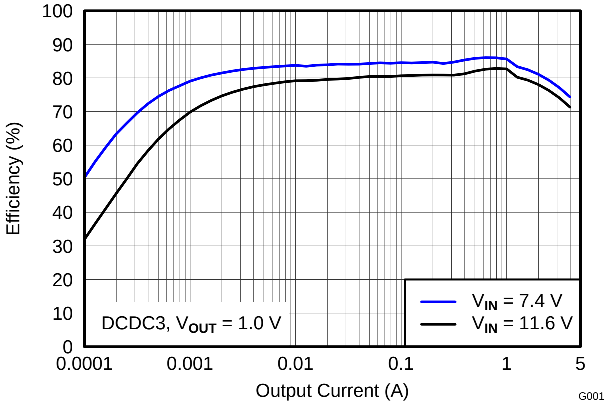


Figure 2-3.

**EFFICIENCY
vs
OUTPUT CURRENT**

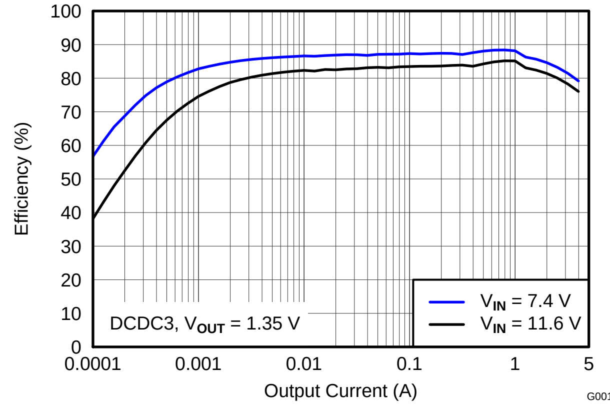


Figure 2-4.

**EFFICIENCY
vs
OUTPUT CURRENT**

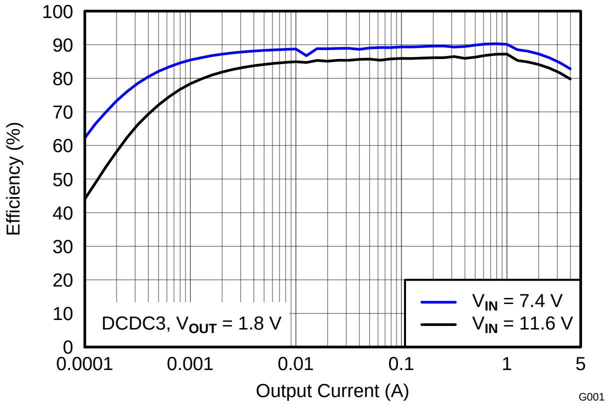


Figure 2-5.

**EFFICIENCY
vs
OUTPUT CURRENT**

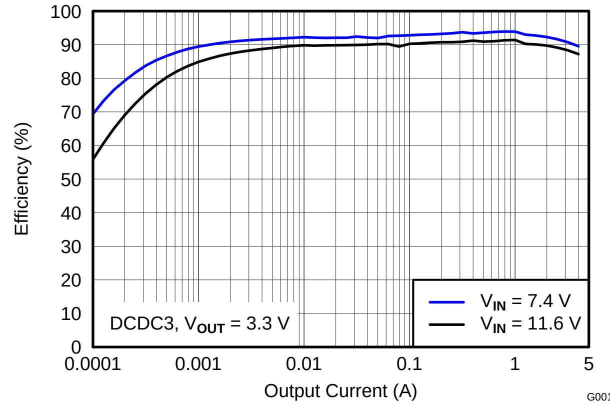


Figure 2-6.

**EFFICIENCY
vs
OUTPUT CURRENT**

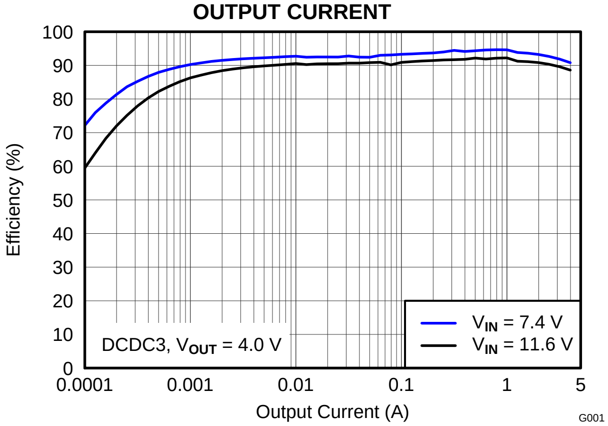


Figure 2-7.

**EFFICIENCY
vs
OUTPUT CURRENT**

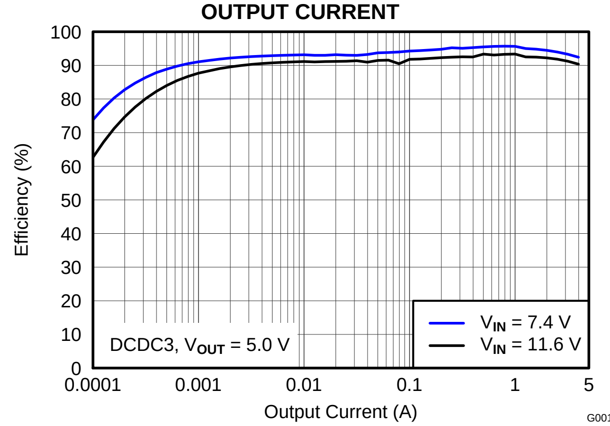


Figure 2-8.

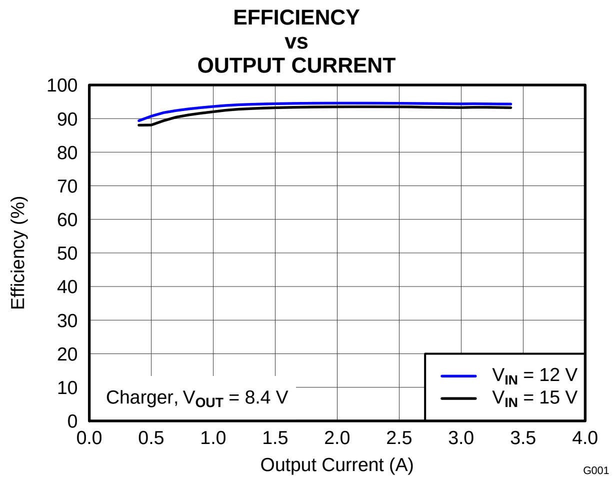


Figure 2-9.

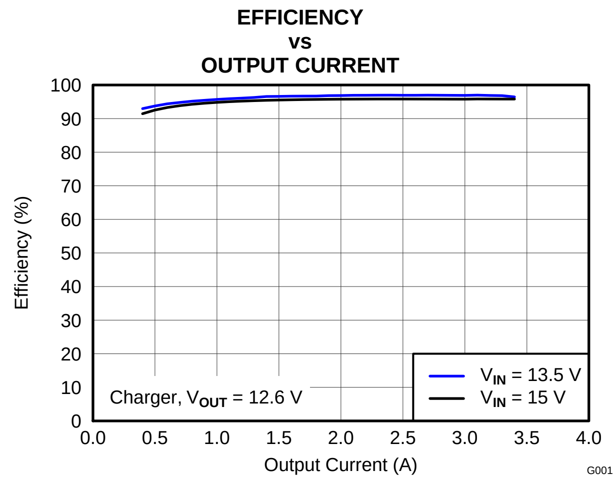


Figure 2-10.

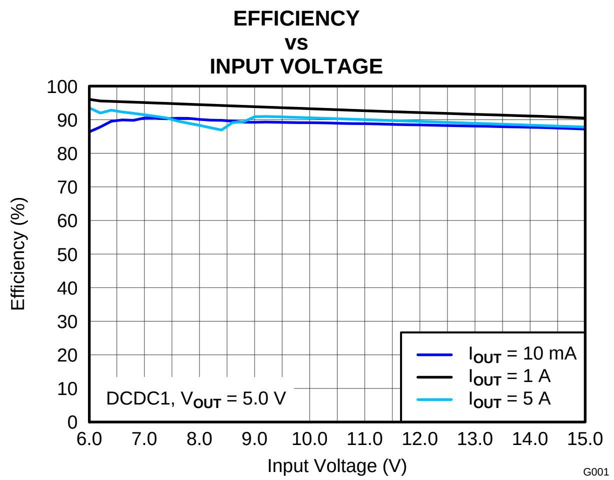


Figure 2-11.

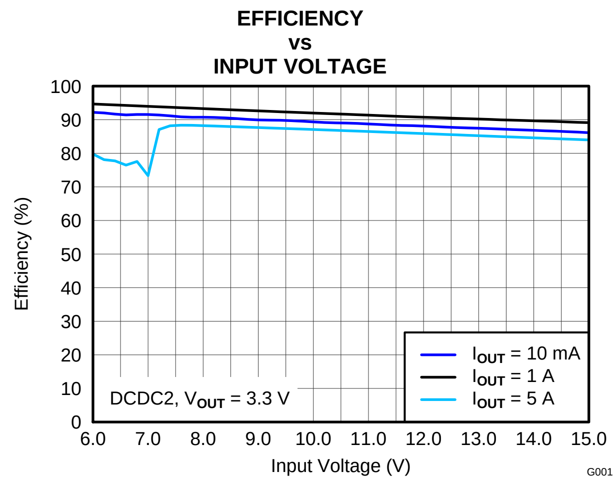


Figure 2-12.

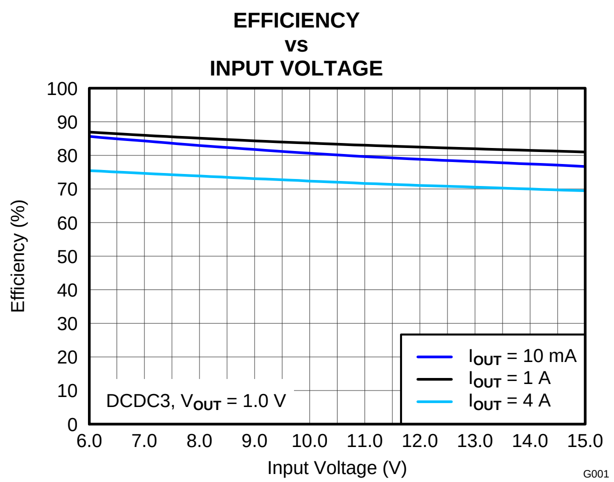


Figure 2-13.

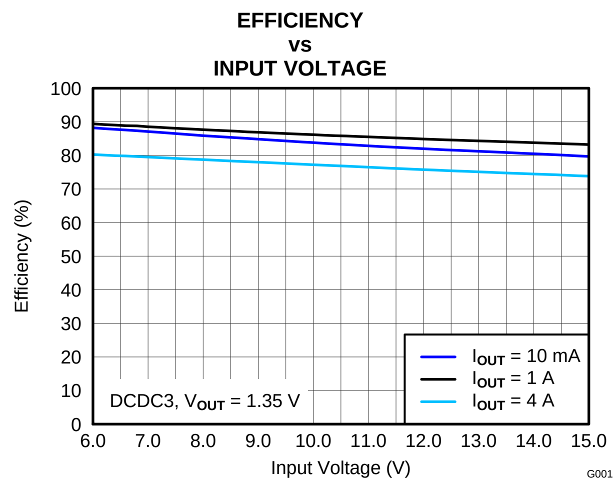


Figure 2-14.

EFFICIENCY vs INPUT VOLTAGE

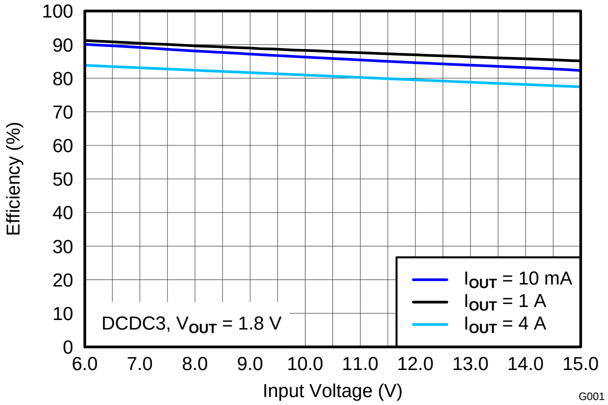


Figure 2-15.

EFFICIENCY vs INPUT VOLTAGE

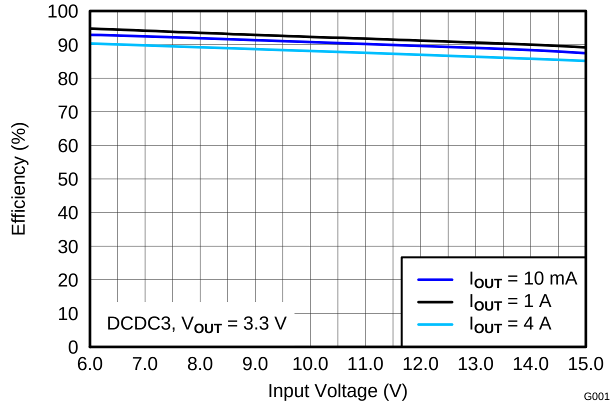


Figure 2-16.

EFFICIENCY vs INPUT VOLTAGE

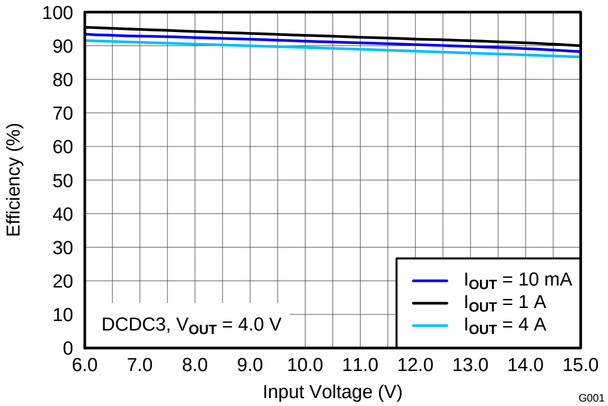


Figure 2-17.

EFFICIENCY vs INPUT VOLTAGE

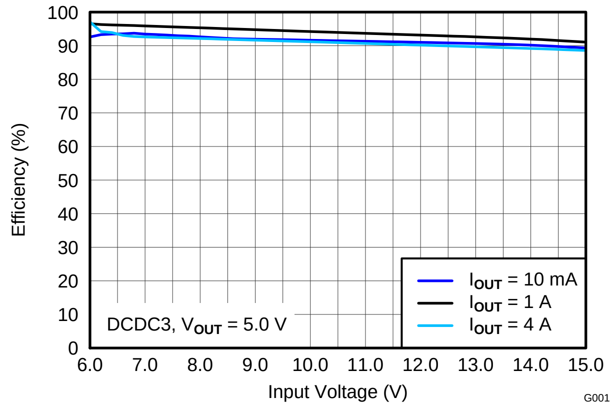


Figure 2-18.

EFFICIENCY vs BATTERY VOLTAGE

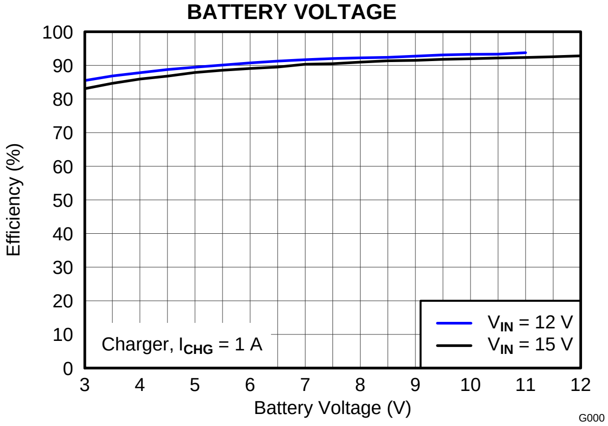


Figure 2-19.

EFFICIENCY vs BATTERY VOLTAGE

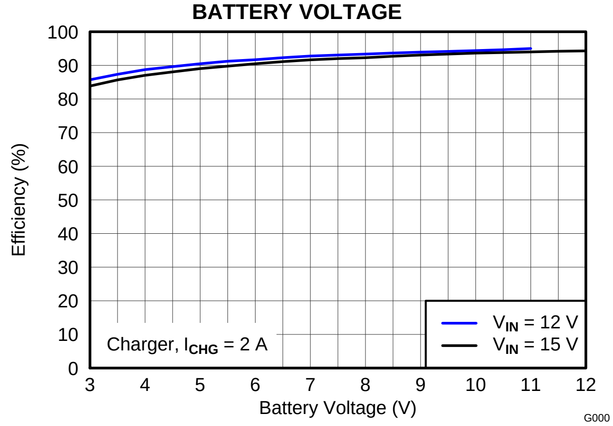


Figure 2-20.

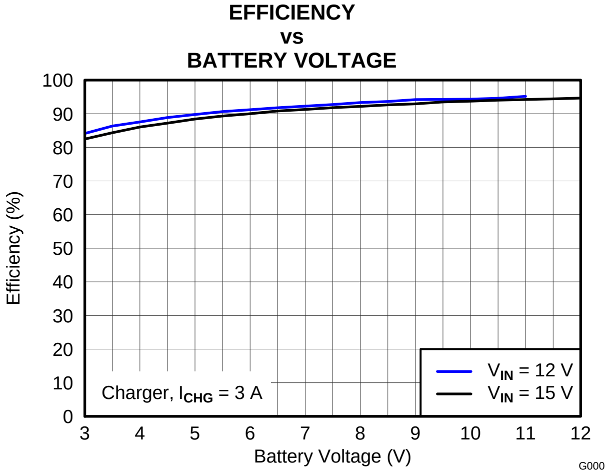


Figure 2-21.

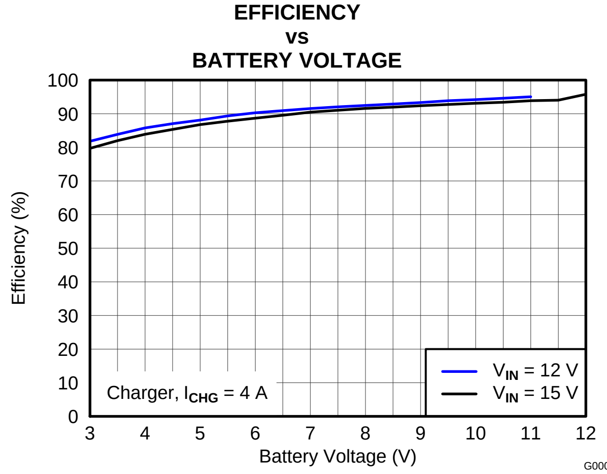


Figure 2-22.

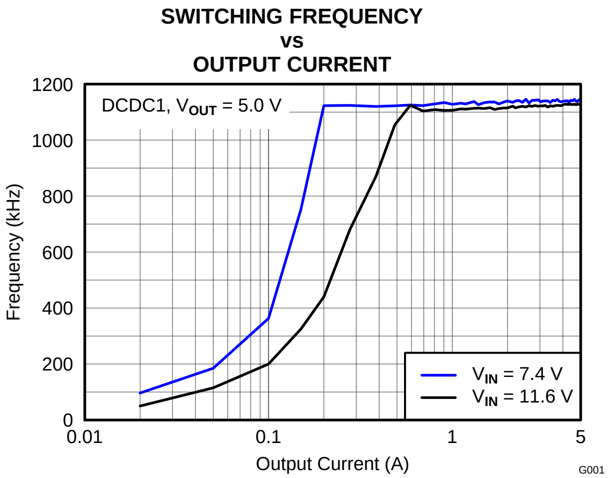


Figure 2-23.

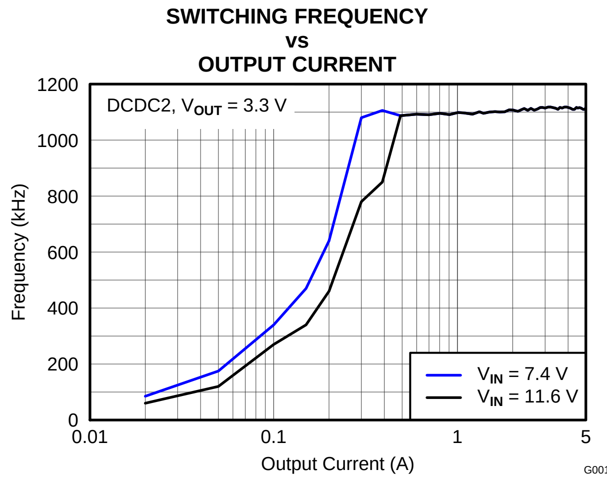


Figure 2-24.

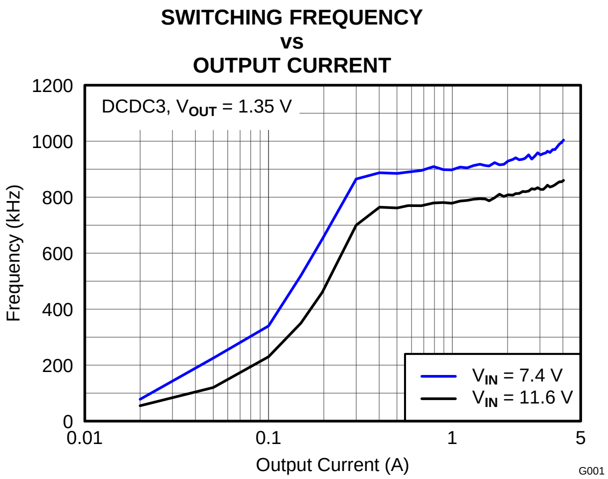


Figure 2-25.

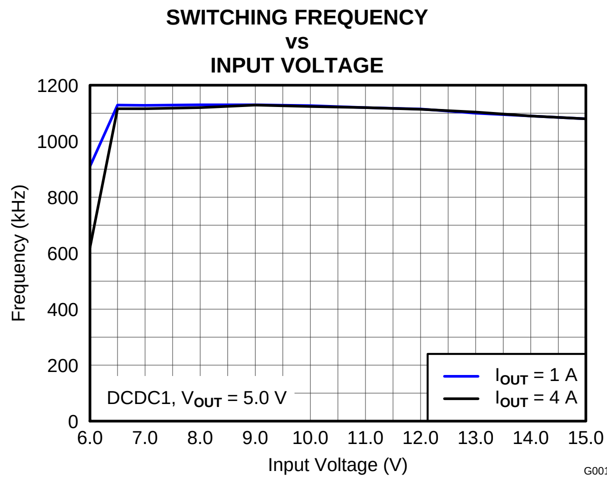


Figure 2-26.

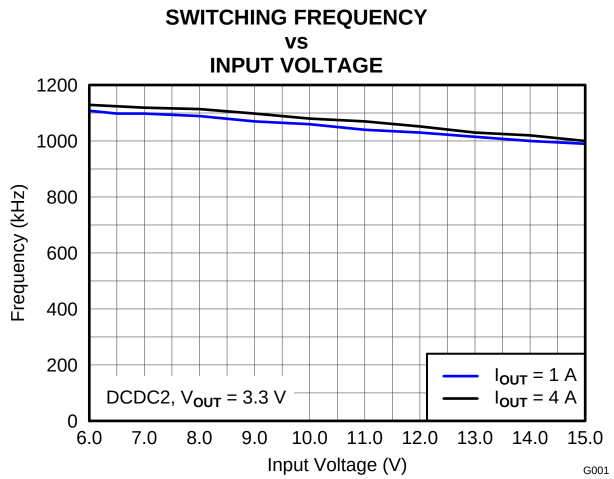


Figure 2-27.

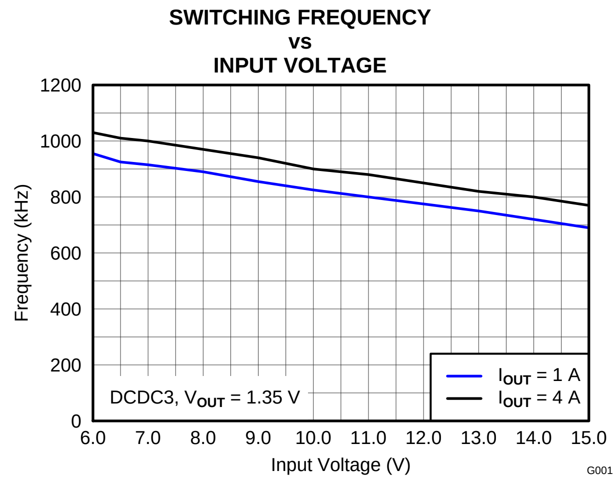


Figure 2-28.

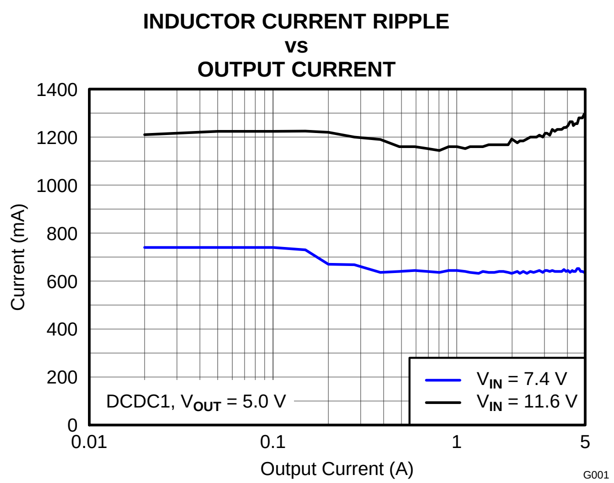


Figure 2-29.

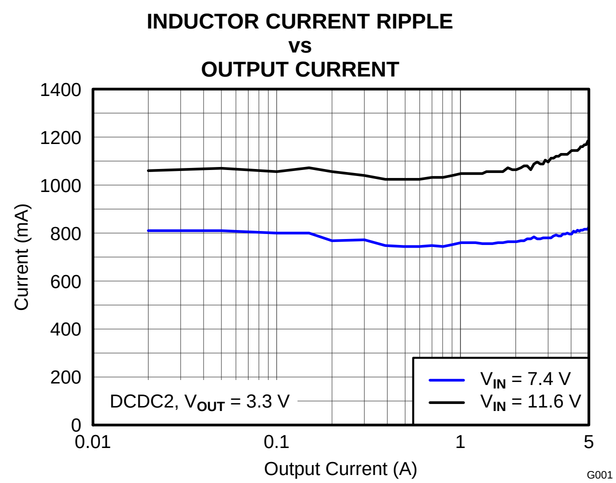


Figure 2-30.

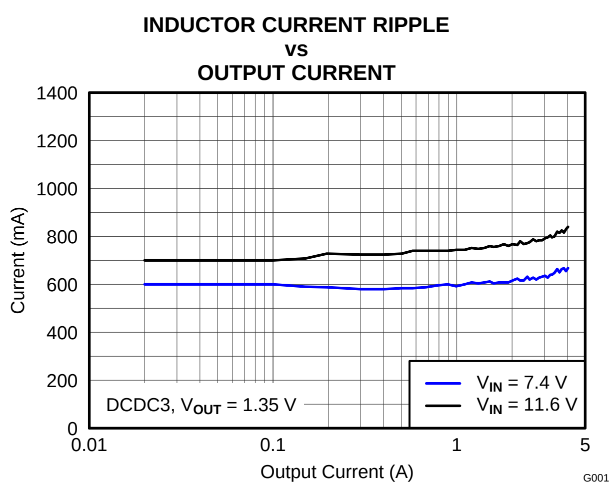


Figure 2-31.

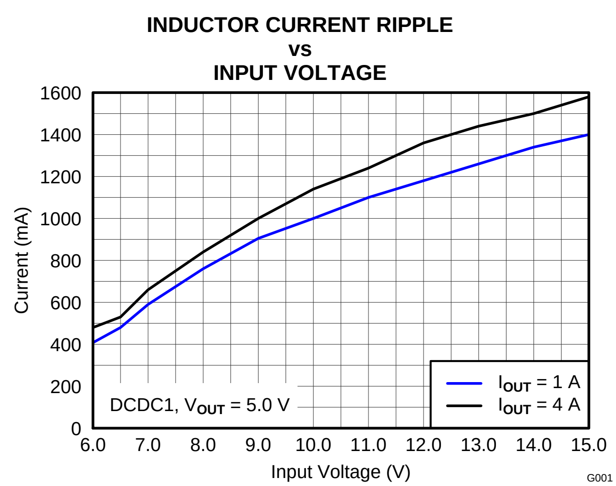


Figure 2-32.

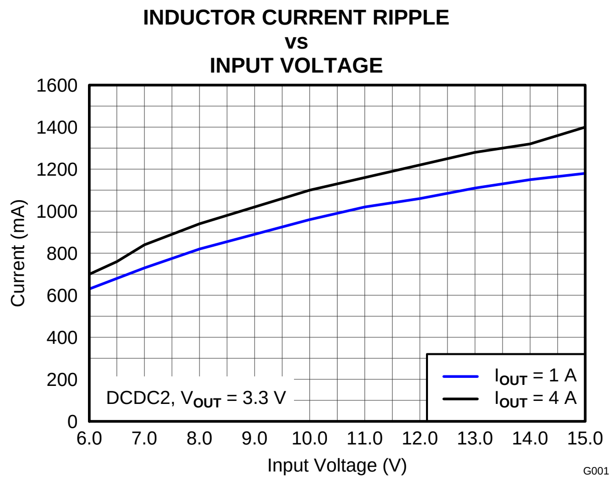


Figure 2-33.

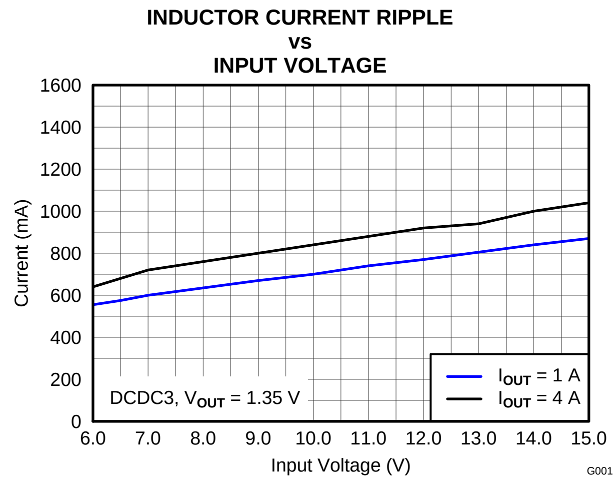


Figure 2-34.

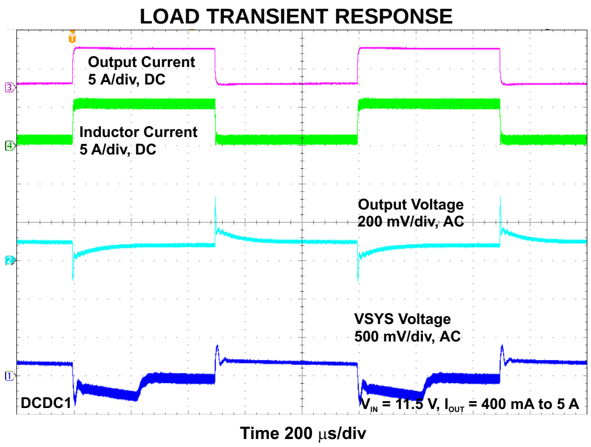


Figure 2-35.

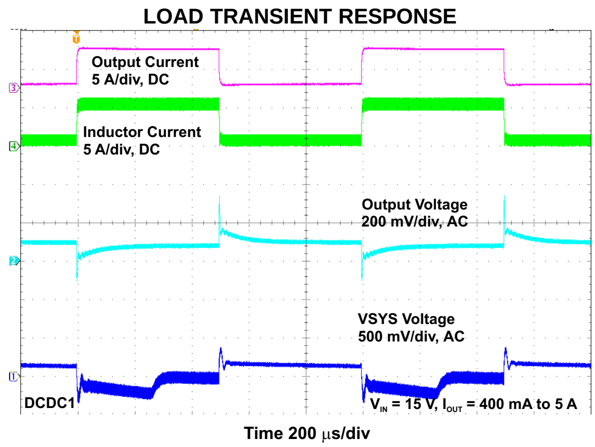


Figure 2-36.

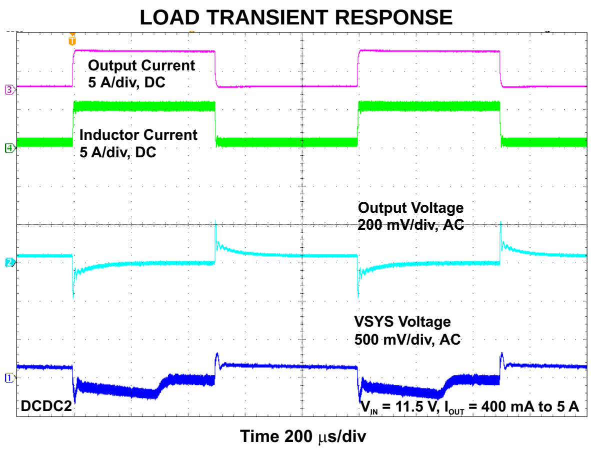


Figure 2-37.

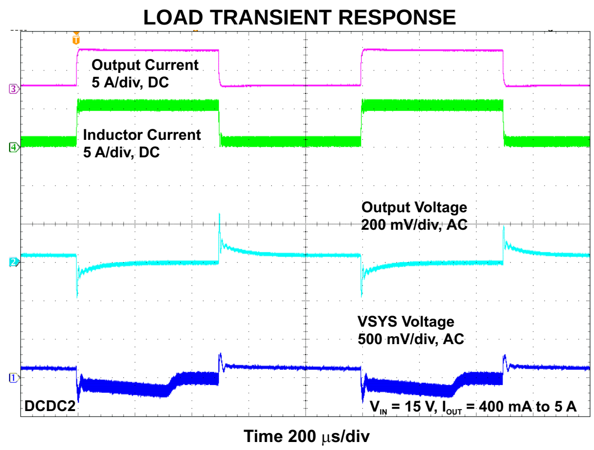


Figure 2-38.

LOAD TRANSIENT RESPONSE

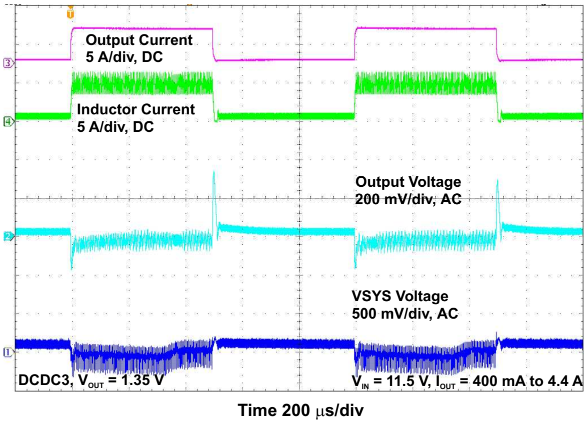


Figure 2-39.

LOAD TRANSIENT RESPONSE

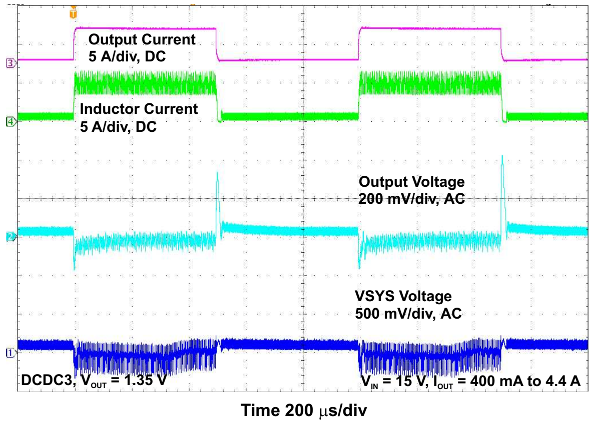


Figure 2-40.

LINE TRANSIENT RESPONSE

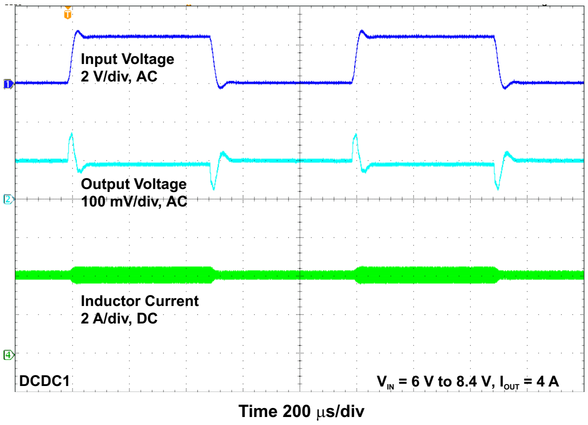


Figure 2-41.

LINE TRANSIENT RESPONSE

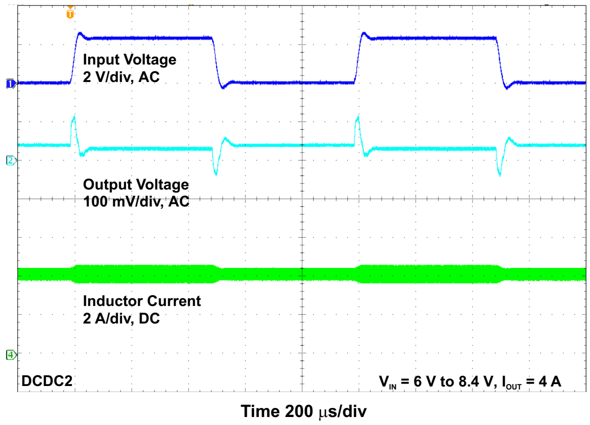


Figure 2-42.

LINE TRANSIENT RESPONSE

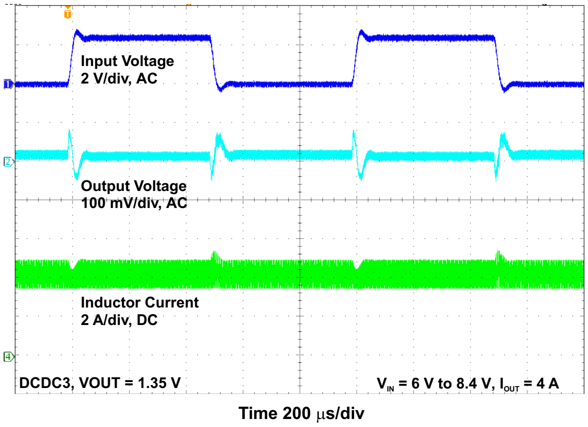


Figure 2-43.

STARTUP AFTER ENABLE

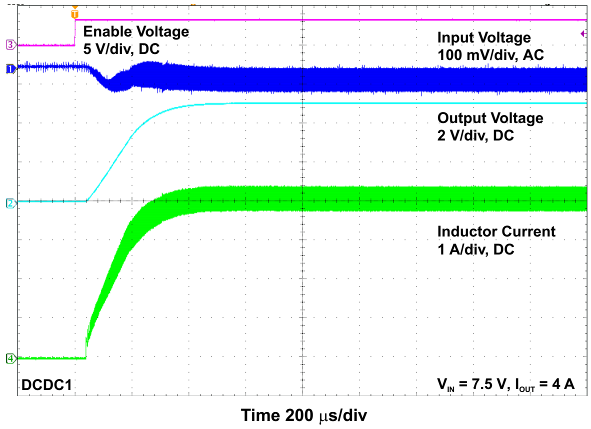


Figure 2-44.

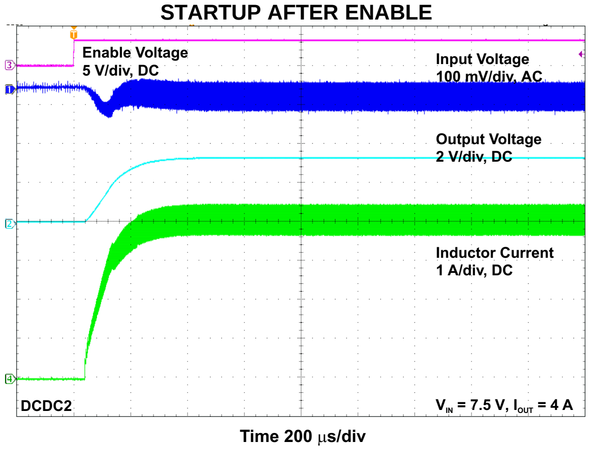


Figure 2-45.

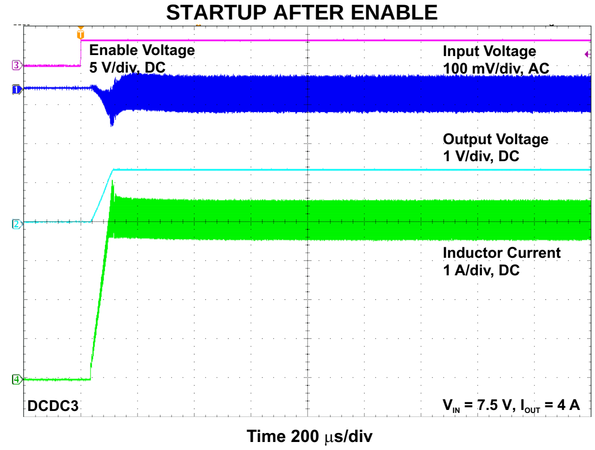


Figure 2-46.

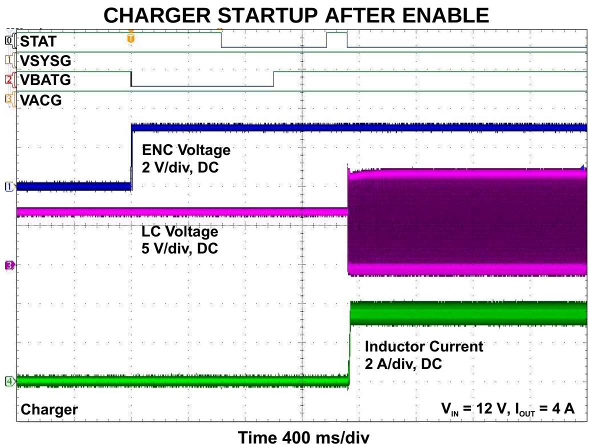


Figure 2-47.

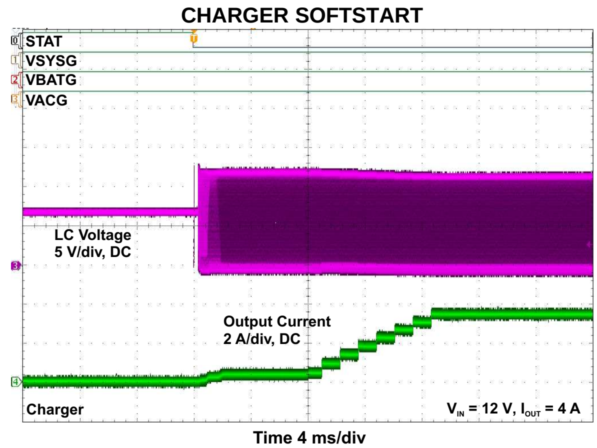


Figure 2-48.

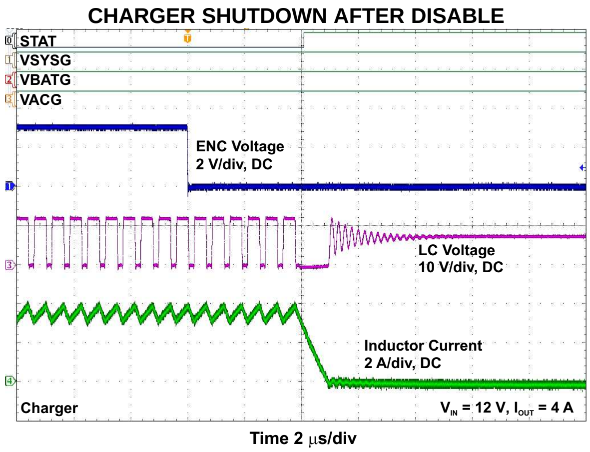


Figure 2-49.

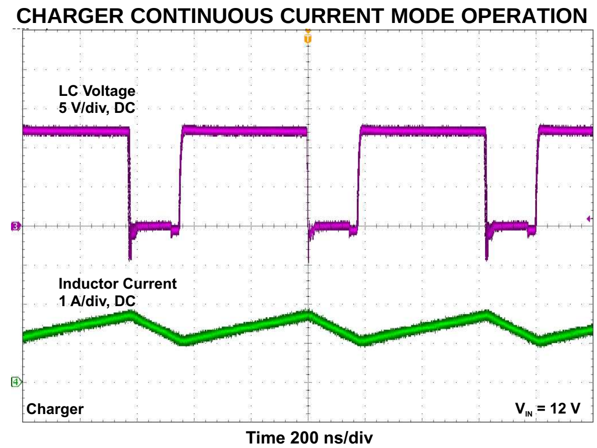
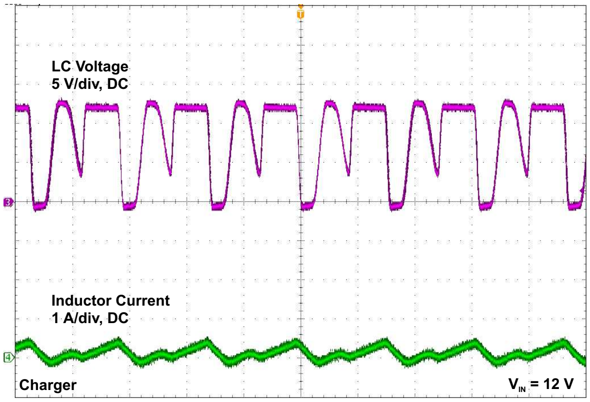


Figure 2-50.

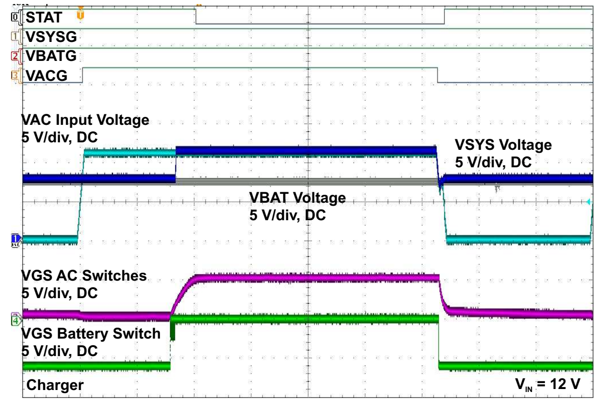
CHARGER DISCONTINUOUS CURRENT MODE OPERATION



Time 200 ns/div

Figure 2-51.

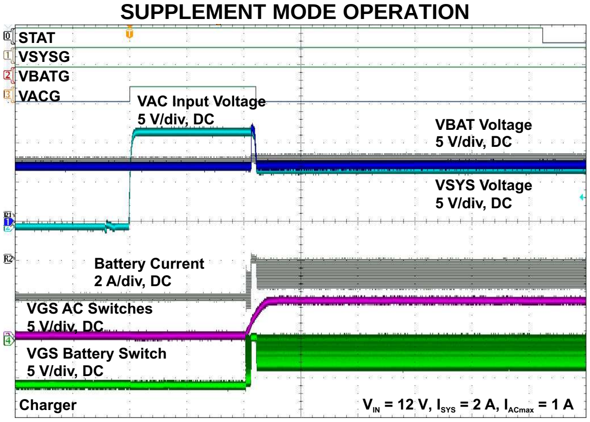
ADAPTER INPUT POWER UP AND POWER DOWN



Time 20 ms/div

Figure 2-52.

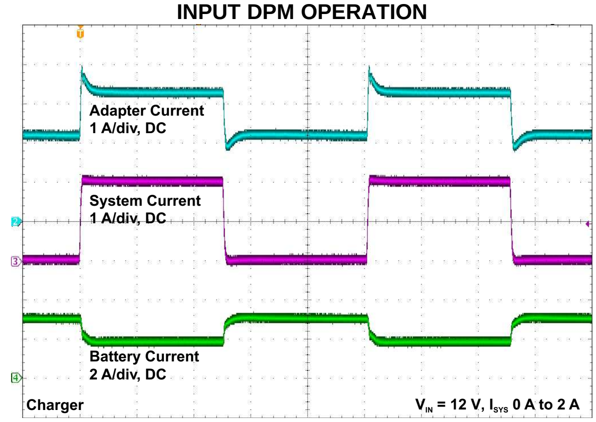
SUPPLEMENT MODE OPERATION



Time 20 ms/div

Figure 2-53.

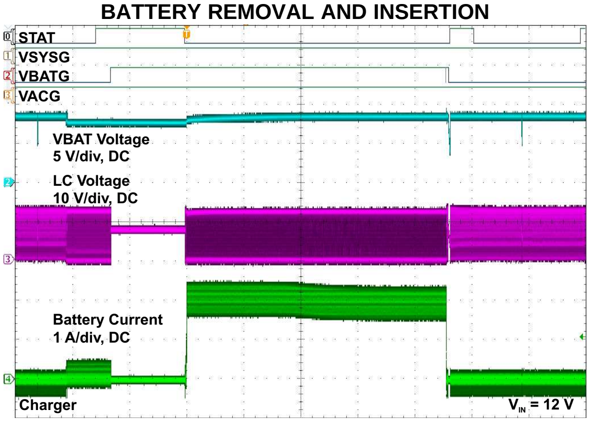
INPUT DPM OPERATION



Time 400 µs/div

Figure 2-54.

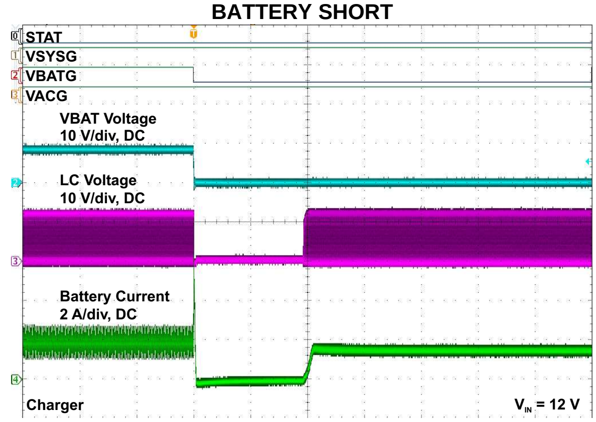
BATTERY REMOVAL AND INSERTION



Time 400 ms/div

Figure 2-55.

BATTERY SHORT

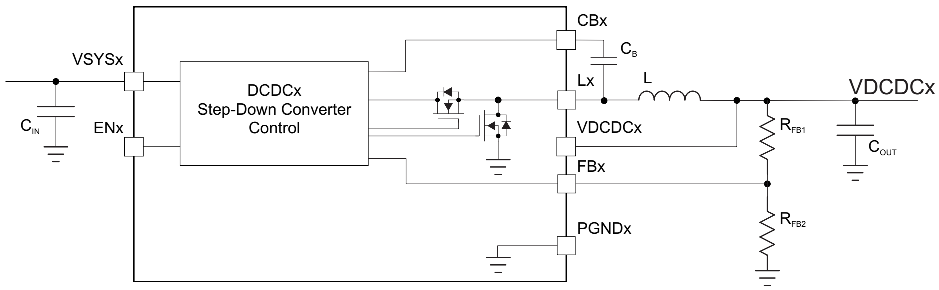


Time 400 µs/div

Figure 2-56.

2.13 PARAMETER MEASUREMENT INFORMATION - DCDC CONVERTERS

2.13.1 Circuit Drawing



2.13.2 Lists of Components

Table 2-3. List of Components - DCDC1

REFERENCE	DESCRIPTION	MANUFACTURER
L	2.2 µH, 5 mm x 5mm x 3 mm	XAL5030-222, Coilcraft
C_{IN}	10 µF, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata
	1 µF, 25 V, 0402, X7R ceramic	GRM155R61E105MA12, Murata
C_{OUT}	4 × 10 µF, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata
	2.2 µF 10 V, 0603, X7R ceramic	GRM155R61A225KE95, Murata
C_{B1}	4700 pF, X7R ceramic	
R_{FB1}	not used, FB1 is directly connected to VDCDC1	
R_{FB2}	not used	

Table 2-4. List of Components - DCDC2

REFERENCE	DESCRIPTION	MANUFACTURER
L	2.2 µH, 5 mm x 5mm x 3 mm	XAL5030-222, Coilcraft
C_{IN}	10 µF, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata
	1 µF, 25 V, 0402, X7R ceramic	GRM155R61E105MA12, Murata
C_{OUT}	4 × 10 µF, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata
	2.2 µF 10 V, 0603, X7R ceramic	GRM155R61A225KE95, Murata
C_{B2}	4700 pF, X7R ceramic	
R_{FB1}	not used, FB2 is directly connected to VDCDC2	
R_{FB2}	not used	

Table 2-5. List of Components - DCDC3

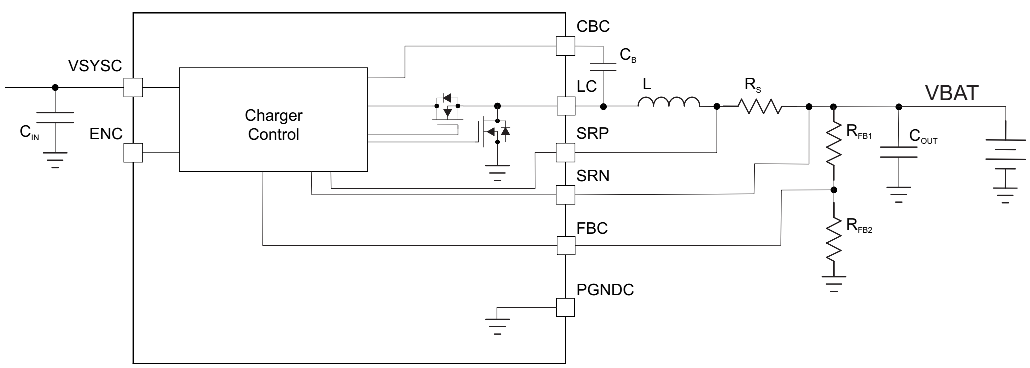
REFERENCE	DESCRIPTION	MANUFACTURER	COMMENTS
L	2.2 µH, 5 mm x 5mm x 3 mm	XAL5030-222, Coilcraft	
C_{IN}	10 µF, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata	
	1 µF, 25 V, 0402, X7R ceramic	GRM155R61E105MA12, Murata	

Table 2-5. List of Components - DCDC3 (continued)

REFERENCE	DESCRIPTION	MANUFACTURER	COMMENTS
C_{OUT}	4 × 10 µF, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata	
	2.2 µF 10 V, 0603, X7R ceramic	GRM155R61A225KE95, Murata	
C_{B1}	4700 pF, X7R ceramic	any	
R_{FB1}	162 kΩ, 1%, 0402	any	V_{DCDC3} = 1.0 V
	330 kΩ, 1%, 0402	any	V_{DCDC3} = 1.35 V
	453 kΩ, 1%, 0402	any	V_{DCDC3} = 1.8 V
	590 kΩ, 1%, 0402	any	V_{DCDC3} = 3.3 V
	649 kΩ, 1%, 0402	any	V_{DCDC3} = 4.0 V
	787 kΩ, 1%, 0402	any	V_{DCDC3} = 5.0 V
R_{FB2}	649 kΩ, 1%, 0402	any	V_{DCDC3} = 1.0 V
	470 kΩ, 1%, 0402	any	V_{DCDC3} = 1.35 V
	365 kΩ, 1%, 0402	any	V_{DCDC3} = 1.8 V
	187 kΩ, 1%, 0402	any	V_{DCDC3} = 3.3 V
	162 kΩ, 1%, 0402	any	V_{DCDC3} = 4.0 V
	150 kΩ, 1%, 0402	any	V_{DCDC3} = 5.0 V

2.14 PARAMETER MEASUREMENT INFORMATION - CHARGER

2.14.1 Circuit Drawing



2.14.2 Lists of Components

Table 2-6. List of Components - Charger

REFERENCE	DESCRIPTION	MANUFACTURER	COMMENTS
L	2.2 µH, 5 mm x 5mm x 3 mm	XAL5030-222, Coilcraft	
C_{IN}	2 x 10 µF, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata	
	1 µF, 25 V, 0402, X7R ceramic	GRM155R61E105MA12, Murata	
C_{OUT}	2 × 10 µF, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata	
	1 µF, 25 V, 0402, X7R ceramic	GRM155R61E105MA12, Murata	
C_{BC}	4700 pF, X7R ceramic	any	
R_S	10 mΩ, 0.1%, 1206	any	maximum charge current 4 A

Table 2-6. List of Components - Charger (continued)

REFERENCE	DESCRIPTION	MANUFACTURER	COMMENTS
R_{FB1}	330 kΩ, 1%, 0402	any	charge termination voltage V_{BAT} = 8.4 V
	1100 kΩ, 1%, 0402	any	charge termination voltage V_{BAT} = 12.6 V
R_{FB2}	110 kΩ, 1%, 0402	any	charge termination voltage V_{BAT} = 8.4 V
	220 kΩ, 1%, 0402	any	charge termination voltage V_{BAT} = 12.6 V

3 DETAILED DESCRIPTION

3.1 I²C INTERFACE

I²C is a 2-wire serial interface developed by NXP (formerly Philips Semiconductor) (see I²C-Bus Specification and user manual, Rev 4, 13 February 2012). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

TPS6509x works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (up to 3.4 Mbps in write mode). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents are loaded when voltage is applied to TPS6509x higher than the undervoltage lockout threshold. The I²C interface is running from an internal oscillator that is automatically enabled when there is an access to the interface.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as H/S-mode.

The TPS6509x supports 7-bit addressing; 10-bit addressing and general call address are not supported. The default device address is set to *1001000*.The 2 LSB bits of the address are factory programmable. Please contact TI about availability of different default device addresses.

All registers are set to their default value when the supply voltage is below the UVLO threshold.

3.1.1 F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, see Figure 3-1. All I²C-compatible devices should recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, see Figure 3-2. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge*, see Figure 3-3, by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit = 0) or receive data from the slave (R/W bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, see Figure 3-1. This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address

Attempting to read data from register addresses not listed in this section results in FFh being read out.

3.1.2 H/S-Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions are used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section results in FFh being read out.

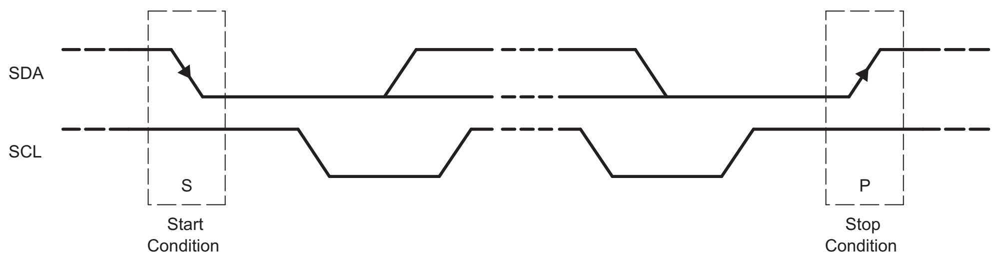


Figure 3-1. START and STOP Conditions

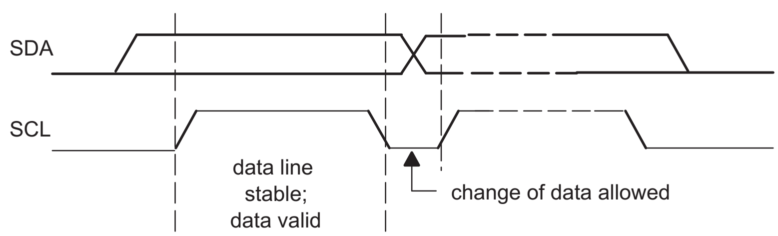


Figure 3-2. Bit Transfer on the I²C-bus

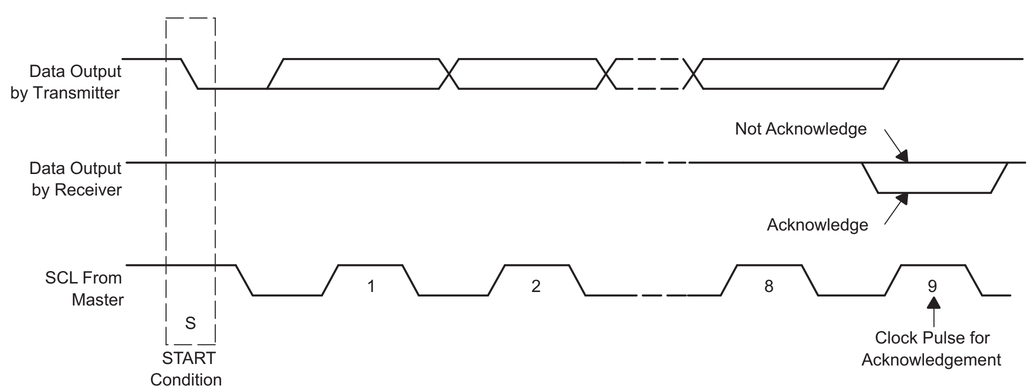


Figure 3-3. Acknowledge on the I²C-bus

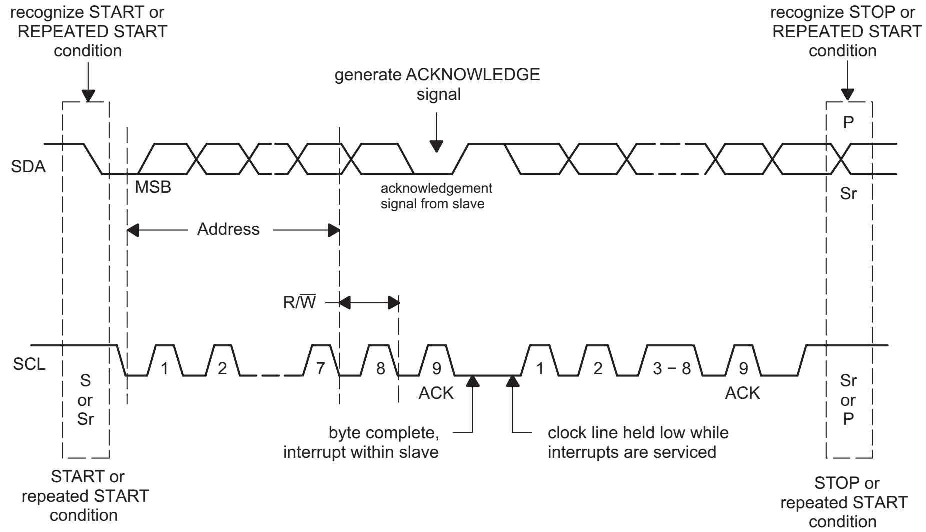


Figure 3-4. Bus Protocol

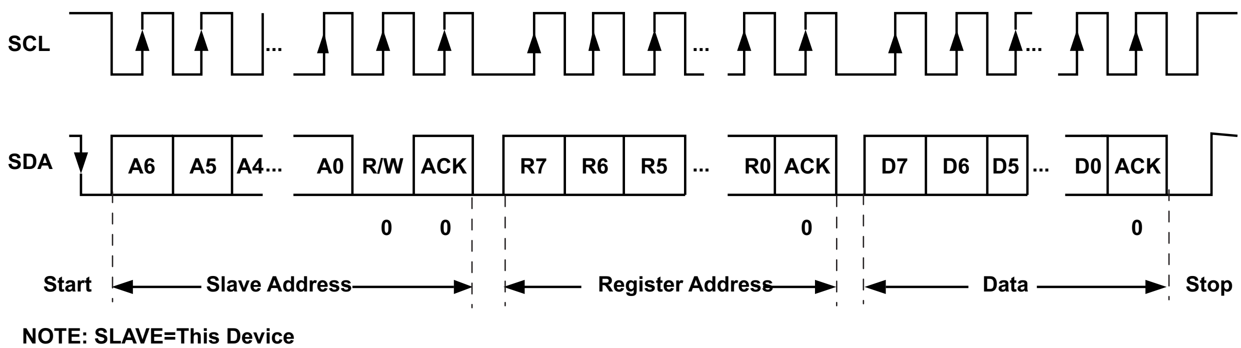


Figure 3-5. I2C Interface WRITE to TPS65090 in F/S Mode

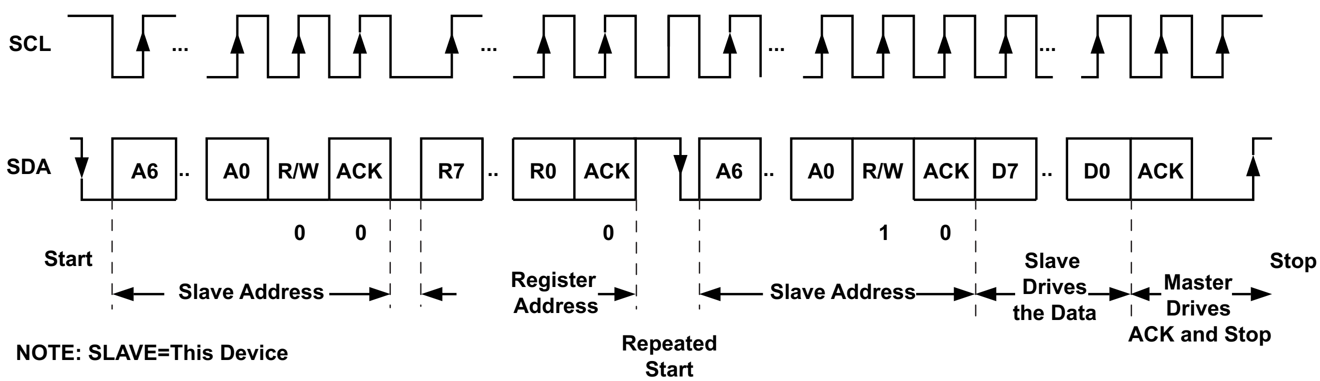


Figure 3-6. I2C Interface READ from TPS65090 in F/S Mode

3.2 REGISTER DEFINITION

IRQ1 Register Address: 0x00							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
OLDCDC2	OLDCDC1	CGCPL	CGACT	VBATG	VSYSG	VACG	IRQ
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	**r**	**r**	**r**	**r**	**r**	**r**	**r/w**
OLDCDC2	Overload on DCDC2, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload						
OLDCDC1	Overload on DCDC1, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload						
CGCPL	Charging completed, IRQ on change to 1, cleared on interrupt clear 0: charging not completed 1: charging completed						
CGACT	Charging status, interrupt on change 0: charging suspended 1: charging active						
VBATG	VBAT status, interrupt on change 0: VBAT not available 1: VBAT available and useable						
VSYSG	VSYS status, interrupt on change 0: VSYS not available 1: VSYS available and useable						
VACG	VAC status, interrupt on change 0: VAC not available 1: VAC available and useable						
IRQ	Interrupt 0: interrupt cleared 1: interrupt asserted						

IRQ2 Register Address: 0x01							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
OLFET7	OLFET6	OLFET5	OLFET4	OLFET3	OLFET2	OLFET1	OLDCDC3
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	**r**	**r**	**r**	**r**	**r**	**r**	**r**
OLFET7	Overload on FET7, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload						
OLFET6	Overload on FET6, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload						
OLFET5	Overload on FET5, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload						
OLFET4	Overload on FET4, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload						
OLFET3	Overload on FET3, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload						
OLFET2	Overload on FET2, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload						
OLFET1	Overload on FET1, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload						
OLDCDC3	Overload on DCDC3, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload						

IRQ1MASK Register Address: 0x02							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
OLDCDC2MASK	OLDCDC1MASK	CGCPLMASK	CGACTMASK	VBATGMASK	VSYSGMASK	VACGMASK	reserved
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r/w	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r**

OLDCDC2MASK	Enable overload on DCDC2 interrupt 0: disabled 1: enabled
OLDCDC1MASK	Enable overload on DCDC1 interrupt 0: disabled 1: enabled
CGCPLMASK	Enable charging completed status interrupt 0: disabled 1: enabled
CGACTMASK	Enable charging status interrupt 0: disabled 1: enabled
VBATGMASK	Enable VBAT status interrupt 0: disabled 1: enabled
VSYSGMASK	Enable VSYS status interrupt 0: disabled 1: enabled
VACGMASK	Enable VAC status interrupt 0: disabled 1: enabled
reserved	

IRQ2MASK Register Address: 0x03							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
OLFET7MASK	OLFET6MASK	OLFET5MASK	OLFET4MASK	OLFET3MASK	OLFET2MASK	OLFET1MASK	OLDCDC3MASK
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r/w	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**

OLFET7MASK	Enable overload on FET7 interrupt 0: disabled 1: enabled
OLFET6MASK	Enable overload on FET6 interrupt 0: disabled 1: enabled
OLFET5MASK	Enable overload on FET5 interrupt 0: disabled 1: enabled
OLFET4MASK	Enable overload on FET4 interrupt 0: disabled 1: enabled
OLFET3MASK	Enable overload on FET3 interrupt 0: disabled 1: enabled
OLFET2MASK	Enable overload on FET2 interrupt 0: disabled 1: enabled
OLFET1MASK	Enable overload on FET1 interrupt 0: disabled 1: enabled
OLDCDC3MASK	Enable overload on DCDC3 interrupt 0: disabled 1: enabled

CG_CTRL0 Register Address: 0x04							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
reserved	IBATSET	IACSET	FASTTIME[2]	FASTTIME[1]	FASTTIME[0]	ENCMASK	ENC
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**
r	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**
reserved							
IBATSET	Maximum battery discharge current 0: 100% of programmed current 1: 90% of programmed current						
IACSET	Maximum adapter current 0: 100% of programmed current 1: 90% of programmed current						
FASTTIME[2:0]	Fastcharge safety timer 000: 2 hrs 001: 3 hrs 010: 4 hrs 011: 5 hrs 100: 6 hrs 101: 7 hrs 110: 8 hrs 111: 10 hrs						
ENCMASK	Enable external charge enable pin 0: external control off 1: external control on						
ENC	Enable charger 0: disabled 1: enabled						

CG_CTRL1 Register Address: 0x05							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
T1_SET[2]	T1_SET[1]	T1_SET[0]	T01_VSET[1]	T01_VSET[0]	T01_ISET[2]	T01_ISET[1]	T01_ISET[0]
0	**0**	**1**	**0**	**0**	**0**	**0**	**0**
r/w	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**
T1_SET[2:0]	Temperature threshold for T1 000: -10 °C (for a default NTC resistor network) 001: 0 °C (for a default NTC resistor network) 010: 10 °C (for a default NTC resistor network) 011: 15 °C (for a default NTC resistor network) 100: 40 °C (for a default NTC resistor network) 101: 45 °C (for a default NTC resistor network) 110: 50 °C (for a default NTC resistor network) 111: 60 °C (for a default NTC resistor network)						
T01_VSET[1:0]	Charge termination feedback voltage for T01 temperature range 00: 2.0 V 01: 2.05 V 10: 2.075 V 11: 2.1 V						
T01_ISET[2:0]	Maximum fast charge current for T01 temperature range 000: 0% of resistor programmed current 001: 25% of resistor programmed current 010: 37.5% of resistor programmed current 011: 50% of resistor programmed current 100: 62.5% of resistor programmed current 101: 75% of resistor programmed current 110: 87.5% of resistor programmed current 111: 100% of resistor programmed current						

CG_CTRL2 Register Address: 0x06							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
T2_SET[2]	T2_SET[1]	T2_SET[0]	T12_VSET[1]	T12_VSET[0]	T12_ISET[2]	T12_ISET[1]	T12_ISET[0]
0	**1**	**0**	**0**	**1**	**0**	**1**	**1**
r/w	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**

T2_SET[2:0]	Temperature threshold for T2 000: -10 °C (for a default NTC resistor network) 001: 0 °C (for a default NTC resistor network) 010: 10 °C (for a default NTC resistor network) 011: 15 °C (for a default NTC resistor network) 100: 40 °C (for a default NTC resistor network) 101: 45 °C (for a default NTC resistor network) 110: 50 °C (for a default NTC resistor network) 111: 60 °C (for a default NTC resistor network)
T12_VSET[1:0]	Charge termination feedback voltage for T12 temperature range 00: 2.0 V 01: 2.05 V 10: 2.075 V 11: 2.1 V
T12_ISET[2:0]	Maximum fast charge current for T12 temperature range 000: 0% of resistor programmed current 001: 25% of resistor programmed current 010: 37.5% of resistor programmed current 011: 50% of resistor programmed current 100: 62.5% of resistor programmed current 101: 75% of resistor programmed current 110: 87.5% of resistor programmed current 111: 100% of resistor programmed current

CG_CTRL3 Register Address: 0x07							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
T3_SET[2]	T3_SET[1]	T3_SET[0]	T23_VSET[1]	T23_VSET[0]	T23_ISET[2]	T23_ISET[1]	T23_ISET[0]
1	**0**	**1**	**1**	**1**	**1**	**1**	**1**
r/w	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**

T3_SET[2:0]	Temperature threshold for T3 000: -10 °C (for a default NTC resistor network) 001: 0 °C (for a default NTC resistor network) 010: 10 °C (for a default NTC resistor network) 011: 15 °C (for a default NTC resistor network) 100: 40 °C (for a default NTC resistor network) 101: 45 °C (for a default NTC resistor network) 110: 50 °C (for a default NTC resistor network) 111: 60 °C (for a default NTC resistor network)
T23_VSET[1:0]	Charge termination feedback voltage for T23 temperature range 00: 2.0 V 01: 2.05 V 10: 2.075 V 11: 2.1 V
T23_ISET[2:0]	Maximum fast charge current for T23 temperature range 000: 0% of resistor programmed current 001: 25% of resistor programmed current 010: 37.5% of resistor programmed current 011: 50% of resistor programmed current 100: 62.5% of resistor programmed current 101: 75% of resistor programmed current 110: 87.5% of resistor programmed current 111: 100% of resistor programmed current

CG_CTRL4 Register Address: 0x08							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
T4_SET[2]	T4_SET[1]	T4_SET[0]	T34_VSET[1]	T34_VSET[0]	T34_ISET[2]	T34_ISET[1]	T34_ISET[0]
1	**1**	**1**	**1**	**0**	**0**	**1**	**1**
r/w	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**
T4_SET[2:0]	Temperature threshold for T4 000: -10 °C (for a default NTC resistor network) 001: 0 °C (for a default NTC resistor network) 010: 10 °C (for a default NTC resistor network) 011: 15 °C (for a default NTC resistor network) 100: 40 °C (for a default NTC resistor network) 101: 45 °C (for a default NTC resistor network) 110: 50 °C (for a default NTC resistor network) 111: 60 °C (for a default NTC resistor network)						
T34_VSET[1:0]	Charge termination feedback voltage for T34 temperature range 00: 2.0 V 01: 2.05 V 10: 2.075 V 11: 2.1 V						
T34_ISET[2:0]	Maximum fast charge current for T34 temperature range 000: 0% of resistor programmed current 001: 25% of resistor programmed current 010: 37.5% of resistor programmed current 011: 50% of resistor programmed current 100: 62.5% of resistor programmed current 101: 75% of resistor programmed current 110: 87.5% of resistor programmed current 111: 100% of resistor programmed current						

CG_CTRL5 Register Address: 0x09							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
reserved	ENRECG	NOITERM	T40_VSET[1]	T40_VSET[0]	T40_ISET[2]	T40_ISET[1]	T40_ISET[0]
1	**1**	**0**	**0**	**0**	**0**	**0**	**0**
r	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**
reserved							
ENRECG	Enable of automatic recharge based on battery voltage detected 0: disabled 1: enabled						
NOITERM	Disable charging termination based on low charge current detected 0: charging stops when low charge current is detected 1: charging continues when low charge current is detected						
T40_VSET[1:0]	Charge termination feedback voltage for T40 temperature range 00: 2.0 V 01: 2.05 V 10: 2.075 V 11: 2.1 V						
T40_ISET[2:0]	Maximum fast charge current for T40 temperature range 000: 0% of resistor programmed current 001: 25% of resistor programmed current 010: 37.5% of resistor programmed current 011: 50% of resistor programmed current 100: 62.5% of resistor programmed current 101: 75% of resistor programmed current 110: 87.5% of resistor programmed current 111: 100% of resistor programmed current						

CG_STATUS1 Register Address: 0x0A							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
STATECG[3]	STATECG[2]	STATECG[1]	STATECG[0]	TOC[1]	TOC[0]	OCC	OTC
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	**r**	**r**	**r**	**r**	**r**	**r**	**r**

STATECG[3:0]	Charger status indication: 0000: not used 0001: not used 0010: charger idle 0011: battery detection 0100: battery detection 0101: charging in precharge 0110: charging in fastcharge 0111: not used 1000: not used 1001: not used 1010: charging completed 1011: not used 1100: not used 1101: battery detection, wait for start charging 1110: not used 1111: not used
TOC[1:0]	Charger timeout indication 00: no timeout 01: precharge timeout 10: fastcharge timeout 11: no timeout
OCC	Overcurrent charger 0: no overcurrent detected 1: overcurrent detected
OTC	Overtemperature charger 0: no overtermperature detected 1: overtemperature detected

CG_STATUS2 Register Address: 0x0B							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
reserved	reserved	TS2_ZONE[2]	TS2_ZONE[1]	TS2_ZONE[0]	TS1_ZONE[2]	TS1_ZONE[1]	TS1_ZONE[0]
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	**r**	**r**	**r**	**r**	**r**	**r**	**r**

reserved[1:0]	
TS2_ZONE[2:0]	Temperature zone reading for TS2 000: temperature zone 01 001: temperature zone 12 010: temperature zone 23 011: temperature zone 34 100: temperature zone 40 101: not used 110: not used 111: not used
TS1_ZONE[2:0]	Temperature zone reading for TS1 000: temperature zone 01 001: temperature zone 12 010: temperature zone 23 011: temperature zone 34 100: temperature zone 40 101: not used 110: not used 111: not used

DCDC1_CTRL Register Address: 0x0C							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
reserved	OC	OT	PG	ADENDCDC	reserved	ENMASK	EN
1	**0**	**0**	**0**	**1**	**1**	**1**	**0**
r	**r**	**r**	**r**	**r/w**	**r**	**r/w**	**r/w**

reserved	
OC	Overcurrent DCDC1 0: no overcurrent detected 1: overcurrent detected
OT	Overtemperature DCDC1 0: no overtermperature detected 1: overtemperature detected
PG	Power good of DCDC1 status 0: no output voltage power good 1: output voltage power good
ADENDCDC	Enable output auto discharge of DCDC1 0: disabled 1: enabled
reserved	
ENMASK	Enable external DCDC1 enable pin 0: external control off 1: external control on
EN	Enable DCDC1 0: disabled 1: enabled

DCDC2_CTRL Register Address: 0x0D							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
reserved	OC	OT	PG	ADENDCDC	reserved	ENMASK	EN
1	**0**	**0**	**0**	**1**	**1**	**1**	**0**
r	**r**	**r**	**r**	**r/w**	**r**	**r/w**	**r/w**

reserved	
OC	Overcurrent DCDC2 0: no overcurrent detected 1: overcurrent detected
OT	Overtemperature DCDC2 0: no overtermperature detected 1: overtemperature detected
PG	Power good of DCDC2 status 0: no output voltage power good 1: output voltage power good
ADENDCDC	Enable output auto discharge of DCDC2 0: disabled 1: enabled
reserved	
ENMASK	Enable external DCDC2 enable pin 0: external control off 1: external control on
EN	Enable DCDC2 0: disabled 1: enabled

DCDC3_CTRL Register Address: 0x0E							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
reserved	OC	OT	PG	ADENDCDC	reserved	ENMASK	EN
1	**0**	**0**	**0**	**1**	**1**	**1**	**0**
r	**r**	**r**	**r**	**r/w**	**r**	**r/w**	**r/w**

reserved	
OC	Overcurrent DCDC3 0: no overcurrent detected 1: overcurrent detected
OT	Overtemperature DCDC3 0: no overtermperature detected 1: overtemperature detected
PG	Power good of DCDC3 status 0: no output voltage power good 1: output voltage power good
ADENDCDC	Enable output auto discharge of DCDC3 0: disabled 1: enabled
reserved	
ENMASK	Enable external DCDC3 enable pin 0: external control off 1: external control on
EN	Enable DCDC3 0: disabled 1: enabled

FET1_CTRL Register Address: 0x0F							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
TOFET1	OCFET1	OTFET1	PGFET1	WTFET1[1]	WTFET1[0]	ADENFET1	ENFET1
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**
r	**r**	**r**	**r**	**r/w**	**r/w**	**r/w**	**r/w**

TOFET1	Timeout FET1, startup, overload 0: no timeout detected 1: timeout detected
OCFET1	Overcurrent FET1 0: no overcurrent detected 1: overcurrent detected
OTFET1	Overtemperature FET1 0: no overtermperature detected 1: overtemperature detected
PGFET1	Power good of FET1 status 0: no output voltage power good 1: output voltage power good
WTFET1[1:0]	Wait time for current limited timeout of FET1 00: 200 us minimum wait time 01: 800 us minimum wait time 10: 1600 us minimum wait time 11: 3200 us minimum wait time
ADENFET1	Enable output auto discharge of FET1 0: disabled 1: enabled
ENFET1	Enable FET1 0: disabled 1: enabled

FET2_CTRL Register Address: 0x10							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
TOFET2	OCFET2	OTFET2	PGFET2	WTFET2[1]	WTFET2[0]	ADENFET2	ENFET2
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**
r	**r**	**r**	**r**	**r/w**	**r/w**	**r/w**	**r/w**

TOFET2	Timeout FET2, startup, overload 0: no timeout detected 1: timeout detected
OCFET2	Overcurrent FET2 0: no overcurrent detected 1: overcurrent detected
OTFET2	Overtemperature FET2 0: no overtermperature detected 1: overtemperature detected
PGFET2	Power good of FET2 status 0: no output voltage power good 1: output voltage power good
WTFET2[1:0]	Wait time for current limited timeout of FET2 00: 200 us minimum wait time 01: 800 us minimum wait time 10: 1600 us minimum wait time 11: 3200 us minimum wait time
ADENFET2	Enable output auto discharge of FET2 0: disabled 1: enabled
ENFET2	Enable FET2 0: disabled 1: enabled

FET3_CTRL Register Address: 0x11							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
TOFET3	OCFET3	OTFET3	PGFET3	WTFET3[1]	WTFET3[0]	ADENFET3	ENFET3
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**
r	**r**	**r**	**r**	**r/w**	**r/w**	**r/w**	**r/w**

TOFET3	Timeout FET3, startup, overload 0: no timeout detected 1: timeout detected
OCFET3	Overcurrent FET3 0: no overcurrent detected 1: overcurrent detected
OTFET3	Overtemperature FET3 0: no overtermperature detected 1: overtemperature detected
PGFET3	Power good of FET3 status 0: no output voltage power good 1: output voltage power good
WTFET3[1:0]	Wait time for current limited timeout of FET3 00: 200 us minimum wait time 01: 800 us minimum wait time 10: 1600 us minimum wait time 11: 3200 us minimum wait time
ADENFET3	Enable output auto discharge of FET3 0: disabled 1: enabled
ENFET3	Enable FET3 0: disabled 1: enabled

FET4_CTRL Register Address: 0x12							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
TOFET4	OCFET4	OTFET4	PGFET4	WTFET4[1]	WTFET4[0]	ADENFET4	ENFET4
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**
r	**r**	**r**	**r**	**r/w**	**r/w**	**r/w**	**r/w**

TOFET4	Timeout FET4, startup, overload 0: no timeout detected 1: timeout detected
OCFET4	Overcurrent FET4 0: no overcurrent detected 1: overcurrent detected
OTFET4	Overtemperature FET4 0: no overtermperature detected 1: overtemperature detected
PGFET4	Power good of FET4 status 0: no output voltage power good 1: output voltage power good
WTFET4[1:0]	Wait time for current limited timeout of FET4 00: 200 us minimum wait time 01: 800 us minimum wait time 10: 1600 us minimum wait time 11: 3200 us minimum wait time
ADENFET4	Enable output auto discharge of FET4 0: disabled 1: enabled
ENFET4	Enable FET4 0: disabled 1: enabled

FET5_CTRL Register Address: 0x13							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
TOFET5	OCFET5	OTFET5	PGFET5	WTFET5[1]	WTFET5[0]	ADENFET5	ENFET5
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**
r	**r**	**r**	**r**	**r/w**	**r/w**	**r/w**	**r/w**

TOFET5	Timeout FET5, startup, overload 0: no timeout detected 1: timeout detected
OCFET5	Overcurrent FET5 0: no overcurrent detected 1: overcurrent detected
OTFET5	Overtemperature FET5 0: no overtermperature detected 1: overtemperature detected
PGFET5	Power good of FET5 status 0: no output voltage power good 1: output voltage power good
WTFET5[1:0]	Wait time for current limited timeout of FET5 00: 200 us minimum wait time 01: 800 us minimum wait time 10: 1600 us minimum wait time 11: 3200 us minimum wait time
ADENFET5	Enable output auto discharge of FET5 0: disabled 1: enabled
ENFET5	Enable FET5 0: disabled 1: enabled

FET6_CTRL Register Address: 0x14							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
TOFET6	OCFET6	OTFET6	PGFET6	WTFET6[1]	WTFET6[0]	ADENFET6	ENFET6
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**
r	**r**	**r**	**r**	**r/w**	**r/w**	**r/w**	**r/w**

TOFET6	Timeout FET6, startup, overload 0: no timeout detected 1: timeout detected
OCFET6	Overcurrent FET6 0: no overcurrent detected 1: overcurrent detected
OTFET6	Overtemperature FET6 0: no overtermperature detected 1: overtemperature detected
PGFET6	Power good of FET6 status 0: no output voltage power good 1: output voltage power good
WTFET6[1:0]	Wait time for current limited timeout of FET6 00: 200 us minimum wait time 01: 800 us minimum wait time 10: 1600 us minimum wait time 11: 3200 us minimum wait time
ADENFET6	Enable output auto discharge of FET6 0: disabled 1: enabled
ENFET6	Enable FET6 0: disabled 1: enabled

FET7_CTRL Register Address: 0x15							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
TOFET7	OCFET7	OTFET7	PGFET7	WTFET7[1]	WTFET7[0]	ADENFET7	ENFET7
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**
r	**r**	**r**	**r**	**r/w**	**r/w**	**r/w**	**r/w**

TOFET7	Timeout FET7, startup, overload 0: no timeout detected 1: timeout detected
OCFET7	Overcurrent FET7 0: no overcurrent detected 1: overcurrent detected
OTFET7	Overtemperature FET7 0: no overtermperature detected 1: overtemperature detected
PGFET7	Power good of FET7 status 0: no output voltage power good 1: output voltage power good
WTFET7[1:0]	Wait time for current limited timeout of FET7 00: 200 us minimum wait time 01: 800 us minimum wait time 10: 1600 us minimum wait time 11: 3200 us minimum wait time
ADENFET7	Enable output auto discharge of FET7 0: disabled 1: enabled
ENFET7	Enable FET7 0: disabled 1: enabled

AD_CTRL Register Address: 0x16							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
reserved	ADSTART	ADEOC	ENADREF	ADC[3]	ADC[2]	ADC[1]	ADC[0]
0	**0**	**1**	**0**	**0**	**0**	**0**	**0**
r	**r/w**	**r**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**

reserved	
ADSTART	A/D converter conversion start, bit is set to 0 if conversion is completed 0: no conversion in progress, conversion completed 1: start conversion
ADEOC	A/D converter end of conversion 0: conversion not finished 1: conversion finished
ENADREF	Enable A/D converter reference voltage 0: disabled 1: enabled
ADC[3:0]	A/D converter input channel select 0000: VAC 0001: VBAT 0010: IAC 0011: IBAT 0100: IDCDC1 0101: IDCDC2 0110: IDCDC3 0111: IFET1 1000: IFET2 1001: IFET3 1010: IFET4 1011: IFET5 1100: IFET6 1101: IFET7 1110: not used 1111: not used

AD_OUT1 Register Address: 0x17							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
AD0	AD0	AD0	AD0	AD0	AD0	AD0	AD0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	**r**	**r**	**r**	**r**	**r**	**r**	**r**

AD0[7:0]	ADC result data [7:0]

AD_OUT2 Register Address: 0x18							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
reserved	reserved	reserved	reserved	reserved	reserved	AD0	AD0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	**r**	**r**	**r**	**r**	**r**	**r**	**r**

reserved[5:0]	
AD0[9:8]	ADC result data [9:8]

SPARE2 Register Address: 0x1B							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
OTP_RELOAD	SPARE2[6]	SPARE2[5]	SPARE2[4]	SPARE2[3]	SPARE2[2]	SPARE2[1]	SPARE2[0]
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r/w	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**	**r/w**

OTP_RELOAD	Register reset, bit is set to 0 after reset 0: no reset 1: reset register content
SPARE2[6:0]	Spare user register cells

3.3 ALWAYS ON LDO's

As soon as a valid voltage at VSYS is applied the LDO's start operating and providing a regulated output voltage at each of them. If DCDC1 is started the output of the DCDC1 converter will be connected to the output of LDO1 with an internal bypass switch to ensure seamless transition. Finally LDO1 will stop operating. It will start again when the voltage at its output drops below its regulation voltage. In this case both outputs will be disconnected from each other. There will be no current flowing backwards from the LDO1 output to the DCDC1 output. The same function is implemented for DCDC2 and LDO2.

3.4 POWER PATH CONTROL

The device automatically switches adapter or battery power to the system load. The battery is connected to the system by default during power up or if the adapter power is not available. As soon as a valid voltage is detected on VACS and the voltage at VAC is higher than the battery voltage the battery is disconnected and the AC power path switches controlled through the pins ACG and ACS are turned on. The system is powered through the adapter input. If the voltage on VACS is higher than the overvoltage protection threshold the AC power path switches are turned off or not turned on to protect the system from damage. Any voltage on VACS lower than the input undervoltage lockout threshold voltage will cause the AC power path switches to be off.

To protect the device and the system against reverse voltage additional external components are required to protect the pins VAC, VACS ACG and ACS which would be exposed to the reverse voltage. Please check the EVM documentation for more details.

In case the maximum adapter output current is not high enough to supply the complete system the system can be powered through the adapter and the battery at the same time. If the adapter current is limited the adapter voltage will drop to the battery voltage level and the backgate diode of the battery switch will conduct current.

To minimize the losses in this mode of operation the battery switch is turned on. To detect whether there is still a power source connected at the AC input the AC power path switches are turned off every 0.5 s for a few milliseconds. While the AC power path switches are off VAC is discharged through a 1 kΩ resistor to GND. If the voltage at VACS did not drop below the input undervoltage lockout threshold voltage the AC power path switches are turned on again to allow the power source connected to the AC input to supply the system again.

3.5 SUPPLY STATUS OUTPUTS

The status of the power supply is indicated through the status pins VACG, VBATG and VSYSG. All pins are open drain outputs and need a pull up resistor to the respective logic supply voltage they are connected to.

VACG will be high if a voltage is detected at VAC and VACS which is in a useable window. This means the voltage detected at VACS must be lower than the overvoltage threshold and it must be higher than the input undervoltage lockout threshold voltage. Also the voltage at VAC must be higher than battery voltage. If no battery is connected the minimum voltage is above the undervoltage lockout threshold.

VSYSG will be high as soon as the system voltage, detected at VSYS_L1 and VSYS_L2 is above its undervoltage thresholds.

VBATG will be high if the voltage detected at FBC is between the minimum and the maximum voltage for battery good detection and the differential voltage V_{SRN} - V_{VBAT} is lower than 20 mV. This indicates that the battery discharge current is not exceeding the programmed maximum level.

3.6 CHARGER

Charging can be enabled by using the ENC pin or by programming the respective register through I2C. The charger will then start working when VACG is detected. If the battery is completely charged or charging has been terminated for any other reason, the charger will stay idle. Charging can be restarted by disabling the charger and enabling it again.

As soon as the charger is enabled it starts with battery detection as shown in Figure 3-7. If no battery or a battery short is detected the charger will continue with battery detection. If the battery is detected it will start charging.

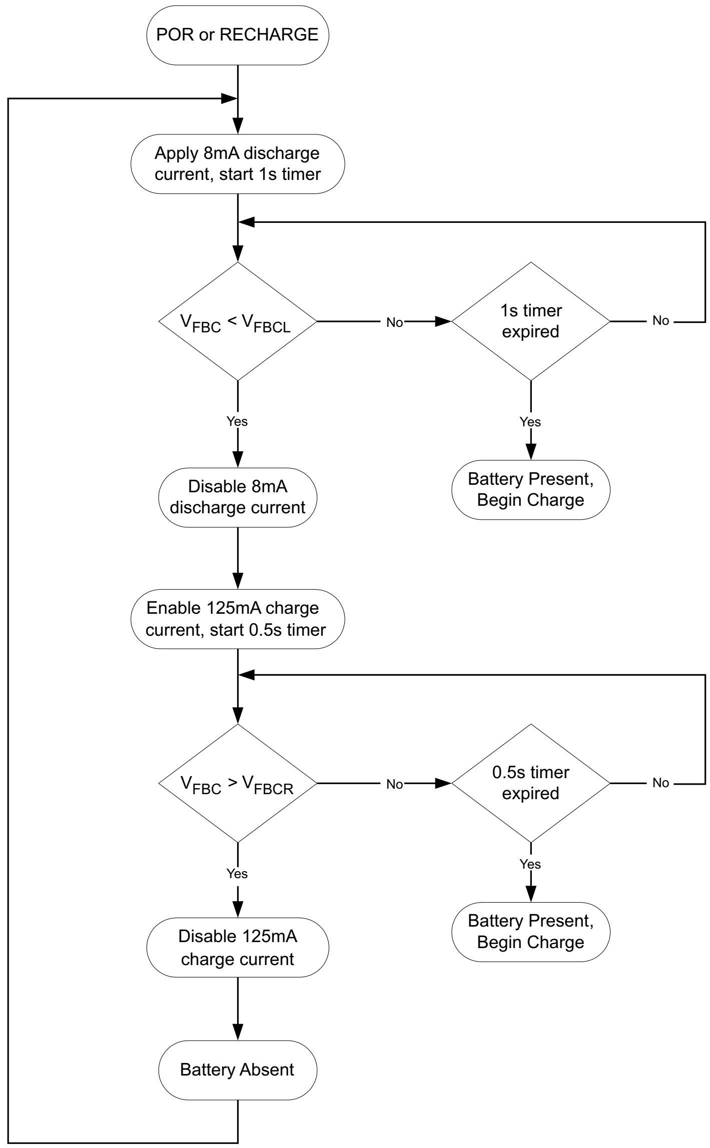


Figure 3-7. Battery Detection

The charger controls a low constant charge current during a precharge phase when the battery is at a very low voltage and needs to be recovered. It controls a high fastcharge current if the battery voltage is above the low voltage threshold and below the charge termination voltage. If the battery voltage has reached the charge termination voltage the charger controls this voltage until the charge current has decayed below the charge termination threshold or the fastcharge safety timer has timed out. Precharge current and charge termination current are either 10% of the programmed fastcharge current if the fastcharge current is set to 1A or higher. Otherwise they will be controlled to 100mA. A complete charging cycle is shown in Figure 3-8.

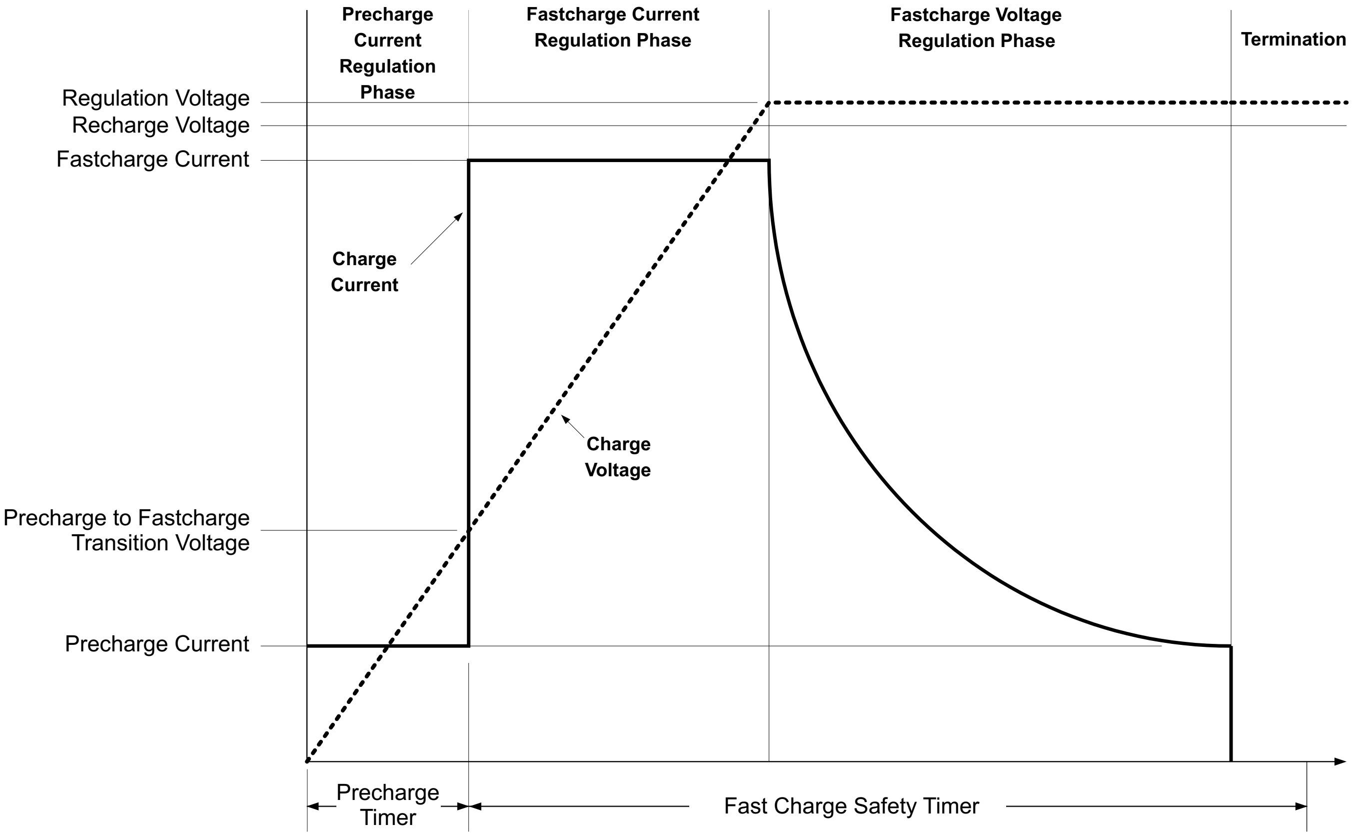


Figure 3-8. Charging Cycle

To support charging with weak power sources the charger stays in operation even if it can not control the charge current at the programmed level. For this operating condition the charge termination based on low charge current can be turned off by programming the respective register.

The fastcharge safety timer is programmed to its lowest value by default. The timeout time can be increased by programming higher values in the respective registers. It cannot be turned off.

All charge currents are defined depending on the current sense resistor connected between the pins SRN and SRP. The maximum fastcharge current generates a 40 mV voltage drop across this resistor. All other currents are lower.

The charge termination voltage is defined by a resistive voltage divider connected between battery, feedback input of the charger (FBC) and GND. The maximum voltage at FBC which is controlled is typically 2.1 V.

The charger has also inputs to measure the battery cell temperature. It supports using 2 different temperature sensors which can be placed at different locations in the battery pack. For more details on the temperature sensing circuit please refer to the applications section. For biasing the temperature sense resistor networks and the internal comparator reference the voltage at the VREFT pin is used. It is turned off if the charger is disabled.

Charge current and charge termination voltage can be programmed to lower than the maximum values using the digital interface. They are also controlled and forced to lower values depending on the measured battery cell temperature. The respective values for the 5 different temperature regions can be programmed in the charge control registers (CG_CTRLx) using the digital interface. Default settings for temperature thresholds and the respective fastcharge current and charge termination voltages are defined according to JEITA recommendations for multicell battery packs. The definitions for the thresholds and temperature zones are shown in Figure 3-9. Figure 3-9 also shows the default values for temperature thresholds, charge current and charge termination voltage, which are programmed in TPS65090A. The optional values which can be programmed via the digital interface, can be found in the electrical characteristics table. The actual temperature zones the charger operates in, can be read out from the charge status register CG_STATUS1.

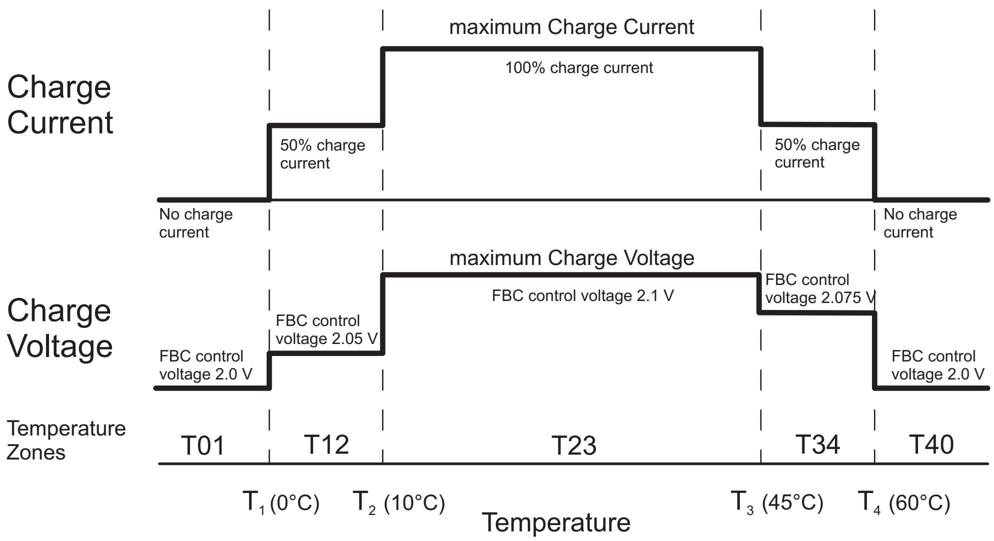


Figure 3-9. JEITA Charging Profile

If the adapter current measured with a sense resistor between the pins ACN and ACP exceeds its programmed value or the adapter voltage measured at VACS drops below a certain level (typically 7V, see electrical characteristics table) the charge current is reduced automatically to avoid an overload condition of the AC adapter and an undervoltage condition for the system. The charge current is also reduced if the charger temperature measured in the IC is exceeding 100°C.

The charger indicates it's current status of operation in 2 different ways. One is the STAT output pin which can be used to drive an LED. It can have 3 different states as described in Table 3-1. To get details about the current state of charging the charging status register CG_STATUS1 can be read.

Table 3-1. Charger status pin STAT

Charging State	STAT pin state
charging complete sleep mode charging disabled	HIGH
charging in progress (including recharging)	LOW
charging suspended no battery detected safety timer fault (precharge, fastcharge)	blinking with 0.5 Hz

A status change from charging suspended to charging active and back sets the interrupt CGACT and charging completed sets the interrupt CGCPL. Both interrupts can be masked. If not masked, they will trigger IRQ pin to go low when they are set.

3.7 DCDC CONVERTERS

The built in DCDC converters are completely integrated except the required passive components. To maintain high efficiency they are implemented as synchronous step down converters. At medium and heavy loads they are operating in a PWM mode. As soon as the inductor current gets discontinuous, which means that the output current gets lower than half of the inductor ripple current the converters enter Power Save Mode. In Power Save Mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

All DCDC converters can be enabled using their ENx pins. If they should be enabled using the digital interface the enable pin function can be masked in the DCDCx_CTRL register. If masked enable only works by writing a 1 to the EN bit in the DCDCx_CTRL register.

As soon as the output voltage reaches 80% of the input voltage the power good register bit for this converter is set to 1. If the output voltage drops below this threshold the power good bit is set back to 0.

The startup of the converter is controlled by an internal softstart to make sure the output voltage is built up smooty and the inrush current during startup is kept at minimum.

All converters are current limited. The current limit is controlling the maximum output current. If the current limit is controlling the converter its respective OLDCDCx interrupt bits are set to 1. The OLDCDCx interrupt bits can be masked. If not masked, they will trigger IRQ pin to go low when they are set.

To make sure that the output voltage of the DCDC converters is decreasing fast to a safe low value a built in output auto discharge function can be enabled using the ADENDCDC bit in the respective DCDCx_CTRL register. If enabled the output capacitors are actively discharged as soon as the converter is disabled. While the converter is enabled its output discharge circuit is off to save power.

3.8 LOAD SWITCHES

Load switches are turned on using the digital control interface by writing a 1 in the ENFETx bit of their load switch control register FETx_CTRL. They can not be enabled before DCDC1 and DCDC2 have been started and their output voltage is above their power good level. If DCDC1 or DCDC2 will be disabled load switches will be immediately disabled as well and enabled if both DCDC converters are enabled again.

After being turned on the output voltage of the load switch is ramped up with a controlled slope (< 1.0 V / µs) . The current limit is active during that time and does not allow the current to overshoot. This means the slope can be slower if controlled by the current limit.

After being turned on a timer is started. If the timer terminates the output voltage must have reached the input voltage. Otherwise the load switch is turned off again expecting an overload condition. The minimum value of the timer is 200 µs. This timer is used as well if the load switch control limits the current. It can be extended via the digital control interface using 4 steps (max factor 16 up to 3 ms). If the load switch has been turned off by this safety timer it can only been turned on again by reprogramming its ENFETx bit to 1 again.

As soon as the output voltage reaches 80% of the input voltage the power good register bit for this load switch is set to 1. If the output voltage drops below this threshold the power good bit is set back to 0.

All load switches are current limited. The current limit is regulating the maximum output current. A temperature sensor can trigger the turn off of the load switch as well. If the current limit is controlling the switch their respective OLFETx interrupt bits are set to 1. The OLFETx interrupt bits can be masked. If not masked, they will trigger IRQ pin to go low when they are set.

To make sure that a voltage on the output of FET2 is not supplying its input while turned off it is reverse current protected. This feature is only available at FET2 to support controlling circuit blocks which can get power from an external source while the system is turned off, like HDMI.

To make sure that the output voltage of the load switches is decreasing fast to a safe low value a built in output auto discharge function can be enabled using the ADENFETx bit in the respective FETx_CTRL register. If enabled the output capacitors are actively discharged as soon as the load switch is disabled. While the load switch is enabled its output discharge circuit is off to save power.

3.9 A/D CONVERTER

A/D conversion is controlled according to the flowchart shown in Figure 3-10. After enabling the A/D converter the channel which should be measured must be defined in the A/D converter control register. A/D conversion is started by writing the start command in the A/D control register. As soon as conversion is finished ADEOC is set to 1 and the data is available in the ADOUT registers.

AD_CTRL[3:0]	Channel
4'b0000	VAC
4'b0001	VBAT
4'b0010	IAC
4'b0011	IBAT
4'b0100	IDCDC1
4'b0101	IDCDC2
4'b0110	IDCDC3
4'b0111	IFET1
4'b1000	IFET2
4'b1001	IFET3
4'b1010	IFET4
4'b1011	IFET5
4'b1100	IFET6
4'b1101	IFET7
4'b1110	IFET7
4'b1111	IFET7

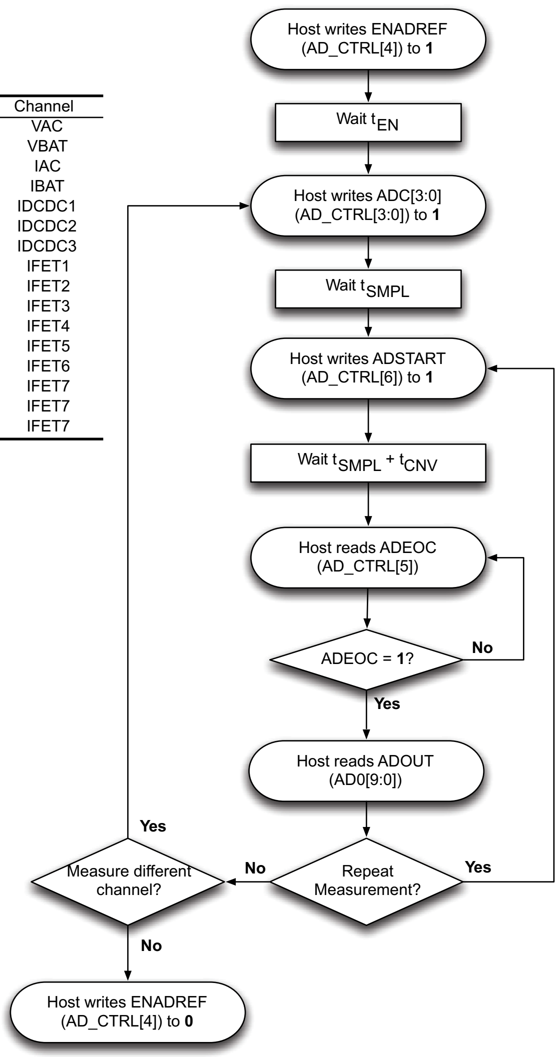


Figure 3-10. A/D Conversion

3.10 PROTECTION

The device has 2 built in under voltage detectors. If the system voltage is not high enough to safely operate the DCDC converters they are shut down with the higher undervoltage threshold which also sets VSYSG high as soon as the system voltage has increased above this threshold. At this condition the LDO's are still on to supply the internal control circuitry. If the system voltage further decreases and hits the second lower undervoltage threshold the LDO's are turned off as well and the internal control circuit is disabled. The control circuit is reset and started again if the supply voltage increases above the lower undervoltage threshold.

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table) the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

3.11 INTERRUPTS

The device monitors several internal states of power path, charger, DCDC converters and load switches. If any of those states changes, an interrupt can be asserted. By default all states are masked, so any state which should generate an interrupt needs to be unmasked. If an unmasked state changes it will generate an interrupt, which means the output impedance of the IRQ pin will go low and, if properly connected the voltage will go low. What has caused the interrupt can be read out from the interrupt status registers IRQ1 and IRQ2. The interrupt will be cleared by writing a zero to the IRQ bit in the interrupt status register IRQ1. The content of the status registers are refreshed only after an interrupt has occurred.

3.1 APPLICATION INFORMATION

3.1.1 DESIGN PROCEDURE

The TPS65090 Front-end PMU Integrated circuit is intended for systems powered by a two or three-cell Li-Ion or Li-Polymer battery with a typical voltage between 6 V and 17 V. Additionally, any other voltage source with a typical output voltage between 6 V and 17 V can power systems where the TPS65090 is used.

3.1.2 PROGRAMMING THE CONVERTER OR CHARGER OUTPUT VOLTAGE

Within the TPS65090 device, there are fixed and adjustable outputs. In the case where the voltage is adjustable, an external resistor divider is used to set the output voltage. The resistor divider must be connected between the output, the feedback pin and GND. When the output voltage is regulated properly, the voltage at the feedback pin will be in the range as defined in the electrical characteristics, i.e. 800 mV for DCDC3 and 2.1 V for the charger. The feedback pin typically has 0.1 μA of leakage; to meet this current requirement and maintain the feedback voltage, it is recommend to set the feedback divider current by at least a factor of ten to one-hundred times that of the pin leakage. Using the feedback voltage of 2.1 V and 10 μA (100 * 0.1 μA), the resistor between the feedback pin and GND can be calculated to need to be less than 210kΩ. This value for the resistor will provide sufficient current through the resistor divider at the typical feedback voltage. Selecting resistor values is a trade off between noise immunity and light load efficiency. The lower the resistor value, the higher the noise immunity; however, the more current through the resistor, the less efficient the converter is at light loads. Consider R1 is connected from the output of the inductor to the feedback pin and R2 from the feedback pin to ground. From the recommendations for R2, less than 210kΩ, the value of the resistor connected between the output and feedback, R1, depending on the desired output voltage V_{OUT}, can be calculated using Equation 1.

$$R1 = R2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \tag{1}$$

The following table contains recommended values for the feedback divider for the most common output voltages.

Table 3-1. Feedback Reistor Values for Common Converter Ouput Voltages

Output Voltage	1.2 V	1.35 V	1.8 V	3.3 V
R1 [kΩ]	260	330	510	750
R2 [kΩ]	510	470	400	240

Table 3-2. Feedback Resistor Value for Common Charger Output Voltages

Output Voltage	8.4 V	12.6 V
R1 [kΩ]	330	1100
R2 [kΩ]	110	220

3.1.3 PROGRAMMING INPUT DPM CURRENT AND CHARGE CURRENT

Maximum input DPM current and charge current are defined by the values of the sense resistors used. The sense resistor value RS can be calculated using Equation 2.

$$RS = \frac{V_S}{I_S} \tag{2}$$

V_S is the differential voltage at the sense input pins, for input current DPM it is the differential voltage between ACP and ACN and for charge current regulation between SRP and SRN. The maximum value for the differential voltage which is recommended to be used here is 40 mV. More details can be found in the electrical characteristics section of power path control and charger.

I_S is the maximum current which needs to be controlled, for input current DPM it is the maximum input current where charging is still allowed and for charge current regulation it is the maximum charge current.

3.1.4 OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS65090 is optimized to work within a range of L and C combinations. The LC output filter inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter.

3.1.5 INDUCTOR SELECTION

At the L pins of the DCDC converters and the charger, connecting an inductor is required.

At the DCDC converters it is recommended to use a 2.2 μH inductor with an appropriate current rating for the application. The derated inductance at high currents should not drop lower than 1 μH.

At the charger it is recommended to use a 2.2 μH inductor for fast charge currents of 3 A and above. For lower fast charge currents, 3.3 μH can be used. The current rating of the inductor must be suitable for the maximum fast charge current required in the application.

The inductor value affects its peak-to-peak ripple current, the PWM-to-PSM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

To properly configure the converter, an inductor must be connected between pin L the output capacitors. To estimate the inductance value, Equation 3 can be used.

$$L = \left(V_{IN} - V_{OUT}\right) \cdot 0.5 \cdot \frac{\mu s}{A} \tag{3}$$

In Equation 3, the minimum inductance value, *L*, is calculated. V_{IN} is the minimum input voltage. As an example, a suitable inductor for generating 1.35V from a two-cell Li-Ion battery is 2.2 μH.

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 4 shows how to calculate the peak current I_{MAX} in step down mode operation.

$$I_{MAX} = \frac{I_{OUT}}{0.8} + \frac{V_{OUT} \cdot \left(V_{IN} - V_{OUT}\right)}{2 \cdot V_{IN} \cdot f \cdot L} \tag{4}$$

In the equation, *f* is the minimum switching frequency, which typically is in the range of 1 MHz. V_{IN} is the minimum input voltage. The critical current value for selecting the right inductor is the value of I_{MAX} . Consideration must be given to the load transients and error conditions that can cause higher inductor currents. This must be taken into consideration when selecting an appropriate inductor.

In DC/DC converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The following inductor types from different suppliers have been used with TPS65090 converters:

Table 3-3. List of Inductors

VENDOR	INDUCTOR SERIES
Coilcraft	XAL4020-222, XAL5030-222
Cyntec	PILE061E-2R2MS-11

Table 3-3. List of Inductors (continued)

VENDOR	INDUCTOR SERIES
Toko	FDV0530-2R2M
Wurth Elektronik	WE 74437324022

3.1.6 CAPACITOR SELECTION

3.1.6.1 Input Capacitor

Because of the nature of the switching converter and charger with a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, at least 10µF ceramic capacitor is recommended. The voltage rating and DC bias characteristic of ceramic capacitors need to be considered. The input capacitor can be increased without any limit for better input voltage filtering. A ceramic capacitor placed as close as possible to the respective VSYS and PGND pins of the IC is recommended.

3.1.6.2 DCDC Converter and Charger Bootstrap Capacitors

To make sure that the internal high side gate drivers are supplied with a stable low noise supply voltage, a capacitor must be connected between the CBx pins and the respective Lx pins.

Using a ceramic capacitor with a value of 4700 pF is recommended. The value of this capacitor should not be lower than 2200 pF or higher than 0.01 µF. For testing, a 4700 pF, size 0402, 6.3 V capacitor was used.

3.1.6.3 DCDC Converter and Charger Output Capacitors

Ceramic capacitors with low ESR values provide the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode and tighten DC output accuracy in PFM Mode. In order to achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC - bias voltage.

For the output capacitors of the DCDC converters and the charger use of a small ceramic capacitors placed as close as possible to the output pins and the respective PGND pins of the IC is recommended. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the output pins and the respective PGND pins of the IC.

At the DCDC converters the capacitance close to the IC is recommended to be close to 22 µF. It should not be lower than 10 µF or higher than 47 µF.

At the charger 22 µF capacitance is recommended.

To get an estimate of the recommended minimum output capacitance, Equation 5 can be used.

$$C_{OUT} \geq \frac{22 \cdot \mu F \cdot \mu H}{L} \tag{5}$$

A capacitor with a value in the range of or higher than the calculated minimum should be used. This is required to maintain control loop stability.

3.1.6.4 LDO Output Capacitors

To achieve stable and accurate output voltage regulation of the LDO's, a small ceramic capacitor is required at their outputs. It is recommended to use at least 2.2 µF.

3.1.6.5 Load Switches Output Capacitors

The maximum expected output capacitance at the load switches is 47 µF. Any lower value can be used.

3.1.7 CHARGER BATTERY TEMPERATURE SENSING

To measure the battery cell temperature, resistors with temperature dependent resistance (NTC) need to be placed close to the cells which need to be measured. The device supports using two independent measuring points with its TS1 and TS2 input pins. The temperature sense resistor and the linearizing resistor network must be the same. If only one temperature sense resistor is used, the sense resistor network must be connected to TS1 and TS2.

As a default, the internal circuit is optimized to work with a 10 kΩ NTC resistor with a temperature characteristic described with a B value in the range of 3450 with one resistor in parallel and one resistor in series for linearization and to define the resistor divider connected to VREFT, TSx and AGND. A possible default example would be NTCS0805E3103FLT from Vishay in parallel with a 6.8 kΩ resistor and a 2.2 kΩ resistor in series.

3.1.8 REVERSE VOLTAGE PROTECTION

To protect the design against reverse voltage at the AC adapter input, additional external components are required. The pins VAC, VACS and the input path switches are exposed to the negative voltage and need some protection.

To protect the VAC pin, using a small signal diode between the adapter input and the VAC pin is recommended.

Protecting VACS can be done either by connecting this pin to the protected VAC with the tradeoff of losing accuracy or connecting VACS to the adapter input with a 10 kΩ resistor.

To make sure that the AC switches are not turned on with the reverse voltage at the AC adapter input, a small signal n-channel FET can be used to short the voltage at ACG to ACS. The source of this FET must be connected to ACS, the drain to ACG. The gate must be connected to the AC adapter input GND either direct or, if the maximum gate voltage rating does not match the maximum input voltage, with a resistor divider between AC adapter input GND and ACS. An example for the small signal FET would be BSS138W-7-F. To protect the ACS and the ACG pin resistors with values in the range of 4.7 kΩ or higher between the pins and the gate and source pins of the AC FET's must be used.

An example for this additional reverse protection circuit can be found in the TPS65090EVM User's Guide.

3.1.9 AC SWITCHES

The AC adapter protection switches are recommended as CSD17304Q3: MOSFET, NChan, 30V, 56A, 9.8 milliOhm.

3.1.10 BATTERY SWITCHES

The battery switches are recommended as CSD25401Q3: MOSFET, PChan, -20V, 60A, 8.7 milliOhm.

3.1.11 LAYOUT CONSIDERATIONS

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, short traces are recommended as well, separation from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

A layout example can be found in the TPS65090EVM User's Guide.

3.1.12 THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the PowerPAD™
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table please check the Thermal Characteristics Application Note (SZZA017) and the IC Package Thermal Metrics Application Note (SPRA953).

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2013) to Revision A	Page
• Added Differential Voltage spec condition "between CBC and LC", –0.3 MIN and 7 MAX	4
• Changed graph title from "ADAPTER INPUT POWER UP AND POWER DOWN" to "SUPPLEMENT MODE OPERATION"	30
• Changed text in ALWAYS ON LDOs and POWER PATH CONTROL sections for clarification.	49
• Changed text in CHARGER section for clarification.	51
• Added INTERRUPTS section for clarification.	55
• Added text to REVERSE VOLTAGE PROTECTION section for clarification.	59
• Added text to THERMAL INFORMATION section for clarification.	60

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65090ARVNR	Active	Production	VQFN-MR (RVN) | 100	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS65090A
TPS65090ARVNR.A	Active	Production	VQFN-MR (RVN) | 100	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS65090A
TPS65090ARVNT	Active	Production	VQFN-MR (RVN) | 100	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS65090A
TPS65090ARVNT.A	Active	Production	VQFN-MR (RVN) | 100	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS65090A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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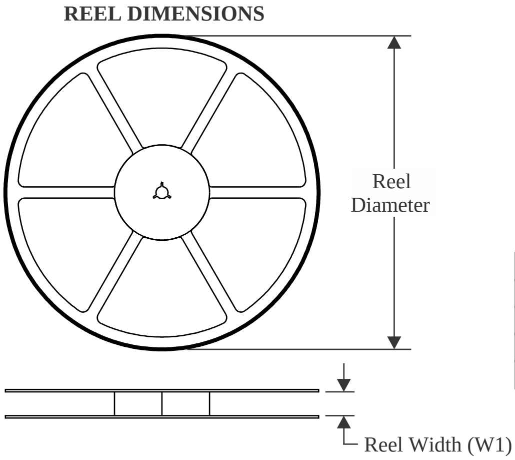
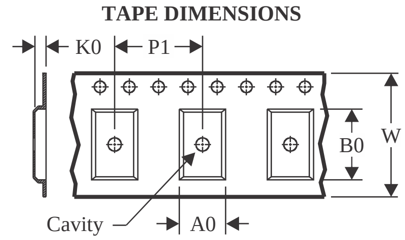
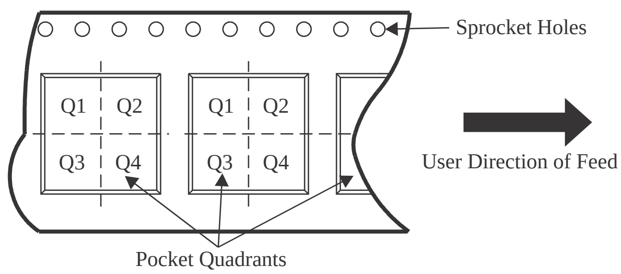
TAPE AND REEL INFORMATION





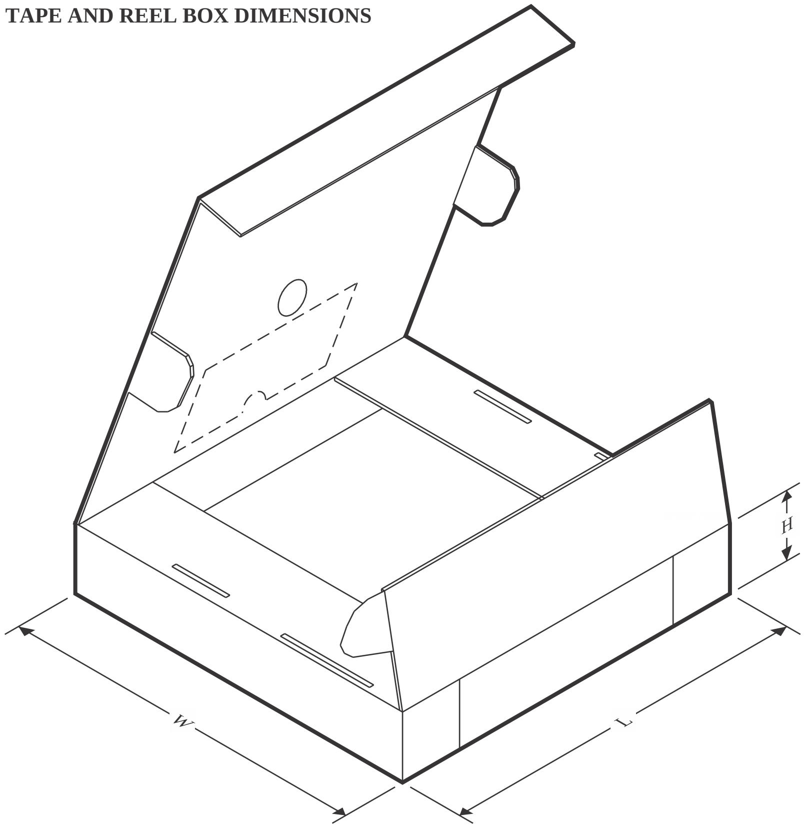
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65090ARVNR	VQFN-MR	RVN	100	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
TPS65090ARVNT	VQFN-MR	RVN	100	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

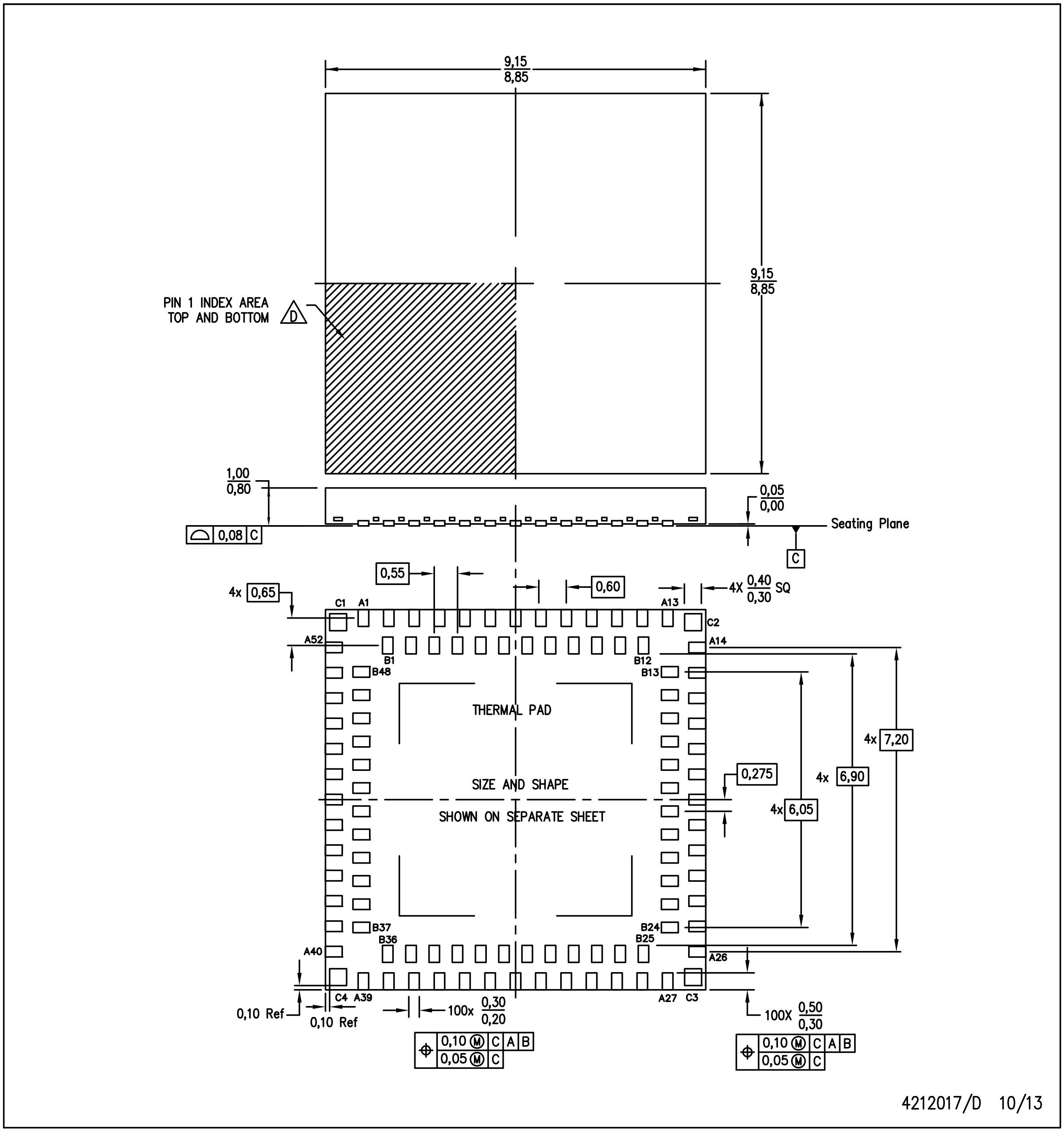
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65090ARVNR	VQFN-MR	RVN	100	2500	367.0	367.0	38.0
TPS65090ARVNT	VQFN-MR	RVN	100	250	210.0	185.0	35.0

RVN (S—PVQFN—N100) PLASTIC QUAD FLATPACK NO—LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No—leads (QFN) staggered multi—row package configuration.
- D. Pin A1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin A1 identifiers are either a molded, marked, or metal feature.
- E. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- F. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

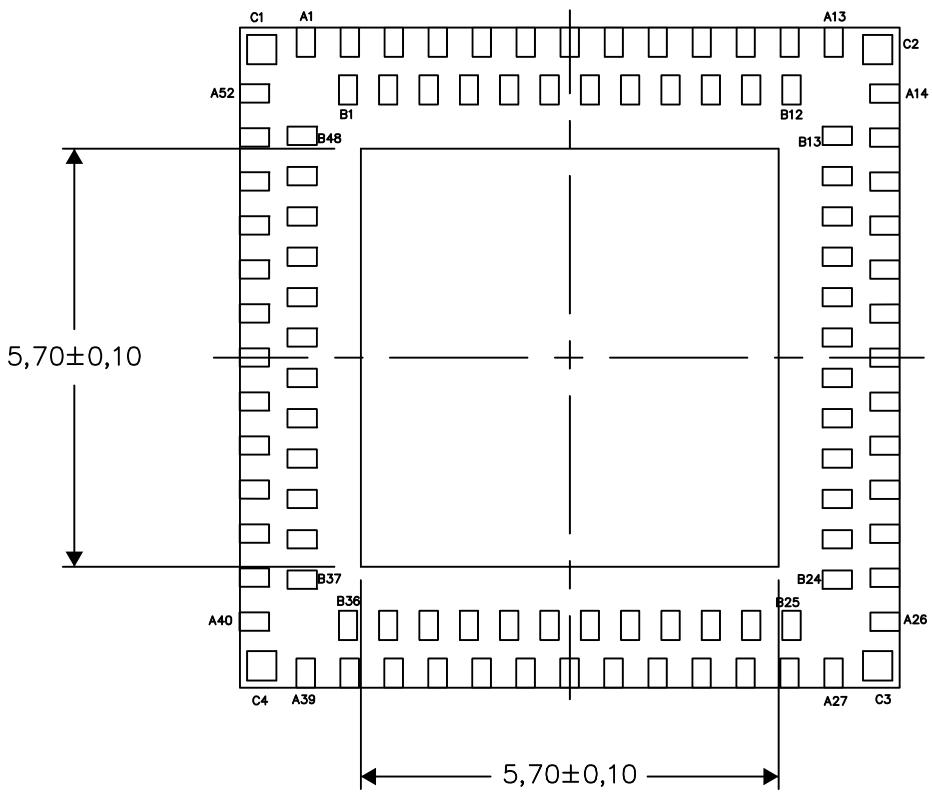
RVN (S-PVQFN-N100) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4212047-3/D 04/13

NOTE: All linear dimensions are in millimeters

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