TPS650830 面向移动计算机的简单而灵活的宽输入电压电源管理单元 (PMU)

1 特性

- 5 个可重新配置的稳压器：
  - 可在宽输入电压和宽输出电流范围内保持高效
  - 可更改电压、电流和序列以优化系统
  - 4 个采用外部功率金属氧化物半导体场效应晶体管 (MOSFET) 的可变输出电压降压控制器：
    - VR1 = 1V；VR3 = 3.3V，VR4 = 1.2V/1.35V/1.1V（对于 DDRx VDDQ），VR5 = 5V
    - V_{IN} 范围：5.4V 至 24V
    - 采用外部功率 MOSFET，连续输出电流范围为 <1A 至 >10A
  - 1 个带有内部功率 MOSFET 的可变输出电压降压转换器：
    - VR2 = 1.8V
    - V_{IN} 范围：3V 至 3.6V
    - 高达 2A 的持续输出电流
  - 输出电压直流精度 ±1%；直流 + 交流精度 ±5%，支持差分输出电压感测
  - 在超低静态电流模式下，每个控制器或转换器的静态电流典型值为 30μA
- 3 个固定输出电压低压降线性稳压器 (LDO)：
  - LDO1：1/2 VR4 固定输出电压 LDO（对于 DDRx VTT）(Vout = VDDQ/2)
    - 连续输出电流高达 1A，直流 + 交流精度 ±5%，峰值电流为 2A
  - LDO3：3.3V 固定输出电压 LDO，直流精度 ±1%，电流 < 40mA
    - 用于外部模数转换器 (ADC) 的高精度参考电源
    - 用于 EC_VCC 电源轨的 3.3V 负载开关
  - LDO5：5V 固定输出电压 LDO，直流精度 ±1%，电流 < 100mA
    - 用于控制器和转换器栅极驱动的电源
    - 可自动切换至 5V 稳压器以实现高效率
- 8 个用于外部稳压器、负载开关或 LDO 的电源正常状态比较器和序列逻辑
- 支持电源按钮逻辑且可编程响应时间
- 2 个通用电平转换器
- 用于实时时钟 (RTC) 域的备用电池/3.1V LDO 选择器输出
- 电源检测和监视：适配器、电池 1 和电池 2
- 过温保护比较器，用于堆叠式正温度系数 (PTC) 热敏电阻或单个负温度系数 (NTC) 热敏电阻
- 1Hz 嵌入式控制器 (EC) 唤醒时钟输出
- 先进的系统复位控制
- I^2C 接口：标准模式 (100kHz)，快速模式 (400kHz)，快速模式+ (1000kHz)

2 应用

- NVDC 或非 NVDC 电源系统架构
- 2 节、3 节或 4 节串联锂电池供电类产品
- 平板电脑、超极本、二合一电脑和笔记本电脑
- 移动 PC、一体化计算机、移动因特网设备
- 现场可编程逻辑门阵列 (FPGA)，工业计量设备，个人医疗产品

3 说明

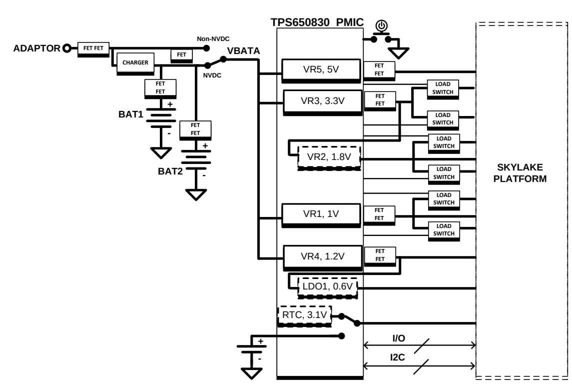
TPS650830 是一款单芯片解决方案电源管理集成电路 (IC)，专为最新的 Intel 处理器而设计，主要应用于由 2 节、3 节或 4 节串联锂离子电池组供电且采用 NVDC 或非 NVDC 电源架构的平板电脑、超极本和笔记本电脑。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS650830	NFBGA (168)	7.00mm x 7.00mm
	NFBGA (159)	9.00mm x 9.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化系统图



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4 修订历史记录

日期	修订版本	注释
2014年12月	*	最初发布。

5 说明（续）

TPS650830 应用于 Volume 系统，该系统采用合并式低电压轨，可实现体积最小且成本最低的系统电源解决方案。

TPS650830 可基于 Intel 参考设计提供完整的电源解决方案。 该器件具有 5 个高效降压稳压器 (VR) 和 1 个灌/拉 LDO，可与上电序列逻辑器件搭配使用以管理外部负载开关，从而提供正确的电源轨、排序和保护，其中包括 DDR3 和 DDR4 存储器电源。 该稳压器支持动态电压调节 (DVS)，可最大限度地提高效率（包括联网待机功能）。 高频稳压器采用小型电感和电容，以减小解决方案体积。 可通过 4 个 VR 控制器调节输出功率。 凭借 I^2C 接口，可以通过嵌入式控制器 (EC) 轻松加以控制。 每个器件版本均提供 7x7 NFBGA 和 9x9 NFBGA 两种封装。 7x7 NFBGA 封装适用于类型 4 印刷电路板 (PCB)，可实现最小电路板面积。 9x9 NFBGA 封装适用于类型 3 和类型 4 PCB 板，可最大限度地降低成本并缩小电路板面积。

6 Pin Configuration and Functions

**168-Pin NFBGA
7x7 ZAJ Package
(Top View)**

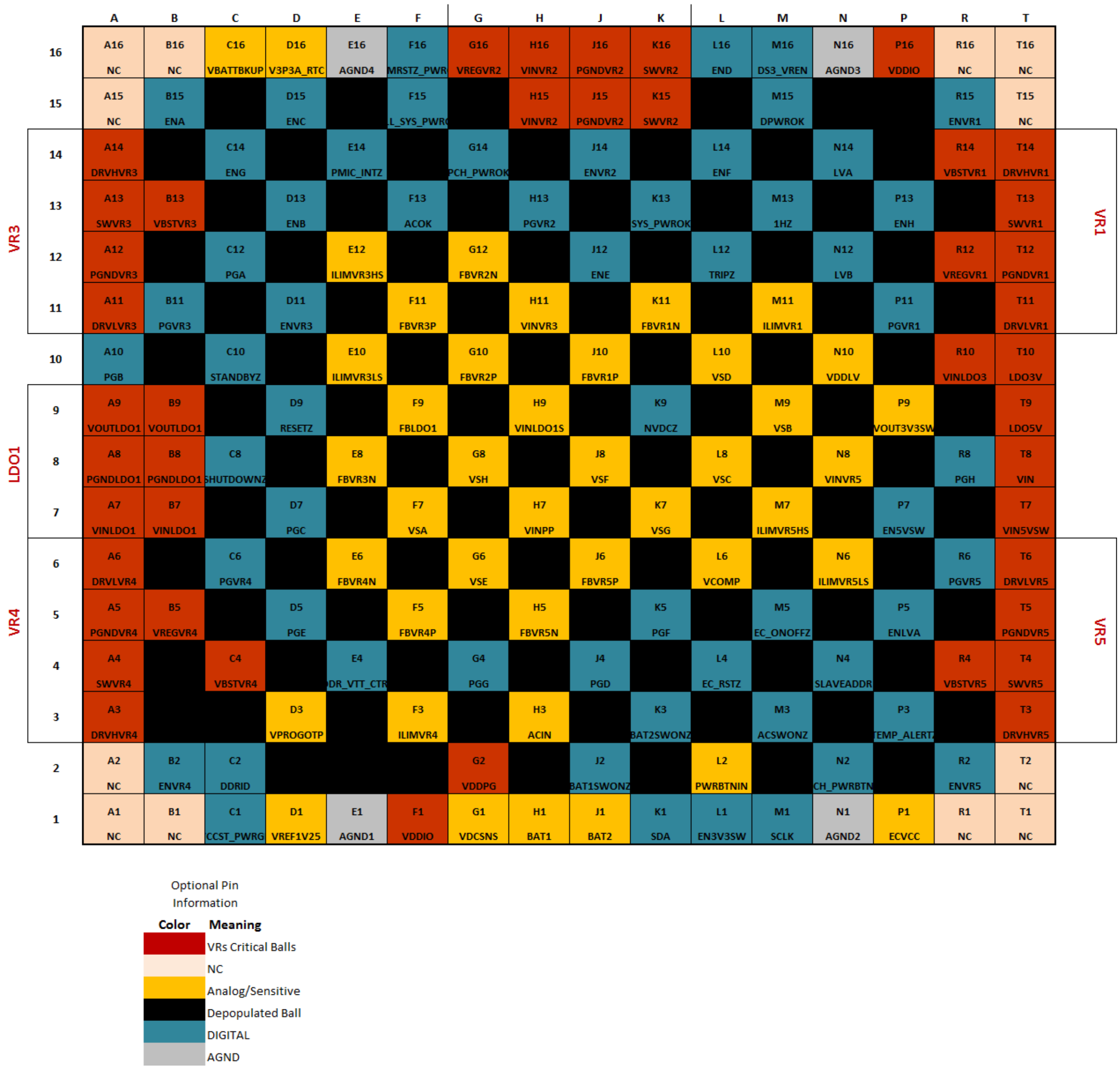
VR1 (rows 12–9, right), VR2 (columns E–H, top), VR3 (rows 12–9, left), LDO1 (rows 8–6, left), VR4 (rows 5–2, left), VR5 (rows 5–2, right)

	A	B	C	D	E	F	G	H	J	K	L	M	N
13	A13 NC	B13 VBATTBKUP	C13 V3P3A_RTC	D13 AGND4	E13 VREGVR2	F13 VINVR2	G13 PGNDVR2	H13 SWVR2	J13 END	K13 DS3_VREN	L13 AGND3	M13 VDDIO	N13 NC
12	A12 DRVHVR3	B12 ENA	C12 ENC	D12 PMIC_INTZ	E12 PGVR2	F12 VINVR2	G12 PGNDVR2	H12 SWVR2	J12 ENF	K12 DPWROK	L12 LVA	M12 ENVR1	N12 DRVHVR1
11	A11 SWVR3	B11 VBSTVR3	C11 ENB	D11 ACOK	E11 PCH_PWROK	F11 ENVR2	G11 ALL_SYS_PWRGD	H11 SYS_PWROK	J11 RSMRSTZ_PWRGD	K11 1HZ	L11 ENH	M11 VBSTVR1	N11 SWVR1
10	A10 PGNDVR3	B10 ENG	C10 FBVR3P	D10 ILIMVR3HS	E10 FBVR2N	F10 ENE	G10 FBVR2P	H10 TRIPZ	J10 VSG	K10 FBVR1P	L10 LVB	M10 VREGVR1	N10 PGNDVR1
9	A9 DRVLVR3	B9 PGVR3	C9 ILIMVR3LS	D9 STANDBYZ	E9 ENVR3	F9 VINLDO1S	G9 VINVR3	H9 NVDCZ	J9 FBVR1N	K9 VSB	L9 ILIMVR1	M9 PGVR1	N9 DRVLVR1
8	A8 VOUTLDO1	B8 VOUTLDO1	C8 RESETZ	D8 FBLDO1	E8 VSF	F8 AGND	G8 AGND	H8 AGND	J8 AGND	K8 VSC	L8 VDDLV	M8 VINLDO3	N8 LDO3V
7	A7 PGNDLDO1	B7 PGNDLDO1	C7 SHUTDOWNZ	D7 FBVR3N	E7 VSA	F7 AGND	G7 AGND	H7 AGND	J7 AGND	K7 AGND	L7 VINVR5	M7 VOUT3V3SW	N7 LDO5V
6	A6 VINLDO1	B6 VINLDO1	C6 PGC	D6 PGA	E6 VSD	F6 AGND	G6 AGND	H6 AGND	J6 AGND	K6 AGND	L6 ENLVA	M6 PGH	N6 VIN
5	A5 DRVLVR4	B5 PGVR4	C5 PGB	D5 FBVR4N	E5 VINPP	F5 VSH	G5 AGND	H5 AGND	J5 AGND	K5 ILIMVR5HS	L5 ILIMVR5LS	M5 EN5VSW	N5 VIN5VSW
4	A4 PGNDVR4	B4 VREGVR4	C4 PGE	D4 DDRID	E4 VCCST_PWRGD	F4 VSE	G4 FBVR5P	H4 PGF	J4 VCOMP	K4 EC_ONOFFZ	L4 FBVR5N	M4 PGVR5	N4 DRVLVR5
3	A3 SWVR4	B3 VBSTVR4	C3 FBVR4P	D3 VPROGOTP	E3 DDR_VTT_CTRL	F3 PGG	G3 VDCSNS	H3 PGD	J3 EC_RSTZ	K3 EN3V3SW	L3 SLAVE ADDR	M3 VBSTVR5	N3 PGNDVR5
2	A2 DRVHVR4		C2 ENVR4	D2 ILIMVR4	E2 ACIN	F2 BAT1SWONZ	G2 BAT2SWONZ	H2 PWRBTNIN	J2 ACSWONZ	K2 PCH_PWRBTNZ	L2 TEMP_ALERTZ	M2 ENVR5	N2 SWVR5
1	A1 NC	B1 VREF1V25	C1 AGND1	D1 VDDPG	E1 VDDIO	F1 BAT1	G1 BAT2	H1 SDA	J1 SCLK	K1 AGND2	L1 ECVCC	M1 DRVHVR5	N1 NC

Optional Pin Information

Color	Meaning
	VRs Critical Balls
	NC
	Analog/Sensitive
	Depopulated Ball
	DIGITAL
	AGND

159-Pin NFBGA
9x9 ZCG Package
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ZAJ PACKAGE NUMBER	ZCG PACKAGE NUMBER		
VBSTVR1	M11	R14	I	VR1 Bootstrap pin
DRVHVR1	N12	T14	O	VR1 High side gate drive output (external power FET)
SWVR1	N11	T13	I	VR1 Switch node connection
DRVLVR1	N9	T11	O	VR1 Low side gate drive output (external power FET)
PGNDVR1	N10	T12	-	VR1 Power GND
FBVR1P	K10	J10	I	VR1 Remote positive feedback sense (Connect to vout of VR1 at output load capacitor)

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	ZAJ PACKAGE NUMBER	ZCG PACKAGE NUMBER		
FBVR1N	J9	K11	I	VR1 Remote negative feedback sense (Connect to GND of VR1 at output load capacitor)
VREGVR1	M10	R12	I	VR1 5V drive supply input (shorted on board with LDO5V), shared with VR5
ILIMVR1	L9	M11	I	VR1 Current limit setting, low-side FET valley current sense
ENVR1	M12	R15	I	VR1 Enable
PGVR1	M9	P11	O	VR1 power good comparator output
VINVR2	F12, F13	H15, H16	I	VR2 Power Input voltage. Connect to a 3.3V voltage regulator, such as V3.3A_DSW
SWVR2	H12, H13	K15, K16	I	VR2 Switch node connection
PGNDVR2	G12, G13	J15, J16	-	VR2 Power GND
FBVR2P	G10	G10	I	VR2 Remote positive feedback sense (Connect to vout of VR2 at output load capacitor)
FBVR2N	E10	G12	I	VR2 Remote negative feedback sense (Connect to GND of VR2 at output load capacitor)
VREGVR2	E13	G16	I	VR2 5V drive supply input (shorted on board with LDO5V)
ENVR2	F11	J14	I	VR2 Enable
PGVR2	E12	H13	O	VR2 Power good comparator output
VBSTVR3	B11	B13	I	VR3 Bootstrap pin
DRVHVR3	A12	A14	O	VR3 High side gate drive output (external power FET)
SWVR3	A11	A13	I	VR3 Switch node connection
DRVLVR3	A9	A11	O	VR3 Low side gate drive output (external power FET)
PGNDVR3	A10	A12	-	VR3 Power GND
FBVR3P	C10	F11	I	VR3 Remote positive feedback sense (Connect to vout of VR3 at output load capacitor)
FBVR3N	D7	E8	I	VR3 Remote negative feedback sense (Connect to GND of VR3 at output load capacitor)
ILIMVR3HS	D10	E12	I	VR3 Current limit setting, high-side FET peak current sense
ILIMVR3LS	C9	E10	I	VR3 Current limit setting, low-side FET valley current sense
VINVR3	G9	H11	I	VR3 Input voltage sense and high-side current-sense kelvin (Connect to drain of high-side FET)
ENVR3	E9	D11	I	VR3 Enable
PGVR3	B9	B11	O	VR3 Power good comparator output
NVDCZ	H9	K9	I	NVDC select [two-level: Low = NVDC, High = non-NVDC]. Connect NVDCZ to GND for NVDC, Connect NVDCZ to LDO3 for non-NVDC
VBSTVR4	B3	C4	I	VR4 Bootstrap pin
DRVHVR4	A2	A3	O	VR4 High side gate drive output (external power FET)
SWVR4	A3	A4	I	VR4 Switch node connection
DRVLVR4	A5	A6	O	VR4 Low side gate drive output (external power FET)
PGNDVR4	A4	A5	-	VR4 Power GND
FBVR4P	C3	F5	I	VR4 Remote positive feedback sense (Connect to vout of VR4 at output load capacitor)
FBVR4N	D5	E6	I	VR4 Remote negative feedback sense (Connect to GND of VR4 at output load capacitor)
VREGVR4	B4	B5	I	VR4 5V drive supply input (shorted on board with LDO5V), shared with VR3

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	ZAJ PACKAGE NUMBER	ZCG PACKAGE NUMBER		
ILIMVR4	D2	F3	I	VR4 Current limit setting, low-side FET valley current sense
ENVR4	C2	B2	I	VR4 Enable
DDRID	D4	C2	I	VR4 Output voltage selection . Low = 1.2V, High = 1.35V, Float = 1.1V
PGVR4	B5	C6	O	VR4 Power good comparator output
VBSTVR5	M3	R4	I	VR5 Bootstrap pin
DRVHVR5	M1	T3	O	VR5 High side gate drive output (external power FET)
SWVR5	N2	T4	I	VR5 Switch node connection
DRVLVR5	N4	T6	O	VR5 Low side gate drive output (external power FET)
PGNDVR5	N3	T5	-	VR5 Power GND
VINVR5	L7	N8	I	VR5 Input voltage sense and high-side current-sense kelvin (Connect to drain of high-side FET)
FBVR5P	G4	J6	I	VR5 Remote positive feedback sense (Connect to vout of VR5 at output load capacitor)
FBVR5N	L4	H5	I	VR5 Remote negative feedback sense (Connect to GND of VR5 at output load capacitor)
ILIMVR5HS	K5	M7	I	VR5 Current limit setting, high-side FET peak current sense
ILIMVR5LS	L5	N6	I	VR5 Current limit setting, low-side FET valley current sense
ENVR5	M2	R2	I	VR5 Enable
PGVR5	M4	B6	O	VR5 Power good comparator output
DDR_VTT_CTRL	E3	E4	I	LDO1 Enable
VINLDO1	A6, B6	A7, B7	I	LDO1 Input supply
VINLDO1S	F9	H9	I	LDO1 Input voltage reference kelvin sense (Connect to vout of VR4 at output load capacitor)
VOUTLDO1	A8, B8	A9, B9	O	LDO1 Output voltage, VOUTLDO1 = (1/2 * VINLDO1SNS)
FBLDO1	D8	F9	I	LDO1 Feedback voltage kelvin sense, (Connect to vout of LDO1 at output load capacitor)
PGNDLDO1	A7, B7	A8, B8	-	LDO1 Power GND
SCLK	J1	M1	I	I2C Clock
SDA	H1	K1	I/O	I2C Data
SLAVEADDR	L3	N4	I	I2C Slave Address select (low = GND = 0x30, high = 3.3V = 0x32, open = float = 0x34) Keep same connection during operation
VDDPG	D1	G2	I	PGx supply, sets output level for PG pins
VSA	E7	F7	I	Power good comparator input and discharge path for external rail
ENA	B12	B15	I	Enable for VSA power good comparator
PGA	D6	C12	O	Power good comparator output, OD or level shifted to VDDLV
VSB	K9	M9	I	Power good comparator input and discharge path for external rail
ENB	C11	D13	I	Enable for VSB power good comparator
PGB	C5	A10	O	Power good comparator output, OD or level shifted to VDDLV
VSC	K8	L8	I	Power good comparator input and discharge path for external rail
ENC	C12	D15	I	Enable for VSC power good comparator

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	ZAJ PACKAGE NUMBER	ZCG PACKAGE NUMBER		
PGC	C6	D7	O	Power good comparator output, OD or level shifted to VDDLV
VSD	E6	L10	I	Power good comparator input and discharge path for external rail
END	J13	L16	I	Enable for VSD power good comparator
PGD	H3	J4	O	Power good comparator output, OD or level shifted to VDDLV
VSE	F4	G6	I	Power good comparator input and discharge path for external rail
ENE	F10	J12	I	Enable for VSE power good comparator
PGE	C4	D5	O	Power good comparator output, OD or level shifted to VDDLV
VSF	E8	J8	I	Power good comparator input and discharge path for external rail
ENF	J12	L14	I	Enable for VSF power good comparator
PGF	H4	K5	O	Power good comparator output, OD or level shifted to VDDLV
VSG	J10	K7	I	Power good comparator input and discharge path for external rail
ENG	B10	C14	I	Enable for VSG power good comparator
PGG	F3	G4	O	Power good comparator output, OD or level shifted to VDDLV
VSH	F5	G8	I	Power good comparator input and discharge path for external rail
VIN5VSW	N5	T7	I	Internal load switch from 5V switching regulator to LDO5 output. Connect VIN5VSW to 5V switching regulator output.
PGH	M6	R8	O	Power good comparator output, OD or level shifted to VDDLV
VDDLV	L8	N10	I	LVx buffer supply, sets output level for PG pins
ENLVA	L6	P5	I	Enable level shifter A Pin not connected electrically. Connect to Ground. (Level Shifter A input is ACOK pin)
LVA	L12	N14	O	Level shifter A open-drain output, used for BC_ACOK output level shifted to EC_VCC. Input is from ACOK pin
LVB	L10	N12	O	Level shifter B push-pull output, level shifted to VDDLV. Input is from ENH pin
EN5VSW	M5	P7	I	Enable Internal load switch from 5V switching regulator to LDO5 output through VIN5VSW. Connect to powergood of 5V switching regulator.
ENH	L11	P13	I	Input to LS B general purpose level shifter.
PWRBTNIN	H2	L2	I	Power button input (internal pull-up to LDO3) (logic low)
PCH_PWRBTNZ	K2	N2	O	Power button signal to PCH (level-shifted DSW domain) (logic low)
EC_ONOFFZ	K4	M5	O	Debounced version of PWRBTNIN (logic low)
1HZ	K11	M13	O	1Hz clock output for waking up embedded controller, EC.
TRIPZ	H10	L12	O	VCOMP comparator push-pull output
VCOMP	J4	L6	I	VCOMP comparator input (Also used for TMODE - > 5.5V)
RSMRSTZ_PWRGD	J11	F16	O	Resume Reset Power Good
ALL_SYS_PWRGD	G11	F15	O	Non-core rails power good
PCH_PWROK	E11	G14	O	Core and Non Core Power Good

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	ZAJ PACKAGE NUMBER	ZCG PACKAGE NUMBER		
SYS_PWROK	H11	K13	O	Delayed ALL_SYS_PWRGD
DPWROK	K12	M15	O	Delayed version of V3.3A_DSW_PG
DS3_VREN	K13	M16	O	DS3 VR enable (enables external power switch)
VCCST_PWRGD	E4	C1	O	VCCST Power Good
EC_RSTZ	J3	L4	O	EC reset (logic low)
ACOK	D11	F13	I	ACOK input
ECVCC	L1	P1	I	EC VCC supply
BAT1	F1	H1	I	Battery 1 voltage sense input
BAT1SWONZ	F2	J2	O	Battery 1 low voltage status (OD) or Battery 1 switch ON (PP, VIN level) (logic low)
BAT2	G1	J1	I	Battery 2 voltage sense input
BAT2SWONZ	G2	K3	O	Battery 2 low voltage status (OD) or Battery 2 switch ON (PP, VIN level) (logic low)
ACIN	E2	H3	I	AC Adaptor voltage sense
ACSWONZ	J2	M3	O	AC adapter low voltage status (OD) or AC adapter switch ON (PP, VIN level) (logic low)
VINPP	E5	H7	I	VIN for Power Path Domain. Connect to external diode OR from: AC, BAT1, BAT2
VDCSNS	G3	G1	I	VDC voltage monitor
PMIC_INTZ	D12	E14	O	PMIC to EC interrupt (logic low)
VBATTBKUP	B13	C16	I	RTC backup battery supply connection
V3P3A_RTC	C13	D16	O	PCH RTC power supply
VIN	N6	T8	I	IC input voltage
VINLDO3	M8	R10	I	LDO3 Iiput supply
AGND1	C1	E1	-	Analog GND1 - tie directly to the ground plane
AGND2	K1	N1	-	Analog GND2 - tie directly to the ground plane
AGND3	L13	N16	-	Analog GND3 - tie directly to the ground plane
AGND4	D13	E16	-	Analog GND4 - tie directly to the ground plane
LDO5V	N7	T9	O	5V internal supply used primarily for the gate drives
LDO3V	N8	T10	O	3.3V LDO used as a reference voltage, and as a pull-up supply.
EN3V3SW	K3	L1	I	Enable for load switch from LDO3V pin to VOUT3V3SW output pin
VOUT3V3SW	M7	P9	O	EC domain load switch output and discharge path from LDO3V
STANDBYZ	D9	C10	I	Set rails in standby (low power mode)
SHUTDOWNZ	C7	C8	I	Set shutdown mode (all supplies off) (logic low)
RESETZ	C8	D9	O	Global disable output for external converters/power tree (logic low)
VDDIO	E1, M13	F1, P16	I	Voltage supply input for I/O buffers. VDDIO should be tied to LDO3 (3.3V)
VREF1V25	B1	D1	O	decoupling cap connection for internal voltage reference
TEMP_ALERTZ	L2	P3	O	Open-drain output of silicon temperature sensor. Input to Power Monitor Unit (connect to PROCHOT# of system). Active low, pull-up to V1.00S with 50ohm
VDD5 VPROGOTP	D3	D3	I	Always connect to LDO5. supply voltage for OTP programming (must be connected to LDO5V in normal operation)

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	ZAJ PACKAGE NUMBER	ZCG PACKAGE NUMBER		
DEPOPULATED BALL - PICK-N-PLACE INDICATOR	B2	C3 (also used for via - see below)	DEPOPULATED BALL	PICK-N-PLACE INDICATOR
NC POPULATED BALL - CORNERS	A1, A13, N1, N13	A1, A2, B1, A15, A16, B16, R16, T16, T15, R1, T1, T2	POPULATED BALL	CORNERS - solder to PCB for mechanical strength
DEPOPULATED BALL - FOR VIAS	No Depopulated Balls for Vias in 7x7. Type 4 PC put micro-vias under each ball pad	B3, B4, B6, B10, B12, B14, C3, C5, C7, C9, C11, C13, C15, D2, D4, D6, D8, D10, D12, D14, E2, E3, E5, E7, E9, E11, E13, E15, F2, F4, F6, F8, F10, F12, F14, G3, G5, G7, G9, G11, G13, G15, H2, H4, H6, H8, H10, H12, H14, J3, J5, J7, J9, J11, J13, K2, K4, K6, K8, K10, K12, K14, L3, L5, L7, L9, L11, L13, L15, M2, M4, M6, M8, M10, M12, M14, N3, N5, N7, N9, N11, N13, N15, P2, P4, P6, P8, P10, P12, P14, P15, R3, R5, R7, R9, R11, R13,	DEPOPULATED BALL	VIA PLACEMENT FOR INTERNAL BALL ROUTES - For Type3 PCBs, put a plated through-hole (PTH) via at each depopulated ball, to connect to the internal row balls.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
CHIP				
Power input pins	VIN, VINLDO3	-0.3	28	V
Analog ground pins	AGND1, AGND2, AGND3, AGND4	-0.3	0.3	V
SWITCHING REGULATORS				
Input pins - controllers	VINVR3, VINVR5	-0.3	28	V
Switch pins - controllers	SWVR1 , SWVR3 , SWVR4 , SWVR5	-1	28	V
High drive pins - controllers	DRVHVR1, DRVHVR3, DRVHVR4, DRVHVR5	-0.3	32	V
Low drive pins - controllers	DRVLVR1, DRVLVR3, DRVLVR4, DRVLVR5	-0.3	7	V
Bootstrap pins - controllers	VBSTVR1, VBSTVR3, VBSTVR4, VBSTVR5	-0.3	32	V
Bootstrap pins - controllers	Differential voltage between VBSTVRx and SWVRx	-0.3	7	V
Input pin - converter	VINVR2	-0.3	3.6	V
Switch pins - converter	SWVR2	-0.3	3.6	V
Power ground pins	PGNDVR1, PGNDVR2, PGNDVR3, PGNDVR4, PGNDVR5	-0.3	0.3	V
Enable pins	ENVR1, ENVR2, ENVR3, ENVR4, ENVR5	-0.3	3.6	V
NVDC select pin	NVDCZ	-0.3	3.6	V
Positive remote feedback pins	FBVR1P, FBVR2P, FBVR3P, FBVR4P	-0.3	3.6	V
Positive remote feedback pin	FBVR5P	-0.3	5.7	V
Negative remote feedback pins	FBVR1N, FBVR2N, FBVR3N, FBVR4N, FBVR5N	-0.3	0.3	V
Gate drive regulator input power pins	VREGVR1 (1_5), VREGVR2, VREGVR4 (3_4)	-0.3	5.7	V
Low-side current limit	ILIMVR1, ILIMVR3LS, ILIMVR4, ILMVR5LS	-0.3	3.6	V
High-side current limit	ILMVR3HS, ILMVR5HS	-0.3	3.6	V
LDO REGULATOR				
Input pin	VINLDO1	-0.3	3.6	V
Output pin	VOUTLDO1	-0.3	3.6	V
Power ground pin	PGNDLDO1	-0.3	0.3	V
Input feedback pin	VINLDO1S	-0.3	3.6	V
Output feedback pin	FBLDO1	-0.3	3.6	V
I2C				
SCLK, SDAT, SLAVEADDR		-0.3	3.6	V
POWERGOOD COMPARATOR LOGIC				
Powergood (push/pull) supply for input pins	VDDPG	-0.3	3.6	V
Powergood input voltage sense pins	VSA, VSB, VSC, VSD, VDE, VSF, VSG, VSH	-0.3	5.7	V
Powergood enable pins	ENA, ENB, ENC, END, ENE, ENF, ENG, ENH	-0.3	3.6	V
Powergood output pins	PGA, PGB, PGC, PGD, PGE, PGF, PGG, PGH, PGVR1, PGVR2, PGVR3, PGVR4, PGVR5	-0.3	3.6	V
POWERGOOD TREE LOGIC				
Open-drain outputs	DPWROK, RSMRSTZ_PWRGD, VCCST_PGOOD, SYS_PWROK, ALL_SYS_PWRGD, PCH_PWROK	-0.3	3.6	V
DDR CONTROL				
Input pins	DDR_VTT_CTRL, DDRID	-0.3	3.6	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Absolute Maximum Ratings (continued)

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
LEVEL SHIFTERS				
Level shifter (push/pull) supply input pin	VDDLV	-0.3	3.6	V
Level shifter enable input pins	ENLVA	-0.3	3.6	V
Level shifter output pins	LVA, LVB	-0.3	3.6	V
POWER PATH LOGIC				
Power path comparator input voltage sense pins	VCOMP, BAT1, BAT2, ACIN	-0.3	7	V
Power path comparator open-drain output pins	BAT1SWONZ, BAT2SWONZ, ACSWONZ	-0.3	28	V
PTC over-temperature comparator open-drain output pin	TRIPZ	-0.3	3.6	V
Power path domain diode OR input pin	VINPP	-0.3	28	V
POWER BUTTON				
PWRBNTIN, PCH_PWRBTNZ, EC_ONOFFZ		-0.3	3.6	V
RESETS				
ECVCC, RESETZ, EC_RSTZ		-0.3	3.6	V
CLOCKS				
EC wake clock: 1HZ		-0.3	3.6	V
POWER MONITOR				
VDCSNS		-0.3	28	V
TEMP_ALERTZ		-0.3	3.6	V
ACOK		-0.3	12	V
REFERENCE				
LDO output pins	LDO5V	-0.3	7	V
LDO output pins	VREF1V25, LDO3V	-0.3	3.6	V
3.3V load switch enable pin	EN3V3SW	-0.3	3.6	V
3.3V load switch output pin	VOUT3V3SW	-0.3	3.6	V
5V load switch enable pin	EN5VSW	-0.3	3.6	V
5V load switch input pin	VIN5VSW	-0.3	7	V
BACKUP BATTERY RTC SELECTOR				
VBATTBKUP, V3P3A_RTC		-0.3	3.6	V
MISC				
Input control pins	STANDBYZ, SHUTDOWNZ	-0.3	3.6	V
Output alert pin	PMIC_INTZ	-0.3	3.6	V
Output DS3 VR enable pin	DS3_VREN	-0.3	3.6	V
Buffers supply input pin	VDDIO	-0.3	3.6	V
VPROGOTP		-0.3	7	V
GENERAL				
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
CHIP			
Power input pins: VIN, VINLDO3	-0.3	21	V
Analog ground pins: AGND1, AGND2, AGND3, AGND4	-0.3	0.3	V
SWITCHING REGULATORS			
Input pins - controllers: VINVR3, VINVR5	-0.3	21	V
Switch pins - controllers: SWVR1 , SWVR3 , SWVR4 , SWVR5	-1	21	V
High drive pins - controllers: DRVHVR1, DRVHVR3, DRVHVR4, DRVHVR5	-0.3	26	V
Low drive pins - controllers: DRVLVR1, DRVLVR3, DRVLVR4, DRVLVR5	-0.3	5	V
Bootstrap pins - controllers: VBSTVR1, VBSTVR3, VBSTVR4, VBSTVR5	-0.3	26	V
Bootstrap pins - controllers: (differential voltage between VBSTVRx and SWVRx):	-0.3	5	V
Input pin - converter: VINVR2	-0.3	3.3	V
Switch pins - Converter: SWVR2	-0.3	3.3	V
Power ground pins: PGNDVR1, PGNDVR2, PGNDVR3, PGNDVR4, PGNDVR5	-0.3	0.3	V
Enable pins: ENVR1, ENVR2, ENVR3, ENVR4, ENVR5	-0.3	3.3	V
NVDC select pin: NVDCZ	-0.3	3.3	V
Positive remote feedback pins: FBVR1P, FBVR2P, FBVR3P, FBVR4P	-0.3	5	V
Positive remote feedback pin: FBVR5P	-0.3	3.3	V
Negative remote feedback pins: FBVR1N, FBVR2N, FBVR3N, FBVR4N, FBVR5N	-0.3	0.3	V
Gate drive regulator input power pins: VREGVR1 (1_5), VREGVR2, VREGVR4 (3_4)	-0.3	5	V
Low-side current limit: ILIMVR1, ILIMVR3LS, ILIMVR4, ILMVR5LS	-0.3	3.3	V
High-side current limit: ILMVR3HS, ILMVR5HS	-0.3	3.3	V
LDO REGULATOR			
Input pin: VINLDO1	-0.3	3.3	V
Output pin: VOUTLDO1	-0.3	1.65	V
Power ground pin: PGNDLDO1	-0.3	0.3	V
Input feedback pin: VINLDO1S	-0.3	3.3	V
Output feedback pin: FBLDO1	-0.3	1.65	V
I2C			
SCLK, SDAT, SLAVEADDR	-0.3	3.3	V
POWERGOOD COMPARATOR LOGIC			
Powergood (push/pull) supply for input pins: VDDPG	-0.3	3.3	V
Powergood input voltage sense pins: VSA, VSB, VSC, VSD, VDE, VSF, VSG, VSH	-0.3	5	V
Powergood enable pins: ENA, ENB, ENC, END, ENE, ENF, ENG, ENH	-0.3	3.3	V
Powergood output pins: PGA, PGB, PGC, PGD, PGE, PGF, PGG, PGH, PGVR1, PGVR2, PGVR3, PGVR4, PGVR5	-0.3	3.3	V
POWERGOOD TREE LOGIC			
Open-drain outputs: DPWROK, RSMRSTZ_PWRGD, VCCST_PGOOD, SYS_PWROK, ALL_SYS_PWRGD, PCH_PWROK	-0.3	3.3	V
DDR CONTROL			
Input pins: DDR_VTT_CTRL, DDRID	-0.3	3.3	V
LEVEL SHIFTERS			
Level shifter (push/pull) supply input pin: VDDLV	-0.3	3.3	V
Level shifter enable input pins: ENLVA	-0.3	3.3	V
Level shifter output pins: LVA, LVB	-0.3	3.3	V

Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
POWER PATH LOGIC			
Power path comparator input voltage sense pins: VCOMP, BAT1, BAT2, ACIN	-0.3	5	V
Power path comparator open-drain output pins: BAT1SWONZ, BAT2SWONZ, ACSWONZ	-0.3	21	V
PTC over-temperature comparator open-drain output pin: TRIPZ	-0.3	3.3	V
Power path domain diode or input pin: VINPP	-0.3	21	V
POWER BUTTON			
PWRBNTIN, PCH_PWRBTNZ, EC_ONOFFZ	-0.3	3.3	V
RESETS			
ECVCC, RESETZ, EC_RSTZ	-0.3	3.3	V
CLOCKS			
EC Wake Clock: 1HZ	-0.3	3.3	V
POWER MONITOR			
VDCSNS	-0.3	21	V
TEMP_ALERTZ	-0.3	3.3	V
ACOK	-0.3	3.3	V
REFERENCE			
LDO output pins: LDO5V	-0.3	5	V
LDO output pins: VREF1V25, LDO3V	-0.3	3.3	V
3.3V load switch enable pin: EN3V3SW	-0.3	3.3	V
3.3V load switch output pin: VOUT3V3SW	-0.3	3.3	V
5V load switch enable pin: EN5VSW	-0.3	3.3	V
5V load switch input pin: VIN5VSW	-0.3	5	V
BACKUP BATTERY RTC SELECTOR			
VBATTBKUP, V3P3A_RTC	-0.3	3.3	V
MISC			
Input control pins: STANDBYZ, SHUTDOWNZ	-0.3	3.3	V
Output alert pin: PMIC_INTZ	-0.3	3.3	V
Output DS3 VR enable pin: DS3_VREN	-0.3	3.3	V
Buffers supply input pin: VDDIO	-0.3	3.3	V
VPROGOTP	-0.3	5	V
GENERAL			
Operating free air temperature, T_A	–40	85	°C
Operating junction temperature, T_J	–40	125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPS650830		UNIT
		ZAJ (168 PINS)	ZCG (159 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.7	34.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.1	15.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	11.8	13.7	
Ψ_{JT}	Junction-to-top characterization parameter	0.3	0.3	
Ψ_{JB}	Junction-to-board characterization parameter	11.7	13.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL						
CONTROL - SYSTEM						
V_{VDC} Parametric	System input voltage	Parametric and functional	5.4	7.4	21	V
V_{VDC} Functional	System input voltage	Functional	5.4	7.4	24	V
I_Q	System quiescent current (includes IDDQ for LDO5V, LDO3V, and VREF1.25V, all registers are default setting)	Measured at VIN = 7.4V		95	150	µA
$V_{UVLO\_5V\_Main}$	System under voltage lockout threshold - All IC functionality including 5VLDO, except LDO3 and internal refsys	V_{VDC} voltage decreasing (falling edge)	4.95	5.1	5.25	V
$V_{Hys\_5V\_Main}$	System under voltage lockout threshold hysteresis	V_{VDC} voltage increasing		200		mV
CONTROL - INTERNAL REFERENCES						
$V_{O(VLDO5)}$	VLDO5 output	VIN = 5.4V - 21V, 10mA load	4.9	5.0	5.1	V
Line regulation $V_{O(LDO5V)}$	Line regulation for regulator over operating voltage range	VIN = 5.4V to 21V, Measured as ($\Delta V_{O(LDO5V)}/V_{O(LDO5V)}$) over this operating range with 40mA load current. measured at VLDO5V pin with respect to AGND pin			0.5%	
Load regulation $V_{O(LDO5V)}$	Load regulation for regulator over operating current range	VIN = 5.4V - 21V Measured as ($\Delta V_{O(LDO5V)}/V_{O(LDO5V)}$) over this operating range with 10mA to 100mA load current. measured at VLDO5V pin with respect to AGND pin			2%	
$I_{SC\ (LDO5V)}$	Over current protection	Measured at 0.9x the regulation voltage	115			mA
$C_{O\ (LDO5V)}$	External output capacitance	Actual capacitance after derating. ex: 2uF capacitance, then use a 4.7uF capacitor with 60% derating. Recommended Part number:	2.7	4.7	10	µF
$V_{O(VREF1V25)}$	VREF1V25 output - Internal buffered bandgap output	See below for output capacitance. measured at VREF1V25 pin with respect to AGND pin	1.244	1.25	1.256	V
$C_{O\ (VREF1V25)}$	External output capacitance	Actual capacitance after derating. ex: 0.2uF capacitance, then use a 0.47uF capacitor with 60% derating. Recommended part number:	0.2	0.22	0.47	µF
$V_{I(LDO3V)}$	LDO3V input	Parametric and functional	5.4	7.4	21	V
$V_{I(LDO3V)}$	LDO3V input	Functional	3.45	7.4	24	V
$V_{O(LDO3V)}$	LDO3V output	VIN = 7.4V, 1mA load	3.267	3.3	3.333	V
$I_{O\ (LDO3V)}$	Output current	Maximum current for external user is limited 40mA			40	mA
$I_{SC\ (LDO3V)}$	Output circuit current limit	Measured at 0.9x VOREG	75			mA
Line regulation $V_{O(LDO3V)}$	Line regulation for regulator over operating voltage range	VIN = 5.4V to 21V, Measured as ($\Delta V_{O(LDO3V)}/V_{O(LDO3V)}$) over the operating range with 20mA load current. measured at VLDO3V pin with respect to AGND pin			0.5%	
Load regulation $V_{O(LDO3V)}$	Load regulation for regulator over operating current range	VIN = 7.4 Measured as ($\Delta V_{O(LDO3V)}/V_{O(LDO3V)}$) over this operating range with 0mA to 50mA load current. measured at VLDO3V pin with respect to AGND pin			0.5%	
$C_{O\ (LDO3V)}$	External output capacitance		2.2	4.7	10	µF
$T_{R\ (LDO3V)}$	Rise time	Measured from 5% to 95% of the output with 2.2µF	300		450	µs

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL - INPUT/ OUTPUT BUFFERS						
CONTROL - DDR_VTT_CTRL (Intel external connection DDR_VTT_CTRL) - 1V logic, tolerates 3V						
$V_{IL\_DDR\_VTT\_CTRL}$	DDR_VTT_CTRL input low voltage	Input low voltage threshold			0.49	V
$V_{IH\_DDR\_VTT\_CTRL}$	DDR_VTT_CTRLL input high voltage	Input high voltage threshold	0.61			V
$V_{HYST\_DDR\_VTT\_CTRL}$	DDR_VTT_CTRLL hysteresis voltage	Hysteresis voltage		70		mV
$I_{leakage\_DDR\_VTT\_CTRL}$	DDR_VTT_CTRL input current	Input current, Clamped to 1.0V		0.01	0.2	μA
CONTROL - INPUT TTL BUFFERS (ALL INPUT PINS), (DEFAULT: SHUTDOWNZ, STANDBYZ, ENLVA, EN3V3SW, EN5VSW, ENVR1, ENVR2, ENVR3, ENVR4, ENVR5, ENA. ENB, ENC, END, ENE, ENF, ENG, ENH), (OPTIONAL: VSA, VSB, VSC, VSD, VSE, VSF, VSG, VSH, ENLVA, ENLVB)						
V_{IL_INPUTS}	Input low voltage				0.4	V
V_{IH_INPUTS}	Input high voltage		1.2			V
V_{HYST_INPUTS}	Hysteresis voltage			300		mV
$I_{leakage\_INPUTS}$	Input current	Clamped on 3.3V		0.01	0.3	μA
$V_{IL\_PWRBTNZ}$	Input low voltage for PWRBTNZ				0.4	V
$V_{IH\_PWRBTNZ}$	Input high voltage for PWRBTNZ	Internal 5kohm pull-up resistor between PWRBTNZ pin and VDDIO	1.6			V
$V_{HYST\_PWRBTNZ}$	Hysteresis voltage for PWRBTNZ			580		mV
$I_{Output\_PWRBTNZ}$	Output current for PWRBTNZ when power button is pressed to close and pulling PWRBTNZ to GND.	PWRBTNZ = GND, Internal 5kohm pull-up resistor between PWRBTNZ pin and VDDIO		660	790	μA
$T_{EC\_ONOFFZ\_DeboUinc\_0e}$	EC_ONOFFZ_Debounce time, 0 setting	Time set to 0 ms, Measured from 0.5% PWBTNZ rising to 5% of the EC_ONOFFZ output		0		ms
$T_{EC\_ONOFFZ\_Deboinc\_30e}$	EC_ONOFFZ_Debounce time, 30 ms setting	Time set to 30 ms, Measured from 0.5% PWBTNZ rising to 5% of the EC_ONOFFZ output		30		ms
CONTROL - PUSH-PULL OUTPUTS (ALL OUTPUT PINS), (DEFAULT: RESETZ, 1HZ, DS3_VREN), (OPTIONAL: PGVR1, PGVR2, PGVR3, PGVR4, PGVR5, PGA, PGB, PGC, PGD, PGE, PGF, PGG, PGH) Pull-Up Rail = VDDIO connect to LDO3 = 3.3V						
V_{PP}	Pull-up output voltage supply	Pulled-Up to VDDIO pin which should by tied to LDO3 pin = 3.3V		VDDIO		V
V_{OL_PP}	Low level output voltage	I_{OL} = 3 mA			0.6	V
V_{OH_PP}	High level output voltage	I_{OH} = 3 mA	VDDIO - 0.6			V
CONTROL - PUSH-PULL OUTPUTS (DEFAULT: LVA, LVB) Pull-Up Rail = VDDLV						
V_{PP_VDDLV}	LV pull-up output voltage supply	Pulled up to VDDLV pin which could by tied to 3.3V or lower		VDDLV		V
$V_{OL\_PP\_LV}$	LV low level output voltage	I_{OL} = 3 mA			0.6	V
$V_{OH\_PP\_LV}$	LV high level output voltage	I_{OH} = 3 mA	VDDLV - 0.6			V
CONTROL - OPEN-DRAIN OUTPUT(ALL OUTPUT PINS), (DEFAULT: ACSWONZ, BAT1SWONZ, BAT2SWONZ, PGVR1, PGVR2, PGVR3, PGVR4, PGVR5, PGA, PGB, PGC, PGD, PGE, PGF, PGG, PGH, VCCST_PWRGD, SYS_PWROK, PCH_PWROK, RSMRSTZ_PWRGD, ALL_SYS_PWRGD, PMIV_INTZ, EC_RSTZ, PCH_PWRBTNZ, EC_ONOFFZ, DPWROK), (OPTIONAL: LVA, LVB)						
V_{OL_OD1}	OD- output voltage	I_{OL} = 2 mA			0.4	V
I_{LK_OD1}	OD leakage current	$V_{(PIN)}$ = 3.3V			0.45	μA

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL - OPEN-DRAIN OUTPUTS (TEMP_ALERT) External pull-up resistor can be 75 ohm to 1V when connected to PROCHOTz of Intel System						
V_{OL_OD}	Open-drain low level output voltage	I_{OL} = 15 mA			0.165	V
I_{LK_OD}	Open-drain leakage current	$V_{(PIN)}$ = 3.3V			0.35	µA
CONTROL - TRISTATE INPUT BUFFER (SLAVEADDR, DDRID)						
$V_{IL\_TRISTATE}$	Low level input voltage	I_{OL} = 6 µA			0.33	V
$V_{IH\_TRISTATE}$	High level input voltage	I_{OH} = 6 µA	1.8			V
$I_{TRISTATE}$	$I_{TRISTATE}$ current	Allowable current when floating	-0.650		0.675	µA
CONTROL - VSA, VSB, VSC, VSD, VSE, VSF, VSG, VSH (ALL LOADSWITCH POWERGOOD COMPARATORS)						
	VSx input voltage range	When VSx configured as voltage sense input	0.7	1.8	5	V
	VSx input leakage current	When VSx configured as voltage sense input, VSx = 5.7V			9	µA
	Power good threshold high VSx	When VSx configured as voltage sense input and powergood window comparator.	106%	108%	110%	
	Power good threshold high VSx hysteresis	When VSx configured as voltage sense input and powergood window comparator.		-3%		
	Power good threshold low VSx	When VSx configured as voltage sense input and powergood window comparator.	90%	92%	94%	
	Power good threshold low VSx hystersis	When VSx configured as voltage sense input and powergood window comparator.		3%		
EMBEDDED CONTROLLER RESET						
V_{OL_OD}	EC_RSTZ output low voltage	I_{OL} = 2mA, V_{EC_RST} = 3.3V			0.4	V
I_{LKG_OD}	EC_RSTZ leakage current	Output buffer in open-drain mode, V_{EC_RST} = 3.3V		0.01	0.2	µA
	EC_RST time duration (Trst)	Reset Timer register value: 00		20		ms
	EC_RST time duration (Trst)	Reset Timer register value: 01		40		ms
	EC_RST time duration (Trst)	Reset Timer register value: 10		80		ms
	EC_RST time duration (Trst) - Default setting	Reset Timer register value: 11		200		ms
I_{LK}	ECVCC input queiscent current				3	µA
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 000	1.344	1.4	1.456	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 001	1.44	1.5	1.56	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 010	1.536	1.6	1.664	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 011	1.632	1.7	1.768	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 100	2.304	2.4	2.496	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 101	2.496	2.6	2.704	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 110	2.688	2.8	2.912	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 111	2.88	3.0	3.12	V

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER PATH COMPARATORS (ACIN, BAT1, BAT2)					
Output low saturation voltage for open-drain logic output pin (TRIPZ)	Comparator input voltage > internal reference voltage. Output pulling low, Sink current = 5mA			0.5	V
IOUT VCOMP- internal current source	Current out of the VCOMP pin when IOUT VCOMP enabled	9.5	10	10.6	µA
VREF_VCOMP_rising, internal reference voltage	Rising voltage at VCOMP pin, changes TRIPZ to logic low	1.211	1.223	1.235	V
VHYST VCOMP_falling, internal hysteresis voltage	Falling voltage at VCOMP pin, changes TRIPZ to logic high		61		mV
Output low saturation voltage for open-drain logic output pin (acswONZ, BAT1SWONZ, BAT2SWONZ)	Comparator input voltage > internal reference voltage. Output pulling low, Sink current = 5mA			0.5	V
ILKG_ACIN_BAT1_BAT2 - Current leakage	Current into the ACIN, BAT1, or BAT2 pins from 5.4V-24V (when pin is below, at, or above 6V internal protection switch.)			0.1	µA
VREF_ACIN_rising - Internal reference voltage	Rising voltage at ACIN pin, makes ACSWONZ trigger low	1.2365	1.25	1.2645	V
VHYST_ACIN_falling - Internal hysteresis voltage	Falling voltage with respect to VREF_ACIN at ACIN pin, makes ACSWONZ trigger high		125		mV
VREF_BAT1_rising - Internal reference voltage	Rising voltage at BAT1 pin, makes BAT1SWONZ trigger low	1.2365	1.25	1.2645	V
VHYST_BAT1_falling - Internal hysteresis voltage	Falling voltage with respect to VREF_BAT1 at BAT1 pin, makes BAT1SWONZ trigger high		125		mV
VREF_BAT2_rising - Internal reference voltage	Rising voltage at BAT2 pin, makes BAT2SWONZ trigger low	1.2365	1.25	1.2645	V
VHYST_BAT2_falling - Internal hysteresis voltage	Falling voltage with respect to VREF_BAT2 at BAT1 pin, makes BAT2SWONZ trigger high		125		mV
Supply voltage (VDCSNS) monitor debounce	Supply voltage monitor register value VDLMTCRT[5:4]: 00		10		µs
Supply voltage(VDCSNS) monitor debounce	Supply voltage monitor register value VDLMTCRT[5:4]: 11		60		µs
Critical supply voltage (VDCSNS) falling threshold	Critical supply voltage threshold register value VDLMTCRT[3:0]: 0001, Supply voltage decreasing. With 2S resistor divider from VDC to VDCSNS with 4R top, R bottom. VDC = 6V when VDCSNS pin = 1.2V.	1.18	1.2	1.22	V
Critical supply voltage (VDCSNS) rising threshold hysteresis	Critical supply voltage hysteresis, Supply voltage increasing. With 2S resistor divider from VDC to VDCSNS with 4R top, R bottom. VDC_hyst = 100mV when VDCSNS_hyst pin = 20mV.		20		mV

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC-ADAPTER DETECTION						
V_{IL}	ACOK input low voltage				0.4	V
V_{IH}	ACOK input high voltage		1.2			V
	ACOK input current	ACOK = 3.3 V		0.01	0.1	μA
	Adapter detection debounce time	ACOKDB register value: 00	50	61	95	μs
	Adapter detection debounce time	ACOKDB register value: 01	7	10	13	ms
	Adapter detection debounce time	ACOKDB register value: 10	15	20	25	ms
	Adapter detection debounce time	ACOKDB register value: 11 default	24	30	36	ms
CONVERTERS						
VR1 POWER						
	Input voltage	Parametric and functional	5.4	7.4	21	V
	Input voltage	Functional	5.4	7.4	24	V
	Output voltage - Default	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V100ACNT[7:6] = 2'b00, V100ACNT[5:4] = 2'b00 (default)		1.05		V
	Output voltage	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V100ACNT[7:6] = 2'b00, V100ACNT[5:4] = 2'b01		1.00		V
	Output voltage	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V100ACNT[7:6] = 2'b00, V100ACNT[5:4] = 2'b10		0.975		V
	Output voltage	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V100ACNT[7:6] = 2'b00, V100ACNT[5:4] = 2'b11		0.950		V
	Output voltage	Power save mode enabled, SLP_S0Z = L , V100ACNT[7:4] = 4'b01XX		0.850		V
	Output voltage	Power save mode enabled, SLP_S0Z = L , V100ACNT[7:4] = 4'b10XX		0.900		V
	Output voltage	Power save mode enabled, SLP_S0Z = L , V100ACNT[7:4] = 4'b11XX		0.950		V
	Low-side output valley current limit (programmed by external resistor)	R_{TRIP} = 10.56kΩ (programmable based on external resistor), RDSON LS FET 7mΩ	7300	9400	12000	mA
	current limit (Vsw - PGND)	V_{TRIP} = 0.8V	-110	-100	-90	mV
	I_{LIM} - Current limit pin source current	T_A 25℃	45	50	55	μA
	TC_{ILIM} - External FET Rdson current limit temperature coefficient	With respect to 25℃		4780		ppm/℃
	V_{ILIM} - Current limit pin setting voltage range	$V_{ILIM} = R_{TRIP} * I_{LIM}$	0.2		2	V
	Maximum line regulation	ULQ/Auto Mode, V_{VIN} = 5.4V to 21V, I_{OUT} = I_{MAX} = 6.810A, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR1P - FBVR1N).	-0.5%		0.5%	
	Maximum load regulation	ULQ/Auto Mode, V_{VIN} = 7.4V, I_{OUT} = 0A to I_{MAX} = 6.810A, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR1P - FBVR1N).	-0.5%		0.61%	

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum total output voltage load transient variation	DC and AC, ULQ/Auto Mode, V_{VIN} = 5.4V to 21V, I_{OUT} = 0A to 70% max load, 70% max load to 0mA and I_{OUT} = 30% max load to max load, max load to 30% max load, di/dt = 2.5A/us	-5%		5%	
VR1_Controller switching frequency (7.4V)	PWM Mode (NVDCZ= 3.3V = programmed to low switching frequency)	379	500	550	kHz
	PWM Mode (NVDCZ= GND = programmed to high switching frequency)	715	800	865	kHz
Start-up time	Delay time from enable to first switching pulse.			150	µs
Output ramp-up tIme	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal).Ssee Cout spec			1000	µs
VR1 MOSFET Drivers					
DRVH resistance	Source, IDRVH = -50mA		3.0	4.5	Ω
DRVH resistance	Sink, IDRVH = 50mA		2.0	3.5	Ω
DRVL resistance	Source, IDRVL = -50mA		3.0	4.5	Ω
DRVL resistance	Sink, IDRVL = 50mA		0.8	2.0	Ω
Dead time	DRVH - off to DRVL - on		10		ns
Dead time	DRVL - off to DRVH - on		20		ns
High-side driver minimum on-time	DRVH - on		80		ns
High-side driver minimum off-time	DRVH - off		260		ns
VR1 OUTPUT DISCHARGE					
Output auto discharge resistance	Discharge register value: 00, Default	1000			kΩ
Output auto discharge resistance	Discharge register value: 01	90	125	160	Ω
Output auto discharge resistance	Discharge register value: 10	170	225	315	Ω
Output auto discharge resistance	Discharge register value: 11	450	550	690	Ω
VR1_Controller Feedback input resistance	Controller enabled		1	2.25	MΩ
VR1_Bootstrap switch ON resistance (Rdson)	$-40 \le T_A \le 125$°C		15	25	Ω
VR1 CONTROL					
VR1_Power good threshold high	Fail when Vout increasing	105.5%	108%	110.5%	
VR1_Power good threshold high hysteresis	Good when Vout decreases (after a PGOOD fail event)		-3%		
VR1_Power good threshold low	Fail when Vout decreasing	89.5%	92%	94.5%	
VR1_Power good threshold low hysteresis	Good when Vout increases (after a PGOOD fail event)		3%		
Overtemperature protection		130	145	160	°C
Overtemperature hysteresis			10		°C
VR2 POWER					
V_{VINVR2} power input voltage - Parametric and functional	V_{VINVR2} voltage range, V_{VIN} = 5.4V to 21V	3.135	3.3	3.465	V
V_{VINVR2} power input voltage - Functional	V_{VINVR2} voltage range, V_{VIN} = 5.4V to 24V	2.97	3.3	3.63	V
Output voltage	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V18ACNT[7:6] = 2'b00, V18ACNT[5:4] = 2'b00		1.854		V

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V18ACNT[7:6] = 2'b00, V18ACNT[5:4] = 2'b01		1.836		V
Output voltage - Default	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V18ACNT[7:6] = 2'b00, V18ACNT[5:4] = 2'b10 (DEFAULT)		1.8		V
Output voltage	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V18ACNT[7:6] = 2'b00, V18ACNT[5:4] = 2'b11		1.764		V
Output voltage	Power save mode enabled, SLP_S0Z = L , V18ACNT[7:4] = 4'b01XX		1.728		V
Output voltage	Power save mode enabled, SLP_S0Z = L , V18ACNT[7:4] = 4'b10XX		1.746		V
Output voltage	Power save mode enabled, SLP_S0Z = L , V18ACNT[7:4] = 4'b11XX		1.764		V
Maximum average output current range	V_{VINVR2} = 2.97V to 3.63V	2500			mA
Ripple current valley positive current limit	V_{VINVR2} = 2.97V to 3.63V	325		1110	mA
Low side valley cycle by cycle positive current limit	V_{VINVR2} = 2.97V to 3.63V	2000		2450	mA
Low side valley cycle by cycle negative current limit	V_{VINVR2} = 2.97V to 3.63V	1400		1875	mA
PFM valley current threshold	V_{VINVR2} = 2.97V to 3.63V	90		125	mA
High side switch on resistance	V_{VINVR2} = 3.3V, 100% duty cycle	30		105	mΩ
Low side switch on resistance	V_{VINVR2} = 3.3V, 0% duty cycle	30		95	mΩ
Maximum line regulation	ULQ/Auto Mode, V_{VINVR2} = 2.97V to 3.63V, I_{OUT} = Imax, ALL VOUTS, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P - FBVR2N).	-0.5%		0.5%	
Maximum load regulation - PWM Mode	ULQ/Auto Mode, V_{VINVR2} = 2.97V to 3.63V, I_{OUT} = 0A to Imax, ALL VOUTS, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P - FBVR2N).	-0.5%		0.5%	
Maximum load regulation - AUTO Mode	ULQ/Auto Mode, V_{VINVR2} =2.97V to 3.63V, I_{OUT} = 0A to Imax, ALL VOUTS, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P - FBVR2N).	-0.65%		1.0%	

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum total output voltage load transient variation	DC and AC, ULQ/Auto Mode, V_{VINVR2} = V2.97V to 3.63V, I_{OUT} = 0A to 70% max load, 70% max load to 0mA, di/dt = 2.5 A/us, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P - FBVR2N).	-5%		5%	
	DC and AC, ULQ/Auto Mode, V_{VINVR2} = 2.97V to 3.63V, I_{OUT} = 30% max load to max load, max load to 30% max load , di/dt = 2.5 A/us, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P - FBVR2N).	-5%		5%	
Switching frequency	PWM Mode, I_{OUT} = 67% of max output current	1700	2000	2300	KHz
Output auto discharge resistance	Discharge register value DISCHGCNT3[7:6]: 00, Default	250	860	1450	kΩ
Output auto discharge resistance	Discharge register value DISCHGCNT3[7:6]: 01	80	100	120	Ω
Output auto discharge resistance	Discharge register value DISCHGCNT3[7:6]: 10	160	200	240	Ω
Output auto discharge resistance	Discharge register value DISCHGCNT3[7:6]: 11	400	500	600	Ω
Feedback input resistance	Enabled			3	MΩ
Quiescent current associated with converter when enabled	I_{Vout} = 0mA, enabled, at T_A=25°C Not switching, Measured at LDO3V, VREGVR2		30	55	µA
VR2 CONTROL					
Power good threshold high	Fail when Vout increasing	106%	108%	110%	
Power good threshold high hysteresis	Good when Vout decreases (after a PGOOD fail event)		-3%		
Power good threshold low	Fail when Vout decreasing	90%	92%	94%	
Power good threshold low hysteresis	Good when Vout increases (after a PGOOD fail event)		3%		
Over temperature protection THOT		120		140	°C
Over temperature hysteresis THOT			10		°C
Over temperature protectionTSHUT		130		160	°C
Over temperature hysteresis TSHUT			10		°C
VR3 POWER					
Input voltage	Parametric and functional	5.4	7.4	21	V
Input voltage	Functional	5.4	7.4	24	V
Output voltage	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V33ADSWCNT[7:6] = 2'b00, V33ADSWCNT[5:4] = 2'b00		3.399		V
Output voltage	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V33ADSWCNT[7:6] = 2'b00, V33ADSWCNT[5:4] = 2'b01		3.366		V

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage - Default	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V33ADSWCNT[7:6] = 2'b00, V33ADSWCNT[5:4] = 2'b10 (DEFAULT)		3.3		V
Output voltage	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V33ADSWCNT[7:6] = 2'b00, V33ADSWCNT[5:4] = 2'b11		3.234		V
Output voltage	Power save mode enabled, SLP_S0Z = L , V33ADSWCNT[7:4] = 4'b01XX		3.168		V
Output voltage	Power save mode enabled, SLP_S0Z = L , V33ADSWCNT[7:4] = 4'b10XX		3.201		V
Output voltage	Power save mode enabled, SLP_S0Z = L , V33ADSWCNT[7:4] = 4'b11XX		3.234		V
High-side output peak current limit (programmed by external resistor)	R_{TRIP} = 25kΩ (programmable based on external resistor), RDSON HS FET 18mΩ	11500	12645	13750	mA
High-side I_{LIM} - current limit pin source current	T_A = 25℃	44	50	56	µA
Current Limit (Vsw - PGND)	V_{TRIP} = 0.8V	-110	-100	-90	mV
High-side TC_{ILIM} - current limit temperature coefficient	With respect to 25℃		3300		ppm/℃
High-side V_{ILIM} - current limit pin setting voltage range	$V_{ILIM} = R_{TRIP}*I_{LIM}$	0.2		2	V
Low-side output valley current limit (programmed by external resistor)	RTRIP = 9.43kΩ (programmable based on external resistor), RDSON LS FET 7mΩ	6400	8420	10500	mA
I_{LIM} - current limit pin source current	T_A = 25℃	45	50	55	µA
Low-side TC_{ILIM} - current limit temperature coefficient	With respect to 25℃		4780		ppm/℃
V_{ILIM} - current limit pin setting voltage range	$V_{ILIM} = R_{TRIP}*I_{LIM}$	0.2		2	V
Maximum range low side zero crossing threshold		-10		10	mV
Maximum line regulation	ULQ/Auto Mode, V_{VIN} = 5.4V to 21V, $I_{OUT} = I_{MAX}$, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR3P - FBVR3N).	-0.5%		0.65%	
Maximum load regulation	ULQ/Auto Mode, V_{VIN} = 7.4V, I_{OUT} = 0A to I_{MAX} , Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR3P - FBVR3N).	-0.5%		0.55%	
Maximum total output voltage load transient variation	DC and AC, ULQ/Auto Mode, V_{VIN} = 5.4V to 21V, I_{OUT} = 0A to 70% max load, 70% max load to 0mA and I_{OUT} = 30% max load to max load, max load to 30% max load, di/dt = 2.5A/us , Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR3P - FBVR3N).	-5%		5%	

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VR3_Controller switching frequency	PWM Mode (NVDCZ= 3.3V = programmed to low switching frequency)	430	500	550	kHz
	PWM Mode (NVDCZ= GND = programmed to high switching frequency)	715	800	865	kHz
Total turn-on time (start-up time + output ramp-up time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal). see Cout spec			1200	µs
VR3 MOSFET Drivers					
DRVH resistance	Source, IDRVH = -50mA		3.0	4.5	Ω
DRVH resistance	Sink, IDRVH = 50mA		2.0	3.5	Ω
DRVL resistance	Source, IDRVL = -50mA		3.0	4.5	Ω
DRVL resistance	Sink, IDRVL = 50mA		0.8	2.0	Ω
Dead time	DRVH - off to DRVL - on		10		ns
Dead time	DRVL - off to DRVH - on		20		ns
High-side driver minimum on-time	DRVH - on		80		ns
High-side driver minimum off-time	DRVH - off		260		ns
VR3 OUTPUT DISCHARGE					
Output auto discharge resistance	Discharge register value: 00, Default	1000			kΩ
Output auto discharge resistance	Discharge register value: 01	90	125	160	Ω
Output auto discharge resistance	Discharge register value: 10	170	225	315	Ω
Output auto discharge resistance	Discharge register value: 11	450	550	690	Ω
VR3_Controller feedback input resistance	Controller enabled		1	2.25	MΩ
VR3_Bootstrap switch ON resistance (Rdson)	T_A = 25°C			20	Ω
VR3_Controller HSD leakage	V_{IN} = 7.4 V, Controller disabled			1.55	µA
VR3 CONTROL					
VR3_Power good threshold high	Fail when Vout increasing	105.5%	108%	110.5%	
VR3_Power good threshold high hysteresis	Good when Vout decreases (after a PGOOD fail event)		-3%		
VR3_Power good threshold low	Fail when Vout decreasing	89.5%	92%	94.5%	
VR3_Power good threshold low hysteresis	Good when Vout increases (after a PGOOD fail event)		3%		
Overtemperature protection		130	145	160	°C
Overtemperature hysteresis			10		°C
VR4 POWER					
Input voltage	Parametric and functional	5.4	7.4	21	V
Input voltage	Functional	5.4	7.4	24	V
Output voltage	Power save mode disabled, Output voltage select register value: 000 DDRID = 0V		1.236		V
Output voltage	Power save mode disabled, Output voltage select register value: 001 DDRID = 0V		1.224		V
Output voltage	Power save mode disabled, Output voltage select register value: 010 DDRID = 0V		1.212		V
Output voltage	Power save mode disabled, Output voltage select register value: 011, default DDRID = 0V		1.200		V

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	Power save mode disabled, Output voltage select register value: 100 DDRID = 0V		1.188		V
Output voltage	Power save mode disabled, Output voltage select register value: 101 DDRID = 0V		1.176		V
Output voltage	Power save mode disabled, Output voltage select register value: 110 DDRID = 0V		1.164		V
Output voltage	Power save mode disabled, Output voltage select register value: 111 DDRID = 0V		1.152		V
Output voltage	Power save mode disabled, Output voltage select register value: 000 DDRID = 3.3V		1.391		V
Output voltage	Power save mode disabled, Output voltage select register value: 001 DDRID = 3.3V		1.377		V
Output voltage	Power save mode disabled, Output voltage select register value: 010 DDRID = 3.3V		1.364		V
Output voltage	Power save mode disabled, Output voltage select register value: 011 DDRID = 3.3V		1.35		V
Output voltage	Power save mode disabled, Output voltage select register value: 100, default DDRID = 3.3V		1.337		V
Output voltage	Power save mode disabled, Output voltage select register value: 101, default DDRID = 3.3V		1.323		V
Output voltage	Power save mode disabled, Output voltage select register value: 110 DDRID = 3.3V		1.310		V
Output voltage	Power save mode disabled, Output voltage select register value: 111 DDRID = 3.3V		1.296		V
Output voltage	Power save mode disabled, Output voltage select register value: 000 DDRID = Open		1.082		V
Output voltage	Power save mode disabled, Output voltage select register value: 001 DDRID = Open		1.133		V
Output voltage	Power save mode disabled, Output voltage select register value: 010 DDRID = Open		1.111		V
Output voltage	Power save mode disabled, Output voltage select register value: 011 DDRID = Open		1.1		V
Output voltage	Power save mode disabled, Output voltage select register value: 100, default DDRID = Open		1.089		V
Output voltage	Power save mode disabled, Output voltage select register value: 101, default DDRID = Open		1.078		V

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	Power save mode disabled, Output voltage select register value: 110 DDRID = Open		1.067		V
Output voltage	Power save mode disabled, Output voltage select register value: 111 DDRID = Open		1.056		V
Low-side output valley current limit (programmed by external resistor)	R_{TRIP} = 10.7kΩ (Programmable based on external resistor), RDSON LS FET 7mΩ	7300	9550	12000	mA
Current limit (Vsw - PGND)	V_{TRIP} = 0.8V	-110	-100	-90	mV
I_{LIM} - current limit pin source current	T_A = 25℃	45	50	55	µA
Low-side TC_{LIM} - current limit temperature coefficient	With respect to 25℃		4780		ppm/℃
V_{ILIM} - current limit pin setting voltage range	$V_{ILIM} = R_{TRIP} * I_{LIM}$	0.2		2	V
Maximum line regulation	ULQ/Auto Mode, V_{VIN} = 5.4V to 21V, I_{OUT} = I_{MAX} =7.5A, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR4P - FBVR4N).	-0.5%		0.5%	
Maximum load regulation	ULQ/Auto Mode, V_{VIN} = 7.4V, I_{OUT} = 0A to I_{MAX} =7.5A, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR4P - FBVR4N).	-0.5%		0.65%	
Maximum total output voltage load transient variation	DC and AC, ULQ/Auto Mode, V_{VIN} = 5.4V to 21V, I_{OUT} = 0A to 70% max load, 70% max load to 0mA and I_{OUT} = 30% max load to max load, max load to 30% max load, di/dt = 2.5A/us , Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR4P - FBVR4N).	-5%		5%	
VR4_Controller switching frequency	PWM Mode (NVDCZ= 3.3V = programmed to low switching frequency)	430	500	550	kHz
	PWM Mode (NVDCZ= GND = programmed to high switching frequency)	715	800	865	kHz
Start-up time	Time to start switching from enable. See Cout spec			200	µs
Total turn-on time (start-up time + output ramp-up time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal). see Cout spec	300		1025	µs

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VR4 MOSFET DRIVERS					
DRVH resistance	Source, IDRVH = -50mA		3.0	4.5	Ω
DRVH resistance	Sink, IDRVH = 50mA		2.0	3.5	Ω
DRVL resistance	Source, IDRVL = -50mA		3.0	4.5	Ω
DRVL resistance	Sink, IDRVL = 50mA		0.8	2.0	Ω
Dead time	DRVH - off to DRVL - on		10		ns
Dead time	DRVL - off to DRVH - on		20		ns
High-side driver minimum on-time	DRVH - on		80		ns
High-side driver minimum off-time	DRVH - off		260		ns
VR4 OUTPUT DISCHARGE					
Output auto discharge resistance	Discharge register value: 00, Default	1000			kΩ
Output auto discharge resistance	Discharge register value: 01	90	100	160	Ω
Output auto discharge resistance	Discharge register value: 10	170	225	315	Ω
Output auto discharge resistance	Discharge register value: 11	450	550	690	Ω
VR4_Controller feedback input resistance	V10 controller enabled		1	2.25	MΩ
VR4_Bootstrap switch ON resistance (Rdson)	T_A = 25°C			20	Ω
VR4 CONTROL					
VR4_Power good threshold high	Fail when Vout increasing	105.5%	108%	110.5%	
VR4_Power good threshold high hysteresis	Good when Vout decreases (after a PGOOD fail event)		-3%		
VR4_Power good threshold low	Fail when Vout decreasing	89.5%	92%	94.5%	
VR4_Power good threshold low hysteresis	Good when Vout increases (after a PGOOD fail event)		3%		
Overtemperature protection		130	145	160	°C
Overtemperature hysteresis			10		°C
LDO1 POWER					
Input voltage	DDRID = 0V		1.2		V
Output voltage	DDRID = 0V, VOUTLDO1 = (VINLDO1S) / 2		0.6		V
Input voltage	DDRID = 3.3V		1.35		V
Output voltage	DDRID = 3.3V, VOUTLDO1 = (VINLDO1S) / 2		0.675		V
Input voltage	DDRID = Open		1.1		V
Output voltage	DDRID = Open, VOUTLDO1 = (VINLDO1S)/ 2		0.55		V
Output voltage tolerance - AC and DC transient load	I_{OUT} ≤ 10 mA, 1.1V ≤ VINLDO1 ≤ 1.35V, Output voltage relative to VINLDO1S / 2, where VINLDO1S = FBVR4 = FBV10, Load transient from 0mA to 70%*10mA, dI/dt = 2.5 A/us	-20		20	mV
	I_{OUT} ≤ 1 A, 1.1V ≤ VINLDO1 ≤ 1.35V, VOUTLDO1 = Output voltage relative to VINLDO1S / 2, where VINDO1S = FBVR4 = FBV10, Load transient from 0mA to 70%*1A, dI/dt = 2.5 A/us	-30		30	mV
Leakage current	T_A = 25°C, VIN13 = 1.2V, Disabled			5	µA
Bias current at VIN13_SENSE	T_A = 25°C Bias current measured when VINLDO13 is at 1.2V			40	µA

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO1 source current limit	Max current from LDO without exceeding load regulation	1000			mA
Sink current limit	Max current sinked into LDO without exceeding load regulation (raise output voltage above programmed value to sink current into LDO)	1000			mA
Source short circuit current limit	Measured with VOUT at 0.9*Programmed voltage	2000			mA
Sink short circuit current limit		2000			mA
Maximum load regulation	V_{VIN} = 1.1V, 1.2V and 1.35V, I_{OUT} = 0A to 1.0A, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBLDO1 - FBVR4N).			4.5%	
Maximum total output voltage variation	DC and AC, V_{VIN} = 1.0V to 1.42V, I_{OUT} = 0A to 1.0A, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBLDO1 - FBVR4N).			5%	
Total turn-on time (enable + ramp)	Measure from LDO enable to V_{OUT} stable. Time to ramp from 0.3V to $V_{O(min)}$. Continuous slope (no slope reversal). Assumes V_{VIN} is present, with a 4x10µF output capacitor bank			35	µs
External output capacitor (Cout)		40			µF
External input capacitor (Cin)		10			µF
Output auto discharge resistance	Discharge register value: 0, Default	1000			kΩ
Output auto discharge resistance	Discharge register value: 1	60	80	100	Ω
FBLDO1 input impedance	Enabled	20	25		MΩ
Quiescent current into $V_{VINLDO1}$	$V_{VINLDO1}$ = 1.35V, I_{LDO1} = 0 mA, Enabled		3.5	5	µA
Quiescent current from 3.3V reference LDO when LDO1 is enabled	$V_{VINLDO1}$ = 1.35V, Enabled			250	µA
LDO1 CONTROL					
LDO1_Power good threshold high	Fail when V_{OUT} increasing	108%	110%	112%	
LDO1_Power good threshold high hysteresis	Good when V_{OUT} decreases (after a PGOOD fail event)		-5%		
LDO1_Power good threshold low	Fail when V_{OUT} decreasing	88%	90%	92%	
LDO1_Power good threshold low hysteresis	Good when V_{OUT} increases (after a PGOOD fail event)		5%		
Overtemperature protection		130	145	160	°C
Overtemperature hysteresis			10		°C
VR5 POWER					
Input voltage	Parametric and functional	5.4	7.4	21	V
Input voltage	Functional	5.4	7.4	24	V
Output voltage	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V5ADS3CNT[7:6] = 2'b00, V5ADS3CNT[5:4] = 2'b00		5.15		V
Output voltage	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V5ADS3CNT[7:6] = 2'b00, V5ADS3CNT[5:4] = 2'b01		5.1		V

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage- Default	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V5ADS3CNT[7:6] = 2'b00, V5ADS3CNT[5:4] = 2'b10 (DEFAULT)		5.0		V
Output voltage	Power save mode disabled (SLPS0Z = H, or SLPS0Z = L & , V5ADS3CNT[7:6] = 2'b00, V5ADS3CNT[5:4] = 2'b11		4.9		V
Output voltage	Power save mode enabled, SLP_S0Z = L , V5ADS3CNT[7:4] = 4'b01XX		4.8		V
Output voltage	Power save mode enabled, SLP_S0Z = L , V5ADS3CNT[7:4] = 4'b10XX		4.85		V
Output voltage	Power save mode enabled, SLP_S0Z = L , V5ADS3CNT[7:4] = 4'b11XX		4.9		V
High-side output peak current limit (programmed by external resistor)	R_{TRIP} = 13.1kΩ (programmable based on external resistor), RDSON HS FET 18mΩ	6600	7245	7900	mA
current limit (Vsw - PGND)	V_{TRIP} = 0.8V	-110	-100	-90	mV
High-side I_{LIM} - current limit pin source current	T_A = 25℃	44	50	56	µA
High-side TC_{ILIM} - current limit temperature coefficient	With respect to 25℃		3300		ppm/℃
High-side V_{ILIM} - current limit pin setting voltage range	$V_{ILIM} = R_{TRIP} * I_{LIM}$	0.2		2	V
Low-side output valley current limit (programmed by external resistor)	R_{TRIP} = 5kΩ (programmable based on external resistor), RDSON LS FET 7mΩ	3350	4465	5600	mA
I_{LIM} - current limit pin source current	T_A = 25℃	45	50	55	µA
Low-side TC_{ILIM} - current limit temperature coefficient	With respect to 25℃		4780		ppm/℃
V_{ILIM} - current limit pin setting voltage range	$V_{ILIM} = R_{TRIP} * I_{LIM}$	0.2		2	V
Maximum range low side zero crossing threshold		-10		10	mV
Maximum line regulation	ULQ/Auto Mode, V_{VIN} = 5.4V to 21V, $I_{OUT} = I_{MAX}$, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR5P - FBVR5N).	-0.5%		1.05%	
Maximum load regulation	ULQ/Auto Mode, V_{VIN} = 7.4V, I_{OUT} = 0A to I_{MAX}, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR5P - FBVR5N).	-0.5%		0.75%	
Maximum total output voltage load transient variation	DC and AC, ULQ/Auto Mode, V_{VIN} = 5.7V to 21V (when Vout=5V), V_{VIN} = 5.4V to 21V (when Vout=1.8V), I_{OUT} = 0A to 70% max load, 70% max load to 0mA and I_{OUT} = 30% max load to max load, max load to 30% max load, di/dt = 2.5A/us , Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR5P - FBVR5N).	-5%		5%	

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VR5_Controller switching frequency	PWM Mode (NVDCZ= 3.3V = programmed to low switching frequency)	430	500	550	kHz
		PWM Mode (NVDCZ= GND = programmed to high switching frequency)Frequency drops at Vin < 6V close to Vout = 5V to extend Ton	25	875	925	
	Total turn-on time (start-up time + output ramp-up time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal). See Cout spec			1200	µs
VR5 MOSFET Drivers						
	DRVH resistance	Source, IDRVH = -50mA		3.0	4.5	Ω
	DRVH resistance	Sink, IDRVH = 50mA		2.0	3.5	Ω
	DRVL resistance	Source, IDRVL = -50mA		3.0	4.5	Ω
	DRVL resistance	Sink, IDRVL = 50mA		0.8	2.0	Ω
	Dead time	DRVH - off to DRVL - on		10		ns
	Dead time	DRVL - off to DRVH - on		20		ns
	High-side driver minimum on-time	DRVH - on		80		ns
	High-side driver minimum off-time	DRVH - off		260		ns
VR5 OUTPUT DISCHARGE						
	Output auto discharge resistance	Discharge register value: 00, Default	1000			kΩ
	Output auto discharge resistance	Discharge register value: 01	90	150	190	Ω
	Output auto discharge resistance	Discharge register value: 10	170	250	315	Ω
	Output auto discharge resistance	Discharge register value: 11	450	575	690	Ω
	VR5_Controller Feedback input resistance	Controller enabled		2.5	4.25	MΩ
	VR5_Bootstrap switch ON resistance (Rdson)	T_A = 25°C			20	Ω
	VR5_Controller HSD leakage	V_{IN} = 7.4 V, Controller disabled			1.55	µA
VR5 CONTROL						
	VR5_Power good threshold high	Fail when Vout increasing	105.5%	108%	110.5%	
	VR5_Power good threshold high hysteresis	Good when Vout decreases (after a PGOOD fail event)		-3%		
	VR5_Power good threshold low	Fail when Vout decreasing	89.5%	92%	94.5%	
	VR5_Power good threshold low hysteresis	Good when Vout increases (after a PGOOD fail event)		3%		
	Overtemperature protection		130	145	160	°C
	Overtemperature hysteresis			10		°C
INPUT POWER SOURCE DETECTION						
AC-ADAPTER DETECTION						
V_{IL}	ACOK input low voltage				0.4	V
V_{IH}	ACOK input high voltage		1.2			V
	ACOK input current	ACOK = 3.3 V		0.01	0.1	µA
	Adapter detection debounce time	ACOKDB register value: 00	50	61	95	µs
	Adapter detection debounce time	ACOKDB register value: 01	7	10	13	ms
	Adapter detection debounce time	ACOKDB register value: 10	15	20	25	ms
	Adapter detection debounce time	ACOKDB register value: 11 Default	24	30	36	ms

Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARACTER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER MONITORING						
1 Hz CLOCK						
1Hz EC CLOCK - pulled-0-up to EC_VCC Internal Pull-up Rail = EC_VCC = 1.8V or 3.3V						
	Clock frequency		0.8	1	1.2	Hz
	Duty cycle			50%		
V_{PP}	Pull-up output voltage supply	Pulled-Up to EC_VCC pin which should be tied to 3.3v LDO3 pin, can also have EC_VCC pull-up to 1.8V, instead of 3.3V		EC_ VCC		V
V_{OL_PP}	Low level output voltage	I_{OL} = 3 mA			0.66	V
V_{OH_PP}	High level output voltage	I_{OH} = 3 mA	EC_VC C - 0.66			V
COINCELL SELECTOR						
V_{3v1LDO}	3V1 LDO regulation voltage	VDCIN > UVLO, 3.3V and 5V LDOs up , Measured at the V3P3A_RTC pin with respect to AGND.. Place a 1µF capacitor at V3P3A_RTC. (Do not exceed 2uF capacitance).	3.0	3.1	3.2	V
I_{3v1LDO}	Maximum 3V1 LDO output current	Maximum output current out of 3V3RTC.			1	mA
$I_{Q\_bkup\_no\_Vsys}$	VBATTBKUP quiescent current, when no adapter and no main battery connected to system, automatically VBATTBKUP internally selected. internal 3.1V LDO automatically off	V_{VDC} < UVLO, V_{BBC} = 2.0V to 3.0V, V_{VDC} = 0V		0.03	0.45	µA
$I_{Q\_bkup\_with\_Vsys}$	VBATTBKUP quiescent current, when adapter or main battery connected to system, automatically VBATTBKUP internally not selected, internal 3.1V LDO automatically on and selected.	V_{VDC} > UVLO, V_{BBC} = 2.0V to 3.0V, V_{VDC} = 7.4V		0.15	0.85	µA
R_{ext_bkup}	External resistor in series with backup battery	Place between backup battery and VBATTBKUP pin, for limiting current out of backup battery		1		kΩ
I2C INTERFACE(1)						
V_{IL}	SDA, SCL input low voltage				0.4	V
V_{IH}	SDA, SCL input high voltage		1.2			V
	SDA, SCL input current	Clamped on 3.3V		0.01	0.3	µA
	SDA output low voltage	I_{SDA} = 5mA (using a 354Ω or larger external pull-up resistor)		0.04	0.4	V
C_b	Capacitive load for SDA and SCL				400	pF

(1) All values referred to V_{IH} min and V_{IH} max levels.

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I2C INTERFACE						
$f_{(SCL)}$	SCL clock frequency	Standard-mode			100	kHz
		Fast-mode			400	
		Fast-mode Plus			1000	
t_{BUF}	Bus free time between a STOP and START condition	Standard-mode	4.7			µs
		Fast-mode	1.3			
		Fast-mode Plus	0.5			
$t_{HD;\ STA}$	Hold time (repeated) START condition	Standard-mode	4			µs
		Fast-mode	600			ns
		Fast-mode Plus	260			ns
$t_{SU;\ STA}$	Setup time for a repeated START condition	Standard-mode	4.7			µs
		Fast-mode	600			ns
		Fast-mode Plus	260			ns
$t_{SU;\ DAT}$	Data setup time	Standard-mode	250			ns
		Fast-mode	100			
		Fast-mode Plus	50			
$t_{HD;\ DAT}$	Data hold time	Standard-mode	0		3.45	µs
		Fast-mode	0		0.9	µs
		Fast-mode Plus	0			ns
t_{rCL}	Rise time of SCL signal	Standard-mode			1000	ns
		Fast-mode	20		300	
		Fast-mode Plus			120	
t_{rDA}	Rise time of SDA signal	Standard-mode (using a 2.95KΩ or smaller external pull-up resistor)			1000	ns
		Fast-mode (using an 885Ω or smaller external pull-up resistor)	20		300	
		Fast-mode Plus (using a 354Ω or smaller external pull-up resistor)			120	
t_{fDA}	Fall time of SDA signal	Standard-mode			300	ns
		Fast-mode	20 x (V_{DD} / 5.5 V)		300	
		Fast-mode Plus	20 x (V_{DD} / 5.5 V)		120	
$t_{SU;\ STO}$	Setup time for STOP condition	Standard-mode	4			µs
		Fast-mode	600			ns
		Fast-mode Plus	260			ns

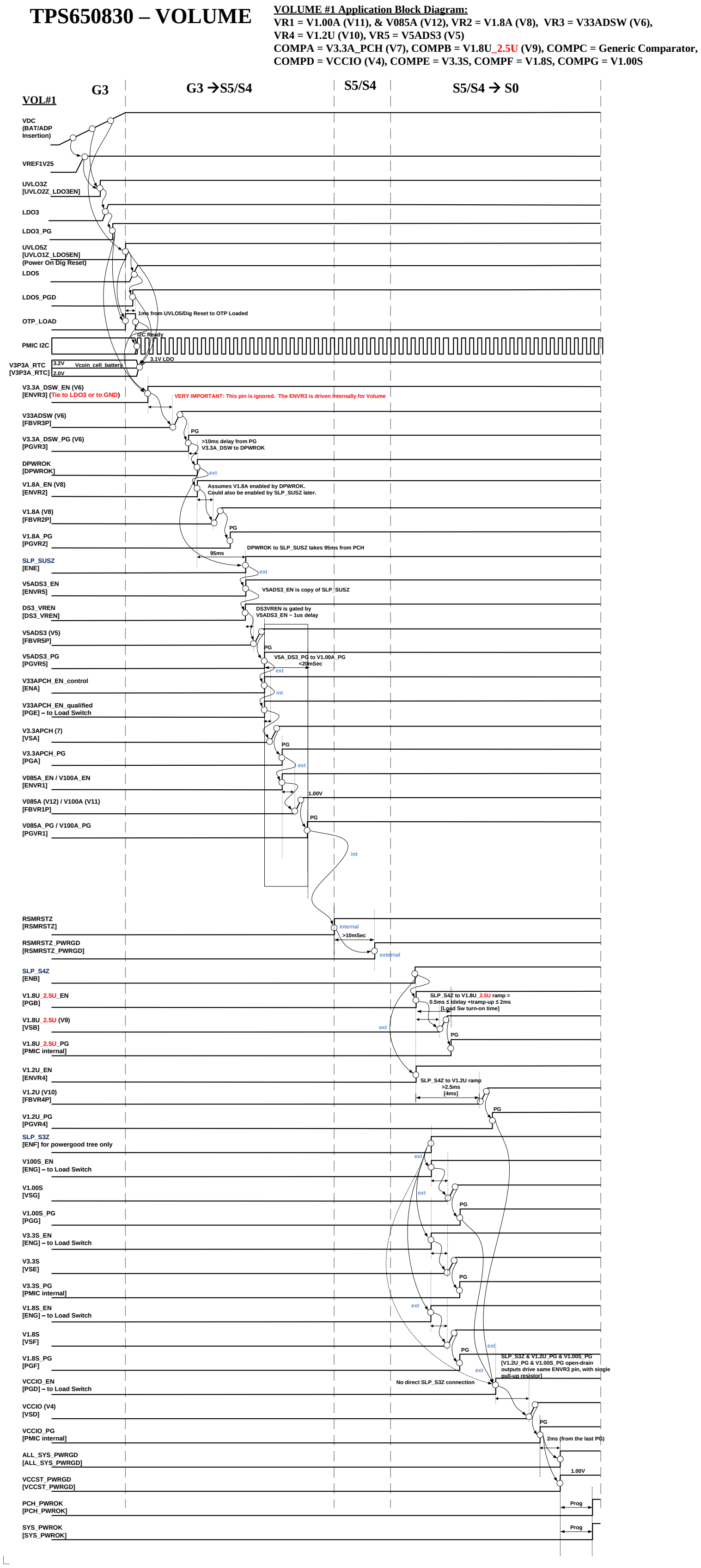


Figure 1. TPS650830 Volume Timing Diagram

7.7 Typical Characteristics

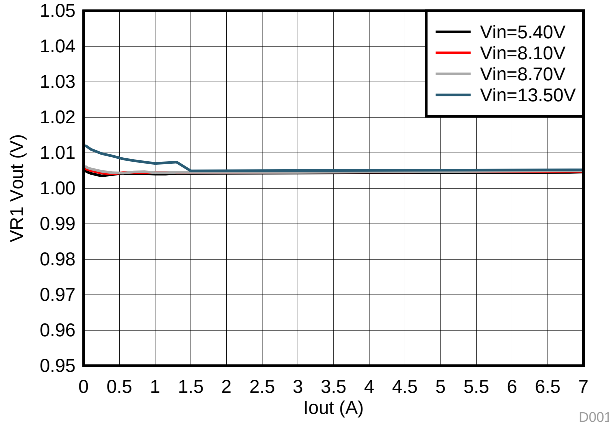


Figure 2. VR1 Output Voltage Load Regulation, NVDC

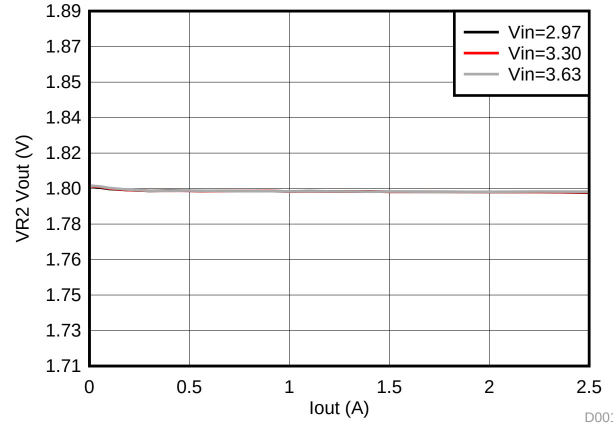


Figure 3. VR2 Output Voltage Load Regulation, NVDC

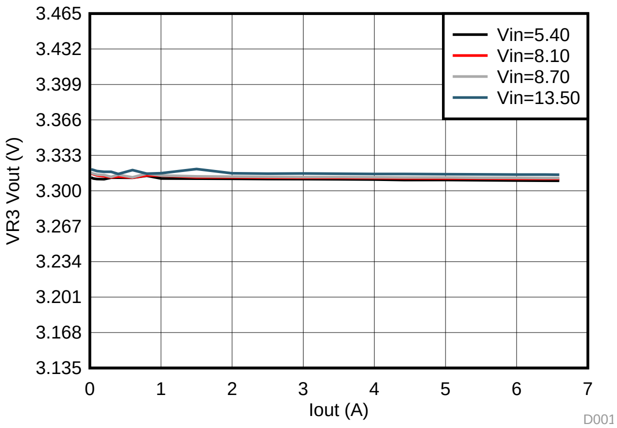


Figure 4. VR3 Output Voltage Load Regulation, NVDC

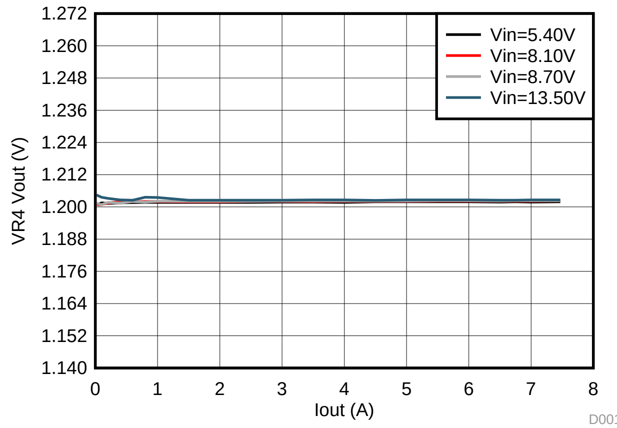


Figure 5. VR4 Output Voltage Load Regulation, NVDC

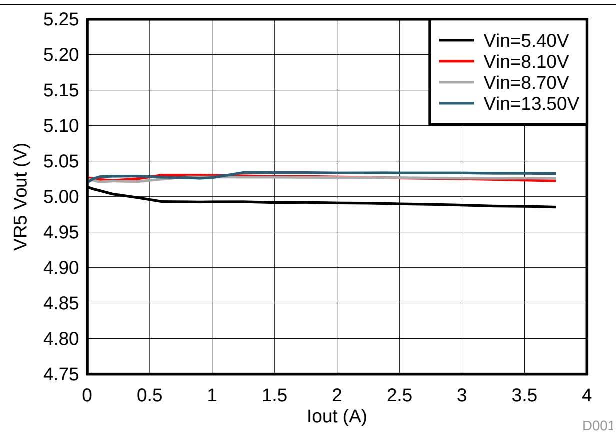


Figure 6. VR5 Output Voltage Load Regulation, NVDC

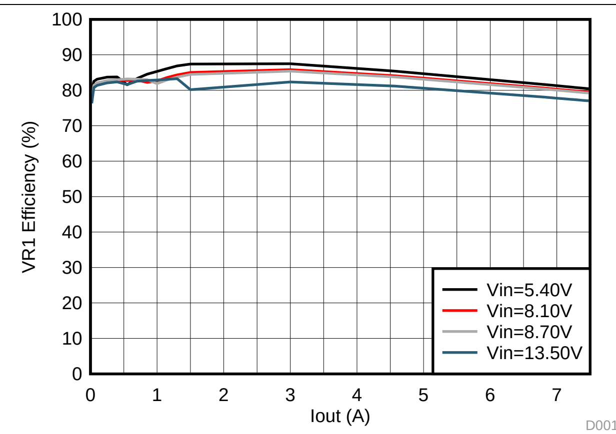


Figure 7. VR1 Efficiency vs Load, NVDC

Typical Characteristics (continued)

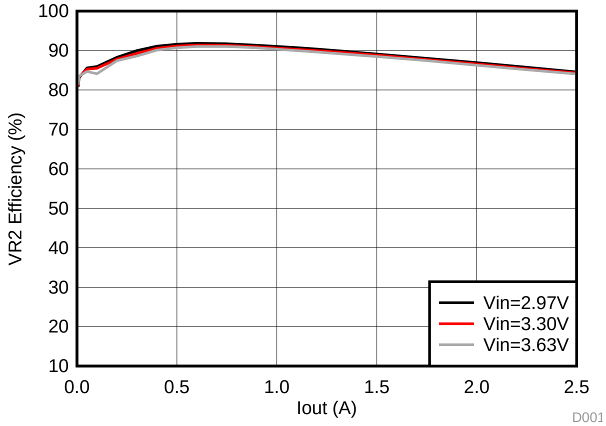


Figure 8. VR2 Efficiency vs Load, NVDC

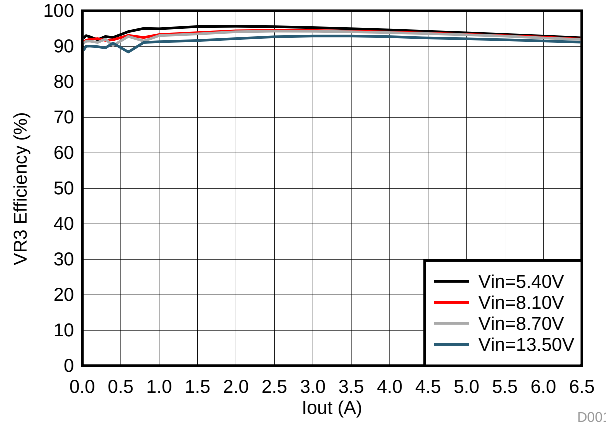


Figure 9. VR3 Efficiency vs Load, NVDC

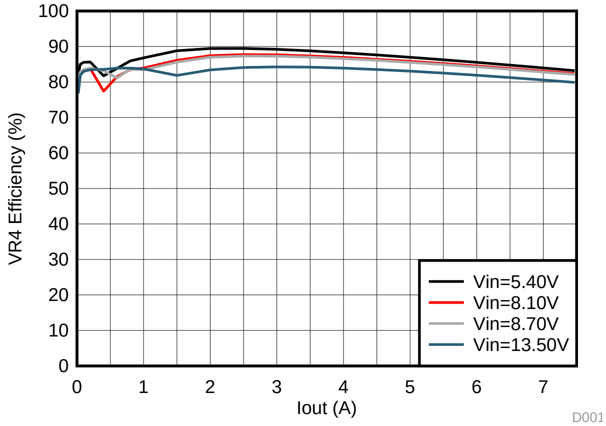


Figure 10. VR4 Efficiency vs Load, NVDC

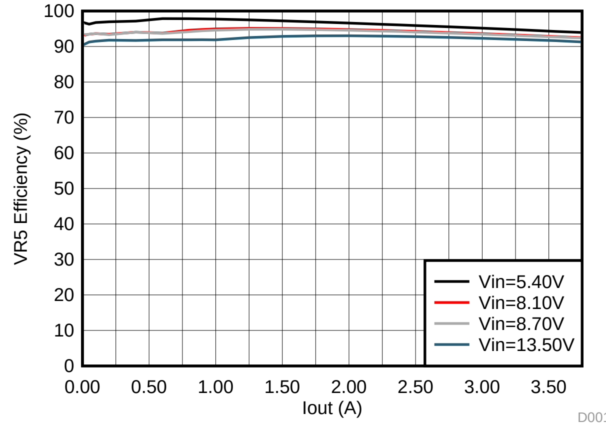


Figure 11. VR5 Efficiency vs Load, NVDC

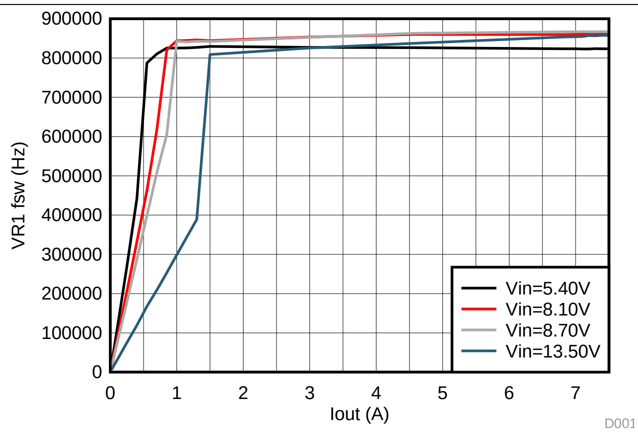


Figure 12. VR1 Switching Frequency vs Load, NVDC

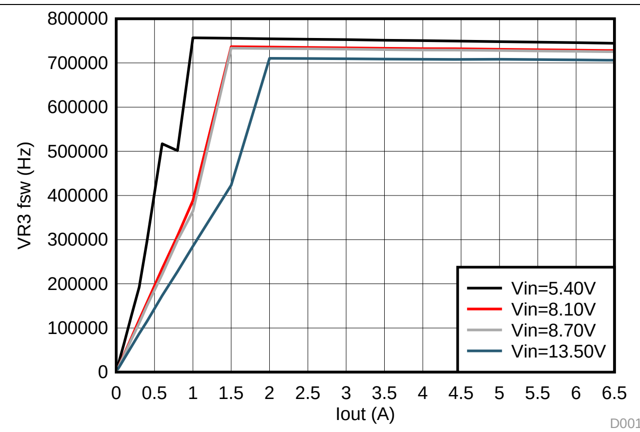


Figure 13. VR3 Switching Frequency vs Load, NVDC

Typical Characteristics (continued)

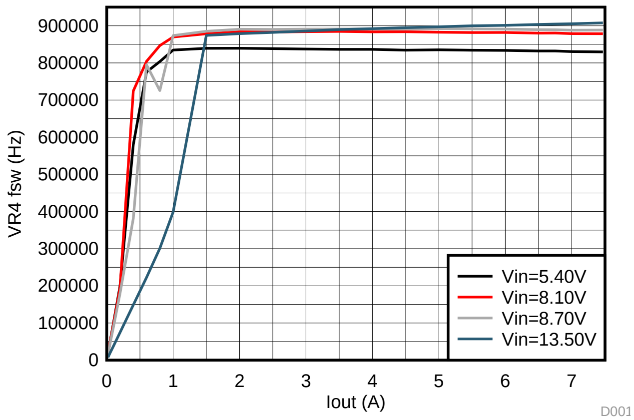


Figure 14. VR4 Switching Frequency vs Load, NVDC

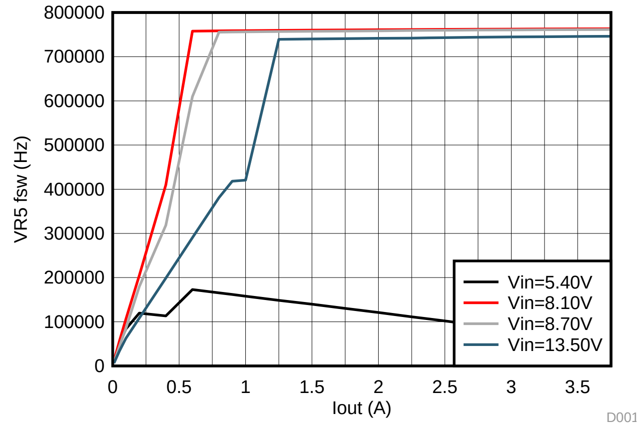


Figure 15. VR5 Switching Frequency vs Load, NVDC

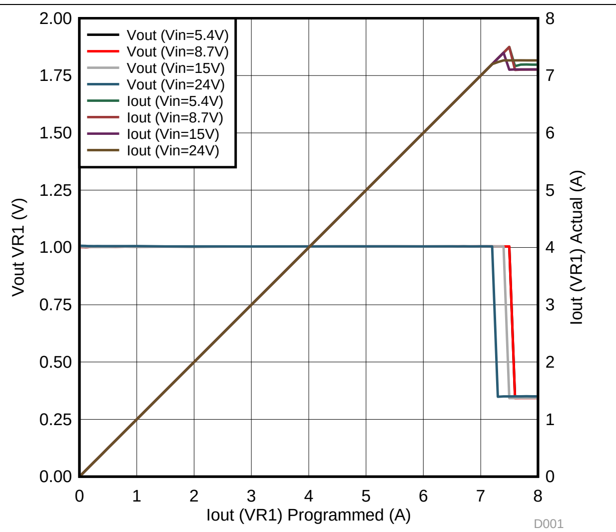


Figure 16. VR1 Current Limit: Vout and Iout vs Load, Non-NVDC

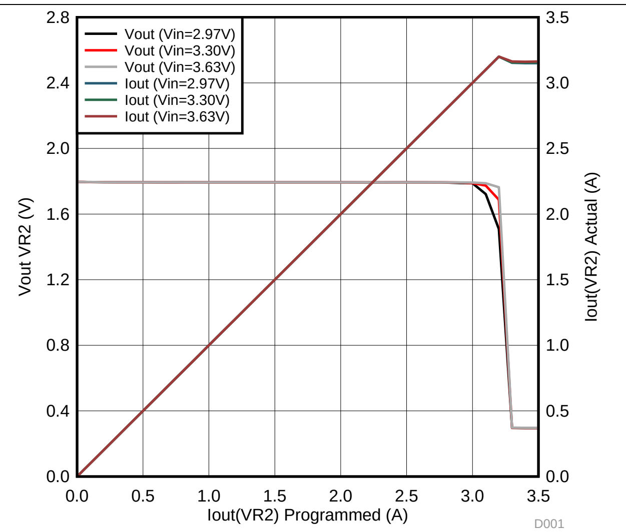


Figure 17. VR2 Current Limit: Vout and Iout vs Load, Non-NVDC

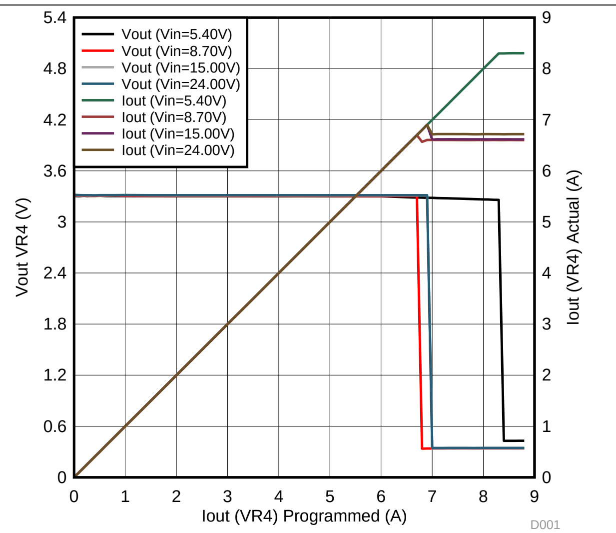


Figure 18. VR3 Current Limit: Vout and Iout vs Load, Non-NVDC

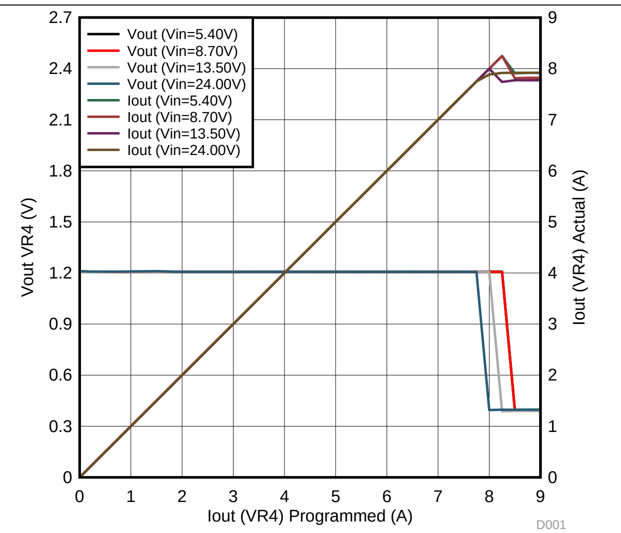


Figure 19. VR4 Current Limit: Vout and Iout vs Load, Non-NVDC

Typical Characteristics (continued)

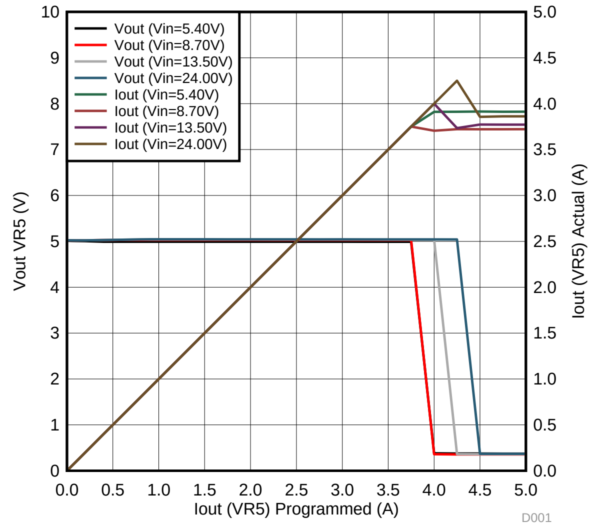


Figure 20. VR5 Current Limit: Vout and Iout vs Load, Non-NVDC

8 Detailed Description

8.1 Overview

The TPS650830 is a single-chip solution Power Management IC designed specifically for the latest Intel Processors targeted for Tablets, Ultrabooks, and Notebooks with NVDC or non-NVDC power architectures, using 2S, 3S, or 4S Lithium-Ion battery packs.

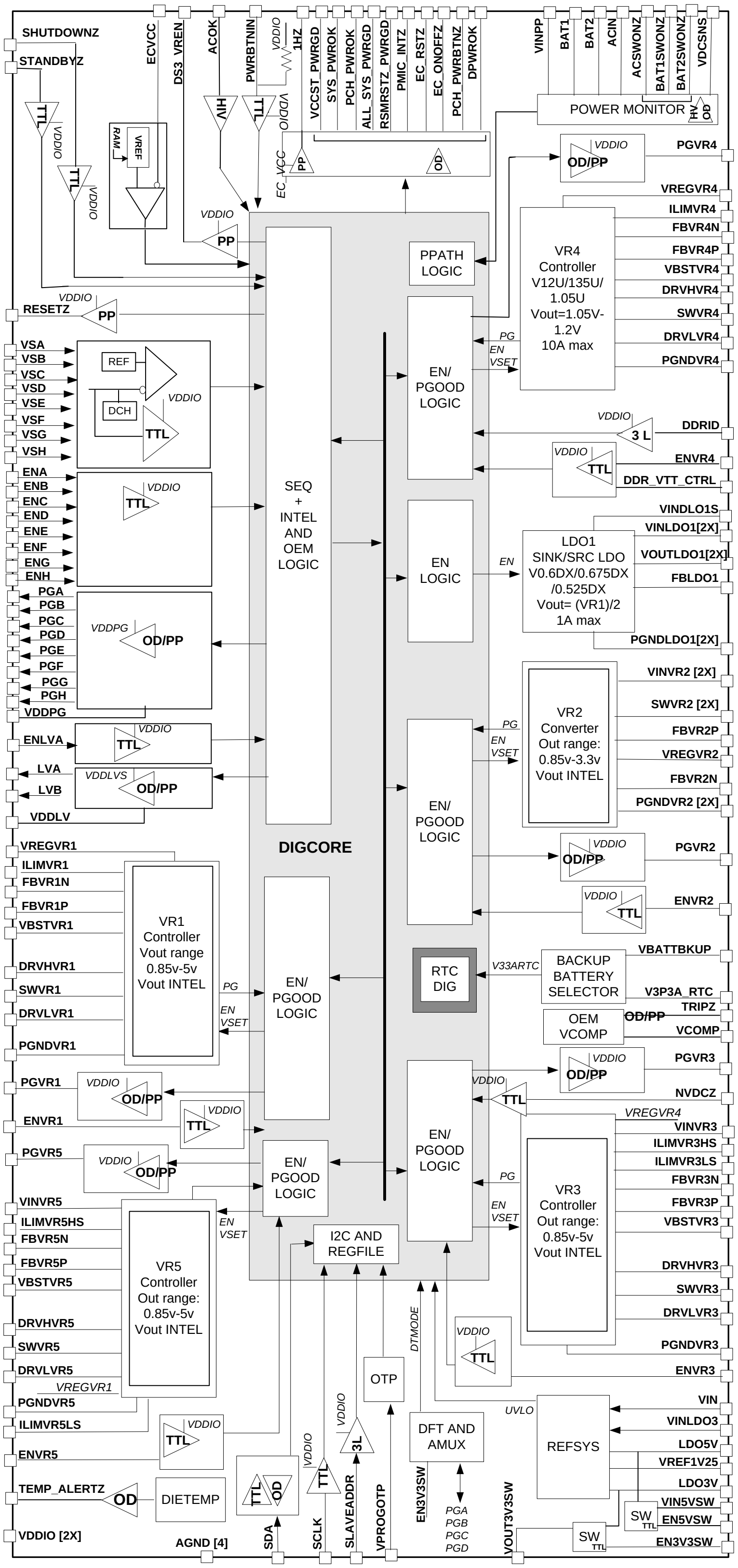
The TPS650830 is used for Volume systems with the low voltage rails merged for the smallest footprint and lowest cost system power solution.

The TPS650830 can provide the complete power solution based on the Intel Reference Designs. Five highly efficient step-down voltage regulators (VRs) and a sink/source LDO, are used along with power-up sequence logic managing external load switches to provide the proper power rails, sequencing, and protection - including DDR3 and DDR4 memory power. The regulators support dynamic voltage scaling (DVS) for maximum efficiency including Connected Standby. The high frequency voltage regulators use small inductors and capacitors to achieve a small solution size. Output power is adjustable on four VR controllers. An I^2C interface allows simple control by the embedded controller (EC). Each version is available in a 7x7 NFBGA package and a 9x9 NFBGA package. The 7x7 NFBGA package can be used in Type 4 PCB boards for the smallest area implementation. The 9x9 NFBGA package can be used in Type 3 and Type 4 PCB boards allowing to minimize cost and area.

The Powergood Comparator Logic allows controlling and monitoring four external load switches within the sequence. All the VR and Load Switch Powergood signals are used in the Power Good Tree of which the outputs are shown with open-drain outputs. Enable inputs allow connecting externally to set the sequence, and it also allows using various Sleep Mode State signals. The STANDBYZ allows entering a Deep Sleep Mode, in which the out put voltages of the voltage regulators can be reduced to save power by DVS.

The Power Monitoring comparators are used to detect and monitor up to three input power sources (adapter, battery1, battery2, or any other combination). Over temperature of the PMIC self-protects, and outputs a Status output, TEMPALERTZ; plus there is a dedicated comparator that can monitor system over temperature with multiple stacked PTC thermistors, or an NTC thermistor. The PMIC automatically swtiches between an internal 3.1V LDO when a powersource is connected; or to a Backup Battery (Coin Cell) when all power sources are removed. This output RTC rail is used to maintain the always-on RTC rails for critical register data.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Voltage Regulator Assignment and Powergood Comparator Logic Assignment (External Voltage Regulator or Load Switch) for SkyLake Platform

For the SkyLake Power Map implementation, the five PMIC voltage regulators and LDO1 are assigned with the low -voltage rails merged or split according to the configuration. For the Volume (merged low voltage rails) configuration six external load switches are controlled and monitored by using six powergood comparator logic blocs.

Table 1. Voltage Regulator and Powergood Comparator Logic Assignment for Intel SkyLake Platform

TPS650830	SkyLake PLATFORM POWER SYSTEM VOLTAGE RAIL VOLUME (Merged Low Voltage Rails)	OUTPUT VOLTAGE, V_{out}	I_{out} ACTIVE MODE	I_{out} CONNECTED STANDBY MODE
VR1	V1.00A / 0.85A	1.00V	6.47A	0mA
VR2	V1.8A	1.8V	1.44A	4mA
VR3	V3.3A_DSW	3.3V	6.29A	6mA
VR4	V1.2U	1.2V,1.35V,1.1V	7.24A	8mA
VR5	V5A_DS3	5V	3.75A	1mA
LDO1	V0.6Dx	0.6V, 0.675V, 0.55V	0.6A	0mA (off)
External VR_a	none	-	-	-
External VR_b	none	-	-	-
Powergood Comparator Logic a	V3.3A_PCH Enable/Sense External Load Switch	3.3V	–	–
Powergood Comparator Logic b	V1.8U_2.5U Enable/Sense External Load Switch	1.8V	–	–
Powergood Comparator Logic c	Generic Comparator	-	–	–
Powergood Comparator Logic d	VCCIO Enable/Sense External Load Switch	1.00V	–	–
Powergood Comparator Logic e	V3.3S Sense External Load Switch	3.3V	–	–
Powergood Comparator Logic f	V1.8S Sense External Load Switch	1.8V	–	–
Powergood Comparator Logic g	V1.0S Sense External Load Switch	1.00V	–	–

8.3.2 Converters

Table 2. Converters

	Enable in Control section
	Power good handling in Control section
	All converters have same input voltage
	All converters have same power good scheme
	All converters have same auto discharge scheme
*	All converters have UVLO with same shutdown voltage and hysteresis

The PMIC has 5 built in DCDC converters. The voltage regulators are highly configurable both in terms of voltage and current. Of the five voltage regulators, four voltage regulators have an external power stage, with programmable current limit (programmed by an external resistor), which allows optimal selection of external passive components based on desired system load. VR2 has a completely integrated power stage, except for the required passive components. To maintain high efficiency, the converters are implemented as synchronous step down converters.

One additional voltage regulators in the form of Low Drop Out (LDO) linear regulators are integrated as part of the PMIC. One of the LDOs, V6, is capable of sinking and sourcing current that regulates from the step down controller (for DDR memory). This LDO is designed to specifically provide the VTT power to DDR memory. Its output voltage tracks the output voltage of the step down controller and is set to regulate to half of the step down controller voltage.

8.3.2.1 Power Save Mode

At medium and heavy loads, the converter and the controllers operate in a PWM mode. As soon as the inductor current gets discontinuous, which means that the output current gets lower than half of the inductor ripple current, the converters enter Power Save Mode. In Power Save Mode the switching frequency decreases linearly with the load current and maintains a high efficiency. By default, the converters and controller operate in the AutoPFM mode such that the transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

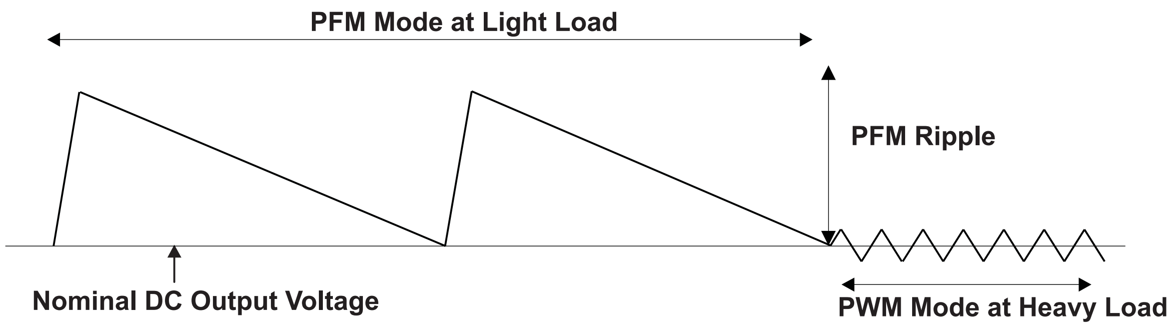


Figure 21. PFM and PWM Mode Operation

The figure above shows the converter/ controller operation in PFM and PWM mode. In PFM mode the minimum voltage that the output falls to is the programmed regulation voltage. The output voltage ripple in PFM mode is determined based on the external passive components (L and C). The regulator ensures that the minimum voltage during PFM mode is the same as the programmed regulation voltage (within the AC and DC tolerance).

8.3.2.2 Voltage Regulator Startup

All the voltage regulators including the VTT LDO1 can be enabled using either pin enables or I2C commands. The default setting uses the pin enable. The VTT LDO1 can only be enabled using the DDR_VTT_CTRL discrete input. VTT LDO1 can be enabled by pin (DDR_VTT_CTRL) or by register (0xE9, MSB bit 7 masks the DDR_VTT_CTRL pin, and bit 6 enables the VTT LDO1). Each other Voltage Regulator (VR) can be enabled by the enable pin (ENAVRx) or by I2C Register (xCNT). The voltage should not be changed by register at the exact same time the voltage regulator is enabled. If a different voltage than the default is needed at power-up, then the register (xCNT) should program the voltage first, and then a separate command should enable the register separately. Dynamic voltage change (DVS) can be done any time after power-up.

Each of the voltage regulators except for the VTT LDO1 are controlled by an internal softstart to make sure the output voltage ramps up gently and does not cause huge inrush current during startup to prevent droop on the input. The VTT LDO1 startup time is driven by the DDR memory requirements for the VTT voltage rail - which requires that the ramp up on voltage be faster than 35µs.

8.3.2.3 Power Good

During operation, when the voltage regulators are enabled, the output voltage for each rail is monitored in order to assess if the output voltage is within a specified voltage range. A power good status bit is generated and stored in the PWRSTAT1 register. If the output voltage is within the specified voltage range, the respective power good status bit is set to a logic low. If the output voltage falls below or goes above the specified voltage range, the power good status bit will be set to a logic high. By default, if any of the output voltage rails experience a power good fault condition, the PMIC will automatically shutdown in order to protect the system unless and until the power fault is masked. The voltage thresholds for each of the power good comparators is a percentage relative to the nominal voltage setting of the output voltage - please see the parametric table for each voltage regulator power good for the USL and LSL limits of the power good comparators.

If a particular voltage rail is not critical to the performance of the overall system, the respective power good output can be masked using the PGMASK1 and PGMASK2 registers. The masking of a power good fault will inhibit an automatic PMIC shutdown. This can be also very helpful for debug purposes incase of system failure to isolate the voltage regulator with the sensitive output voltage.

In order to avoid an erroneous power good fault during the turn-on of the voltage regulators, the power good output is masked for a fixed 30µs relative to the enable whether it be from the discrete signal or from an I2C command. Power Good is also masked when coming out of sleep (S3 state) for a period of 100µs to ensure that there is no false triggering of the power good comparator.

8.3.2.4 Current Limit

All voltage regulators are current limited, the current limit can be set based on the application load current using an external resistor for all VRs except for VR2 which has an internally set current limit as it has an integrated power stage. The current limit controls the maximum output current. If the maximum current is reached, the output voltage will start to droop since the load can no longer be supplied with sufficient power. If the voltage drops below the power good threshold, the power fault status will be set to a logic high and if the power fault is not masked, the PMIC will automatically shutdown in a controlled manner to protect the system.

For voltage regulators with an externally programmable current limit, please use the following equation to calculate the desired resistor value to prevent inductor saturation under nominal operation. I_{REF} is typically in the order of 50µA. R_{DSON} is the resistance of the low side FET under nominal operating conditions. A scaling factor of 1.5 is used to take into account for the inductor variation (±20%) and temperature coefficient differences between the reference current and the FET R_{DSON}. Note that the inductor should be sized appropriately (dimension, saturation current, heat rating) based on the intended application load.

$$R_{EXT}=R_{DSON^*} (I_{LOAD}+I_{ripple}/2)*1.5/I_{REF} \quad (1)$$

8.3.2.5 Output Discharge Feature

All the voltage regulators have a built in output discharge feature. The output discharge feature consists of being able to configure register bits to enable a discharge resistor which is only active whenever the voltage regulator is disabled. The discharge resistors for each of the voltage regulators can be configured using the DISCHCNT1, DISCHCNT2, DISCHCNT3 and DISCHCNT4 registers. The discharge resistors are disconnected when the voltage regulators are enabled in order to minimize any losses within the PMIC.

8.3.2.6 Output Voltage Control

All voltage regulators are designed to regulate a fixed output voltage. To achieve high accuracy the output voltage for the converters and controller is sensed using a separate feedback pin. For each of the voltage rails, except for the VTT LDO, the output voltage can be changed to slightly higher or lower values by changing the default setting in the voltage regulator control registers (see section on the Voltage Regulator Voltage Options). This function can be used to save power when supplying the connected load at its minimum possible supply voltage or to compensate for voltage drops during load transients by programming it slightly higher. In addition the range of the output voltage for the regulators is highly programmable. If you need a different output voltage configuration from the specified default, please contact TI to generate you a custom part.

8.3.2.7 Converter Low Power Mode Operation

For optimizing low power operation, the output voltage of the converters can be set to a specific value. The low power output voltage is set by the specific register and bits shown in the Voltage Regulator Voltage Options tables. Entering the low power mode is accomplished by asserting the SLP_S0# signal to a logic low. In this low power mode, the power good function remains active and is not affected by the transition from normal operation mode to the low power mode and vice versa.

8.3.2.8 Controller Low Power Mode Operation

For optimizing low power operation, the output voltage of the V10 controller can be set to a specific value. The low power output voltage is set by the specific register and bits shown in the Voltage Regulator Voltage Options tables. Entering the low power mode is accomplished by asserting the DDR_VTT_CTRL signal to a logic low. In this low power mode, the power good function remains active and is not affected by the transition from normal operation mode to the low power mode and vice versa.

In situations where the output current demand from the controller is very small, the controller can be placed in an Ultra Low Quiescent (ULQ) mode to reduce power consumption and increase the efficiency.

8.3.2.9 Undervoltage Lockout

An undervoltage lockout function prevents converter start-up if the supply voltage on the VIN pin of the PMIC is lower than the undervoltage lockout threshold (see electrical characteristics table). When in operation, the converter triggers a shut down of the system if the supply voltage on the VIN pin drops below the undervoltage lockout threshold and the system will not automatically restart.

8.3.3 Coincell Selector

8.3.3.1 Functional Description of RTC Powerpath and LDO

In case where the main system battery is removed and there is no alternate power source, the RTC data, configuration and status registers, oscillator and timekeeping path of the RTC block are backed up by either a super capacitor or a coin cell battery. If the coincell/ super capacitor battery voltage falls below the minimum operational voltage and there is no input voltage (AC/ DC above the PMIC UVLO), the RTC data registers will be invalid. As the Intel RTC cannot handle a max voltage higher than 3.2V, when AC/ DC is present and is higher than the UVLO threshold, the RTC is supplied by the AC/DC rather than from the coincell - thus maximizing the stored charge in the coincell battery. When AC/DC is present, the internal coincell selector selects the higher of the coincell voltage and the AC/DC voltage. When AC/DC is chosen as a source, there is a coincell LDO which is driven from the 5V PMIC LDO to regulate The output voltage is programmable to 2.975V, 3.0V, 3.025V, 3.05V, 3.075V, 3.1V, 3.13V, 3.16V.

The main power source for the RTC LDO is the 5V PMIC internal LDO, when the main system battery (VDC) is greater than 5.4V. The RTC LDO will be bypassed and the RTC supply will be powered by the coincell when VDC falls below this threshold - to maximize the coincell battery life. The coincell is used as a last resort. All power routing of the source selection for the RTC power is done internally and no external connections other than the coin cell or super cap is required.

8.3.4 I^{2}C - Interface

I^{2}C is a 2-wire serial interface developed by NXP (formerly Philips Semiconductor) (see I^{2}C-Bus Specification and user manual, Rev 4, 13 February 2012). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^{2}C compatible devices connect to the I^{2}C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS650830 works as a slave and supports the following data transfer modes, as defined in the I^{2}C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents are loaded when voltage is applied to TPS650830 higher than the undervoltage lockout threshold. The I^{2}C interface is running from an internal oscillator that is automatically enabled when there is an access to the interface.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document.

The TPS650830 supports 7-bit addressing; 10-bit addressing and general call address are not supported. The default device address is defined by the status of the SLAVEADDR pin. 3 different slave addresses are possible, 0x30 (SLAVEADDR 0 V), 0x32 (SLAVEADDR 3.3 V) and 0x34 (SLAVEADDR floating).

All registers are set to their default value when the supply voltage is below the UVLO threshold.

8.3.4.1 F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, see Figure 22. All I^2C-compatible devices should recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, see Figure 23. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge*, see Figure 24, by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit = 0) or receive data from the slave (R/W bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, see Figure 22. This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address

Attempting to read data from register addresses not listed in this section results in FFh being read out. FS I^2C operation does not support repeated start

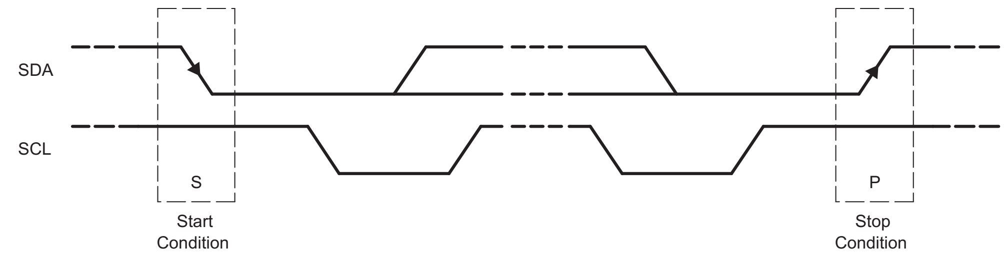


Figure 22. START and STOP Conditions

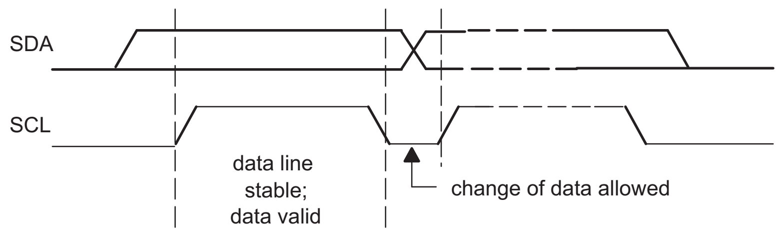


Figure 23. Bit Transfer on the I²C-bus

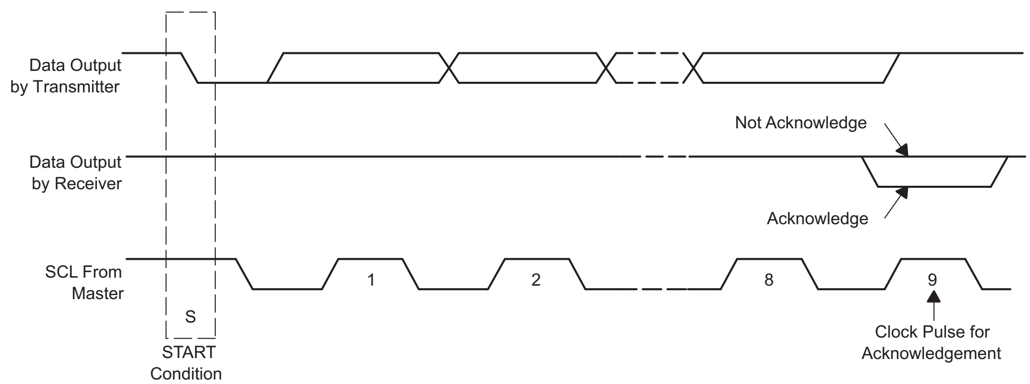


Figure 24. Acknowledge on the I²C-Bus

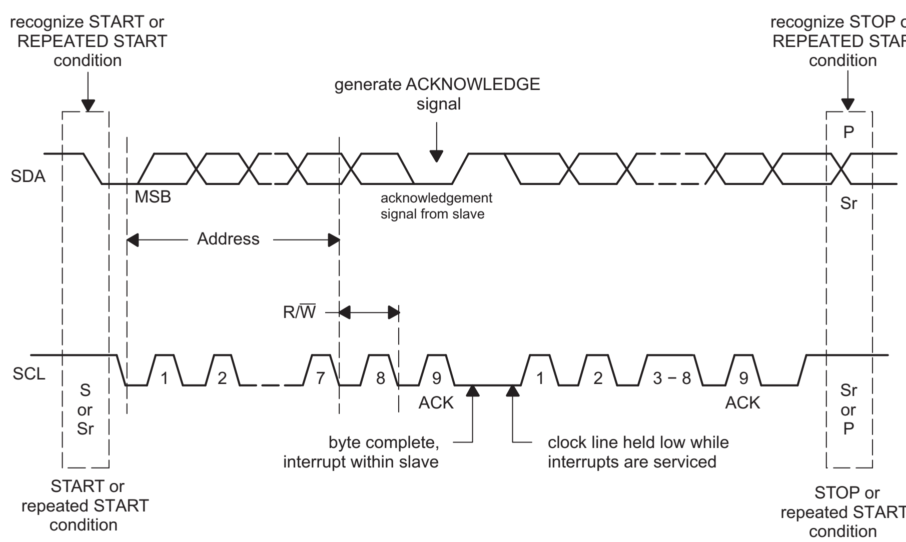


Figure 25. Bus Protocol

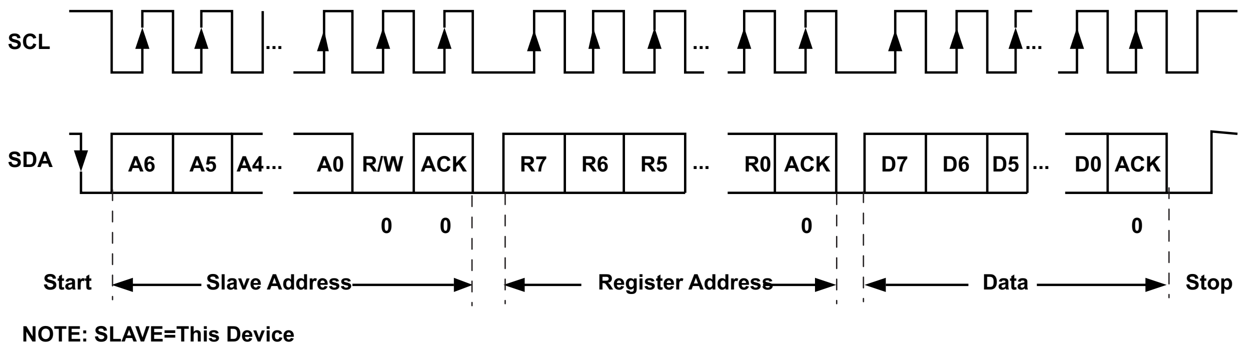


Figure 26. I²C Interface WRITE to TPS650830 in F/S Mode

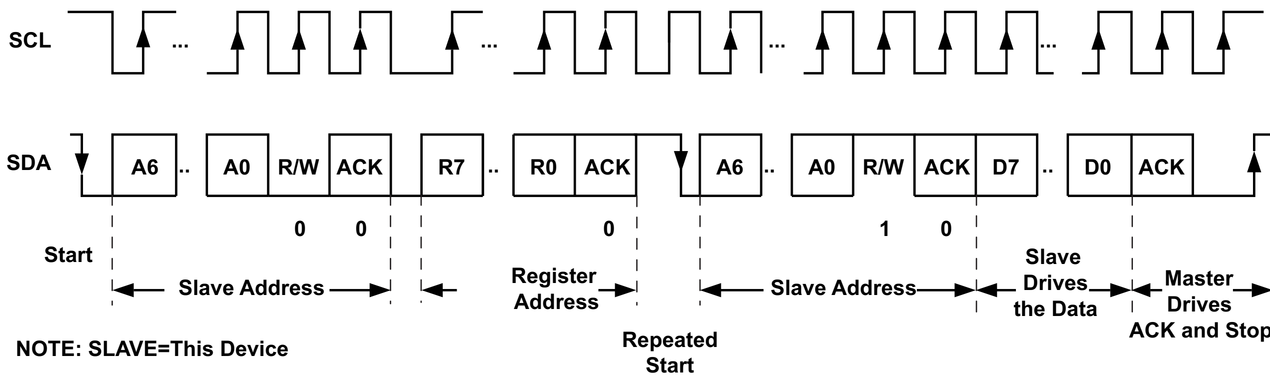


Figure 27. I²C Interface READ from TPS650830 in F/S Mode

8.4 Device Functional Modes

The TPS650830 PMIC has been designed to provide the overall power solution for use with the latest Intel Processors. This section describes the internal state machine of the TPS650830 PMIC.

NO POWER State: If the VIN pin of the PMIC is below the VUVLO voltage threshold and the voltage on the VBATTBKUP pin is below 2.3V, the PMIC will be in the NO POWER state. Naturally, in this state, all voltage regulators are off.

RTC DOMAIN State: If a coincell or supercap is connected to the VBATTBKUP pin of the PMIC and its voltage is greater than 2.3V, the state machine will be in the RTC DOMAIN state. When entering this state, all I2C registers that reside in the RTC Domain will reset to their default settings.

POWER UP State: If the voltage on the VIN pin is greater than the VUVLO voltage threshold, the PMIC will enter the POWER UP state. In this state, I2C control of all the registers is possible. If this is the first time entering the POWER UP state, it will remain in this state until a high level is detected on the SHUTDOWNZ pin which could be controlled by an external source. (Typically SHUTDOWNZ is connected to LDO3 to always keep it high). Once a high level is detected on the SHUTDOWNZ pin, the PMIC will assert the VR3 internal enable high (This internal signal is AND'ed with the VR3EN pin to turn on VR3). This enables the VR3 (V3.3A_DSW) regulator. The PMIC will generate the V3.3A_DSW power good signal, PGVR3. The PMIC will then generate the DPWROK signal which is a delayed version of the PGVR3 signal and sends it to the Platform Controller Hub (PCH) of the system.

Device Functional Modes (continued)

POWER SEQUENCE State: The PMIC enters this state once a low to high transition is detected on the SLP_SUS# pin. This pin is driven by the PCH. In this state, the PMIC asserts the ENVR5 pin high to enable the V5A_DS3 regulator, VR5. The SLP_SUS# signal also enables an external load switch which provides 3.3V to the EC. The output of this load switch is monitored by the main PMIC on the ECVCC pin. Once the voltage on this pin is detected, the PMIC will assert the PGVR3 pin , which should be connected externally to the ENVR2 pin. The ENVR2 pin enables the V1.8V voltage regulator, VR2.

NORMAL MODE State: Entering this state occurs after the RSMRST#_PWRGD is asserted high. This power good output is the AND of the V3.3A_DSW_PG (PGVR3), V5A_DSW_PG (PGVR3), V3.3A_PCH_PG (PGA), V1.8A_PG (PGVR2), V1.00A_PG (PGVR1), and the V0.85A_PG (PGVR1). The PMIC will remain in this state during normal operation. Only certain events will send the PMIC to other states as described in this section.

COLD OFF State: The PMIC will enter this state if the PCH detects that the PWRBTN# has been asserted for at least 5 seconds. In this state, all the voltage regulators except for the V3.3A_DSW (VR3) regulator are turned off. The 1Hz clock is turned off. Exiting this state occurs if the PWRBTNIN pin is asserted low and the SLP_SUS# transitions from a logic low to a logic high. These events will send the State Machine to the POWER SEQUENCE state.

EMERGENCY SHUTDOWN State: The EMERGENCY SHUTDOWN state occurs through various avenues. In this state, all voltage regulators and 1 Hz clock are turned off. Exiting this state requires that the PWRBTNIN pin detect a high to low transition or that the ACOK pin detect a low to high transition. Either of these events will send the State Machine to the POWER UP state.

VOLTAGE REGULATOR FAULT: Every voltage regulator has a power good fault associated with it. If at any point, any power good fault is detected, the state machine will enter the EMERGENCY SHUTDOWN state. TI recommends that the power good faults not be masked during normal operation.

FORCE SHUTDOWN: If the Force Shutdown command is issued via the SHDWNCTRL register, the state machine will enter the EMERGENCY SHUTDOWN state.

POWER BUTTON INTERRUPT: If the PWRBTNIN pin is held low for longer than the time defined by the FLT[3:0] bits in the PBCONFIG register, the state machine will enter the EMERGENCY SHUTDOWN state.

CRITICAL TEMP: If at any point the PMIC die temperature exceeds the Overtempeture Protection parameter, the state machine will enter the EMERGENCY SHUTDOWN state. In order to avoid the PMIC die temperature from reaching the Critical Temperature range, all the voltage rail power good faults default to being enabled. TI recommends that the power good faults not be masked during normal operation.

DVS: When Dynamic Voltage Scaling (DVS) is programmed, include an Active State when STANDBYZ pin is Hi; and a Low Power Mode State when the STANDBYZ pin is low. The output voltages will typically be at a higher voltage setting in the Active Mode to allow a high performance operation from the system. The output voltages will typically be at a lower voltage setting in the Sleep Mode to allow a low-power operation from the system and increase battery run-time. If DVS is not programmed, then the output voltage will always be at the same value, regardless what the logic value is of the STANDBYZ pin.

8.5 Register Map

8.5.1 OTP_SPARE2 Register (address = 0xF0) [reset = 00000000]

Figure 28. OTP_SPARE2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
SPARE2[7]	SPARE2[6]	SPARE2[5]	SPARE2[4]	SPARE2[3]	SPARE2[2]	SPARE2[1]	SPARE2[0]
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3. OTP_SPARE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SPARE2[7:0]	RW	00000000	OTP SPARE BYTE for Future use

8.5.2 OTP_SPARE1 Register (address = 0xEF) [reset = 00000000]

Figure 29. OTP_SPARE1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
SPARE1[7]	SPARE1[6]	SPARE1[5]	SPARE1[4]	SPARE1[3]	SPARE1[2]	SPARE1[1]	SPARE1[0]
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. OTP_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SPARE1[7:0]	RW	00000000	OTP SPARE BYTE for future use

8.5.3 VREN_PIN_OVR Register (address = 0xEE) [reset = 00000000]

Figure 30. VREN_PIN_OVR Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V12_PIN_OVR	V11_PIN_OVR	V10_PIN_OVR	V9_PIN_OVR	V8_PIN_OVR	V7_PIN_OVR	V5_PIN_OVR	V4_PIN_OVR
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. VREN_PIN_OVR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	V12_PIN_OVR	RW	0	V12 ENABLE PIN Over Ride **0**: V12 Pin controls V12 (Default) **1**: V12 is ON if VREN PIN MASK = '0'
6	V11_PIN_OVR	RW	0	V11 ENABLE PIN Over Ride **0**: V11 Pin controls V11 (Default) **1**: V11 is ON if VREN PIN MASK = '0'
5	V10_PIN_OVR	RW	0	V10 ENABLE PIN Over Ride **0**: V10 Pin controls V10 (Default) **1**: V10 is ON if VREN PIN MASK = '0'
4	V9_PIN_OVR	RW	0	V9 ENABLE PIN Over Ride **0**: V9 Pin controls V9 (Default) **1**: V9 is ON if VREN PIN MASK = '0'
3	V8_PIN_OVR	RW	0	V8 ENABLE PIN Over Ride **0**: V8 Pin controls V8 (Default) **1**: V8 is ON if VREN PIN MASK = '0'
2	V7_PIN_OVR	RW	0	V7 ENABLE PIN Over Ride **0**: V7 Pin controls V7 (Default) **1**: V7 is ON if VREN PIN MASK = '0'
1	V5_PIN_OVR	RW	0	V5 ENABLE PIN Over Ride **0**: V5 Pin controls V5 (Default) **1**: V5 is ON if VREN PIN MASK = '0'
0	V4_PIN_OVR	RW	0	V4 ENABLE PIN Over Ride **0**: V4 Pin controls V4 (Default) **1**: V4 is ON if VREN PIN MASK = '0'

8.5.4 TEMPHOT Register (address = 0xEC) [reset = 00000000]

Figure 31. TEMPHOT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_TEMPHOT[1]	RESERVED_TEMPHOT[0]	LDO1_HOT	VR5_HOT	VR4_HOT	VR3_HOT	VR2_HOT	VR1_HOT
0	0	0	0	0	0	0	0
R	R	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. TEMPHOT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED_TEMPHOT[1:0]	R	00	Read Always Returns '1'
5	LDO1_HOT	RW	0	LDO1 HOT TEMP **0**: Not asserted (Default) **1**: Asserted, write '1' to clear
4	VR5_HOT	RW	0	VR5 HOT TEMP **0**: Not asserted (Default) **1**: Asserted, write '1' to clear
3	VR4_HOT	RW	0	VR4 HOT TEMP **0**: Not asserted (Default) **1**: Asserted, write '1' to clear
2	VR3_HOT	RW	0	VR3 HOT TEMP **0**: Not asserted (Default) **1**: Asserted, write '1' to clear
1	VR2_HOT	RW	0	VR2 HOT TEMP **0**: Not asserted (Default) **1**: Asserted, write '1' to clear
0	VR1_HOT	RW	0	VR1 HOT TEMP **0**: Not asserted (Default) **1**: Asserted, write '1' to clear

8.5.5 TEMPCRIT Register (address = 0xEB) [reset = 00000000]

Figure 32. TEMPCRIT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_TEMPCRIT[1]	RESERVED_TEMPCRIT[0]	LDO1_CRIT	VR5_CRIT	VR4_CRIT	VR3_CRIT	VR2_CRIT	VR1_CRIT
0	0	0	0	0	0	0	0
R	R	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. TEMPCRIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED_TEMPCRIT[1:0]	R	00	Read Always Returns '1'
5	LDO1_CRIT	RW	0	LDO1 CRITTEMP **0**: Not asserted (Default) **1**: Asserted, write '1' to clear
4	VR5_CRIT	RW	0	VR5 CRITTEMPs **0**: Not asserted (Default) **1**: Asserted, write '1' to clear
3	VR4_CRIT	RW	0	VR4 CRITTEMPs **0**: Not asserted (Default) **1**: Asserted, write '1' to clear
2	VR3_CRIT	RW	0	VR3 CRITTEMP **0**: Not asserted (Default) **1**: Asserted, write '1' to clear
1	VR2_CRIT	RW	0	VR2 CRITTEMP **0**: Not asserted (Default) **1**: Asserted, write '1' to clear
0	VR1_CRIT	RW	0	VR1 CRITTEMP **0**: Not asserted (Default) **1**: Asserted, write '1' to clear

8.5.6 STDBY_CTRL Register (address = 0xEA) [reset = 11111110]

Figure 33. STDBY_CTRL Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_STDBY_CTRL[4]	RESERVED_STDBY_CTRL[3]	RESERVED_STDBY_CTRL[2]	RESERVED_STDBY_CTRL[1]	RESERVED_STDBY_CTRL[0]	EN_VCOMP_10U	VCOMP_EN	QLSLPS0_ACTIVE
1	1	1	1	1	1	1	0
R	R	R	R	R	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. STDBY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED_STDBY_CTRL[4:0]	R	11111	Read Always Returns '1'
2	EN_VCOMP_10U	RW	1	VCOMP Current Source Control bit: **0**: Disable **1**: Enable (Default)
1	VCOMP_EN	RW	1	VCOMP Enable Control bit: **0**: Disable **1**: Enable (Default)
0	QLSLPS0_ACTIVE	RW	0	SLP_S0 & DDR_VTT_CTRL Detect logic Control **0**: Normal Operation DELAY_ALL_SYS_PG is used in QSLPS0Z (Default) **1**: DELAY_ALL_SYS_PG is ignored for QSLPS0Z

8.5.7 MISC_BITS Register (address = 0xE9) [reset = 00010000]

Figure 34. MISC_BITS Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V13_PIN_OVR	MV13EN	V6_PIN_OVR	MV6EN	msLP_S3ZPG	msLP_SUSZPG	SPARE	V13DISCHG
0	0	0	1	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. MISC_BITS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	V13_PIN_OVR	RW	0	V13 ENABLE PIN Over Ride **0**: V13 is OFF if MV13EN is '1' (Default) **1**: V13 is ON if MV13EN is '1'
6	MV13EN	RW	0	V13 Enable Pin Mask **0**: DDR_VT_CTRL Pin controls V13 (Default) **1**: V13_EN_PIN Bit [Bit(3)] controls V13
5	V6_PIN_OVR	RW	0	V6 ENABLE PIN Over Ride **0**: V6 Pin controls V6 (Default) **1**: V6 is ON if VREN PIN MASK = '0'
4	MV6EN	RW	1	V6 Enable Pin Mask **0**: VR Enable Pin controls VR enable **1**: VR Enable Pin masked V*CTLV controls VR enable (Default)
3	msLP_S3ZPG	RW	0	SLP_S3Z is part of the power good tree **0**: SLP_S3Z is part of Power Good Tree (Default) **1**: SLP_S3Z is masked and set to 1 (not part of the Power Good tree)
2	msLP_SUSZPG	RW	0	SLP_SUSZ is part of the power good tree **0**: SLP_SUSZ is part of Power Good Tree (Default) **1**: SLP_SUSZ is masked and set to 1 (not part of the Power Good tree)
1	BC_ACOK_EN	RW	1	Enables BC_ACOK output out of LVA pin. The in put is ACOK pin, instead of ENLVA pin. **0**: LVA pin is not BC_ACOK, and ENLVA is the input for LVA output, behaving as a general purpose level-shifter. **1**: LVA pin is BC_ACOK, and ACOK is the input, and ENLVA is not functional. BC_ACOK is a level-shifted version of ACOK. (Default)
0	V13DISCHG	RW	0	V0.6DX discharge resistance (V13) **0**: no discharge (Default) **1**: 100 Ω

8.5.8 PGOOD_STAT2 Register (address = 0xE8) [reset = 00000000]

Figure 35. PGOOD_STAT2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_PGOOD_STAT2[2]	RESERVED_PGOOD_STAT2[1]	RESERVED_PGOOD_STAT2[0]	V12_PGOOD	V11_PGOOD	V11_SPGD	V8_SPGD	V6_SPGD
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. PGOOD_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED_PGOOD_STAT2[2:0]	R	000	Read Always Returns '1'
4	V12_PGOOD	R	0	V12 PGOOD STATUS **0**: Fail (Default) **1**: Pass
3	V11_PGOOD	R	0	V11 PGOOD STATUS **0**: Fail (Default) **1**: Pass
2	V11_SPGD	R	0	V11S PGOOD STATUS **0**: Fail (Default) **1**: Pass
1	V8_SPGD	R	0	V8S PGOOD STATUS **0**: Fail (Default) **1**: Pass
0	V6_SPGD	R	0	V6S PGOOD STATUS **0**: Fail (Default) **1**: Pass

8.5.9 PGOOD_STAT1 Register (address = 0xE7) [reset = 00000000]

Figure 36. PGOOD_STAT1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V13_PGOOD	V10_PGOOD	V9_PGOOD	V8_PGOOD	V7_PGOOD	V6_PGOOD	V5_PGOOD	V4_PGOOD
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. PGOOD_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	V13_PGOOD	R	0	V13 PGOOD STATUS **0**: Fail (Default) **1**: Pass
6	V10_PGOOD	R	0	V10 PGOOD STATUS **0**: Fail (Default) **1**: Pass
5	V9_PGOOD	R	0	V9 PGOOD STATUS **0**: Fail (Default) **1**: Pass
4	V8_PGOOD	R	0	V8 PGOOD STATUS **0**: Fail (Default) **1**: Pass
3	V7_PGOOD	R	0	V7 PGOOD STATUS **0**: Fail (Default) **1**: Pass
2	V6_PGOOD	R	0	V6 PGOOD STATUS **0**: Fail (Default) **1**: Pass
1	V5_PGOOD	R	0	V5 PGOOD STATUS **0**: Fail (Default) **1**: Pass
0	V4_PGOOD	R	0	V4 PGOOD STATUS **0**: Fail (Default) **1**: Pass

8.5.10 PWFAULT_MASK2 Register (address = 0xE6) [reset = 00000000]

Figure 37. PWFAULT_MASK2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_PWFAULT_MASK2[5]	RESERVED_PWFAULT_MASK2[4]	RESERVED_PWFAULT_MASK2[3]	RESERVED_PWFAULT_MASK2[2]	RESERVED_PWFAULT_MASK2[1]	RESERVED_PWFAULT_MASK2[0]	V11_FLTmsK	V12_FLTmsK
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. PWFAULT_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED_PWFAULT_MASK2[5:0]		000000	Read Always Returns '1'
1	V11_FLTmsK		0	V11 Power Fault Masked **0**: Not Masked (Default) **1**: Masked
0	V12_FLTmsK		0	V12 Power Fault Masked **0**: Not Masked (Default) **1**: Masked

8.5.11 PWFAULT_MASK1 Register (address = 0xE5) [reset = 00000000]

Figure 38. PWFAULT_MASK1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V4_FLTmsK	V5_FLTmsK	V6_FLTmsK	V7_FLTmsK	V8_FLTmsK	V9_FLTmsK	V10_FLTmsK	V13_FLTmsK
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. PWFAULT_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	V4_FLTmsK	RW	0	V4 Power Fault Masked **0**: Not Masked (Default) **1**: Masked
6	V5_FLTmsK	RW	0	V5 Power Fault Masked **0**: Not Masked (Default) **1**: Masked
5	V6_FLTmsK	RW	0	V6 Power Fault Masked **0**: Not Masked (Default) **1**: Masked
4	V7_FLTmsK	RW	0	V7 Power Fault Masked **0**: Not Masked **1**: Masked
3	V8_FLTmsK	RW	0	V8 Power Fault Masked **0**: Not Masked (Default) **1**: Masked
2	V9_FLTmsK	RW	0	V9 Power Fault Masked **0**: Not Masked (Default) **1**: Masked
1	V10_FLTmsK	RW	0	V10 Power Fault Masked **0**: Not Masked (Default) **1**: Masked
0	V13_FLTmsK	RW	0	V13 Power Fault Masked **0**: Not Masked (Default) **1**: Masked

8.5.12 COMPH_REF Register (address = 0xE4) [reset = 00000000]

Figure 39. COMPH_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
COMP_H_DISCHG	COMP_H_REF[6]	COMP_H_REF[5]	COMP_H_REF[4]	COMP_H_REF[3]	COMP_H_REF[2]	COMP_H_REF[1]	COMP_H_REF[0]
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. COMPH_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	COMP_H_DISCHG	RW	0	Comparator H Discharge value **0**: No discharge **1**: 100 Ω
6:0	COMP_H_REF[6:0]	RW	0000000	Comparator Ref: Bits(2:0) => Reference Voltage Bits(6:3) => Feedback selection

8.5.13 COMPG_REF Register (address = 0xE3) [reset = 00011110]

Figure 40. COMPG_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_COMPG_REF	COMP_G_REF [6]	COMP_G_REF [5]	COMP_G_REF [4]	COMP_G_REF [3]	COMP_G_REF [2]	COMP_G_REF [1]	COMP_G_REF [0]
0	0	0	1	1	1	1	0
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. COMPG_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Comparator PGOOD Mode[7]	RW	0	Comparator Ref: **0**: PGOOD Mode **1**: Comparator Mode
6:0	COMP_G_REF[6:0]	RW	0011110	Comparator Ref: Bits(2:0) => Reference Voltage Bits(6:3) => Feedback selection
	RESERVED_COMPG_REF	R	0	

8.5.14 COMPF_REF Register (address = 0xE2) [reset = 00011110]

Figure 41. COMPF_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_COMPF_REF	COMP_F_REF[6]	COMP_F_REF[5]	COMP_F_REF[4]	COMP_F_REF[3]	COMP_F_REF[2]	COMP_F_REF[1]	COMP_F_REF[0]
0	0	0	1	1	1	1	0
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. COMPF_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Comparator PGOOD Mode[7]	RW	0	Comparator Ref: **0**: PGOOD Mode **1**: Comparator Mode
6:0	COMP_F_REF[6:0]	RW	0011110	Comparator Ref: Bits(2:0) => Reference Voltage Bits(6:3) => Feedback selection
7	RESERVED_COMPF_REF	R	0	

8.5.15 COMPE_REF Register (address = 0xE1) [reset = 00011110]

Figure 42. COMPE_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_COMPE_REF	COMP_E_REF[6]	COMP_E_REF[5]	COMP_E_REF[4]	COMP_E_REF[3]	COMP_E_REF[2]	COMP_E_REF[1]	COMP_E_REF[0]
0	0	0	1	1	1	1	0
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. COMPE_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_COMPE_REF	R	0	
6:0	COMP_E_REF[6:0]	RW	0011110	Comparator Ref: Bits(2:0) => Reference Voltage Bits(6:3) => Feedback selection
	Comparator PGOOD Mode[7]			Comparator Ref: **0**: PGOOD Mode **1**: Comparator Mode

8.5.16 COMPD_REF Register (address = 0xE0) [reset = 00011110]

Figure 43. COMPD_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_COMPD_REF	COMP_D_REF[6]	COMP_D_REF[5]	COMP_D_REF[4]	COMP_D_REF[3]	COMP_D_REF[2]	COMP_D_REF[1]	COMP_D_REF[0]
0	0	0	1	1	1	1	0
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. COMPD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_COMPD_REF	R	0	
6:0	COMP_D_REF[6:0]	RW	0011110	Comparator Ref: Bits(2:0) => Reference Voltage Bits(6:3) => Feedback selection
	Comparator PGOOD Mode[7]			Comparator Ref: **0**: PGOOD Mode **1**: Comparator Mode

8.5.17 COMPC_REF Register (address = 0xDF) [reset = 00011110]

Figure 44. COMPC_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_COMPC_REF	COMP_C_REF[6]	COMP_C_REF[5]	COMP_C_REF[4]	COMP_C_REF[3]	COMP_C_REF[2]	COMP_C_REF[1]	COMP_C_REF[0]
0	0	0	1	1	1	1	0
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. COMPC_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_COMPC_REF	R	0	
6:0	COMP_C_REF[6:0]	RW	0011110	Comparator Ref: Bits(2:0) => Reference Voltage Bits(6:3) => Feedback selection
	Comparator PGOOD Mode[7]			Comparator Ref: **0**: PGOOD Mode **1**: Comparator Mode

8.5.18 COMPB_REF Register (address = 0xDE) [reset = 00011110]

Figure 45. COMPB_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_COMPB_REF	COMP_B_REF[6]	COMP_B_REF[5]	COMP_B_REF[4]	COMP_B_REF[3]	COMP_B_REF[2]	COMP_B_REF[1]	COMP_B_REF[0]
0	0	0	1	1	1	1	0
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. COMPB_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_COMPB_REF	R	0	
6:0	COMP_B_REF[6:0]	RW	0011110	Comparator Ref: Bits(2:0) => Reference Voltage Bits(6:3) => Feedback selection
	Comparator PGOOD Mode[7]			Comparator Ref: **0**: PGOOD Mode **1**: Comparator Mode

8.5.19 COMPA_REF Register (address = 0xDD) [reset = 00011110]

Figure 46. COMPA_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_COMPA_REF	COMP_A_REF[6]	COMP_A_REF[5]	COMP_A_REF[4]	COMP_A_REF[3]	COMP_A_REF[2]	COMP_A_REF[1]	COMP_A_REF[0]
0	0	0	1	1	1	1	0
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. COMPA_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_COMPA_REF	R	0	
6:0	COMP_A_REF[6:0]	RW	0011110	Comparator Ref: Bits(2:0) => Reference Voltage Bits(6:3) => Feedback selection
	Comparator PGOOD Mode[7]			Comparator Ref: **0**: PGOOD Mode **1**: Comparator Mode

8.5.20 CLKCTRL1 Register (address = 0xD0) [reset = 00000000]

Figure 47. CLKCTRL1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_CLKCTRL1[6]	RESERVED_CLKCTRL1[5]	RESERVED_CLKCTRL1[4]	RESERVED_CLKCTRL1[3]	RESERVED_CLKCTRL1[2]	RESERVED_CLKCTRL1[1]	RESERVED_CLKCTRL1[0]	ECWAKEEN
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. CLKCTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED_CLKCTRL1[6:0]	RW	0000000	
0	ECWAKEEN	RW	0	**1** Hz clock **0**: clock OFF (Default) **1**: Clock ON

8.5.21 SPWRSRCINT Register (address = 0x6F) [reset = 00000000]

Figure 48. SPWRSRCINT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1_SPWRSRCINT	SLOWBATT2	SLOWBATT1	SACOK	RESERVED_SPWRSRCINT[3]	RESERVED_SPWRSRCINT[2]	RESERVED_SPWRSRCINT[1]	RESERVED_SPWRSRCINT[0]
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. SPWRSRCINT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED1_SPWRSRCINT	R	0	
6	SLOWBATT2	R	0	LOWBATT2 detection status **0**: BATT2 above threshold (Default) **1**: BATT2 below threshold
5	SLOWBATT1	R	0	LOWBATT1 detection status **0**: BATT1 above threshold (Default) **1**: BATT1 below threshold
4	SACOK	R	0	AC adapter (ACOK) detection status **0**:Aadapter removed (Default) **1**: Adapter inserted
3:0	RESERVED_SPWRSRCINT[3:0]	R	0000	

8.5.22 LOWBATTDET Register (address = 0x6A) [reset = 11111000]

Figure 49. LOWBATTDET Register Format

B7	B6	B5	B4	B3	B2	B1	B0
LOWBATTDB[1]	LOWBATTDB[0]	LOWBATT2_EN	LOWBATT1_EN	ACIN_EN	RESERVED_LOWBATTDET[2]	RESERVED_LOWBATTDET[1]	RESERVED_LOWBATTDET[0]
1	1	1	1	1	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. LOWBATTDET Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	LOWBATTDB[1:0]	RW	11	Low battery detection debounce time **00**: 4 RTC periods (120 us) **01**: 32 RTC periods (960us) **10**: 64 RTC periods (1920 us) **11**: 128 RTC periods (3840us) (Default)
5	LOWBATT2_EN	RW	1	Low battery Two detection Enable **0**: Disable **1**: Enable (Default)
4	LOWBATT1_EN	RW	1	Low battery One detection Enable **0**: Disable **1**: Enable (Default)
3	ACIN_EN	RW	1	AC IN Comparator **0**: Disable **1**: Enable (Default)
2:0	RESERVED_LOWBATTDET[2:0]	RW	000	

8.5.23 ACOKDBDM Register (address = 0x69) [reset = 00001111]

Figure 50. ACOKDBDM Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_ACOKDBDM[3]	RESERVED_ACOKDBDM[2]	RESERVED_ACOKDBDM[1]	RESERVED_ACOKDBDM[0]	ACOKDB[1]	ACOKDB[0]	ACOKDM[1]	ACOKDM[0]
0	0	0	0	1	1	1	1
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. ACOKDBDM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED_ACOKDBDM[3:0]	RW	0000	
3:2	ACOKDB[1:0]	RW	11	Adapter detection debounce time **00**: 81 us **01**: 10 ms **10**: 20 ms **11**: 30 ms (Default)
1:0	ACOKDM[1:0]	RW	11	Adapter detection mode **00**: reserved **01**: low-to-high **10**: high-to-low **11**: both, low-to-high and high-to-low (Default)

8.5.24 VDLMTCRT Register (address = 0x51) [reset = 00000101]

Figure 51. VDLMTCRT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_VDLMTCRT	VDLMTCOMP	TDBNCVDLMTCRT[1]	TDBNCVDLMTCRT[0]	VDLMTCRTH[3]	VDLMTCRTH[2]	VDLMTCRTH[1]	VDLMTCRTH[0]
0	0	0	0	0	1	0	1
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. VDLMTCRT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_VDLMTCRT	RW	0	
6	VDLMTCOMP	RW	0	Critical supply voltage comparator for VDCSNS pin input voltage sense. Connect voltage divider resistors from VIN to detect when input voltage is low **0**: disable (Default) **1**: enable
5:4	TDBNCVDLMTCRT[1:0]	RW	00	Supply voltage monitor debounce of VDCSNS input voltage sense pin **00**: No Deglitch disable (Default) **01**: 10 us **10**: 1x RTC (30us) **11**: 2x RTC (60us)
3:0	VDLMTCRTH[3:0]	RW	0101	Critical supply voltage falling threshold on VDCSNS pin. Connect voltage divider resistors from VIN to detect when input voltage is low. For 2S should be 4X top resistor, X bottom resistor. [rising hysteresis = 20mV] **0000**: no limit **0001**: 1.2 V **0010**: 1.18 V **0011**: 1.16 V **0100**: 1.14 V **0101**: 1.12 V (Default) **0110**: 1.10 V **0111**: 1.08 V **1000**: NA **1001**: NA **1010**: NA **1011**: NA **1100**: NA **1101**: NA **1110**: NA **1111**: NA

8.5.25 SDWNCTRL Register (address = 0x49) [reset = 00000000]

Figure 52. SDWNCTRL Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_SDWNCTRL[6]	RESERVED_SDWNCTRL[5]	RESERVED_SDWNCTRL[4]	RESERVED_SDWNCTRL[3]	RESERVED_SDWNCTRL[2]	RESERVED_SDWNCTRL[1]	RESERVED_SDWNCTRL[0]	SDWN
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. SDWNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED_SDWNCTRL[6:0]	R	0000000	
0	SDWN	RW	0	Forced emergency reset, bit is self clearing **0**: No action **1**: Force emergency reset

8.5.26 RSTCTRL Register (address = 0x48) [reset = 00011100]

Figure 53. RSTCTRL Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_RSTCTRL[2]	RESERVED_RSTCTRL[1]	RESERVED_RSTCTRL[0]	TRST[1]	TRST[0]	VTHRST[2]	VTHRST[1]	VTHRST[0]
0	0	0	1	1	1	0	0
R	R	R	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED_RSTCTRL[2:0]	R	000	
4:3	TRST[1:0]	RW	11	Reset time duration **00**: 20 ms **01**: 40 ms **10**: 80 ms **11**: 200 ms (Default)
2:0	VTHRST[2:0]	RW	100	Reset voltage threshold **000**: 1.4 V **001**: 1.5 V **010**: 1.6 V **011**: 1.7 V **100**: 2.4 V (Default) **101**: 2.6 V **110**: 2.8 V **111**: 3.0 V

8.5.27 VRENPINMASK Register (address = 0x43) [reset = 00000000]

Figure 54. VRENPINMASK Register Format

B7	B6	B5	B4	B3	B2	B1	B0
MV12EN	MV11EN	MV10EN	MV9EN	MV8EN	MV7EN	MV5EN	MV4EN
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. VRENPINMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MV12EN	RW	0	V12 Enable Pin Mask **0**: VR Enable Pin controls VR enable (Default) **1**: VR Enable Pin masked V*CTLV controls VR enable
6	MV11EN	RW	0	V11 Enable Pin Mask **0**: VR Enable Pin controls VR enable (Default) **1**: VR Enable Pin masked V*CTLV controls VR enable
5	MV10EN	RW	0	V10 Enable Pin Mask **0**: VR Enable Pin controls VR enable (Default) **1**: VR Enable Pin masked V*CTLV controls VR enable
4	MV9EN	RW	0	V9 Enable Pin Mask **0**: VR Enable Pin controls VR enable (Default) **1**: VR Enable Pin masked V*CTLV controls VR enable
3	MV8EN	RW	0	V8 Enable Pin Mask **0**: VR Enable Pin controls VR enable (Default) **1**: VR Enable Pin masked V*CTLV controls VR enable
2	MV7EN	RW	0	V7 Enable Pin Mask **0**: VR Enable Pin controls VR enable (Default) **1**: VR Enable Pin masked V*CTLV controls VR enable
1	MV5EN	RW	0	V5 Enable Pin Mask **0**: VR Enable Pin controls VR enable **1**: VR Enable Pin masked V*CTLV controls VR enable
0	MV4EN	RW	0	V4 Enable Pin Mask **0**: VR Enable Pin controls VR enable (Default) **1**: VR Enable Pin masked V*CTLV controls VR enable

8.5.28 REGLOCK Register (address = 0x42) [reset = 00000000]

Figure 55. REGLOCK Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED[6]	RESERVED[5]	RESERVED[4]	RESERVED[3]	RESERVED[2]	RESERVED[1]	RESERVED[0]	CNTLOCK
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. REGLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED[6:0]	R	0000000	
0	CNTLOCK	RW	0	Locks all V*CNT registers **0**: All V*CNT registers are unlocked and can be overwritten (Default) **1**: All V*CNT registers are locked and can't be overwritten

8.5.29 VREN Register (address = 0x41) [reset = 00000000]

Figure 56. VREN Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_VREN[5]	RESERVED_VREN[4]	RESERVED_VREN[3]	RESERVED_VREN[2]	RESERVED_VREN[1]	RESERVED_VREN[0]	EC_SLP_S4	EC_DS4
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. VREN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED_VREN[5:0]	RW	000000	
1	EC_SLP_S4	RW	0	**0**: Disable (Default) **1**: Enable
0	EC_DS4	RW	0	**0**: Disable (Default) **1**: Enable

8.5.30 PWRGDCNT1 Register (address = 0x40) [reset = 01011111]

Figure 57. PWRGDCNT1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_PWRGDCNT1	RSMRSTN_PWRGD[1]	RSMRSTN_PWRGD[0]	PCH_PWROK[1]	PCH_PWROK[0]	DEL_ALL_SYS_PWRGD[2]	DEL_ALL_SYS_PWRGD[1]	DEL_ALL_SYS_PWRGD[0]
0	1	0	1	1	1	1	1
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. PWRGDCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_PWRGDCNT1	R	0	
6:5	RSMRSTN_PWRGD[1:0]	RW	10	Delay of RSMRSTN_PWRGD **00**: No Delay **01**: 164x RTC (about 5 ms) **10**: 328x RTC (about 10 ms) (Default) **11**: 656x RTC (about 20 ms)
4:3	PCH_PWROK[1:0]	RW	11	Delay of PCH_PWROK compared to ALL_SYS_PWRGD **00**: 82x RTC (about 2.5 ms) **01**: 164x RTC (about 5 ms) **10**: 328x RTC (about 10 ms) **11**: 656x RTC (about 20 ms) (Default)
2:0	DEL_ALL_SYS_PWRGD[2:0]	RW	111	Delay of SYS_PWR_OK compared to ALL_SYS_PWRGD **000**: 82x RTC (about 2.5 ms) **001**: 164x RTC (about 5 ms) **010**: 328x RTC (about 10 ms) **011**: 492x RTC (about 15 ms) **100**: 656x RTC (about 20 ms) **101**: 1640x RTC (about 50 ms) **110**: 2460x RTC (about 75 ms) **111**: 3280x RTC (about 100 ms) (Default)

8.5.31 DISCHCNT4 Register (address = 0x3F) [reset = 00000000]

Figure 58. DISCHCNT4 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_DISCHCNT4[1]	RESERVED_DISCHCNT4[0]	V33SDISCHG[1]	V33SDISCHG[0]	V18SDISCHG[1]	V18SDISCHG[0]	V100SDISCH[1]	V100SDISCH[0]
0	0	0	0	0	0	0	0
R	R	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. DISCHCNT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED_DISCHCNT4[1:0]	R	00	
5:4	V33SDISCHG[1:0]	RW	00	V3.3S discharge resistance (V6S) **00**:No discharge (Default) **01**: 100 Ohm **10**: 200 Ohm **11**: 500 Ohm
3:2	V18SDISCHG[1:0]	RW	00	V18S discharge resistance (V8S) **00**: No discharge (Default) **01**: 100 Ohm **10**: 200 Ohm **11**: 500 Ohm
1:0	V100SDISCH[1:0]	RW	00	V100S discharge resistance (V11S) **00**: No discharge (Default) **01**: 100 Ohm **10**: 200 Ohm **11**: 500 Ohm

8.5.32 DISCHCNT3 Register (address = 0x3E) [reset = 00000000]

Figure 59. DISCHCNT3 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V18U25UDISCHG[1]	V18U25UDISCHG[0]	V12UDISCHG[1]	V12UDISCHG[0]	V100ADISCHG[1]	V100ADISCHG[0]	V085ADISCH[1]	V085ADISCH[0]
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. DISCHCNT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V18U25UDISCHG[1:0]	RW	00	V1.8U_2.5U discharge resistance (V9) **00**: No discharge (Default) **01**: 100 Ohm **10**: 200 Ohm **11**: 500 Ohm
5:4	V12UDISCHG[1:0]	RW	00	V1.2U discharge resistance (V10) **00**: No discharge (Default) **01**: 100 Ohm **10**: 200 Ohm **11**: 500 Ohm
3:2	V100ADISCHG[1:0]	RW	00	V100A discharge resistance (V11) **00**: No discharge (Default) **01**: 100 Ohm **10**: 200 Ohm **11**: 500 Ohm
1:0	V085ADISCH[1:0]	RW	00	V085A discharge resistance (V12) **00**: No discharge (Default) **01**: 100 Ohm **10**: 200 Ohm **11**: 500 Ohm

8.5.33 DISCHCNT2 Register (address = 0x3D) [reset = 00000000]

Figure 60. DISCHCNT2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V5ADS3DISCHG[1]	V5ADS3DISCHG[0]	V33ADSWDISCHG[1]	V33ADSWDISCHG[0]	V33PCHDISCHG[1]	V33PCHDISCHG[0]	V18ADISCH[1]	V18ADISCH[0]
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. DISCHCNT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V5ADS3DISCHG[1:0]	RW	00	V5ADS3 discharge resistance (V5) **00**: No discharge (Default) **01**: 100 Ohm **10**: 200 Ohm **11**: 500 Ohm
5:4	V33ADSWDISCHG[1:0]	RW	00	V33A_DSW discharge resistance (V6) **00**: No discharge (Default) **01**: 100 Ohm **10**: 200 Ohm **11**: 500 Ohm
3:2	V33PCHDISCHG[1:0]	RW	00	V33PCH discharge resistance (V7) **00**: No discharge (Default) **01**: 100 Ohm **10**: 200 Ohm **11**: 500 Ohm
1:0	V18ADISCH[1:0]	RW	00	V18A discharge resistance (V8) **00**: No discharge (Default) **01**: 100 Ohm **10**: 200 Ohm **11**: 500 Ohm

8.5.34 DISCHCNT1 Register (address = 0x3C) [reset = 00000000]

Figure 61. DISCHCNT1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_DISCHCNT1[5]	RESERVED_DISCHCNT1[4]	RESERVED_DISCHCNT1[3]	RESERVED_DISCHCNT1[2]	RESERVED_DISCHCNT1[1]	RESERVED_DISCHCNT1[0]	VCCIODISCHG[1]	VCCIODISCHG[0]
0	0	0	0	0	0	0	0
R	R	R	R	R	R	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. DISCHCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED_DISCHCNT1[5:0]	R	000000	
1:0	VCCIODISCHG[1:0]	RW	00	VCCIO discharge resistance (V4) **00**: No discharge (Default) **01**: 100 Ohm **10**: 200 Ohm **11**: 500 Ohm

8.5.35 VRMODECTRL Register (address = 0x3B) [reset = 00111111]

Figure 62. VRMODECTRL Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_VRMODECTRL[1]	RESERVED_VRMODECTRL[0]	V33ADSW_LPM	VCCIO_LPM	V085A_LPM	V12U_LPM	V100A_LPM	V5ADS3_LPM
0	0	1	1	1	1	1	1
R	R	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. VRMODECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED_VRMODECTRL[1:0]	R	00	
5	V33ADSW_LPM	RW	1	Force low power mode (LPM mode) **0**: Force Auto mode when SLP_S0# is asserted (low) **1**: LPM & Mode set by CTLV bits, ignore SLP_S0# (Default)
4	VCCIO_LPM	RW	1	Force low power mode (Auto mode) **0**: Force Auto mode when SLP_S0# is asserted (low) **1**: Mode set by CTLV bits, ignore SLP_S0# (Default)
3	V085A_LPM	RW	1	Force low power mode (Auto mode) **0**: Force Auto mode when SLP_S0# is asserted (low) **1**: Mode set by CTLV bits, ignore SLP_S0# (Default)
2	V12U_LPM	RW	1	Force low power mode (LPM mode) **0**: Force Auto mode when DDR_VTT_CTRL is low **1**: LPM & Mode set by CTLV bits, ignore SLP_S0# (Default)
1	V100A_LPM	RW	1	Force low power mode (Auto mode) **0**: Force Auto mode when SLP_S0# is asserted (low) **1**: Mode set by CTLV bits, ignore SLP_S0# (Default)
0	V5ADS3_LPM	RW	1	Force low power mode (LPM mode) **0**: Force Auto mode when SLP_S0# is asserted (low) **1**: LPM & Mode set by CTLV bits, ignore SLP_S0# (Default)

8.5.36 V085ACNT Register (address = 0x38) [reset = 00101010]

Figure 63. V085ACNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V085ALVSEL[1]	V085ALVSEL[0]	V085AVSEL[1]	V085AVSEL[0]	AOACCNTV085A[1]	AOACCNTV085A[0]	CTLV085A[1]	CTLV085A[0]
0	0	1	0	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. V085ACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V085ALVSEL[1:0]	RW	00	V085A low power mode output voltage set point - set at assertion of SLP_S0# **00**: Disabled, voltage stays at value set by V085AVSEL[1:0] (Default) **01**: 0.70V **10**: 0.75V **11**: 0.80V
5:4	V085AVSEL[1:0]	RW	00	Output voltage select **00**: 0.95V (Default) **01**: 0.90V **10**: 0.85V **11**: 0.80V
3:2	AOACCNTV085A[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, forced PFM/ Auto **10**: Bits D[1:0] set to 10, forced Auto/ Forced PWM (Default) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLV085A[1:0]	RW	10	Mode control (V12) **00**: Converter disabled **01**: Forced PFM/ Auto **10**: Auto/ forced PWM enabled (If auto mode not present) (Default) **11**: Forced PWM operation

8.5.37 V100ACNT Register (address = 0x37) [reset = 00101010]

Figure 64. V100ACNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V100ALVSEL[1]	V100ALVSEL[0]	V100AVSEL[1]	V100AVSEL[0]	AOACCNTV100A[1]	AOACCNTV100A[0]	CTLV100A[1]	CTLV100A[0]
0	0	1	0	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. V100ACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V100ALVSEL[1:0]	RW	00	V100A low power mode output voltage set point - set at assertion of SLP_S0# **00**: Disabled, voltage stays at value set by V100AVSEL[1:0] (Default) **01**: Vnom - 4% **10**: Vnom - 3% **11**: Vnom - 2%
5:4	V100AVSEL[1:0]	RW	10	Output voltage select **00**: Vnom + 5 % (1.05V) **01**: Vnom (1 V) **10**: Vnom -2.5 % (0.975V) (Default) **11**: Vnom - 5 % (0.95V)
3:2	AOACCNTV100A[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, forced PFM/ Auto **10**: Bits D[1:0] set to 10, forced Auto/ Forced PWM (Default) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLV100A[1:0]	RW	10	Mode control (V11) **00**: Converter disabled **01**: Forced PFM/ Auto **10**: Auto/ forced PWM enabled (If auto mode not present) (Default) **11**: Forced PWM operation

8.5.38 V1P2UCNT Register (address = 0x36) [reset = 00111010]

Figure 65. V1P2UCNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V1P2ULVSEL	V1P2UVSEL[2]	V1P2UVSEL[1]	V1P2UVSEL[0]	AOACCNTV1P2U[1]	AOACCNTV1P2U[0]	CTLV1P2U[1]	CTLV1P2U[0]
0	0	1	1	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. V1P2UCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	V1P2ULVSEL	RW	0	V1.2U low power mode output voltage set point - set at assertion of SLP_S0# **0**: Disabled, voltage stays at value set by V1P2UVSEL (Default) **1**: Vnom - 3%
6:4	V1P2UVSEL[2:0]	RW	011	Output voltage select **000**: Vnom + 3% **001**: Vnom + 2% **010**: Vnom + 1% **011**: Vnom +0% (Default) **100**: Vnom - 1% **101**: Vnom -2% **110**: Vnom -3% **111**: Vnom -4%
3:2	AOACCNTV1P2U[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: no change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, forced PFM/ Auto **10**: Bits D[1:0] set to 10, forced Auto/ Forced PWM (Default) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLV1P2U[1:0]	RW	10	Mode control (V10) **00**: Converter disabled **01**: Forced PFM/ Auto **10**: Auto/ forced PWM enabled (If auto mode not present) (Default) **11**: Forced PWM operation

8.5.39 V18U25UCNT Register (address = 0x35) [reset = 00001010]

Figure 66. V18U25UCNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_V18U25UCNT[3]	RESERVED_V18U25UCNT[2]	RESERVED_V18U25UCNT[1]	RESERVED_V18U25UCNT[0]	AOACCNTV18U25U[1]	AOACCNTV18U25U[0]	CTLV18U25U[1]	CTLV18U25U[0]
0	0	0	0	1	0	1	0
R	R	R	R	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 41. V18U25UCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED_V18U25UCNT[3:0]	R	0000	
3:2	AOACCNTV18U25U[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01 **10**: Bits D[1:0] set to 10 (Default) **11**: Bits D[1:0] set to 11
1:0	CTLV18U25U[1:0]	RW	10	Mode control (V9) **00**: Disabled **01**: Enabled **10**: Enabled (Default) **11**: Enabled

8.5.40 V18ACNT Register (address = 0x34) [reset = 00101010]

Figure 67. V18ACNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V18ALVSEL[1]	V18ALVSEL[0]	V18AVSEL[1]	V18AVSEL[0]	AOACCNTV18A[1]	AOACCNTV18A[0]	CTLV18A[1]	CTLV18A[0]
0	0	1	0	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 42. V18ACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V18ALVSEL[1:0]	RW	00	V18A low power mode output voltage set point - set at assertion of SLP_S0# **00**: Disabled, voltage stays at value set by V18AVSEL[1:0] (Default) **01**: Vnom - 4% **10**: Vnom - 3% **11**: Vnom - 2%
5:4	V18AVSEL[1:0]	RW	10	Output voltage select **00**: Vnom + 3 % **01**: Vnom + 2 % **10**: Vnom (Default) **11**: Vnom - 2 %
3:2	AOACCNTV18A[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, forced PFM/ Auto **10**: Bits D[1:0] set to 10, forced Auto/ Forced PWM (Default) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLV18A[1:0]	RW	10	Mode control (V8) **00**: Converter disabled **01**: Forced PFM/ Auto **10**: Auto/ forced PWM enabled (If auto mode not present) (Default) **11**: Forced PWM operation

8.5.41 V33APCHCNT Register (address = 0x33) [reset = 00001010]

Figure 68. V33APCHCNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_V33APCHCNT[3]	RESERVED_V33APCHCNT[2]	RESERVED_V33APCHCNT[1]	RESERVED_V33APCHCNT[0]	AOACCNTV33APCH[1]	AOACCNTV33APCH[0]	CTLV33APCH[1]	CTLV33APCH[0]
0	0	0	0	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 43. V33APCHCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED_V33APCHCNT[3:0]	RW	0000	
3:2	AOACCNTV33APCH[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01 **10**: Bits D[1:0] set to 10 (Default) **11**: Bits D[1:0] set to 11
1:0	CTLV33APCH[1:0]	RW	10	Mode control (V7) **00**: Disabled **01**: Enabled **10**: Enabled (Default) **11**: Enabled

8.5.42 V33ADSWCNT Register (address = 0x32) [reset = 00101010]

Figure 69. V33ADSWCNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V33ADSWLVSEL[1]	V33ADSWLVSEL[0]	V33ADSWVSEL[1]	V33ADSWVSEL[0]	AOACCNTV33ADSW[1]	AOACCNTV33ADSW[0]	CTLV33ADSW[1]	CTLV33ADSW[0]
0	0	1	0	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 44. V33ADSWCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V33ADSWLVSEL[1:0]	RW	00	V33A_DSW low power mode output voltage set point - set at assertion of SLP_S0# **00**: Disabled, voltage stays at value set by V33ADSWVSEL[1:0] (Default) **01**: Vnom - 4% **10**: Vnom - 3% **11**: Vnom - 2%
5:4	V33ADSWVSEL[1:0]	RW	10	Output voltage select **00**: Vnom + 3 % **01**: Vnom + 2 % **10**: Vnom (Default) **11**: Vnom - 2 %
3:2	AOACCNTV33ADSW[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, forced PFM/ Auto **10**: Bits D[1:0] set to 10, forced Auto/ Forced PWM (Default) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLV33ADSW[1:0]	RW	10	Mode control (V6) **00**: Converter disabled **01**: Forced PFM/ Auto **10**: Auto/ forced PWM enabled (If auto mode not present) (Default) **11**: Forced PWM operation

8.5.43 V5ADS3CNT Register (address = 0x31) [reset = 00101010]

Figure 70. V5ADS3CNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V5ADS3LVSEL [1]	V5ADS3LVSEL [0]	V5ADS3VSEL[1]	V5ADS3VSEL[0]	AOACCNTV5A DS3[1]	AOACCNTV5A DS3[0]	CTLV5ADS3[1]	CTLV5ADS3[0]
0	0	1	0	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 45. V5ADS3CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V5ADS3LVSEL[1:0]	RW	00	V5ADS3 low power mode output voltage set point - set at assertion of SLP_S0# **00**: Disabled, voltage stays at value set by V5ADS3VSEL[1:0] (Default) **01**: Vnom - 4% **10**: Vnom - 3% **11**: Vnom - 2%
5:4	V5ADS3VSEL[1:0]	RW	10	Output voltage select **00**: Vnom + 3 % **01**: Vnom + 2 % **10**: Vnom (Default) **11**: Vnom - 2 %
3:2	AOACCNTV5ADS3[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, forced PFM/ Auto **10**: Bits D[1:0] set to 10, forced Auto/ Forced PWM (Default) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLV5ADS3[1:0]	RW	10	Mode control (V5) **00**: Converter disabled **01**: Forced PFM/ Auto **10**: Auto/ forced PWM enabled (If auto mode not present) (Default) **11**: Forced PWM operation

8.5.44 VCCIOCNT Register (address = 0x30) [reset = 00001010]

Figure 71. VCCIOCNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_VCCIOCNT	CSDECAYEN	VCCIOVSEL[1]	VCCIOVSEL[0]	AOACCNTVCCIO[1]	AOACCNTVCCIO[0]	CTLVVCCIO[1]	CTLVVCCIO[0]
0	0	0	0	1	0	1	0
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 46. VCCIOCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_VCCIOCNT	R	0	
6	CSDECAYEN	RW	0	Enables VCCIO decay when SLP_S0# is asserted. [wait 2us after removing FPWM, before entering DECAY mode. Direct FPWM to DECAY by SLP0Z may cause ringing. Decay exit time within 100us not guaranteed for Vout > 1V.] **0**: VCCIO stays at voltage set by VCCIOVSEL independent of state of SLP_S0# (Default) **1**: VCCIO decays to 0V, PGOOD is maintained when SLP_S0# is asserted (low)
5:4	VCCIOVSEL[1:0]	RW	00	Output voltage select **00**: 0.975V (Default) **01**: 0.950V **10**: 0.875V **11**: 0.850V
3:2	AOACCNTVCCIO[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, forced PFM/ Auto **10**: Bits D[1:0] set to 10, forced Auto/ Forced PWM (Default) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLVVCCIO[1:0]	RW	10	Mode control (V4) **00**: Converter disabled **01**: Forced PFM/ Auto **10**: Auto/ forced PWM enabled (If auto mode not present) (Default) **11**: Forced PWM operation

8.5.45 PGMASK2 Register (address = 0x19) [reset = 00000000]

Figure 72. PGMASK2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_PGMASK2[3]	RESERVED_PGMASK2[2]	RESERVED_PGMASK2[1]	RESERVED_PGMASK2[0]	V18U25UPG	MV12UPG	MV33SPG	MV18SPG
0	0	0	0	0	0	0	0
R	R	R	R	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 47. PGMASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED_PGMASK2[3:0]	R	0000	
3	V18U25UPG	RW	0	V1.8_2.5U PG is part of the power good tree **0**: Power Good function is enabled (Default) **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
2	MV12UPG	RW	0	V1.2U PG is part of the power good tree **0**: Power Good function is enabled (Default) **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
1	MV33SPG	RW	0	V3.3S PG is part of the power good tree **0**: Power Good function is enabled (Default) **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
0	MV18SPG	RW	0	V1.8S PG is part of the power good tree **0**: Power Good function is enabled (Default) **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)

8.5.46 PGMASK1 Register (address = 0x18) [reset = 00000000]

Figure 73. PGMASK1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
MVCCIOPG	MV085APG	MV100APG	MV18APG	MV33APCHPG	MV5ADS3PG	MV33ADSWPG	MV100SPG
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 48. PGMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MVCCIOPG	RW	0	VCCIO PG is part of the power good tree **0**: Power Good function is enabled (Default) **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
6	MV085APG	RW	0	V0.85A PG is part of the power good tree **0**: Power Good function is enabled (Default) **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
5	MV100APG	RW	0	V100A PG is part of the power good tree **0**: Power Good function is enabled (Default) **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
4	MV18APG	RW	0	V1.8A PG is part of the power good tree **0**: Power Good function is enabled (Default) **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
3	MV33APCHPG	RW	0	V3.3A PCH PG is part of the power good tree **0**: Power Good function is enabled (Default) **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
2	MV5ADS3PG	RW	0	V5A DS3 PG is part of the power good tree **0**: Power Good function is enabled (Default) **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
1	MV33ADSWPG	RW	0	V3.3A DSW PG is part of the power good tree **0**: Power Good function is enabled (Default) **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
0	MV100SPG	RW	0	V100S PG is part of the power good tree **0**: Power Good function is enabled (Default) **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)

8.5.47 PWRSTAT2 Register (address = 0x17) [reset = 00000000]

Figure 74. PWRSTAT2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED[5]	RESERVED[4]	RESERVED[3]	RESERVED[2]	RESERVED[1]	RESERVED[0]	V100A_FAULT	V085A_FAULT
0	0	0	0	0	0	0	0
R	R	R	R	R	R	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 49. PWRSTAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED[5:0]	R	000000	
1	V100A_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register (Default) **1**: Indicates power fault
0	V085A_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register (Default) **1**: Indicates power fault

8.5.48 PWRSTAT1 Register (address = 0x16) [reset = 00000000]

Figure 75. PWRSTAT1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
VCCIO_FAULT	V5A_DS3_FAULT	V33A_DSW_FAULT	V33A_PCH_FAULT	V18A_FAULT	V18U_25U_FAULT	V12U_FAULT	V06DX_FAULT
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 50. PWRSTAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VCCIO_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register (Default) **1**: Indicates power fault
6	V5A_DS3_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register (Default) **1**: Indicates power fault
5	V33A_DSW_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register (Default) **1**: Indicates power fault
4	V33A_PCH_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register (Default) **1**: Indicates power fault
3	V18A_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register (Default) **1**: Indicates power fault
2	V18U_25U_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register (Default) **1**: Indicates power fault
1	V12U_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register **1**: Indicates power fault
0	V06DX_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register (Default) **1**: Indicates power fault

8.5.49 PBSTATUS Register (address = 0x15) [reset = 00000000]

Figure 76. PBSTATUS Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_PBSTATUS	LVL	HT[5]	HT[4]	HT[3]	HT[2]	HT[1]	HT[0]
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 51. PBSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_PBSTATUS	R	0	
6	LVL	R	0	Power button present level **0**: Power button held (Default) **1**: Power button released
5:0	HT[5:0]	R	000000	Time that the button has been held **00000**: Disabled (Default) **00001**: Disabled **000010**: 2 s **000011**: 3 s **000100**: 4 s **000101**: 5 s **000110**: 6 s **000111**: 7 s **001000**: 8 s **001001**: 9 s **001010**: 10 s .. ... **111100**: 60 s **111101**: 61 s **111110**: 62 s **111111**: 63 s

8.5.50 PBCONFIG Register (address = 0x14) [reset = 00011111]

Figure 77. PBCONFIG Register Format

B7	B6	B5	B4	B3	B2	B1	B0
PWRBTNDBN	CLRHT	FLT[5]	FLT[4]	FLT[3]	FLT[2]	FLT[1]	FLT[0]
0	0	0	1	1	1	1	1
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 52. PBCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWRBTNDBN	RW	0	Power button debounce **0**: 30 ms (Default) **1**: 0 ms (no debounce)
6	CLRHT	RW	0	Reset of power button timer logic **0**: No action (Default) **1**: Reset of HT, bit is self clearing
5:0	FLT[5:0]	RW	011111	Time that the button must be held to force an emergency reset **000000**: 0 s **000001**: 1 s **000010**: 2 s **000011**: 3 s **000100**: 4 s **000101**: 5 s **000110**: 6 s **000111**: 7 s **001000**: 8 s **001001**: 9 s **001010**: 10 s .. **011111**: 31 s (Default) ... **111100**: 60 s **111101**: 61 s **111110**: 62 s **111111**: 63 s

8.5.51 IRQLVL1msK Register (address = 0x13) [reset = 10100101]

Figure 78. IRQLVL1msK Register Format

B7	B6	B5	B4	B3	B2	B1	B0
MRESET	RESERVED2_IRQLVL1msK	MPMU	RESERVED1_IRQLVL1msK[1]	RESERVED1_IRQLVL1msK[0]	MPWRSRC	RESERVED_IRQLVL1msK	MPWRBTN
1	0	1	0	0	1	0	1
RW	R	RW	R	R	RW	R	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 53. IRQLVL1msK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MRESET	RW	1	RESET mask interrupt **0**: Not masked **1**: Masked (Default)
6	RESERVED2_IRQLVL1msK	R	0	
5	MPMU	RW	1	Power monitor mask interrupt **0**: Not masked **1**: Masked (Default)
4:3	RESERVED1_IRQLVL1msK[1:0]	R	00	
2	MPWRSRC	RW	1	Power source mask interrupt **0**: Not masked **1**: Masked (Default)
1	RESERVED_IRQLVL1msK	R	0	
0	MPWRBTN	RW	1	Power button mask interrupt **0**: Not masked **1**: Masked (Default)

8.5.52 RESETIRQ2MASK Register (address = 0x12) [reset = 00000010]

Figure 79. RESETIRQ2MASK Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1_RESETIRQ2MASK[5]	RESERVED1_RESETIRQ2MASK[4]	RESERVED1_RESETIRQ2MASK[3]	RESERVED1_RESETIRQ2MASK[2]	RESERVED1_RESETIRQ2MASK[1]	RESERVED1_RESETIRQ2MASK[0]	MCRITTEMP	RESERVED_RESETIRQ2MASK
0	0	0	0	0	0	1	0
R	R	R	R	R	R	RW	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 54. RESETIRQ2MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED1_RESETIRQ2MASK[5:0]	R	000000	
1	MCRITTEMP	RW	1	Temperature triggered reset mask interrupt **0**: Not masked **1**: Masked (Default)
0	RESERVED_RESETIRQ2 MASK	R	0	

8.5.53 RESETIRQ1MASK Register (address = 0x11) [reset = 00110000]

Figure 80. RESETIRQ1MASK Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1_RESETIRQ1MASK[1]	RESERVED1_RESETIRQ1MASK[0]	MFCO	MVRFAULT	RESERVED_RESETIRQ1MASK[3]	RESERVED_RESETIRQ1MASK[2]	RESERVED_RESETIRQ1MASK[1]	RESERVED_RESETIRQ1MASK[0]
0	0	1	1	0	0	0	0
R	R	RW	RW	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 55. RESETIRQ1MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED1_RESETIRQ1MASK[1:0]	R	00	
5	MFCO	RW	1	Power button triggered reset mask interrupt **0**: Not masked **1**: Masked (Default)
4	MVRFAULT	RW	1	Voltage regulator triggered reset mask interrupt **0**: Not masked **1**: Masked (Default)
3:0	RESERVED_RESETIRQ1MASK[3:0]	R	0000	

8.5.54 MPWRSRCINT Register (address = 0x0C) [reset = 01111000]

Figure 81. MPWRSRCINT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1_MPWRSRCINT	MLOWBAT2	MLOWBAT1	MACOK	MPMICHOT	RESERVED_MPWRSRCINT[2]	RESERVED_MPWRSRCINT[1]	RESERVED_MPWRSRCINT[0]
0	1	1	1	1	0	0	0
R	RW	RW	RW	RW	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 56. MPWRSRCINT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED1_MPWRSRCINT	R	0	
6	MLOWBAT2	RW	1	Low battery voltage mask interrupt **0**: Not masked **1**: Masked (Default)
5	MLOWBAT1	RW	1	Low battery voltage mask interrupt **0**: Not masked **1**: Masked (Default)
4	MACOK	RW	1	AC/DC adapter detection mask interrupt **0**: Not masked **1**: Masked (Default)
3	MPMICHOT	RW	1	PMIC internal temperature mask interrupt **0**: Not masked **1**: Masked (Default)
2:0	RESERVED_MPWRSRCINT[2:0]	R	000	

8.5.55 MPMUINT Register (address = 0x0B) [reset = 00010100]

Figure 82. MPMUINT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED2_ MPMUINT[2]	RESERVED2_ MPMUINT[1]	RESERVED2_ MPMUINT[0]	MPMUACOK	RESERVED1_ MPMUINT	MPMUVDC	RESERVED_M PMUINT[1]	RESERVED_M PMUINT[0]
0	0	0	1	0	1	0	0
R	R	R	RW	R	RW	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 57. MPMUINT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED2_MPMUINT[2:0]	R	000	
4	MPMUACOK	RW	1	Power monitor critical supply voltage (adapter) mask interrupt **0**: Not masked **1**: Masked (Default)
3	RESERVED1_MPMUINT	R	0	
2	MPMUVDC	RW	1	Power monitor critical supply voltage mask interrupt **0**: Not masked **1**: Masked (Default)
1:0	RESERVED_MPMUINT[1:0]	R	00	

8.5.56 RESETIRQ2 Register (address = 0x09) [reset = 00000000]

Figure 83. RESETIRQ2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1[5]	RESERVED1[4]	RESERVED1[3]	RESERVED1[2]	RESERVED1[1]	RESERVED1[0]	CRITTEMP	RESERVED_R ESETIRQ2
0	0	0	0	0	0	0	0
R	R	R	R	R	R	RW	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 58. RESETIRQ2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED1[5:0]	R	000000	
1	CRITTEMP	RW	0	Temperature triggered reset interrupt **0**: Critical temperature not reached (Default) **1**: Critical temperature reached, forcing emergency shutdown
0	RESERVED_RESETIRQ2	R	0	

8.5.57 RESETIRQ1 Register (address = 0x08) [reset = 00000000]

Figure 84. RESETIRQ1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1_ RESETIRQ1[1]	RESERVED1_ RESETIRQ1[0]	FCO	VRFAULT	RESERVED[3]	RESERVED[2]	RESERVED[1]	RESERVED[0]
0	0	0	0	0	0	0	0
R	R	RW	RW	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 59. RESETIRQ1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED1_RESETIRQ1[1:0]	R	00	
5	FCO	RW	0	Power button triggered reset interrupt **0**: Power button counter has not forced an emergency reset (Default) **1**: Power button counter has forced an emergency reset
4	VRFAULT	RW	0	Voltage regulator triggered reset interrupt **0**: Voltage regulator fault has not triggered an emergency reset (Default) **1**: Voltage regulator fault has triggered an emergency reset
3:0	RESERVED[3:0]	R	0000	

8.5.58 PMUINT Register (address = 0x05) [reset = 00000000]

Figure 85. PMUINT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED2[2]	RESERVED2[1]	RESERVED2[0]	PMUACOK	RESERVED1_ PMUINT	PMUVDC	RESERVED_P MUINT[1]	RESERVED_P MUINT[0]
0	0	0	0	0	0	0	0
R	R	R	RW	R	RW	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 60. PMUINT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED2[2:0]	R	000	
4	PMUACOK	RW	0	Adapter detection interrupt **0**: No Interrupt Pending (Default) **1**: AC Adapter removed (SACOK H -> L)
3	RESERVED1_PMUINT	R	0	
2	PMUVDC	RW	0	Power monitor critical supply voltage interrupt **0**: Critical supply voltage over threshold limit (Default) **1**: Critical supply voltage below threshold limit
1:0	RESERVED_PMUINT[1:0]	R	00	

8.5.59 PWRSRCINT Register (address = 0x04) [reset = 00000000]

Figure 86. PWRSRCINT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1_PWRSRCINT	LOWBATT2	LOWBATT1	ACOK	PMICHOT	RESERVED[2]	RESERVED[1]	RESERVED[0]
0	0	0	0	0	0	0	0
R	RW	RW	RW	RW	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 61. PWRSRCINT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED1_PWRSRCINT	R	0	
6	LOWBATT2	RW	0	Low battery2 interrupt [rising-edge detect threshold =1.25V; falling-edge hysteresis = 125mV] **0**: No battery2 detected (Default) **1**: Battery2 detected
5	LOWBATT1	RW	0	Low battery1 interrupt [rising-edge detect threshold =1.25V; falling-edge hysteresis = 125mV] **0**: No battery1 detected (Default) **1**: Battery1 detected
4	ACOK	RW	0	AC/DC adapter detection interrupt. [rising-edge detect threshold =1.25V; falling-edge hysteresis = 125mV] **0**: No adapter detected (Default) **1**: Adapter detected
3	PMICHOT	RW	0	PMIC internal temperature interrupt **0**: PMIC temperature normal (Default) **1**: PMIC temperature hot
2:0	RESERVED[2:0]	R	000	

8.5.60 IRQLVL1 Register (address = 0x02) [reset = 00000000]

Figure 87. IRQLVL1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESET	RESERVED2	PMU	RESERVED1[1]	RESERVED1[0]	PWRSRC	RESERVED	PWRBTN
0	0	0	0	0	0	0	0
RW	R	RW	R	R	RW	R	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 62. IRQLVL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	R	0	RESET interrupt **0**: Not asserted **1**: Asserted
6	RESERVED2	R	0	
5	PMU	R	0	Power monitor interrupt **0**: Not asserted **1**: Asserted
4:3	RESERVED1[1:0]	R	00	
2	PWRSRC	R	0	Power source interrupt **0**: Not asserted **1**: Asserted
1	RESERVED	R	0	
0	PWRBTN	RW	0	Power button interrupt **0**: Not asserted **1**: Asserted, write '1' to clear

8.5.61 REVID Register (address = 0x01) [reset = 00000000]

Figure 88. REVID Register Format

B7	B6	B5	B4	B3	B2	B1	B0
MINREV[3]	MINREV[2]	MINREV[1]	MINREV[0]	MAJREV[3]	MAJREV[2]	MAJREV[1]	MAJREV[0]
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 63. REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MINREV[3:0]	RW	0000	Major revision ID **1010**: A **1011**: B **1100**: C **1101**: D **1110**: E **1111**: F
3:0	MAJREV[3:0]	RW	0000	Minor revision ID **0000**: 0 **0001**: 1 **0010**: 2 **0011**: 3 **0100**: 4 **0101**: 5 **0110**: 6 **0111**: 7

8.5.62 VENDORID Register (address = 0x00) [reset = 00100010]

Figure 89. VENDORID Register Format

B7	B6	B5	B4	B3	B2	B1	B0
VENDORID[7]	VENDORID[6]	VENDORID[5]	VENDORID[4]	VENDORID[3]	VENDORID[2]	VENDORID[1]	VENDORID[0]
0	0	1	0	0	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 64. VENDORID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VENDORID[7:0]	RW	00100010	Vendor ID: 0x22

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS65083x can be used in several different applications from computing, industrial interfacing and much more. This section describes the general application information and provides more detailed description on the TPS65083x powering the Intel SkyLake system.

9.2 Typical Applications

9.2.1 General Application

The TPS65083x can be used in any system that needs multiple voltage rails. A DC supply voltage in between 5.4V and 21V is required. If the supply voltage is less than this range then a small boost can be added to supply the VIN and VINLDO3.

Along with the 5 DCDCs and 1 LDO, the TPS65083x has 8 general purpose comparators, 2 level shifters, board temperature monitoring system and 3 power path comparators. latter 2 can be used as simple comparators if desired increasing the total comparators available for use to 12 on the TPS65083x.

Typical Applications (continued)

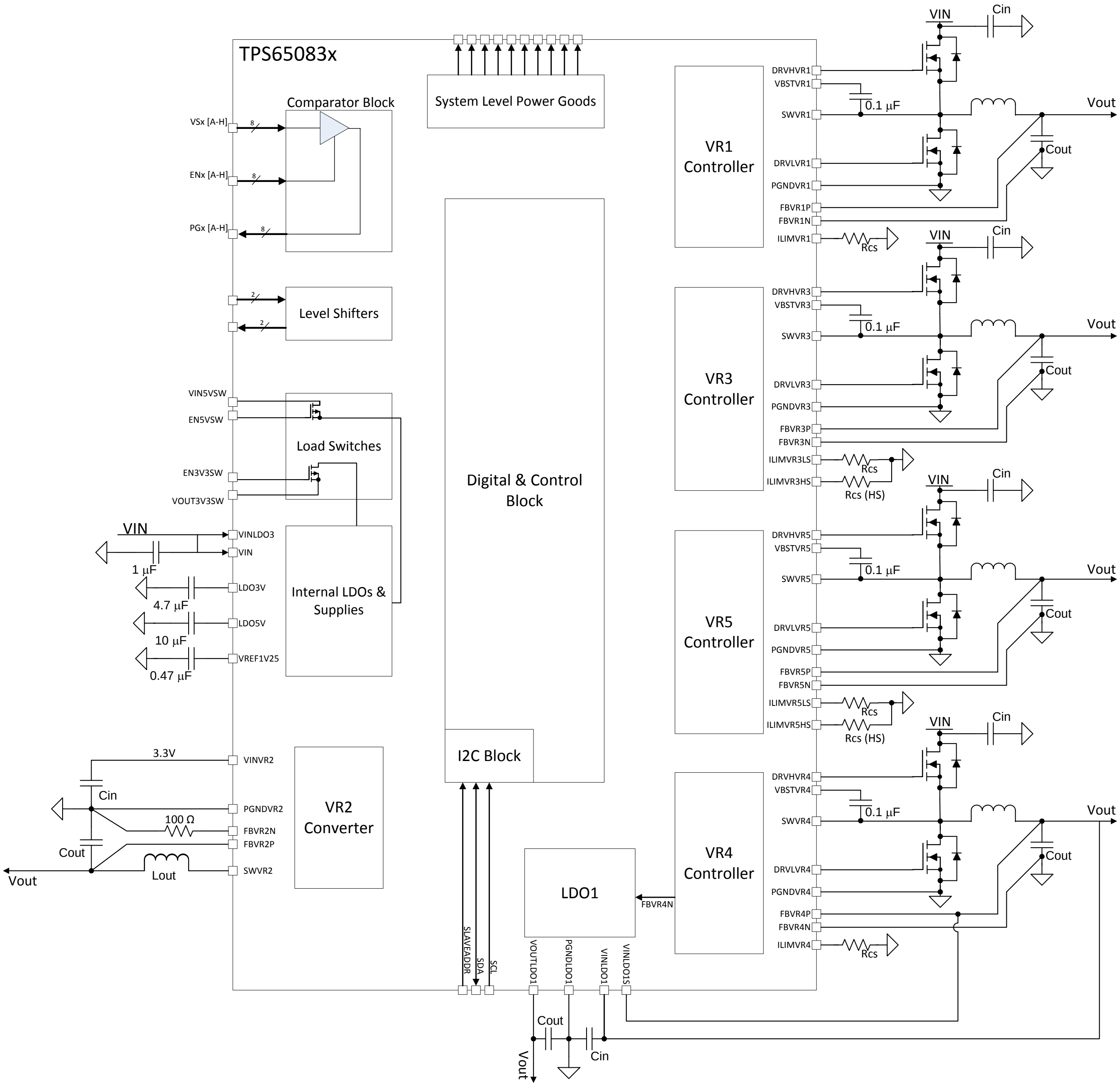


Figure 90. Simplifed General Block Diagram

9.2.1.1 Design Requirements

The TPS65083x requires decoupling caps on the supply pins. Follow the Electrical Characteristics for recommended capacitance on these supplies.

The controllers, converter, LDO, and some other features can be adujusted to meet the application needs. The following describes how to design and adjust the external components to achieve desired performances.

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Controller Design Procedure

Designing the controller breaks down into several steps: designing the output filter, selecting the FETs, bootstrap capacitor, and input capacitors and setting the current limits.

Controllers VR1 and VR4 require VREG supply and capacitors. VREG should be connected to the 5V LDO and a 1uF, X5R, 20%, 10V or similar capacitor should be used for decoupling.

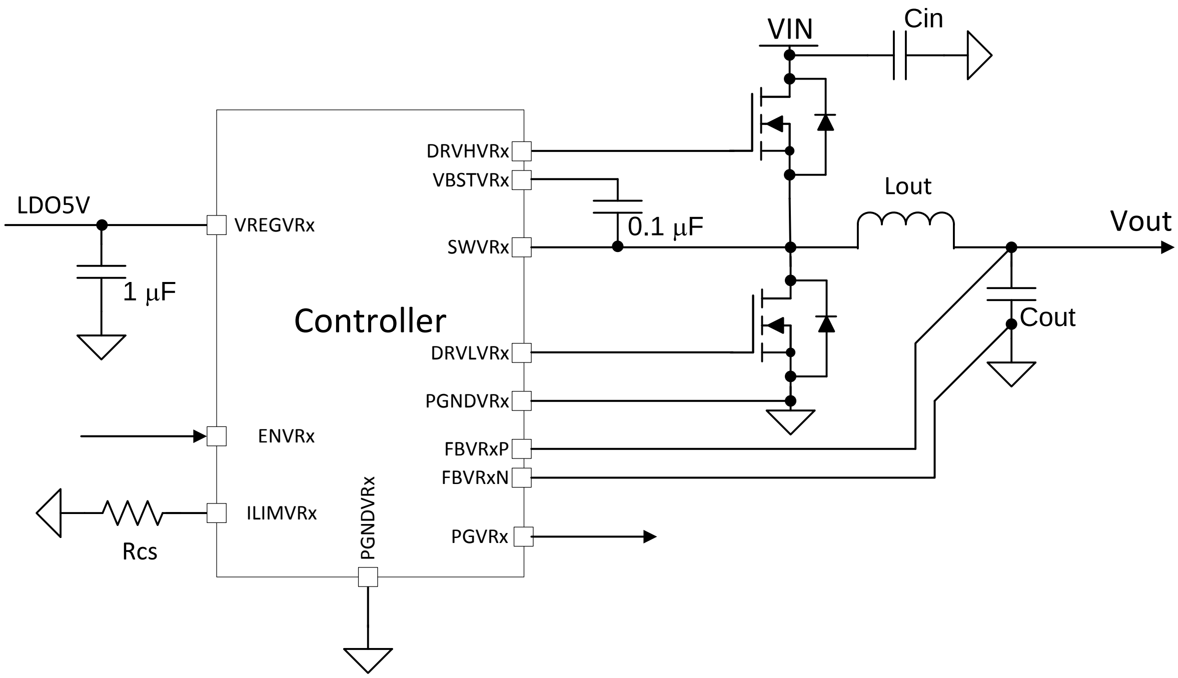


Figure 91. Controller Diagram

9.2.1.2.1.1 Selecting the Inductor

An inductor is required to be placed between the external FETs and the output capacitors. The inductor and output capacitors together make the double-pole which contributes towards stability. In addition, the inductor is directly responsible for the output ripple, efficiency, and transient performance. With an increase in inductance used the ripple current decreases which, typically increases efficiency. However, with an increase in inductance used, the transient performance decreases. Finally, the inductor selected has to be rated for appropriate saturation current, core losses and DC resistance (DCR).

Use the equation below to calculate the recommended inductance for the controller. Let K_{IND} be the ratio of $I_{Lripple}$ to the $Iout_{MAX}$. It is recommended that K_{IND} is set to a value between 0.2 and 0.4.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times Iout_{MAX} \times K_{IND}} \tag{2}$$

With the chosen inductance value, the peak current for the inductor in steady state operation, I_{Lmax}, can be calculated using the equation below. The rated saturation current of the inductor must be higher than the I_{Lmax} current.

$$I_{Lmax} = Iout_{max} + \left\{ \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{SW} \times L} \right\} \tag{3}$$

Following these equations the preferred inductor selected for the controllers are listed below in the Table 65.

Typical Applications (continued)

Table 65. Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	SIZE	HEIGHT
Cyntec	PIME031B	0.47 µH - 1 µH	3.3 mm x 3.7 mm	1.2 mm
Cyntec	PIMB041B	0.33 µH - 2.2 µH	4.45 mm x 4.75 mm	1.2 mm
Cyntec	PIMB051B	1 µH - 3.3 µH	5.4 mm x 5.75 mm	1.2 mm
Cyntec	PIME051E	0.33 µH - 4.7 µH	5.4 mm x 5.75 mm	1.5 mm
Cyntec	PIMB051H	0.47 µH - 4.7 µH	5.4 mm x 5.75 mm	1.8 mm
Cyntec	PIME061B	0.56 µH - 3.3 µH	6.8 mm x 7.3 mm	1.2 mm
Cyntec	PIME061E	0.33 µH - 4.7 µH	6.8 mm x 7.3 mm	1.5 mm
Cyntec	PIMB061H	0.1 µH - 4.7 µH	6.8 mm x 7.3 mm	1.8 mm

9.2.1.2.1.2 Selecting the Output Capacitors

Ceramic capacitors with low ESR values provide the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode. In order to achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC bias voltage.

For the output capacitors of the DCDC controller the use of a small ceramic capacitors placed as close as possible to the inductor and the respective PGND pins of the IC is recommended. This solution typically, provides the smallest and lowest cost solution available for DCAP2 controllers.

When selecting different output capacitance for the DCAP2 controller, use the equation below to determine the minimum Cout required for stability of the controller.

$$C_{OUT} > \frac{V_{OUT} \times 9}{V_{IN} \times f_{SW} \times L} \times 10^{-6} \quad (4)$$

Following this criteria, it is recommended to use listed capacitors in or similar capacitors.

9.2.1.2.1.3 Selecting the FETs

This controller is designed to drive NMOS FETs. Typically, the lower R_{DSon} for the high and low side FETs the better but, be sure to size the FETs, inductor and output capacitors appropriately as the R_{DSon} for the low side FET decreases, the minimum current limit increases. The Texas Instruments CSD87381P is recommended for the controllers.

9.2.1.2.1.4 Bootstrap Capacitor

To make sure that the internal high side gate drivers are supplied with a stable low noise supply voltage, a capacitor must be connected between the VBSTVRx pins and the respective SWVRx pins. Using ceramic capacitors with the value of 0.1 µF are recommended for the converters and the controllers, respectfully. For testing, a 0.1 µF, size 0402, 10 V capacitor was used for the controllers.

It is recommended to reserve a small resistor in series with the bootstrap capacitor in case the turn on / off of the FETs need to be slowed in order to reduce voltage ringing on the switch node. This is common practice for controller design.

9.2.1.2.1.5 Setting the Current Limits

The controller has a Valley Current Limit topology, also known as a Low Side Current Limit. This type of current limit works by limiting the current only when the low side FET is on. If the current being sourced by the low side FET is greater than the set low side current limit, I_{LS}, the controller will hold the low side FET on and the high side off until the current through the low side FET decreases below the set I_{LS}. Only if the current through the low side FET is less than the I_{LS} will the low side FET be allowed to turn off and the high side FET to turn on.

A fast current increase is limited by the maximum on time for the high side FET. This forces the low side FET to turn on every period. Once the low side FET turns on, the Low Side Current Limit can control the FETs until the current decreases below the I_{LS}. The maximum on time for the high side FET limits the current increase to maximum on time multiplied by the di/dt of the inductor until the low side FET is switched on.

I_{OCL} is the average current when the valley current is consistently the I_{LS}.

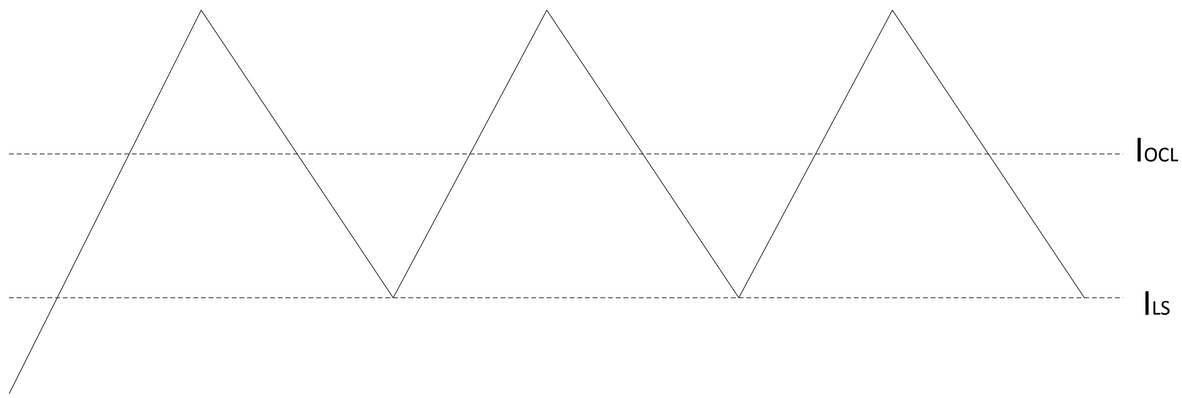


Figure 92. I_{OCL} Depiction

The low side current limit for the controllers is set by a resistor, R_{CS}, at the I_{LIMx} pin. A current, I_{TRIP}, is sourced across the R_{CS} to set the voltage for the current limit comparator. Use the equation below to determine the R_{CS} resistor. It is recommended to set I_{OCL} to 130% of I_{OUTmax} and use a resistor with ±1% or less tolerance for best results. Since the current limit is when the inductor current is near its maximum it is recommended to use the saturation derating of the inductor when calculating the R_{CS}.

$$R_{CS} = \frac{8 \times R_{DS_{on}} \times (I_{OCL} - \frac{(V_{in} - V_{out}) \times V_{out}}{2 \times L \times f_{sw} \times V_{in}})}{I_{TRIP}} \quad (5)$$

There is a minimum and a maximum I_{OCL} that can be achieved for the given parameters used in the equation above. To ensure that the R_{CS} has been sized correctly, the following equation must be true across the application temperature range.

$$V_{CSmin} < I_{TRIP} \times R_{CS} < V_{CSmax} \quad (6)$$

If the controller has high side current limit then, use Equation 7 to calculate the high side R_{CS} resistor. The high side current limit must be set higher than the low side current limit. Again, since the current limit is when the inductor current is near its maximum it is recommended to use the saturation derating of the inductor when calculating the R_{CS}.

$$R_{CS\,(HS)} = \frac{\left(\frac{\left(R_{DSon} \times \left(I_{OCL} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}}\right)\right)}{3200\Omega} - 8\mu A\right) \times 20k\Omega}{I_{TRIP}} \quad (7)$$

9.2.1.2.1.6 Selecting the Input Capacitors

Because of the nature of the switching converter and controller with a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For the controller, 12µF of input capacitance is recommended for most applications. To achieve the low ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC bias characteristic of ceramic capacitors need to be considered. The input capacitor can be increased without any limit for better input voltage filtering. Be sure to size the ceramic capacitor to achieve the recommended input capacitance. A ceramic capacitor placed as close as possible to the respective VINx and PGNDx pins of the FETs is recommended.

The preferred capacitors for the controllers are two muRata GRM21BR61E106MA73: 10 µF, 0805, 25 V, +/-20% or similar.

9.2.1.2.2 Converter Design Procedure

Designing the converter has only 2 steps: designing the output filter and selecting the input capacitors. The converter must be supplied by a 3.3V source which can be provided by one of the TPS65083x controllers.

The converter requires VREG supply and capacitors. VREG should be connected to the 5V LDO and a 1uF, X5R, 20%, 10V or similar capacitor should be used for decoupling.

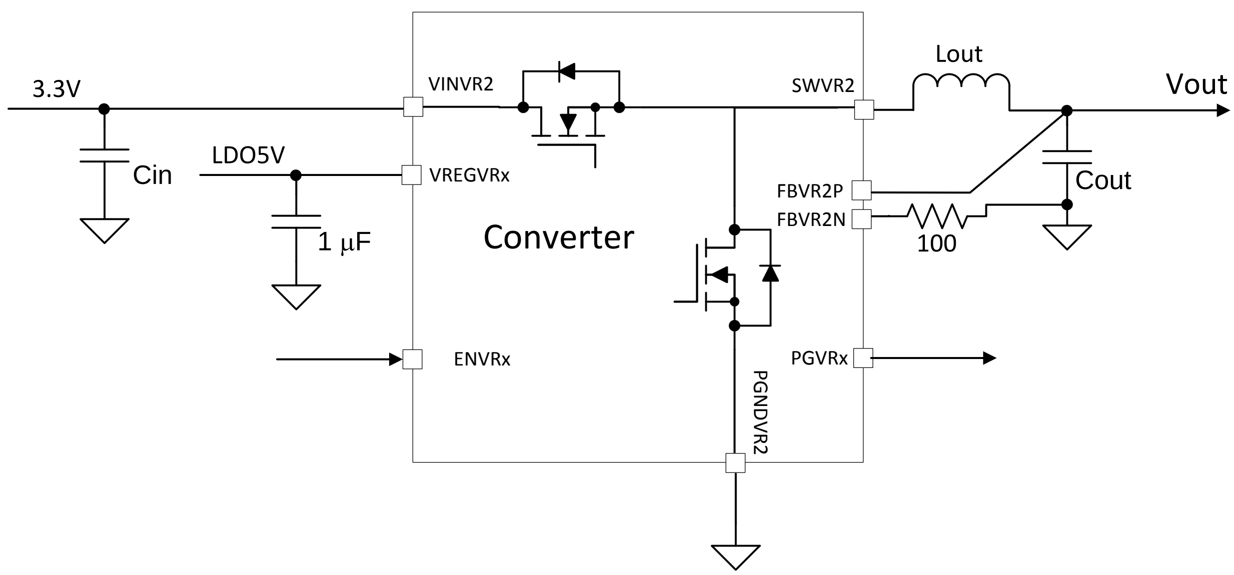


图 93. Converter Diagram

9.2.1.2.2.1 Selecting the Inductor

An inductor is required to be placed between the SWVRx and the output capacitors. The inductor and output capacitors together make the double-pole which contributes towards stability. In addition, the inductor is directly responsible for the output ripple, efficiency, and transient performance. With an increase in inductance used the ripple current decreases which, typically increases efficiency. However, with an increase in inductance used, the transient performance decreases. Finally, the inductor selected has to be rated for appropriate saturation current, core losses and DC resistance (DCR).

Use the equation below to calculate the recommended inductance for the controller. Let K_{IND} be the ratio of $I_{Lripple}$ to the $Iout_{MAX}$. It is recommended that K_{IND} is set to a value between 0.2 and 0.4.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times Iout_{MAX} \times K_{IND}} \tag{8}$$

With the chosen inductance value, the peak current for the inductor in steady state operation, I_{-Lmax} , can be calculated using the equation below. The rated saturation current of the inductor must be higher than the I_{Lmax} current.

$$I_{Lmax} = Iout_{max} + \left\{ \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{SW} \times L} \right\} \quad (9)$$

Following these equations the preferred inductors selected for the converter are listed below in the Table 66.

Table 66. Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	SIZE	HEIGHT
Cyntec	PIFE32251B-R68MS	0.68 µH	3.2 mm x 2.5 mm	1.2 mm
Würth	744383230068	0.68 µH	2.5 mm x 2 mm	1.0 mm

9.2.1.2.2.2 Selecting the Output Capacitors

Ceramic capacitors with low ESR values provide the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode. In order to achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC bias voltage.

For the output capacitors of the DCDC converters the use of a small ceramic capacitors placed as close as possible to the inductor and the respective PGND pins of the IC is recommended. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the inductor and the respective PGND pins of the IC.

At the DCDC converters the recommended capacitor for use is the muRata GRM188R60J226MEAO: 22 µF, 0603, 6.3 V, ±20% or similar. This capacitor was selected to achieve the highest derated capacitance in a small 0603 package. If the selected output voltage is greater than 3.3V then the muRata GRM21BR61A226ME44: 22µF, 0805, 10V, ± 20%, or similar is recommended for use. This capacitor is recommended to maintain the actual capacitance as DC bias increases.

9.2.1.2.2.3 Selecting the Input Capacitors

Because of the nature of the switching converter and controller with a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For the controller, 12µF of input capacitance is recommended for most applications. To achieve the low ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC bias characteristic of ceramic capacitors need to be considered. The input capacitor can be increased without any limit for better input voltage filtering. Be sure to size the ceramic capacitor to achieve the recommended input capacitance. A ceramic capacitor placed as close as possible to the respective VINx and PGNDx pins of the IC is recommended.

The preferred capacitors for the controllers are two muRata GRM21BR61E106MA73: 10 µF, 0805, 25 V, +/-20% or similar.

9.2.1.2.3 LDO Design Procedure

The LDO must handle the fast load transients from the DDR memory for termination. Therefore, it is important to maintain a high amount of capacitance with low ESR on the LDO outputs and inputs. Ceramic capacitors are ideal for this. Below is the recommended capacitors.

The preferred output capacitor for the LDO is muRata GRM188R60J476M: 47 µF, 0603, 6.3 V, +/-20% or similar.

The preferred input capacitor for the LDO is muRata GRM155R60J106ME44: 10 µF, 0402, 6.3 V, +/-20% or similar.

9.2.1.2.4 Board Temperature Monitoring Design Procedure

Board temperature monitoring requires only 1 thermistor if only 1 sense point is desired. It can be scaled by adding as many thermistors as sense points desired. Simply connect a PTC thermistor that has an exponential coefficient curve from the VCOMP pin to GND and a pull up to desired voltage source on the TRIPZ pin. Place thermistor where desired. If multiple sense points are desired string the thermistors together in a series connection while placing the thermistors where desired.

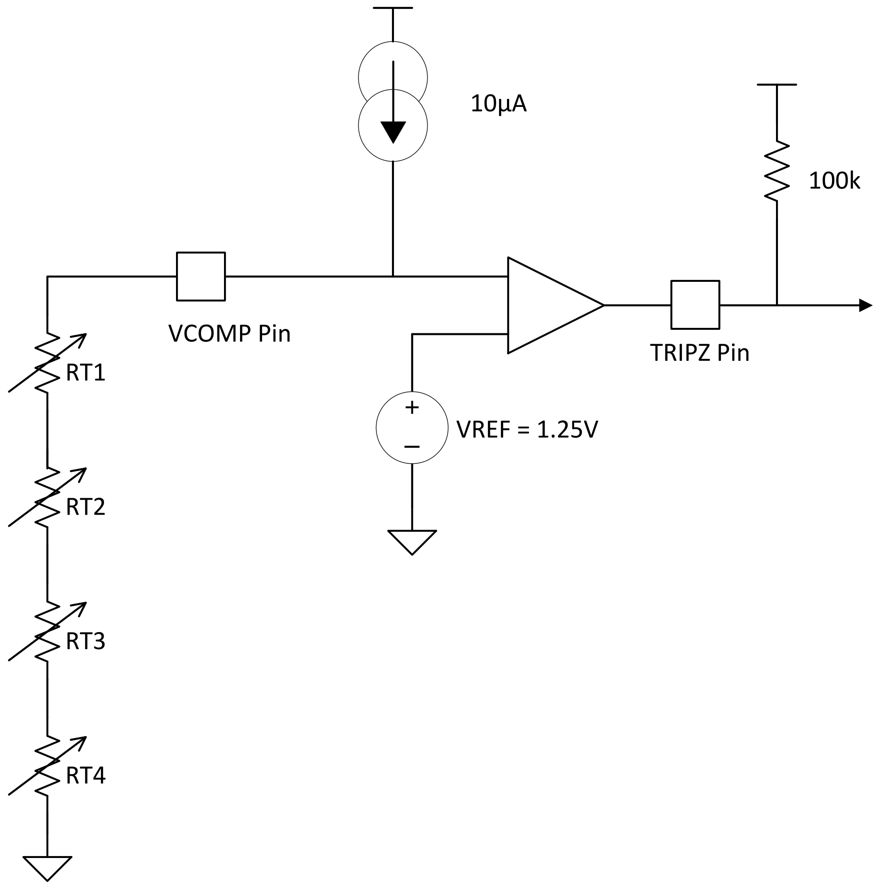


图 94. Board Temperature Monitoring Circuit Example

The thermistors should have low room and mid temperature resistances in the range of 1kΩ to 10kΩ. The hot point resistance should be roughly 10x mid temperature resistance in the range of 100kΩ to 200kΩ. There is an internal 10µA current source that provides a voltage across the thermistors. Once this voltage exceeds the comparator thershold of 1.25V the TRIPZ pin switches to LOW indicating a HOT board temperature. Therefore, the resistance required for HOT board temperature is 125kΩ. Select thermistors that align this resistance with the desired HOT temperature setpoint.

The recommended thermistors for this feature is the muRata PRF15BG102RB6RC.

9.2.1.2.5 Sequencing the Voltage Rails

To sequence the voltage rails of the PMIC, the power goods of the VRs and PG comparators can be feed back into the enables for the VRs and comparators. RC delays can be added externally the PMIC can be programmed to have delays set internally.

9.2.1.2.6 Power Path Design Procedure

The TPS65083x has power path comparators and outputs to control the power path switches. Simiply connect a voltage divider to the adaptor and batteries to set the threshold to the desired value. The outputs of the comparators require a pull up since they are open-drain outputs. In-order for the power path comparators to work without VIN supplied connect the VINPP to the power rails that are being monitored by using a diode to select the highest voltage among the sources.

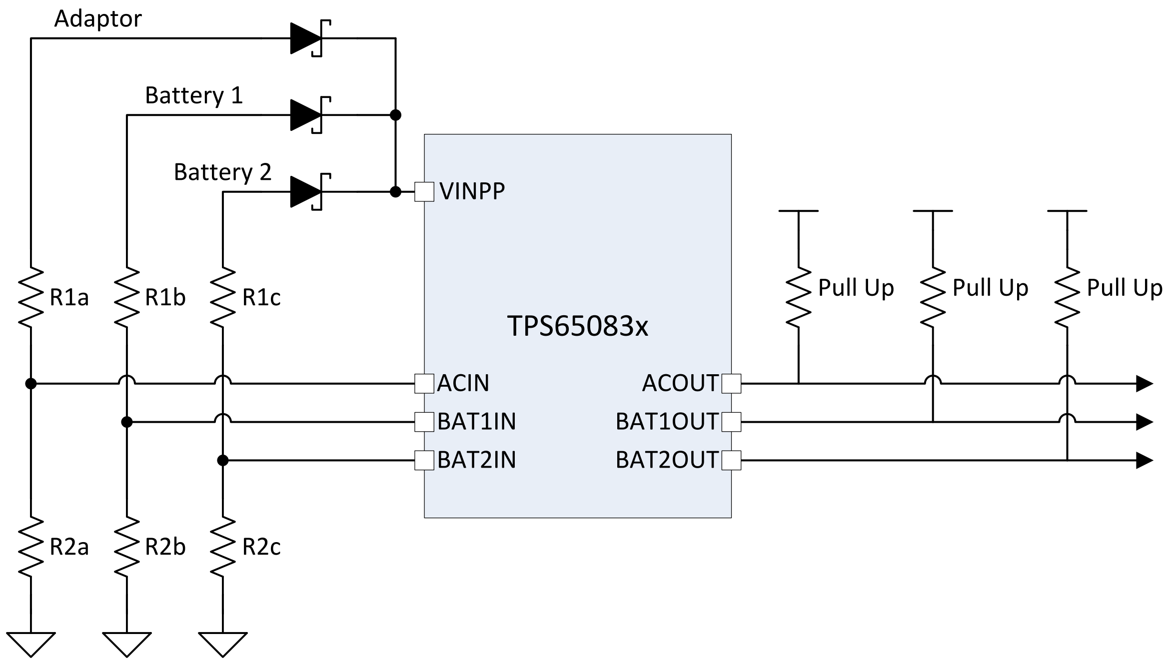


图 95. Power Path Comparators and VINPP Supply

Example:

Desired is to measure a battery and an adaptor to decide when to switch over from battery to adaptor. The votlages desired for thresholds are 9V and 6V respectively. Using 公式 10 the resistors required to set the 9V threshold are R1a = and R2a = . The resistors required to set the 6V threshold are R1b = and R2b = .

$$R_1 = R_2 \times \left(\frac{V_{IN}}{V_{Threshold}} - 1\right) \tag{10}$$

9.2.1.3 Application Performance Curves

表 67. Application Curves Overview

TYPE	DESCRIPTION AND ASSUMPTIONS	FIGURE NUMBER
Efficiency VR1	Using CSD87381P FET Block, PIME051H-1R0MS, 3 x GRM31CR60G227ME11 + 1 x GRM21BR60J107M, NDVCZ = HIGH, **Vout = 1V**	图 96
Efficiency VR2	Using PIFE32251B-R68MS, 4 x ZRB18AR60G476ME01, NDVCZ = HIGH, **Vout = 1.8V**	图 97
Efficiency VR3	Using CSD87381P FET Block, PIMB061H-1R5MS, 3 x GRM21BR60J107M , NDVCZ = HIGH, **Vout = 3.3V**	图 98
Efficiency VR4	Using CSD87381P FET Block, PIME051H-1R0MS, 2 x GRM31CR60G227ME11 + 1 x GRM21BR60J107M, NDVCZ = HIGH, **Vout = 1.2V**	图 99
Efficiency VR5	Using CSD87381P FET Block, PIMB051H-3R3MS, 11 x GRM21BR61A476ME15, NDVCZ = HIGH, **Vout = 5V**	图 100

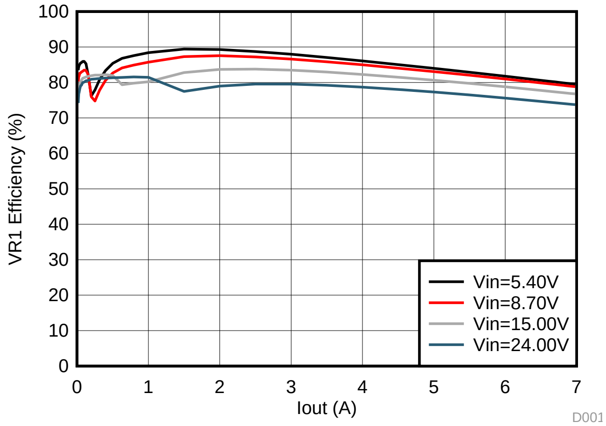


图 96. Typical Efficiency for VR1

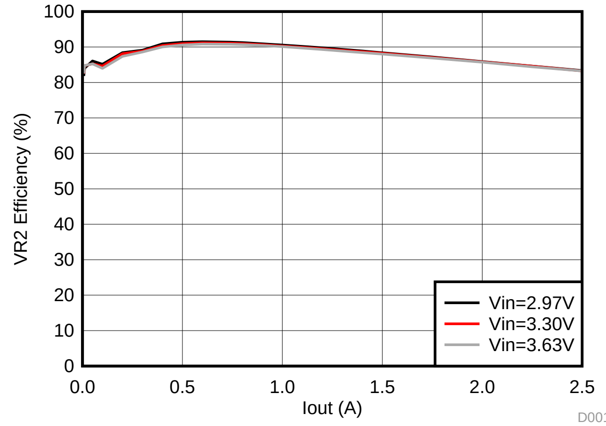


图 97. Typical Efficiency for VR2

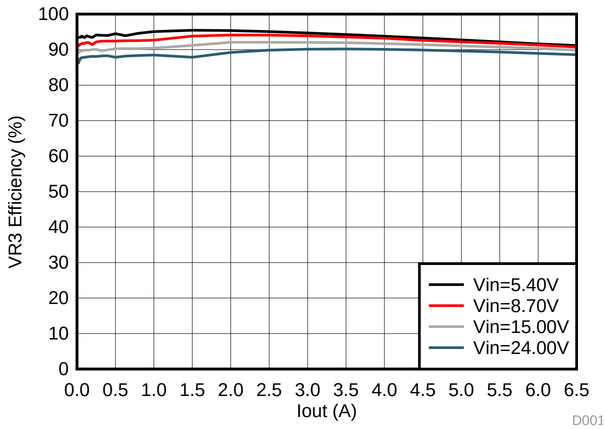


图 98. Typical Efficiency for VR3

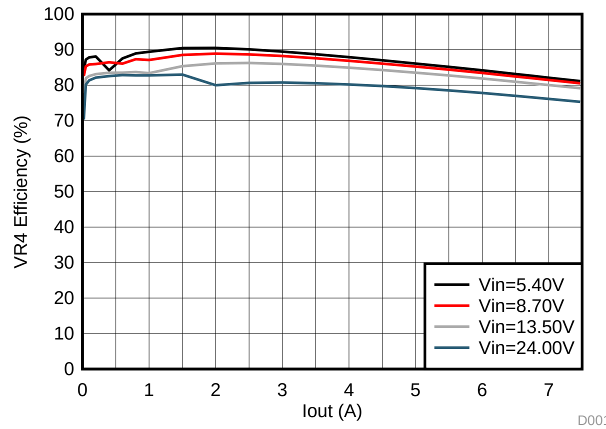


图 99. Typical Efficiency for VR4

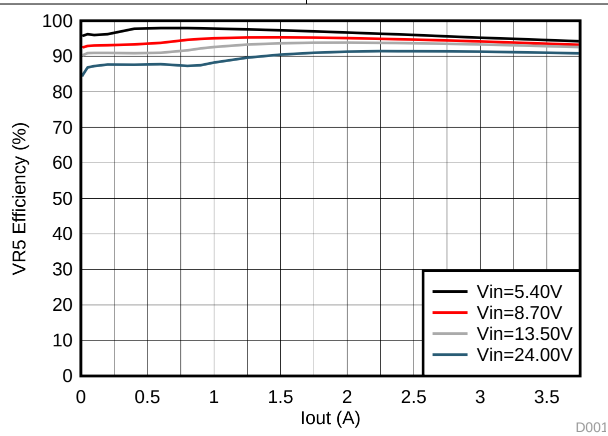
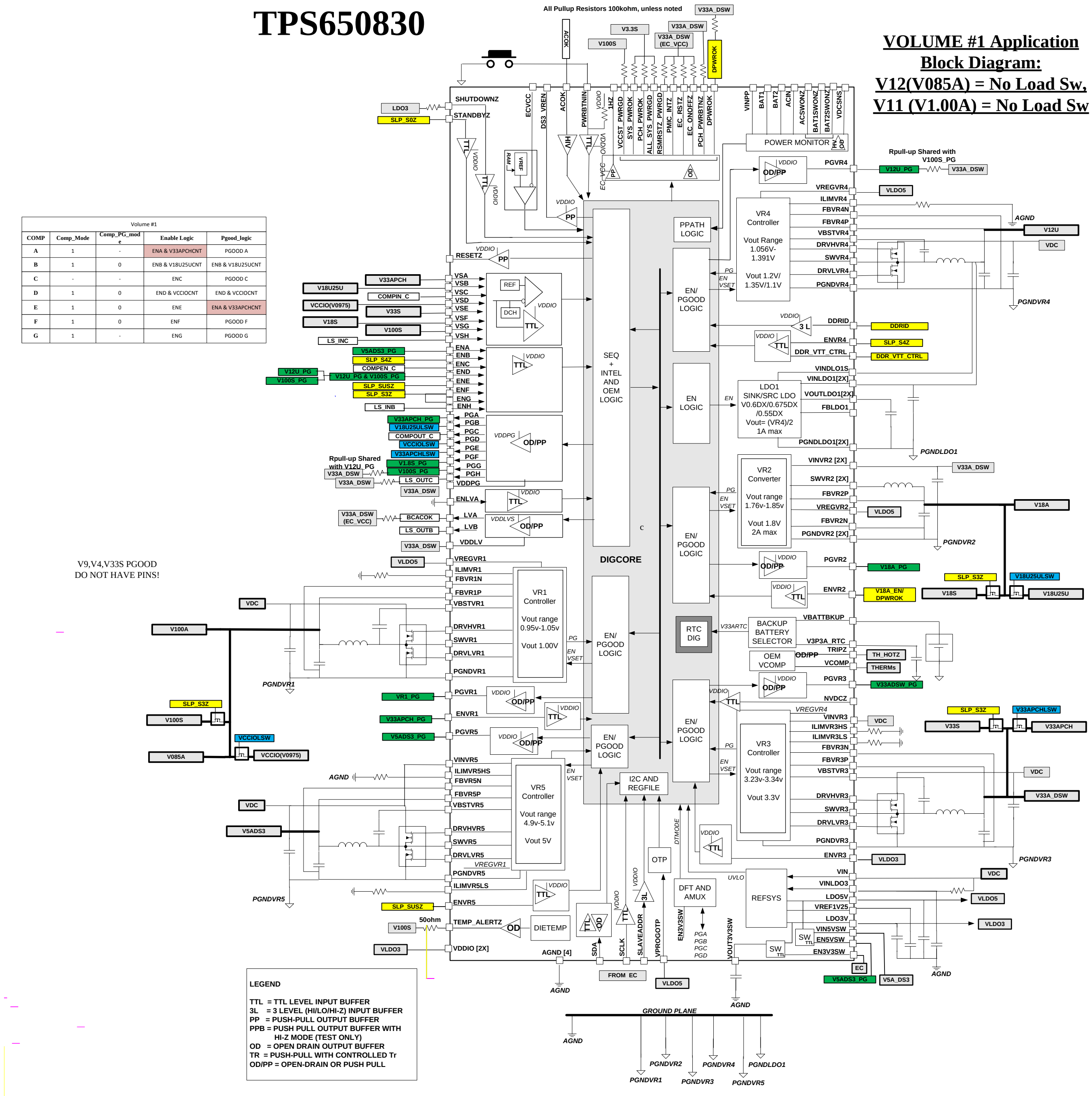


图 100. Typical Efficiency for VR5

9.2.2 Specific Application - TPS650830 Powering the Intel SkyLake Platform Volume Configuration

Volume configuration is the lowest cost and smallest solution for SkyLake power. It combines multiple same voltage rails into one rail reducing cost and size. Load switches are utilized to separate the rails and power the system with correct sequencing. The PMIC controls these load switches with the power good comparators. The TPS65083x also supports Premium configurations, see TPS650831 and TPS650832 or literature numbers: SLVSCS5 and SLVSCS6.



Volume #1				
COMP	Comp_Mode	Comp_PG_mode	Enable Logic	Pgood_logic
A	1	-	ENA & V33APCHCNT	PGOOD A
B	1	0	ENB & V18U25UCNT	ENB & V18U25UCNT
C	-	-	ENC	PGOOD C
D	1	0	END & VCCIOCNT	END & VCCIOCNT
E	1	0	ENE	ENA & V33APCHCNT
F	1	0	ENF	PGOOD F
G	1	-	ENG	PGOOD G

图 101. TPS650830 Volume Application Diagram

9.2.2.1 Design Requirements

The deisgn requirements are set by the Intel SkyLake Platform. Below are the requirements of the power supply system. This procedure assumes the system is a 2S NVDC system but, the TPS65083x supports 3S NVDC, as well as non-NVDC systems. 2S NVDC system has an input voltage range of 5.4V to 8.7V.

- There must be 9 separate voltage rails:
  - V5A_DS3 - 5V, I_{MAX} = 3.5A
  - V3.3A_DSW - 3.3V, I_{MAX} = 3.5A
  - V3.3A_PCH - 3.3V, I_{MAX} = 3A

  - V1.00A - 1.0V, I_{MAX} = 4.9A
  - VCCIO - 1.0V, I_{MAX} = 2.9A
  - V1.8A - 1.8V, I_{MAX} = 1A
  - V1.8U - 1.8V, I_{MAX} = 1A
  - VDDQ - 1.2V, I_{MAX} = 7.5A
  - VTT - 0.6V, I_{MAX} = ±1A
- All rails must have maximum tolerance of ±5% of the nominal voltage at all times with load transients.
  - Load Transients are defined as 0% to 70%, 70% to 0%, 30% to 100% and 100% to 30% load current steps relative of the I_{MAX} current defined for each rail.
- Maximum height of components = 1.8 mm.
- Sequence in the order below:
  - V3.3A_DSW with VIN supplied
  - V1.8A with VIN supplied
  - V5A_DS3 with SLP_SUS# transition to HIGH
  - V3.3A_PCH with SLP_SUS# transition to HIGH
  - V1.00A with SLP_SUS# transition to HIGH
  - VDDQ with SLP_S4# transition to HIGH
  - V1.8U with SLP_S4# transition to HIGH
  - VCCIO with SLP_S3# transition to HIGH
  - VTT with DDR_VTT_CTRL / SLP_S0# transition to HIGH

9.2.2.2 Detailed Design Procedure

The TPS650830 supplies 6 voltage rails and controls 3 load switches to meet the sequence order for the V3.3A_PCH, V1.8U, and VCCIO rails.

- VR1 supplies the V1.00A rail and the VCCIO rail with a load switch.
- VR2 supplies the V1.8A rail and the V1.8U rail with a load switch.
- VR3 supplies the V3.3A_DSW rail and the V3.3A_PCH rail with a load switch.
- VR4 supplies the VDDQ rail and the VINLDO1 for termination.
- VR5 supplies the V5A_DS3 rail.
- VLDO1 supplies the VTT rail.

To meet the sequencing requirement the power goods of the VRs and PG comparators are feed back into the enables for the VRs and comparators. The 5 external control signals SLP_SUS#, _S4#, _S3#, _S0#, and DDR_VTT_CTRL are responsible for transitioning the system from sleep state to sleep state and the reverse sequencing.

Since, the requirements are for a 2S NVDC system the NVDCZ pin should be tied LOW.

9.2.2.2.1 Output Inductance and Capacitance

Following the recommend design procedure in Detailed Design Procedure will yield output inductance and capacitance similar to 表 68.

表 68. SkyLake Volume Configuration Output L and C

VRx	OUTPUT INDUCTANCE	MINIMUM OUTPUT CAPACITANCE	RECOMMENDED OUTPUT CAPACITORS	CAPACITOR MANUFACTURER
VR1	0.56 µH	160 µF	1 x GRM31CR60G227ME11 and 1 x ZRB18AR60G476ME01	muRata
VR2	0.68 µH	47 µF	4 x ZRB18AR60G476ME01	muRata
VR3	1 µH	87 µF	2 x GRM31CR60G227ME11	muRata
VR4	0.56 µH	117 µF	1 x GRM31CR60G227ME11	muRata
VR5	2.2 µH	76 µF	8 x GRM21BR61A476ME15	muRata

9.2.2.3 Application Performance Curves

表 69. Application Curves Overview

TYPE	DESCRIPTION AND ASSUMPTIONS	FIGURE NUMBER
Efficiency VR1	Using CSD87381P FET Block, PIMB051H-0R56M, 1 x GRM31CR60G227ME11 + 1 x ZRB18AR60G476ME01, NDVCZ = LOW, **Vout = 1V**	图 102
Efficiency VR2	Using PIFE32251B-R68MS, 4 x ZRB18AR60G476ME01, NDVCZ = LOW, **Vout = 1.8V**	图 103
Efficiency VR3	Using CSD87381P FET Block, PIME051H-1R0MS, 2 x GRM31CR60G227ME11, NDVCZ = LOW, **Vout = 3.3V**	图 104
Efficiency VR4	Using CSD87381P FET Block, PIMB051H-0R56M, 1 x GRM31CR60G227ME11, NDVCZ = LOW, **Vout = 1.2V**	图 105
Efficiency VR5	Using CSD87381P FET Block, PIME051B-2R2MS, 8 x GRM21BR61A476ME15, NDVCZ = LOW, **Vout = 5V**	图 106

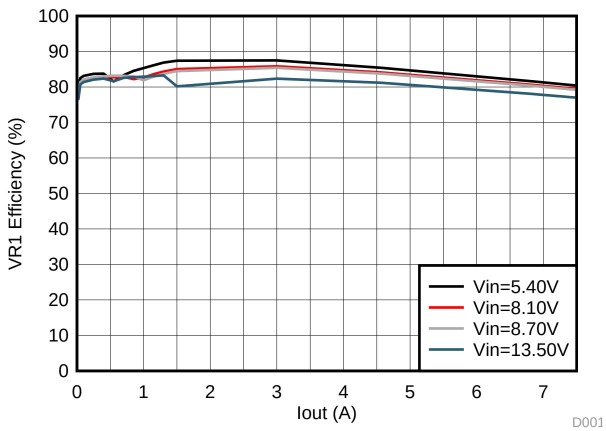


图 102. Typical Efficiency for VR1

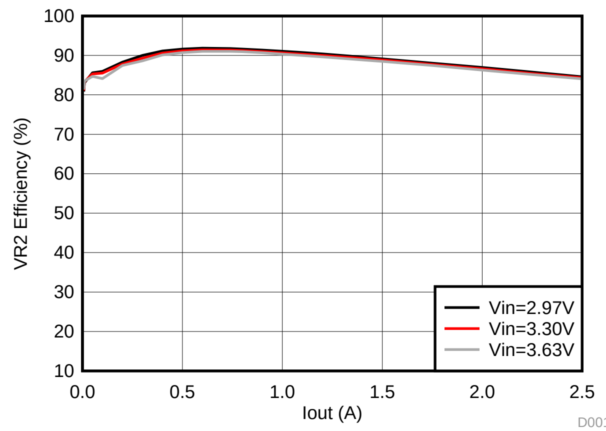


图 103. Typical Efficiency for VR2

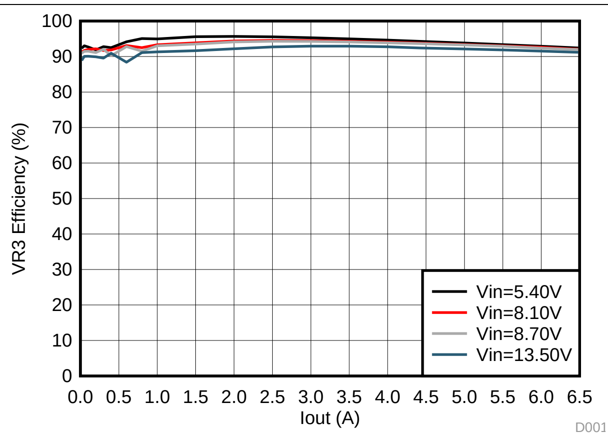


图 104. Typical Efficiency for VR3

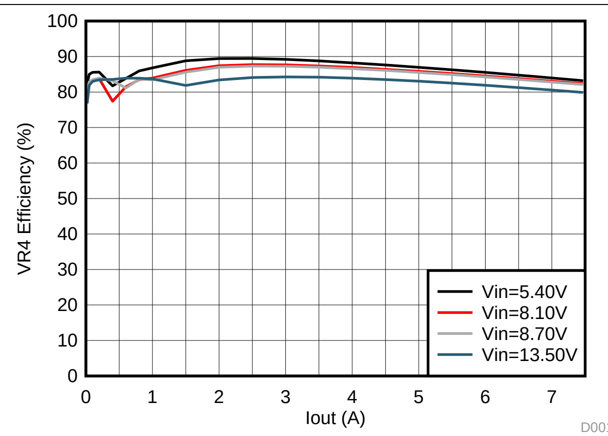


图 105. Typical Efficiency for VR4

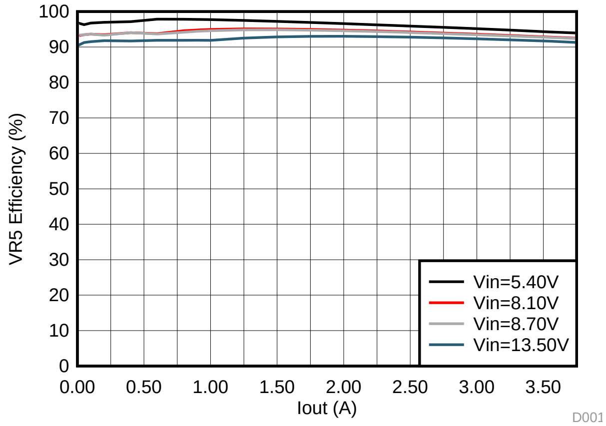


图 106. Typical Efficiency for VR5

9.3 System Examples

Below is a diagram of the SkyLake Platform System Power Delivery. The PMIC is flexible and adjusts well across SkyLake platforms.

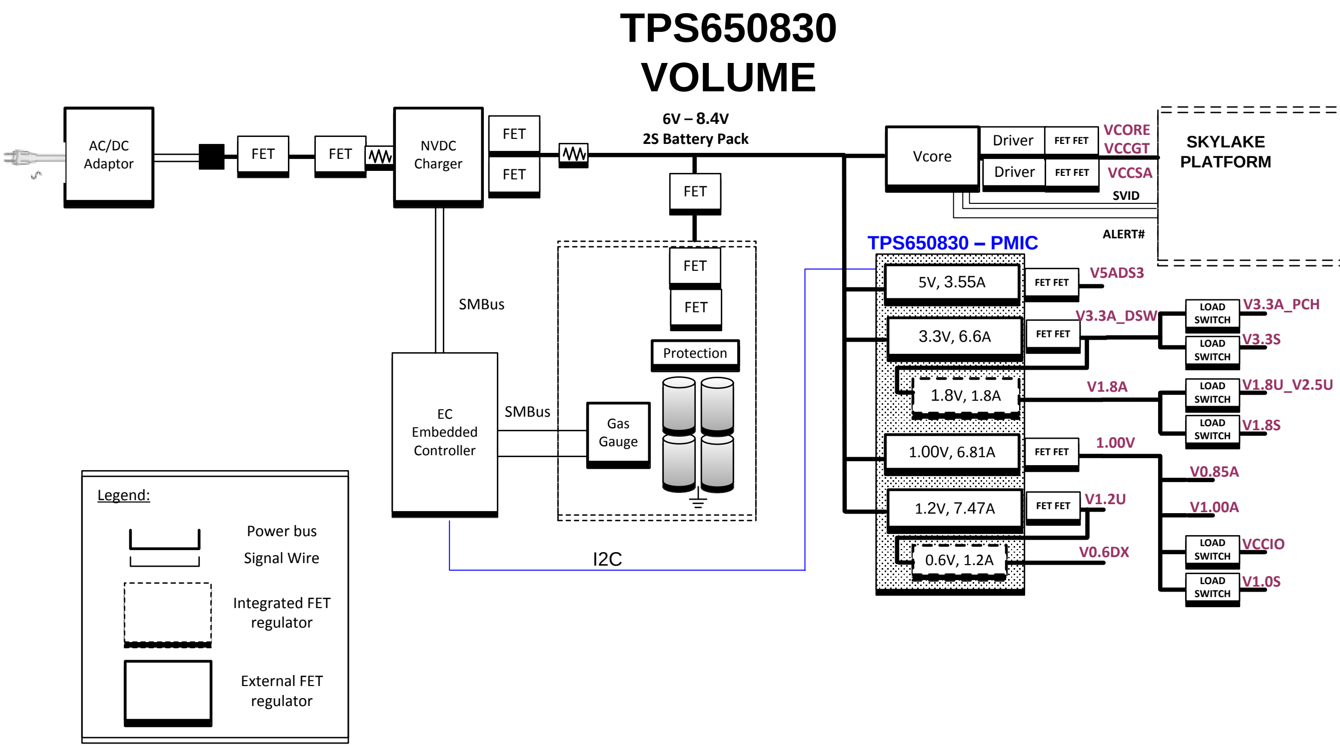


图 107. TPS650830 Volume Simplified System Power Configuration Diagram

9.4 Do's and Don'ts

- Always either float or connect the VINPP to the same voltage as VIN. Never ground VINPP.
- If not using a voltage regulator connect the enable to ground and float the output.

10 Power Supply Recommendations

Any power supply capable of delivering the required input power is acceptable provided that there is a source within the recommended operating conditions for VIN and VINLDO3. The input voltage for the VR2 converter must be 3.3V always. The input voltage of the controllers may vary from the VIN and VINLDO3 voltage. Ensure that VINPP is connected to the VIN or floated but not grounded.

11 Layout

11.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

There are 2 packages availible for the TPS65083x, the ZAJ and ZCG. The ZAJ is a 7 mm x 7 mm BGA with 0.5 mm ball pitch. The ZCG is a 9 mm x 9 mm BGA with 0.5 mm ball pitch but, some of the inner balls have been removed for easier routing. Both packages preform relatively the same and the decision between which package is best for the application depends on the space constraints and routing technology used.

11.1.1 Fanout for ZAJ using Type 4 Routing

This small 7 mm x 7 mm package utilizes the Type 4 routing technique to decrease system board area as much as possible. This Type 4 rounting has vias in pad, blind and buried vias, and minimum trace width / spacing of 4 mils.

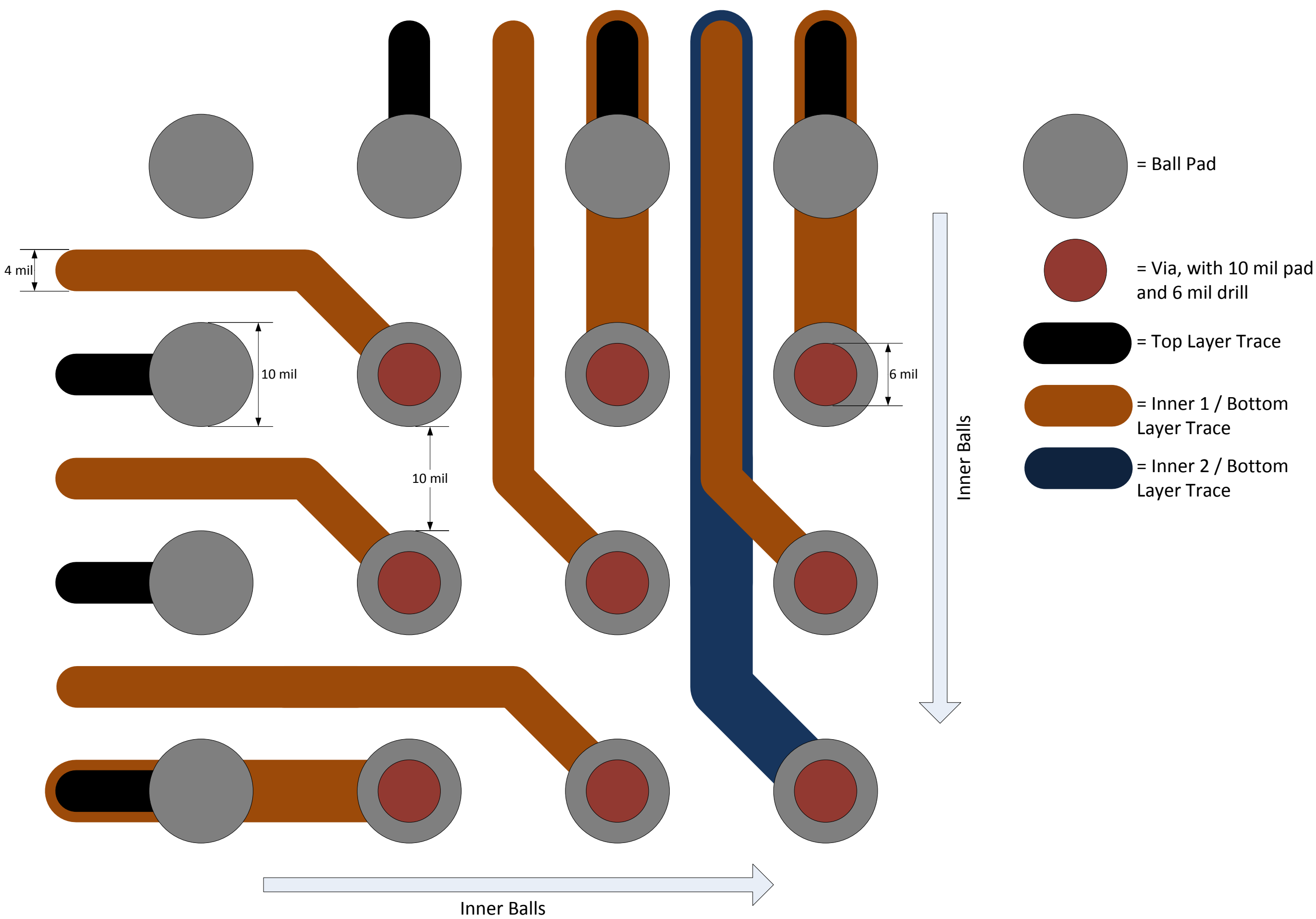


图 108. Fanout for ZAJ Package Using Type 4 Routing

Layout Guidelines (接下页)

11.1.2 Fanout for ZCG using Type 3 Routing

The ZCG has some of the inner balls removed to essentially create a 0.1 mm ball pitch for the inner balls of the package. This feature allows for Type 3 routing of the board. This Type 3 routing has no vias in pad, no blind and buried vias, and minimum trace width / spacing of 4 mils.

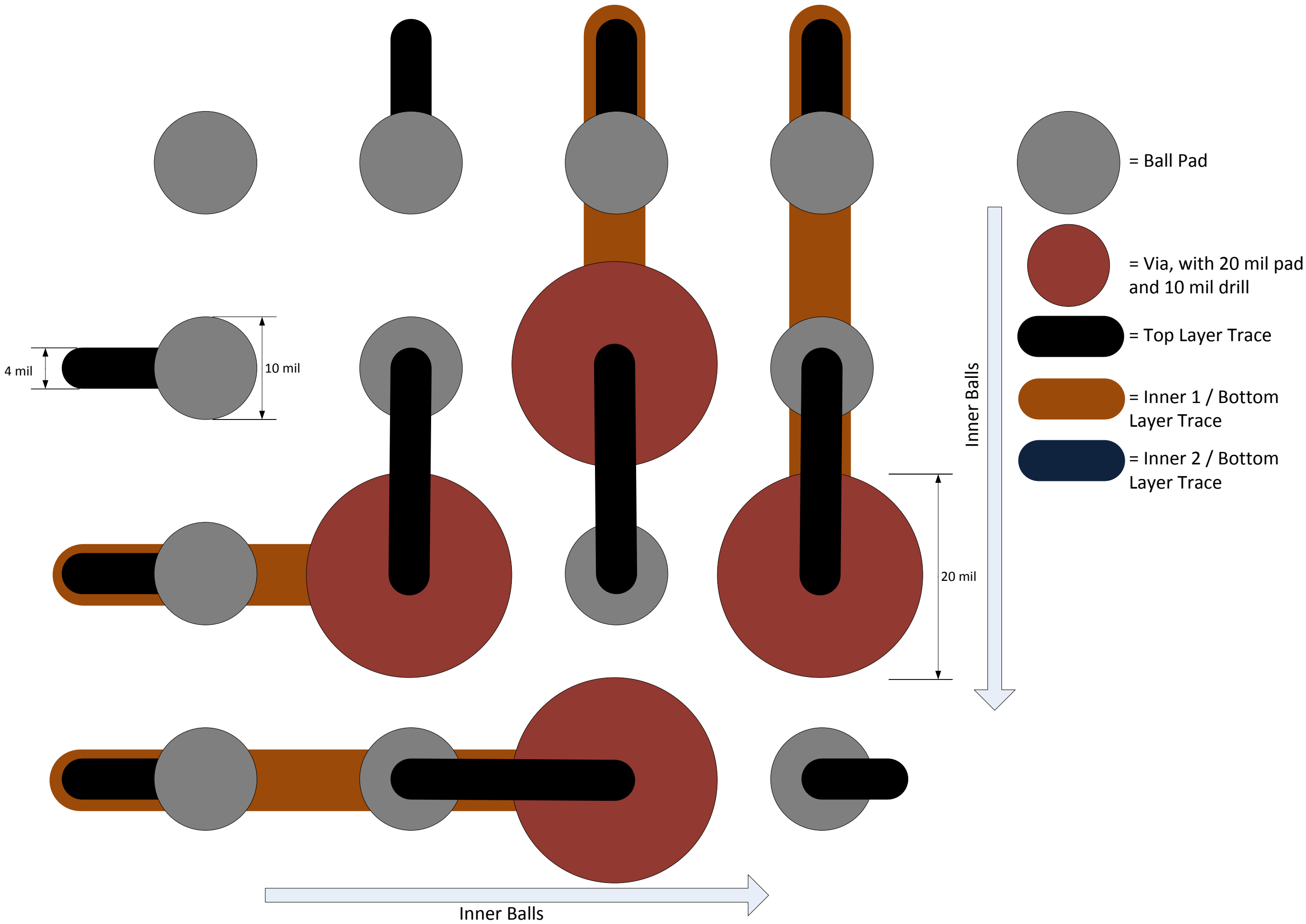


图 109. Fanout for ZCG Package using Type 3 Routing

11.1.3 Layout Checklist

- All inductors, input/output caps and FETs for the converters and controller should be on the same board layer as the IC.
- Place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible to achieve the best regulation performance.
- Bootstrap capacitors must be place close to the IC from the SWVRx to VBSTVRx pins.
- DRVLVRx signals must be routed on the same layer as the IC and the FETs and minimize the length and parasitic inductance of the trace as much as possible.
- Each converter and controller should have their own separate ground and each ground should connect to the common ground separately. The input capacitors, output capacitors, and FET grounds for each VRx converter and controller must be connected to the ground plane for the respective VRx rail. Since, the PGNDs for each rail are not connect to each other or AGND, it is required to use the PGNDVRx pins for the input and ouput capacitors for each VRx rail. This ground plane should connect in one place to the common ground close to the input and output capacitor ground pads. See the figure below for a visual representation of the converter layout scheme.
- The internal reference regulators must have their input and output caps close to the IC pins.

Layout Guidelines (接下页)

- Route the FBVRxP and FBVRxN signals as a differential pair.

11.2 Layout Example

11.2.1 ZAJ Package

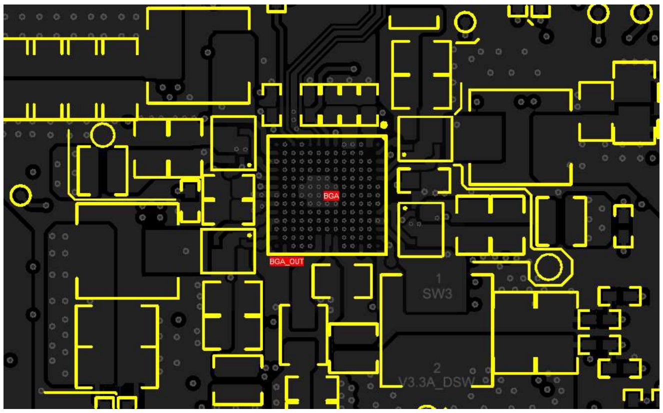


图 110. Top Layer ZAJ Layout

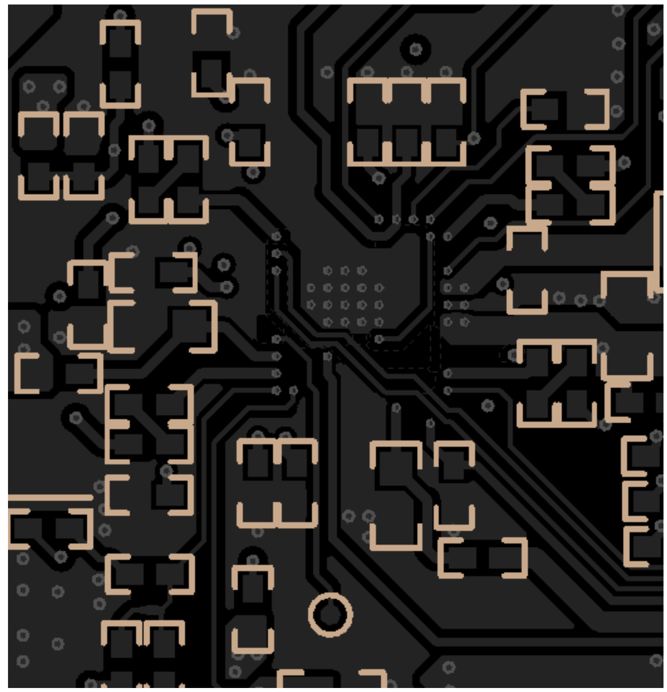


图 111. Bottom Layer ZAJ Layout

11.2.2 ZCG Package

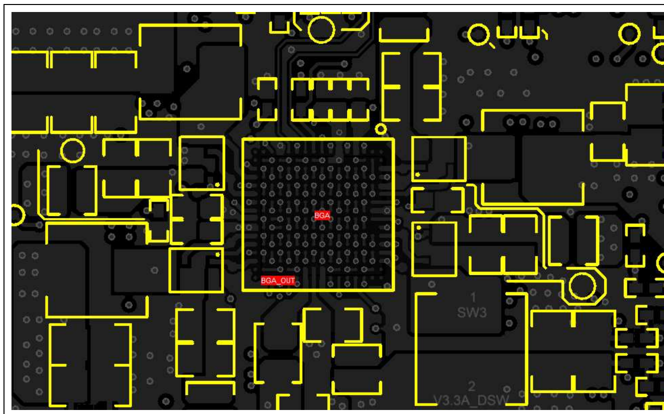


图 112. Top Layer ZCG Layout

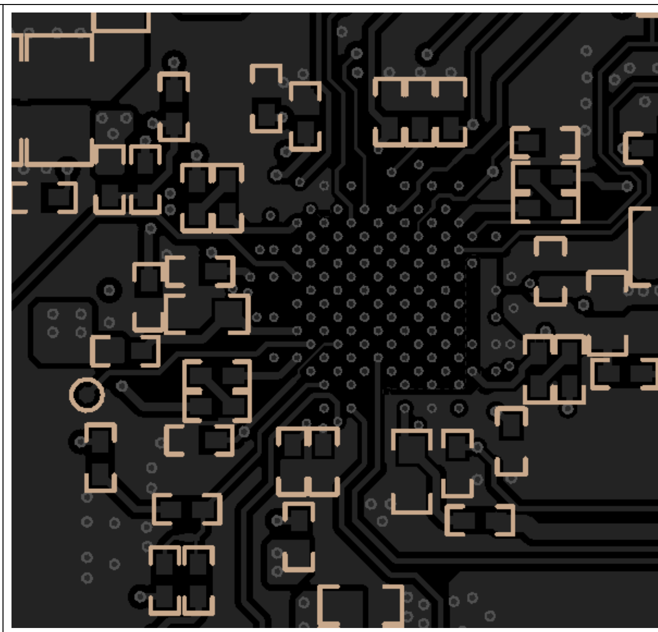


图 113. Bottom Layer ZCG Layout

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the PowerPAD™
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table please check the *Thermal Characteristics Application Note* (SZZA017) and the *IC Package Thermal Metrics Application Note* (SPRA953).

12 器件和文档支持

12.1 器件支持

12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

如需获得器件支持，请在此将问题提交至 E2E 论坛：e2e.ti.com

12.1.2 开发支持

关于 TPS65083x 的常见问题解答 (FAQ)，请参见此处的 FAQ：http://e2e.ti.com/support/power_management/pmu/w/design_notes/2898.tps65083x-faqs

12.2 文档支持

12.2.1 相关文档

应用报告《采用 JEDEC PCB 设计的线性和逻辑封装散热特性》（文件编号：SZZA017）

应用报告《半导体和 IC 封装热指标》（文件编号：SPRA953）

12.3 商标

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

SLYZ022 — *TI 术语表*。
　这份术语表列出并解释术语、首字母缩略词和定义。

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS650830ZAJR	Active	Production	NFBGA (ZAJ) | 168	2000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZAJR.A	Active	Production	NFBGA (ZAJ) | 168	2000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZAJT	Active	Production	NFBGA (ZAJ) | 168	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZAJT.A	Active	Production	NFBGA (ZAJ) | 168	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZCGR	Active	Production	NFBGA (ZCG) | 159	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZCGR.A	Active	Production	NFBGA (ZCG) | 159	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZCGT	Active	Production	NFBGA (ZCG) | 159	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZCGT.A	Active	Production	NFBGA (ZCG) | 159	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

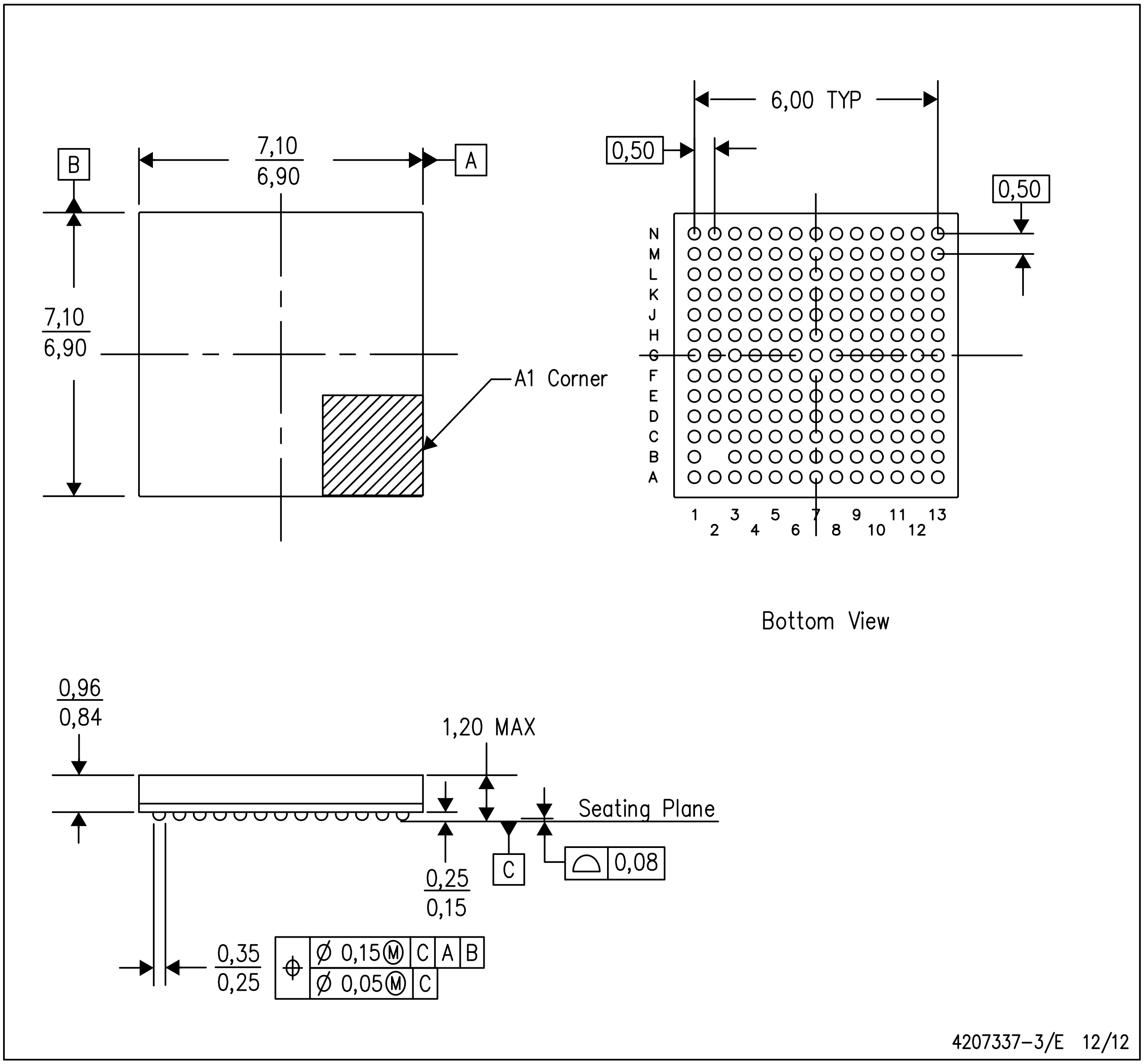
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

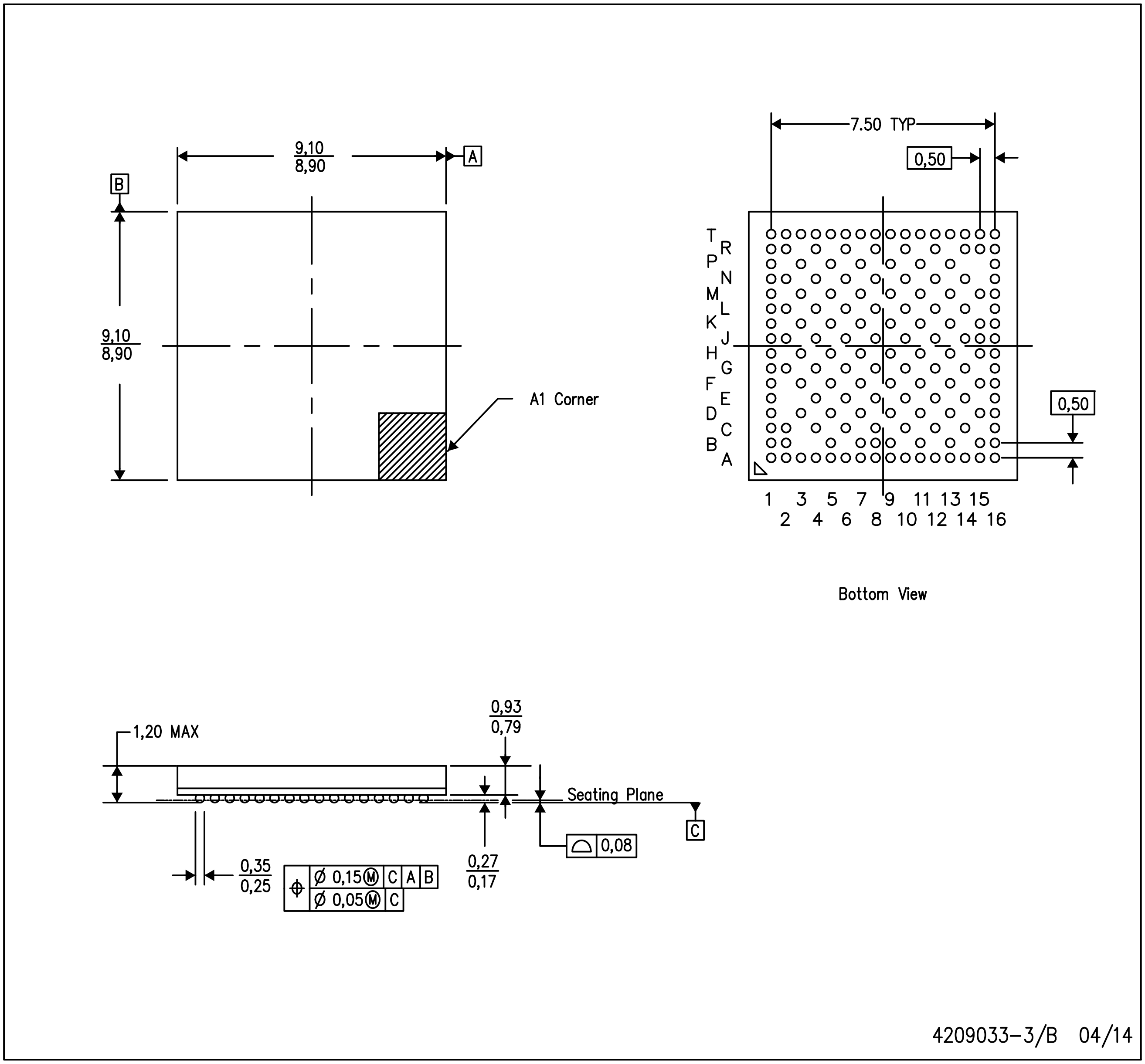
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

ZAJ (S–PBGA–N168) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

ZCG (S–PBGA–N159) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.