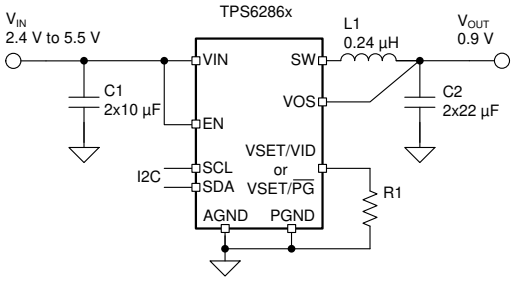
具有 I²C 接口、采用 WCSP 封装的 TPS62864/6 2.4V 至 5.5V 输入、4A 和 6A 同步降压转换器

1 特性

- 7mΩ 和 6.5mΩ 内部功率 MOSFET
- > 90% 效率（0.9V 输出）
- 可实现快速瞬态响应的 DCS-Control 拓扑
- 1% 的输出电压精度
- 4μA 工作静态电流
- 2.4V 至 5.5V 输入电压范围
- 2.4MHz 开关频率
- 通过外部电阻器进行选择
  - 启动输出电压
  - I²C 从器件地址
- I²C 接口选择
  - 节电模式或强制 PWM 模式
  - 输出放电
  - 断续或锁存短路保护
  - 输出电压斜坡速度
- 动态电压调节 (DVS) 的 VID 引脚
- 热预警和热关断
- 电源正常状态指示器引脚选项
- 兼容 I²C 的接口速率高达 3.4Mbps
- 采用 1.05mm x 1.78mm x 0.5mm 15 引脚 WCSP 封装，间距为 0.35mm
- 使用 TPS62866 并借助 WEBENCH® Power Designer 创建定制设计方案



典型应用

2 应用

- 为 FPGA、CPU、ASIC 或视频芯片组提供内核电源
- 摄像头模块
- 固态硬盘
- 光学模块

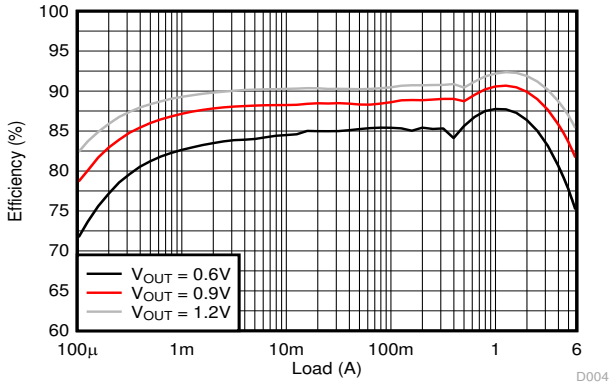
3 说明

TPS62864 和 TPS62866 器件是采用 I²C 接口的高频同步降压转换器，可提供高效、自适应和高功率密度解决方案。该转换器在中高负载条件下以 PWM 模式运行，并在轻负载时自动进入省电模式运行，从而在整个负载电流范围内保持高效率。该器件还可强制进入 PWM 模式运行，以实现最小的输出电压纹波。凭借其 DCS-Control 架构，该器件可实现出色的负载瞬态性能并符合严格的输出电压精度要求。通过 I²C 接口和专用 VID 引脚，可快速调整输出电压，使负载的功耗适应应用不断变化的性能需求。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS62864	WCSP (15)	1.05mm x 1.78mm x 0.5mm
TPS62866		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



V_{IN} = 3.3V 时的效率

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (March 2020) to Revision C (October 2020)	Page
• 删除了 QFN 封装实例	1
• 更新了整个文档的表、图和交叉参考的编号格式。	1
• Updated *Device Options*	3
• Removed Power Good (PG) section	13
• Updated *I²C Register Reset* section	17

Changes from Revision A (December 2019) to Revision B (March 2020)	Page
• Updated 图 9-12	23

Changes from Revision * (June 2019) to Revision A (December 2019)	Page
• 将器件状态从“预告信息”更改为“量产数据”	1

5 Device Options

PART NUMBER(1)	START-UP OUTPUT VOLTAGE	OUTPUT CURRENT	VID OR $\overline{PG}$ PIN
TPS628640AYCG	0.4 V to 1.15 V, Selectable	4 A	VID
TPS628640BYCG			$\overline{PG}$
TPS628660AYCG		6 A	VID
TPS628660BYCG			$\overline{PG}$

(1) For all available packages, see the orderable addendum at the end of the data sheet.

6 Pin Configuration and Functions

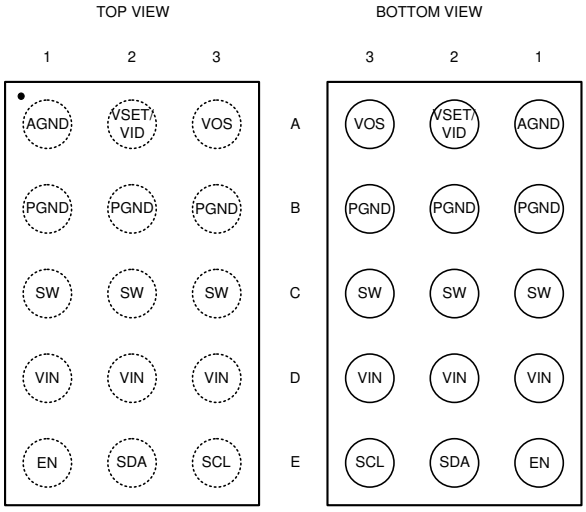


图 6-1. YCG (15 Pin)

表 6-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AGND	A1	Analog ground pin
VSET/VID	A2	Start-up output voltage and device address selection pin. An external resistor must be connected. After start-up, the pin can be used to select the V_{OUT} registers for the output voltage. (Low = V_{OUT} register 1; High = V_{OUT} register 2). See 节 8.4.4.
VSET/ $\overline{PG}$	A2	Start-up output voltage and device address selection pin. An external resistor must be connected. After start-up, the pin is used for the $\overline{\text{power good}}$ indicator. When the output voltage is not regulated, the pin is driven high. When the output voltage is regulated, the pin is pulled low through the external resistor. The function after start-up depends on the device option. See 节 5.
VOS	A3	Output voltage sense pin. This pin must be directly connected to the output capacitor.
PGND	B1,B2,B3	Power ground pin
SW	C1,C2,C3	Switch pin of the power stage
VIN	D1,D2,D3	Power supply input voltage pin
EN	E1	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. Do not leave floating.
SDA	E2	I^2C serial data pin. Do not leave it floating. Connect it to AGND if not used.
SCL	E3	I^2C serial clock pin. Do not leave it floating. Connect it to AGND if not used.

7 Specifications

7.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage(1)	VIN, EN, SDA, SCL, VOS, VSET/VID, VSET/$\overline{PG}$	-0.3	6	V
	SW (DC)	-0.3	V_{IN} + 0.3	
	SW (AC, less than 10ns)(2)	-2.5	10	
$I_{SOURCE\_\overline{PG}}$	Source current at VSET/$\overline{PG}$		1	mA
$I_{SINK\_SDA,SCL}$	Sink current at SDA, SCL		2	mA
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) All voltage values are with respect to network ground terminal.
(2) While switching.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.4		5.5	V
t_{F_VIN}	Falling transition time at VIN(1)			10	mV/µs
I_{OUT}	Output current, TPS62864 (2)	0		4	A
	Output current, TPS62866 (3)	0		6	
T_J	Junction temperature	-40		125	°C

(1) The falling slew rate of V_{IN} should be limited if V_{IN} goes below V_{UVLO}.
(2) Lifetime is reduced when operating continuously at 4-A output current and the junction temperature is higher than 105 °C.
(3) Lifetime is reduced when operating continuously at 6-A output current and the junction temperature is higher than 85 °C.

7.4 Thermal Information

THERMAL METRIC(1)		TPS6286x YCG		UNIT
		JEDEC 51-7	TPS62866EVM-051	
		15 PINS	15 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.8	56.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.8	n/a(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.5	n/a(2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23.3	27.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Not applicable to an EVM.

7.5 Electrical Characteristics

T_J = -40 °C to 125 °C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25 °C and V_{IN} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, no load, device not switching		4	10	µA
I_{SD}	Shutdown current	EN = Low, T_J = -40℃ to 85℃		0.1	1	µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} rising	2.2	2.3	2.4	V
		V_{IN} falling	2.1	2.2	2.3	V
T_{JW}	Thermal warning threshold	T_J rising		130		°C
	Thermal warning hysteresis	T_J falling		20		°C
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN, SDA, SCL						
V_{IH}	High-level input threshold voltage at EN, SCL, SDA, VSET/VID		1.0			V
V_{IL}	Low-level input threshold voltage at EN, SCL, SDA, VSET/VID				0.4	V
$I_{SCL,LKG}$	Input leakage current into SCL pin			0.01	0.2	µA
$I_{SDA,LKG}$	Input leakage current into SDA pin			0.01	0.1	µA
$I_{EN,LKG}$	Input leakage current into EN pin			0.01	0.1	µA
C_{SCL}	Parasitic capacitance at SCL			1		pF
C_{SDA}	Parasitic capacitance at SCL			2.4		pF
STARTUP, POWER GOOD						
t_{Delay}	Enable delay time	Time from EN high to device starts switching, R1 = 249kΩ	420	700	1100	µs
t_{Ramp}	Output voltage ramp time	Time from device starts switching to power good	0.9	1	1.5	ms
V_{PG}	Power good lower threshold	V_{VOS} referenced to V_{OUT} nominal	85	91	96	%
	Power good upper threshold	V_{VOS} referenced to V_{OUT} nominal	103	111	120	%
$t_{PG,DLY}$	Power good deglitch delay	Rising and falling edges		34		µs
OUTPUT						
V_{OUT}	Output voltage accuracy(1)	$V_{OUT} \geqslant$ 0.59 V, FPWM, no Load, T_J = 25℃ to 125℃	-1		1	%
		V_{OUT} < 0.59 V, FPWM, no Load, T_J = 25℃ to 125℃	-2		2	%
$I_{VOS,LKG}$	Input leakage current into VOS pin	EN = High, V_{VOS} = 1.8 V		18		µA
		EN = Low, Output discharge disabled, V_{VOS} = 1.8 V		0.2	2.5	µA
R_{DIS}	Output discharge resistor at VOS pin			15		Ω
	Load regulation	V_{OUT} = 0.9 V, FPWM		0.04		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			7		mΩ
	Low-side FET on-resistance			6.5		mΩ
I_{LIM}	High-side FET forward current limit	TPS62864	5	5.5	6	A
		TPS62866	7	7.7	8.5	A
	Low-side FET forward current limit	TPS62864		4.5		A
		TPS62866		6.5		A
	Low-side FET negative current limit	TPS62864, TPS62866		-3		A

7.5 Electrical Characteristics (continued)

T_J = -40 °C to 125 °C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25 °C and V_{IN} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	PWM switching frequency	I_{OUT} = 1 A, V_{OUT} = 0.9 V		2.4		MHz

(1) Exclude codes: 0x20 (560 mV), 0x40 (720 mV), 0x60 (880 mV), 0x80 (1040 mV), 0xC4 (1360 mV), 0xE0 (1520 mV).

7.6 I²C InterfaceTiming Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL Clock Frequency	Standard mode		100	kHz
		Fast mode		400	kHz
		Fast mode plus		1	MHz
		High-speed mode (write operation), C_B – 100 pF max		3.4	MHz
		High-speed mode (read operation), C_B – 100 pF max		3.4	MHz
		High-speed mode (write operation), C_B – 400 pF max		1.7	MHz
		High-speed mode (read operation), C_B – 400 pF max		1.7	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast mode plus	0.5		µs
t_{HD}, t_{STA}	Hold Time (Repeated) START condition	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-speed mode	160		ns
t_{LOW}	LOW Period of the SCL Clock	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast mode plus	0.5		µs
		High-speed mode, C_B – 100 pF max	160		ns
		High-speed mode, C_B – 400 pF max	320		ns
t_{HIGH}	HIGH Period of the SCL Clock	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-speed mode, C_B – 100 pF max	60		ns
		High-speed mode, C_B – 400 pF max	120		ns
t_{SU}, t_{STA}	Setup Time for a Repeated START Condition	Standard mode	4.7		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-speed mode	160		ns
t_{SU}, t_{DAT}	Data Setup Time	Standard mode	250		ns
		Fast mode	100		ns
		Fast mode plus	50		ns
		High-speed mode	10		ns
t_{HD}, t_{DAT}	Data Hold Time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	µs
		Fast mode plus	0		µs
		High-speed mode, C_B – 100 pF max	0	70	ns
		High-speed mode, C_B – 400 pF max	0	150	ns

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{RCL}	Rise Time of SCL Signal	Standard mode		1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100 pF max	10	40	ns
		High-speed mode, C_B – 400 pF max	20	80	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max	20	160	ns
t_{FCL}	Fall Time of SCL Signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode		300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100 pF max	10	40	ns
		High-speed mode, C_B – 400 pF max	20	80	ns
t_{RDA}	Rise Time of SDA Signal	Standard mode		1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max	20	160	ns
t_{FDA}	Fall Time of SDA Signal	Standard mode		300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max	20	160	ns
t_{SU}, t_{STO}	Setup Time of STOP Condition	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-Speed mode	160		ns
C_B	Capacitive Load for SDA and SCL	Standard mode		400	pF
		Fast mode		400	pF
		Fast mode plus		550	pF
		High-Speed mode		400	pF

7.7 Typical Characteristics

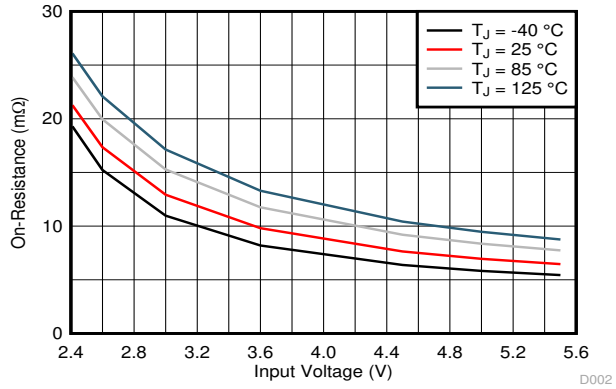


图 7-1. High-Side FET On-Resistance

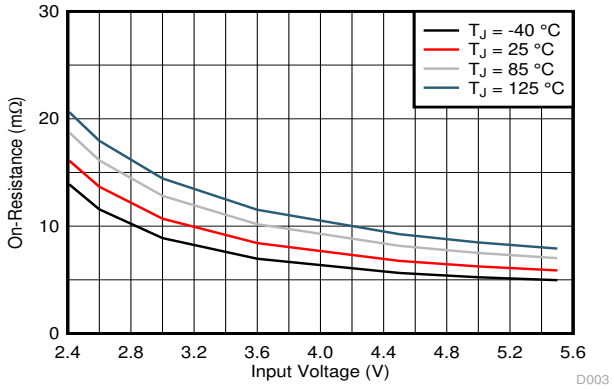


图 7-2. Low-Side FET On-Resistance

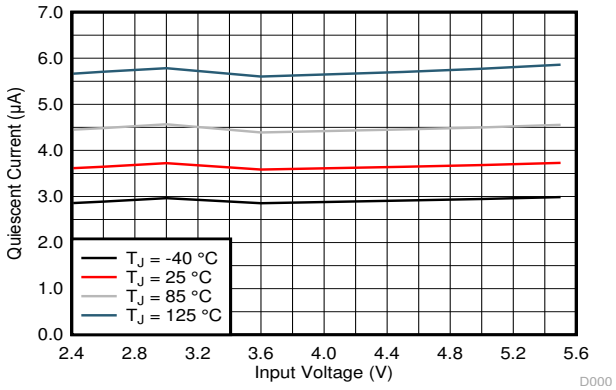


图 7-3. Quiescent Current

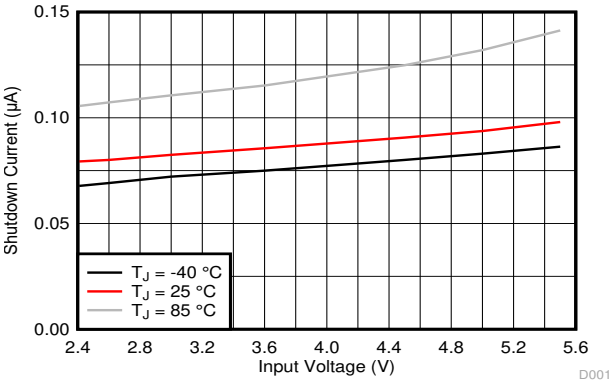


图 7-4. Shutdown Current

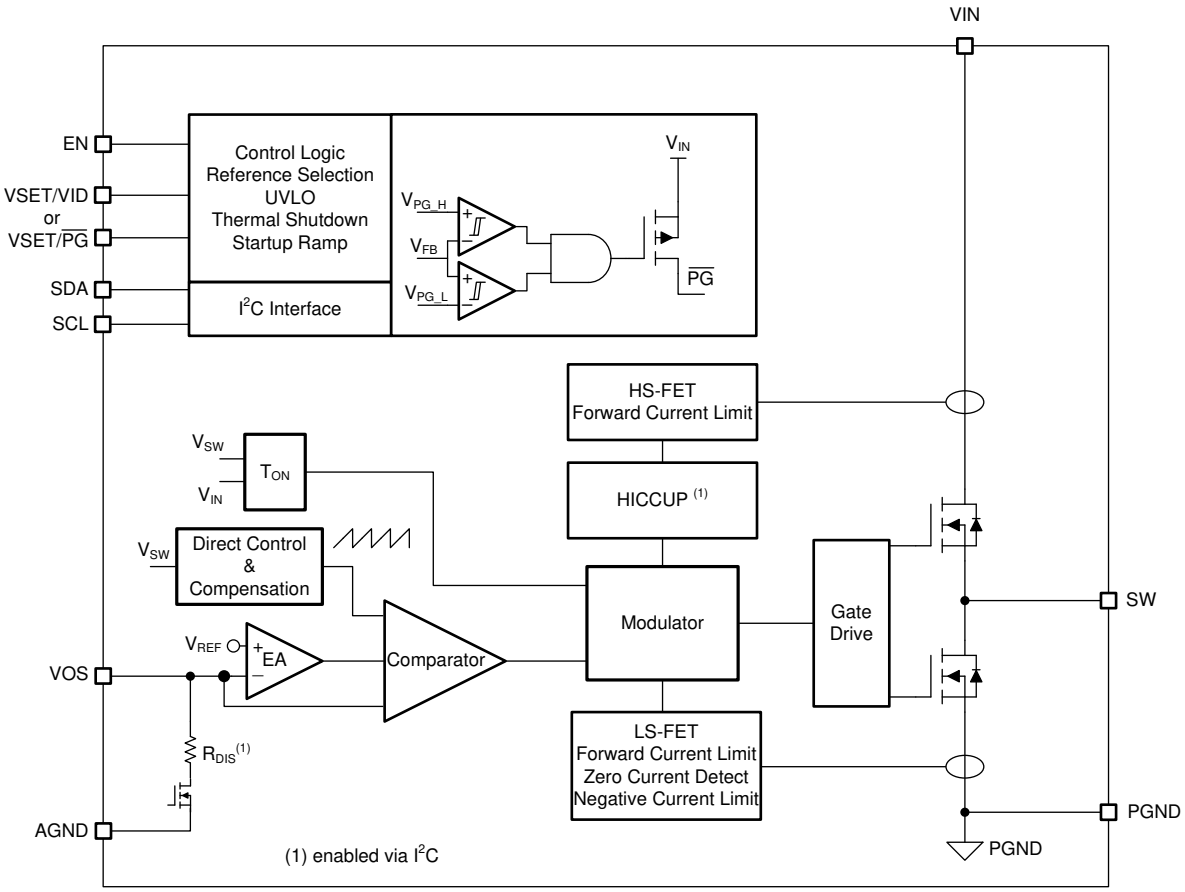
8 Detailed Description

8.1 Overview

The TPS62864 and TPS62866 synchronous step-down converters use the DCS-Control (Direct Control with Seamless transition into Power Save Mode) topology. This is an advanced regulation topology that combines the advantages of hysteretic and current-mode control schemes.

The DCS-Control™ topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2.4 MHz, having a controlled frequency variation over the input voltage range. Because DCS-Control supports both operation modes (PWM and PFM) within a single building block, the transition from PWM mode to Power Save Mode is seamless without affecting the output voltage. The devices offer both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power Save Mode

As the load current decreases, the device enters Power Save Mode (PSM) operation. PSM occurs when the inductor current becomes discontinuous, which is when it reaches 0 A during a switching cycle. Power Save Mode is based on a fixed on-time architecture, as shown in 方程式 1.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 416\text{ns} \quad (1)$$

In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or inductor value.

8.3.2 Forced PWM Mode

With I^2C, set the device in forced PWM (FPWM) mode by the CONTROL register. The device switches at 2.4 MHz, even with a light load. This reduces the output voltage ripple and allows simple filtering of the switching frequency for noise-sensitive applications. Efficiency at light load is lower in FPWM mode.

8.3.3 Start-up

After enabling the device, there is an enable delay (t_{Delay}) before the device starts switching. During this period, the device sets the internal reference voltage, and determines the start-up output voltage through the resistor connected to the VSET/VID or VSET/ $\overline{PG}$ pin. After t_{delay}, all registers can be read and written by the I^2C interface.

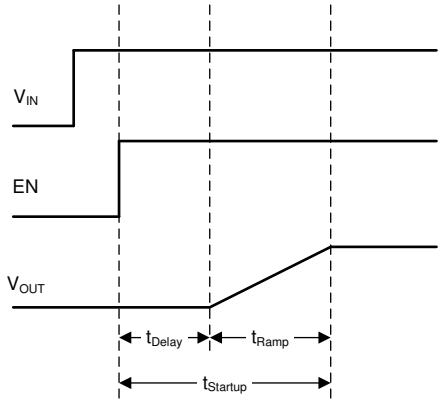


图 8-1. Start-up Sequence

After the enable delay, an internal soft start-up circuitry ramps up the output voltage with a period of 1 ms (t_{Ramp}). This avoids excessive inrush current and creates a smooth output voltage rising-slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The device is able to start into a pre-biased output capacitor. It starts with the applied bias voltage and ramps the output voltage to its nominal value.

8.3.4 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from high inductor current and drawing excessive current from the battery or input voltage rail. Excessive current can occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, cycle by cycle, the high-side MOSFET is turned off and the low-side MOSFET is turned on, while the inductor current ramps down to the low-side MOSFET current limit.

When the high-side MOSFET current limit is triggered 32 times, the device stops switching. The device then automatically re-starts, with an internal soft start-up, after a typical delay time of 128 µs has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears.

The HICCUP is disabled by the CONTROL register bit Enable HICCUP. Disabling HICCUP changes the overcurrent protection to latching protection. The device stops switching after the high-side MOSFET current limit is triggered 32 times. Toggling the EN pin, removing and reapplying the input voltage, or writing to the CONTROL register bit Software Enable Device unlatches the device.

8.3.5 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, undervoltage lockout (UVLO) is implemented when the input voltage is lower than V_{UVLO}. The device stops switching and the output voltage discharge is active (if enabled through I^2C) when the device is in UVLO. When the input voltage recovers, the device automatically returns to operation with an internal soft start-up. During UVLO, the internal register values are kept.

The UVLO bit in the STATUS Register is set when the input voltage is less than the UVLO falling threshold. When the input voltage is below 1.8 V (typ), all registers are reset.

8.3.6 Thermal Warning and Shutdown

When the junction temperature goes up to T_{JW}, the device gives a pre-warning indicator in the STATUS register. The device keeps running.

When the junction temperature exceeds T_{JSD}, the device goes into thermal shutdown, stops switching, and activates the output voltage discharge. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically with an internal soft start-up. During thermal shutdown, the internal register values are kept.

8.4 Device Functional Modes

8.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic High. In shutdown mode (EN = Low), the internal power switches as well as the entire control circuitry are turned off, and all the registers are reset, except for the Enable Output Discharge bit. Do not leave the EN pin floating.

In shutdown mode (EN = Low), all registers cannot be read and written by the I^2C interface.

The typical threshold value of the EN pin is 0.61 V for rising input signals, and 0.51 V for falling input signals.

The device is also enabled or disabled by setting the bit, Software Enable Device in CONTROL register while EN = High. After being disabled/enabled by this bit, the device stops switching and has a new start-up beginning with t_{Ramp}. There is no T_{Delay} time and the registers are not reset.

8.4.2 Output Discharge

An internal MOSFET switch smoothly discharges the output through the VOS pin in shutdown mode (EN = Low or Software Enable Device bit = 0). The output discharge is also active when the device is in thermal shutdown and UVLO.

When the Enable Output Discharge bit is set to 0, the output discharge function is disabled. The input voltage must remain higher than 1 V (TYP) to keep the output discharge function operational and the status of the Enable Output Discharge bit retained. The Enable Output Discharge bit is reset on the rising edge of the EN pin.

8.4.3 Start-up Output Voltage and I^2C Slave Address Selection (VSET)

During the enable delay (t_{Delay}), the start-up output voltage and device I^2C slave address are set by an external resistor connected to the VSET/VID or VSET/ $\overline{PG}$ pin through an internal R2D (resistor to digital) converter. 表 8-1 shows the options.

表 8-1. Start-up Output Voltage and I^2C Slave Address Options

RESISTOR (E96 SERIES, ±1% ACCURACY) AT VSET/VID OR VSET/ $\overline{PG}$	START-UP OUTPUT VOLTAGE (TYP)	I^2C SLAVE ADDRESS
249 kΩ	1.15 V	1000 110
205 kΩ	1.10 V	1000 101
162 kΩ	1.05 V	1000 100
133 kΩ	1.00 V	1000 011
105 kΩ	0.95 V	1000 010
86.6 kΩ	0.90 V	1000 001
68.1 kΩ	0.85 V	1001 000
56.2 kΩ	0.80 V	1001 001
44.2 kΩ	0.75 V	1001 010
36.5 kΩ	0.70 V	1001 011
28.7 kΩ	0.65 V	1001 100
23.7 kΩ	0.60 V	1001 101

表 8-1. Start-up Output Voltage and I²C Slave Address Options (continued)

RESISTOR (E96 SERIES, ±1% ACCURACY) AT VSET/VID OR VSET/ $\overline{PG}$	START-UP OUTPUT VOLTAGE (TYP)	I²C SLAVE ADDRESS
18.7 kΩ	0.55 V	1001 110
15.4 kΩ	0.50 V	1001 111
12.1 kΩ	0.45 V	1000 000
10 kΩ	0.40 V	1000 111

The R2D converter has an internal current source which applies current through the external resistor, and an internal ADC which reads back the resulting voltage level. Depending on the level, the correct start-up output voltage and I²C slave address are set. Once this R2D conversion is finished, the current source is turned off to avoid current flowing through the external resistor. Ensure that there is no additional current path or capacitance greater than 30 pF from this pin to GND during R2D conversion. Otherwise a false value is set.

During the ramp up period (t_{Ramp}), the output voltage ramps to the target value set by VSET first, then ramps up or down to the new value when the value of the output register is changed by I²C interface commands.

8.4.4 Select Output Voltage Registers (VID)

After the start-up period ($t_{Startup}$), the output voltage can be selected between two output voltage registers by the VID pin. When VID is pulled low, the output voltage is set by 表 8-4. When VID is pulled high, the output voltage is set by 表 8-5. This is also called dynamic voltage scaling (DVS).

During an output voltage change through I²C or the VSET/VID pin, the device can be set in FPWM by the Enable FPWM Mode during Output Voltage Change bit in CONTROL register. The output voltage change speed is set by the Voltage Ramp Speed bit.

8.4.5 Power Good ($\overline{PG}$)

The TPS62864 and TPS62864 families provide device options with the VSET/ $\overline{PG}$ pin, instead of a VSET/VID pin, shown in 图 9-1.

After the enable delay (t_{Delay}), the device starts to compare the output voltage with the nominal value set by the external resistor or the output voltage registers. 表 8-2 shows the logic level of the $\overline{PG}$ pin. The pin is driven up to the input voltage for a logic high. The pin is pulled down to GND by the external resistor R1 for a logic low.

For the VSET/ $\overline{PG}$ option devices, be aware of the following:

- VSET/ $\overline{PG}$ can not be connected to GND. A resistor, R1, must be connected between VSET/ $\overline{PG}$ and GND, for the start-up output voltage and I²C slave address setup.
- The source current of the VSET/ $\overline{PG}$ pin is up to 1 mA.
- V_{OUT} Register 2 is disabled.
- When the device is in shutdown, the shutdown current is high because of the leakage current through the external resistor, R1, when the VSET/ $\overline{PG}$ pin is high.

The VSET/ $\overline{PG}$ has a deglitch time, before the signal goes high or low, during normal operation. For start-up, the VSET/ $\overline{PG}$ has a delay time of 200 µs after the output voltage reaches the nominal voltage.

表 8-2. VSET/ $\overline{PG}$ Pin Logic

DEVICE CONDITIONS		$\overline{PG}$ LOGIC STATUS	
		HIGH	LOW
Enable	$0.91 \times V_{OUT\_NOM} \leqslant V_{VOS} \leqslant 1.11 \times V_{OUT\_NOM}$		√
	$V_{VOS} < 0.91 \times V_{OUT\_NOM}$ or $V_{VOS} > 1.11 \times V_{OUT\_NOM}$	√	
Shutdown	EN = Low	√	
Thermal Shutdown	$T_J > T_{JSD}$	√	
UVLO	$1.8\ V < V_{IN} < V_{UVLO}$	√	

表 8-2. VSET/ $\overline{PG}$ Pin Logic (continued)

DEVICE CONDITIONS		$\overline{PG}$ LOGIC STATUS	
		HIGH	LOW
Power Supply Removal	V_{IN} < 1.8 V	undefined	

8.5 Programming

8.5.1 Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors. The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives or transmits data on the bus under control of the master device, or both.

The device works as a *slave* and supports the following data transfer *modes*, as defined in the I^2C-Bus Specification: standard mode (100 kbps) and fast mode (400 kbps), fast mode plus (1 Mbps) and high-speed mode (3.4 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the input voltage remains above 1.8 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and it is referred to as HS-mode.

It is recommended that the I^2C master initiates a STOP condition on the I^2C bus after the initial power up of SDA and SCL pullup voltages to ensure reset of the I^2C engine.

8.5.2 Standard-, Fast-, and Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in 图 8-2. All I^2C-compatible devices recognize a start condition.

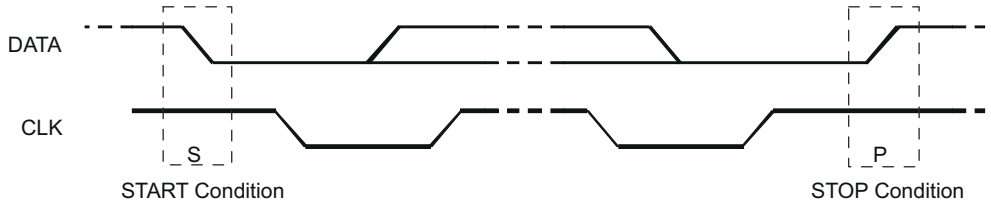


图 8-2. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 图 8-3). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see 图 8-4) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

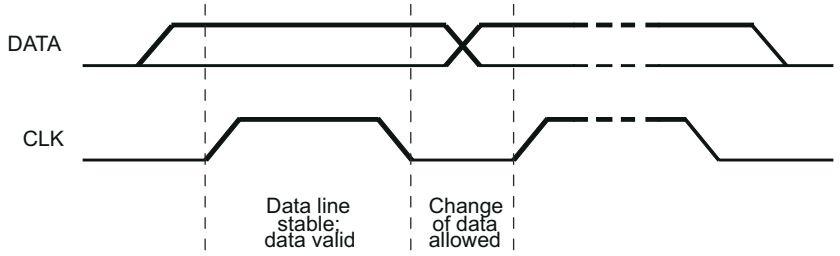


图 8-3. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 图 8-2). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

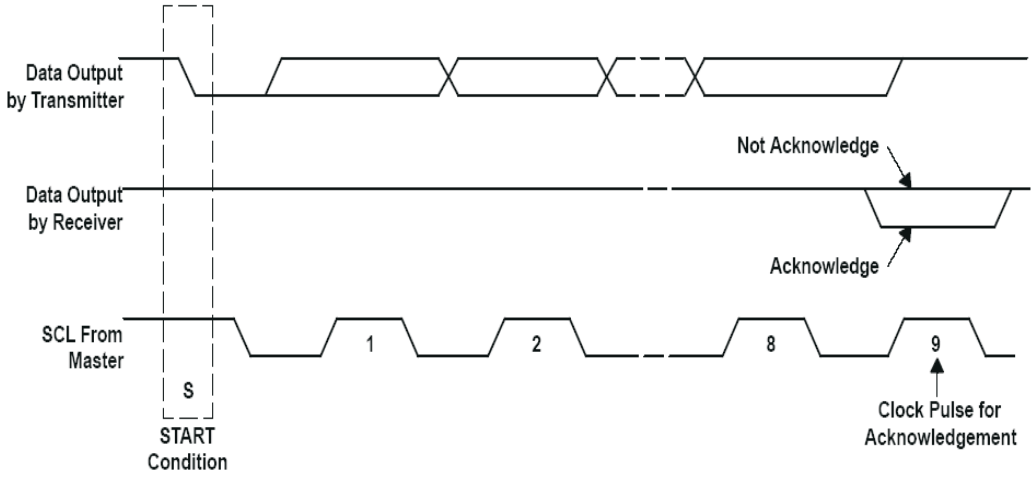


图 8-4. Acknowledge on the I^2C Bus

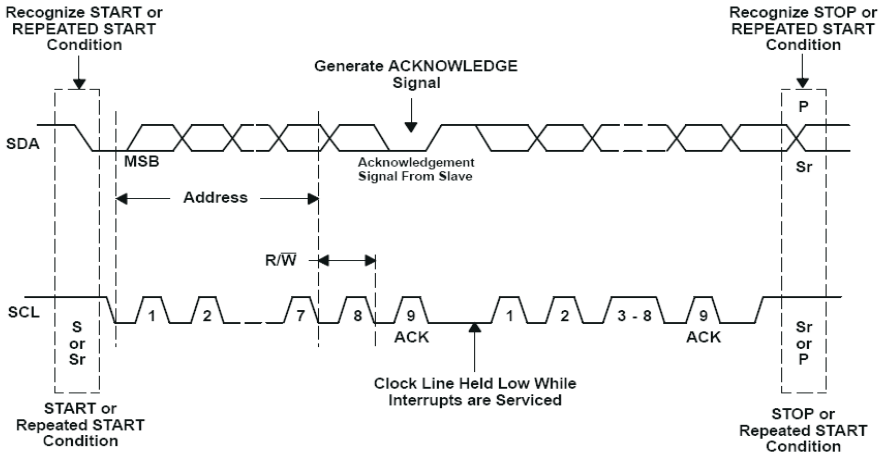


图 8-5. Bus Protocol

8.5.3 HS-Mode Protocol

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4 Mbps operation.

The master then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions must be used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

8.5.4 I²C Update Sequence

The sequence requires a start condition, a valid I²C slave address, a register address byte, and a data byte for a single update. After the receipt of each byte, the device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the device. The device performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

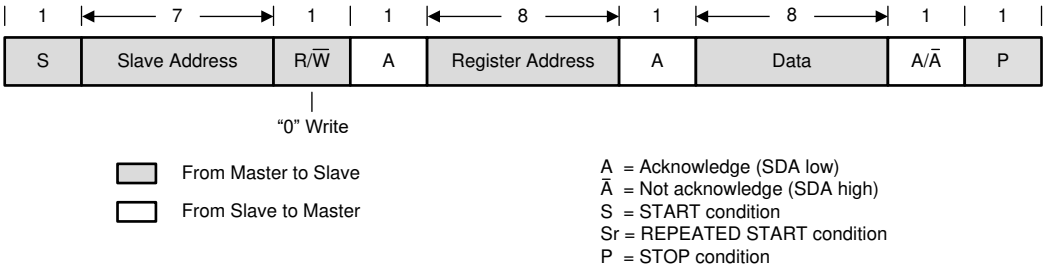


图 8-6. "Write" Data Transfer Format in Standard-, Fast, and Fast-Plus Modes

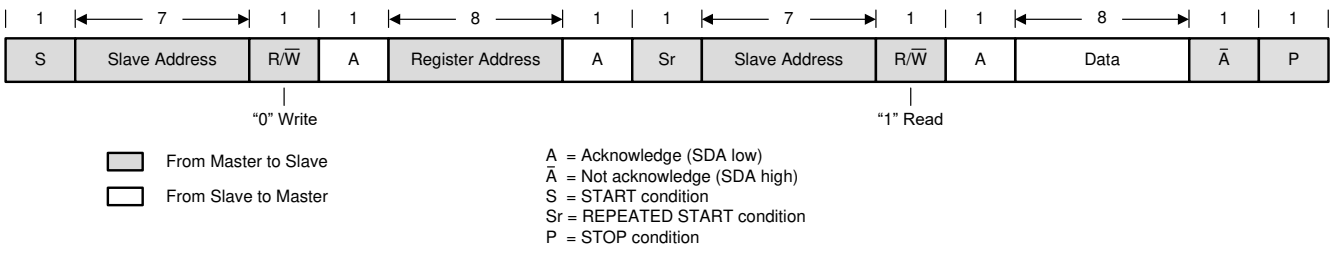


图 8-7. "Read" Data Transfer Format in Standard-, Fast, and Fast-Plus Modes

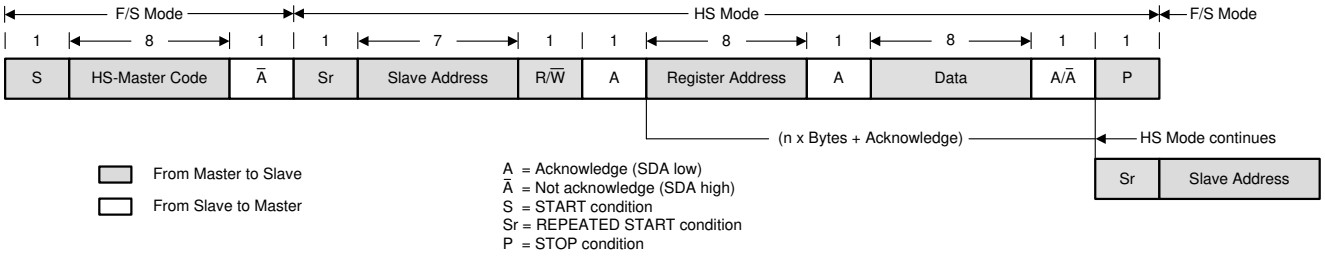


图 8-8. Data Transfer Format in HS-Mode

8.5.5 I²C Register Reset

The I²C registers can be reset by:

- Pulling the input voltage below 1.8 V (typ)
- A high to low transition on EN.
- Setting the Reset bit in the CONTROL register. When Reset is set to 1, all registers are reset to the default values and a new start-up is begun immediately. After t_{Delay}, the I²C registers can be programmed again.

8.6 Register Map

表 8-3. Register Map

REGISTER ADDRESS (HEX)	REGISTER NAME	FACTORY DEFAULT (HEX)	DESCRIPTION
0x01	V_{OUT} Register 1	0x64	Sets the target output voltage
0x02	V_{OUT} Register 2	0x64	Sets the target output voltage
0x03	CONTROL Register	0x6F	Sets miscellaneous configuration bits
0x05	STATUS Register	0x00	Returns status flags

8.6.1 Slave Address Byte

7	6	5	4	3	2	1	0
1	x	x	x	x	x	x	R/W

The slave address byte is the first byte received following the START condition from the master device. The slave addresses can be assigned by an external resistor, see 表 8-1.

8.6.2 Register Address Byte

7	6	5	4	3	2	1	0
0	0	0	0	0	D2	D1	D0

Following the successful acknowledgment of the slave address, the bus master sends a byte to the device, which contains the address of the register to be accessed.

8.6.3 V_{OUT} Register 1

表 8-4. V_{OUT} Register 1 Description

REGISTER ADDRESS 0X01 READ/WRITE			
BIT	FIELD	VALUE (HEX)	OUTPUT VOLTAGE (TYP)(1)
7:0	VO1_SET	0x00	400 mV
		0x01	405 mV
		...	
		0x64	900 mV
		...	
		0xFE	1670 mV
		0xFF	1675 mV

(1) It is not recommended to use the following codes, as their output voltage accuracy may have a wider tolerance than the specification: 0x20 (560 mV), 0x40 (720 mV), 0x60 (880 mV), 0x80 (1040 mV), 0xC4 (1360 mV), 0xE0 (1520 mV).

8.6.4 V_{OUT} Register 2

表 8-5. V_{OUT} Register 2 Description

REGISTER ADDRESS 0X02 READ/WRITE			
BIT	FIELD	VALUE (HEX)	OUTPUT VOLTAGE (TYP)(1)
7:0	VO2_SET	0x00	400 mV
		0x01	405 mV
		...	
		0x64	**900 mV** (default value)
		...	
		0xFE	1670 mV
		0xFF	1675 mV

(1) It is not recommended to use the following codes, as their output voltage accuracy may have a wider tolerance than the specification: 0x20 (560 mV), 0x40 (720 mV), 0x60 (880 mV), 0x80 (1040 mV), 0xC4 (1360 mV), 0xE0 (1520 mV).

8.6.5 CONTROL Register

表 8-6. CONTROL Register Description

REGISTER ADDRESS 0X03 WRITE ONLY				
BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	Reset	R/W	0	1 - Reset all registers to default.
6	Enable FPWM Mode during Output Voltage Change	R/W	1	0 - Keep the current mode status during output voltage change 1 - Force the device in FPWM during output voltage change
5	Software Enable Device	R/W	1	0 - Disable the device. All registers values are still kept. 1 - Re-enable the device with a new startup without the t_{Delay} period.
4	Enable FPWM Mode	R/W	0	0 - set the device in power save mode at light loads. 1 - set the device in forced PWM mode at light loads.
3	Enable Output Discharge	R/W	1	0 - Disable output discharge 1 - Enable output discharge
2	Enable HICCUP	R/W	1	0 - Disable HICCUP. Enable latching protection. 1 - Enable HICCUP, Disable latching protection.
0:1	Voltage Ramp Speed	R/W	11	00 - 20mV/µs (0.25 µs/step) 01 - 10 mV/µs (0.5 µs/step) 10 - 5 mV/µs (1 µs/step) 11 - 1 mV/µs (5 µs/step, default)

8.6.6 STATUS Register

表 8-7. STATUS Register Description

REGISTER ADDRESS 0X05 READ ONLY(1)				
BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	Reserved			
4	Thermal Warning	R	0	1: Junction temperature is higher than 130°C
3	HICCUP	R	0	1: Device has HICCUP status once
2	Reserved			
1	Reserved			
0	UVLO	R	0	1: The input voltage is less than UVLO threshold (falling edge)

(1) All bit values are latched until the device is reset, or the STATUS register is read. Then, the STATUS register is reset to its default values.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Applications

9.2.1 6-A Output Current Application

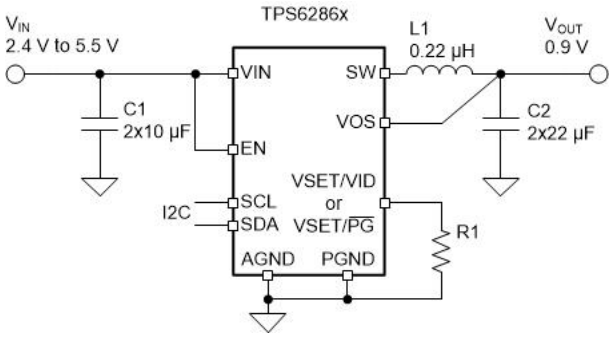


图 9-1. Typical Application

9.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as the input parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.4 V to 5.5 V
Output voltage	0.9 V
Maximum output current	6 A

表 9-2 lists the components used for the example.

表 9-2. List of Components of Figure 9-1

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	10 µF, Ceramic capacitor, 6.3 V, X7R, size 0603, CL10B106MQ8NRNC	Samsung Electro-Mechanics
C2	22 µF, Ceramic capacitor, 6.3 V, X7R, size 0805, GRM21BZ70J226ME44L	Murata
L1	0.22 µH, Power inductor, XAL4020-221ME (12 A, 5.81 mΩ)	Coilcraft
R1	Depending on the start-up output voltage, size 0603	Std

(1) See *Third-party Products* disclaimer.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62866 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.1.2.2 Setting The Output Voltage

The initial output voltage is set by an external resistor connected to the VSET/VID or VSET/$\overline{PG}$ pin, according to 表 8-1. After the soft start-up, the output voltage can be changed in the V_{OUT} Registers. Refer to 表 8-4 and 表 8-5.

9.2.1.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, 表 9-3 outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

表 9-3. Matrix of Output Capacitor and Inductor Combinations

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)			
	22	2 x 22 or 47	3 x 22	150
0.24		+(1)	+	+

(1) This LC combination is the standard value and recommended for most applications.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and – 30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and – 30%.

9.2.1.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, Equation 2 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (2)$$

where

- $I_{OUT,MAX}$ = maximum output current
- ΔI_L = inductor current ripple

- f_{SW} = switching frequency
- L = inductor value

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size must also be taken into account when selecting an appropriate inductor. 表 9-4 lists recommended inductors.

表 9-4. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING, I_{SAT} [A]	DIMENSIONS [L x W x H mm]	DC RESISTANCE [mΩ]	PART NUMBER(1)
0.22	18.7	4 x 4 x 2	5.81	Coilcraft, XAL4020-221ME
0.24	6.6	2 x 1.6 x 1.2	13	Murata, DFE201612E-R24M

(1) See *Third-party Products* disclaimer.

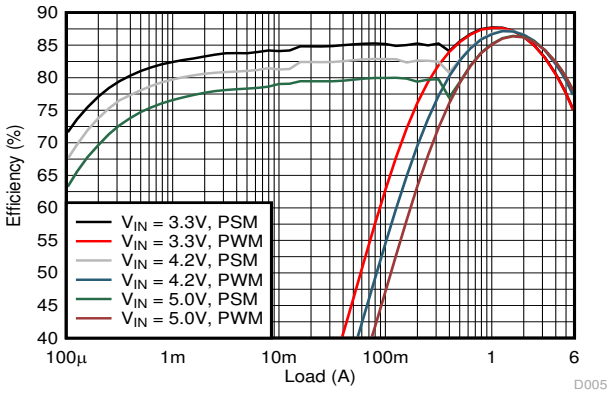
9.2.1.2.5 Capacitor Selection

The input capacitor is the low-impedance energy source for the converter which helps to provide stable operation. A low-ESR multilayer ceramic capacitor is recommended for best filtering and must be placed between VIN and PGND as close as possible to those pins. For most applications, 8 µF is a sufficient value for the effective input capacitance, though a larger value reduces input current ripple.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. The recommended minimum output effective capacitance is 30 µF; this capacitance can vary over a wide range as outline in the output filter selection table.

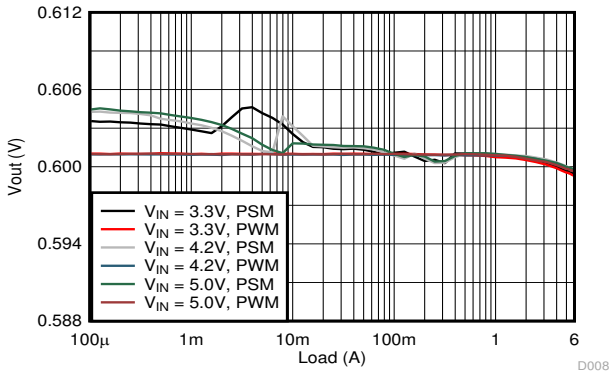
9.2.1.3 Application Curves

V_{IN} = 5.0 V, V_{OUT} = 0.9 V, T_A = 25°C, BOM = 表 9-2, unless otherwise noted.



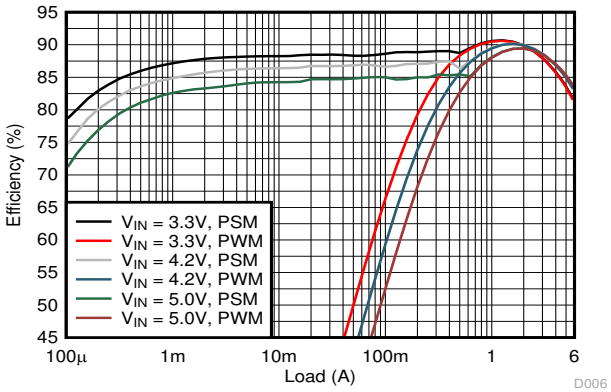
V_{OUT} = 0.6 V Power Save Mode

图 9-2. Efficiency



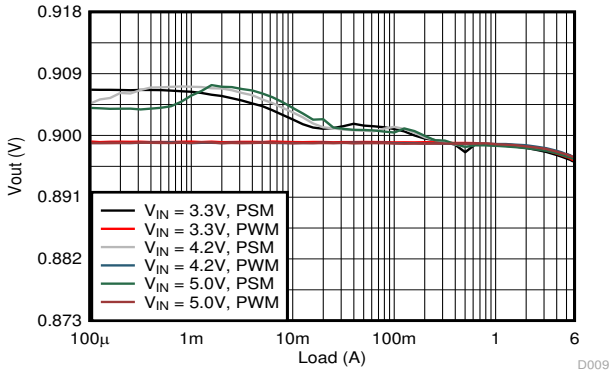
V_{OUT} = 0.6 V Power Save Mode

图 9-3. Load Regulation



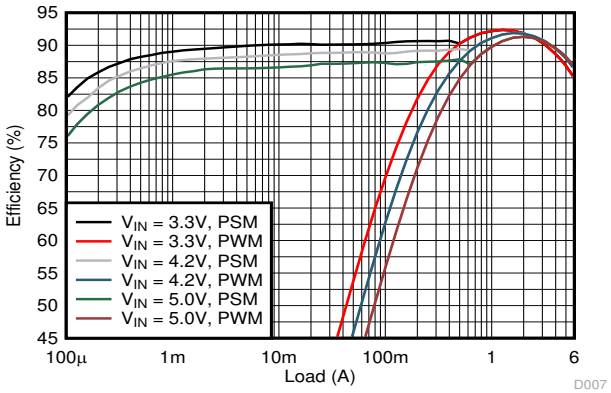
V_{OUT} = 0.9 V

图 9-4. Efficiency



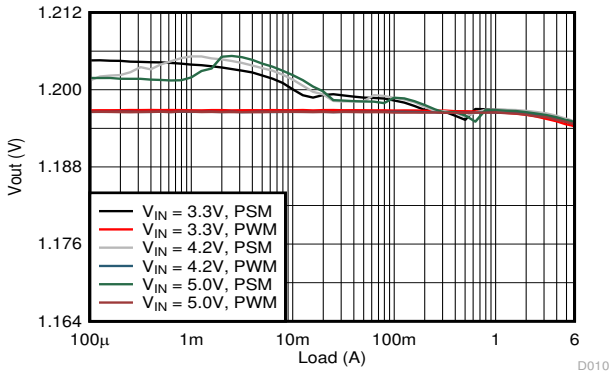
V_{OUT} = 0.9 V

图 9-5. Load Regulation



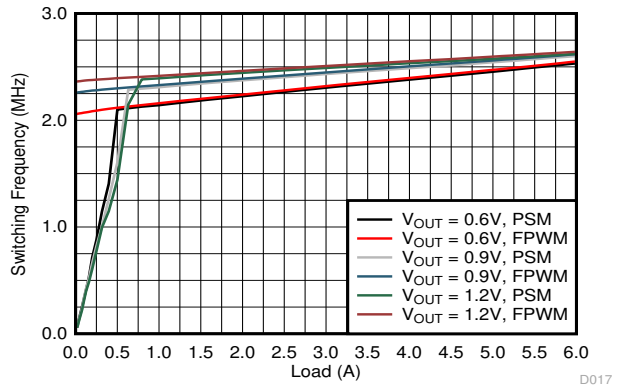
V_{OUT} = 1.2 V Power Save Mode

图 9-6. Efficiency



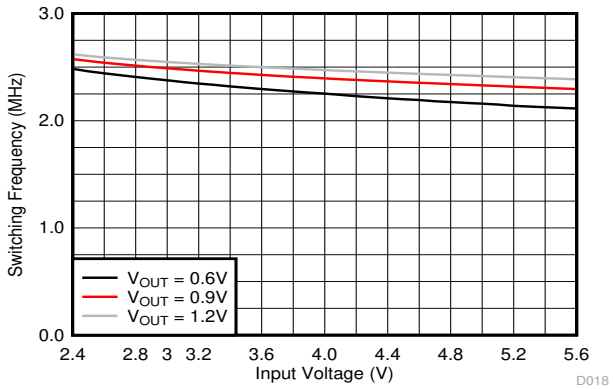
V_{OUT} = 1.2 V Power Save Mode

图 9-7. Load Regulation



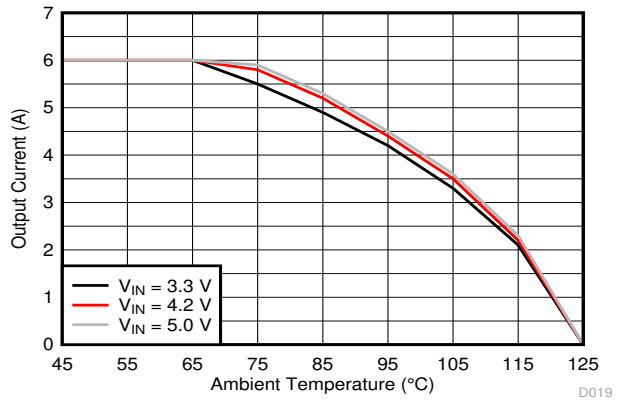
V_{IN} = 5.0 V

图 9-8. Switching Frequency



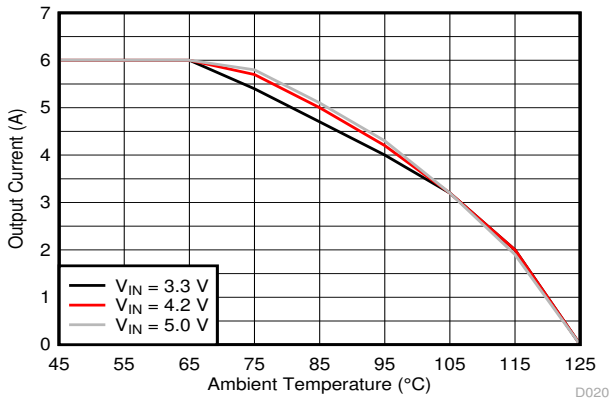
I_{OUT} = 1.0 A

图 9-9. Switching Frequency



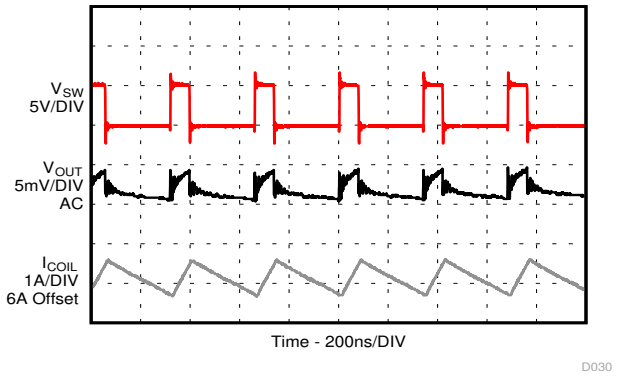
V_{OUT} = 0.9 V θ_{JA} = 56.5°C/W

图 9-10. Thermal Derating



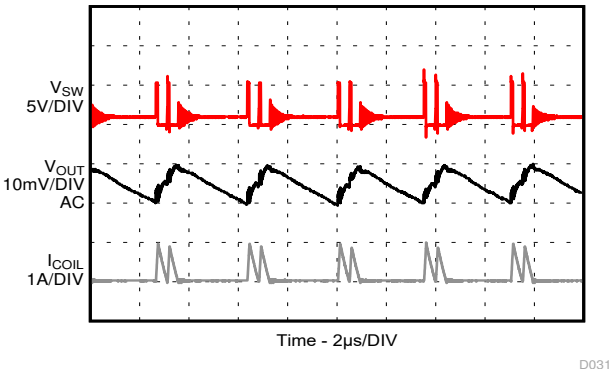
V_{OUT} = 1.675 V θ_{JA} = 56.5°C/W

图 9-11. Thermal Derating



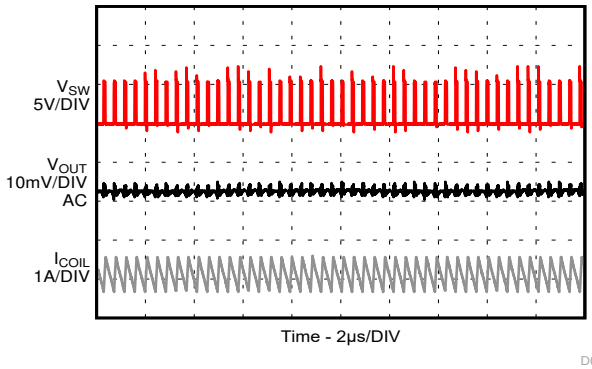
I_{OUT} = 6.0 A

图 9-12. PWM Operation



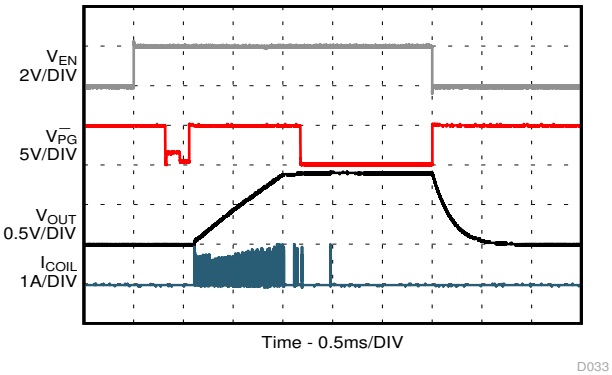
I_{OUT} = 0.1 A

图 9-13. PSM Operation



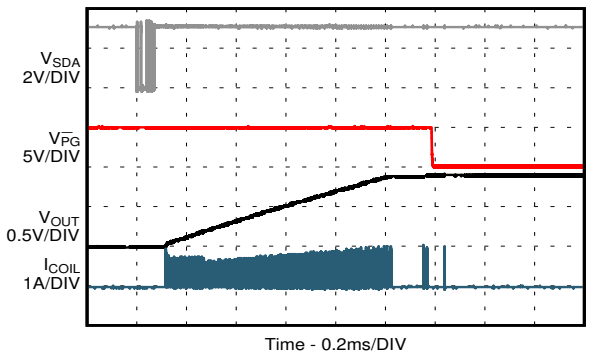
I_{OUT} = 0.1 A

图 9-14. Forced PWM Operation



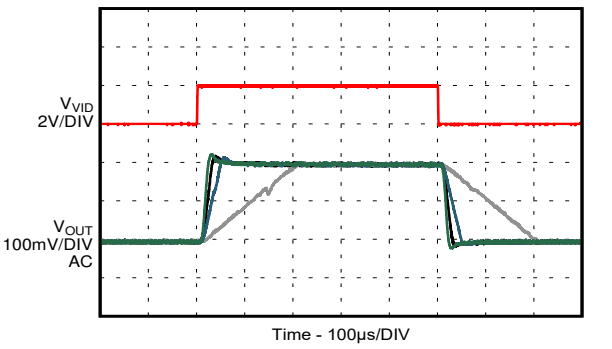
No Load

图 9-15. Startup and Shutdown by EN Pin



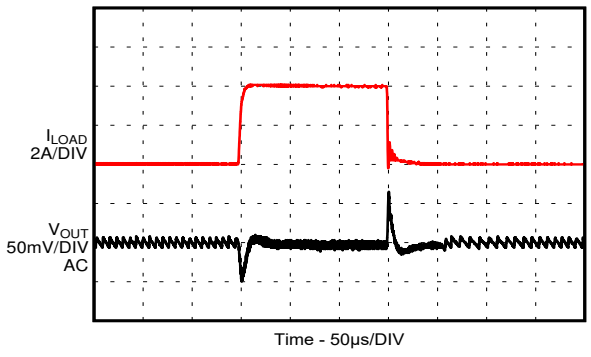
No Load

图 9-16. Start-up by Software Enable Device Bit



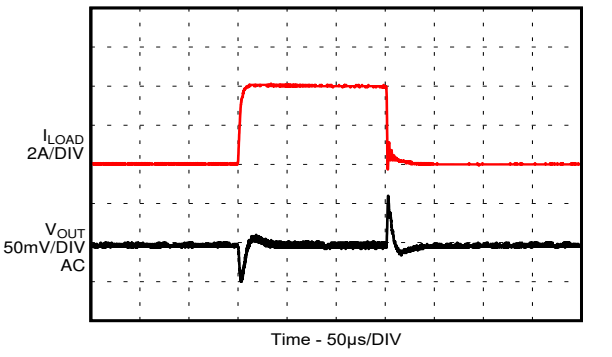
I_{OUT} = 1 A V_{OUT} = 0.9 V to 1.1 V

图 9-17. V_{OUT} Transition with Different Slew Rate Settings



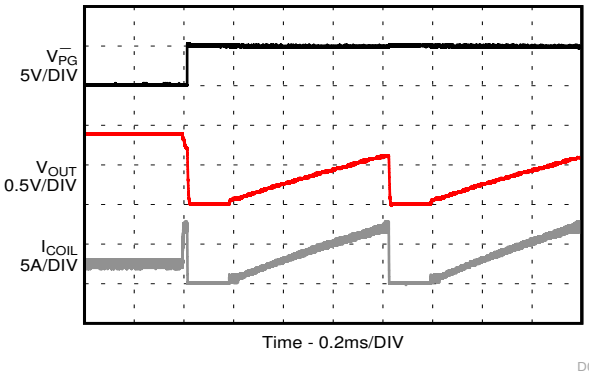
I_{OUT} = 0.05 A to 4 A PSM

图 9-18. Load Transient



I_{OUT} = 0.05 A to 4 A Forced PWM

图 9-19. Load Transient



I_{OUT} = 2.5 A TPS62866

图 9-20. HICCUP Protection

9.2.2 Smaller Application Solution

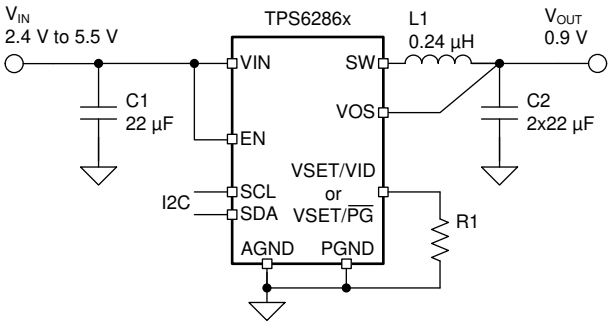


图 9-21. Smaller Application

9.2.2.1 Design Requirements

For this design, use the parameters listed in 表 9-5 as the input parameters. The design (表 9-6) is optimized for the smallest solution size.

表 9-5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.3 V
Output voltage	0.9 V
Maximum output current	4 A
Ambient temperature	25°C

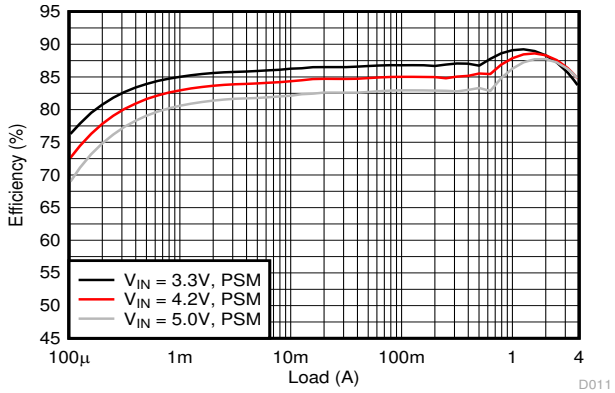
表 9-6. List of Components of Table 9-5

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1, C2	22 µF, Ceramic capacitor, 6.3 V, X5R, size 0402, GRM155R60J226ME11	Murata
L1	0.24 µH, Power inductor, size 0806, DFE201612E-R24M	Murata
R1	Depending on the startup output voltage, size 0402	Std

(1) See *Third-party Products* disclaimer.

9.2.2.2 Application Curves

V_{IN} = 5.0 V, V_{OUT} = 0.9 V, T_A = 25°C, BOM = 表 9-6, unless otherwise noted.



V_{OUT} = 0.9 V

图 9-22. Efficiency

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application. The power supply must avoid a fast ramp down. The falling ramp speed must be slower than 10 mV/µs, if the input voltage drops below V_{UVLO}.

11 Layout

11.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device.

- The input/output capacitors and the inductor must be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the PGND to avoid a GND potential shift.
- The sense traces connected to the VOS pin is a signal trace. Special care must be taken to avoid noise being induced. Keep the trace away from SW.
- Refer to 图 11-1 for an example of component placement, routing, and thermal design.

11.2 Layout Example

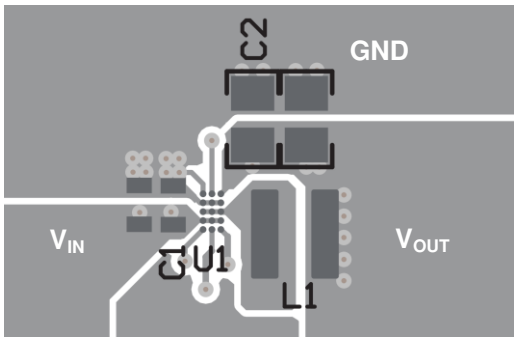


图 11-1. Layout Example

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are improving the power dissipation capability of the PCB design and introducing airflow in the system. For more details on how to use the thermal parameters, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

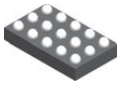
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

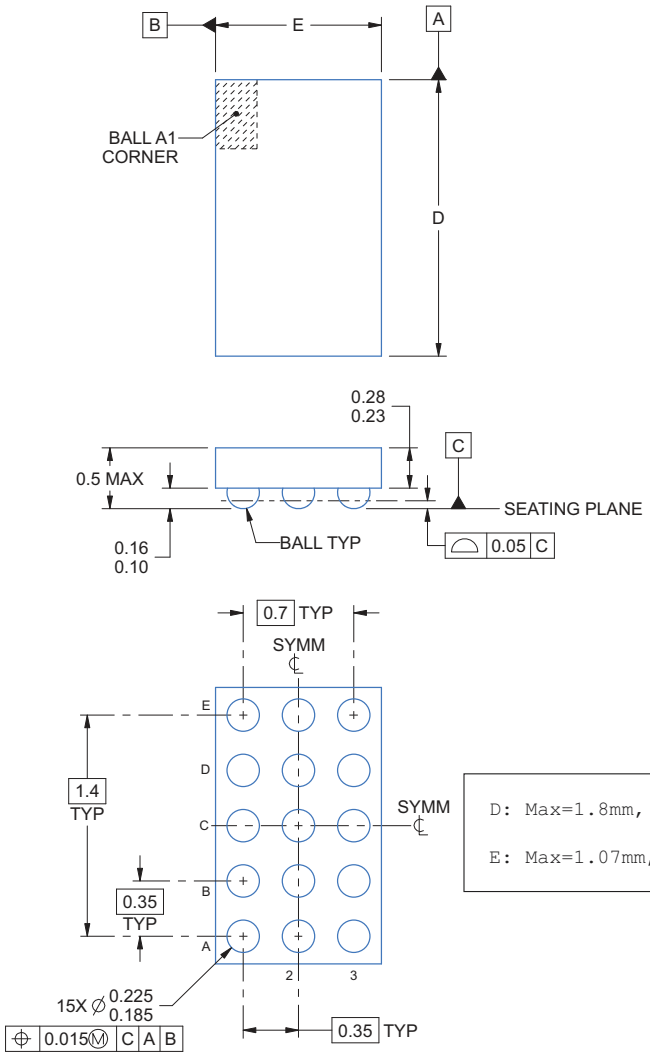


PACKAGE OUTLINE

YCG0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

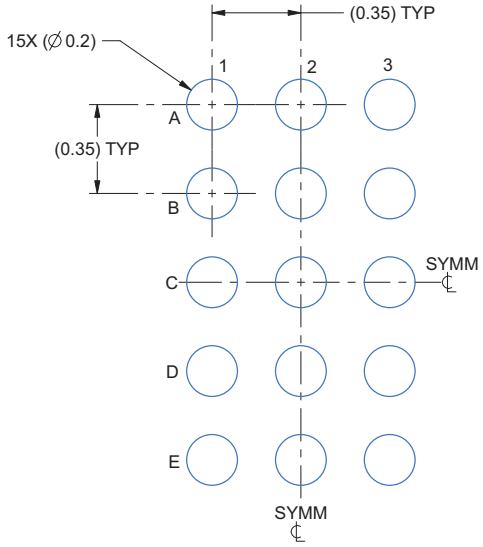
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

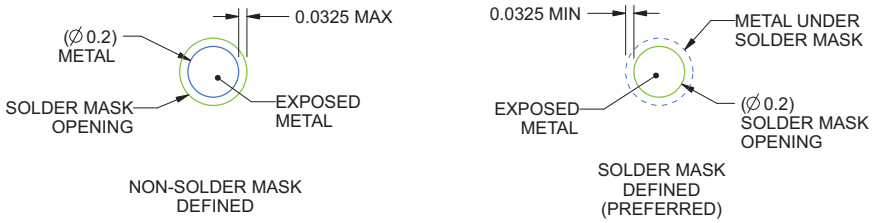
YCG0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4224261/B 08/2019

NOTES: (continued)

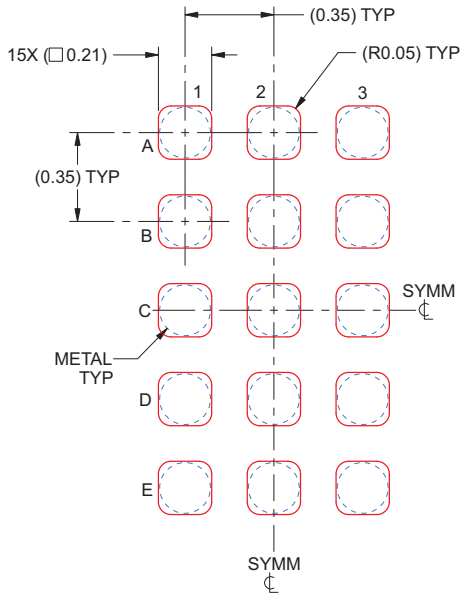
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCG0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

4224261/B 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS628640AYCGR	Active	Production	DSBGA (YCG) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8640A
TPS628640AYCGR.A	Active	Production	DSBGA (YCG) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8640A
TPS628640BYCGR	Active	Production	DSBGA (YCG) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8640B
TPS628640BYCGR.A	Active	Production	DSBGA (YCG) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8640B
TPS628660AYCGR	Active	Production	DSBGA (YCG) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8660A
TPS628660AYCGR.A	Active	Production	DSBGA (YCG) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8660A
TPS628660BYCGR	Active	Production	DSBGA (YCG) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8660B
TPS628660BYCGR.A	Active	Production	DSBGA (YCG) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8660B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

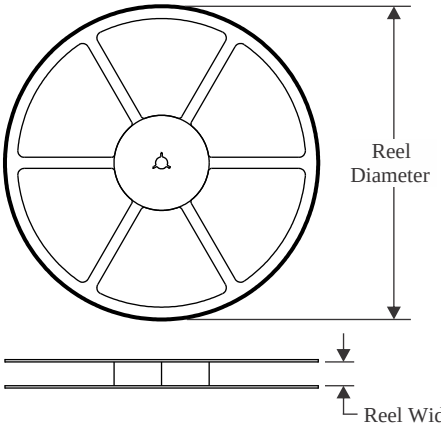
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

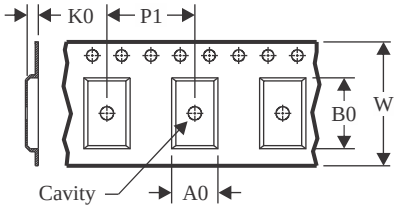
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

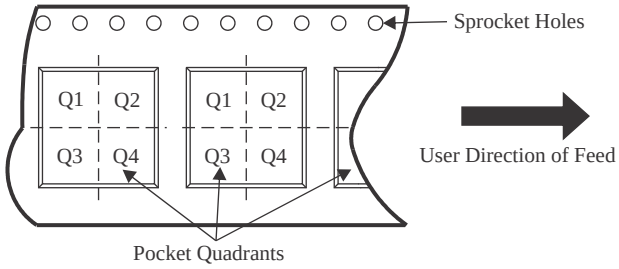


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

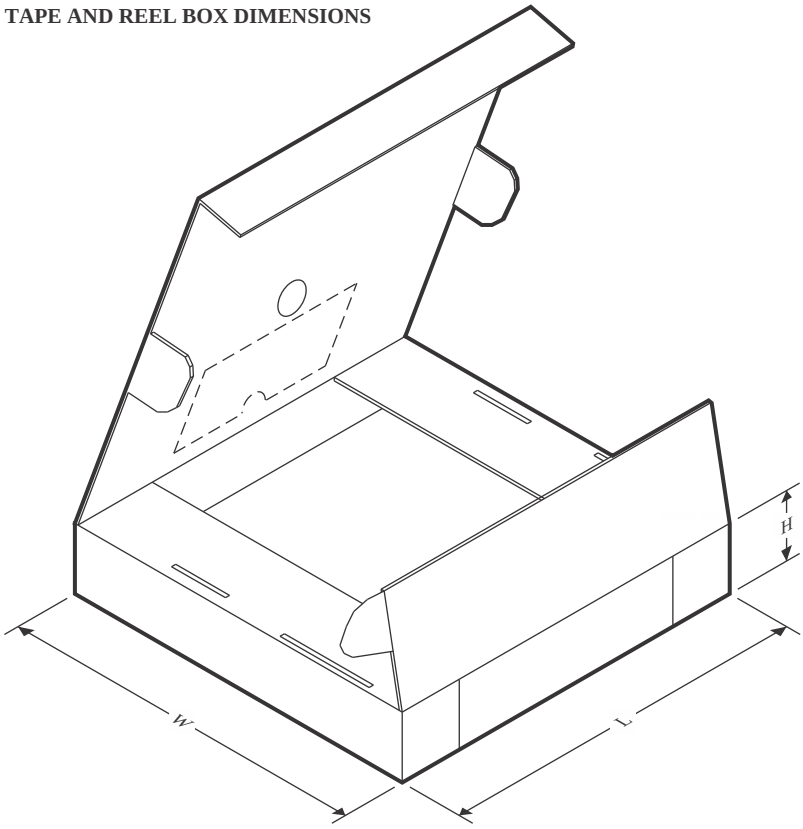
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS628640AYCGR	DSBGA	YCG	15	3000	180.0	8.4	1.22	1.95	0.6	4.0	8.0	Q1
TPS628640BYCGR	DSBGA	YCG	15	3000	180.0	8.4	1.22	1.95	0.6	4.0	8.0	Q1
TPS628660AYCGR	DSBGA	YCG	15	3000	180.0	8.4	1.22	1.95	0.6	4.0	8.0	Q1
TPS628660BYCGR	DSBGA	YCG	15	3000	180.0	8.4	1.22	1.95	0.6	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

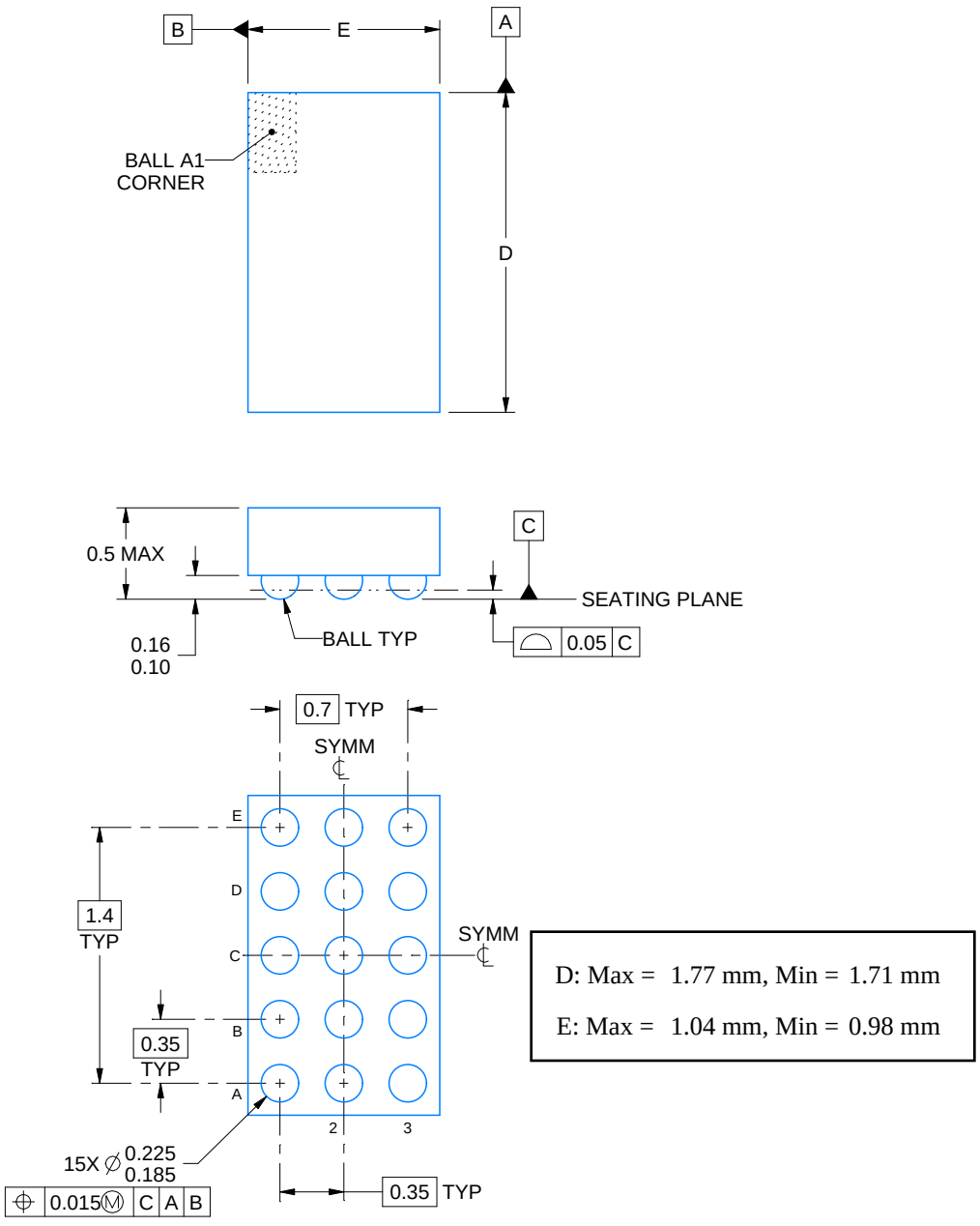
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS628640AYCGR	DSBGA	YCG	15	3000	182.0	182.0	20.0
TPS628640BYCGR	DSBGA	YCG	15	3000	182.0	182.0	20.0
TPS628660AYCGR	DSBGA	YCG	15	3000	182.0	182.0	20.0
TPS628660BYCGR	DSBGA	YCG	15	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YCG0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



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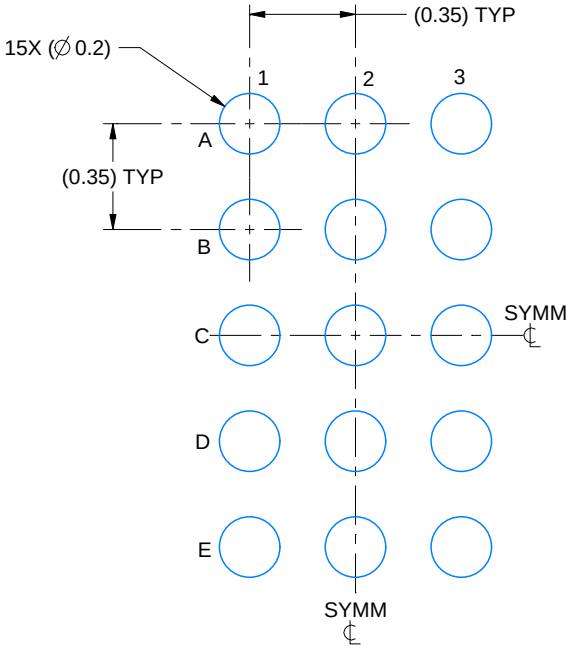
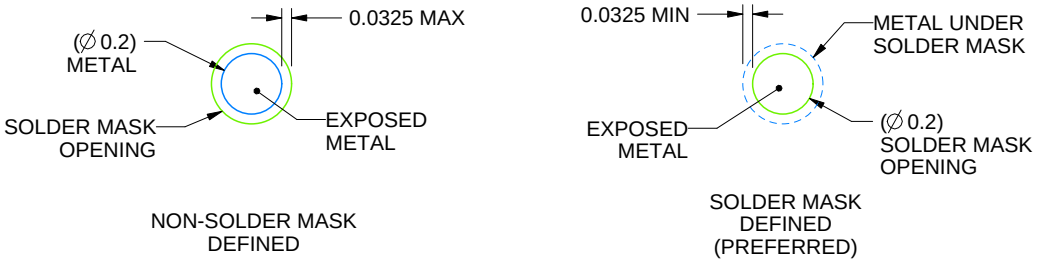
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

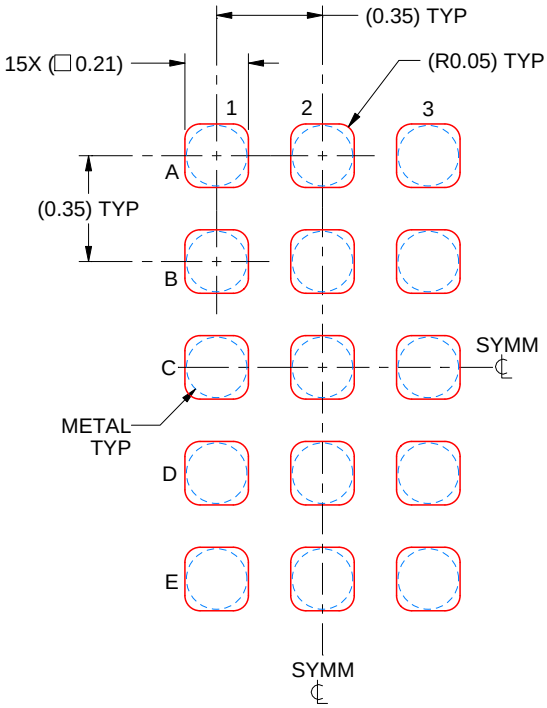
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCG0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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