DDC / 薄型小外形尺寸晶体管 (TSOT)23 封装内的 2.25MHz 300mA 降压转换器

查询样品: TPS62242-Q1

特性

- 符合汽车应用要求
- 具有符合 **AEC-Q100** 的下列结果：
  - 器件温度 **2** 级
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H2**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C4B**
- 高效率-大于 **94%**
- 输出电流高达 **300mA**
- V_{IN} 范围从 **2V** 至 **6V**
- **2.25MHz** 固定频率运行
- 轻负载电流上的省电模式
- 脉宽调制 **(PWM)** 模式中的输出电压精度为 **±1.5%**
- **1.2V** 固定输出电压
- 典型值为 **15μA** 的静态电流
- 针对最低压降的 **100%** 占空比
- 采用 **TSOT23** 封装
- 允许 **< 1mm** 的解决方案高度

应用范围

- 汽车应用
- **Bluetooth™** 耳机
- 手机、智能电话
- 无线局域网 **(WLAN)**
- 低功耗数字信号处理器 **(DSP)** 电源
- 便携式媒体播放器

说明

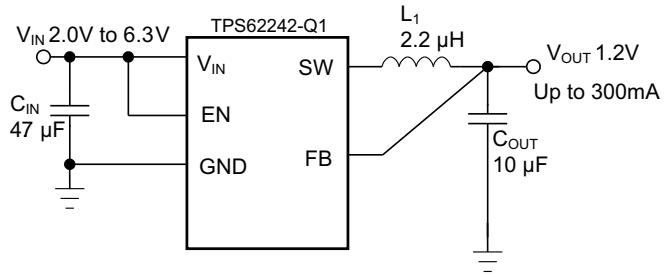
TPS62242-Q1 器件是一款针对电池供电类便携式应用进行了优化的高效同步降压转换器。 它使用一个单一锂离子电池提供高达 300mA 的输出电流并且此器件非常适合于为诸如移动电话和其它便携式设备的便携式应用供电。

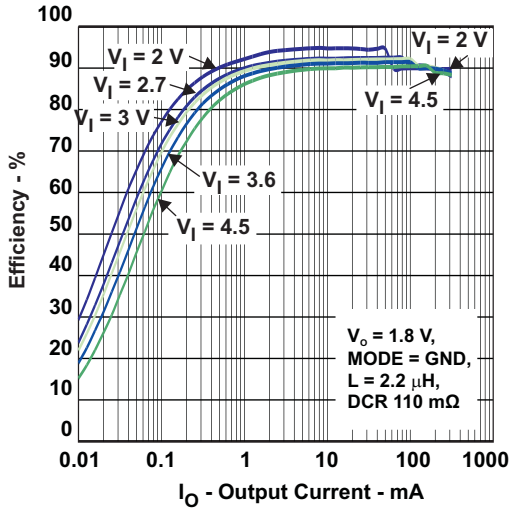
借助于 2V 至 6V 的输入电压范围，此器件支持由具有扩展电压范围的锂离子电池、两节和三节碱性电池、3.3V 和 5V 输入电压电源轨供电的应用。

TPS62242-Q1 运行在 2.25MHz 固定频率下并在轻负载电流时进入省电运行模式以在整个负载电流范围内保持高效率。

此省电模式针对低输出电压纹波进行了优化。 在关断模式下，流耗减少至小于 1μA。 为了实现小解决方案尺寸，TPS62242-Q1 允许使用小型电感器和电容器。

TPS62242-Q1 采用 5 引脚 TSOT23 封装方式。





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE	OUTPUT	ORDERABLE PART NUMBER(2)	TOP-SIDE MARKING
–40°C to 115°C	TSOT23-5 – DDC Reel of 3000	1.2 V fixed	TPS62242QDDCRQ1	SAW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
V_I	Input voltage range(2)		–0.3 to 7	V
	Voltage range at EN		–0.3 to V_{IN} +0.3, ≤7	V
	Voltage on SW		–0.3 to 7	V
	Peak output current		Internally limited	A
	ESD rating(3)	Human Body Model (HBM) AEC-Q100 Classification Level H2	2	kV
		Charged Device Model (CDM) AEC-Q100 Classification Level C4B	750	V
T_J	Maximum operating junction temperature		–40 to 150	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The human body model is a 100-pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	POWER RATING FOR T_A ≤ 25°C	DERATING FACTOR ABOVE T_A = 25°C
DDC	250°C/W	400 mW	4 mW/°C

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Supply voltage, VIN	2		6	V
	Output voltage range for adjustable voltage	0.6		VIN	V
T_A	Operating ambient temperature	–40		115	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 4.7 µF 0603, C_{OUT} = 10 µF 0603, L = 2.2 µH, refer to parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2		6	V
I_{OUT}	Output current	2.3 V ≤ V_{IN} ≤ 6 V			300	mA
		2 V ≤ V_{IN} ≤ 2.3 V			150	
I_Q	Operating quiescent current	I_{OUT} = 0 mA. PFM mode enabled, device not switching		15		µA
		I_{OUT} = 0 mA. PFM mode enabled, device switching, V_{OUT} = 1.8 V (1)		18.5		
		I_{OUT} = 0 mA, switching with no load , PWM operation , V_{OUT} = 1.8 V, V_{IN} = 3 V		3.8		mA
I_{SD}	Shutdown current	EN = GND, T_A = 25°C		0.1	1	µA
		EN = GND, T_A = –40°C to 115°C			5	µA
UVLO	Undervoltage lockout threshold	Falling		1.85		V
		Rising		1.95		
ENABLE, MODE						
V_{IH}	High level input voltage, EN	2 V ≤ V_{IN} ≤ 6 V	1		V_{IN}	V
V_{IL}	Low level input voltage, EN	2 V ≤ V_{IN} ≤ 6 V, T_A = 25°C	0		0.4	V
		2 V ≤ V_{IN} ≤ 6 V , T_A = –40°C to 115°C			0.35	V
I_{IN}	Input bias current, EN	EN		0.01	1	µA
POWER SWITCH						
$R_{DS(on)}$	High side MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V, T_A = 25°C		240	480	mΩ
	Low side MOSFET on-resistance			180	380	
I_{LIMF}	Forward current limit MOSFET high-side and low side	V_{IN} = V_{GS} = 3.6 V, T_A= 25°C	0.56	0.7	0.84	A
		V_{IN} = V_{GS} = 3.6 V, T_A = –40°C to 115°C	0.54		0.95	
TSD	Thermal shutdown	Increasing junction temperature	135	150	165	°C
	Thermal shutdown hysteresis	Decreasing junction temperature	12	14	16	°C
OSCILLATOR						
f_{SW}	Oscillator frequency	2 V ≤ V_{IN} ≤ 6 V	2	2.25	2.5	MHz
OUTPUT						
V_{OUT}	Output voltage			1.2		V
V_{REF}	Reference voltage	T_A = 25°C	594	600	606	mV

(1) See the parameter measurement information.

ELECTRICAL CHARACTERISTICS (continued)

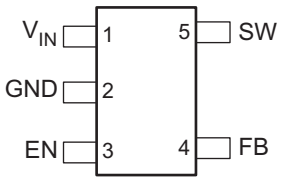
Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 4.7 µF 0603, C_{OUT} = 10 µF 0603, L = 2.2 µH, refer to parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage	PWM operation, 2 V ≤ V_{IN} ≤ 6 V, in fixed output voltage versions V_{FB} = V_{OUT}, See (2) ,T_A = 25°C	–1.5%	0%	1.5%	
		PWM operation, 2 V ≤ V_{IN} ≤ 6 V, in fixed output voltage versions V_{FB} = V_{OUT}, See (2) ,T_A = –40°C to 115°C	–1.5%		2.5%	
	Feedback voltage PFM mode	Device in PFM mode		0%		
	Load regulation			–0.5		%/A
$t_{Start\ Up}$	Start-up Time	Time from active EN to reach 95% of V_{OUT} nominal		500		µs
t_{Ramp}	V_{OUT} ramp UP time	Time to ramp from 5% to 95% of V_{OUT}		250		µs
I_{lkg}	Leakage current into SW pin	V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND,(3) , T_A = 25°C		0.1	1	µA
		V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND, (3), T_A = –40°C to 115°C			10	

(2) for V_{IN} = V_O + 0.6
(3) In fixed output voltage versions, the internal resistor divider network is disconnected from FB pin.

PIN ASSIGNMENTS

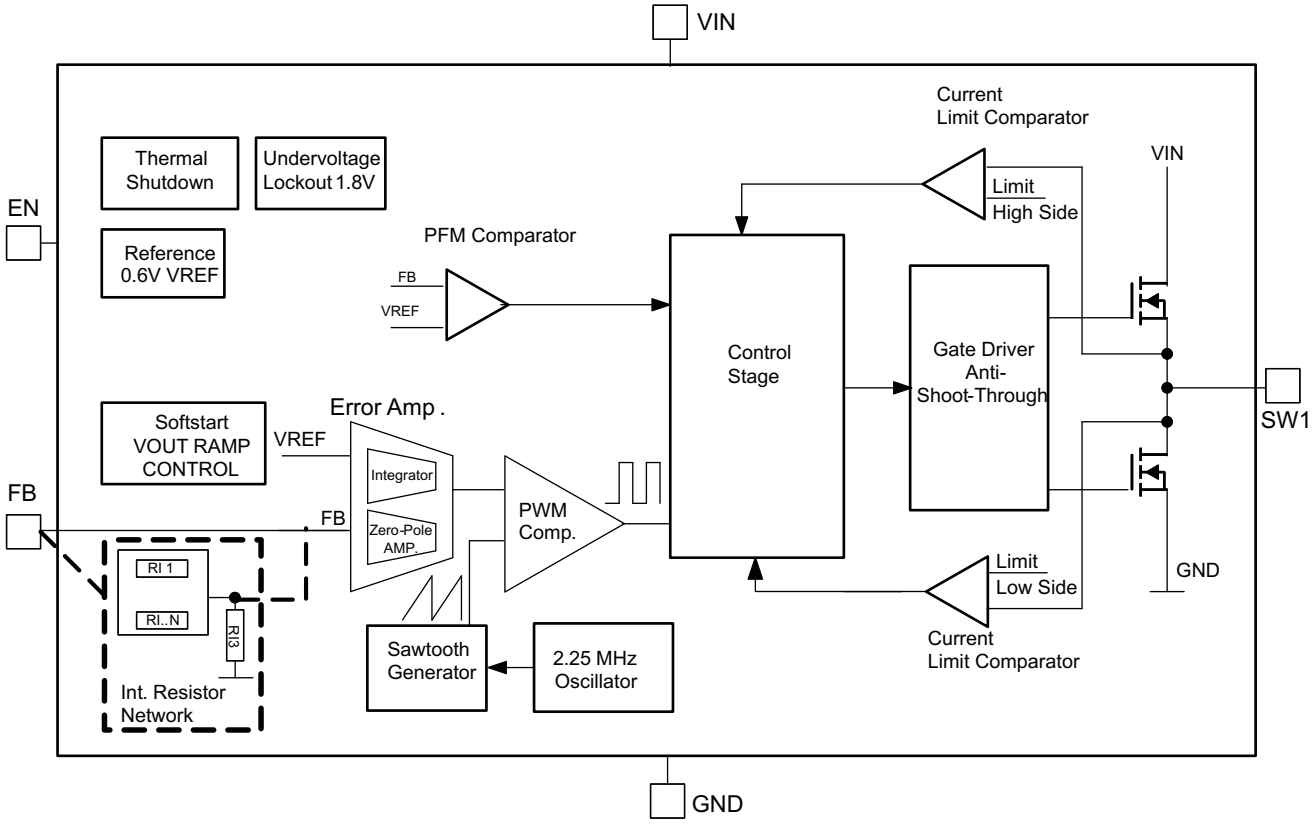
DDC PACKAGE
(TOP VIEW)



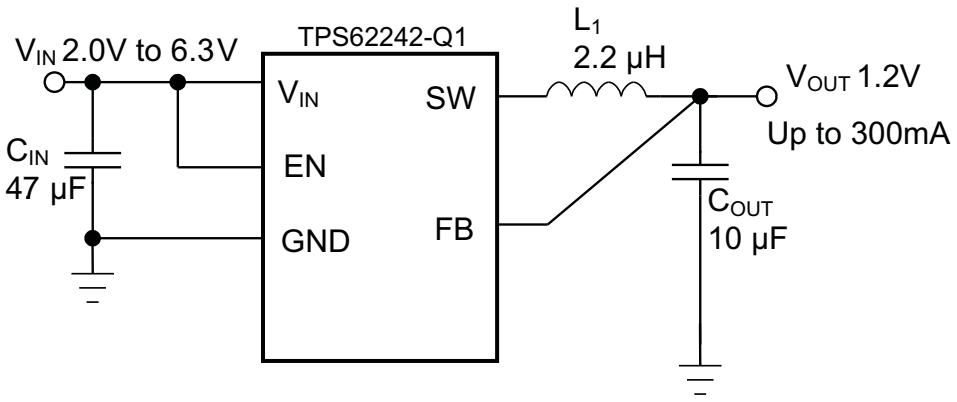
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{IN}	1	PWR	V_{IN} power supply pin.
GND	2	PWR	GND supply pin
EN	3	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
SW	5	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal.
FB	4	I	Feedback Pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

		FIGURE
Efficiency	vs Output current, Power Save Mode	Figure 1
	vs Output current, Forced PWM Mode	
	vs Output current	
	vs Output current	
Output voltage accuracy	vs Output current, T_A = 25°C	Figure 3
	vs Output current, T_A = –40°C	Figure 4
	vs Output current, T_A = 85°C	Figure 5
	vs Output current, T_A = 25°C	
	vs Output current, T_A = 85°C	
	vs Output current, T_A = –40°C	
Startup timing		Figure 6
Typical operation	PWM Mode with V_O = 1.8 V	Figure 7
	PFM Mode with V_O = 1.8 V	Figure 8
	PFM Mode Ripple	Figure 9
PFM load transient	1 mA to 50 mA with V_O = 1.8 V	Figure 10
	20 mA to 200 mA with V_O = 1.8 V	Figure 11
	50 mA to 200 mA with V_O = 1.8 V	
PFM line transient	I_O = 50 mA, 3.6 V to 4.2 V	Figure 12
	I_O= 250 mA, 3.6 V to 4.2 V	Figure 13
Mode transition	PFM to PWM	Figure 14
	PWM to PFM	Figure 15
Shutdown Current into VIN	vs Input Voltage, (T_A = 85°C, T_A = 25°C, T_A = –40°C)	Figure 16
Quiescent Current	vs Input Voltage, (T_A = 85°C, T_A = 25°C, T_A = –40°C)	Figure 17
Static Drain-Source On-State Resistance	vs Input Voltage, (T_A = 85°C, T_A = 25°C, T_A = –40°C)	Figure 18
		Figure 19

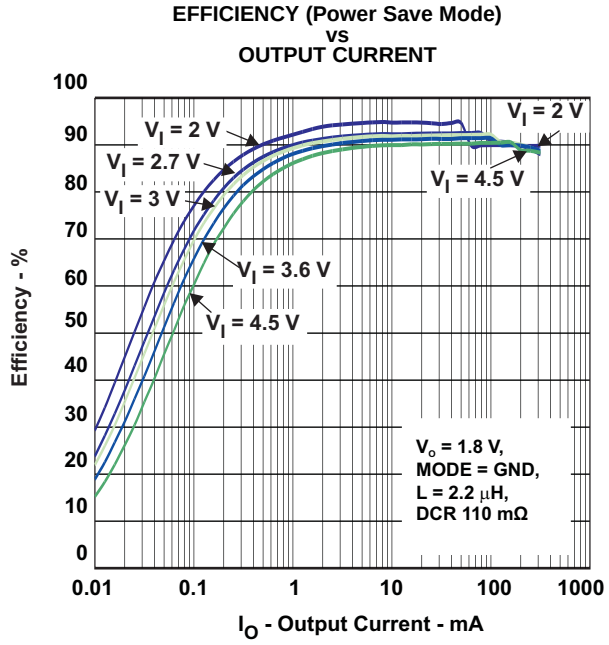


Figure 1.

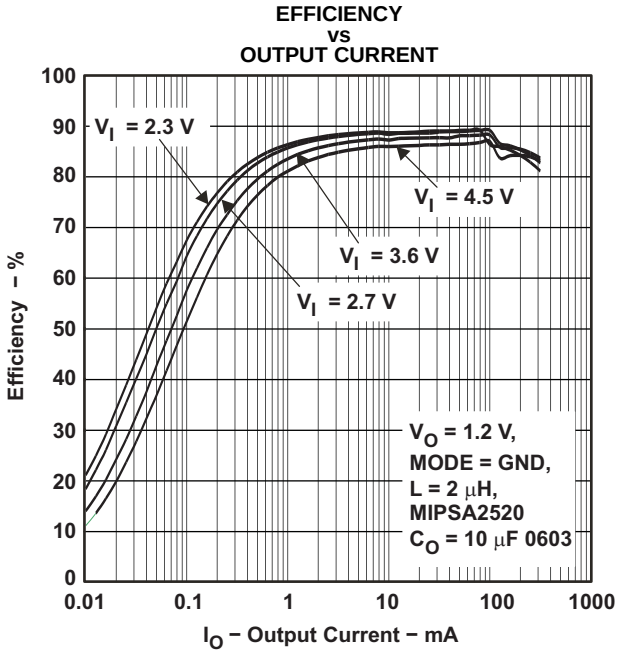


Figure 2.

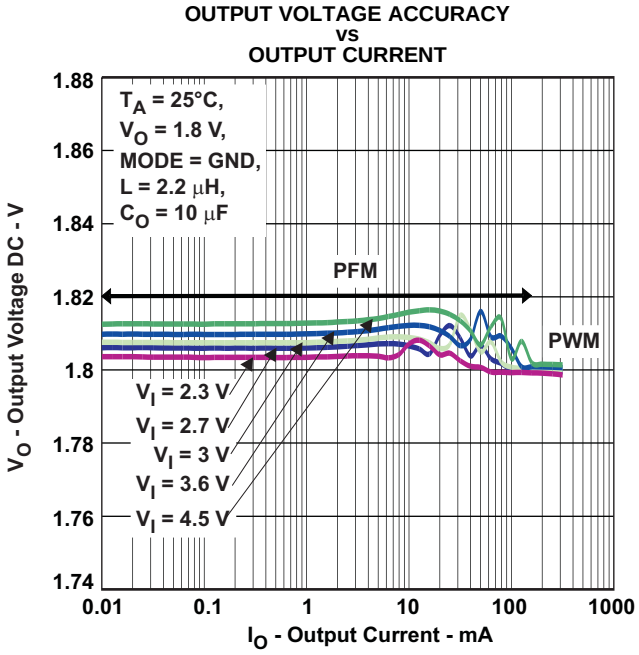


Figure 3.

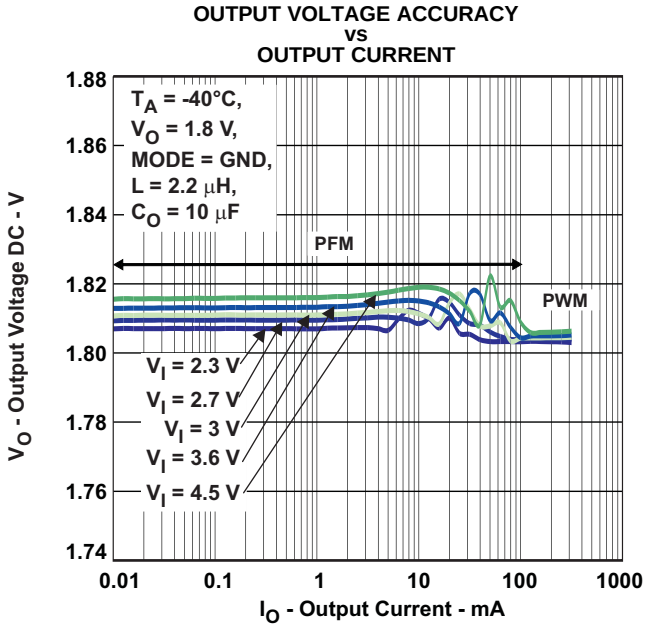


Figure 4.

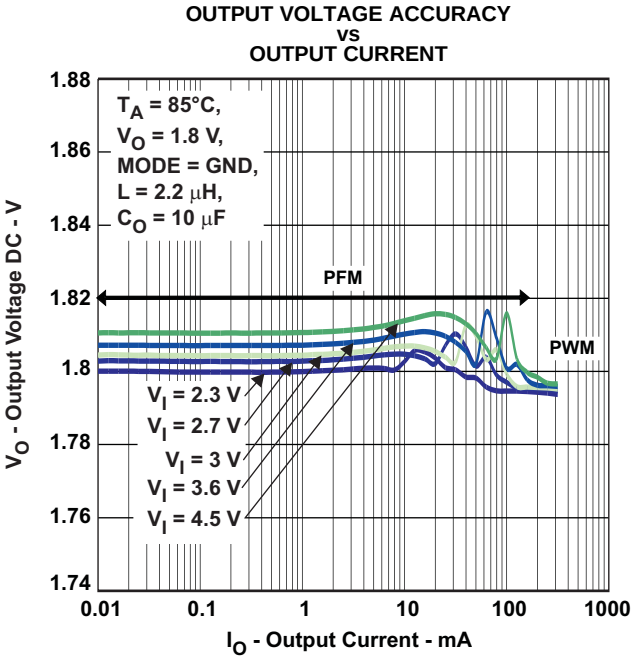


Figure 5.

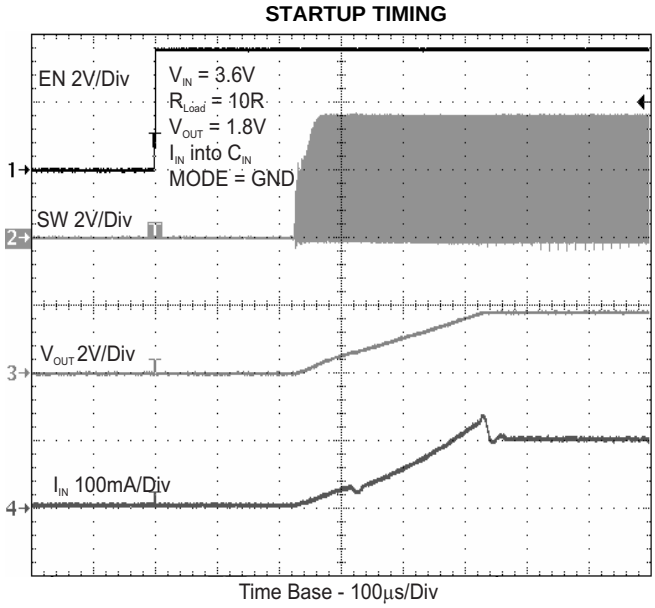


Figure 6.

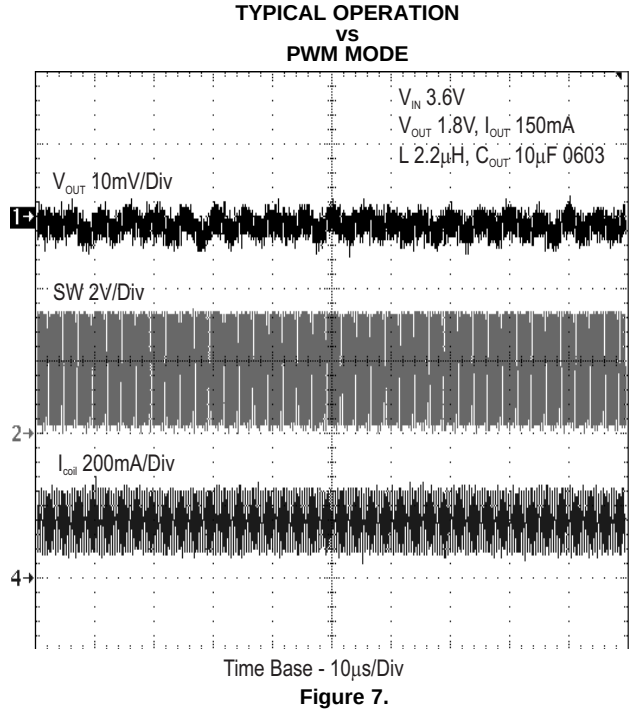


Figure 7.

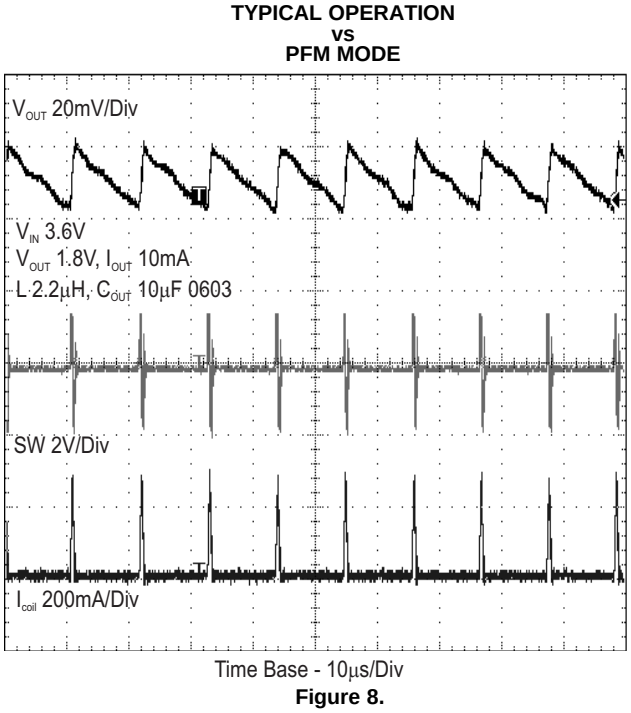


Figure 8.

PFM MODE RIPPLE

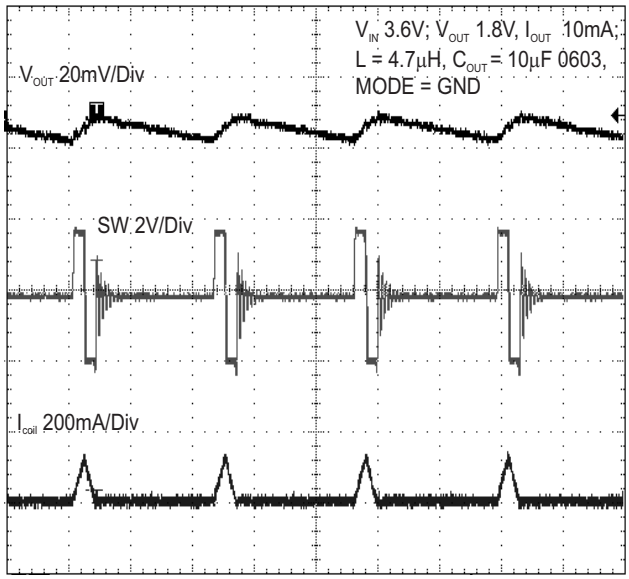


Figure 9.

PFM LOAD TRANSIENT

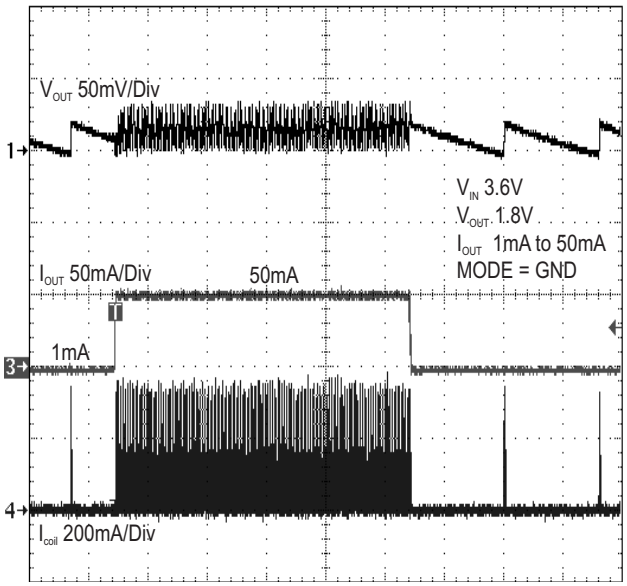


Figure 10.

PFM LOAD TRANSIENT

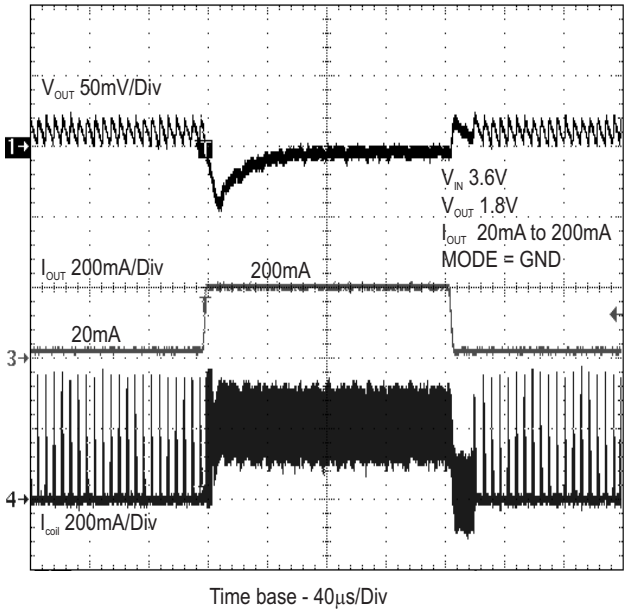


Figure 11.

PFM LINE TRANSIENT

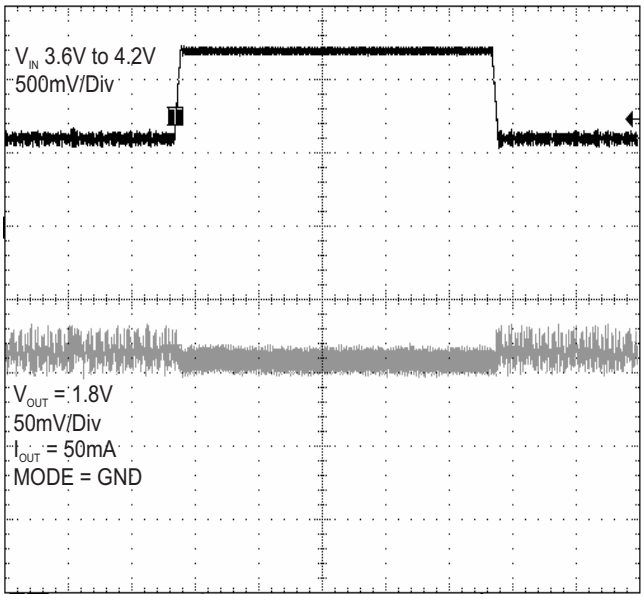


Figure 12.

PFM LINE TRANSIENT

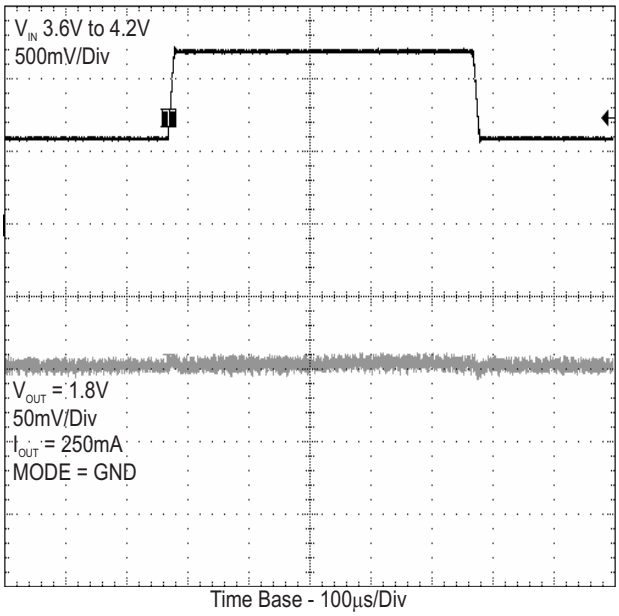


Figure 13.

MODE TRANSITION
PFM to PWM

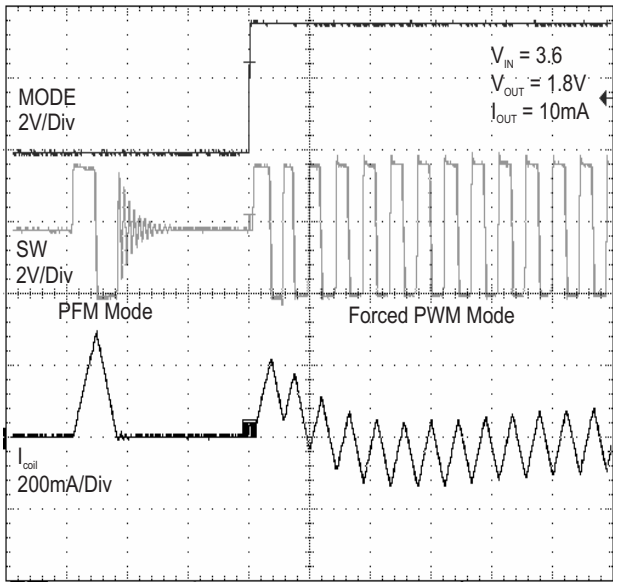


Figure 14.

MODE TRANSITION
PWM to PFM

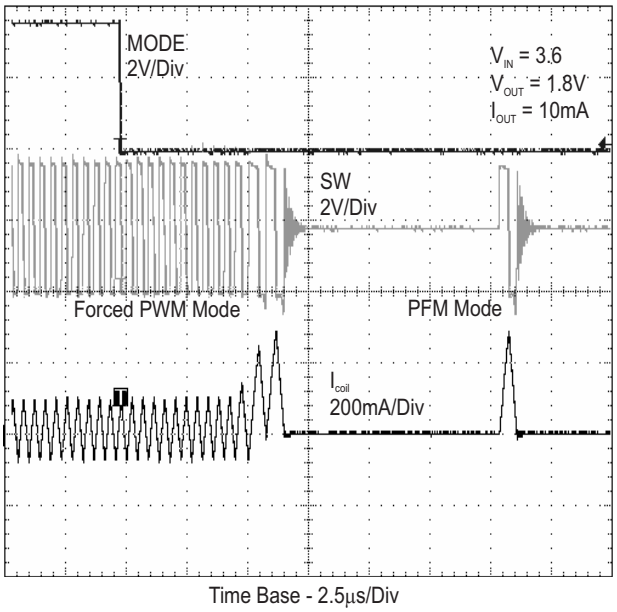


Figure 15.

SHUTDOWN CURRENT INTO VIN
vs
INPUT VOLTAGE

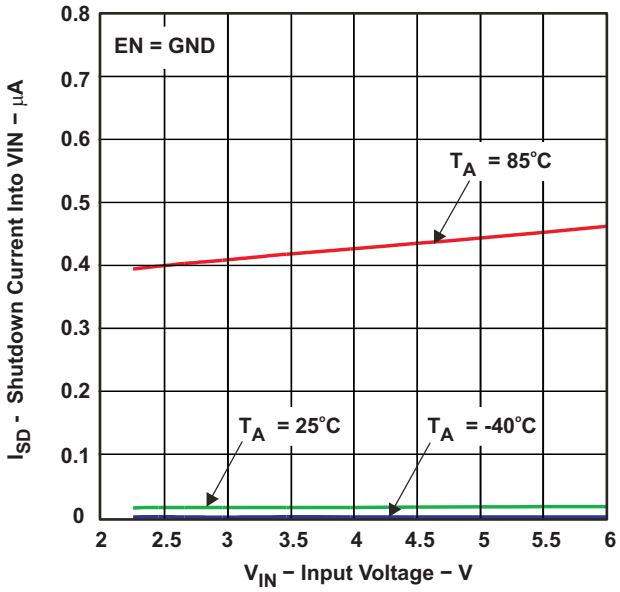


Figure 16.

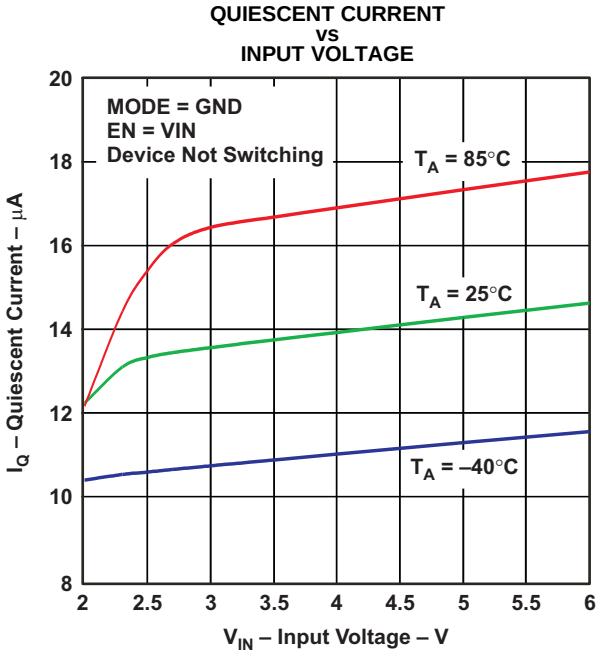


Figure 17.

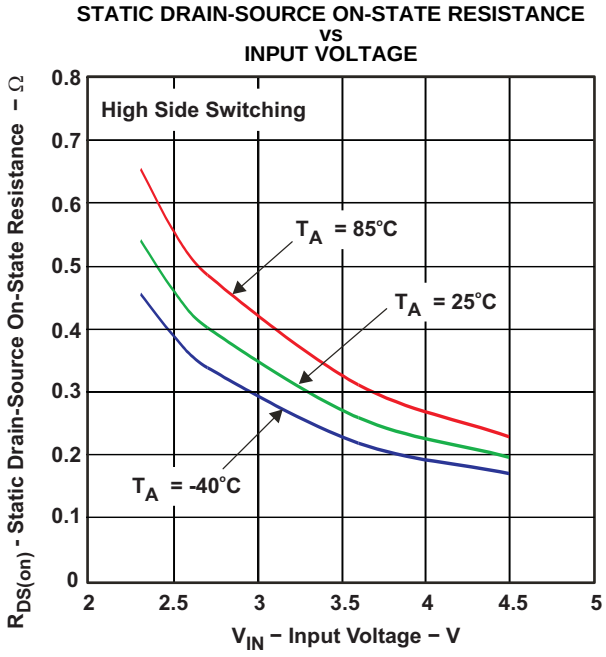


Figure 18.

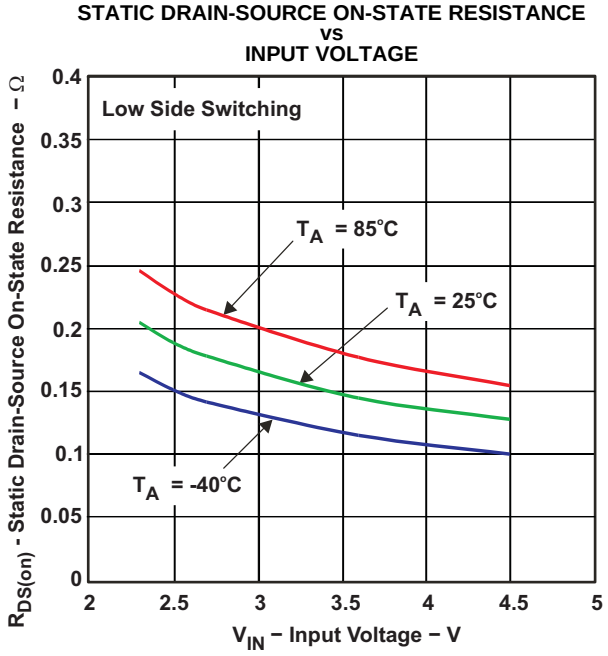


Figure 19.

DETAILED DESCRIPTION

OPERATION

The TPS62242-Q1 step down converter typically operates with 2.25 MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power save mode and then operates in PFM mode.

During PWM operation, the converter uses a unique fast response voltage mode control scheme with input voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current then flows from the input capacitor via the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch if the current limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot through current, the low-ide MOSFET rectifier is turned on and the inductor current ramps down. The current then flows from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

POWER SAVE MODE

The power save mode is enabled. If the load current decreases, the converter enters power save mode operation automatically. During power save mode, the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency.

The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the power save mode, the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of V_{OUT} nominal, the device starts a PFM current pulse. The high-side MOSFET switch turns on, and the inductor current ramps up. After the On-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage rises. If the output voltage is equal to or greater than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15-µA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single-threshold comparator, the output voltage ripple during PFM mode operation can be kept to a minimum. The PFM Pulse is time controlled, allowing the user to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency both depend on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values minimize the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values.

If the output current cannot be supported in PFM mode, the device exits PFM mode and enters PWM mode.

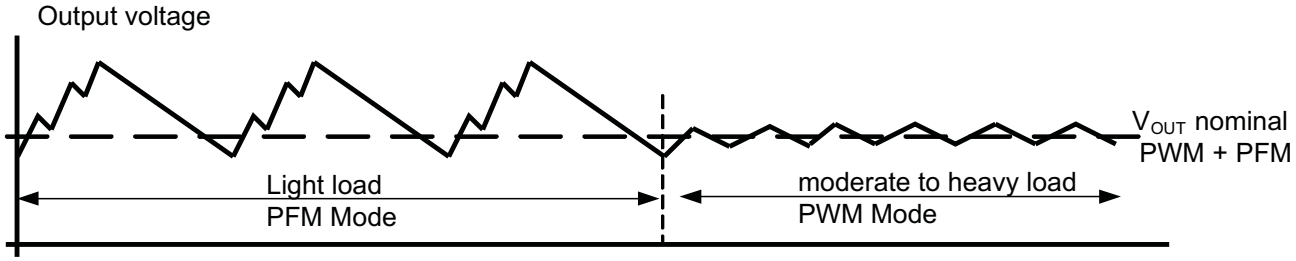


Figure 20. Power Save Mode

100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the high side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing V_{IN} the high side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the entire battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$V_{IN}min = V_Omax + I_Omax (R_{DS(on)}max + R_L)$

With:

$I_O$max = maximum output current plus inductor ripple current
$R_{DS(on)}$max = maximum P-channel switch $R_{DS(on)}$.
R_L = DC resistance of the inductor
$V_O$max = nominal output voltage plus maximum output voltage tolerance

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85 V with falling V_{IN}.

ENABLE

The device is enabled by setting the EN pin to high. During the start up time $t_{Start\ Up}$, the internal circuits are settled and the soft start circuit is activated. The EN input can be used to control power sequencing in a system with various dc/dc converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN pin = GND, the device enters shutdown mode in which all circuits are disabled. In fixed output voltage versions, the internal resistor divider network is then disconnected from FB pin.

SOFT START

The TPS62242-Q1 has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typical 250µs. This limits the inrush current in the converter during ramp up and prevents possible input voltage drops when a battery or high impedance power source is used. The soft start circuit is enabled within the start up time, $t_{Start\ up}$.

SHORT-CIRCUIT PROTECTION

The high-side and low-side MOSFET switches are short-circuit protected with maximum switch current equal to I_{LIMF}. The current in the switches is monitored by current limit comparators. Once the current in the high-side MOSFET switch exceeds the threshold of it's current limit comparator, it turns off and the low-side MOSFET switch is activated to ramp down the current in the inductor and high-side MOSFET switch. The high-side MOSFET switch can only turn on again, once the current in the low-side MOSFET switch has decreased below the threshold of its current limit comparator.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

APPLICATION INFORMATION

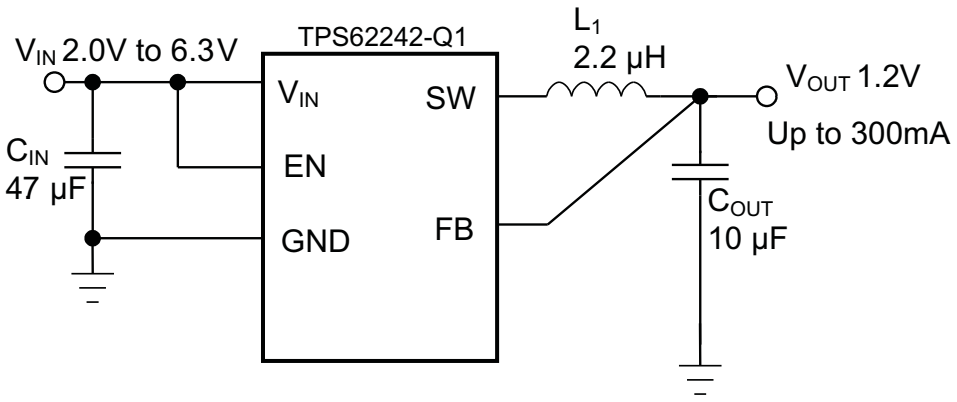


Figure 21. Fixed 1.2 V

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The TPS62242-Q1 is designed to operate with inductors in the range of 1.5 µH to 4.7 µH and with output capacitors in the range of 4.7 µF to 22 µF. The part is optimized for operation with a 2.2 µH inductor and 10 µF output capacitor.

Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter may not fall below 1 µH effective Inductance and 3.5 µF effective capacitance. Selecting larger capacitors is less critical because the corner frequency of the L-C filter moves to lower frequencies with fewer stability problems.

Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

The inductor selection also has an impact on the output voltage ripple in the PFM mode. Higher inductor values lead to lower output voltage ripple and higher PFM frequency, and lower inductor values lead to a higher output voltage ripple but lower PFM frequency.

Equation 1 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. This is recommended because during heavy load transients the inductor current rises above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

With:

f = Switching Frequency (2.25 MHz typical)
L = Inductor Value
ΔI_L = Peak to Peak inductor ripple current
I_{Lmax} = Maximum Inductor current

A more conservative approach is to select the inductor current rating just for the maximum switch current limit I_{LIMF} of the converter.

Accepting larger values of ripple current allows the use of low inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil strongly impact the efficiency of the dc/dc conversion and consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 2. List of Inductors

DIMENSIONS [mm^3]	INDUCTANCE µH	INDUCTOR TYPE	SUPPLIER
2.5 × 2 × 1	2	MIPS2520D2R2	FDK
2.5 × 2 × 1.2	2	MIPSA2520D2R2	FDK
2.5 × 2 × 1	2.2	KSLI-252010AG2R2	Hitachi Metals
2.5 × 2 × 1.2	2.2	LQM2HPN2R2MJ0L	Murata
3 × 3 × 1.4	2.2	LPS3015	Coilcraft

Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS62242-Q1 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values are the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (3)$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (4)$$

At light load currents, the converter operates in power save mode and the output voltage ripple depends on the output capacitor and inductor value. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten dc output accuracy in PFM mode.

Input Capacitor Selection

The buck converter has a natural pulsating input current; therefore, a low ESR input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 4.7-µF to 10-µF ceramic capacitor is recommended. Because ceramic capacitors lose up to 80% of their initial capacitance at 5 V, it is recommended that a 10-µF input capacitor be used for input voltages greater than 4.5 V. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input, and the power is being supplied through long wires, such as from a wall adapter, a load step at the output, or VIN step on the input, can induce ringing at the VIN pin. The ringing can couple to the output and be mistaken as loop instability, or could even damage the part by exceeding the maximum ratings

Table 3. List of Capacitors

CAPACITANCE	TYPE	SIZE	SUPPLIER
4.7 µF	GRM188R60J475K	0603: 1.6 × 0.8 × 0.8 mm^3	Murata
10 µF	GRM188R60J106M69D	0603: 1.6 × 0.8 × 0.8 mm^3	Murata

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, and additional stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND pin of the device to the PowerPAD™ land of the PCB and use this pad as a star point. Use a common Power GND node and a different node for the Signal GND to minimize the effects of ground noise. Connect these ground nodes together to the PowerPAD land (star point) underneath the IC. Keep the common path to the GND pin, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. The FB line should be connected right to the output capacitor and routed away from noisy components and traces (for example, the SW line).

REVISION HISTORY

Changes from Revision A (March 2012) to Revision B **Page**

- 在特性中将 C3B 更改为 C4B 1
- Changed 将“特性”列表中的着重号点从“0.6V 至 $V_{输入}$的可调输出电压”改为“1.2V 固定输出电压” 1
- Added Output column for fixed voltage to Ordering Information table. 2
- Changed C3B to C4B in Abs Max table. 2
- Added EN = GND to I_{SD} test conditions. 3
- Added 2 V ≤ V_{IN} ≤ 6 V to V_{IL} test conditions. 3
- Added V_{IN} = V_{GS} = 3.6 V to I_{LIMF} test conditions. 3
- Changed min and typ values for V_{REF} from 0.594 to 594 and 0.606 to 606, respectively. 3
- Added PWM operation, 2 V ≤ V_{IN} ≤ 6 V, in fixed output voltage versions V_{FB} = V_{OUT}, See (2) to the V_{FB} test conditions. 4
- Added V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND,(3), to the I_{lkg} test conditions. 4
- Changed "T_a = 115°C" to "T_a = –40°C°C to 115°C" in all instances in the electrical characteristics table 5
- Changed - Added "T_a = 25°C" to following parameters listed in the electrical characteristics table: "Shutdown current," "Low level input voltage," "Feedback voltage," and "Leakage current into SW pin" 5
- Added missing parentheses to equation. 13
- Changed the junction temperature in the thermal shutdown detail from "TBD" to "150°C" 13

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62242QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 115	SAW
TPS62242QDDCRQ1.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 115	SAW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS62242-Q1 :

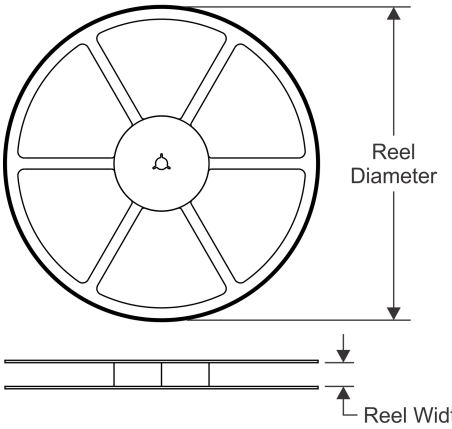
- Catalog : TPS62242

NOTE: Qualified Version Definitions:

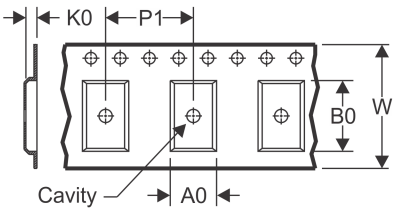
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

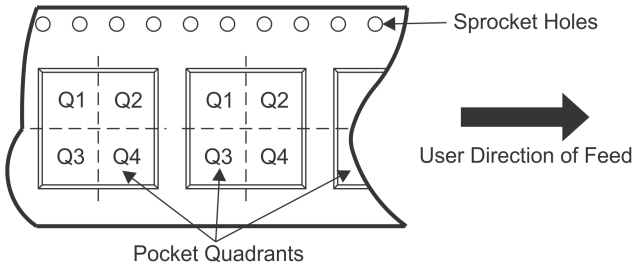


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

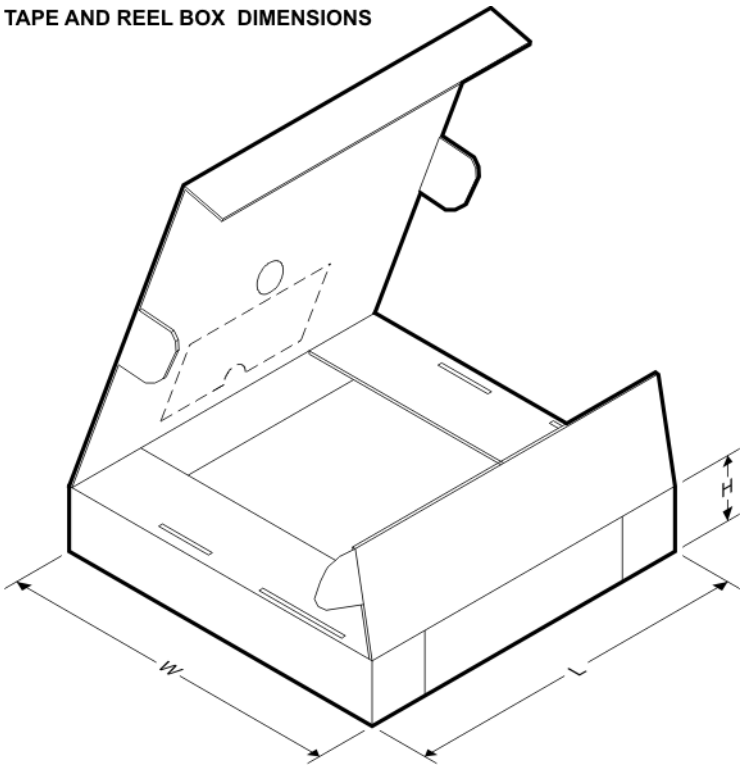
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62242QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

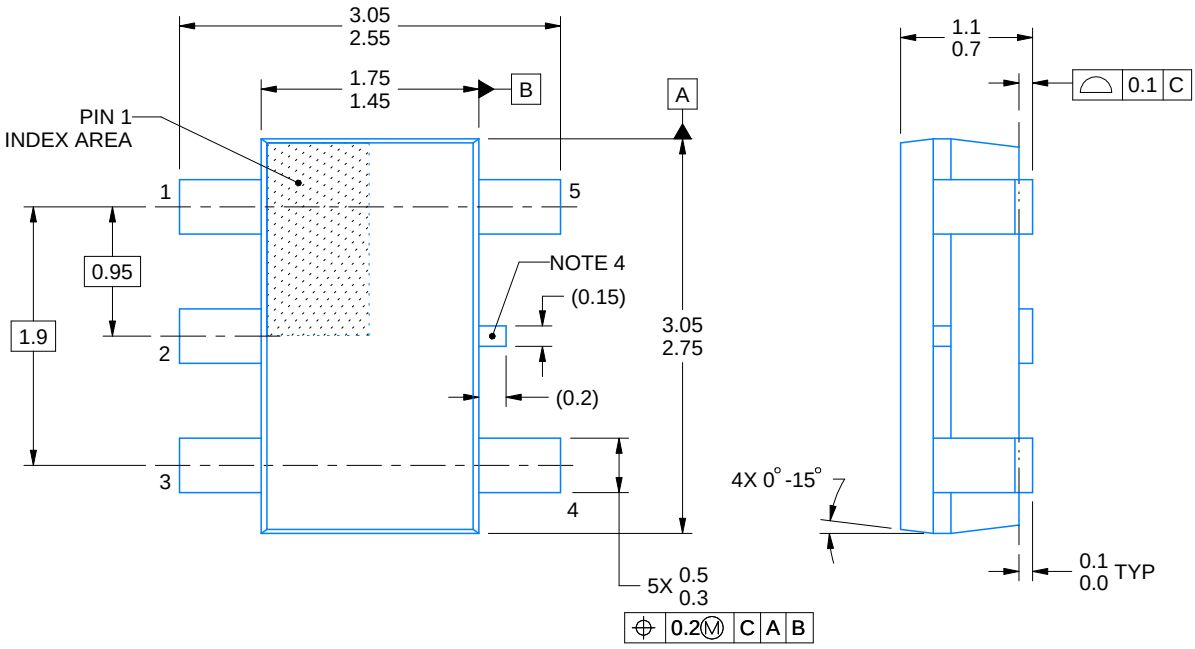
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62242QDDCRQ1	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0

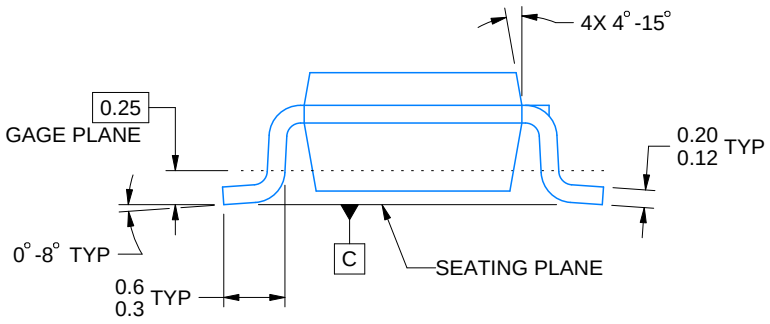
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR





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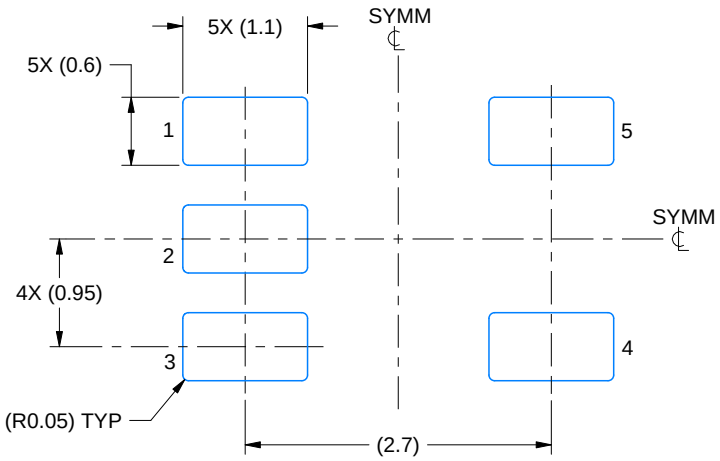
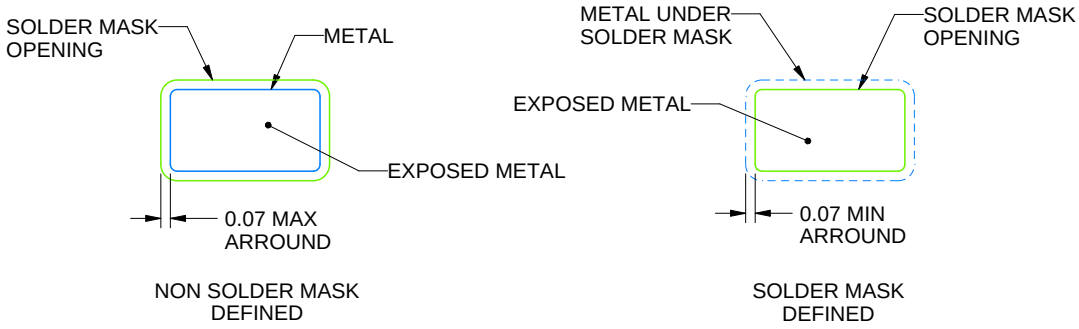
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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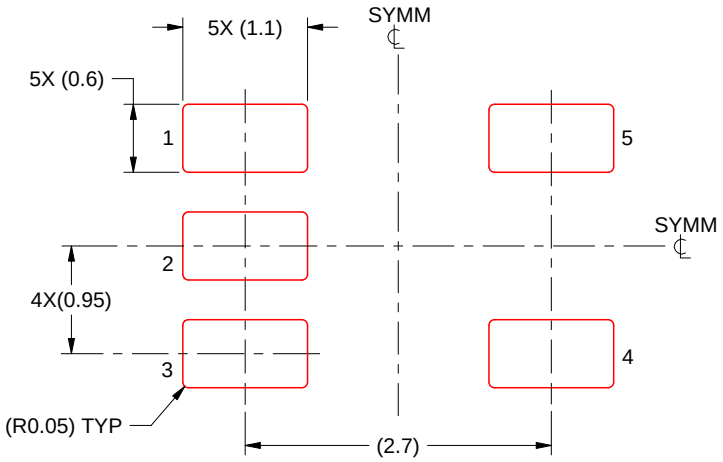
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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