TPS6218x 4V 至 15V、6A、双相降压转换器，具有 AEE™

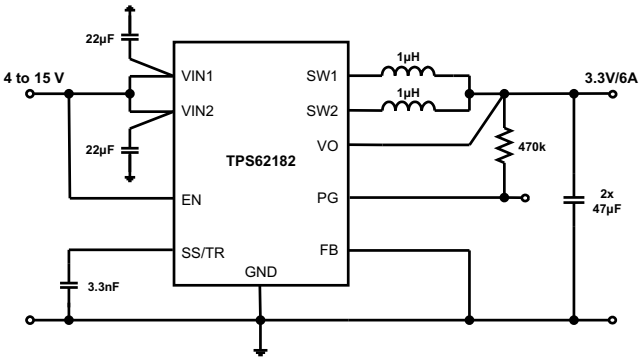
1 特性

- 双相平衡峰值电流模式
- 输入电压范围：4V 至 15V
- 输出电压范围：0.9V 至 6V
- 输出电流高达 6A
- 典型静态电流为 28µA
- 输出电压精度达 ±1%（脉宽调制 (PWM) 模式）
- 自动效率提高 (AEE™)
- 相移操作
- 自动节能模式
- 可调软启动
- 电源正常输出
- 欠压闭锁
- HICCUP 过流保护
- 与 TPS62184 引脚对引脚兼容
- 过热保护
- NanoFree™2.10mm x 3.10mm 芯片尺寸球状引脚栅格阵列 (DSBGA) 封装
- 结合使用 TPS62180 和 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 薄型负载点 (POL) 电源
- 窄 VDC (NVDC) 供电系统
- 两/三节锂离子电池
- 超便携式/嵌入式/平板电脑
- 计算网络解决方案
- 微型服务器和固态硬盘 (SSD)

简化电路原理图



3 说明

TPS6218x 是一款适用于薄型电源轨的双相降压 DC-DC 转换器。它采用峰值电流控制且两相电流平衡，适合高度受限的应用。

该器件具有 4V 到 15V 的宽工作输入电压范围，非常适合通过多节锂离子电池或 12V 电源轨供电运行的系统。两相可持续提供 6A 输出电流（每相 3A），从而允许使用薄型外部元件。两相异相运行，这样可显著减小开关噪声。

TPS6218x 可在超轻负载时自动进入节能模式以保持高效率，并且还集成有自动效率提高功能 (*AEE*™)，适用于整个占空比范围。

该器件支持 电源正常信号和可调软启动。其静态电流典型值为 28µA，并且能够在 100% 模式下运行，即便在最低输出电压下也不存在占空比限制。

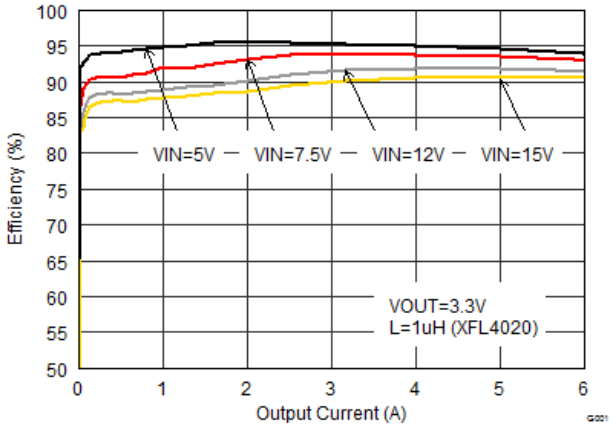
TPS6218x 提供了可调节输出电压和固定输出电压两种选项，并且采用 24 凸点、0.5mm 间距的小型 DSBGA 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS62180	DSBGA (24)	2.10mm x 3.10mm
TPS62182	DSBGA (24)	2.10mm x 3.10mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

效率与输出电流间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (August 2014) to Revision B **Page**

- 新增特性：与 TPS62184 引脚对引脚兼容 ... 1
- 已添加 WEBENCH® 信息 *特性*、*详细设计流程和开发支持*部分。 ... 1
- 在*器件信息*表中将“封装尺寸”值从 2.14mm x 3.14mm 更改为 2.10mm x 3.10mm ... 1
- Added SW1, SW2, (AC, less than 10ns) and Note (3) to the Pin voltage range in the *Absolute Maximum Ratings* table ... 4
- Changed Handling Ratings To: *ESD Ratings* table ... 4
- Added Table 1 ... 9
- Added the application note ... 14
- Changed the *Design Requirements* paragraph ... 14
- Added Note (2) to Table 6 ... 17
- Added Figure 31 and Figure 32 ... 21
- Added Figure 37 ... 22
- Changed the *Design Requirements* paragraph ... 24
- Added Figure 38 and Figure 39 to the *Inductor* section ... 24
- Changed Figure 55 ... 31

Changes from Original (August 2014) to Revision A **Page**

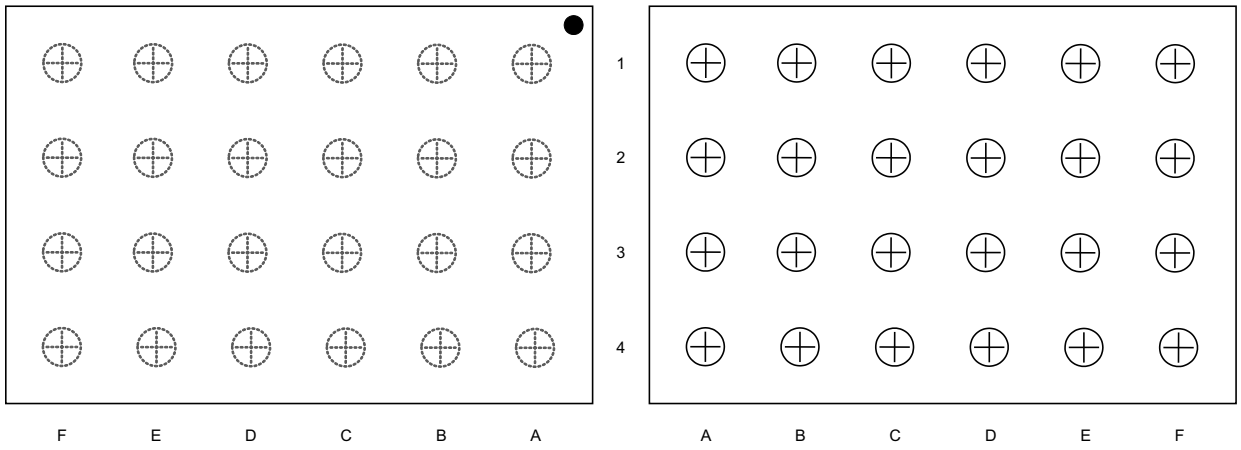
- 已投入量产 ... 1

5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	T_J
TPS62180	Adjustable	-40°C to 125°C
TPS62182	3.3 V	-40°C to 125°C

6 Pin Configuration and Functions

24-Pin DSBGA
YZF Package
(Top View - Left, Bottom View - Right)



Pin Functions

PIN (1)		DESCRIPTION
NAME	NUMBER	
AGND	C4	Analog Ground. Connect on PCB directly with PGND.
EN	E4	Enable input (High = enabled, Low = disabled)
FB	B4	Output voltage feedback. Connect resistive voltage divider to this pin and AGND. On TPS62182, connect to AGND.
PG	F4	Output power good (High = VOUT ready, Low = VOUT below nominal regulation); open drain (requires pull-up resistor)
PGND	A3, B3, C3, D3, E3, F3	Common power ground.
SS/TR	D4	Soft-Start and Tracking Pin. An external capacitor connected to this pin sets the internal voltage reference rise time.
SW1	A2, B2, C2	Switch node for Phase 1 (master), connected to the internal MOSFET switches. Connect inductor 1 between SW1 and output capacitor.
SW2	D2, E2, F2	Switch node for Phase 2 (follower), connected to the internal MOSFET switches. Connect inductor 2 between SW2 and output capacitor.
VIN1	A1, B1, C1	Supply voltage for Phase 1.
VIN2	D1, E1, F1	Supply voltage for Phase 2.
VO	A4	Output Voltage Connection

(1) For more information about connecting pins, see *Detailed Description* and *Application Information* sections.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Pin voltage range(2)	VIN1, VIN2	–0.3	17	V
	EN, PG	–0.3	V_{IN} + 0.3	V
	SW1, SW2, (DC)	–0.3	V_{IN} + 0.3	V
	SW1, SW2, (AC, less than 10ns)(3)	–2	24.5	
	SS/TR	–0.3	V_{IN} + 0.3, but ≤ 7	V
	FB, VO	–0.3	7	V
Power good sink current	PG		10	mA
Operating junction temperature range	T_J	–40	150	°C
Storage Temperature Range	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground pin.
(3) While switching.

7.2 ESD Ratings

		MIN	MAX	UNIT
V_{ESD}(1)	Human Body Model (HBM) ESD stress voltage(2)	–1	1	kV
	Charge device model (CDM) ESD stress voltage	–0.5	0.5	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
Supply voltage range, V_{IN}		4		15	V
Output voltage range, V_{OUT}		0.9		6	V
Maximum Output current, $I_{OUT(max)}$	0.9V ≤ V_{OUT} ≤ 3.3V	6			A
	3.3V < V_{OUT}		6		
Operating junction temperature, T_J		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6218x YZF (24 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.5	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance	10.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.1	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to +125°C) and V_{IN} = 4 V to 15 V.
Typical values at V_{IN} = 12 V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range			4		15	V
I_Q	Operating quiescent current	EN = High, I_{OUT} = 0 mA, Device not switching, (T_J = –40°C to +85°C)			28	55	µA
I_{SD}	Shutdown current	EN = Low (≤ 0.3 V), (T_J = –40°C to +85°C)			2.8	15	µA
V_{UVLO}	Undervoltage lockout threshold (1)	Falling input voltage		3.5	3.6	3.7	V
		Hysteresis			300		mV
T_{SD}	Thermal shutdown	Rising junction temperature			160		°C
		Hysteresis			20		
CONTROL (EN, SS/TR, PG)							
V_{H_EN}	High-level input threshold voltage (EN)			0.97	1	1.03	V
V_{L_EN}	Low-level input threshold voltage (EN)			0.87	0.9	0.93	V
I_{LKG_EN}	Input leakage current (EN)	EN = V_{IN} or GND			0.01	1.2	µA
$I_{SS/TR}$	SS/TR pin source current			4.5	5	5.5	µA
V_{TH_PG}	Power good threshold voltage	Rising (%V_{OUT})		94%	96%	98%	
		Falling (%V_{OUT})		90%	92%	94%	
V_{OL_PG}	Power good output low voltage	I_{PG}= -2 mA				0.3	V
I_{LKG_PG}	Input leakage current (PG)				1	100	nA
POWER SWITCH							
$R_{DS(ON)}$	High-side MOSFET ON-resistance	V_{IN} = 7.5 V	Phase 1		27	65	mΩ
			Phase 2				
	Low-side MOSFET ON-resistance		Phase 1		21	45	mΩ
			Phase 2				
I_{LIM}	High-side MOSFET current limit	Each phase, V_{IN} = 7.5 V		4.0	4.7	5.5	A
T_{PSD}	Phase shift delay time	Phase 2 after Phase 1, PWM mode			250		ns
OUTPUT							
V_{REF}	Internal reference voltage			0.792	0.8	0.808	V
I_{LKG_FB}	Input leakage current (FB)	V_{FB} = 0.8 V			1	100	nA
$R_{DISCHARGE}$	Output discharge resistance	EN = Low			60		Ω
V_{OUT}	Output voltage range (TPS62180)	V_{IN} ≥ V_{OUT}		0.9		6	V
	Output voltage (TPS62182)				3.3		V
	Feedback voltage accuracy (TPS62180) (2)	PWM Mode, V_{IN} ≥ V_{OUT} + 1 V		–1%		1%	
		Power Save Mode, V_{OUT} = 3.3 V, I_{load} ≥ 1 mA, L = 1 µH, C_{OUT} = 2 x 47 µF, (T_J = –40°C to +85°C)		–1%		2%	
		Power Save Mode, V_{OUT} = 1.8 V, I_{load} ≥ 1 mA, L = 1 µH, C_{OUT} = 4 x 47 µF, (T_J = –40°C to +85°C)					
		Power Save Mode, V_{OUT} = 0.9 V, I_{load} ≥ 1 mA, L = 1 µH, C_{OUT} = 4 x 47 µF, (T_J = –40°C to +85°C)		–1%		3%	
	Output voltage accuracy (TPS62182) (2)	PWM Mode, V_{IN} ≥ V_{OUT} + 1 V		–1%		1%	
		Power Save Mode, I_{load} ≥ 1 mA, L = 1 µH, C_{OUT} = 2 x 47 µF, (T_J = –40°C to +85°C)		–1%		2%	
	Load regulation	V_{OUT} = 3.3 V, PWM Mode operation			0.04		%/A
	Line regulation	4 V ≤ V_{IN} ≤ 15 V, V_{OUT} = 3.3 V, I_{OUT} = 4 A			0.01		%/V
t_{HICCUP}	Hiccup on time				0.9		ms
	Hiccup off time				5		

(1) The minimum V_{IN} value of 4 V is not violated by UVLO threshold and hysteresis variations.
(2) The accuracy in Power Save Mode can be improved by increasing the output capacitor value, reducing the output voltage ripple.

7.6 Typical Characteristics

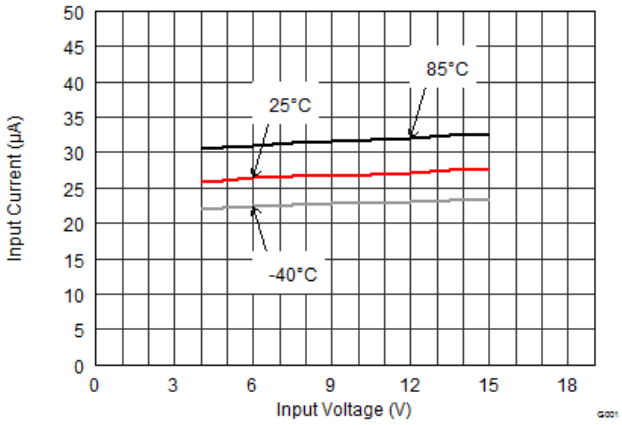


Figure 1. Quiescent Current

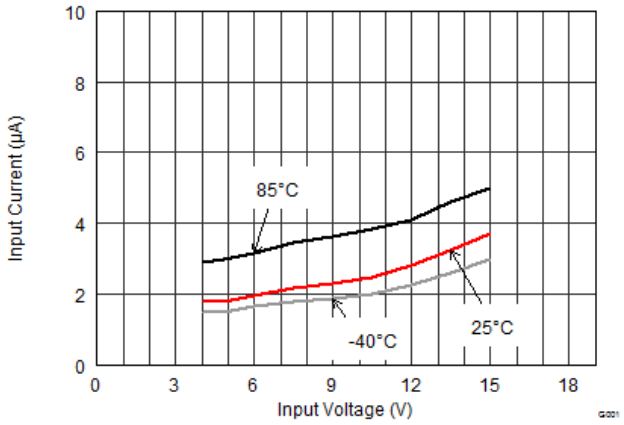


Figure 2. Shutdown Current

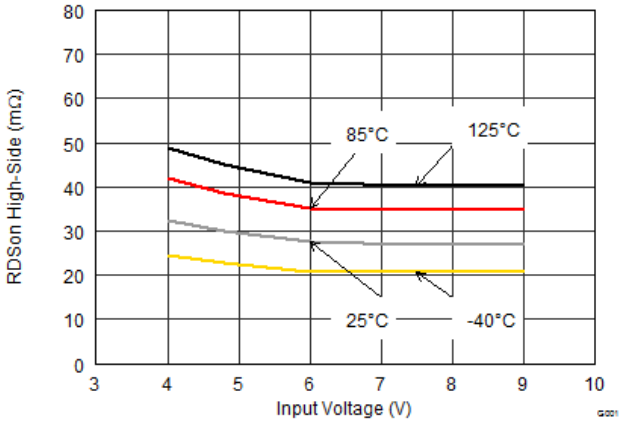


Figure 3. High-Side Switch Resistance

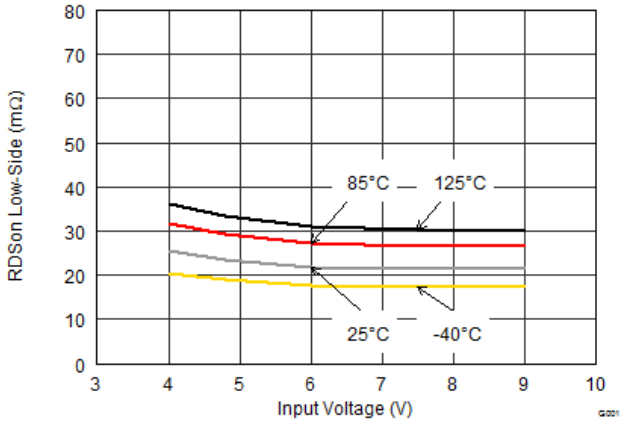


Figure 4. Low-Side Switch Resistance

8 Detailed Description

8.1 Overview

The TPS6218x is a high efficiency synchronous switched mode step-down converter based on a peak current control topology. It is designed for smallest solution size low-profile applications, converting multi-cell Li-Ion supply voltages to output voltages of 0.9 V to 6 V. While an outer voltage loop sets the regulation threshold for the current loop based on the actual V_{OUT} level, the inner current loop adapts the peak inductor current for every switching cycle. The regulation network is internally compensated. The switching frequency is set by an OFF-time control and features Power Save Mode (PSM) and AEE™ (Automatic Efficiency Enhancement) to keep the efficiency high over the whole load current and duty cycle range. The switching frequency is set depending on V_{IN} and V_{OUT} and remains unchanged for steady state operating conditions.

The TPS6218x is a dual phase converter, sharing the load current among the phases. Identical in construction, the follower control loop is connected with a fixed delay to the master control loop. Both the phases use the same regulation threshold and cycle-by-cycle peak current setpoint. This ensures a phase-shifted as well as current-balanced operation. Using the advantages of the dual phase topology, a 6-A continuous output current is provided with high performance and smallest system solution size.

While the TPS62180 offers an adjustable output voltage, the TPS62182 supports a fixed 3.3-V output voltage, saving external components.

8.2 Functional Block Diagram

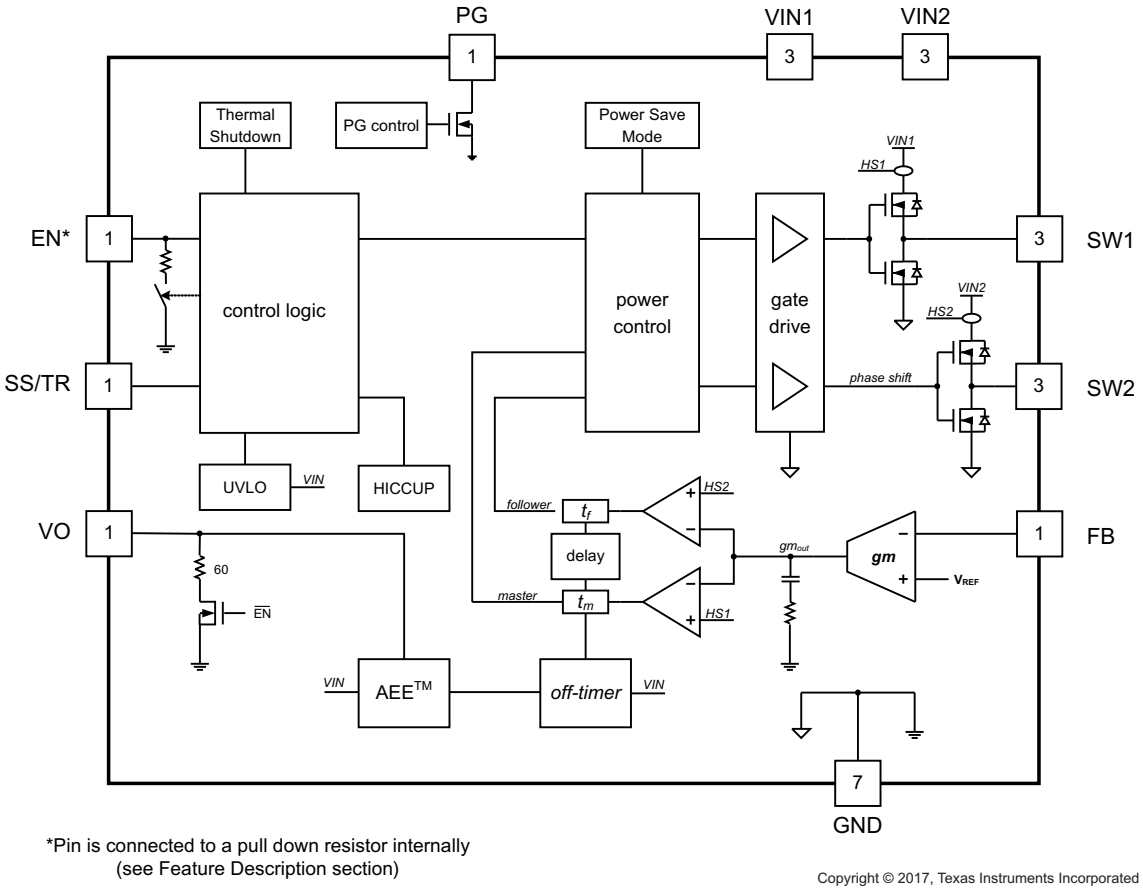


Figure 5. TPS62180 (Adjustable output voltage)

Functional Block Diagram (continued)

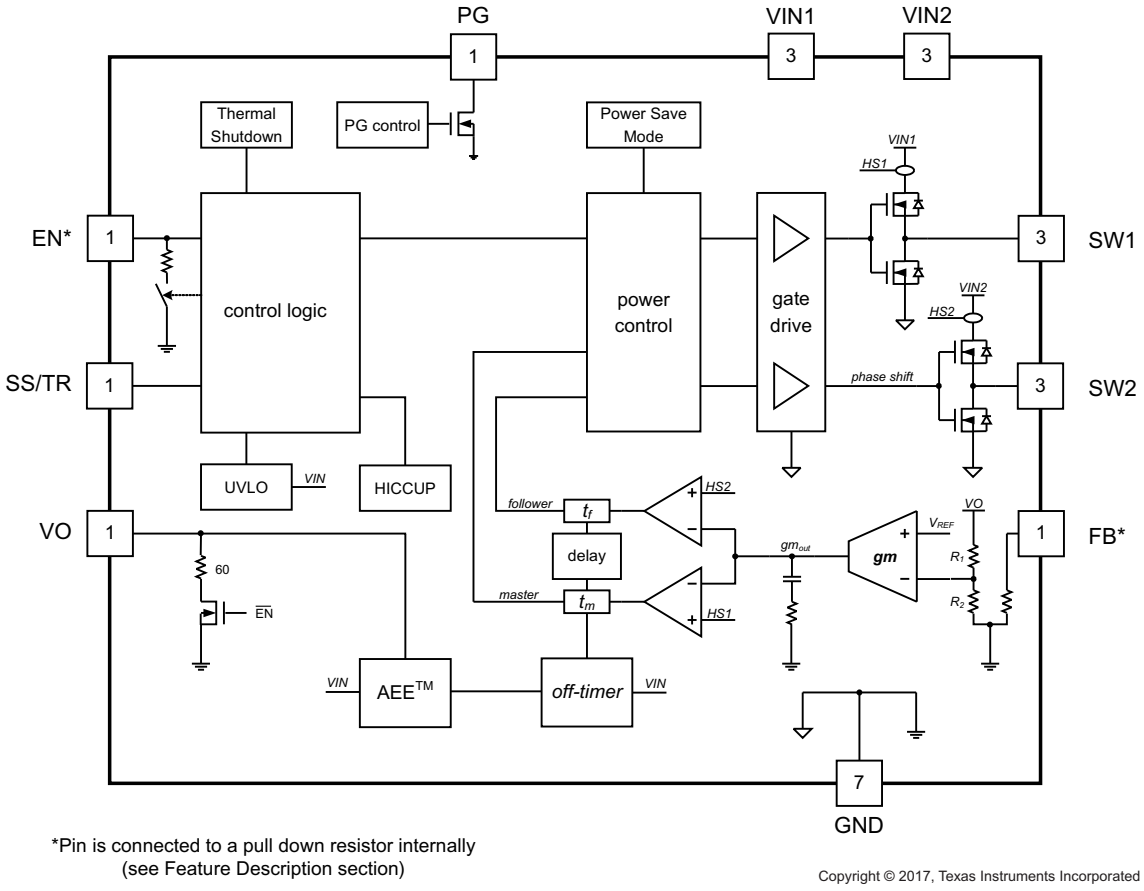


Figure 6. TPS62182 (Fixed output voltage)

8.3 Feature Description

8.3.1 Enable / Shutdown (EN)

The device starts operation, when V_{IN} is present and Enable (EN) is set High. The EN threshold is 1 V for rising and 0.9 V for falling voltages, providing a threshold accuracy of ±3%. That makes it suitable for precise switching on and off in accurate power sequencing arrangements as well as for slowly rising EN control voltage signals (see Using the Accurate EN Threshold for more details).

The device is disabled by pulling EN Low. A discharge resistor of about 60 Ω is then connected to the output. At the EN pin, an internal pull down resistor of about 350 kΩ keeps the Low state, if EN gets high impedance or floating afterwards.

The EN pin can be connected to V_{IN} to always enable the device. A delay of 1 ms, after V_{IN} exceeds V_{UVLO}, ensures safe operating conditions before the device starts switching. If V_{IN} is already present, a soft start sequence is initiated about 100 µs after EN is pulled High.

8.3.2 Soft Start / Tracking (SS/TR)

The soft start circuit controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drop from high impedance power sources or batteries. When EN is set to start device operation, the device starts switching and V_{OUT} rises with a slope, controlled by the external capacitor connected to the SS/TR pin. There is no theoretical limit for the longest startup time. It is not recommended to leave the SS/TR pin floating, because V_{OUT} may overshoot. Typical startup operation is shown in Application Performance Curves.

Feature Description (continued)

The device can track an external voltage (see Tracking). The device can monotonically start into a pre-biased output.

8.3.3 Power Good (PG)

The TPS6218x has a built in power good (PG) function. The PG pin goes High, when the output voltage has reached its nominal value. Otherwise, including when disabled, in UVLO or in thermal shutdown, PG is Low. The PG pin is an open drain output that requires a pull-up resistor and can sink typically 2 mA. If not used, the PG pin can be left floating or grounded.

Table 1. Power Good Pin Logic Table

Device Information		PG Logic Status	
		High Z	Low
Enable (EN=High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown (EN=Low)			√
UVLO	$0.7V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7V$	√	

8.3.4 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) prevents misoperation of the device, if the input voltage drops below the UVLO threshold. It is set to 3.6 V typically with a hysteresis of typically 300mV. (See also Device Functional Modes).

8.3.5 Thermal Shutdown

The junction temperature T_J of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typ.), the device goes in thermal shutdown with a hysteresis of typically 20°C. Both the power FETs are turned off, the discharge resistor is connected to the output and the PG pin goes Low. Once T_J has decreased enough, the device resumes normal operation with Soft Start.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

The TPS6218x is based on a predictive OFF-time peak current control topology, operating with PWM in continuous conduction mode for heavier loads. Since the OFF-time is automatically adjusted according to the actual V_{IN} and V_{OUT}, it provides highest efficiency over the entire input and output voltage range. The OFF-time is calculated as:

$$t_{OFF} = \left[\frac{V_{IN}}{5V_{OUT}} 500ns \right] + 50ns \quad (1)$$

While the OFF-time is predicted, the ON-time is set depending on the converter's duty cycle and calculated as:

$$t_{ON} = \frac{t_{OFF} \cdot V_{OUT}}{V_{IN} - V_{OUT}} \quad (2)$$

Device Functional Modes (continued)

Thereby the switching frequency is fixed for a given input and output voltage and is calculated as:

$$f_{SW} = \frac{1-D}{t_{OFF}} = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Both the master and follower phases regulate to the same level of V_{OUT} with separate current loops, using the same peak current setpoint, cycle by cycle. This provides excellent peak current balancing, independent of inductor dc resistance matching. Since the follower phase operates with a fixed delay to the master phase, also cycle by cycle, phase shifted operation is obtained.

The device features an automatic transition into Power Save Mode, entered at light loads, running in discontinuous conduction mode (DCM).

8.4.2 Power Save Mode (PSM) Operation

As the load current decreases, the converter enters Power Save Mode operation. During PSM, the converter operates with a reduced switching frequency maintaining highest efficiency due to minimum quiescent current. Power Save Mode is based on a fixed peak current architecture, where the peak current (I_{PEAK}) is set depending on V_{IN}, V_{OUT}, and L. After each single pulse, a pause time until the internal V_{OUT_Low} level threshold is reached completes the switching cycle in PSM.

The switching frequency for PSM in one phase operation is calculated as :

$$f_{PSM} = \frac{2I_{OUT} \cdot V_{OUT}\left(V_{IN} - V_{OUT}\right)}{L \cdot I_{PEAK}^2 \cdot V_{IN}} \quad (4)$$

Equation 4 shows the linear relationship of output current and switching frequency. Typical values of the fixed peak current are shown in Figure 7.

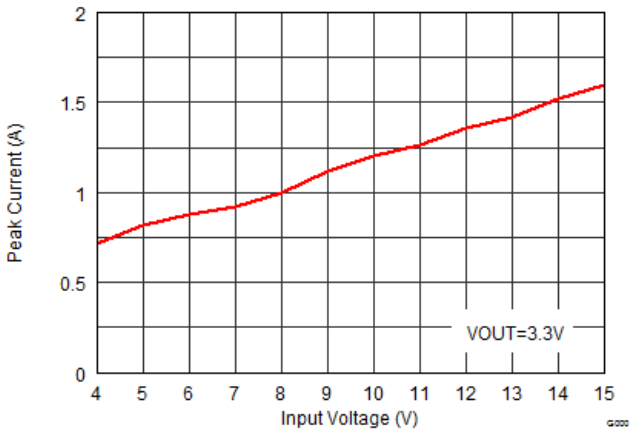


Figure 7. Typical Fixed Peak Current (I_{PEAK}) in Power Save Mode

If the load decreases to very light loads and only one phase is needed, either phase (master or follower) might be active. The load current level at which Power Save Mode is entered is calculated as follows:

Device Functional Modes (continued)

$$I_{load(PSM)} = \Delta I_L \quad (5)$$

Equation 7 is used to calculate ΔI_L.

8.4.3 Minimum Duty Cycle and 100% Mode Operation

When the input voltage comes close to the output voltage, the device enters 100% mode and both high-side FETs are continuously switched on as long as V_{OUT} remains below its setpoint. The minimum V_{IN} to maintain output voltage regulation is calculated as:

$$V_{IN(\min)} = V_{OUT(\min)} + I_{OUT}\left[\frac{R_{DS(ON)}}{2} + DCR_{L1} // DCR_{L2}\right] \quad (6)$$

This allows the conversion of small input to output voltage differences, for example for the longest operation time in battery powered applications. In 100% duty cycle mode, the low-side FET is switched off.

While the maximum ON-time is not limited, the AEE feature, explained in the next section, secures a minimum ON-time of about 100 ns.

8.4.4 Automatic Efficiency Enhancement (AEE™)

AEE™ provides highest efficiency over the entire input voltage and output voltage range by automatically adjusting the converter's switching frequency. This is achieved by setting the predictive off-time of the converter.

The efficiency of a switched mode converter is determined by the power losses during the conversion. The efficiency decreases, if V_{OUT} decreases and/or V_{IN} increases. In order to keep the efficiency high over the entire duty cycle range (V_{OUT}/V_{IN} ratio), the switching frequency is adjusted while maintaining the ripple current. The following equation shows the relation between the inductor ripple current, switching frequency and duty cycle.

$$\Delta I_L = V_{OUT} \cdot \left(\frac{1-D}{L \cdot f_{SW}}\right) = V_{OUT} \cdot \left(\frac{1-\frac{V_{OUT}}{V_{IN}}}{L \cdot f_{SW}}\right) \quad (7)$$

Efficiency increases by decreasing switching losses, preserving high efficiency for varying duty cycles, while the ripple current amplitude remains low enough to deliver the full output current without reaching current limit. The AEE™ feature provides an efficiency enhancement for various duty cycles, especially for lower Vout values, where fixed frequency converters suffer from a significant efficiency drop. Furthermore, this feature compensates for the very small duty cycles of high V_{IN} to low V_{OUT} conversion, which limits the control range in other topologies.

Figure 8 shows the typical switching frequency over the input voltage range.

Device Functional Modes (continued)

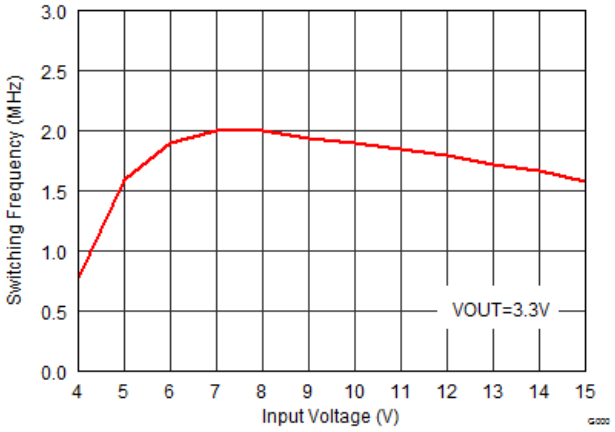


Figure 8. Typical Switching Frequency vs Input Voltage

8.4.5 Phase-Shifted Operation

While, for a buck converter, the input current source provides the average current that is needed to support the output current, an input capacitance is needed to support pulse currents. One of the natural benefits of a two- (or multi-) phase converter is the possibility to operate out of phase, which decreases the pulse currents and switching noise. In PWM mode, the TPS6218x devices run with a fixed delay of typically 250 ns between the phases. This ensures that the phases run phase-delayed, limiting input RMS current and corresponding noise. If in PSM, both phases run, the phase delay is about 100 ns.

8.4.6 Current Limit, Current Balancing, and Short Circuit Protection

Each phase has a separate integrated peak current limit. While its minimum value limits the output current of the phase, the maximum number gives the current that must be considered to flow in any operating case. If the current limit of a phase is reached, the peak current setpoint is unable to increase further. The device provides its maximum output current. Detecting this heavy load or short circuit condition for about 0.9 ms, the device switches off for about 5 ms and then restarts again with a soft start cycle. As long as the overload condition is present, the device hiccups that way, limiting the output power.

The two phases are peak current balanced with a variation within about ±10% at 6-A output current (see Figure 9). Since the control topology does not depend on inductor or output current measurements, the current balancing accuracy is independent of inductor matching (binning) and does not need matched power routing.

Device Functional Modes (continued)

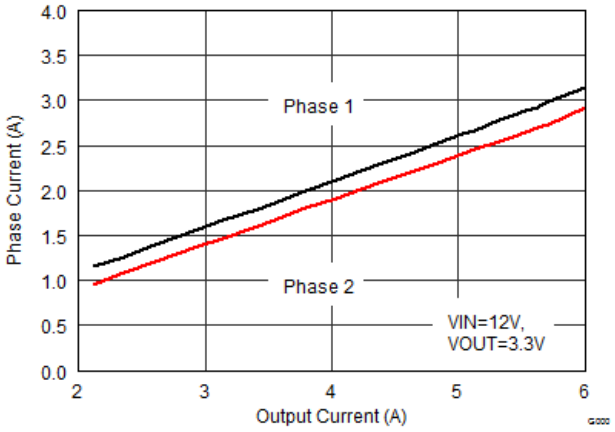


Figure 9. Typical Current Balancing vs Load Current

8.4.7 Tracking

V_{OUT} can track a voltage that is applied at the SS/TR pin. The tracking range at the SS/TR pin is 50 mV to 1.2 V and the FB pin voltage tracks this as given in Equation 8:

$$V_{FB} \approx 0.64 \cdot V_{SS/TR} \tag{8}$$

Due to the factor of about 0.64, the minimum output voltage for tracking is 1.25 V. Once the SS/TR pin voltage reaches about 1.2 V, the internal voltage is clamped to the internal feedback voltage and the device goes to normal regulation. This works for falling tracking voltage as well. If, in this case, the SS/TR voltage decreases, the device does not sink current from the output. Thus, the resulting decrease of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is V_{IN}+0.3 V.

Note: If the voltage at the FB pin is below its typical value of 0.8 V, the output voltage accuracy may have a wider tolerance than specified.

8.4.8 Operation with Fixed V_{OUT}

The TPS62182 provides a fixed output voltage of 3.3 V (±1%). In this case, the feedback divider is integrated and the FB pin is internally connected to GND with a resistor of about 350 kΩ. It is recommended to connect the FB pin to PCB ground to improve thermal behavior.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS62180/2 are switched mode step-down converters, able to convert a 4-V to 15-V input voltage into a lower 0.9-V to 6-V output voltage, providing up to 6 A. It needs a minimum amount of external components. Apart from the LC output filter and the input capacitors only an optional pull-up resistor for Power Good (PG) and a small capacitor for adjustable soft start are used. The TPS62180 with an adjustable output voltage needs an additional resistive divider to set the output voltage level.

9.2 Typical Applications

9.2.1 Typical TPS62180 Application

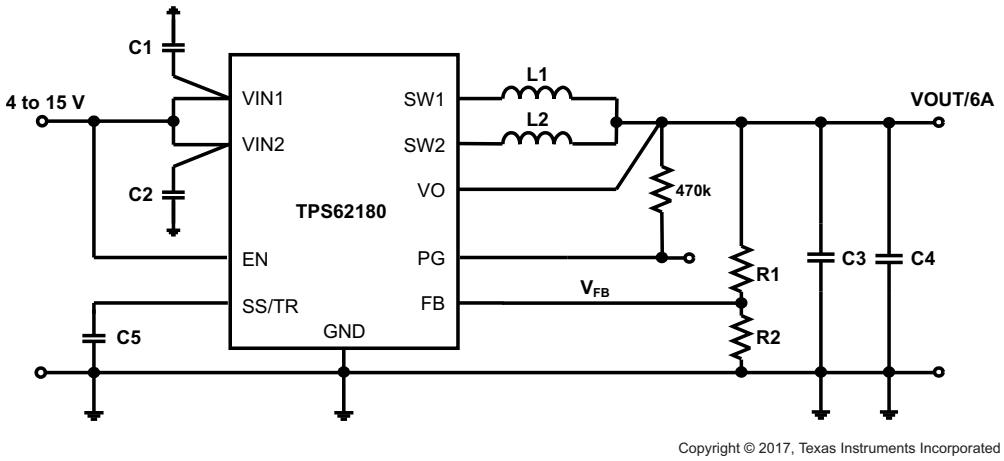


Figure 10. Typical 4-V to 15-V Input, 6A Converter

9.2.1.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions. The component selection is given in Table 2 and gives a total solution size of about 99 mm^2 with a maximum height of 2.1 mm:

Table 2. Components Used for Application Characteristics

REFERENCE NAME	DESCRIPTION / VALUE	MANUFACTURER
TPS62180YZF	2 phase step down converter, 2 x 3 mm WCSP	Texas Instruments
L1, L2	Inductor XFL4020-102ME, 1 µH ±20%, 4 x 4 x 2.1 mm	Coilcraft
C1, C2	Ceramic capacitor GRM21BR61E226ME44, 2 x 22 µF, 25 V, X5R, 0805	muRata
C3, C4	Ceramic capacitor GRM21BR60J476ME15, 2 x 47 µF, 6.3 V, X5R, 0805	muRata
C5	Ceramic capacitor, 3.3 nF	Standard
R1	Chip resistor, value depending on V_{OUT}	Standard
R2	Chip resistor, value depending on V_{OUT}	Standard
R3	Chip resistor, 470 kΩ, 0603, 1/16 W, 1%	Standard

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62180 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.1.2.2 Programming the Output Voltage

The output voltage of the TPS62180 is programmed using an external resistive divider. While the voltage at the FB pin is regulated to 0.8 V, the output voltage range is specified from 0.9 up to 6 V. The value of the output voltage is set by selection of the resistive divider (from VOUT to FB to AGND) from Equation 9.

$$\frac{R_1}{R_2} = \frac{V_{OUT}}{V_{FB}} - 1 \tag{9}$$

The current through those resistors contributes to the light load efficiency, which makes larger resistor values beneficial. However, to get sufficient noise immunity these values should not be oversized. Using this, the resistor values are calculated by converting Equation 9 as follows:

$$R_2 = \frac{V_{FB}}{I_{FB}} = \frac{0.8V}{5\mu A} = 160k\Omega \tag{10}$$

Inserting the R_2 value in Equation 11, R_1 can be obtained.

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \tag{11}$$

Calculating for V_{OUT} = 3.3 V gives R_1 = 500 kΩ. Using standard resistor values R_1 = 470 kΩ and R_2 = 150 kΩ are chosen.

For applications requiring lowest current consumption, the use of fixed output voltage options is recommended. Using the TPS62182, the FB pin can be left floating, but it is recommended to connect it to AGND which decreases thermal resistance.

In case the FB pin of the adjustable output voltage version gets opened or an over voltage appears at the output, an internal clamp limits the output voltage to about 7.4 V.

9.2.1.2.3 Output Filter Selection

Since the TPS6218x is compensated internally, it is optimized for a range of external component values, which is specified below. Table 3 and Table 4 are used to simplify the output filter component selection. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

Table 3. Recommended LC Output Filter Combinations for V_{OUT} ≥ 1.8 V(1)

	2 x 47 µF	4 x 47 µF	6 x 47 µF	8 x 47 µF
0.47 µH				
1.0 µH	√	√	√	√
1.5 µH				

(1) The values in the table are the nominal values of inductors and ceramic capacitors. The effective capacitance can vary by +20 and –60%.

Table 4. Recommended LC Output Filter Combinations for V_{OUT} < 1.8 V(1)

	2 x 47 µF	4 x 47 µF	6 x 47 µF	8 x 47 µF
0.68 µH				
1.0 µH		√	√	
1.5 µH				

(1) The values in the table are nominal values of inductors and ceramic capacitors. The effective capacitance can vary by +20 and –40%.

For the output capacitors, a voltage rating of 6.3 V and an X5R dielectric are chosen. If space allows for higher voltage rated capacitors in larger case sizes, the dc bias effect is lowered and the effective capacitance value increases.

9.2.1.2.4 Inductor Selection

The TPS6218x is designed to work with two inductors of 1 µH nominal. They have to be selected for adequate saturation current and a low dc resistance (DCR). The minimum inductor current rating $I_{L(min)}$ that is needed under static load conditions is calculated using Equation 12 and Equation 13. A current imbalance of 10% at most is incorporated.

$$I_{peak(\max)} = I_{L(\min)} = \frac{1.1 \cdot I_{OUT(\max)}}{2} + \frac{\Delta I_{L(\max)}}{2} \tag{12}$$

$$\Delta I_{L(\max)} = V_{OUT} \cdot \left(\frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}} \right) \tag{13}$$

This calculation gives the minimum saturation current of the inductor needed and an additional margin of about 20% is recommended to cover dynamic overshoot due to load transients. For low profile solutions, the physical inductor size and the power losses have to be traded off. Smallest solution size (for example with chip inductors) are less efficient than bigger inductors with lower losses due to lower DCR and/or core losses. The following inductors have been tested with the TPS6218x:

Table 5. List of Inductors

TYPE	INDUCTANCE [µH]	CURRENT RATING MIN/TYP [A] (1)	DCR MAX [mΩ]	DIMENSIONS (LxBxH) [mm]	MANUFACTURER
DFE201612E-1R0M	1 ±20%	4.0/4.4	48	2.0 x 1.6 x 1.2	TOKO
DFE252012F-1R0M	1 ±20%	4.7/5.3	40	2.5 x 2.0 x 1.2	TOKO
DFE252012P-1R0M	1 ±20%	3.8/4.5	42	2.5 x 2.0 x 1.2	TOKO
PIFE32251B-1R0MS	1 ±20%	4.2/4.7	42	3.2 x 2.5 x 1.2	CYNTEC
PIME031B-1R0MS	1 ±20%	4.5/5.4	55	3.7 x 3.3 x 1.2	CYNTEC
PISB25201T-1R0MS	1 ±20%	3.6/3.9	62	2.5 x 2.0 x 1.0	CYNTEC
IHLP1212AB-11	1 ±20%	/5.0	37.5	3.6 x 3.0 x 1.2	VISHAY
IHLP1212AE-11	1 ±20%	/5.3	33	3.6 x 3.0 x 1.5	VISHAY
XFL4015-122ME_	1.2±20%	/4.5	20.7	4.0 x 4.0 x 1.5	COILCRAFT
XFL4020-102ME_	1 ±20%	/5.4	11.9	4.0 x 4.0 x 2.1	COILCRAFT
TFM201610-GHM	1 ±20%	3.6/3.8	60	2.0 x 1.6 x 1.0	TDK
TFM252010-GHM	1 ±20%	3.5/4.0	56	2.5 x 2.0 x 1.0	TDK

(1) I_{SAT} at 30% drop of inductance ($\Delta I_L/I_L$).

The TPS6218x is not designed to operate with only one inductor.

9.2.1.2.5 Output Capacitor Selection

The TPS6218x provides a wide output voltage range of 0.9 V to 6 V. While stability is a critical criteria for the output filter selection, the output capacitor value also determines transient response behavior, ripple and accuracy of V_{OUT}. Table 6 gives recommendations to achieve various transient design targets using 1-µH inductors and small sized output capacitors (see Table 2).

Table 6. Recommended Output Capacitor Values

OUTPUT VOLTAGE [V]	LOAD STEP [A]	(NOMINAL) CAPACITOR VALUE(1)	TYPICAL TRANSIENT RESPONSE ACCURACY	
			±mV	±%
0.9(2)	2-6-2(3)	4 x 47 µF	90	10
		6 x 47 µF	70	8
1.8	2-6-2(3)	2 x 47 µF	150	8
		4 x 47 µF	120	7
		8 x 47 µF	90	5
3.3	2-6-2(3)	2 x 47 µF	170	5
		4 x 47 µF	135	4
		8 x 47 µF	100	3

(1) Ceramic capacitors have a dc bias effect where the effective capacitance differs significantly from the nominal value, depending on package size, voltage rating and dielectric material.
(2) For output voltages < 1.8V an additional feedforward capacitor of 82pF, parallel to R_1 is recommended to increase stability margin at heavy load steps.
(3) The transient load step is tested with 1-µs/step rising/falling slopes.

The architecture of the TPS6218x allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectrics. Using even higher values than demanded for stability and transient response has further advantages like smaller voltage ripple and tighter dc output accuracy in Power Save Mode.

9.2.1.2.6 Input Capacitor Selection

The input current of a buck converter is pulsating. Therefore, a low ESR input capacitor is required to prevent large voltage transients and provide peak currents. The recommended value for most applications is 2 x 22 µF, split between the VIN1 and VIN2 inputs and placed as close as possible to these pins and PGND pins. If additional capacitance is needed, it can be added as bulk capacitance. To ensure proper operation, the effective capacitance at the VIN pins must not fall below 2 x 2 µF (close) + 10 µF bulk (effective capacitances).

Low ESR multilayer ceramic capacitors are recommended for best filtering. Increasing with input voltage, the dc bias effect reduces the nominal capacitance value significantly. To decrease input ripple current further, larger values of input capacitors can be used.

9.2.1.2.7 Soft Start Capacitor Selection

The TPS6218x provides a user programmable soft start time. A constant current source of 5 µA, internally connected to the SS/TR pin, allows control of the startup slope by connecting a capacitor to this pin. The current source charges the capacitor and the soft start time is given by:

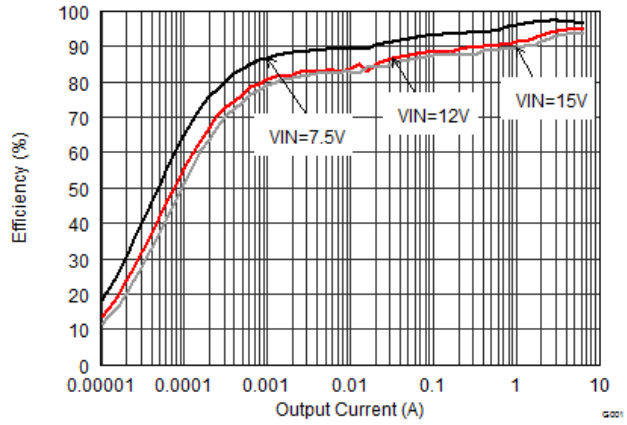
$$C_{SS} = t_{SS} \cdot \frac{5\mu A}{1.25V} \tag{14}$$

where C_{SS} is the soft-start capacitance required at the SS/TR pin and t_{ss} is the resulting soft-start ramp time.

The SS/TR pin should not be left floating and a minimum capacitance of 220 pF is recommended. Using Equation 14, and inserting t_{SS} = 750 µs, a value of 3 nF is calculated. 3.3 nF is chosen as a standard value for this example.

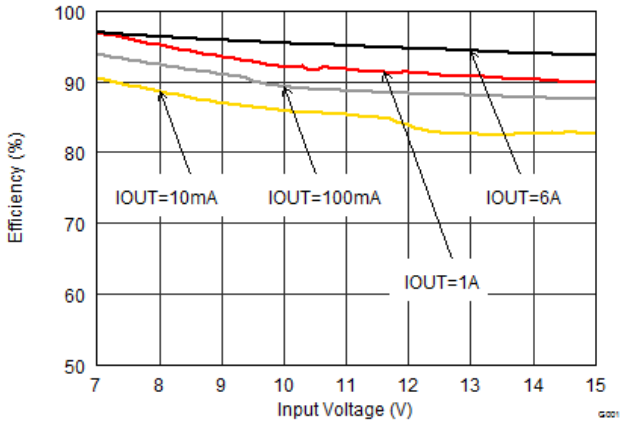
9.2.1.3 Application Performance Curves

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)



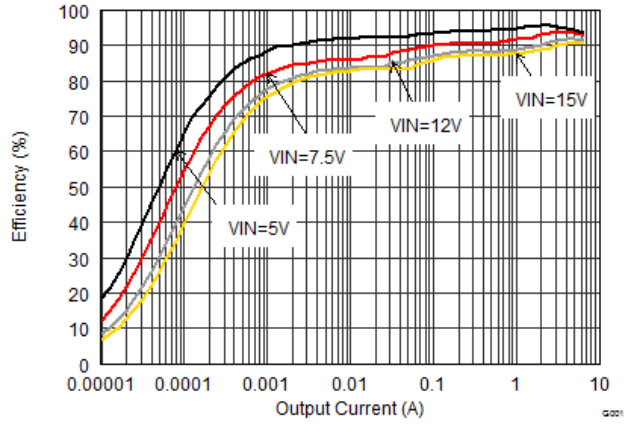
V_{OUT} = 6 V

Figure 11. Efficiency vs Load Current



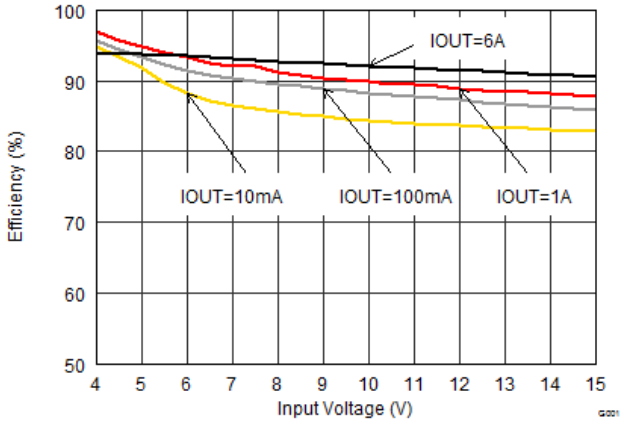
V_{OUT} = 6 V

Figure 12. Efficiency vs Input Voltage



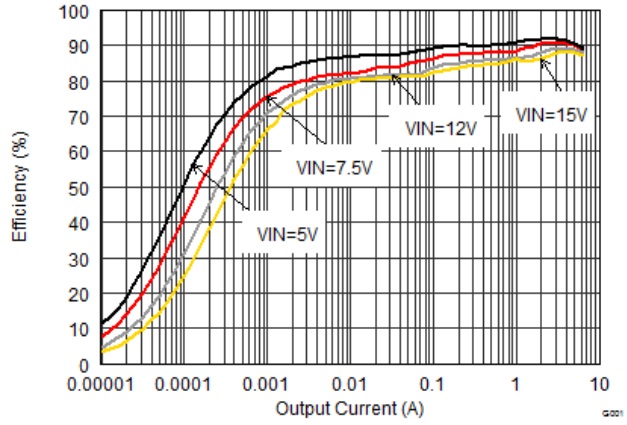
V_{OUT} = 3.3 V

Figure 13. Efficiency vs Load Current



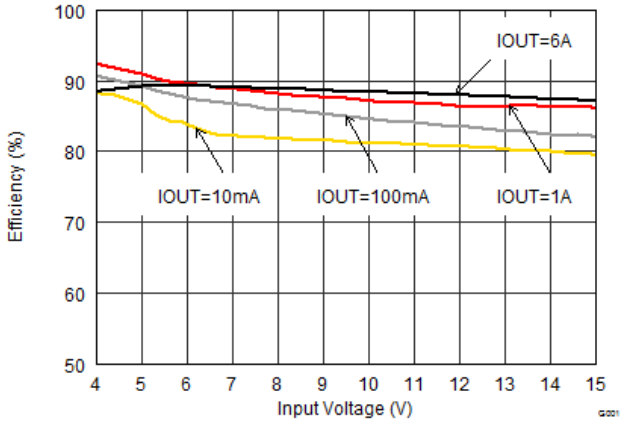
V_{OUT} = 3.3 V

Figure 14. Efficiency vs Input Voltage



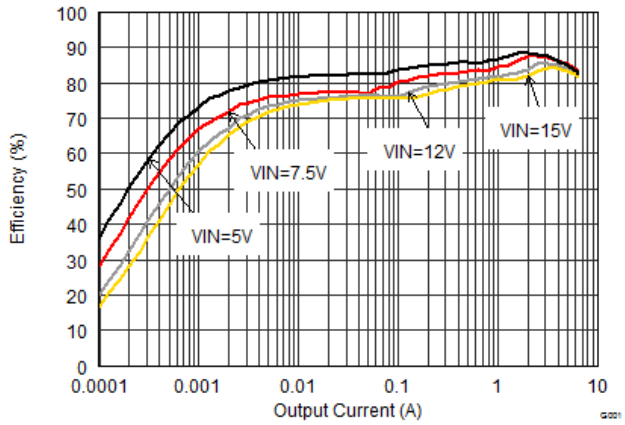
V_{OUT} = 1.8 V

Figure 15. Efficiency vs Load Current



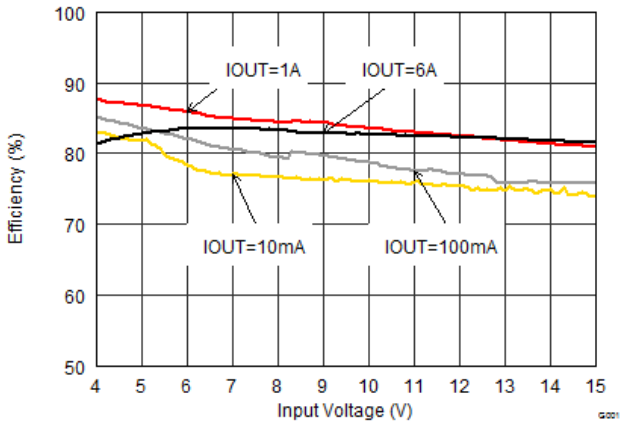
V_{OUT} = 1.8 V

Figure 16. Efficiency vs Input Voltage



V_{OUT} = 0.9 V

Figure 17. Efficiency vs Load Current



V_{OUT} = 0.9 V

Figure 18. Efficiency vs Input Voltage

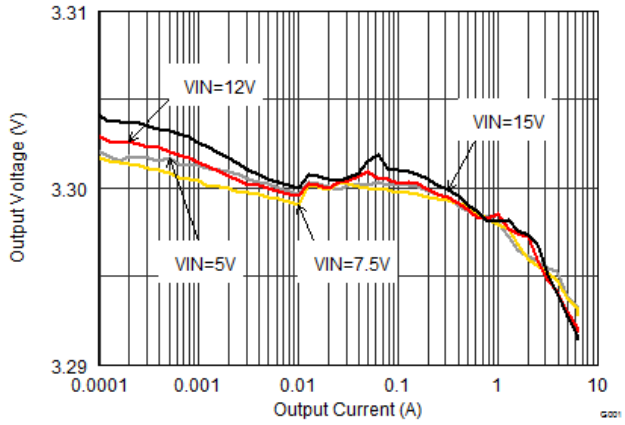


Figure 19. Output Voltage vs Output Current (Load regulation)

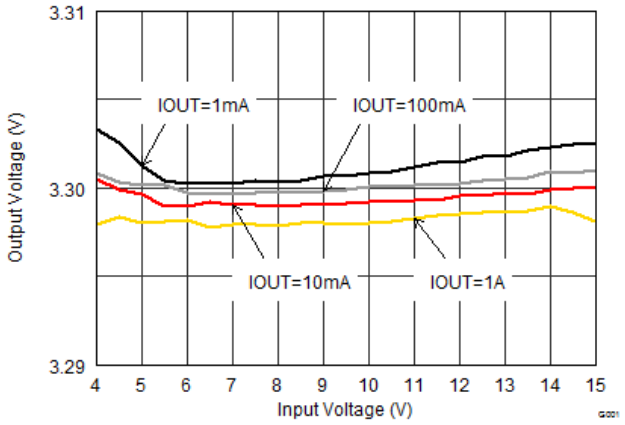


Figure 20. Output Voltage vs Input Voltage (Line regulation)

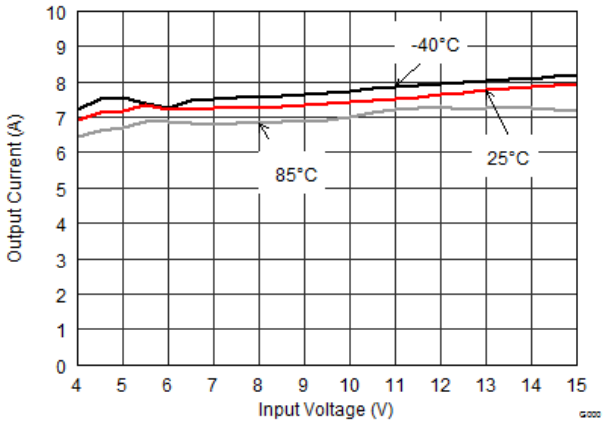


Figure 21. Maximum Output Current vs Input Voltage

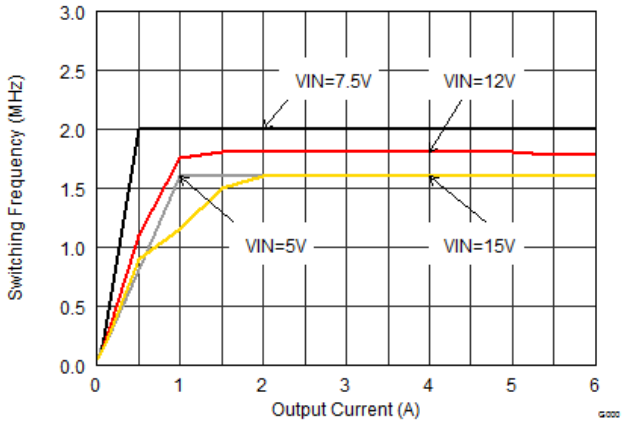


Figure 22. Switching Frequency vs Output Current

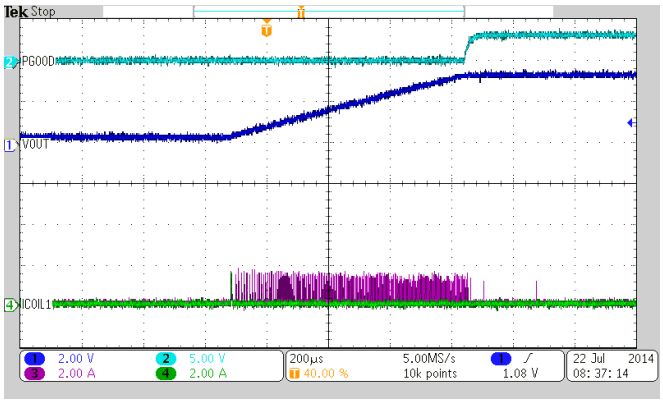


Figure 23. Startup into 33 Ω (100 mA)

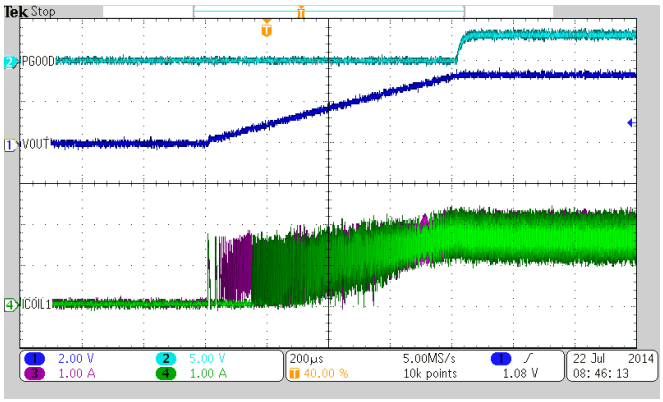


Figure 24. Startup into 1 Ω (3.3 A)

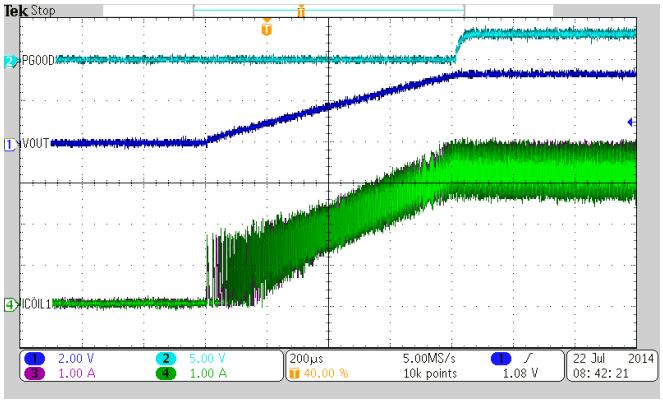


Figure 25. Startup into 0.5 Ω (6.6 A)

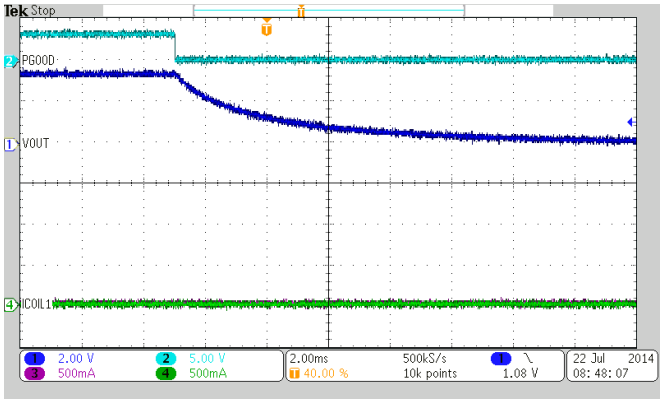
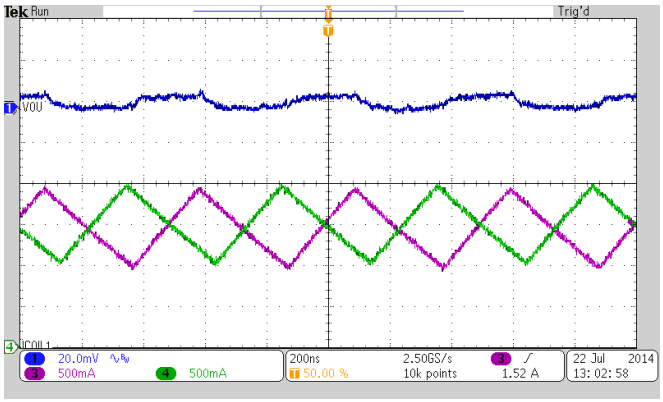
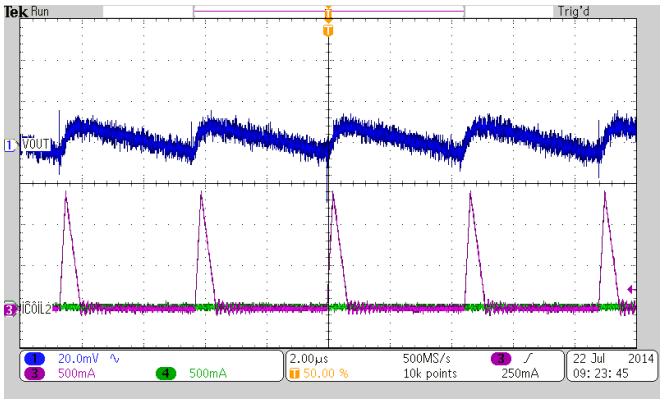


Figure 26. Output Discharge (No load)



I_{OUT} = 3 A

Figure 27. Typical Operation (PWM)



I_{OUT} = 100 mA

Figure 28. Typical Operation (PSM)

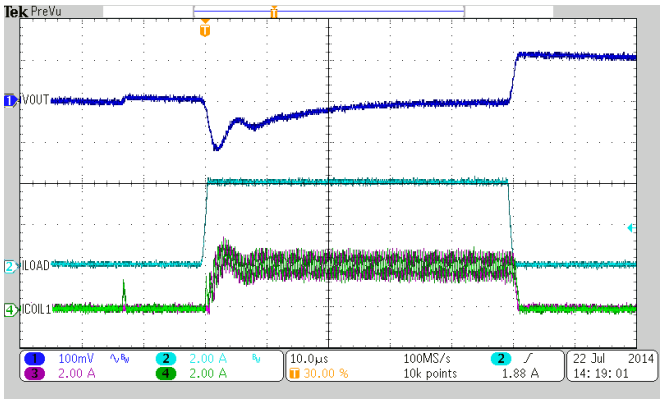


Figure 29. Load Transient Response (PSM-PWM)

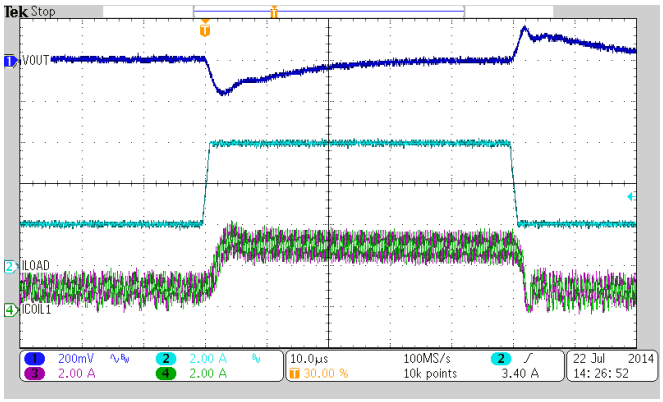
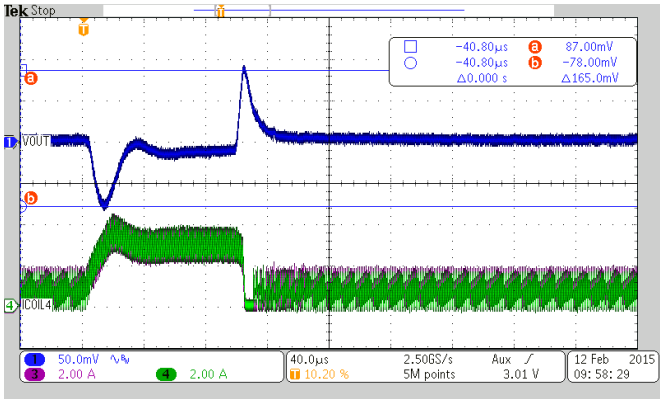
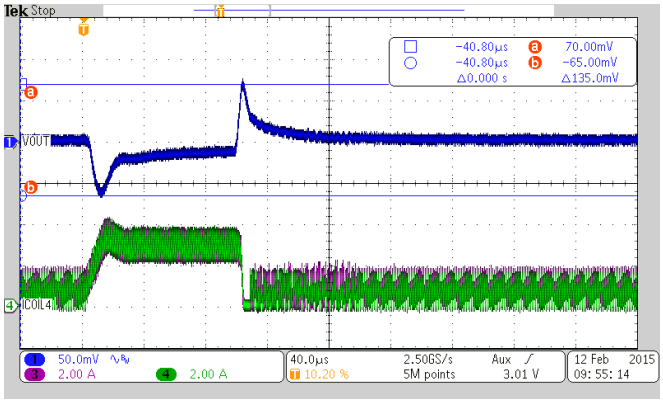


Figure 30. Load Transient Response (PWM-PWM)



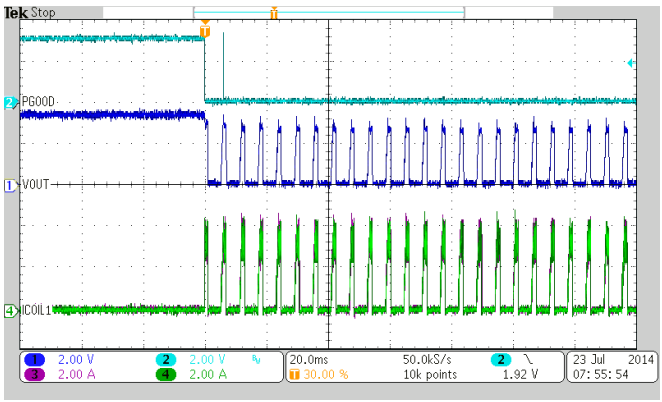
V_{OUT} = 1.8 V C_{OUT} = 6x47 µF

Figure 31. Transient Response to a load step of 1-6A (1A/µs)



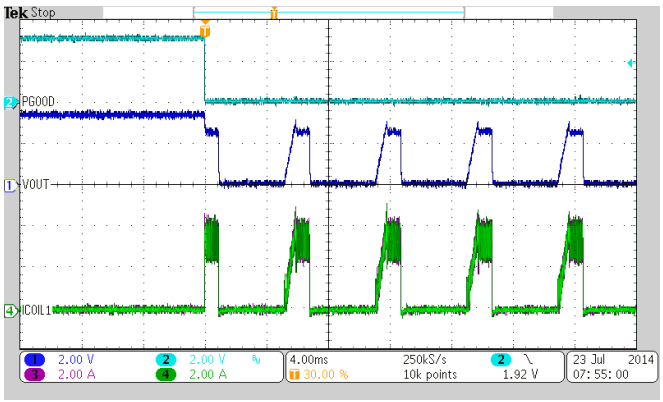
V_{OUT} = 1.8 V C_{OUT} = 6x47 µF additional C_{FF} = 82 pF

Figure 32. Transient Response to a load step of 1-6A (1A/µs)



R_{LOAD} = 0.33 Ω

Figure 33. HICCUP at Overload Condition



R_{LOAD} = 0.33 Ω

Figure 34. HICCUP at Overload Condition

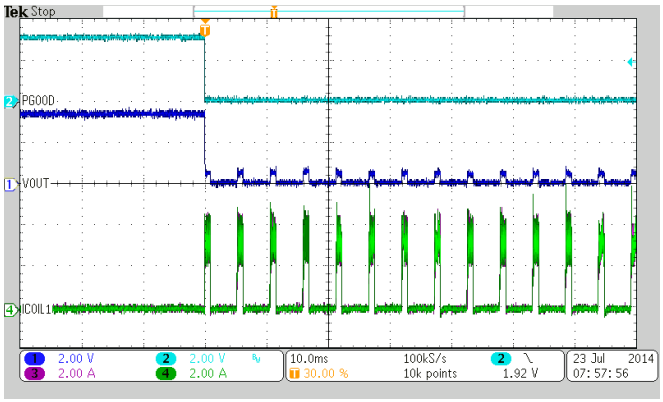


Figure 35. HICCUP at Short Circuit

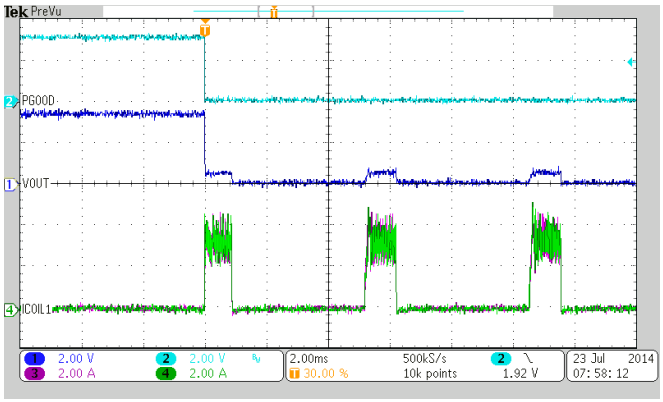


Figure 36. HICCUP at Short Circuit

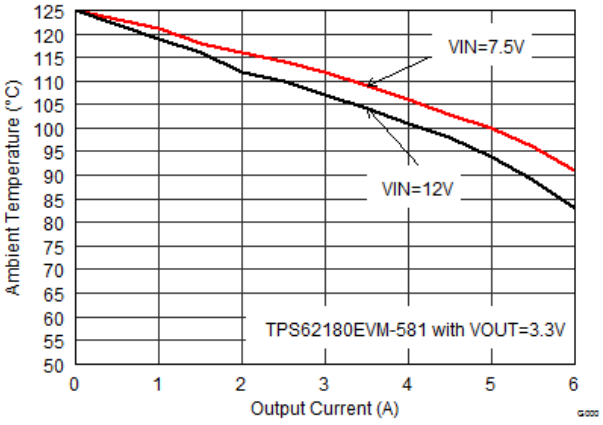


Figure 37. Maximum Ambient Temperature

9.2.2 TPS62180 Low Profile Solution

This design example is based on Figure 10 again, providing a very small (see Figure 38) and low profile solution, using low profile inductors.

9.2.2.1 Design Requirements

The input parameters used for this design are given in Table 7 and give a total solution size of about 72mm^2, using inductors with a maximum height of 1.2 mm:

Table 7. Components Used for Application Characteristics

REFERENCE NAME	DESCRIPTION / VALUE	MANUFACTURER
TPS62180YZF	2 phase step down converter, 2 x 3 mm WCSP	Texas Instruments
L1, L2	Inductor DFE252012P, 1 µH ±20%, 2.5 x 2 x 1.2 mm	Toko
C_{IN}	Ceramic capacitor GRM21BR61E226ME44, 2 x 22 µF, 25 V, X5R, 0805	muRata
C_{OUT}	Ceramic capacitor GRM21BR60J476ME15, 2 x 47 µF, 6.3 V, X5R, 0805	muRata
C_{SS}	Ceramic capacitor, 10 nF	Standard
R1	Chip resistor, value depending on V_{OUT}	Standard
R2	Chip resistor, value depending on V_{OUT}	Standard
R3	Chip resistor, 470 kΩ, 0603, 1/16 W, 1%	Standard

9.2.2.2 Detailed Design Procedure

As opposed to the previous example, the solution size, including height, is limited and the soft start time is longer. This is achieved by using smaller inductors, as well as using a different soft start capacitor.

9.2.2.2.1 Inductor

Using Table 5, the 1-µH DFE252012P is chosen with dimensions of 2.5 x 2.0 x 1.2 mm. The larger DCR of 42 mΩ maximum causes some efficiency drop (see comparison below).

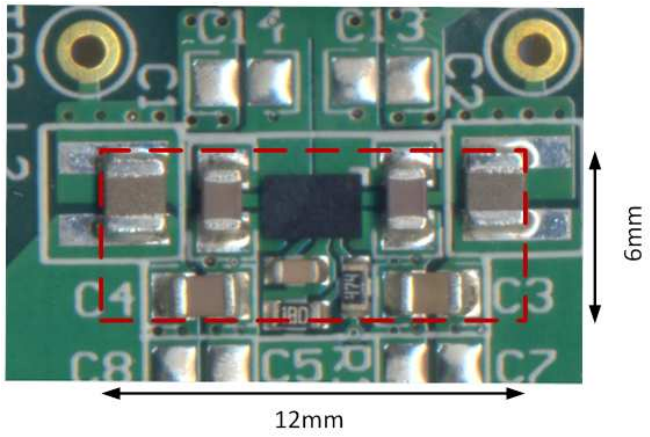


Figure 38. Ultra Small Solution Size

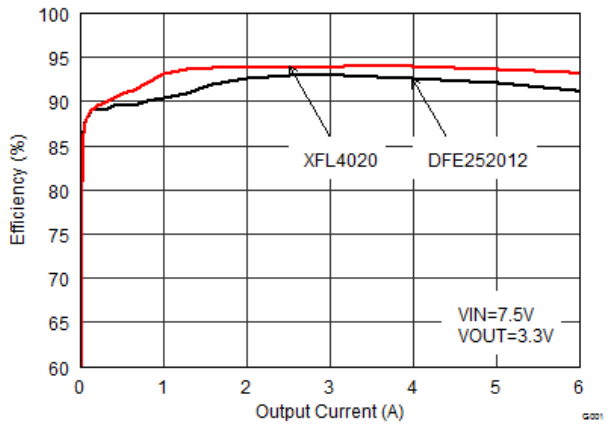


Figure 39. Efficiency vs Inductor Size/Type

9.2.2.2.2 Input and Output Capacitors

Since electrical design parameters are unchanged, the same values as chosen in the previous example are used for these capacitors.

9.2.2.2.3 Soft Start Capacitor

Using Equation 14 again, and inserting t_{SS} = 2.5 ms gives a capacitance of 10 nF, which is chosen.

9.2.2.2.4 Using the Accurate EN Threshold

The TPS6218x provides a very accurate EN threshold voltage. This can be used to switch on the device according to a V_{IN} or another voltage level by using a resistive divider as shown below.

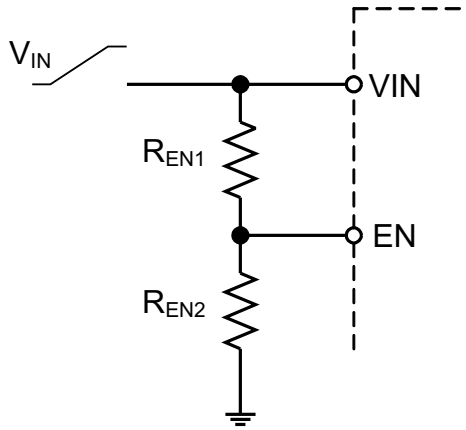


Figure 40. Resistive Divider for Controlled EN Threshold

The values of R_{EN1} and R_{EN2}, needed to set EN = High at a specific V_{IN} can be calculated according to Kirchhoff's laws, shown in Equation 15 and used in the following example:

$$V_{IN} = V_{EN\_threshold} \cdot \frac{R_{EN1} + R_{EN2}}{R_{EN2}} \quad (15)$$

For a typical 8-V input rail, the device turn on target value is set to 5.5 V. The current through the resistive divider is set to 10 µA, which indicates a total resistance of about 800 kΩ. Appropriate standard resistor values, fitting Equation 15, are R_{EN1} = 680 kΩ and R_{EN2} = 150 kΩ. As a result, the device switches on, when V_{IN} has reached 5.5 V and the current through the divider is 9.6 µA. The device switches off at a threshold of 0.9 V. Using Equation 15 again, this case gives a level of V_{IN} = 5.0 V.

Figure 47 to Figure 50 show thresholds and appropriate device behavior with a startup time of about 800 µs.

9.2.2.3 Application Performance Curves

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)

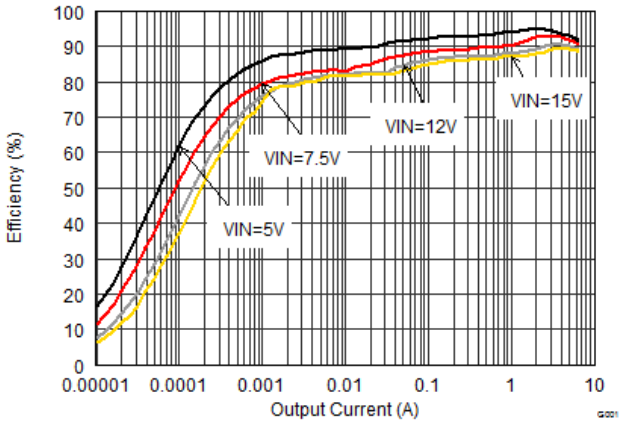


Figure 41. Efficiency vs Load Current

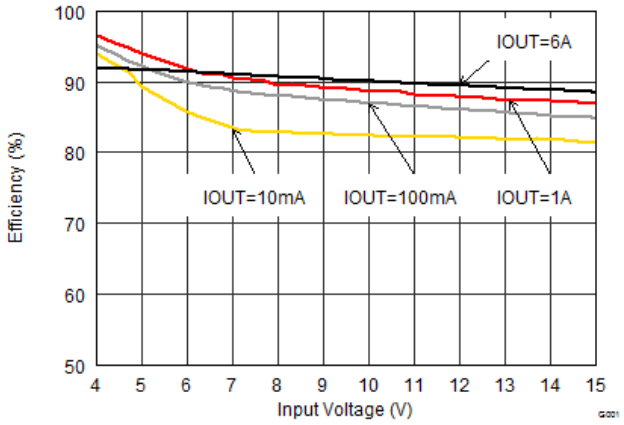
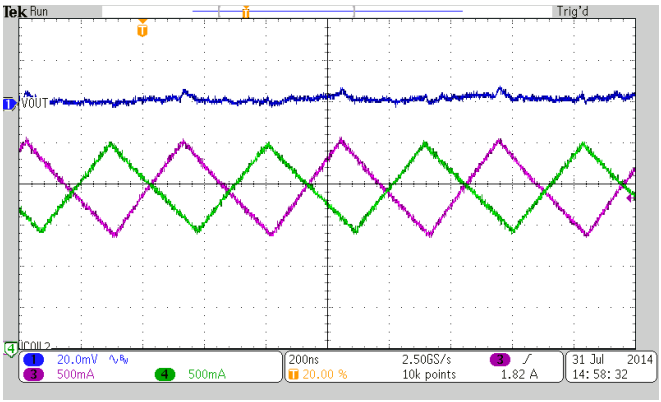
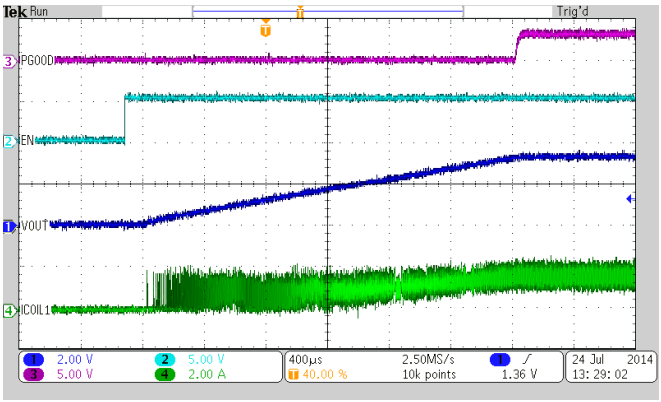


Figure 42. Efficiency vs Input Voltage



V_{IN} = 8 V, I_{OUT} = 4 A

Figure 43. Typical Operation (PWM)



C_{SS} = 10 nF

Figure 44. Startup into 1 Ω (3.3 A)

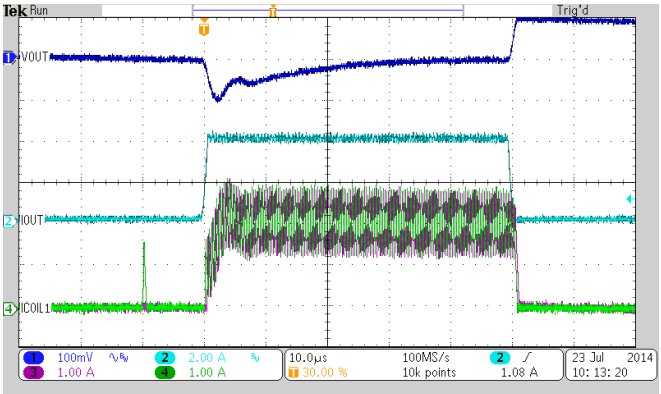


Figure 45. Load Transient Response (PSM-PWM)

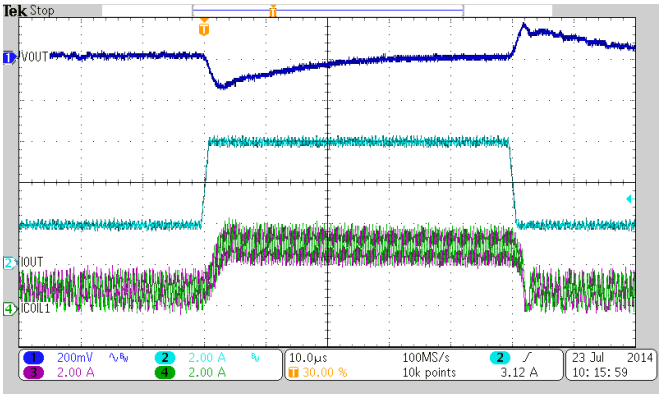
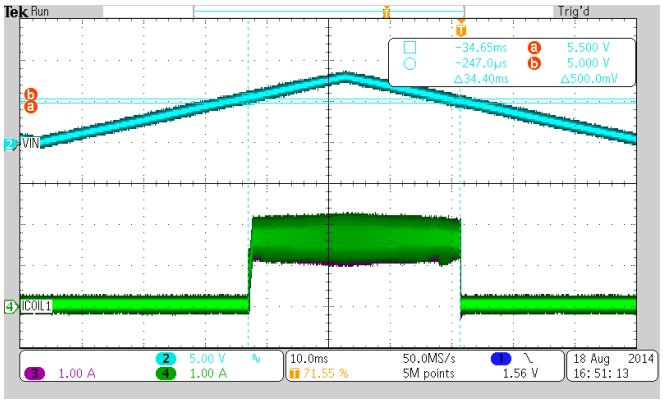


Figure 46. Load Transient Response (PWM-PWM)



V_{IN} = 5.5 V (Rising), V_{IN} = 5.0 V (Falling)

Figure 47. Accurate EN Threshold

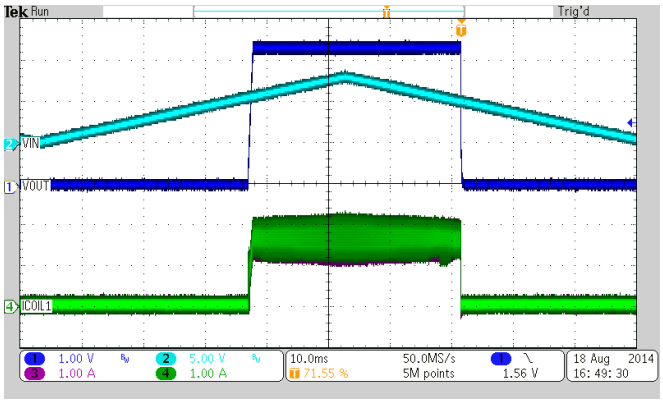
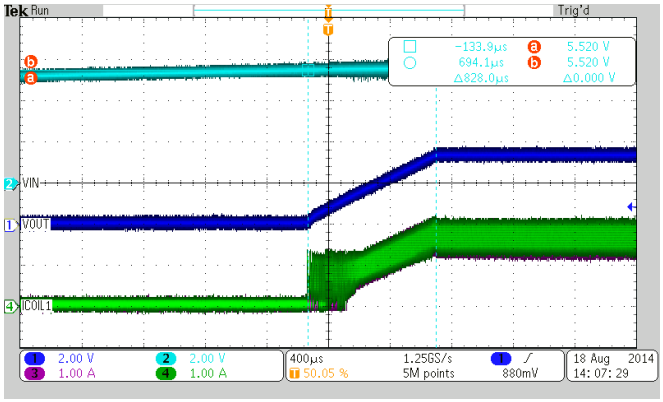
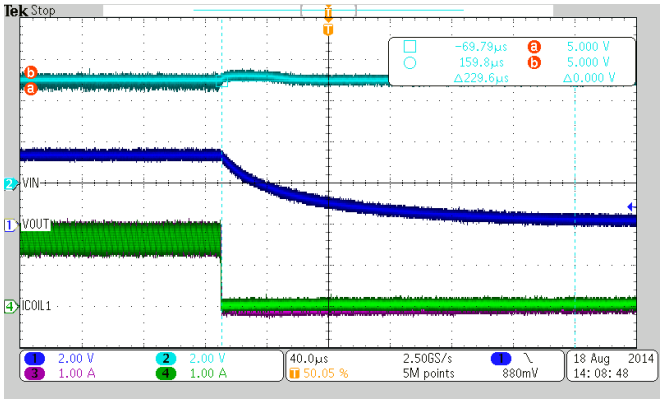


Figure 48. Accurate EN Threshold Showing V_{OUT}



V_{IN} = 5.5 V (Rising)

Figure 49. Accurate EN Threshold



V_{IN} = 5.0 V (Falling)

Figure 50. Accurate EN Threshold

9.3 TPS62180 Output Voltage Application Examples

This section provides typical schematics for commonly used output voltage values.

9.3.1 Application Schematic Examples

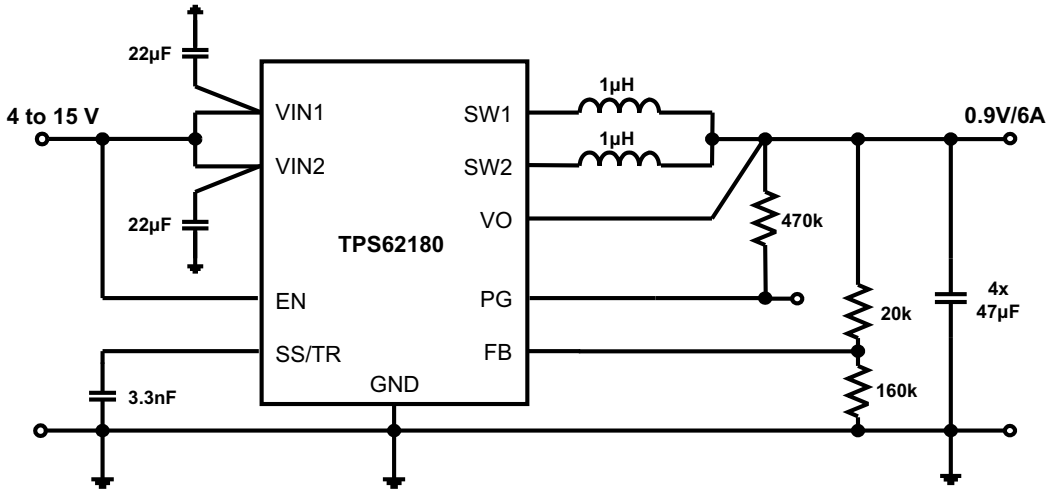


Figure 51. 0.9-V/6-A Power Supply

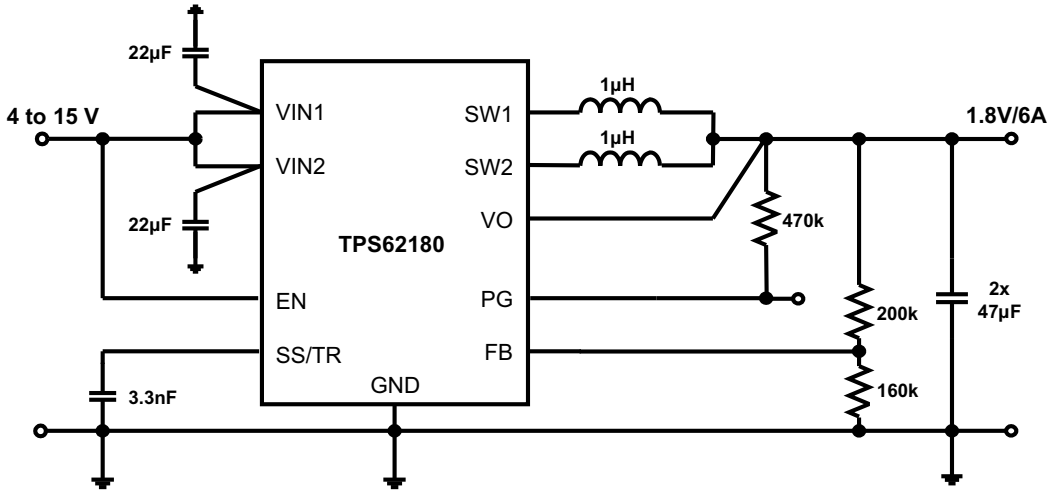


Figure 52. 1.8-V/6-A Power Supply

TPS62180 Output Voltage Application Examples (continued)

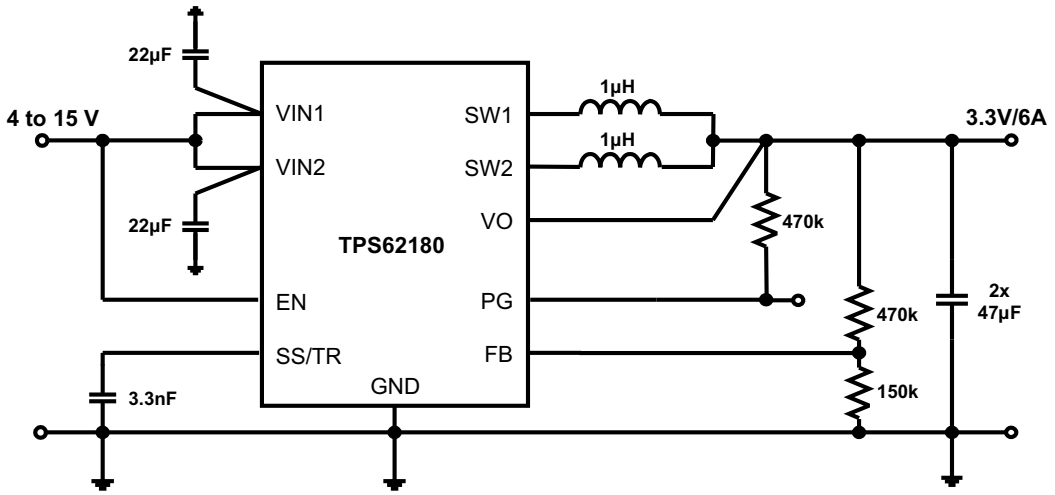


Figure 53. 3.3-V/6-A Power Supply

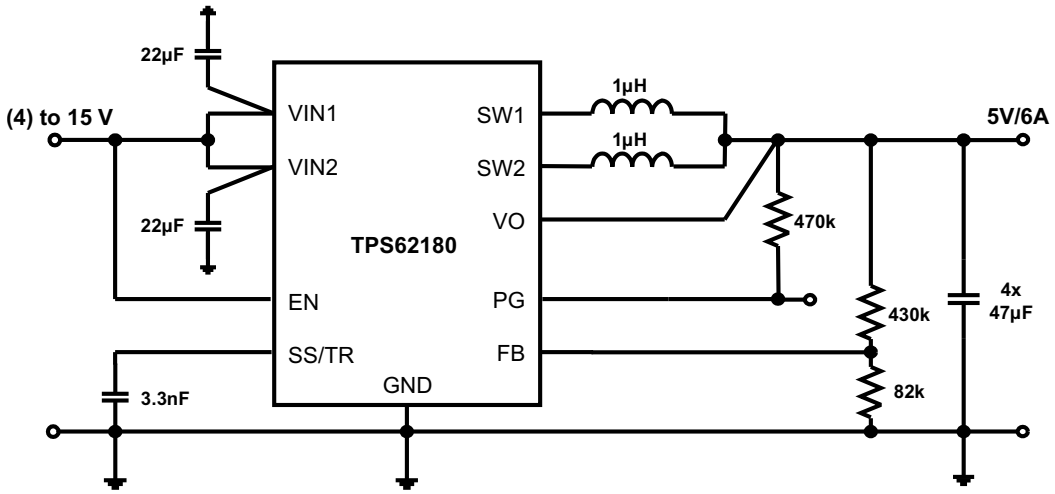


Figure 54. 5-V/6-A Power Supply

9.3.2 Design Requirements

Based on Figure 10, the schematics shown in Figure 51 through Figure 54 show different output voltage divider values to get different V_{OUT}. Another design target is to have about 5-µA current through the divider.

9.3.3 External Component Selection

The values for the voltage divider are derived using the procedure given in Programming the Output Voltage. While Equation 10 and Equation 11 are used to calculate R2 and R1, the values are aligned with standard resistor values.

10 Power Supply Recommendations

The TPS6218x are designed to operate from a 4-V to 15-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

11 Layout

11.1 Layout Guidelines

The PCB layout of the TPS6218x demands careful attention to ensure proper operation, thermal profile, low noise emission and to achieve best performance. A poor layout can lead to issues like poor regulation, stability and accuracy weaknesses, increased EMI radiation and noise sensitivity. While the TPS6218x provides very high power density, the PCB layout also contributes significantly to the thermal performance.

11.1.1 PCB Layout

A recommended PCB layout for the TPS62180 dual phase solution is shown below. It ensures best electrical and optimized thermal performance considering the following important topics:

- The input capacitors must be placed as close as possible to the appropriate pins of the device. This provides low resistive and inductive paths for the high di/dt input current. The input capacitance is split, as is the V_{IN} connection, to avoid interference between the input lines.
- The SW node connection from the IC to the inductor conducts high currents. It should be kept short and can be designed in parallel with an internal or bottom layer plane, to provide low resistance and enhanced thermal behavior.
- The V_{OUT} regulation loop is closed with C_{OUT} and its ground connection. If a ground layer or plane is used, a direct connection by vias, as shown, is recommended. Otherwise the connection of C_{OUT} to GND must be short for good load regulation.
- The FB node is sensitive to dv/dt signals. Therefore the resistive divider should be placed close to the FB pin, avoiding long trace distance. Using the TPS62182 (fixed output voltage version), the FB pin can be left floating, but it is good practice and recommended to connect it to AGND for best thermal characteristics.

11.2 Layout Example

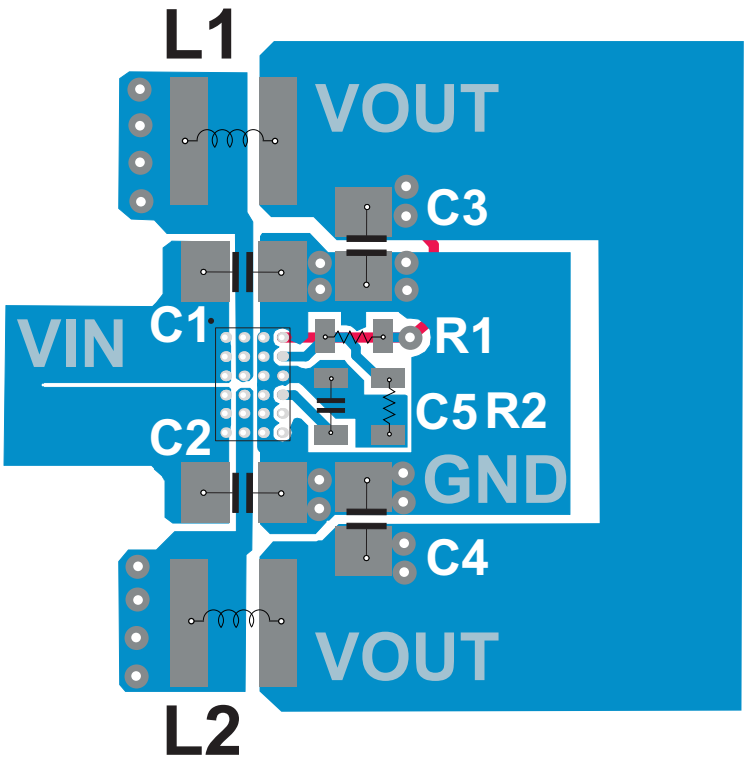


Figure 55. TPS62180 Board Layout

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **8.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
TPS62180	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62182	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 商标

AEE, NanoFree are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62180YZFR	Active	Production	DSBGA (YZF) | 24	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ELC180
TPS62180YZFR.A	Active	Production	DSBGA (YZF) | 24	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ELC180
TPS62180YZFT	Active	Production	DSBGA (YZF) | 24	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ELC180
TPS62180YZFT.A	Active	Production	DSBGA (YZF) | 24	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ELC180
TPS62182YZFR	Active	Production	DSBGA (YZF) | 24	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ELC182
TPS62182YZFR.A	Active	Production	DSBGA (YZF) | 24	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ELC182
TPS62182YZFT	Active	Production	DSBGA (YZF) | 24	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ELC182
TPS62182YZFT.A	Active	Production	DSBGA (YZF) | 24	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ELC182

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

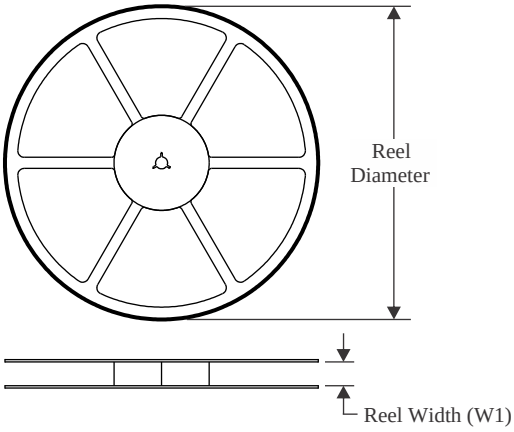
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

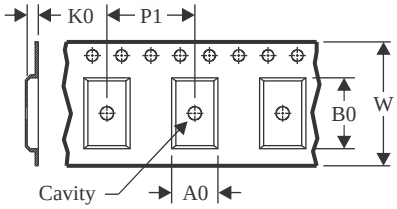
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

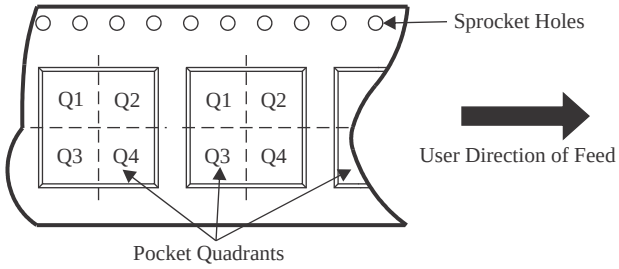


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

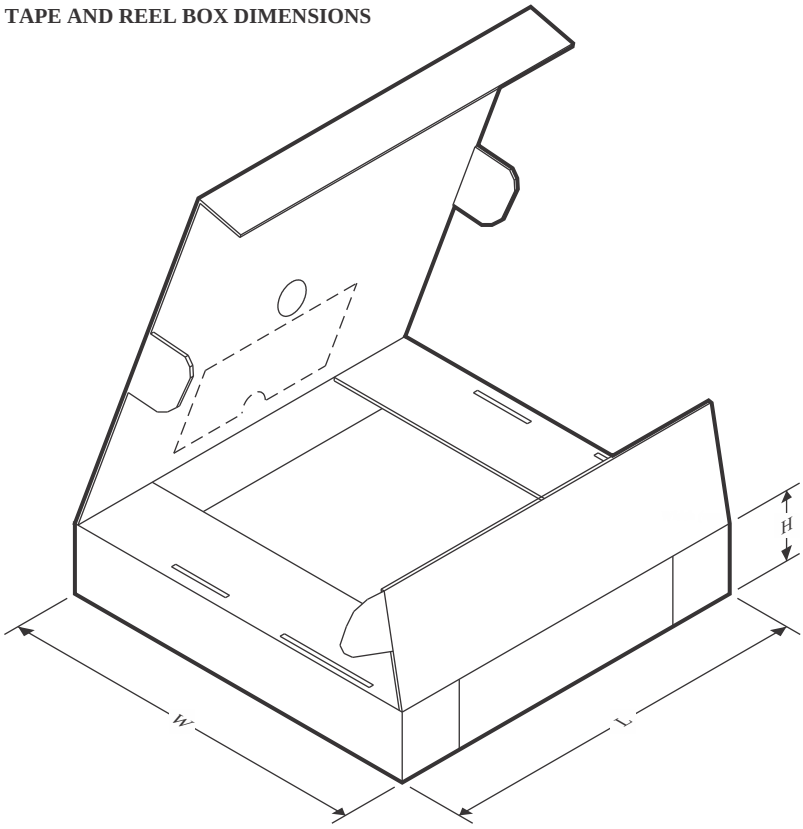
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62180YZFR	DSBGA	YZF	24	3000	330.0	12.4	2.25	3.25	0.81	4.0	12.0	Q1
TPS62180YZFT	DSBGA	YZF	24	250	330.0	12.4	2.25	3.25	0.81	4.0	12.0	Q1
TPS62182YZFR	DSBGA	YZF	24	3000	330.0	12.4	2.25	3.25	0.81	4.0	12.0	Q1
TPS62182YZFT	DSBGA	YZF	24	250	330.0	12.4	2.25	3.25	0.81	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

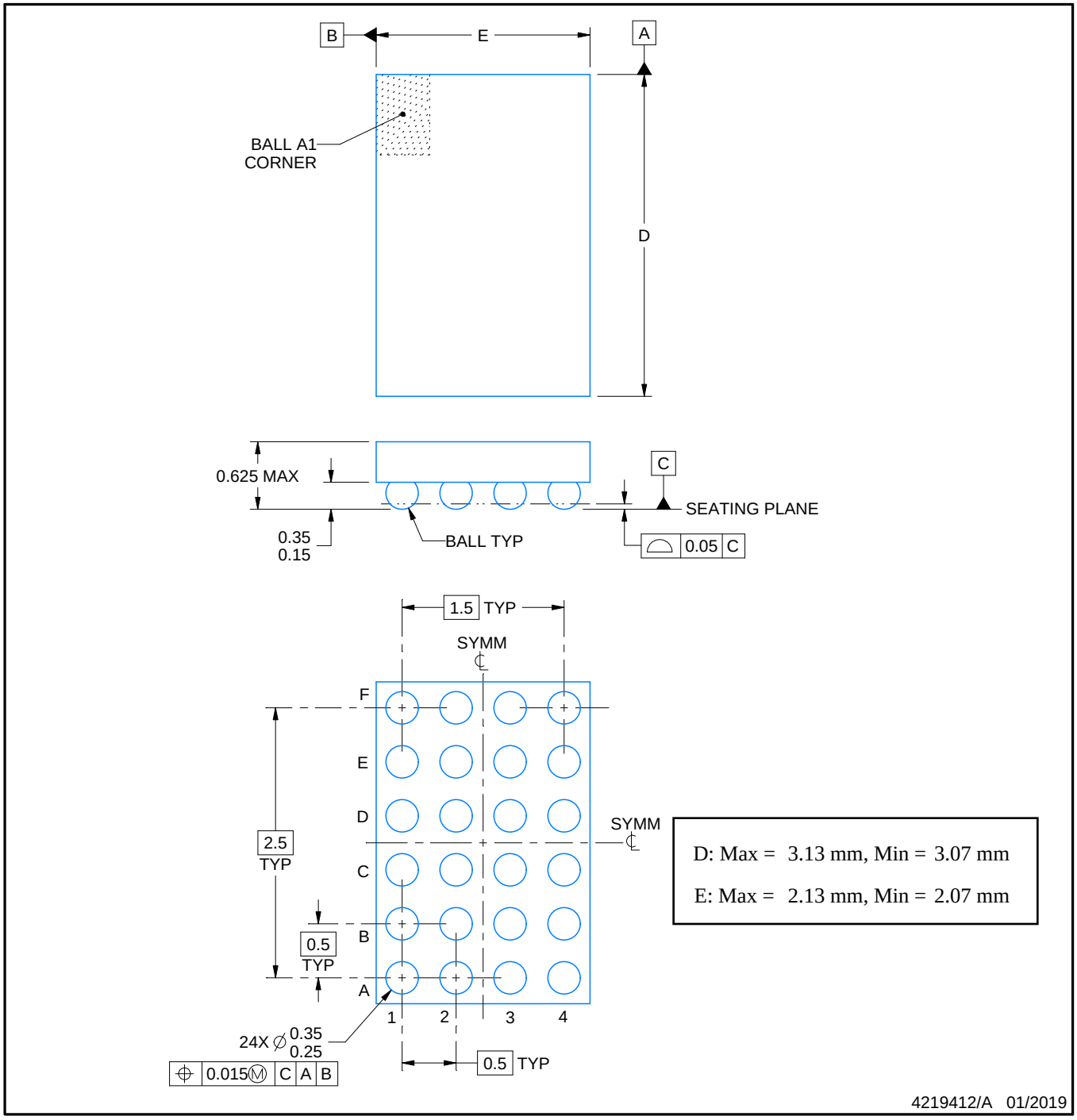
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62180YZFR	DSBGA	YZF	24	3000	335.0	335.0	25.0
TPS62180YZFT	DSBGA	YZF	24	250	335.0	335.0	25.0
TPS62182YZFR	DSBGA	YZF	24	3000	335.0	335.0	25.0
TPS62182YZFT	DSBGA	YZF	24	250	335.0	335.0	25.0

PACKAGE OUTLINE

YZF0024

DSBGA - 0.625 mm max height

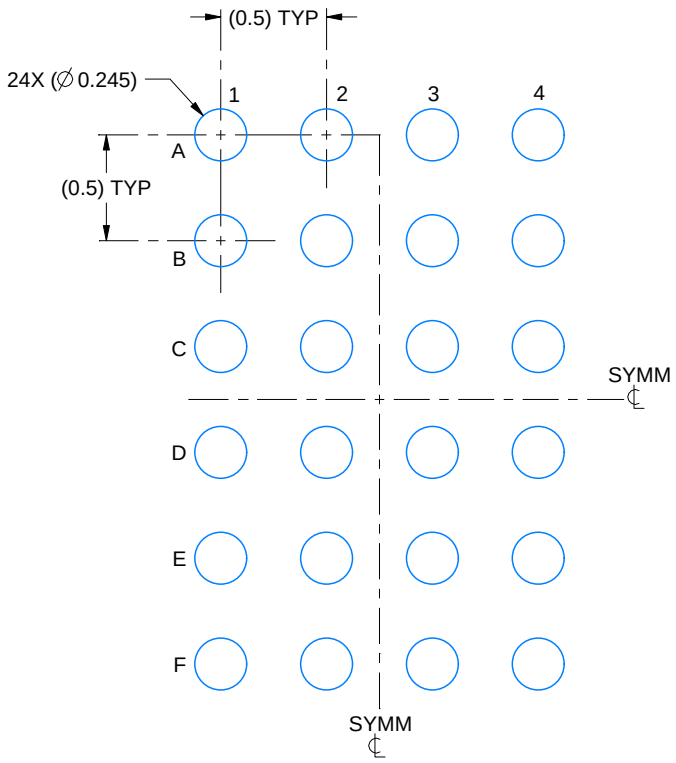
DIE SIZE BALL GRID ARRAY



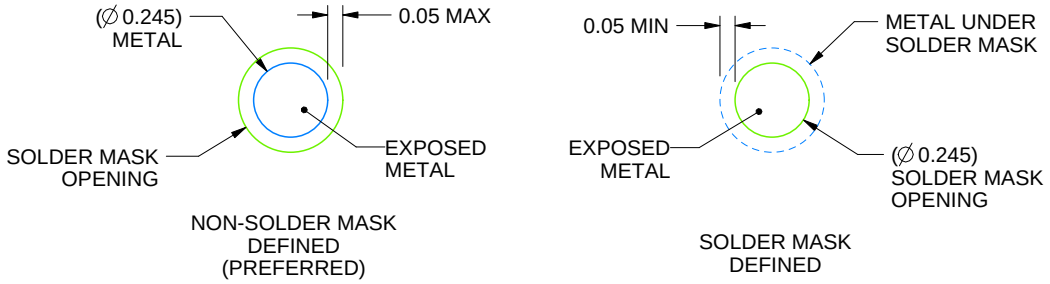
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:28X

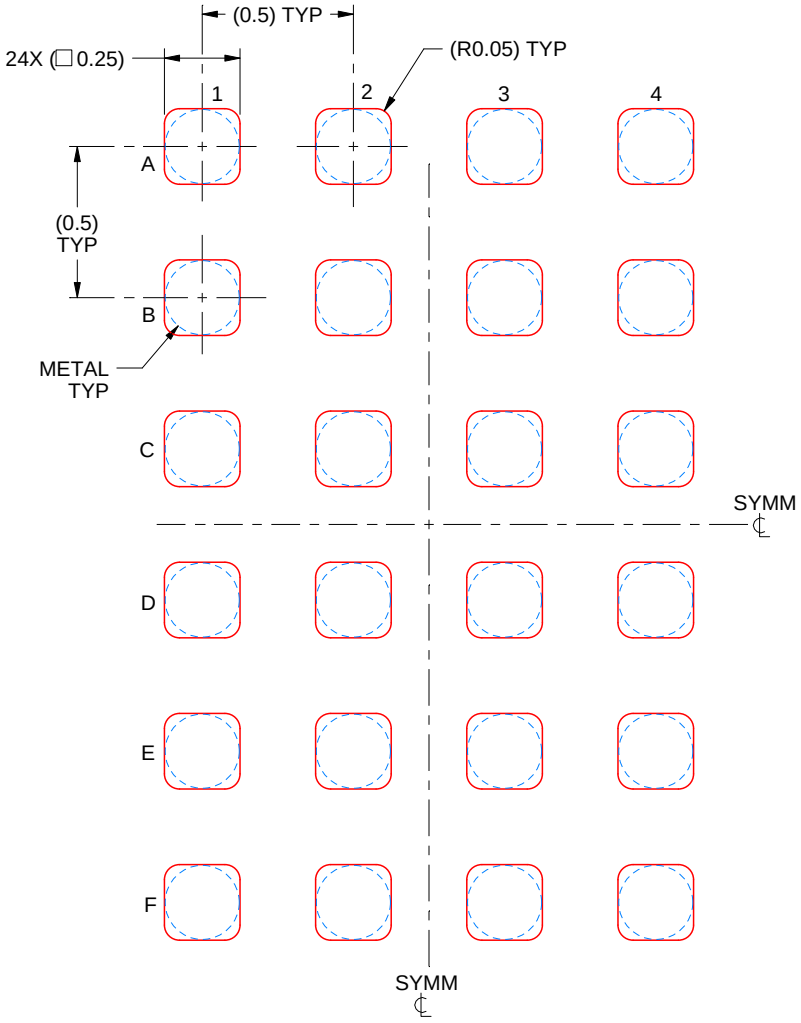


SOLDER MASK DETAILS
NOT TO SCALE

4219412/A 01/2019

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219412/A 01/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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