采用可湿侧面 QFN 封装的 TPS62097-Q1 2A 高效降压转换器

1 特性

- 符合 AEC-Q100 标准，其中包括以下内容：
  – 器件温度 1 级：–40°C 至 125°C 工作结温范围
  – 器件人体放电模型 (HBM) 静电放电 (ESD) 分类等级 2
  – 器件 CDM ESD 分类等级 C6
- 具有可选开关频率的 iDCS-Control 拓扑
- 强制 PWM 或省电模式
- 效率高达 97%
- 2.5V 至 6.0V 输入电压
- 0.8V 至 V_{IN} 可调输出电压
- 3.3V 固定输出电压，TPS6209733-Q1
- 输出电压精度为 ±1%
- 间断短路保护功能
- 可编程软启动
- 输出电压跟踪
- 可实现 100% 占空比，以确保最低压降
- 输出放电
- 电源正常输出
- 热关断保护
- 采用可湿侧面 3mm x 3mm QFN 封装

2 应用

- 网关
- 音响主机
- 仪表组
- 远程信息处理

3 说明

TPS62097-Q1 器件是一款同步降压转换器，经优化可用于高效率和噪声关键 应用。此器件主要用于宽输出电流范围内的高效转换。在中等负载至重负载状态下，此转换器在 PWM 模式下运行，且会在轻负载下自动进入节能运行模式。可使用外部电阻器在 1.5MHz 至 2.5MHz 范围内选择开关频率。iDCS-Control 可在强制 PWM 模式下以恒定开关频率实现低噪声运行。

为了解决系统电源轨的需求，内部补偿电路支持使用电容值高于 150μF 的各种外部输出电容器。为在启动过程中控制浪涌电流，此器件通过连接至 SS/TR 引脚的外部电容器提供了可编程软启动功能。SS/TR 引脚还可用于电压跟踪配置中。此器件还集成了短路保护、电源正常和热关断 功能。

器件信息[(1)]

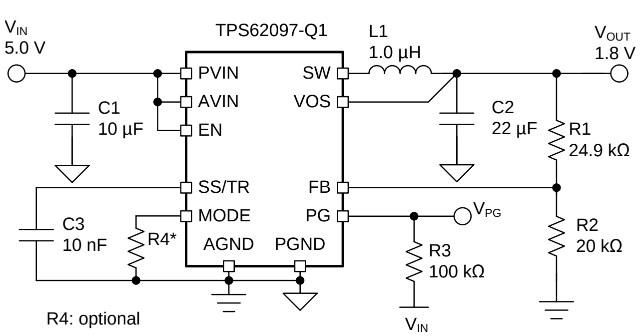
器件型号	封装	封装尺寸（标称值）
TPS62097-Q1	QFN (16)	3.0mm x 3.0mm
TPS6209733-Q1	QFN (16)	3.0mm x 3.0mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

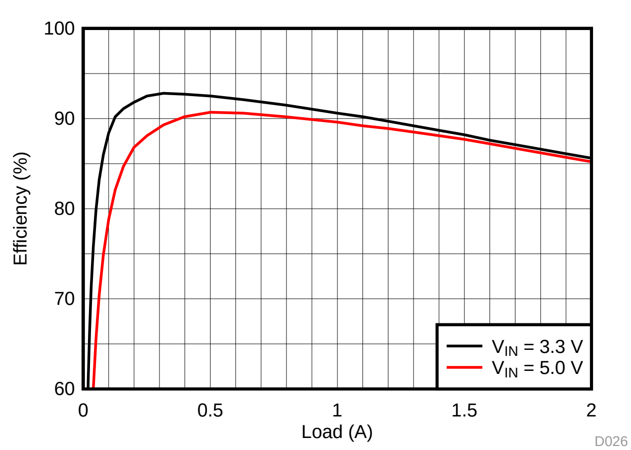
输出电压选项

器件型号	输出电压	标记符号
TPS62097-Q1	可调	9700Q
TPS6209733-Q1	3.3V	9733Q

1.8V 输出，典型应用



1.8V 输出，效率，模式 **=** 开环



目录

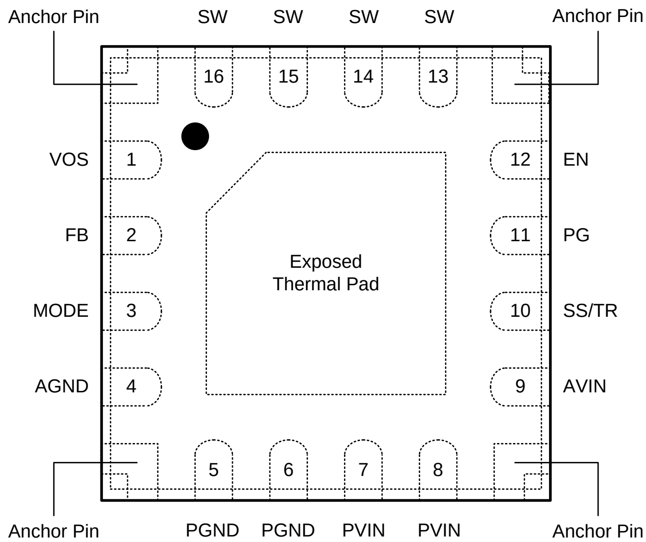
4 修订历史记录

Changes from Original (August 2017) to Revision A **Page**

- 产品数据发布。 ... 1

5 Terminal Configuration and Functions

RGT Package with Wettable Flanks
16-Pin VQFN
(Top View)



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Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
PGND	5,6		Power ground pin.
SW	13,14,15,16	PWR	Switch pin. It is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
VOS	1	I	Output voltage sense pin. This pin must be directly connected to the output capacitor.
FB	2	I	Feedback pin. For the adjustable output voltage version, a resistor divider sets the output voltage. For the fixed output voltage versions, this pin is recommended to be connected to AGND for improved thermal performance. The pin also can be left floating as an internal 400kΩ resistor is connected between this pin and AGND for fixed output voltage versions.
PG	11	O	Power good open drain output pin. The pull-up resistor should not be connected to any voltage higher than 6 V. If it's not used, leave the pin floating.
EN	12	I	Enable pin. To enable the device this pin needs to be pulled high. Pulling this pin low disables the device. This pin has an internal pull-down resistor of typically 375kΩ when the device is disabled.
PVIN	7,8	PWR	Power input supply pin.
AVIN	9	I	Analog input supply pin. Connect it to the PVIN pin together.
SS/TR	10	I	Soft startup and voltage tracking pin. A capacitor is connected to this pin to set the soft startup time. Leaving this pin floating sets the minimum startup time.
MODE	3	I	Mode selection pin. Connect this pin to AGND to enable Power Save Mode with automatic transition between PWM and Power Save Mode. Connect this pin to an external resistor or leave floating to enable forced PWM mode only. See 表 1.
AGND	4		Analog ground pin.
Exposed Thermal Pad			The exposed thermal pad is connected to AGND. It must be soldered for mechanical reliability.
Anchor Pins			These pins do not require an electrical connection but can be connected to AGND. They must be soldered for mechanical reliability. Refer to **EXAMPLE BOARD LAYOUT** at the end of this data sheet.

6 Specifications

6.1 Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
Voltage at Pins[2]	AVIN, PVIN, EN, VOS, PG	–0.3	6.0	V
	MODE, SS/TR, SW (DC)	–0.3	V_{IN}+0.3V	V
	FB	–0.3	3.0	V
	SW (AC, less than 100ns)[3]	-3	11	V
Sink current	PG	0	1.0	mA
Temperature	Operating Junction, T_J	-40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2500	V
		Charged-device model (CDM), per AEC Q100-011[1]	±1500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommend Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage range	2.5	6.0	V
V_{PG}	Pull-up resistor voltage	0	6.0	V
V_{OUT}	Output voltage range	0.8	V_{IN}	V
I_{OUT}	Output current range	0	2.0	A
T_J	Operating junction temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS62097-Q1WRGT	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953

6.5 Electrical Characteristics

T_J = -40°C to 125°C, and V_{IN} = 2.5V to 6.0V. Typical values are at T_J = 25°C and V_{IN} = 3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current into AVIN, PVIN	EN = High, Device not switching, T_J = –40°C to 85°C		40	57	µA
		EN = High, Device not switching		40	65	
I_{SD}	Shutdown current into AVIN, PVIN	EN = Low, T_J = –40°C to 85°C		0.7	3	µA
		EN = Low		0.7	10	
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling	2.2	2.3	2.4	V
		V_{IN} rising	2.3	2.4	2.5	
$T_{Q\ JSD}$	Thermal shutdown threshold	T_J rising		160		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE (EN, MODE)						
V_{H_EN}	High-level input voltage, EN pin			1.6	2.0	V
V_{L_EN}	Low-level input voltage, EN pin		1.0	1.3		V
$I_{EN,LKG}$	Input leakage current into EN pin	EN = High		0.01	0.9	µA
R_{PD}	Pull-down resistance at EN pin	EN = Low		375		kΩ
V_{H_MO}	High-level input voltage, MODE pin				1.2	V
V_{L_MO}	Low-level input voltage, MODE pin		0.4			V
$I_{MO,LKG}$	Input leakage current into MODE pin	MODE = High		0.01	0.16	µA
SOFT STARTUP, POWER GOOD (SS/TR, PG)						
I_{SS}	Soft startup current		5.5	7.5	9.5	µA
	Voltage tracking gain factor	V_{FB} / $V_{SS/TR}$		1		
V_{PG}	Power good threshold	V_{OUT} rising, referenced to V_{OUT} nominal	92	95	98	%
		V_{OUT} falling, referenced to V_{OUT} nominal	87	90	92	
$V_{PG,OL}$	Low-level output voltage, PG pin	I_{sink} = 1mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0V		0.01	1.6	µA
OUTPUT						
V_{OUT}	Output voltage accuracy TPS6209733Q	PWM mode, No load	–1.0		1.0	%
		PSM mode(1)	–1.0		2.1	
V_{FB}	Feedback reference voltage	PWM mode	792	800	808	mV
		PSM mode(1)	792	800	817	
$I_{FB,LKG}$	Input leakage current into FB pin	V_{FB} = 0.8V		0.01	0.1	µA
R_{DIS}	Output discharge resistor	EN = Low, V_{OUT} = 1.8V		165		Ω
	Line regulation	I_{OUT} = 0.5A, V_{OUT} = 1.8V(1)		0.02		%/V
	Load regulation	PWM mode, V_{OUT} = 1.8V (1)		0.2		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance	I_{SW} = 500mA, V_{IN} = 5.0V		42		mΩ
		I_{SW} = 500mA, V_{IN} = 3.6V		53		
	Low-side FET on-resistance	I_{SW} = 500mA, V_{IN} = 5.0V		40		mΩ
		I_{SW} = 500mA, V_{IN} = 3.6V		50		
I_{LIMF}	High-side FET forward current limit		3.1	3.6	4.2	A
		V_{IN} = 5.0V	3.3	3.6	3.9	
I_{LIMN}	Low-side FET negative current limit	Forced PWM mode	–1.25	–1.1	-0.7	A

(1) Conditions: L = 1µH, C_{OUT} = 22µF, Switching Frequency = 2.0MHz

6.6 Typical Characteristics

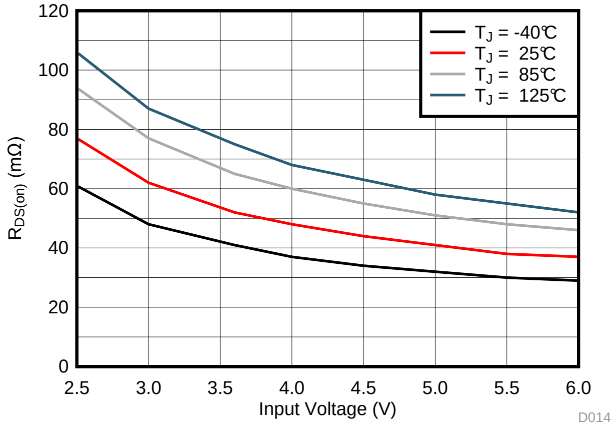


图 1. High-Side FET On-Resistance

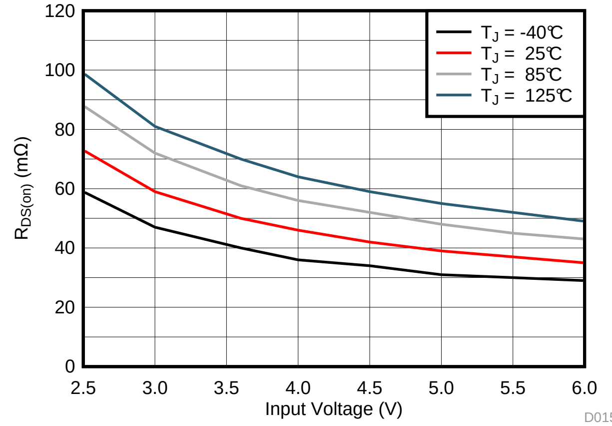


图 2. Low-Side FET On-Resistance

7 Detailed Description

7.1 Overview

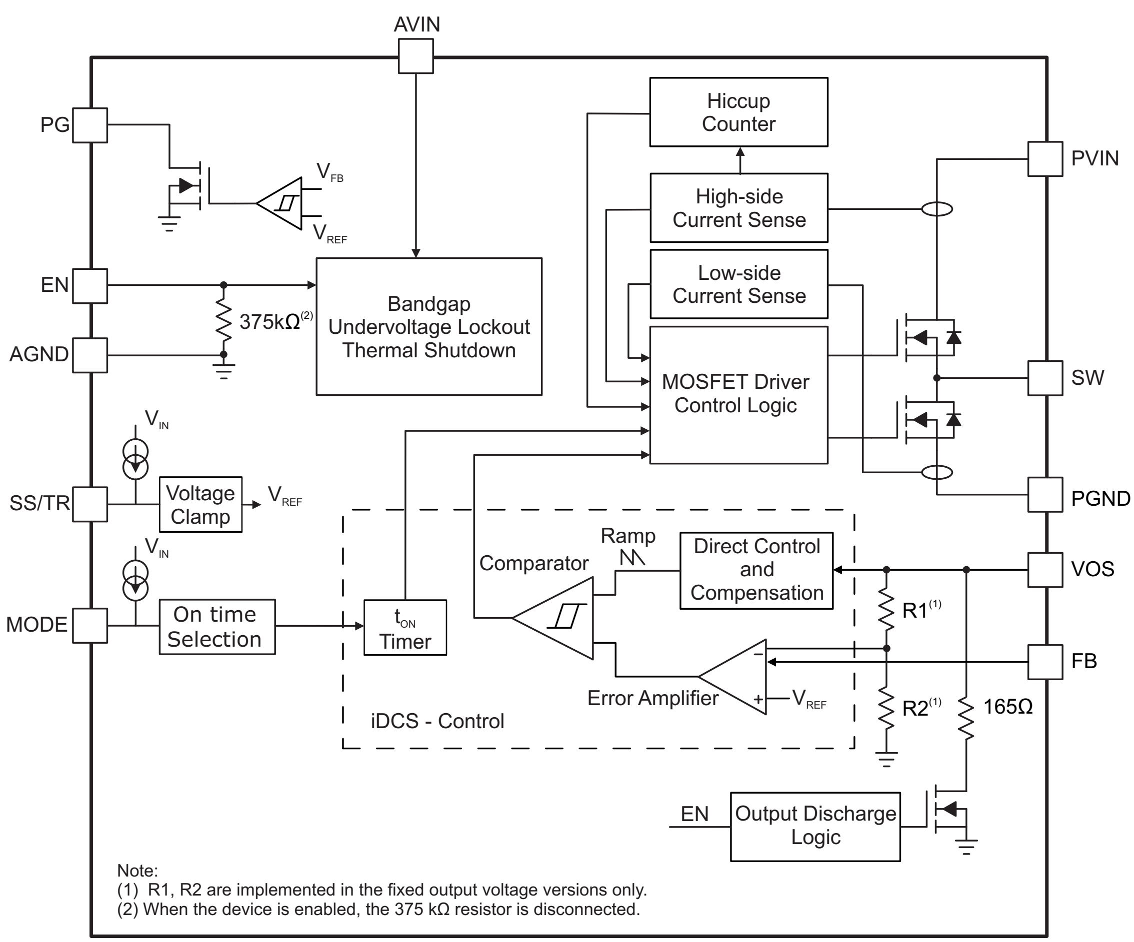
The TPS62097-Q1 synchronous step-down converter is based on the iDCS-Control (Industrial Direct Control with Seamless transition into Power Save Mode) topology. The control topology not only keeps the advantages of DCS-Control, but also provides other features:

- Forced PWM mode over the whole load range
- Selectable PWM switching frequency
- 1% output voltage accuracy
- Output voltage sequencing and tracking

The iDCS-Control topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in Power Save Mode (PSM) at light load conditions. Or the forced PWM mode removes power save mode operation and operates the device always at its nominal switching frequency.

In PWM mode, the device operates with a predictive On-time switching pulse. A constant switching frequency over the input and output voltage range is achieved by using an input and output voltage feed forward to set the on-time, as shown in 表 1. In PSM mode, the switching frequency is reduced to achieve high efficiency over the entire load current range. Since iDCS-Control supports both operation modes within a single building block, the transition from PWM mode to Power Save Mode is seamless and without effects on the output voltage.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 100% Duty Cycle Mode

The device offers a low input to output voltage dropout by entering 100% duty cycle mode, when the input voltage reaches the level of the output voltage. In this mode the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times (R_{DS(on)} + R_L) \quad (1)$$

where

- $V_{IN(min)}$ = Minimum input voltage to maintain a minimum output voltage
- I_{OUT} = Output current
- $R_{DS(on)}$ = High side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

When the device operates close to 100% duty cycle mode, the TPS62097-Q1 can't enter Power Save Mode regardless of the load current if the input voltage decreases to typically 15% above the output voltage. The device maintains output regulation in PWM mode.

7.3.2 Switch Current Limit and Hiccup Short Circuit Protection

The switch current limit prevents the devices from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted/saturated inductor or a heavy load/shorted output circuit condition. If the inductor current reaches the threshold I_{LIMF}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. Once this switch current limit is triggered 32 times, the devices stop switching and enable the output discharge. The devices then automatically start a new startup after a typical delay time of 100µs has passed. This is HICCUP short circuit protection and is implemented to reduce the current drawn during a short circuit condition. The devices repeat this mode until the high load condition disappears.

When the device is in forced PWM mode, the negative current limit of the low-side MOSFET is active. The negative current limit prevents excessive current from flowing back through the inductor to the input.

7.3.3 Under Voltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an under voltage lockout is implemented, which shuts down the devices at voltages lower than V_{UVLO} with a hysteresis of 100mV.

7.3.4 Thermal Shutdown

The device goes into thermal shutdown and stops switching once the junction temperature exceeds T_{JSD}. Once the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

7.4 Device Function Modes

7.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic High. Accordingly, shutdown mode is forced if the EN pin is pulled Low with a shutdown current of typically 0.7 µA.

In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal resistor of 165 Ω discharges the output via the VOS pin smoothly. The output discharge function also works when thermal shutdown, undervoltage lockout or HICCUP short circuit protection are triggered.

An internal pull-down resistor of 375 kΩ is connected to the EN pin when the EN pin is Low. The pull-down resistor is disconnected when the EN pin is High.

7.4.2 Power Save Mode and Forced PWM Mode (MODE)

The MODE pin is a multi-functional pin that allows the device operation in forced PWM mode or PWM/PSM mode, and to select the PWM switching frequency.

Device Function Modes (接下页)

Once the EN pin is pulled high, the IC enables internal circuit blocks and prepares to ramp the output up. The period between the rising edge of the EN pin and the beginning of the power stage switching is called the MODE detection time, typically 50µs. During the MODE detection time period, shown in 图 3, the PWM switching frequency and operating mode are set by the MODE pin status, as shown in 表 1.

The PWM switching frequency can't be changed after the detection time period. Only when the device is set in PWM/PSM mode during the MODE detection time period (MODE = AGND), it is possible to switch between PWM/PSM and forced PWM operation modes by toggling the MODE pin with a GPIO pin of a micro-controller, for example. The other four MODE pin selections force the device in PWM mode only.

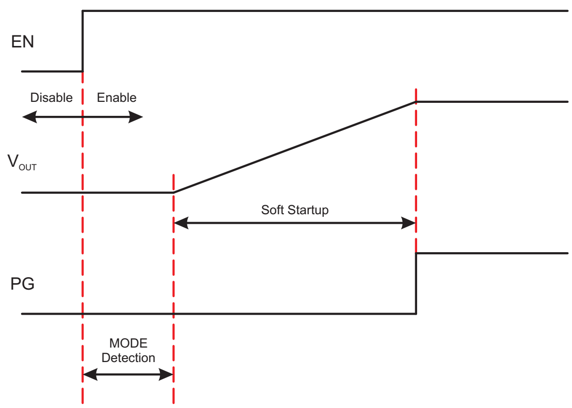


图 3. Power Up Sequence

表 1. Switching Frequency and Mode Selection

Typical PWM Switching Frequency (MHz)	Resistance at MODE pin (E24 EIA Value)	Toggle MODE pin after MODE detection	ON-Time Equation	Operating Mode
1.50	8.2kΩ ±5%	No	t_{ON} = 667ns x V_{OUT} / V_{IN}	Forced PWM
1.75	18kΩ ±5%	No	t_{ON} = 571ns x V_{OUT} / V_{IN}	Forced PWM
2.00	AGND	Yes	t_{ON} = 500ns x V_{OUT} / V_{IN}	PWM/PSM and Forced PWM
2.25	39kΩ ±5%	No	t_{ON} = 444ns x V_{OUT} / V_{IN}	Forced PWM
2.50	75kΩ ±5% or Open	No	t_{ON} = 400ns x V_{OUT} / V_{IN}	Forced PWM

Connecting the MODE pin to AGND with a resistor or leaving the MODE pin open forces the device into PWM mode for the whole load range. The device operates with a constant switching frequency that allows simple filtering of the switching frequency for noise sensitive applications. In forced PWM mode, the efficiency is lower than that of PSM at light load.

Connecting the MODE pin to the AGND pin enables Power Save Mode with an automatic transition between PWM and Power Save Mode. As the load current decreases and the inductor current becomes discontinuous, the device enters Power Save Mode operation automatically. In Power Save Mode, the switching frequency is reduced and estimated by 公式 2. In Power Save Mode, the output voltage rises slightly above the nominal output voltage, as shown in 图 13. This effect is minimized by increasing the output capacitor.

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^{2} \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (2)$$

When the device operates close to 100% duty cycle mode, the TPS62097-Q1 can't enter Power Save Mode regardless of the load current if the input voltage decreases to typically 15% above the output voltage. The device maintains output regulation in PWM mode.

7.4.3 Soft Startup (SS/TR)

The TPS62097-Q1 programs its output voltage ramp rate with the SS/TR pin. Connecting an external capacitor to SS/TR enables output soft startup to reduce inrush current from the input supply. The device charges the capacitor voltage to the input supply voltage with a constant current of typically 7.5µA. The FB pin voltage follows the SS/TR pin voltage until the internal reference voltage of 0.8V is reached. The soft startup time is calculated using 公式 3. Keep the SS/TR pin floating to set the minimum startup time.

$$t_{SS} = C_{SS/TR} \times \frac{0.8V}{7.5\mu A} \quad (3)$$

An active pull-down circuit is connected to the SS/TR pin. It discharges the external soft startup capacitor in case of disable, UVLO, thermal shutdown and HICCUP short circuit protection.

7.4.4 Voltage Tracking (SS/TR)

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in 图 4. From 0 V to 0.8 V, the internal reference voltage to the internal error amplifier follows the SS/TR pin voltage. When the SS/TR pin voltage is above 0.8 V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.8 V. The device achieves ratiometric or coincidental (simultaneous) output tracking, as shown in 图 5.

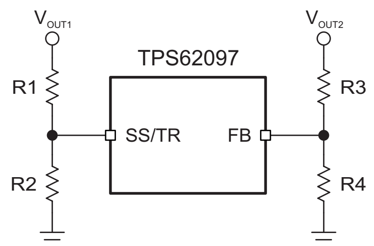


图 4. Output Voltage Tracking

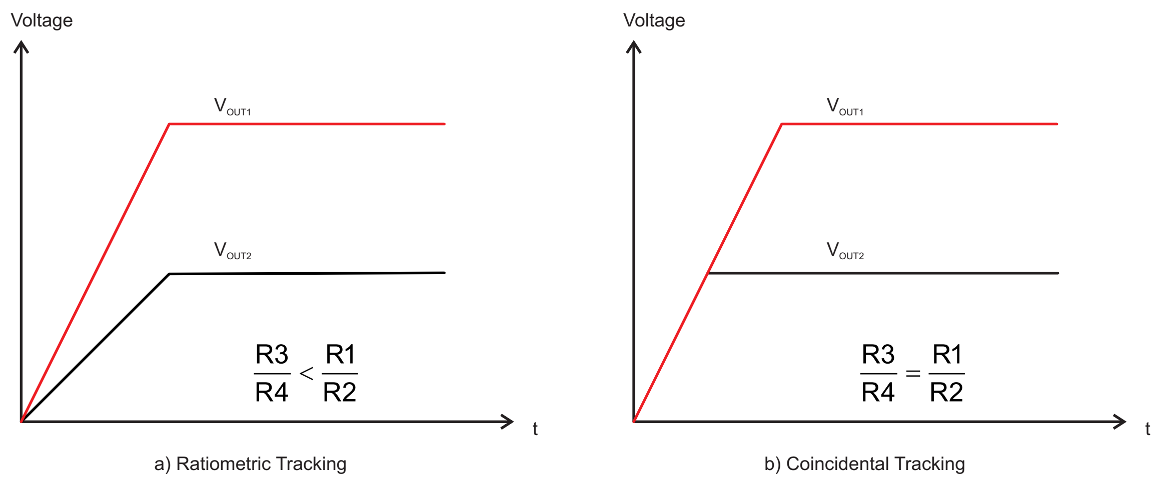


图 5. Voltage Tracking Options

The R2 value should be set properly to achieve accurate voltage tracking by taking 7.5 µA soft startup current into account. 1 kΩ or smaller is a sufficient value for R2.

For decreasing SS/TR pin voltage, the device doesn't sink current from the output when the device is in PSM. So the resulting decreases of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is V_{IN}+0.3V.

7.4.5 Power Good (PG)

The TPS62097-Q1 has a power good output. The PG pin goes high impedance once the output voltage is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open drain output and is specified to sink up to 1mA. The power good output requires a pull-up resistor connected to any voltage rail less than 6V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin floating when not used. 表 2 shows the PG pin logic.

表 2. PG Pin Logic

Device Conditions		Logic Status	
		High Z	Low
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = Low, $V_{FB} \leq V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	0.7 V < V_{IN} < V_{UVLO}		√
Power Supply Removal	$V_{IN} \leq 0.7$ V	√	

8 Application Information

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design of the TPS62097-Q1.

8.2 1.8-V Output Application

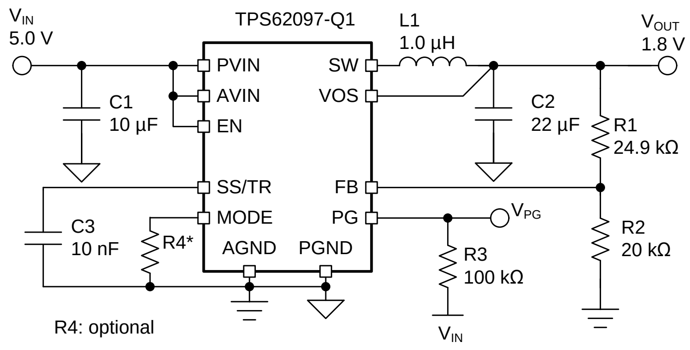


图 6. 1.8-V Output Application Schematic

8.2.1 Design Requirements

For this design example, use the following as the input parameters.

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 6 V
Output voltage	1.8 V
Output current	2.0 A

表 4 lists the components used for the example.

表 4. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	10 µF, Ceramic Capacitor, 6.3V, X7R, size 0805, C2012X7R0J106M125AB	TDK
C2	22 µF, Ceramic Capacitor, 6.3V, X7S, size 0805, C2012X7S1A226M125AC	TDK
C3	10 nF, Ceramic Capacitor, 6.3V, X7R, size 0603, GRM188R70J103KA01	Murata
L1	1 µH, Shielded, 5.4A, XFL4020-102MEB	Coilcraft
R1	Depending on the output voltage, 1% accuracy	Std
R2	20 kΩ, 1% accuracy	Std
R3	100 kΩ, 1% accuracy	Std

(1) See *Third-party Products Disclaimer*

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \quad (4)$$

R2 should not be higher than 20 kΩ to reduce noise coupling into the FB pin and improve the output voltage regulation. Choose additional resistor values for other outputs. A feed forward capacitor is not required.

The fixed output voltage version, TPS6209733-Q1, does not need an external resistor divider. TI recommends to connect the FB pin to AGND for improved thermal performance.

8.2.2.2 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify the selection process, 表 5 outlines possible inductor and capacitor value combinations for most applications.

表 5. Output Capacitor / Inductor Combinations

NOMINAL L [µH](1)	NOMINAL C_{OUT} [µF](2)				
	10	22	47	100	150
0.47					
1		+(3)	+	+	+
2.2					

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%. The required effective inductance is 500nH minimum.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and -50%.
(3) Typical application configuration. Other '+' mark indicates recommended filter combinations. Other values may be acceptable in applications but should be fully tested by the user. Refer to the application note SLVA710.

8.2.2.3 Inductor Selection

The main parameters for the inductor selection are the inductor value and the saturation current. To calculate the maximum inductor current under static load conditions, 公式 5 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (5)$$

Where:

$I_{OUT,MAX}$ = Maximum output current
ΔI_L = Inductor current ripple
f_{SW} = Switching frequency
L = Inductor value

TI recommends to choose the saturation current for the inductor 20% to 30% higher than the $I_{L,MAX}$, out of 公式 5. A higher inductor value is also useful to lower ripple current but increases the transient response time as well.

8.2.2.4 Capacitor Selection

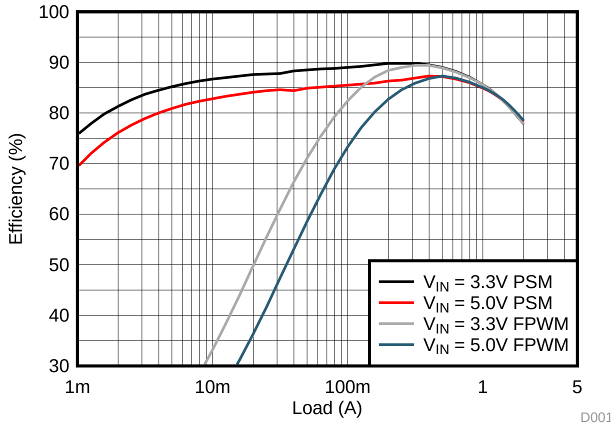
The input capacitor is the low impedance energy source for the converters which helps to provide stable operation. A low ESR multilayer ceramic capacitor is required for best filtering and should be placed between PVIN and PGND as close as possible to those pins. For most applications a 10-µF capacitor is sufficient, though a larger value reduces input current ripple.

The architecture of the TPS62097-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends to use X7R or X5R dielectrics. The recommended typical output capacitor value is 22 µF and can vary over a wide range as outlined in 表 5.

Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating. Ensure that the input effective capacitance is at least 5 µF and the output effective capacitance is at least 10 µF.

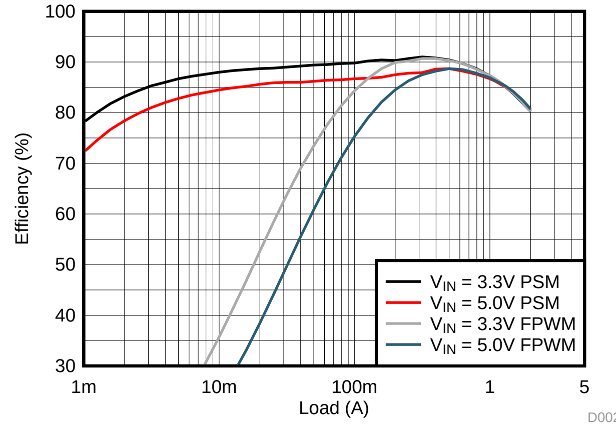
8.2.3 Application Performance Curves

T_A = 25°C, BOM = 表 4 unless otherwise noted.



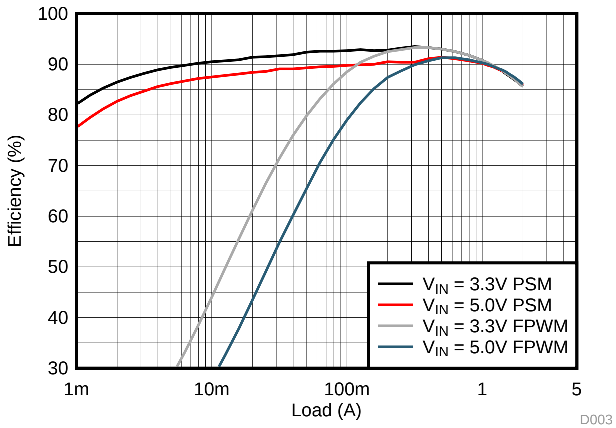
V_{OUT} = 1.0 V　　F_{SW} = 2.0 MHz

图 7. Efficiency



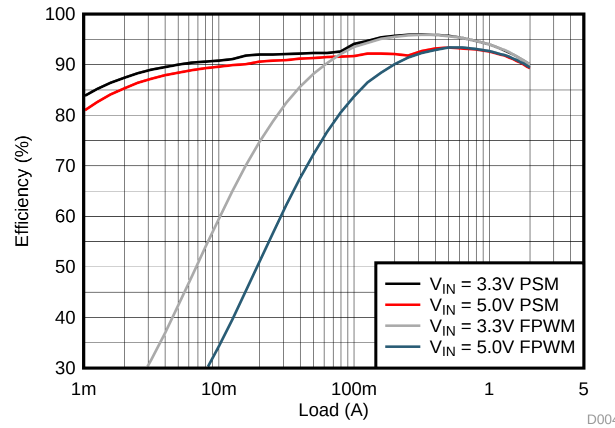
V_{OUT} = 1.2 V　　F_{SW} = 2.0 MHz

图 8. Efficiency



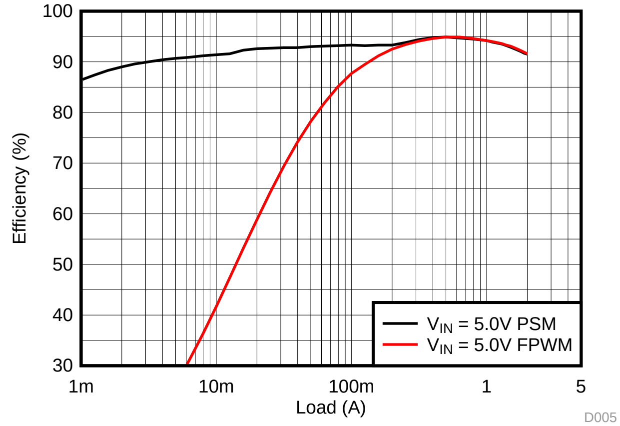
V_{OUT} = 1.8 V　　F_{SW} = 2.0 MHz

图 9. Efficiency



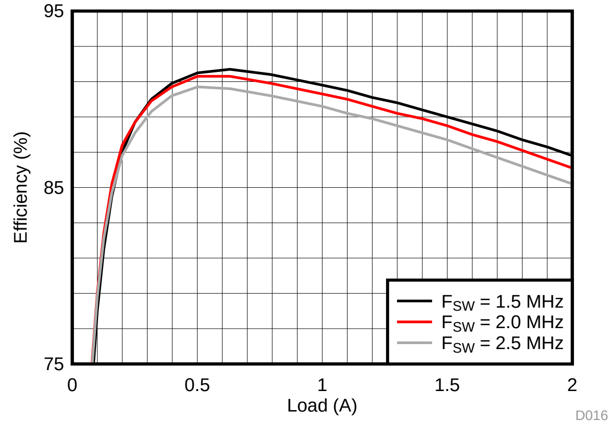
V_{OUT} = 2.5 V　　F_{SW} = 2.0 MHz

图 10. Efficiency



V_{OUT} = 3.3 V F_{SW} = 2.0 MHz

图 11. Efficiency



V_{OUT} = 1.8 V V_{IN} = 5.0 V

图 12. Efficiency with Different Switching Frequency

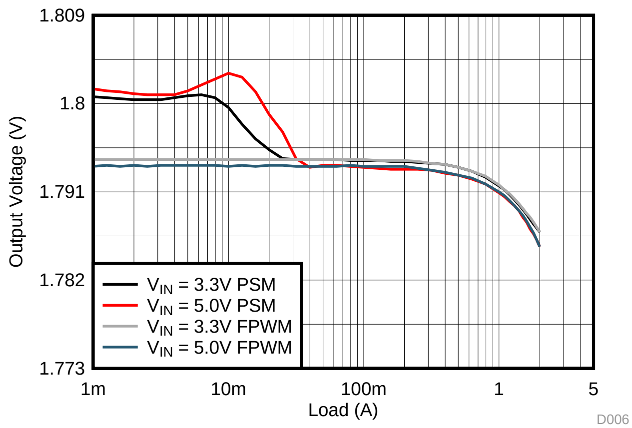


图 13. Load Regulation

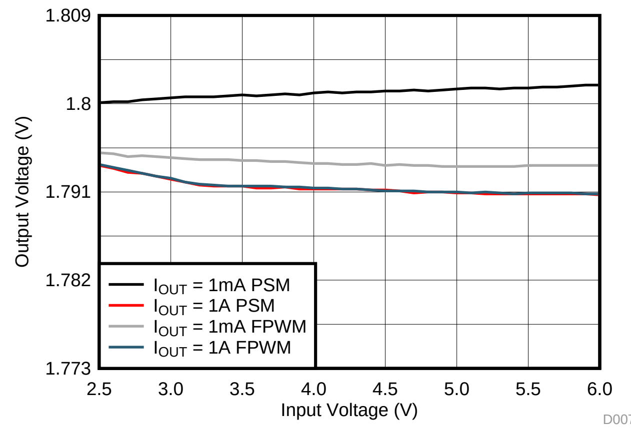
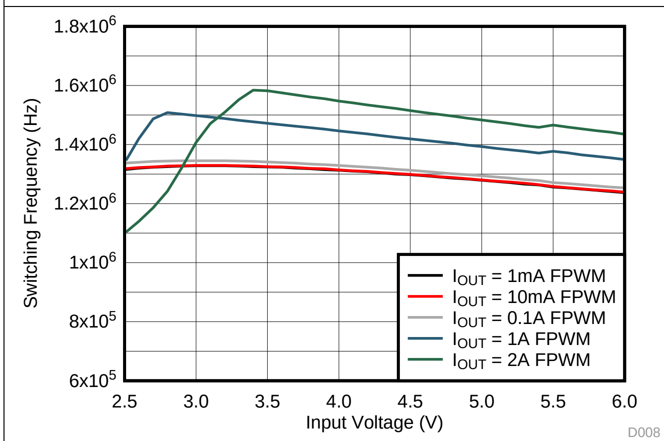
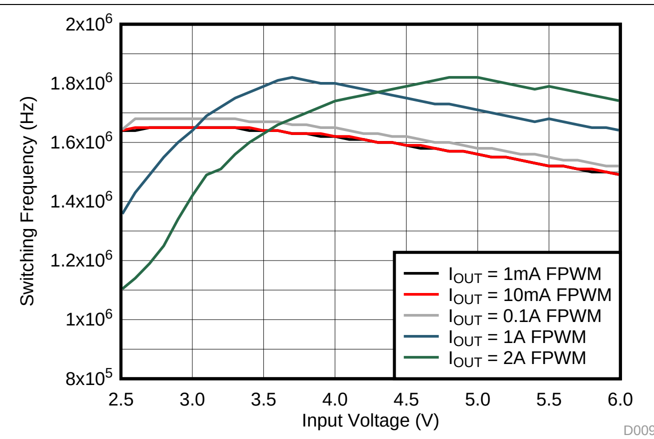


图 14. Line Regulation



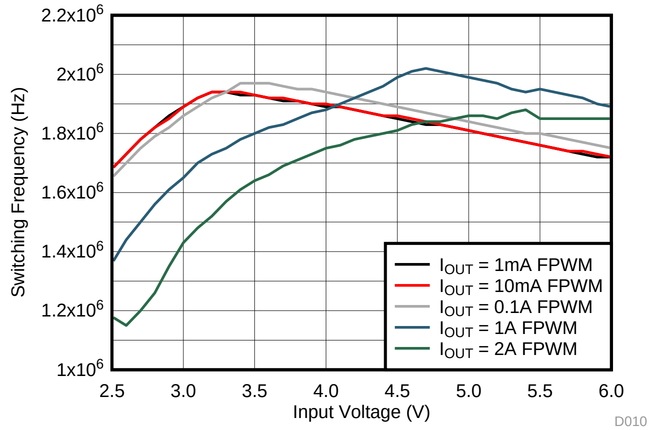
V_{OUT} = 1.0 V R_{Mode} = 8.2 kΩ

图 15. Switching Frequency, Forced PWM Mode (1.5 MHz)



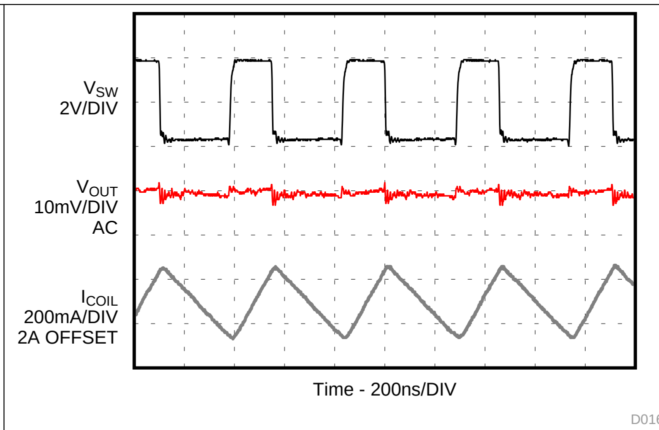
V_{OUT} = 1.0 V   MODE = AGND, Forced PWM

图 16. Switching Frequency, Forced PWM Mode (2.0MHz)



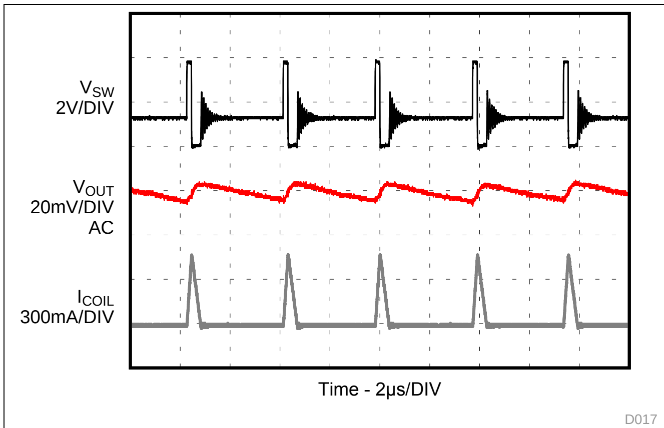
V_{OUT} = 1.0 V　　MODE = Open

图 17. Switching Frequency, Forced PWM Mode (2.5MHz)



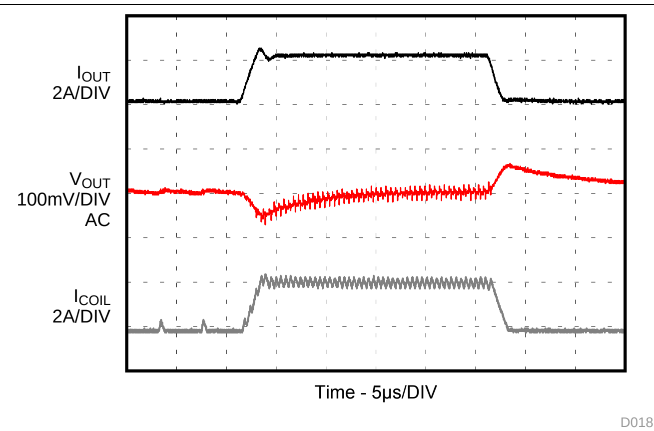
V_{OUT} = 1.2 V　　I_{OUT} = 2 A

图 18. Output Ripple, PWM Operation (2.0MHz)



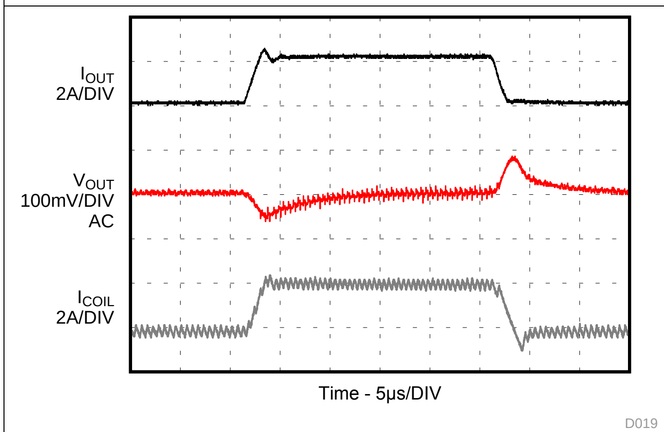
V_{OUT} = 1.2 V　　I_{OUT} = 30 mA

图 19. Output Ripple, PSM Operation



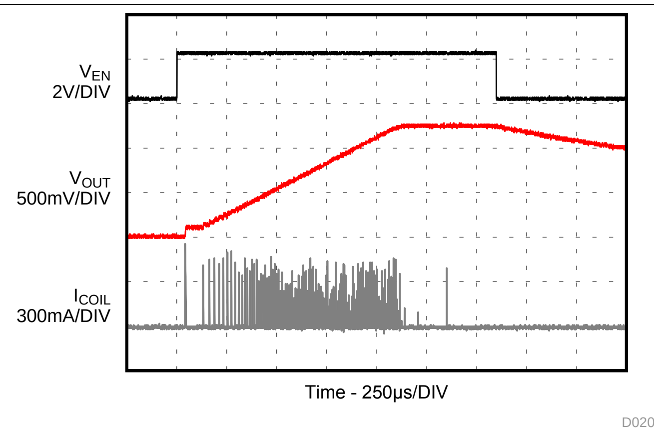
V_{OUT} = 1.2 V　　I_{OUT} = 0 A to 2 A, 1A / µs

图 20. Load Transient, PWM/PSM Mode (2.0MHz)



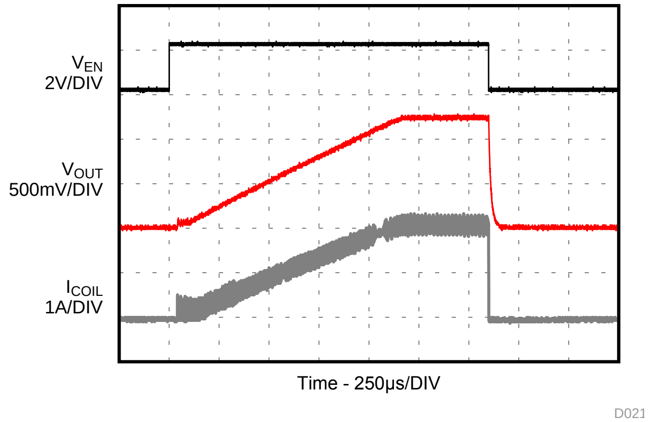
V_{OUT} = 1.2 V　　I_{OUT} = 0 A to 2 A, 1A / µs

图 21. Load Transient, Forced PWM Mode (2.0MHz)



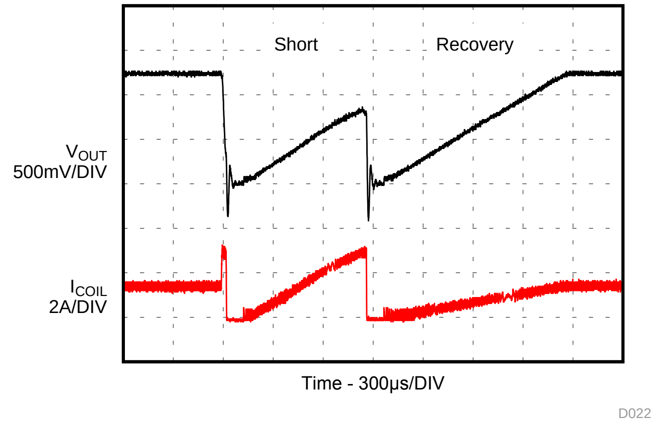
V_{OUT} = 1.2 V　　R_{OUT} = No Load

图 22. Startup and Shutdown without Load



V_{OUT} = 1.2 V R_{OUT} = 0.6 Ω (2 A)

图 23. Startup and Shutdown with Load



V_{OUT} = 1.2 V R_{OUT} = 0.8 Ω (1.5 A) with 1-ms short

图 24. Short Circuit Protection, HICCUP

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 2.5V and 6V. The average input current of the TPS62097-Q1 is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \quad (6)$$

Ensure that the power supply has a sufficient current rating for the application.

10 PCB Layout

10.1 Layout Guidelines

- TI recommends to place all components as close as possible to the IC. Specially, the input capacitor placement must be closest to the PVIN and PGND pins of the device.
- The low side of the input and output capacitors must be connected directly to the PGND pin to avoid a ground potential shift.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- The sense trace connected to VOS pin is a signal trace. Special care should be taken to avoid noise being induced. Keep the trace away from SW nodes.
- Refer to 图 25 for an example of component placement, routing and thermal design.

10.2 Layout Example

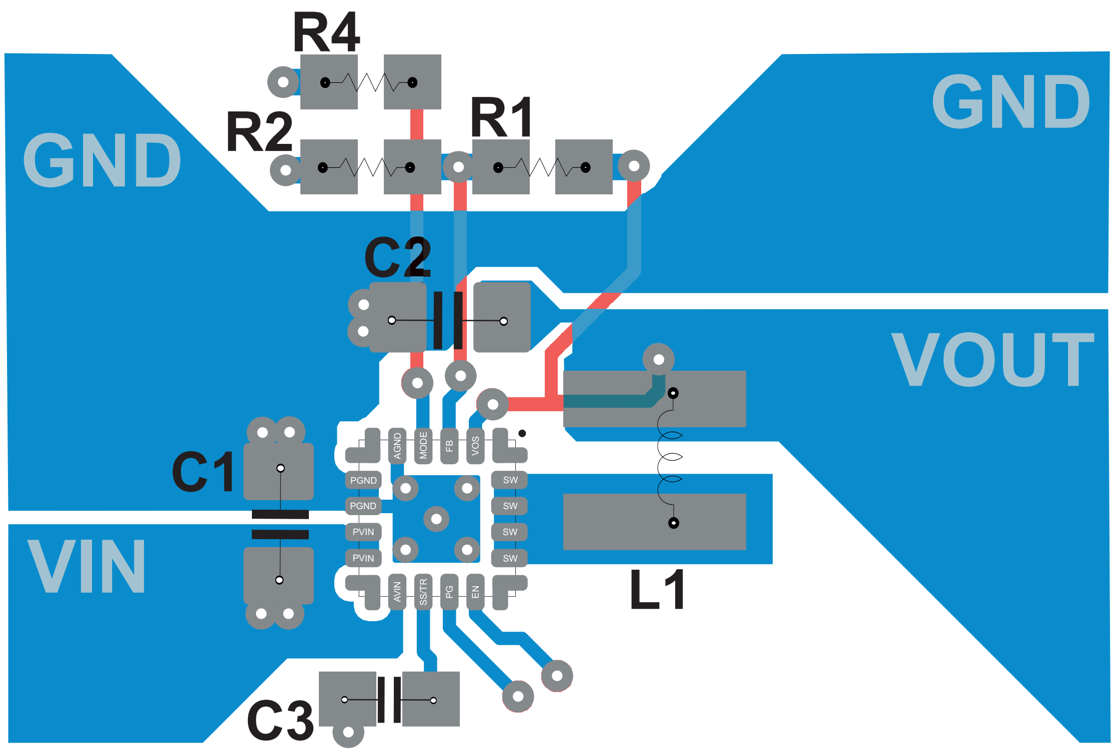


图 25. TPS62097-Q1 PCB Layout

10.3 Thermal Information

Implementation of integrated circuits in low-profile and fine pitch surface mount packages typically requires special attention to power dissipation. Many system dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component. For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes SZZA017 and SPRA953.

11 器件和文档支持

11.1 器件支持

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

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11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS6209733QWRGTRQ1	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	9733Q
TPS6209733QWRGTRQ1.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	9733Q
TPS6209733QWRGTRQ1.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	9733Q
TPS62097QWRGTRQ1	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	9700Q
TPS62097QWRGTRQ1.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	9700Q
TPS62097QWRGTRQ1.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	9700Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62097-Q1 :

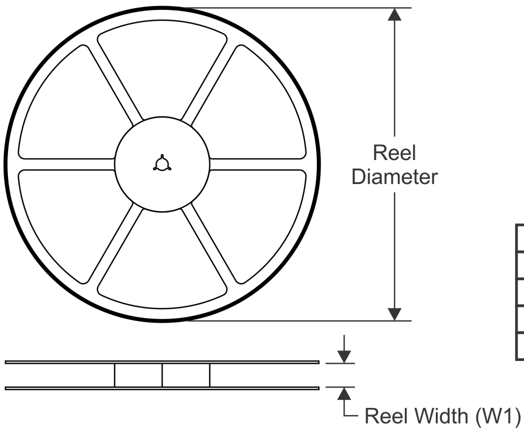
- Catalog : TPS62097

NOTE: Qualified Version Definitions:

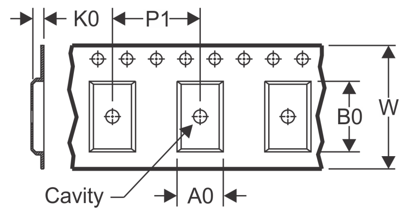
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

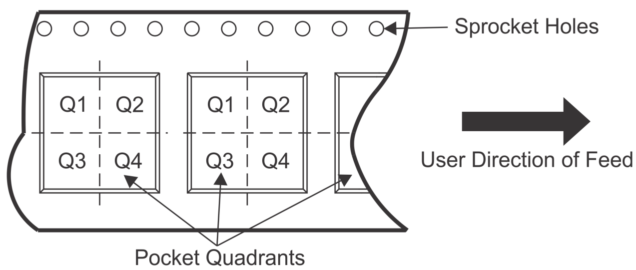


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

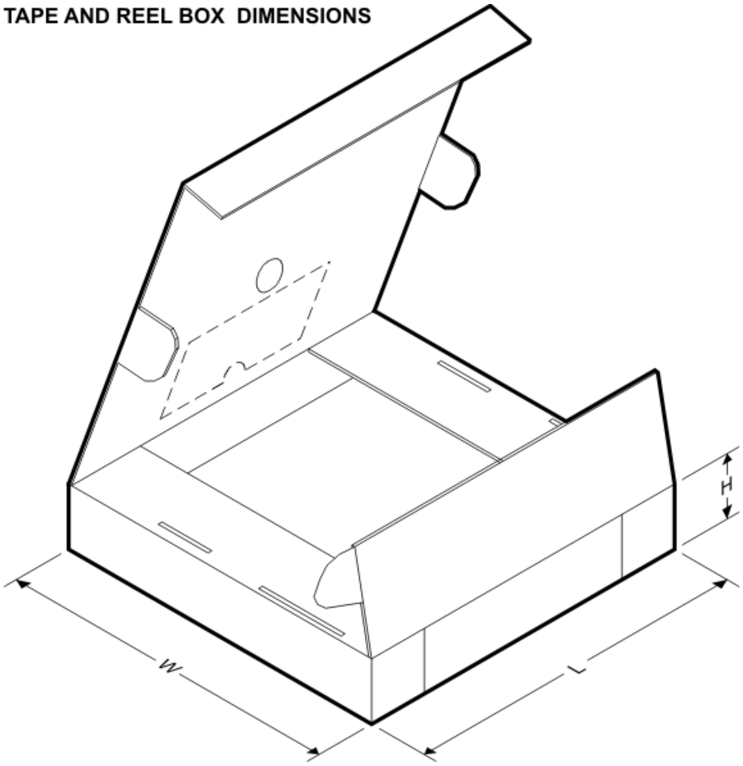
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6209733QWRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS62097QWRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6209733QWRGTRQ1	VQFN	RGT	16	3000	367.0	367.0	38.0
TPS62097QWRGTRQ1	VQFN	RGT	16	3000	367.0	367.0	38.0

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265