带有 DCS™ 控制的 3A 高效同步降压转换器

查询样品: TPS62090, TPS62091, TPS62092, TPS62093

特性

- **2.5 V** 至 **6 V** 输入电压范围
- **DCS™** 控制
- 转换器效率 **95%**
- 省电模式
- **20 µA** 运行静态电流
- 针对最低压降的 **100%** 占空比
- **2.8 MHz/1.4 MHz** 典型开关频率
- **0.8 V** 至 V_{IN} 的可调输出电压
- 固定输出电压版本
- 输出放电功能
- 可调节软启动
- 两级短路保护
- 输出电压跟踪
- 宽输出电容值选择
- 采用 **3mm x 3mm 16** 引脚四方扁平无引线 **(QFN)** 封装

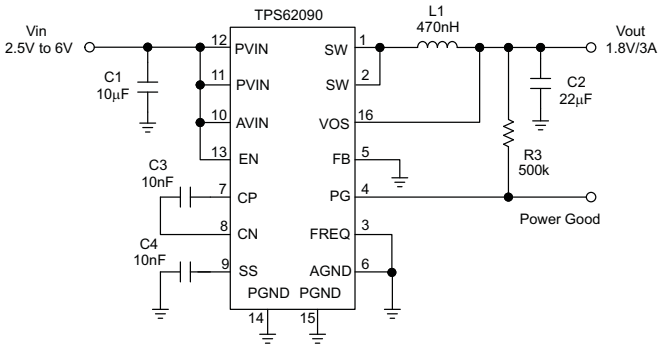
应用

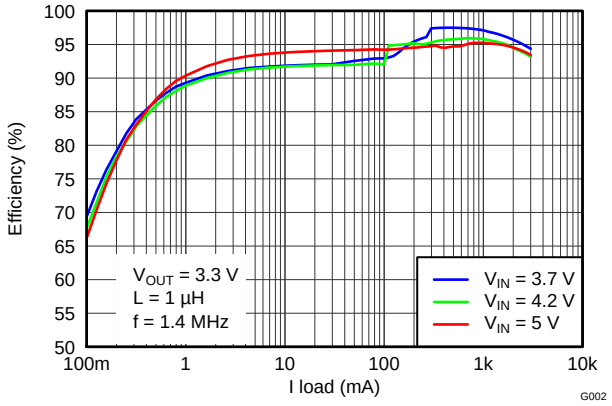
- 分布式电源
- 笔记本、笔记本电脑
- 硬盘驱动器
- 处理器电源
- 电池供电型应用

说明

TPS6209x 器件是一款高效同步降压转换器，此转换器针对小外形尺寸、高效应用进行了优化并适合于电池供电类应用。 为了最大限度地提升效率，此转换器运行在 2.8 MHz/1.4 MHz 的标称开关频率的脉宽调制 (PWM) 模式下并在轻负载时自动进入省电运行模式。 当被用于分布式电源和负载点调制时，此器件允许到其它电源轨的电压跟踪并可耐受范围在 10 µF 到高达 150 µF 甚至更高的输出电容。 通过使用 DCS™ 控制技术，此器件可实现出色的负载静态性能以及精确的输出电压调制。

此输出电压启动斜波由软启动引脚控制，从而使器件可作为独立电源运行或运行在跟踪配置下。 通过配置使能和开漏电源正常引脚也有可能实现电源排序。 在省电模式下，此器件运行在典型值为 20 µA 静态电流下。 在全部负载电流范围内，自动进入省电模式并且无缝保持高效。





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	VOUT	ORDERING	PACKAGE	PACKAGE MARKING
-40°C to 85°C	adjustable	TPS62090	RGT	SBW
	3.3 V	TPS62091	RGT	SBX
	2.5 V	TPS62092	RGT	SBY
	1.8 V	TPS62093	RGT	SBZ

(1) For detailed ordering information please see the PACKAGE OPTION ADDENDUM section at the end of the datasheet.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage range	PVIN, AVIN, FB, SS, EN, FREQ, VOS(2)	–0.3	7	V
	SW, PG	–0.3	V_{IN}+0.3	V
Power Good sink current	PG		1	mA
ESD rating	Human Body Model		2	kV
	Charged Device Model		500	V
Continuous total power dissipation		See the Thermal Table		
Operating junction temperature range, T_J		–40	150	°C
Operating ambient temperature range, T_A		–40	85	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS62090	UNITS
		QFN (16 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	47	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	60	
θ_{JB}	Junction-to-board thermal resistance	20	
ψ_{JT}	Junction-to-top characterization parameter	1.5	
ψ_{JB}	Junction-to-board characterization parameter	20	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	5.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range V_{IN}	2.5		6	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) See the application section for further information

ELECTRICAL CHARACTERISTICS

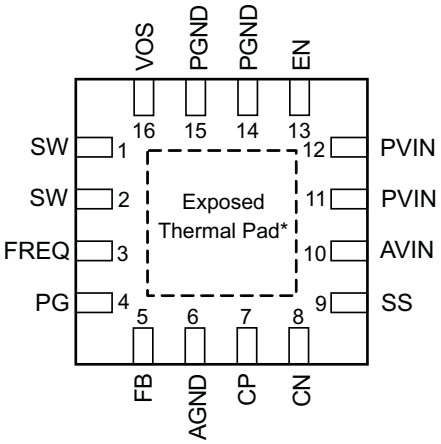
V_{IN} = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		6	V
I_{QIN}	Quiescent current	Not switching, FB = FB +5 %, Into PVIN and AVIN		20		µA
I_{sd}	Shutdown current	Into PVIN and AVIN		0.6	5	µA
UVLO	Undervoltage lockout threshold	V_{IN} falling	2.1	2.2	2.3	V
	Undervoltage lockout hysteresis			200		mV
	Thermal shutdown	Temperature rising		150		ºC
	Thermal shutdown hysteresis			20		ºC
Control SIGNALS EN, FREQ						
V_H	High level input voltage	V_{IN} = 2.5 V to 6 V	1			V
V_L	Low level input voltage	V_{IN} = 2.5 V to 6 V			0.4	V
I_{lkg}	Input leakage current	EN, FREQ = GND or V_{IN}		10	100	nA
R_{PD}	Pull down resistance			400		kΩ
Softstart						
I_{SS}	Softstart current		6.3	7.5	8.7	µA
POWER GOOD						
V_{th}	Power good threshold	Output voltage rising		95%		
		Output voltage falling		90%		
V_L	Low level voltage	$I_{(sink)}$ = 1mA			0.4	V
I_{PG}	PG sinking current				1	mA
I_{lkg}	Leakage current	V_{PG} = 3.6V		10	100	nA
POWER SWITCH						
$R_{DS(on)}$	High side FET on-resistance	I_{SW} = 500 mA		50		mΩ
	Low side FET on-resistance	I_{SW} = 500 mA		40		mΩ
I_{LIM}	High side FET switch current limit		3.7	4.6	5.5	A
f_s	Switching frequency	FREQ = GND, I_{OUT} = 3 A		2.8		MHz
		FREQ = VIN, I_{OUT} = 3 A		1.4		MHz
OUTPUT						
V_s	Output voltage range		0.8		V_{IN}	V
R_{od}	Output discharge resistor	EN = GND, V_{OUT} = 1.8 V		200		Ω
V_{FB}	Feedback regulation voltage			0.8		V
V_{FB}	Feedback voltage accuracy (1) (2)(3)	V_{IN} ≥ V_{OUT} + 1 V, TPS62090 adjustable output version				
		I_{OUT} = 1 A, PWM mode	-1.4%		+1.4%	
		I_{OUT} = 0 mA, FREQ = 2.8 MHz, V_{OUT} ≥ 0.8 V, PFM mode	-1.4%		+3%	
		I_{OUT} = 0 mA, FREQ = 1.4 MHz, V_{OUT} ≥ 1.2 V, PFM mode	-1.4%		+3%	
		I_{OUT} = 0 mA, FREQ = 1.4 MHz, V_{OUT} < 1.2V, PFM mode	-1.4%		+3.7%	
I_{FB}	Feedback input bias current	V_{FB} = 0.8V, TPS62090 adjustable output version		10	100	nA
V_{OUT}	Output voltage accuracy (2)(3)	V_{IN} ≥ V_{OUT} + 1 V, Fixed output voltage				
		I_{OUT} = 1 A, PWM mode	-1.4%		+1.4%	
		$_{OUT}$ = 0 mA, FREQ = High and Low, PFM mode	-1.4%		+2.5%	
	Line regulation	V_{OUT} = 1.8 V, PWM operation		0.016		%/V
	Load regulation	V_{OUT} = 1.8 V, PWM operation		0.04		%/A

(1) For output voltages < 1.2 V, use a 2 x 22 µF output capacitance to achieve +3% output voltage accuracy.
(2) Conditions: f = 2.8 MHz, L = 0.47 µH, C_{OUT} = 22 µF or f = 1.4 MHz, L = 1 µH, C_{OUT} = 22 µF.
(3) For more information, see the Power Save Mode Operation section of this data sheet.

DEVICE INFORMATION

16 PIN 3x3mm QFN
TOP VIEW

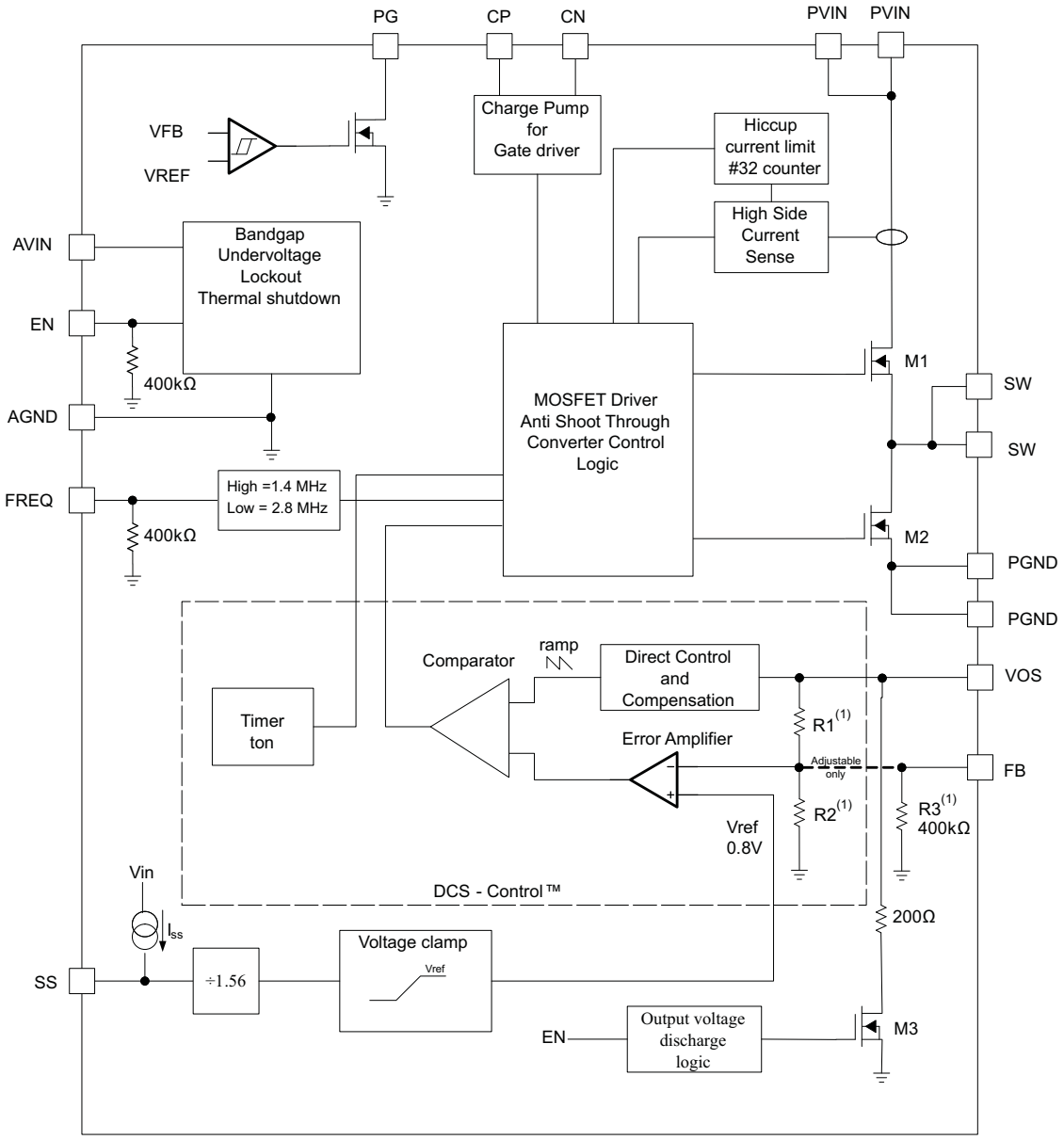


NOTE: *The exposed Thermal Pad is connected to AGND.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
SW	1, 2	I	Switch pin of the power stage.
FREQ	3	I	This pin selects the switching frequency of the device. FREQ=low sets the typical switching frequency to 2.8 MHz. FREQ=high sets the typical switching frequency to 1.4 MHz. This pin has an active pull down resistor of typically 400 kΩ and can be left floating for 2.8 MHz operation.
PG	4	O	Power good open drain output. This pin is high impedance if the output voltage is within regulation. This pin is pulled low if the output is below its nominal value. The pull up resistor can not be connected to any voltage higher than the input voltage of the device.
FB	5		Feedback pin of the device. For the fixed output voltage versions this pin needs to be connected to GND for improved thermal performance. If, desired then this pin can also be left floating since it is internally connected with 400 kΩ to GND for fixed output voltage versions.
AGND	6		Analog ground.
CP	7		Internal charge pump flying capacitor. Connect a 10 nF capacitor between CP and CN.
CN	8		Internal charge pump flying capacitor. Connect a 10 nF capacitor between CP and CN.
SS	9	I	Soft-start control pin. A capacitor is connected to this pin and sets the softstart time. Leaving this pin floating sets the minimum start-up time.
AVIN	10		Bias supply input voltage pin.
PVIN	11,12		Power supply input voltage pin.
EN	13		Device enable. To enable the device this pin needs to be pulled high. Pulling this pin low disables the device. This pin has an active pull down resistor of typically 400 kΩ.
PGND	14,15		Power ground connection.
VOS	16		Output voltage sense pin. This pin needs to be connected to the output voltage.
Thermal Pad			The exposed thermal pad is connected to AGND.

FUNCTIONAL BLOCK DIAGRAM



(1) R1, R2, R3 are implemented in the fixed output voltage version only.

Table 1. List of components

REFERENCE	DESCRIPTION	MANUFACTURER
TPS62090	High efficient step down converter	Texas Instruments
L1	Inductor: 1uH, 0.47uH, 0.4uH	Coilcraft XFL4020-102, XAL4020-401, TOKO DEF252012-R47
C1	Ceramic capacitor: 10uF, 22uF	(6.3V, X5R, 0603), (6.3V, X5R, 0805)
C2	Ceramic capacitor: 22uF	(6.3V, X5R, 0805)
C3, C4	Ceramic capacitor	Standard
R1, R2, R3	Resistor	Standard

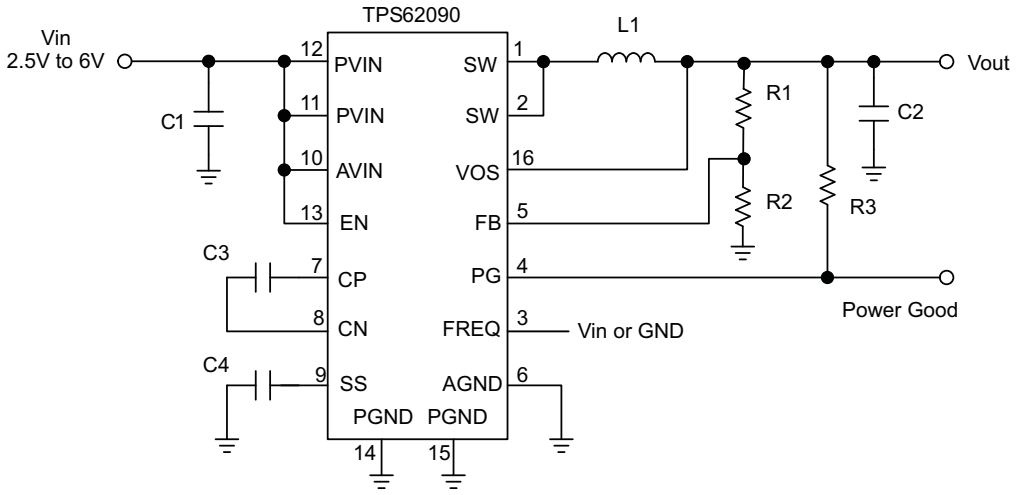


Figure 1. Parametric Measurement Circuit

TYPICAL CHARACTERISTICS

		FIGURE
Efficiency	vs load current (V_O = 3.3 V, f = 1.4 MHz, f = 2.8 MHz)	Figure 2, Figure 3
Efficiency	vs load current (V_O = 1.8 V, f = 1.4 MHz, f = 2.8 MHz)	Figure 4, Figure 5
Efficiency	vs load current (V_O = 1.05 V, f = 1.4 MHz, f = 2.8 MHz)	Figure 6, Figure 7
Output voltage	vs load current (V_O = 1.8 V, f = 1.4 MHz, f = 2.8 MHz)	Figure 8, Figure 9
High Side FET on-resistance	vs input voltage	Figure 10
Switching frequency	vs load current (V_O = 1. 8 V, f = 1.4 MHz)	Figure 11
Switching frequency	vs input voltage (V_O = 1.8 V, f = 1.4 MHz)	Figure 12
Switching frequency	vs load current (V_O = 1. 8 V, f = 2.8 MHz)	Figure 13
Switching frequency	vs input voltage (V_O = 1.8 V, f = 2.8 MHz)	Figure 14
Quiescent current	vs input voltage (V_O = 1.8 V, f = 1.4 MHz)	Figure 15
PWM operation	V_O = 1.8 V, f = 1.4 MHz	Figure 16
PFM operation	V_O = 1.8 V, f = 1.4 MHz	Figure 17
PFM operation	V_O = 1.8 V, f = 2.8 MHz	Figure 18
Load sweep	V_O = 1.8 V, f = 1.4 MHz	Figure 19
Load sweep	V_O = 1.8 V, f = 2.8 MHz	Figure 20
Start-up	V_O = 1.8 V, f = 2.8 MHz, C_{SS} = 10 nF	Figure 21
Shutdown	V_O = 1.8 V, f = 2.8 MHz	Figure 22
Hiccup short circuit protection	V_O = 1.8 V, f = 1.4 MHz	Figure 23
Hiccup Short circuit protection	V_O = 1.8 V, f = 1.4 MHz, recovery after short circuit	Figure 24
Load transient response	V_O = 1.8 V, f = 1.4 MHz, 300 mA to 2.5 A	Figure 25
Load transient response	V_O = 1.8 V, f = 1.4 MHz, 300 mA to 2.5 A	Figure 26
Load transient response	V_O = 1.8 V, f = 1.4 MHz, 20 mA to 1 A	Figure 27

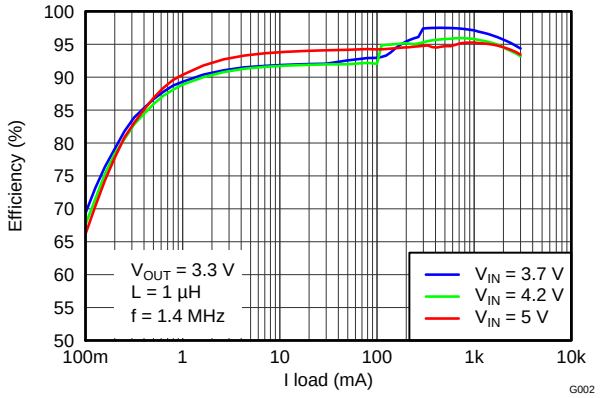


Figure 2. Efficiency vs Load Current

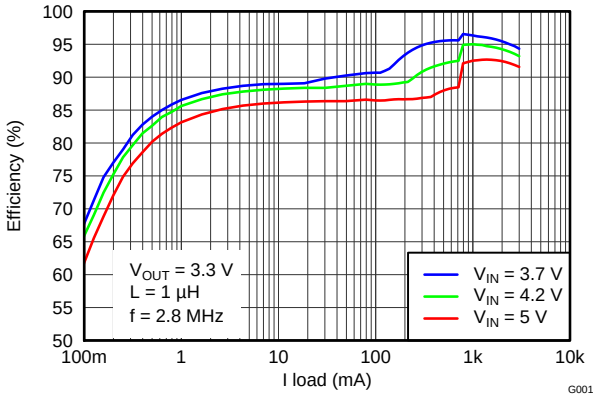


Figure 3. Efficiency vs Load Current

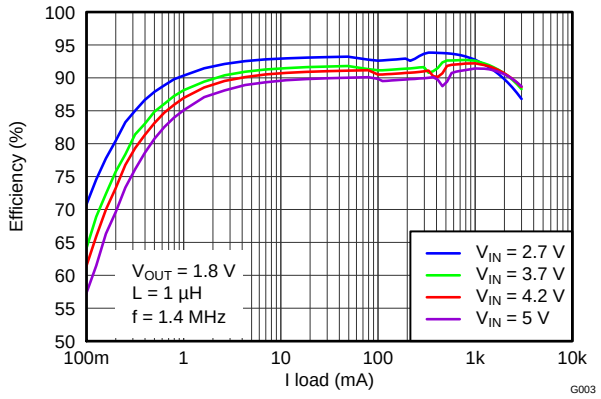


Figure 4. Efficiency vs Load Current

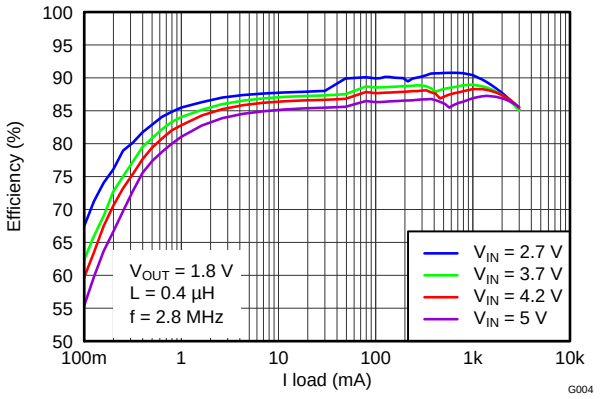


Figure 5. Efficiency vs Load Current

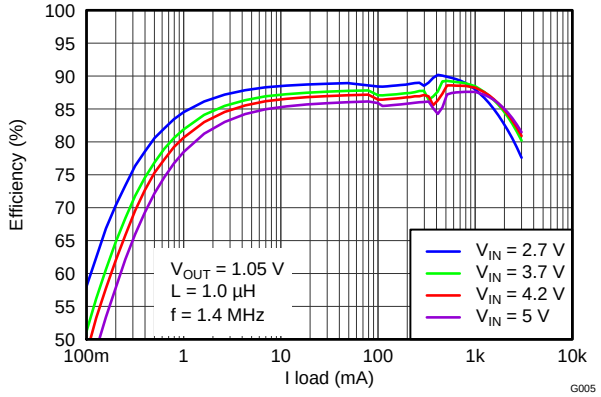


Figure 6. Efficiency vs Load Current

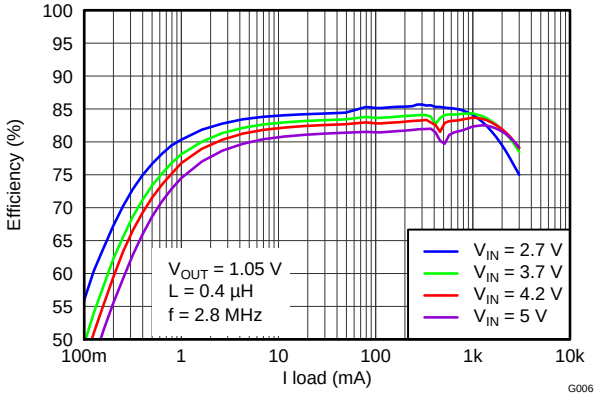


Figure 7. Efficiency vs Load Current

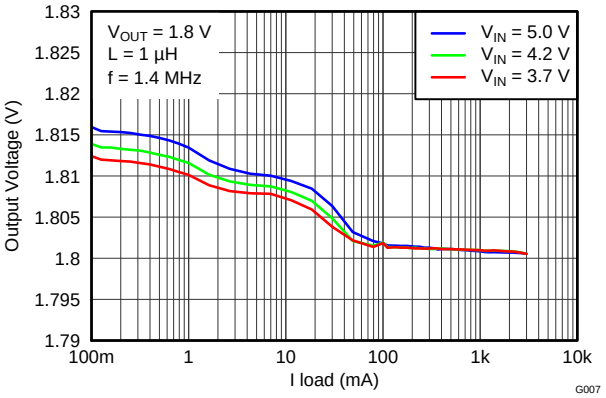


Figure 8. Output Voltage vs Load Current

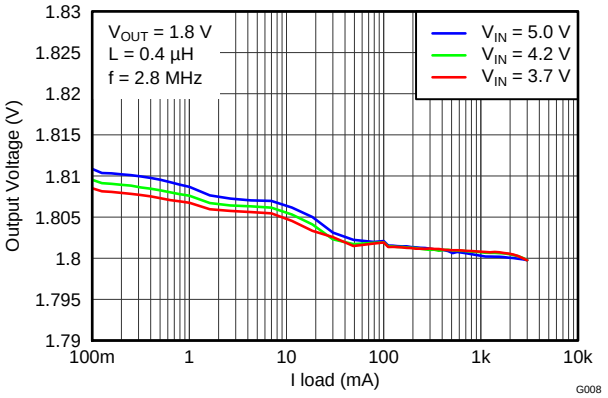


Figure 9. Output Voltage vs Load Current

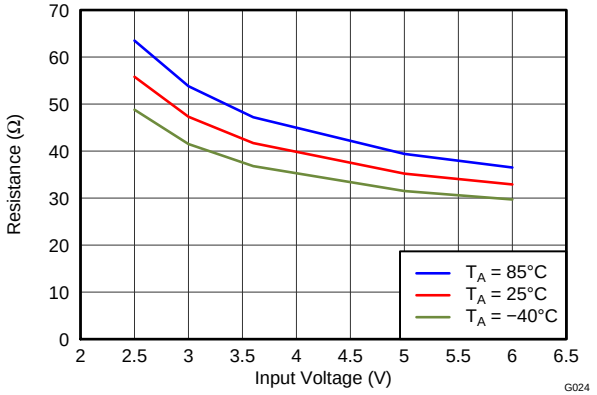


Figure 10. High Side FET On-Resistance vs Input Voltage

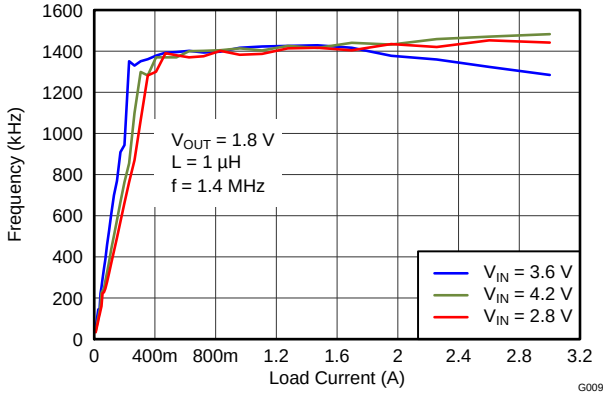


Figure 11. Switching Frequency vs Load Current

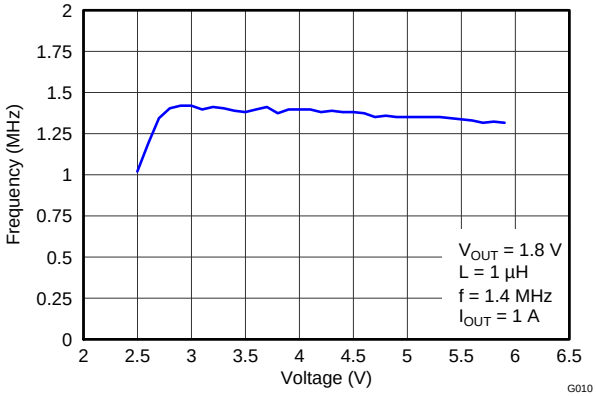


Figure 12. Switching Frequency vs Input Voltage

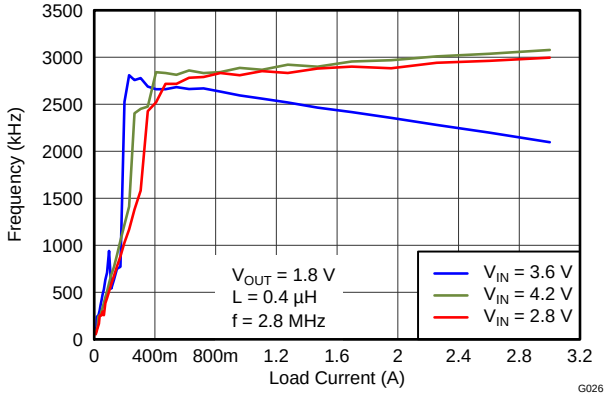


Figure 13. Frequency vs Load Current

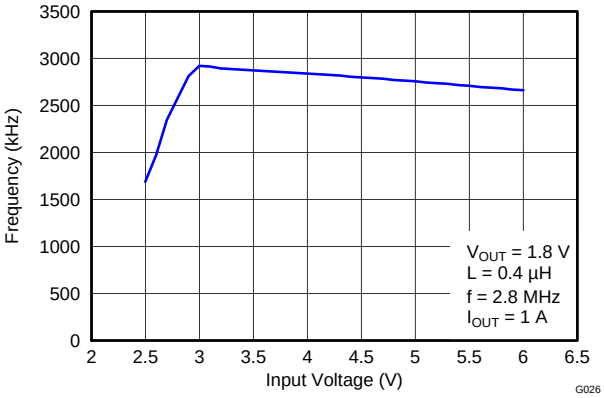


Figure 14. Frequency vs Input Voltage

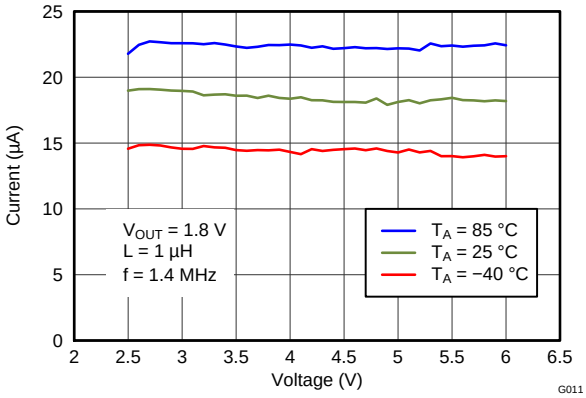


Figure 15. Quiescent Current vs Input Voltage

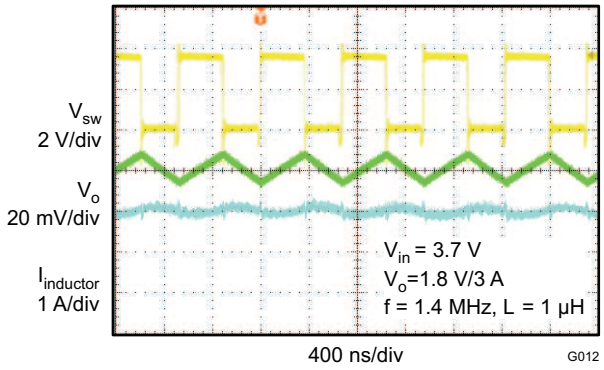


Figure 16. PWM Operation

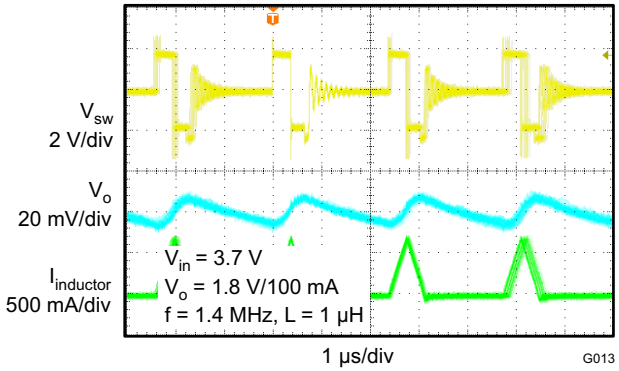


Figure 17. PFM Operation

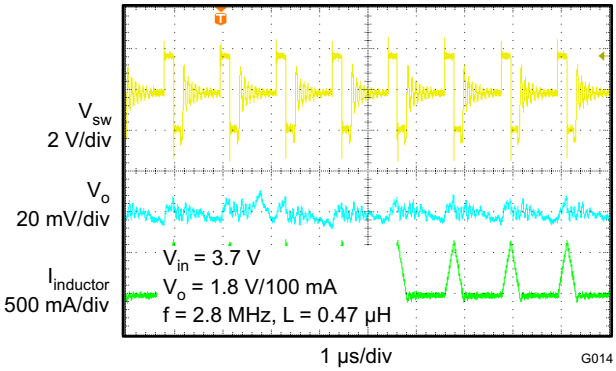


Figure 18. PFM Operation

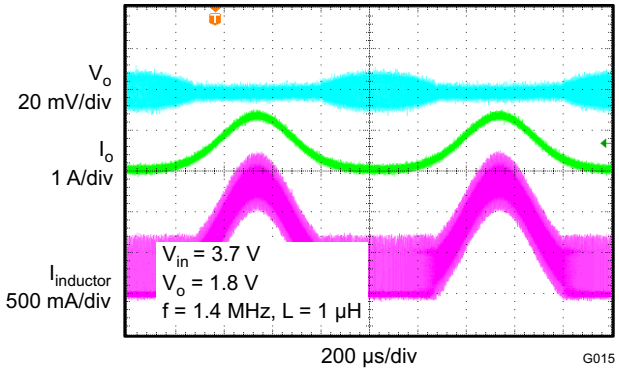


Figure 19. Load Sweep

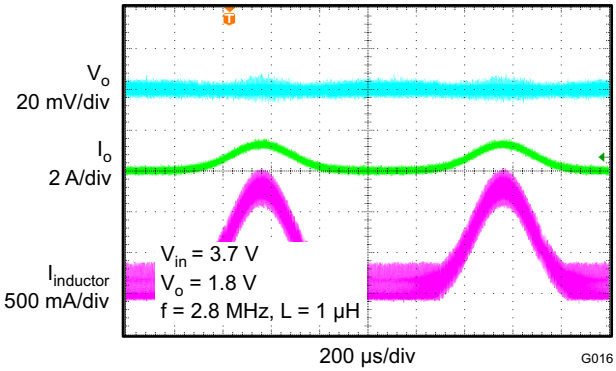


Figure 20. Load Sweep

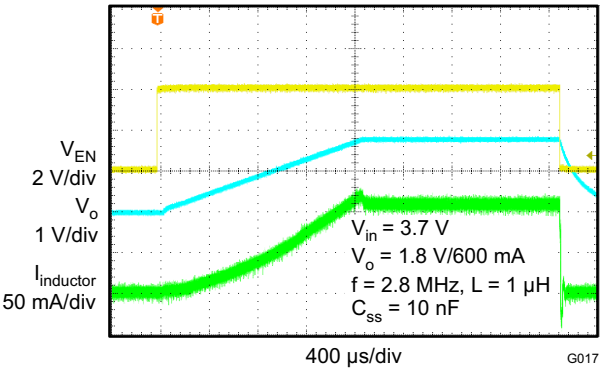


Figure 21. Start-Up

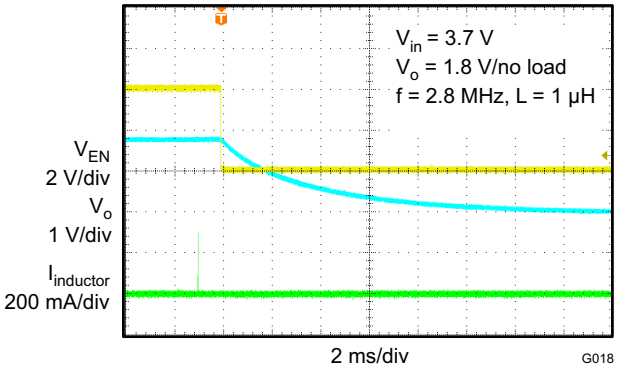


Figure 22. Shutdown

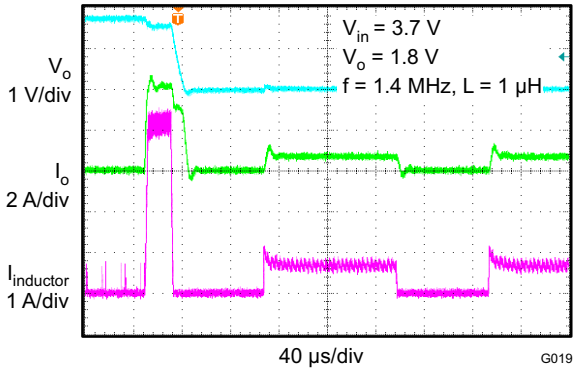


Figure 23. Hiccup Short Circuit Protection

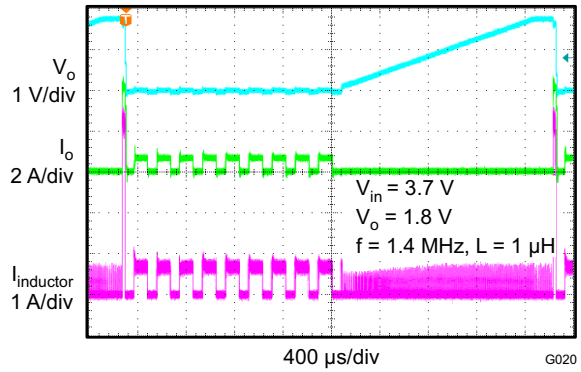


Figure 24. Hiccup Short Circuit Protection

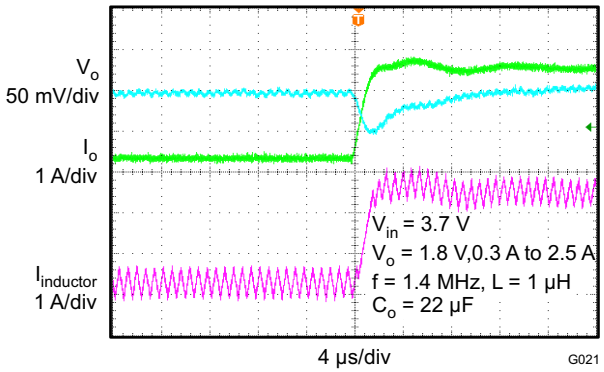


Figure 25. Load Transient Response

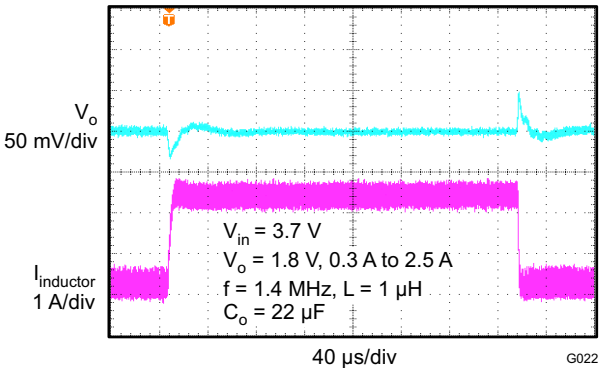


Figure 26. Load Transient Response

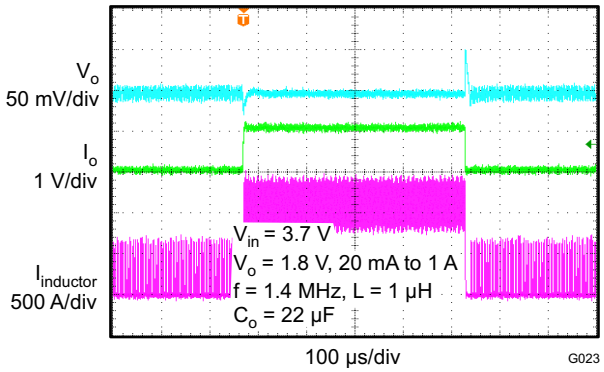


Figure 27. Load Transient Response

DETAILED DESCRIPTION

Operation

The TPS6209x synchronous switched mode converters are based on DCS™ Control (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS™ Control topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM, the converter operates with its nominal switching frequency of 2.8 MHz/1.4 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. DCS™ Control supports both operation modes (PWM and PFM) using a single building block having a seamless transition from PWM to Power Save Mode without effects on the output voltage. Fixed output voltage versions provide smallest solution size combined with lowest quiescent current. The TPS6209x family offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

PWM Operation

At medium to heavy load currents, the device operates with pulse width modulation (PWM) at a nominal switching frequency of 2.8 MHz or 1.4 MHz depending on the setting of the FREQ pin. As the load current decreases, the converter enters the Power Save Mode operation reducing its switching frequency. The device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM).

Power Save Mode Operation

As the load current decreases, the converter enters Power Save Mode operation. During Power Save Mode the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current while maintaining high efficiency. The Power Save Mode is based on a fixed on-time architecture following Equation 1. When operating at 1.4 MHz the on-time is twice as long as the on-time for 2.8 MHz operation. This results in larger output voltage ripple, as shown in Figure 17 and Figure 18, and slightly higher output voltage at no load, as shown in Figure 8 and Figure 9. To have the same output voltage ripple at 1.4 MHz during PFM mode, either the output capacitor or the inductor value needs to be increased. As an example, operating at 2.8 MHz using 0.47 µH inductor gives the same output voltage ripple as operating with 1.4 MHz using 1 µH inductor.

$$ton_{2.8MHz} = \frac{V_{OUT}}{V_{IN}} \times 360ns$$

$$ton_{1.4MHz} = \frac{V_{OUT}}{V_{IN}} \times 360ns \times 2$$

$$f = \frac{2 \times I_{OUT}}{ton^2 \left(1 + \frac{V_{IN} - V_{OUT}}{V_{OUT}} \right) \times \frac{V_{IN} - V_{OUT}}{L}} \quad (1)$$

In Power Save Mode the output voltage rises slightly above the nominal output voltage in PWM mode, as shown in Figure 8 and Figure 9. This effect can be reduced by increasing the output capacitance or the inductor value. This effect can also be reduced by programming the output voltage of the TPS62090 lower than the target value. As an example, if the target output voltage is 3.3 V, then the TPS62090 can be programmed to 3.3V - 0.8%. As a result the output voltage accuracy is now -2.2% to +2.2% instead of -1.4% to 3%. The output voltage accuracy in PFM operation is reflected in the electrical specification table and given for a 22 µF output capacitance.

Low Dropout Operation (100% Duty Cycle)

The device offers low input to output voltage difference by entering 100% duty cycle mode. In this mode the high side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage where the output voltage falls below its nominal regulation value is given by:

$$V_{IN(min)} = V_{OUT(max)} + I_{OUT} \times (R_{DS(on)} + R_L) \quad (2)$$

Where

$R_{DS(on)}$ = High side FET on-resistance

R_L = DC resistance of the inductor

$V_{OUT(max)}$ = nominal output voltage plus maximum output voltage tolerance

Softstart (SS)

To minimize inrush current during start up, the device has an adjustable softstart depending on the capacitor value connected to the SS pin. The device charges the softstart capacitor with a constant current of typically 7.5 µA. The feedback voltage follows this voltage with a fraction of 1.56 until the internal reference voltage of 0.8 V is reached. The softstart operation is completed once the voltage at the softstart capacitor has reached typically 1.25 V. The soft-start time can be calculated using Equation 3. The larger the softstart capacitor the longer the softstart time. The relation between softstart voltage and feedback voltage can be estimated using Equation 4.

$$t_{SS} = C_{SS} \times \frac{1.25V}{7.5\mu A} \quad (3)$$

$$V_{FB} = \frac{V_{SS}}{1.56} \quad (4)$$

This is also the case for the fixed output voltage option having the internal regulation voltage. Leaving the softstart pin floating sets the minimum start-up time.

Start-up Tracking (SS)

The softstart pin can also be used to implement output voltage tracking with other supply rails. The internal reference voltage follows the voltage at the softstart pin with a fraction of 1.56 until the internal reference voltage of 0.8 V is reached. The softstart pin can be used to implement output voltage tracking as shown in Figure 28.

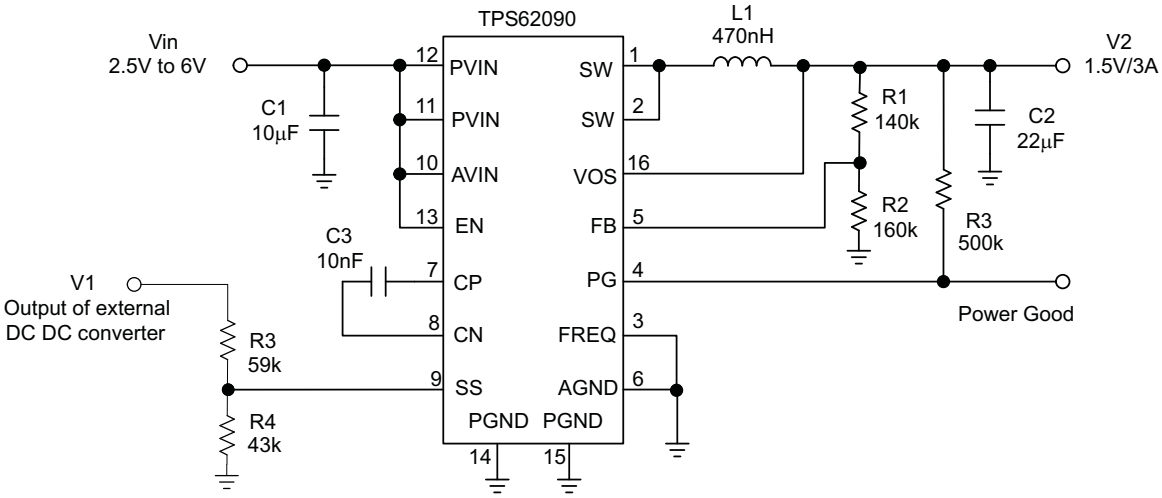


Figure 28. Output Voltage Tracking

In Figure 28, the output V2 will track the voltage applied to V1. The voltage will track simultaneously when following conditions are met:

$$\frac{R3}{R4} = \frac{R1}{R2} \times 1.56 \tag{5}$$

As the fraction of R3/R4 becomes larger the voltage V1 will ramp up faster than V2 and if it gets smaller than the ramp will be slower than V2. R4 needs to be determined first using Equation 6.

$$R4 = \frac{1.25V}{300\mu A} \tag{6}$$

In the calculation of R4, 300 µA current is used to achieve sufficient accuracy by taking into account the typical 7.5 µA soft-start current. After determining R4, R3 can be calculated using Equation 5.

Short Circuit Protection (Hiccup-Mode)

The device is protected against hard short circuits to GND and over-current events. This is implemented by a two level short circuit protection. During start-up and when the output is shorted to GND the switch current limit is reduced to 1/3 of its typical current limit of 4.6 A. Once the output voltage exceeds typically 0.6 V the current limit is released to its nominal value. The full current limit is implemented as a hiccup current limit. Once the internal current limits is triggered 32 times the device stops switching and starts a new start-up sequence after a typical delay time of 66 µS passed by. The device will go through these cycles until the high current condition is released.

Output Discharge Function

To make sure the device starts up under defined conditions, the output gets discharged via the VOS pin with a typical discharge resistor of 200 Ω whenever the device shuts down. This happens when the device is disabled or if thermal shutdown, undervoltage lockout or short circuit hiccup-mode is triggered.

Power Good Output (PG)

The power good output is low when the output voltage is below its nominal value. The power good will become high impedance once the output is within 5% of regulation. The PG pin is an open drain output and is specified to typically sink up to 1 mA. This output requires a pull-up resistor to be monitored properly. The pull-up resistor cannot be connected to any voltage higher than the input voltage of the device.

Frequency Set Pin (FREQ)

The FREQ pin is a digital logic input which sets the nominal switching frequency. Pulling this pin to GND sets the nominal switching frequency to 2.8 MHz and pulling this pin high sets the nominal switching frequency to 1.4 MHz. Since this pin changes the switching frequency it also changes the on-time during PFM mode. At 1.4 MHz the on-time is twice the on-time as operating at 2.8 MHz. This pin has an active pull-down resistor of typically 400 kΩ. For applications where efficiency is of highest importance, a lower switching frequency should be selected. A higher switching frequency allows the use of smaller external components, faster load transient response and lower output voltage ripple when using same L-C values.

Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. UVLO shuts down the device at input voltages lower than typically 2.2 V with a 200 mV hysteresis.

Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically 150°C with a 20°C hysteresis.

APPLICATION INFORMATION

DESIGN PROCEDURE

The first step is the selection of the output filter components. To simplify this process, Table 2 and Table 3 outline possible inductor and capacitor value combinations.

Table 2. Output Filter Selection (2.8 MHz Operation, FREQ = GND)

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)				
	10	22	47	100	150
0.47		√(3)	√	√	√
1.0	√	√	√	√	√
2.2					
3.3					

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and -50%.
(3) Typical application configuration. Other check mark indicates alternative filter combinations

Table 3. Output Filter Selection (1.4 MHz Operation, FREQ = V_{IN})

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)				
	10	22	47	100	150
0.47		√	√	√	√
1.0	√	√(3)	√	√	√
2.2	√	√	√	√	√
3.3					

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%.
(3) Typical application configuration. Other check mark indicates alternative filter combinations

Inductor Selection

The inductor selection is affected by several parameter like inductor ripple current, output voltage ripple, transition point into Power Save Mode, and efficiency. See Table 4 for typical inductors.

Table 4. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat/DCR
0.6 µH	Coilcraft XAL4012-601	4 x 4 x 2.1	7.1A/9.5 mΩ
1 µH	Coilcraft XAL4020-102	4 x 4 x 2.1	5.9A/13.2 mΩ
1 µH	Coilcraft XFL4020-102	4 x 4 x 2.1	5.1 A/10.8 mΩ
0.47 µH	TOKO DFE252012 R47	2.5 x 2 x 1.2	3.7A/39 mΩ
1 µH	TOKO DFE252012 1R0	2.5 x 2 x 1.2	3.0A/59 mΩ
0.68 µH	TOKO DFE322512 R68	3.2 x 2.5 x 1.2	3.5A/37 mΩ
1 µH	TOKO DFE322512 1R0	3.2 x 2.5 x 1.2	3.1A/45 mΩ

In addition, the inductor has to be rated for the appropriate saturation current and DC resistance (DCR). The inductor needs to be rated for a saturation current as high as the typical switch current limit, of 4.6 A or according to Equation 7 and Equation 8. Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions. The formula takes the converter efficiency into account. The converter efficiency can be taken from the data sheet graph`s or 80% can be used as a conservative approach. The calculation must be done for the maximum input voltage where the peak switch current is highest.

$$I_L = I_{OUT} + \frac{\Delta I_L}{2} \tag{7}$$

$$I_L = I_{OUT} + \frac{\frac{V_{OUT}}{\eta} \times \left(1 - \frac{V_{OUT}}{V_{IN} \times \eta}\right)}{2 \times f \times L} \tag{8}$$

where

f = Converter switching frequency (typical 2.8 MHz or 1.4 MHz)
L = Selected inductor value
η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as an conservative assumption)
Note: The calculation must be done for the maximum input voltage of the application

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current. A margin of 20% needs to be added to cover for load transients during operation.

Input and Output Capacitor Selection

For best output and input voltage filtering, low ESR ceramic capacitors are recommended. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 22 µF or larger input capacitor is recommended for 1.4 MHz operation frequency. For 2.8 MHz operation frequence a 10 µF input capacitor or larger is recommended. The output capacitor value can range from 10 µF up to 150 µF and beyond. The recommended typical output capacitor value is 22 µF and can vary over a wide range as outline in the output filter selection table.

Table 5. Input Capacitor Selection

INPUT CAPACITOR	COMMENT
10 µF	FREQ=low, f=2.8 MHz
22 µF	FREQ=high, f=1.4 MHz

Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equations:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \quad (9)$$

$$R2 = \frac{V_{FB}}{I_{FB}} = \frac{0.8\ V}{5\ \mu A} \approx 160\ k\Omega \quad (10)$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.8V} - 1\right) \quad (11)$$

When sizing R2, in order to achieve low quiescent current and acceptable noise sensitivity, use a minimum of 5 µA for the feedback current I_{FB}. Larger currents through R2 improve noise sensitivity and output voltage accuracy. Lowest quiescent current and best output voltage accuracy can be achieved with the fixed output voltage versions. For the fixed output voltage versions, the FB pin can be left floating or connected to GND to improve the thermal package performance.

Layout Guideline

It is recommended to place all components as close as possible to the IC. The VOS connection is noise sensitive and needs to be routed as short and directly to the output terminal of the inductor. The exposed thermal pad of the package, analog ground (pin 6) and power ground (pin 14, 15) should have a single joint connection at the exposed thermal pad of the package. This minimizes switch node jitter. The charge pump capacitor connected to CP and CN should be placed close to the IC to minimize coupling of switching waveforms into other traces and circuits. Refer to the evaluation module User Guide (SLVU670) for an example of component placement, routing and thermal design.

TYPICAL APPLICATIONS

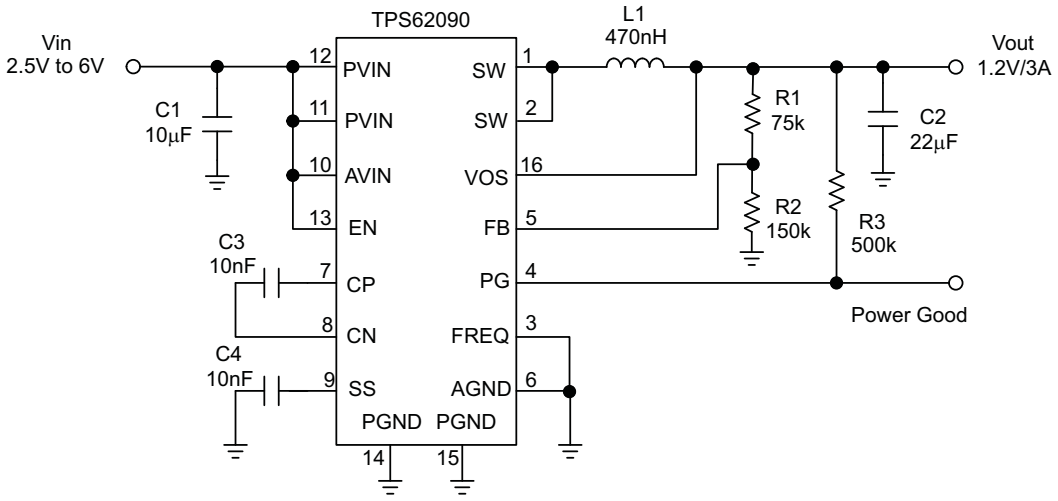


Figure 29. 1.2 V Adjustable Version Operating at 2.8 MHz

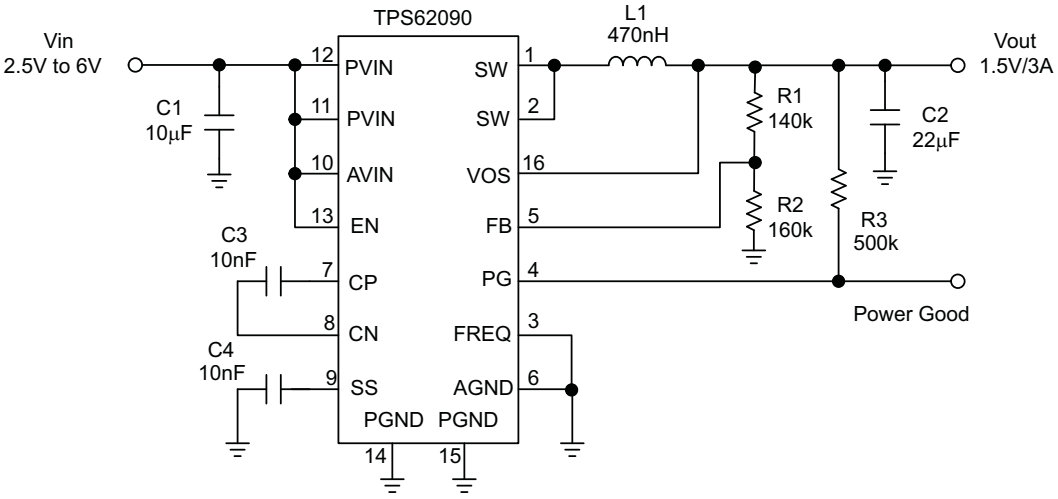


Figure 30. 1.5 V Adjustable Version Operating at 2.8 MHz

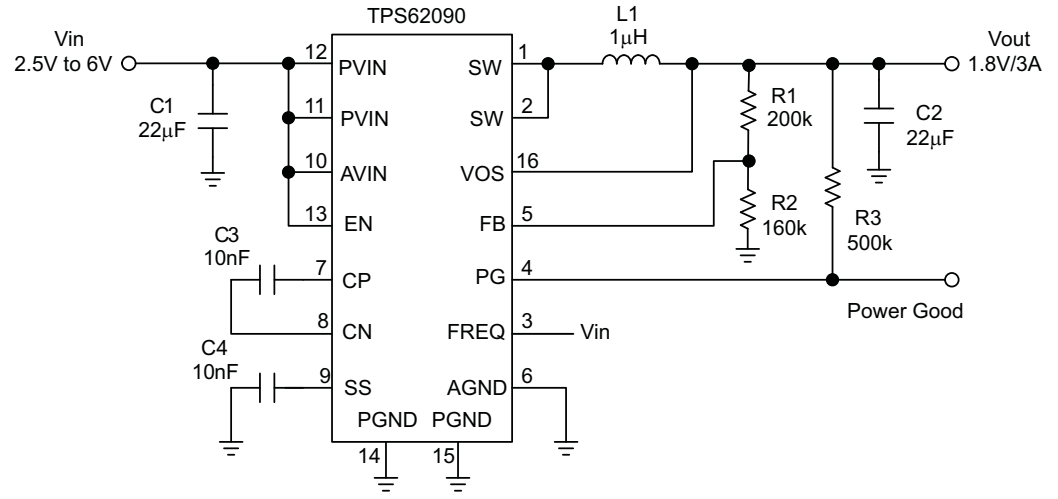


Figure 31. 1.8 V Adjustable Version Operating at 1.4 MHz

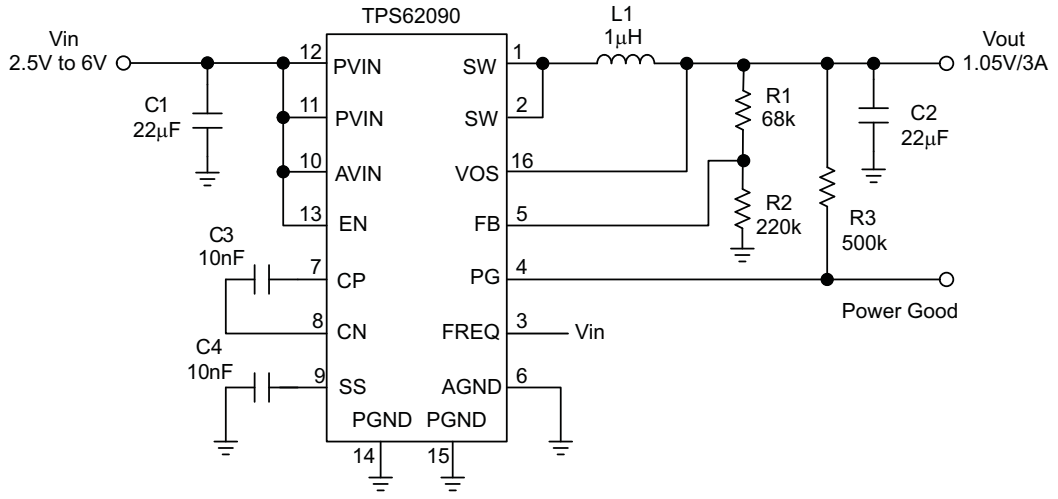


Figure 32. 1.05 V Adjustable Version Operating at 1.4 MHz

REVISION HISTORY

Changes from Original (March 2012) to Revision A	Page
• Changed the FUNCTIONAL BLOCK DIAGRAM	5
• Changed R1, R2 and R4 values in Figure 28	13
• Changed R1 and R2 values in Figure 29	16

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62090RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBW
TPS62090RGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBW
TPS62090RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBW
TPS62090RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBW
TPS62090RGTT.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBW
TPS62090RGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBW
TPS62090RGTTG4	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBW
TPS62090RGTTG4.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBW
TPS62090RGTTG4.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBW
TPS62091RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBX
TPS62091RGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBX
TPS62091RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBX
TPS62091RGTRG4	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBX
TPS62091RGTRG4.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBX
TPS62091RGTRG4.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBX
TPS62091RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBX
TPS62091RGTT.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBX
TPS62091RGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBX
TPS62092RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBY
TPS62092RGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBY
TPS62092RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBY
TPS62092RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBY
TPS62092RGTT.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBY
TPS62092RGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBY
TPS62093RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBZ
TPS62093RGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBZ
TPS62093RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBZ
TPS62093RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBZ
TPS62093RGTT.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBZ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62093RGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBZ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS62090 :

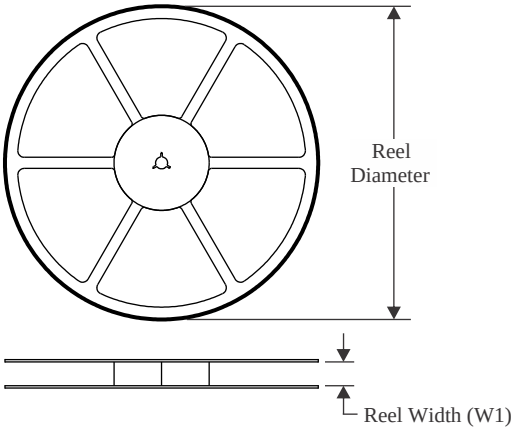
- Automotive : TPS62090-Q1

NOTE: Qualified Version Definitions:

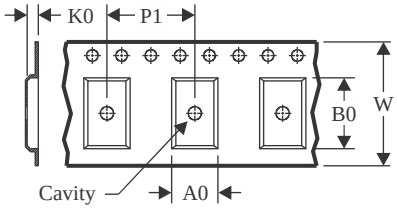
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

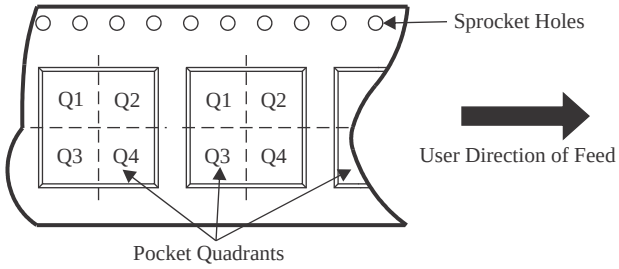


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

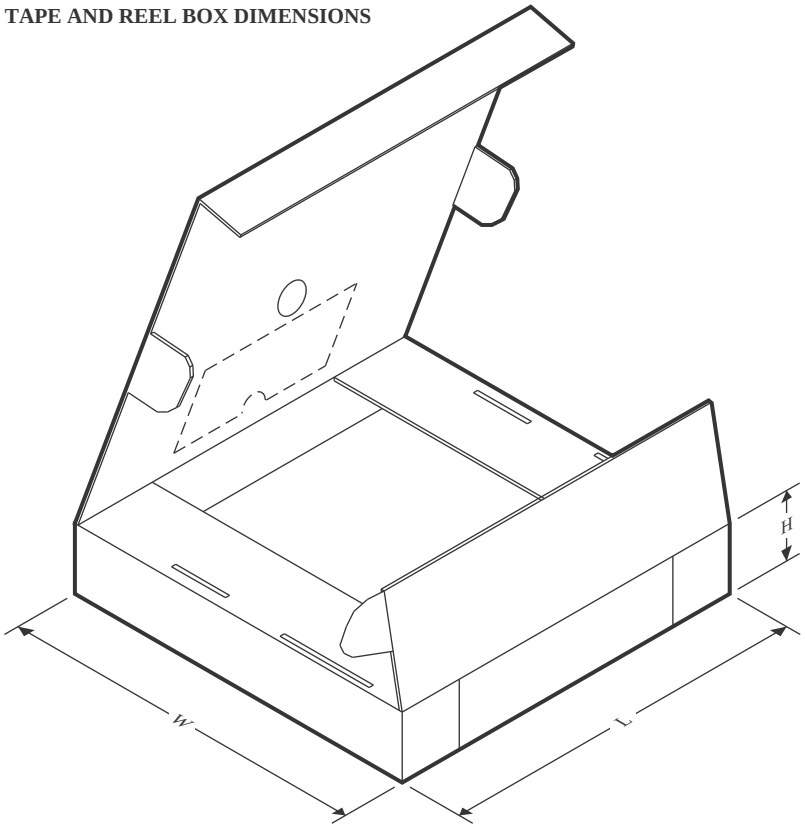


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62090RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62090RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62090RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62090RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62090RGTTG4	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62091RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62091RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62091RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62091RGTRG4	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62091RGTT	VQFN	RGT	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS62091RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62091RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62092RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62092RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62092RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62092RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62092RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62092RGTT	VQFN	RGT	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS62093RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62093RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62093RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62093RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62093RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62093RGTT	VQFN	RGT	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



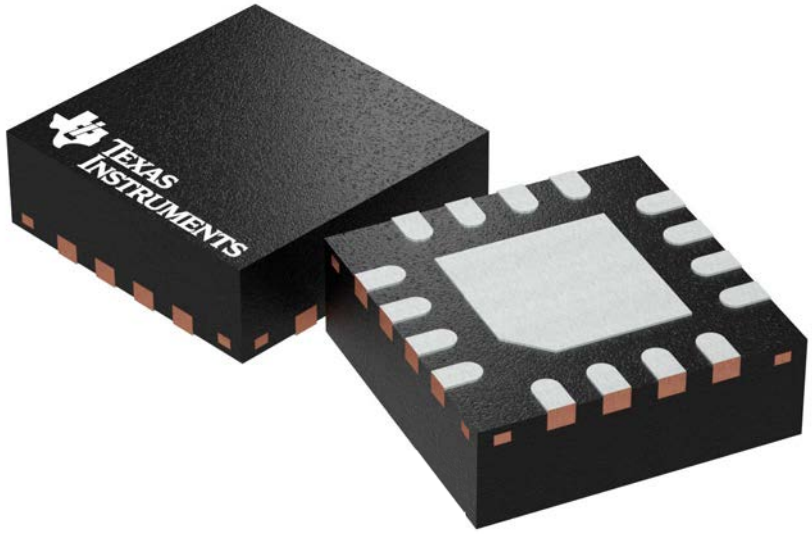
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62090RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
TPS62090RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62090RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62090RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62090RGTTG4	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62091RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
TPS62091RGTR	VQFN	RGT	16	3000	338.0	355.0	50.0
TPS62091RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62091RGTRG4	VQFN	RGT	16	3000	338.0	355.0	50.0
TPS62091RGTT	VQFN	RGT	16	250	338.0	355.0	50.0
TPS62091RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62091RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62092RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
TPS62092RGTR	VQFN	RGT	16	3000	338.0	355.0	50.0
TPS62092RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62092RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62092RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62092RGTT	VQFN	RGT	16	250	338.0	355.0	50.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62093RGTR	VQFN	RGT	16	3000	338.0	355.0	50.0
TPS62093RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
TPS62093RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62093RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62093RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62093RGTT	VQFN	RGT	16	250	338.0	355.0	50.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



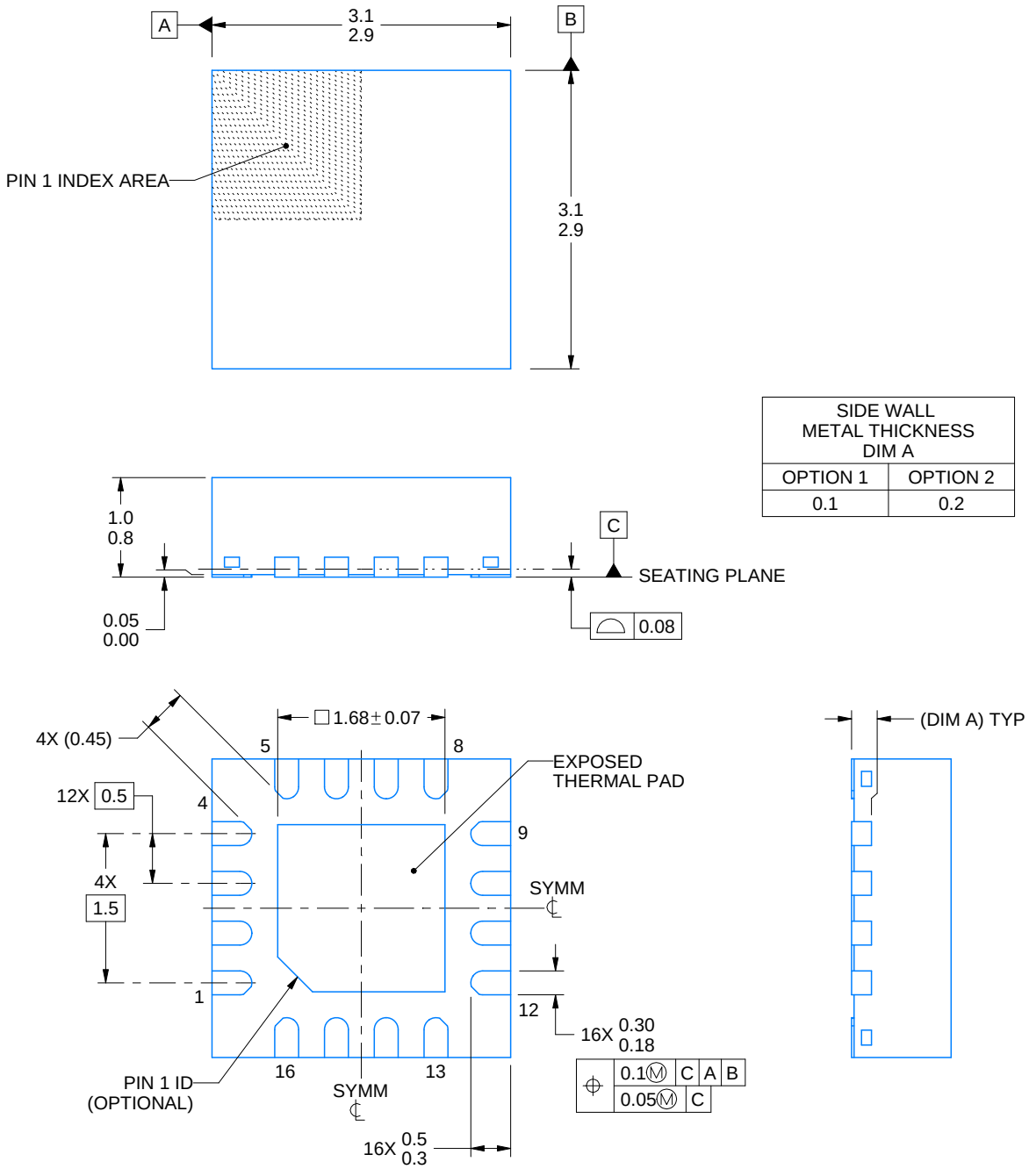
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

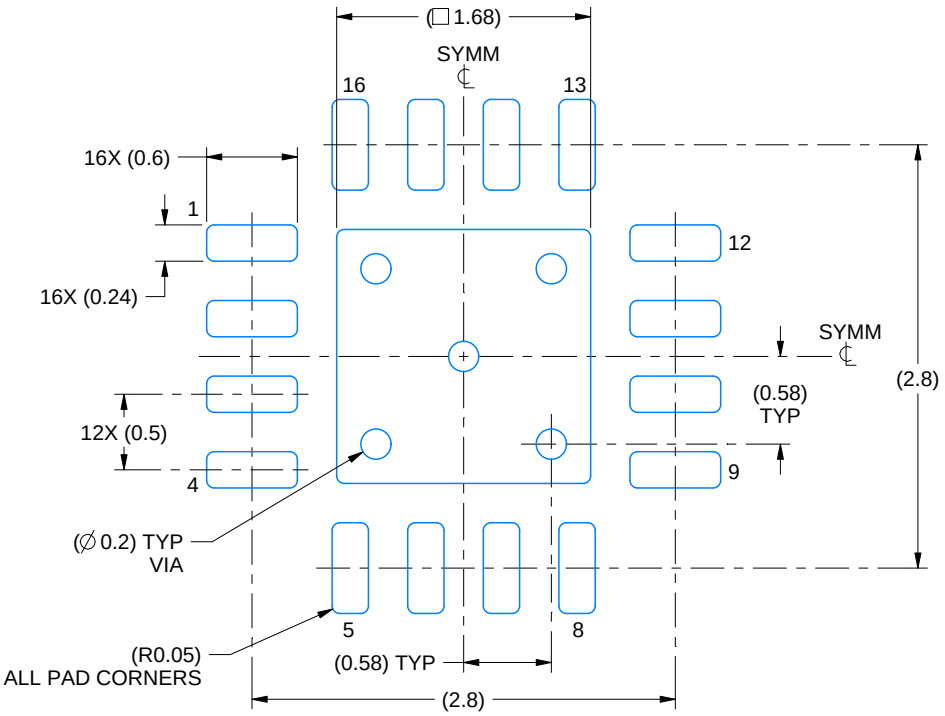
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

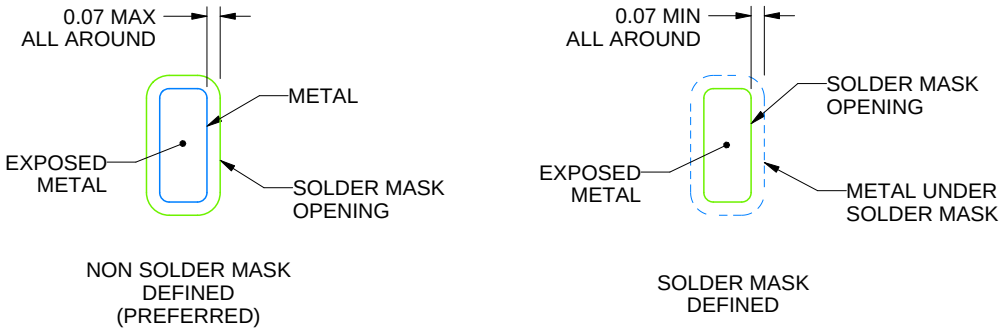


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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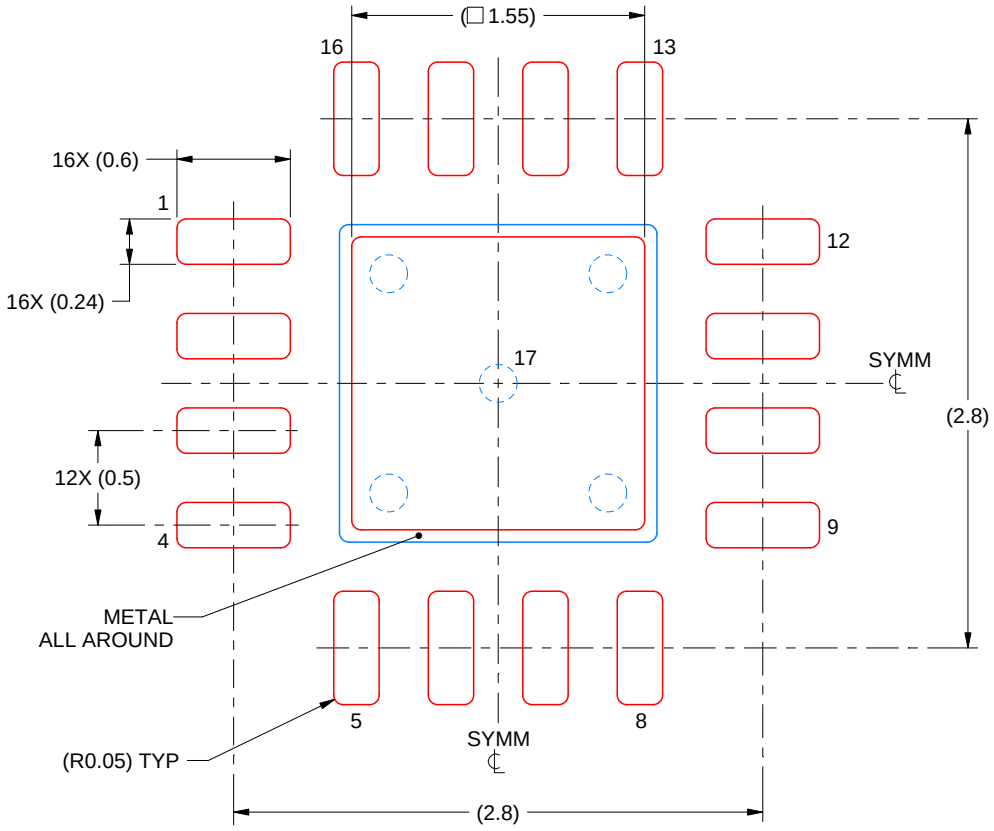
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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