TPS6208x 具有 DCS-Control™ 和贪睡模式的 1.2A、高效降压转换器

1 特性

- DCS-Control™架构，用于快速瞬态稳压
- 贪睡模式下的超低静态电流为 6.5µA
- 输入电压范围：2.3V 至 6V
- 可实现最低压降的 100% 占空比
- 在轻负载条件下实现高效率的省电模式
- 输出放电功能
- 短路保护功能
- 电源正常输出
- 热关断
- 采用 2mm x 2mm、8 引脚晶圆级小外形无引线 (WSON) 封装

2 应用范围

- 电池供电类便携式器件
- 负载点稳压器
- 系统电源轨电压转换

3 说明

TPS6208x 器件是高频同步降压转换器系列产品。该器件的输入电压范围为 2.3V 至 6V，支持常用电池技术。此外，该器件可用于低电压系统电源轨。

TPS6208x 专注于在宽输出电流范围下实现高效降压转换。该转换器在中等程度的负载到高负载时运行于脉宽调制 (PWM) 模式，并在轻负载电流条件下自动进入省电模式运行，从而在整个负载电流范围内保持高效率。为了在超低负载或无负载电流下保持高效率运行，该器件采用具有超低静态电流的贪睡模式。该功能通过 MODE 引脚使能，可延长增加电池驱动 应用 的运行时间，同时保持最低待机电流，以满足针对低待机电流的绿色能源标准。

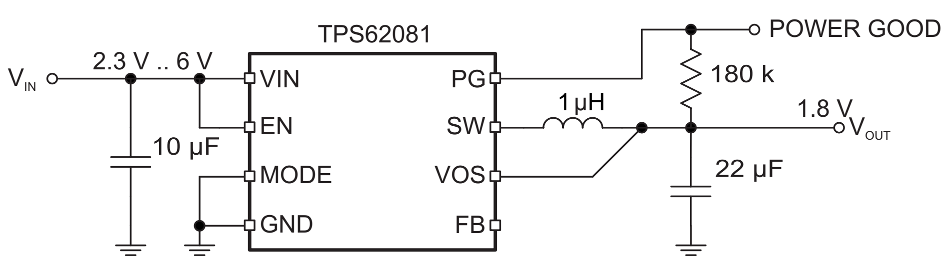
为了满足系统电源轨需求，内部补偿电路支持使用高于 100µF 的外部输出电容。凭借 DCS-Control™架构，可实现出色的负载瞬态性能和输出电压调节精度。该器件采用带有散热焊盘的 2mm x 2mm WSON 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS62080	WSON (8)	2.00mm x 2.00mm
TPS62080A		
TPS62081		
TPS62082		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (April 2015) to Revision F	Page
• Changed From: T_A = –40°C to 85°C To: T_J = –40°C to 125°C in the *Electrical Characteristics* condition statement	6
• Added a Test Condition to I_{SD} in the *Electrical Characteristics*	6
• Changed the $R_{DS(on)}$ High-side TYP value From: 120 mΩ To: 95 mΩ in the *Electrical Characteristics*	6
• Changed the $R_{DS(on)}$ Low-side TYP value From: 90 mΩ To: 70 mΩ in the *Electrical Characteristics*	6
• Changed the graphs to include a 125°C curve in the *Typical Characteristics*	7
• Added 50 Ω value to the Power Good block in Figure 5	8
• Added 50 Ω value to the Power Good block in Figure 6	9
• Added Table 1	9

Changes from Revision D (July 2013) to Revision E	Page
• 已添加 *引脚配置和功能部分，ESD 额定值表，特性 说明 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分*	1

Changes from Revision C (May 2013) to Revision D	Page
• Deleted TPS62080ADGN from ORDERING INFORMATION table	4
• Deleted TPS62080A column from the *Thermal Information* table	5

Changes from Revision B (March 2012) to Revision C	Page
• Changed the Thermal Information tables values	5

Changes from Revision A (February 2012) to Revision B **Page**

- Changed TPS62080ADSG from Product Preview to Production Data in ORDERING INFORMATION................................ 4

Changes from Original (September 2011) to Revision A **Page**

- 已添加 TPS62080A 器件 1
- Added TPS62080ADSG (Product Preview) and TPS62080ADGN (Product Preview) to ORDERING INFORMATION 4
- Added TPS62080A output discharge resistor 6

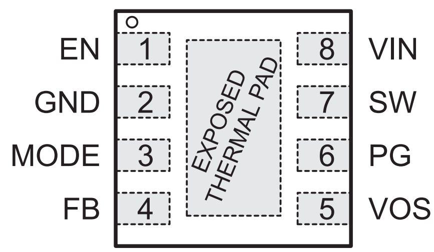
5 Device Comparison Table

PART NUMBER(1)	OUTPUT VOLTAGE(2)	OUTPUT DISCHARGE RESISTOR	PACKAGE MARKING	PACKAGE
TPS62080DSG	Adjustable	1 kΩ	QVR	8-Pin WSON
TPS62081DSG	1.8 V	1 kΩ	QVS	8-Pin WSON
TPS62082DSG	3.3 V	1 kΩ	QVT	8-Pin WSON
TPS62080ADSG	Adjustable	40 Ω	SBN	8-Pin WSON

(1) For detailed ordering information, see *机械、封装和可订购信息*.
(2) Contact the factory to check availability of other fixed output voltage versions.

6 Pin Configuration and Functions

DSG Package
8-Pin WSON With Thermal Pad
(Top View)



Pin Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
EN	1	IN	Device Enable Logic Input. Logic HIGH enables the device, logic LOW disables the device and turns it into shutdown. Do not leave floating.
GND	2	PWR	Power and Signal Ground.
MODE	3	IN	Snooze Mode Enable Logic Input. Logic HIGH enables the Snooze Mode, logic LOW disables the Snooze Mode. Do not leave floating.
FB	4	IN	Feedback Pin for the internal control loop. Connect this pin to the external feedback divider for the adjustable output versions. For the fixed output voltage versions, this pin must be left floating or connected to GND.
VOS	5	IN	Output Voltage Sense Pin for the internal control loop. Must be connected to output voltage.
PG	6	OUT	Power Good open drain output. This pin is pulled to low if the output voltage is below regulation limits. Can be left floating if not used.
SW	7	PWR	Switch Pin connected to the internal MOSFET switches and inductor terminal. Connect the inductor of the output filter here.
VIN	8	PWR	Power Supply Voltage Input.
Exposed Thermal Pad	—	—	Connect it to GND. The thermal pad must be soldered to achieve appropriate power dissipation and mechanical reliability.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Voltage at VIN, PG, VOS(2)	–0.3	7	V
Voltage at SW(2)(3)	–1	7	V
Voltage at FB(2)	–0.3	3.6	V
Voltage at EN, MODE(2)	–0.3	VIN + 0.3	V
Sink current at PG	0	0.5	mA
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) During operation, device switching.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.3		6	V
V_{OUT}	Output voltage	0.5		4	V
I_{SNOOZE}	Load current in Snooze Mode			2	mA
T_J	Operating junction temperature	–40		125	°C

(1) Refer to the *Application and Implementation* section for further information.

7.4 Thermal Information

THERMAL METRIC(1)		TPS6208x DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	59.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Over recommended free-air temperature range, T_J = –40°C to 125°C. Typical values are at T_A = 25°C (unless otherwise noted), V_{IN}= 3.6 V, MODE = LOW.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range			2.3		6	V
I_Q	Quiescent current into VIN	I_{OUT} = 0 mA, Device not switching			30		uA
	Quiescent current into VIN (SNOOZE MODE)	I_{OUT} = 0 mA, Device not switching, MODE=HIGH			6.5		uA
I_{SD}	Shutdown current into VIN	EN = LOW				7	µA
			T_A = -40°C to 85°C			1	
V_{UVLO}	Undervoltage lockout	Input voltage falling			1.8	2	V
	Undervoltage lockout hysteresis	Rising above V_{UVLO}			120		mV
T_{JSD}	Thermal shutdown	Temperature rising			150		°C
	Thermal shutdown hysteresis	Temperature falling below T_{JSD}			20		°C
LOGIC INTERFACE (EN MODE)							
V_{IH}	High level input voltage	2.3 V ≤ V_{IN} ≤ 6 V		1			V
V_{IL}	Low level input voltage	2.3 V ≤ V_{IN} ≤ 6 V				0.4	V
I_{LKG}	Input leakage current				0.01	0.5	µA
POWER GOOD							
V_{PG}	Power good threshold	V_{OUT} falling referenced to V_{OUT} nominal		–15%	–10%	–5%	
	Power good hysteresis				5%		
V_{OL}	Low level voltage	I_{sink} = 500 µA				0.3	V
$I_{PG,LKG}$	PG Leakage current	V_{PG} = 5.0 V			0.01	0.1	µA
OUTPUT							
V_{OUT}	Output voltage range TPS62080, TPS62080A			0.5		4.0	V
	Output voltage accuracy TPS62081	I_{OUT} = 0 mA; V_{IN} ≥ 2.3 V		–2.5%		2.5%	
	Output voltage accuracy TPS62082	I_{OUT} = 0 mA; V_{IN} ≥ 3.6 V		–2.5%		2.5%	
	Snooze Mode output voltage accuracy	MODE = HIGH; V_{IN} ≥ 2.3 V and V_{IN} ≥ V_{OUT} + 1 V		–5%		5%	
V_{FB}	Feedback regulation voltage TPS62080, TPS62080A	V_{IN} ≥ 2.3 V and V_{IN} ≥ V_{OUT} + 1 V		0.438	0.45	0.462	V
I_{FB}	Feedback input bias current TPS62080, TPS62080A	V_{FB} = 0.45 V			10	100	nA
R_{DIS}	Output discharge resistor	EN = LOW, V_{OUT} = 1.8 V			1		kΩ
		TPS62080A, EN = LOW, V_{OUT} = 1.2 V		25	40	65	Ω
	Line Regulation				0		%/V
	Load Regulation	TPS62081, TPS62082			–0.25		%/A
$R_{DS(on)}$	High-side FET ON-resistance	I_{SW} = 500 mA			95		mΩ
	Low-side FET ON-resistance	I_{SW} = 500 mA			70		mΩ
I_{LIM}	High-side FET switch current limit	Rising inductor current		1.6	2.8	4	A

7.6 Typical Characteristics

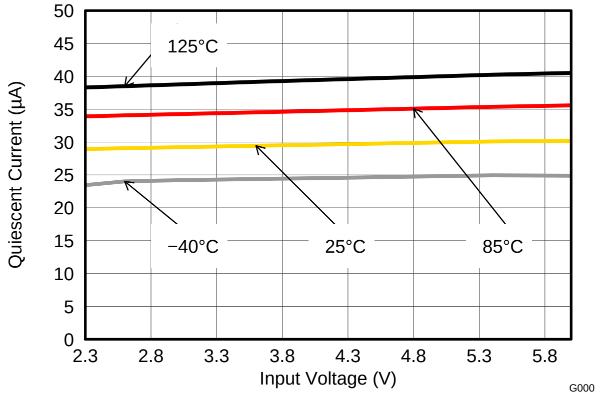


Figure 1. Quiescent Current vs Input Voltage in Normal Mode

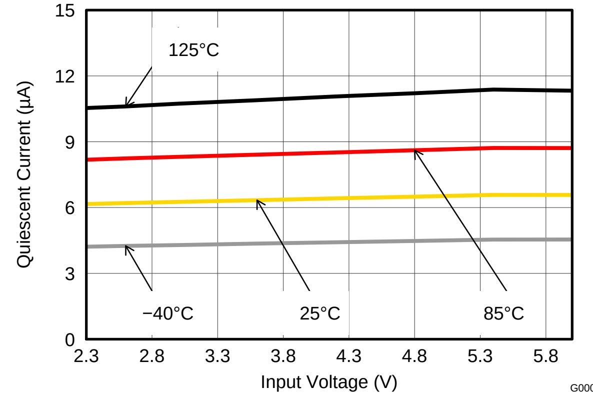


Figure 2. Quiescent Current vs Input Voltage in Snooze Mode

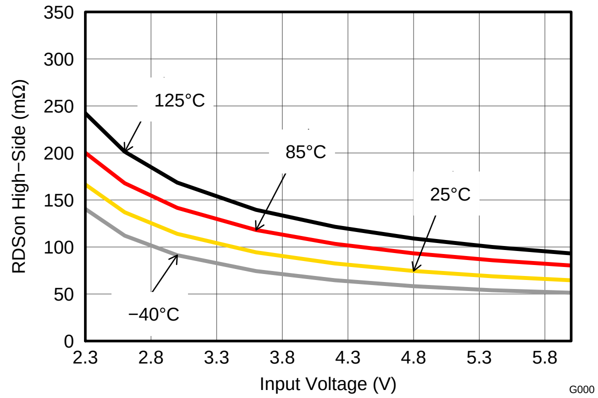


Figure 3. High-Side FET $R_{DS(on)}$ vs Input Voltage

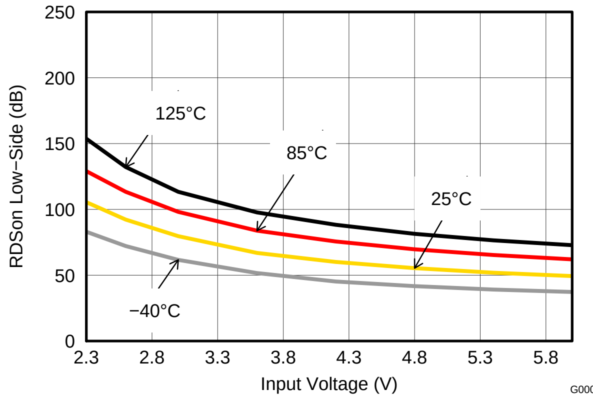


Figure 4. Low-Side FET $R_{DS(on)}$ vs Input Voltage

8 Detailed Description

8.1 Overview

The TPS6208x synchronous switched mode converters are based on DCS-Control™ (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic, voltage and current mode control.

The DCS-Control topology operates in pulse width modulation (PWM) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. DCS-Control supports both operation modes (PWM and PFM) using a single building block having a seamless transition from PWM to Power Save Mode without effects on the output voltage. Fixed output voltage versions provide smallest solution size combined with lowest no load current consumption. The TPS6208x offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

The device is equipped with Snooze Mode functionality, which is enabled with the MODE pin. Snooze Mode supports high efficiency conversion at lowest output currents below 2 mA. If no load current is drawn, the ultra low quiescent current of 6.5 µA is sufficient to maintain the output voltage. This extends battery run time by reducing the quiescent current during lowest or no load conditions in battery-driven applications. For mains-operated voltage supplies, Snooze Mode reduces the system's stand-by energy consumption. During shutdown (EN = LOW), the device reduces energy consumption to less than 1 µA.

8.2 Functional Block Diagrams

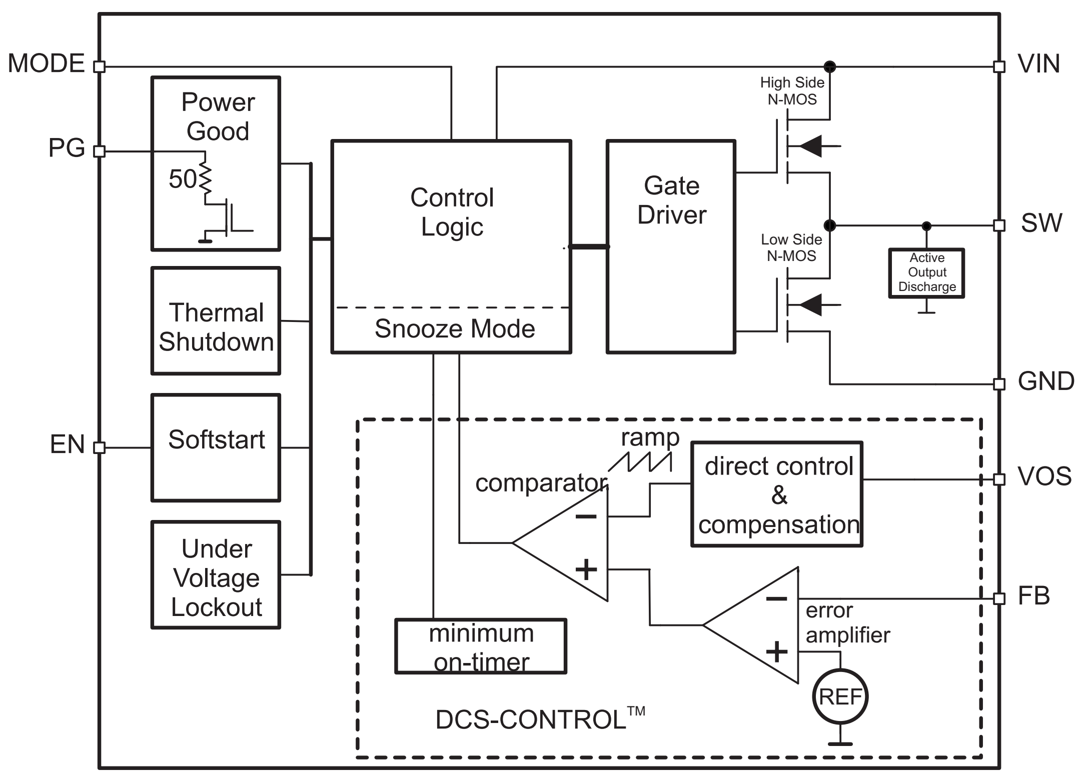


Figure 5. Functional Block Diagram (Adjustable Output Voltage Version)

Functional Block Diagrams (continued)

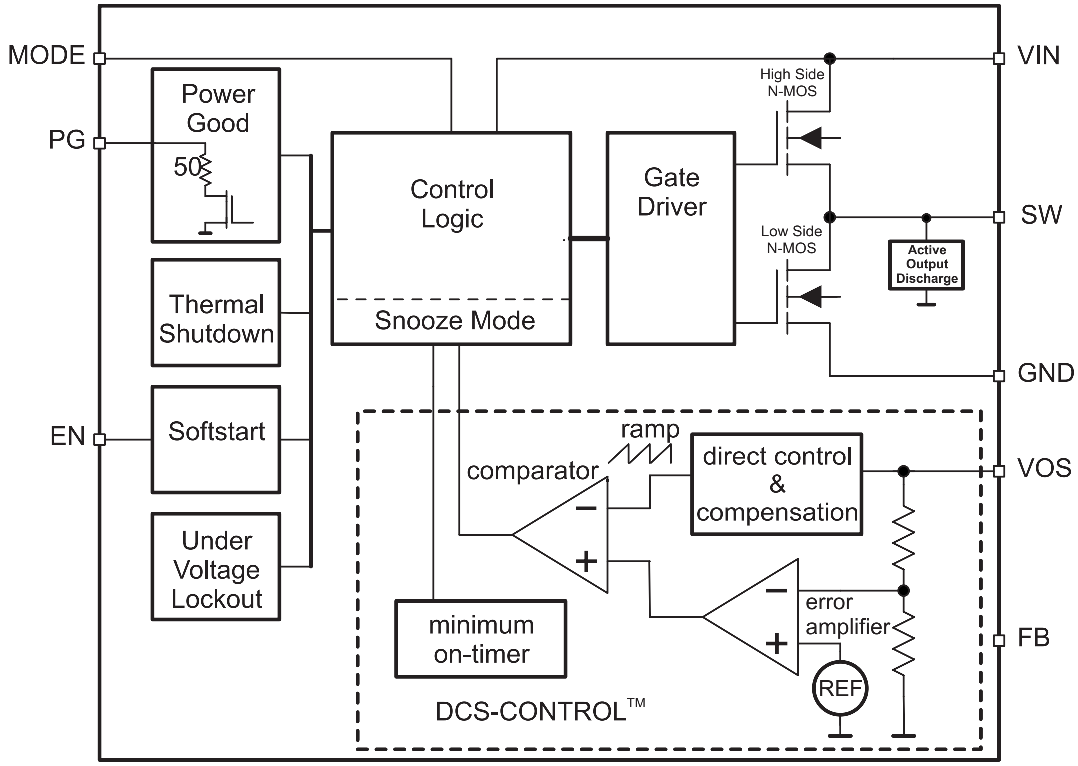


Figure 6. Functional Block Diagram (Fixed Output Voltage Version)

8.3 Feature Description

8.3.1 Power Good

The TPS6208x has a power good output which goes low when the output voltage is below its nominal value. The power good is high impedance once the output is above 95% of the regulated voltage, and is driven to low once the output voltage falls below typically 90% of the regulated voltage. The PG pin is an open drain output and can sink up to 0.5 mA. The power good output requires a pull-up resistor. When the device is off due to disable, UVLO or thermal shutdown, the PG pin is high impedance (see Table 1). The PG signal can be used for sequencing of multiple rails by connecting to the EN pin of other converters. Leave the PG pin unconnected when not used.

Table 1. Power Good Pin Logic Table

Device Information		PG Logic Status	
		High Z	Low
Enable (EN=High)	$V_{FB} \geq V_{PG}$	√	
	$V_{FB} \leq V_{PG}$		√
Shutdown (EN=Low)		√	
UVLO	$0.7V < V_{IN} < V_{UVLO}$	√	
Thermal Shutdown	$T_J > T_{JSD}$	√	
Power Supply Removal	$V_{IN} < 0.7V$	√	

8.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input to output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain an output voltage is calculated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L) \quad (1)$$

where

- $V_{IN,MIN}$ = Minimum input voltage
- $I_{OUT,MAX}$ = Maximum output current
- $R_{DS(on)}$ = High-side FET ON-resistance
- R_L = Inductor ohmic resistance

8.3.3 Output Discharge

The output gets discharged by the SW pin with a typical discharge resistor of R_{DIS} whenever the device shuts down. This is the case when the device gets disabled by enable, thermal shutdown, or undervoltage lockout. The TPS6208A differs from the TPS62080 only in its stronger discharge.

8.3.4 Soft-Start

When EN is set to start device operation, the device starts switching after a delay of about 40 μs and VOUT rises with a slope of about 10mV/μs (See Figure 27 andFigure 29 for typical startup operation). This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

If the output voltage is not reached within the soft start time, such as in the case of heavy load, the converter enters regular operation. Consequently, the inductor current limit operates as described below. The TPS6208x is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps up the output voltage to its nominal value.

8.3.5 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is implemented that shuts down the device at voltages lower than V_{UVLO} with a 120 mV typical hysteresis.

8.3.6 Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically T_{JSD}. Once the device temperature falls below the threshold minus hysteresis, the device returns to normal operation automatically.

8.3.7 Inductor Current Limit

The Inductor Current Limit prevents the device from high inductor current and drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted/saturated inductor or a heavy load/shorted output circuit condition.

The incorporated inductor peak current limit measures the current in the high-side and low-side power MOSFET. Once the high-side switch current limit is tripped, the high-side MOSFET is turned off and the low-side MOSFET is turned on to reduce the inductor current. When the inductor current drops down to the low-side switch current limit, the low-side MOSFET is turned off and the high-side switch is turned on again. This operation repeats until the inductor current does not reach the high-side switch current limit. Due to internal propagation delays, the real current limit value can exceed the static current limit in *Electrical Characteristics*.

8.4 Device Functional Modes

8.4.1 Enabling and Disabling the Device

The device is enabled by setting the EN input to a logic HIGH. Accordingly, a logic LOW disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the programmed threshold. The EN input must be terminated and not left floating.

8.4.2 Power Save Mode

As the load current decreases, the TPS6208x enters Power Save Mode operation. During Power Save Mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current maintaining high efficiency. Power Save Mode occurs when the inductor current becomes discontinuous. It is based on a fixed on time architecture. The typical on time is given by t_{on} = 500 ns × (V_{OUT}/V_{IN}). The switching frequency over the whole load current range is shown in Figure 21 and Figure 22.

8.4.3 Snooze Mode

The TPS6208x offers a Snooze Mode function. If Snooze Mode is enabled by an external logic signal setting the MODE pin to HIGH, the device's quiescent current consumption is reduced to typically 6.5 µA. As a result, the high efficiency range is extended towards the range of lowest output currents below 2 mA. See the efficiency figures in *Application Curves*.

If the device is operating in Snooze Mode, a dedicated, low power consuming block monitors the output voltage. All other control blocks are snoozing during that time. If the output voltage falls below the programmed output voltage by 3.5% (typ), the control blocks wake up, regulate the output voltage and allow themselves to snooze again until the output voltage drops again. Snooze Mode operation provides a clear efficiency improvement at lowest output currents. If the load current increases, the advantage of efficiency in Snooze mode is reduced. Because the dynamic load regulation operates best if Snooze Mode is disabled, it is recommended to turn off Snooze Mode when the load current exceeds 2 mA. Generally, a microcontroller operates the MODE pin.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS62080 and TPS62080A are synchronous step-down converter whose output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference. The TPS62081 and TPS62082 provide a fixed output volage which do not need an external resistor divider.

9.2 Typical Application

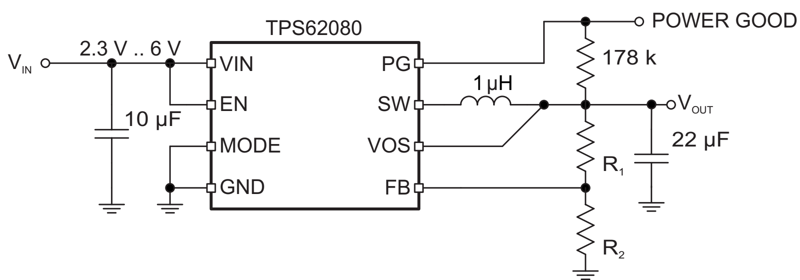


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Figure 7. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.3 V to 6 V
Output voltage	1.2 V
Output ripple voltage	< 20 mV
Maximum output current	1.2 A

9.2.2 Detailed Design Procedure

Table 3 lists the components used for the example.

Table 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 uF, Ceramic Capacitor, 6.3 V, X5R, size 0603	Std
C2	22 uF, Ceramic Capacitor, 6.3 V, X5R, size 0805, GRM21BR60J226ME39L	Murata
L1	1.0 µH, Power Inductor, 2.2 A, size 3 × 3 × 1.2 mm, XFL3012-102MEB	Coilcraft
R1	Depending on the output voltage of TPS62080, 1%; Not populated for TPS62081, TPS62082;	Std
R2	39.2k, Chip Resistor, 1/16W, 1%, size 0603	Std
R3	178k, Chip Resistor, 1/16W, 1%, size 0603	Std

9.2.2.1 Setting the Output Voltage

The TPS608x devices are available as fixed and adjustable output voltage versions. The fixed voltage versions are internally programmed to a fixed output voltage, whereas the adjustable output voltage version needs to be programmed via an external voltage divider to set the desired output voltage.

9.2.2.1.1 Adjustable Output Voltage Version

For the adjustable output voltage version, an external resistor divider is used. By selecting R_1 and R_2, the output voltage is programmed to the desired value.

When the output voltage is regulated, the typical voltage at the FB pin is V_{FB} for the adjustable devices. The following equation can be used to calculate R_1 and R_2.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.45V \times \left(1 + \frac{R1}{R2}\right) \tag{2}$$

For best accuracy, R2 should be kept smaller than 40kΩ to ensure that the current flowing through R2 is at least 100 times larger than I_{FB}. Changing towards a lower value increases the robustness against noise injection. Changing towards higher values reduces the input current. For lowest input current during Snooze Mode, it is recommended to use a fixed output voltage version such as TPS62081 and TPS62082.

9.2.2.2 Output Filter Design

The inductor and the output capacitor together provide a low pass filter. To simplify this process, Table 4 outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

Table 4. Matrix of Output Capacitor and Inductor Combinations

L [µH][1]	C_{OUT} [µF][1]				
	10	22	47	100	150
0.47					
1	+	+[2][3]	+	+	
2.2	+	+	+	+	
4.7					

(1) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%. Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Plus mark indicates recommended filter combinations.
(3) Filter combination in typical application.

9.2.2.3 Inductor Selection

The main parameters for the inductor selection are the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, Equation 3 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value (3)

TI recommends to choose the saturation current for the inductor 20%~30% higher than the $I_{L,MAX}$, out of Equation 3. A higher inductor value is also useful to lower ripple current, but increases the transient response time as well. The following inductors are recommended for use.

Table 5. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING [mA]	DIMENSIONS L x W x H [mm^3]	DC RESISTANCE [mΩ typ]	TYPE	MANUFACTURER
1.0	2500	3 x 3 x 1.2	35	XFL3012-102ME	Coilcraft
1.0	1650	3 x 3 x 1.2	40	LQH3NPN1R0NJ0	Murata
2.2	2500	4 x 3.7 x 1.65	49	LQH44PN2R2MP0	Murata
2.2	1600	3 x 3 x 1.2	81	XFL3012-222ME	Coilcraft

9.2.2.4 Capacitor Selection

The input capacitor is the low impedance energy source for the converter which helps to provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between VIN and GND as close as possible to those pins. For most applications 10 μF is sufficient, though a larger value reduces input current ripple.

The architecture of the TPS6208X allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use X7R or X5R dielectric. The TPS6208x is designed to operate with an output capacitance of 10 µF to 100 µF and beyond, as outlined in Table 4. Load transient testing and measuring the bode plot are good ways to verify stability with larger capacitor values.

Table 6. List of Recommended Capacitors

CAPACITANCE [µF]	TYPE	DIMENSIONS L x W x H [mm^3]	MANUFACTURER
10	GRM188R60J106M	0603: 1.6 x 0.8 x 0.8	Murata
22	GRM188R60G226M	0603: 1.6 x 0.8 x 0.8	Murata
22	GRM21BR60J226M	0805: 2.0 x 1.2 x 1.25	Murata

9.2.3 Application Curves

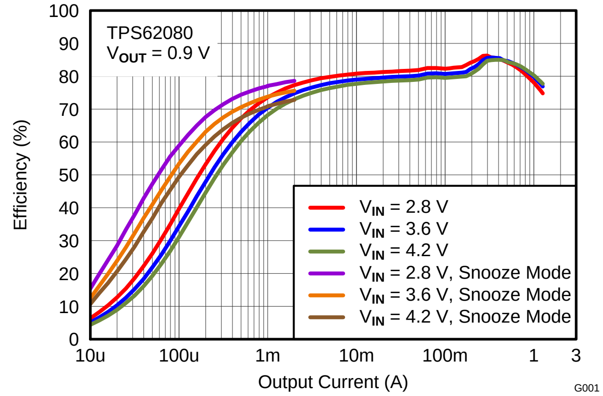


Figure 8. Efficiency vs Load Current

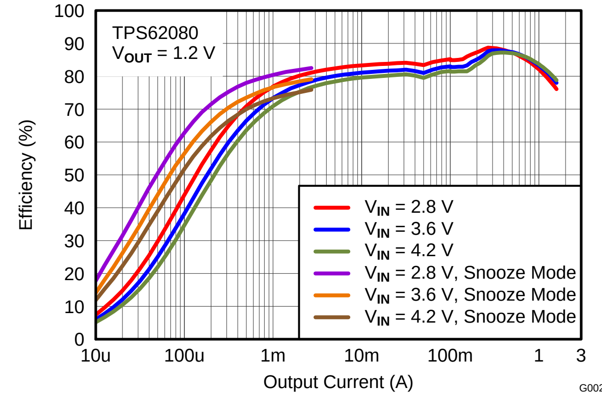


Figure 9. Efficiency vs Load Current

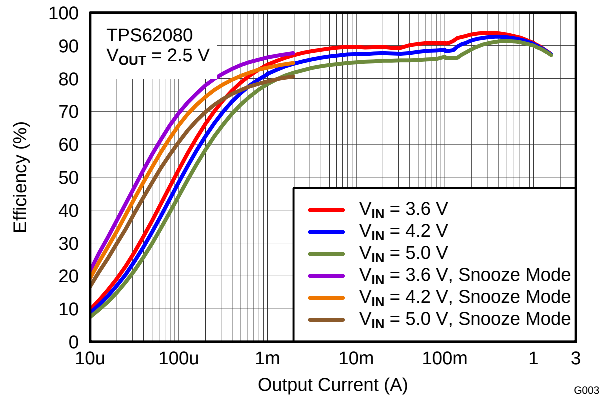


Figure 10. Efficiency vs Load Current

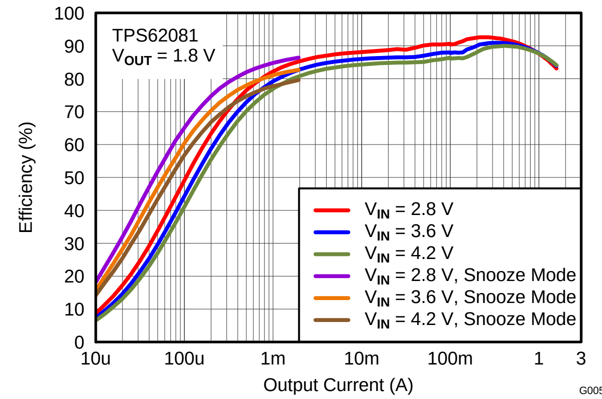


Figure 11. Efficiency vs Load Current

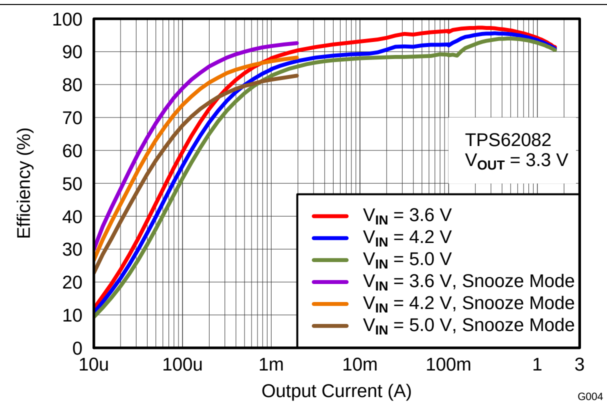


Figure 12. Efficiency vs Load Current

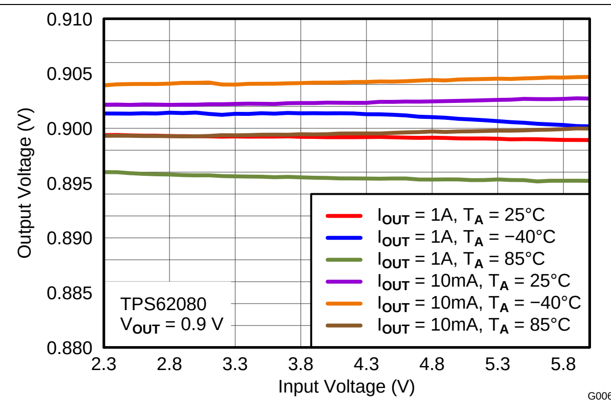


Figure 13. Output Voltage vs Input Voltage

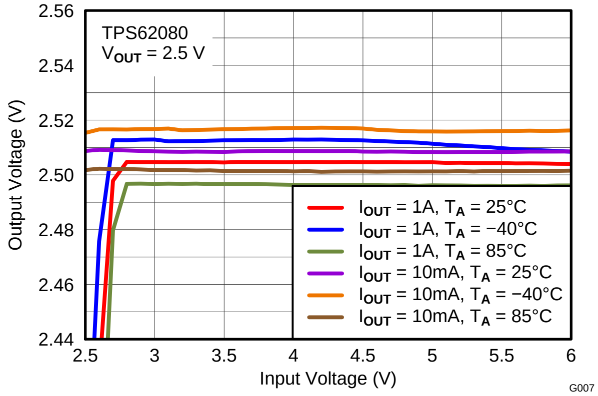


Figure 14. Output Voltage vs Input Voltage

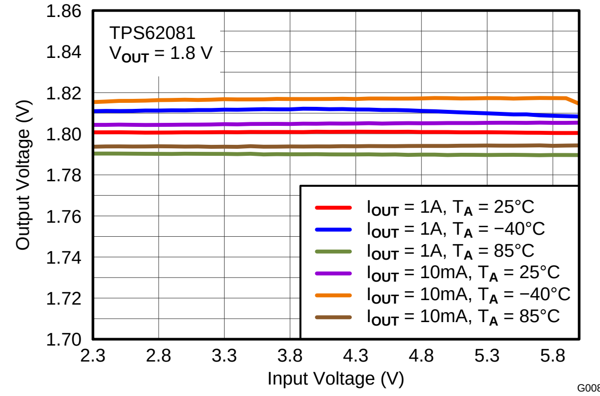


Figure 15. Output Voltage vs Input Voltage

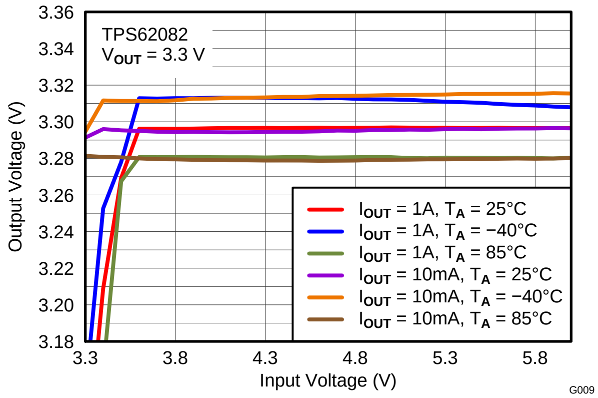


Figure 16. Output Voltage vs Input Voltage

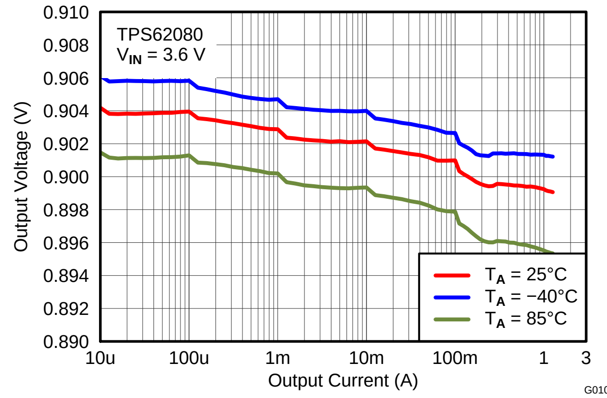


Figure 17. Output Voltage vs Load Current

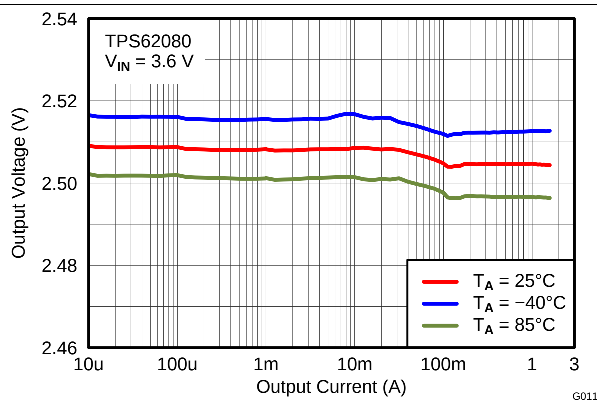


Figure 18. Output Voltage vs Load Current

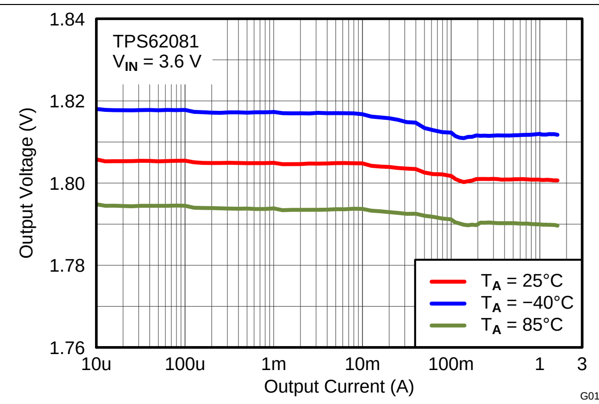


Figure 19. Output Voltage vs Load Current

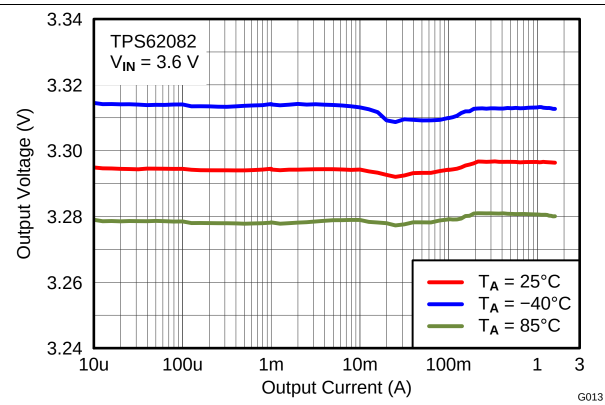


Figure 20. Output Voltage vs Load Current

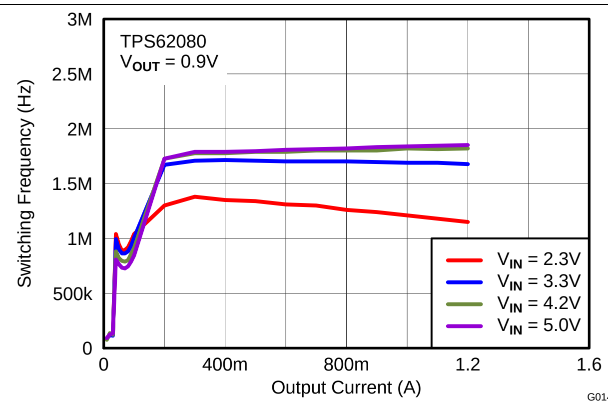


Figure 21. Switching Frequency vs Load Current

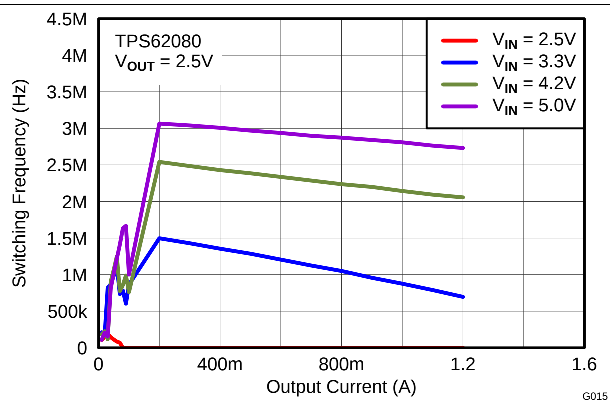
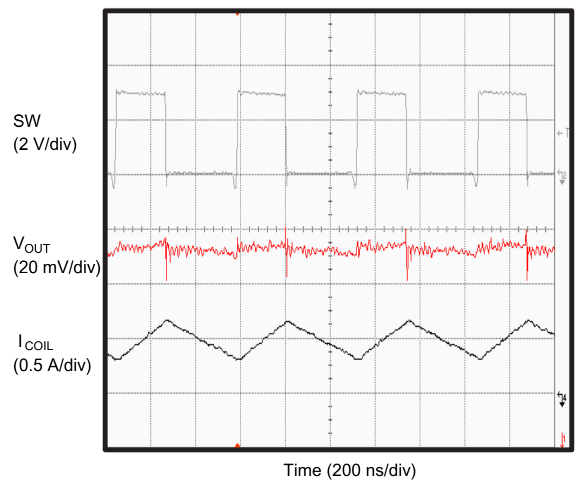
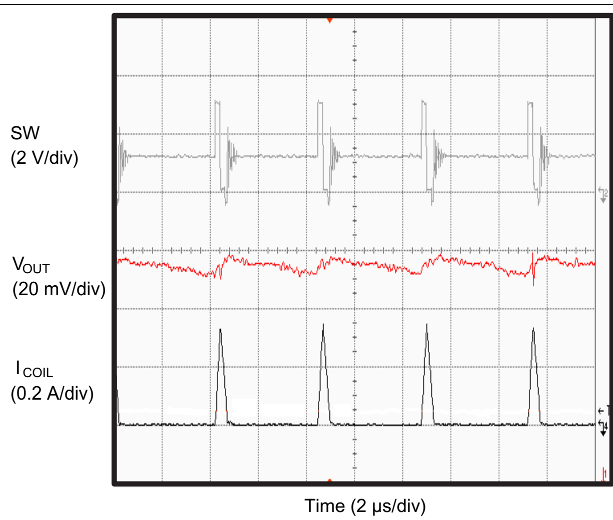


Figure 22. Switching Frequency vs Load Current



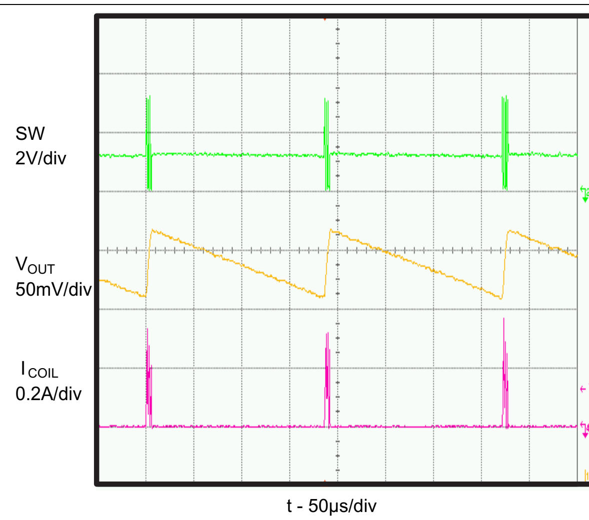
V_{IN} = 3.3 V, V_{OUT} = 1.2 V, Load Current = 500 mA

Figure 23. Typical Application (PWM Mode)



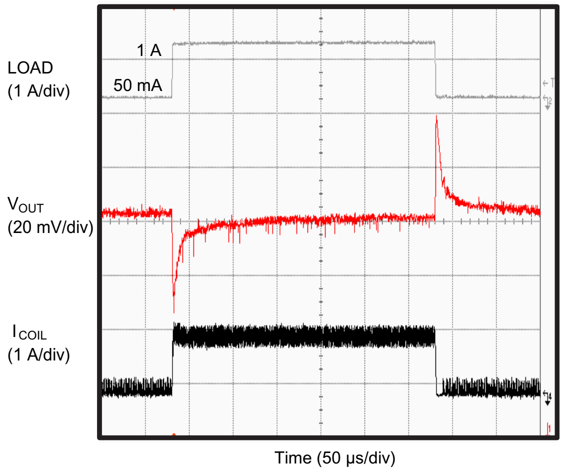
V_{IN} = 3.3 V, V_{OUT} = 1.2 V, Load Current = 10 mA

Figure 24. Typical Application (PFM Mode)



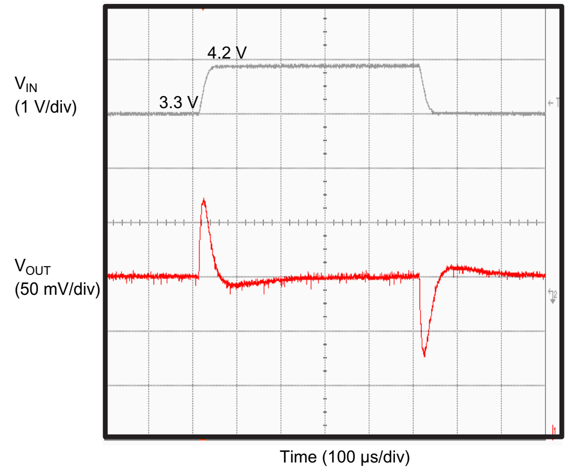
V_{IN} = 3.3 V, V_{OUT} = 1.2 V, Load Current = 2 mA

Figure 25. Typical Application (Snooze Mode)



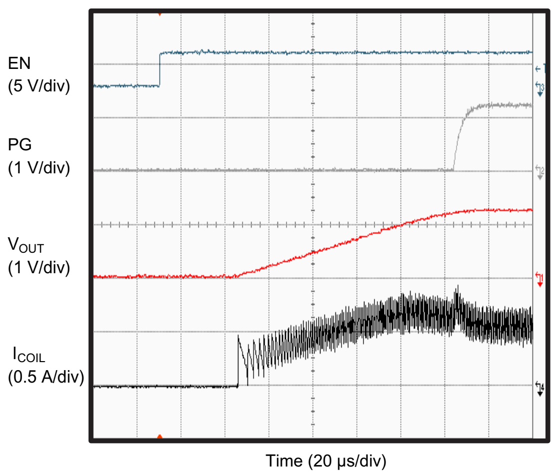
V_{IN} = 3.3 V, V_{OUT} = 1.2 V, Load Current = 50 mA to 1 A

Figure 26. Load Transient



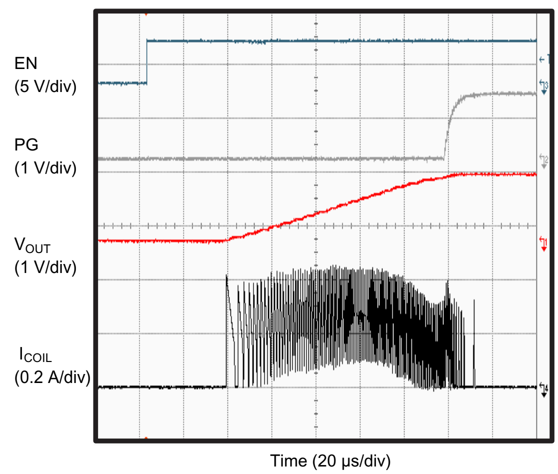
V_{IN} = 3.3 V to 4.2 V, V_{OUT} = 1.2 V, Load = 2.2 Ω

Figure 27. Line Transient



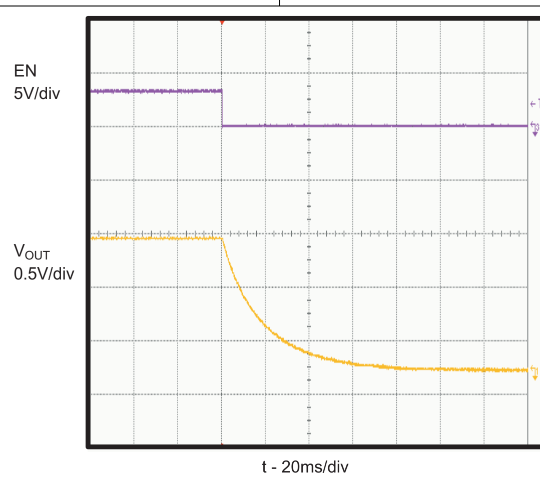
V_{IN} = 3.3 V, V_{OUT} = 1.2 V, Load = 2.2 Ω

Figure 28. Start Up



V_{IN} = 3.3 V, V_{OUT} = 1.2 V, No Load

Figure 29. Start Up (Without Load)



V_{IN} = 3.3 V, V_{OUT} = 1.2 V, No Load

Figure 30. Shutdown

10 Power Supply Recommendations

The device is designed to operate from an input supply voltage range between 2.3 V and 6 V. Ensure that the input power supply has a sufficient current rating for the application.

11 Layout

11.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TPS6208x devices.

The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance. A common power GND should be used. The low-side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.

The sense traces connected to the FB and VOS pins are signal traces. Special care should be taken to avoid noise being induced. By a direct routing, parasitic inductance can be kept small. GND layers might be used for shielding. Keep these traces away from SW nodes.

11.2 Layout Example

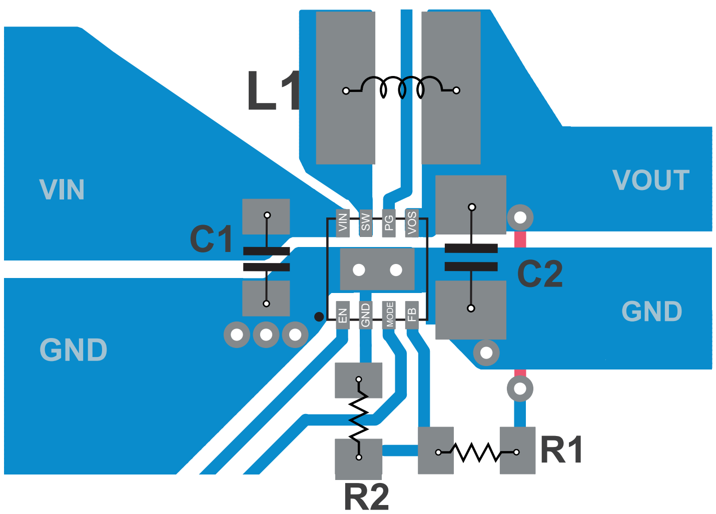


Figure 31. PCB Layout Suggestion

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering Exposed Thermal Pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017) and *Semiconductor and IC Package Thermal Metrics* (SPRA953).

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 文档支持

12.2.1 相关文档

相关文档请参见以下部分：

《采用 JEDEC PCB 设计的线性和逻辑封装散热特性》(SZZA017)

12.3 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，以及样片或购买的快速访问。

表 **7.** 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS62080	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62080A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62081	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62082	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.5 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 商标

DCS-Control, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62080ADSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	Call TI | Nipdauag | Nipdau	Level-2-260C-1 YEAR	-40 to 125	SBN
TPS62080ADSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SBN
TPS62080ADSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBN
TPS62080ADSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	Call TI | Nipdauag | Nipdau	Level-2-260C-1 YEAR	-40 to 125	SBN
TPS62080ADSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SBN
TPS62080DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	Call TI | Nipdauag | Nipdau	Level-2-260C-1 YEAR	-40 to 125	QVR
TPS62080DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVR
TPS62080DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVR
TPS62080DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QVR
TPS62080DSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QVR
TPS62080DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	Call TI | Nipdauag | Nipdau	Level-2-260C-1 YEAR	-40 to 125	QVR
TPS62080DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVR
TPS62080DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVR
TPS62081DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	Call TI | Nipdauag | Nipdau	Level-2-260C-1 YEAR	-40 to 125	QVS
TPS62081DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVS
TPS62081DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	Call TI | Nipdauag | Nipdau	Level-2-260C-1 YEAR	-40 to 125	QVS
TPS62081DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVS
TPS62082DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	Call TI | Nipdauag | Nipdau	Level-2-260C-1 YEAR	-40 to 125	QVT
TPS62082DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVT
TPS62082DSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVT
TPS62082DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	Call TI | Nipdauag | Nipdau	Level-2-260C-1 YEAR	-40 to 125	QVT
TPS62082DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVT

(1) **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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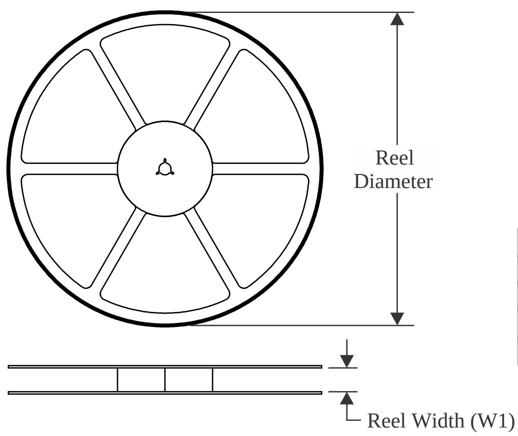
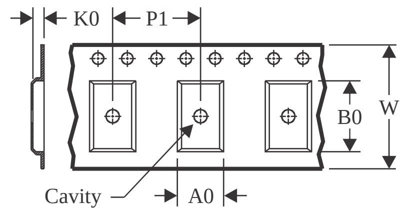
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

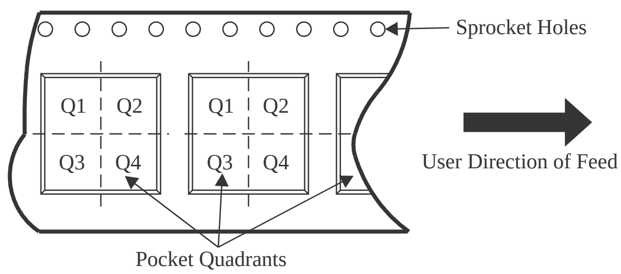


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

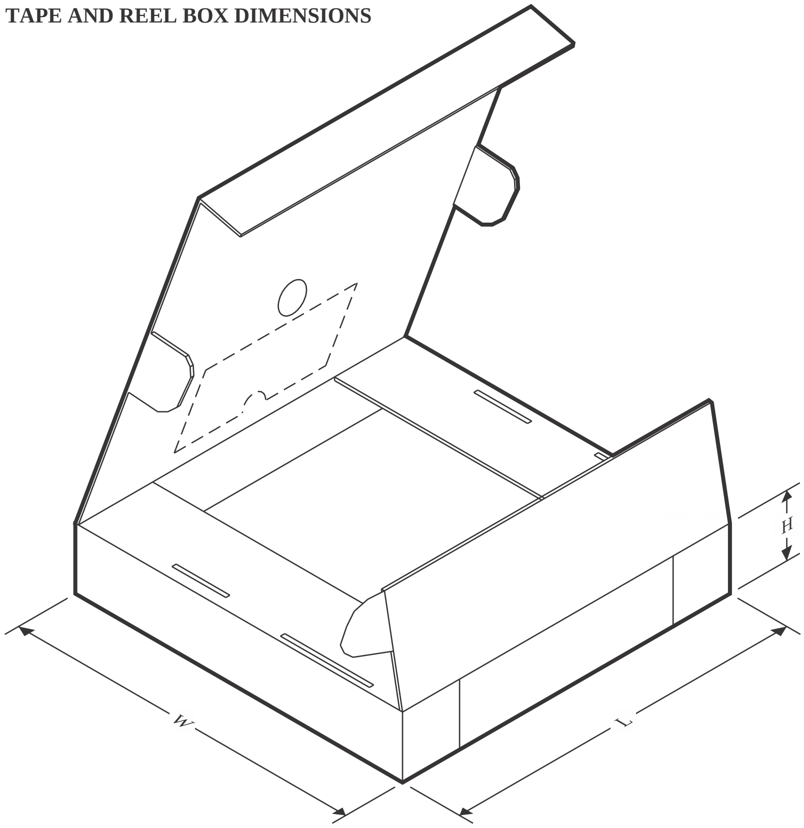
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62080ADSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62080ADSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62080DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62080DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62080DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62080DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62080DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62081DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62081DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62082DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62082DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62082DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2

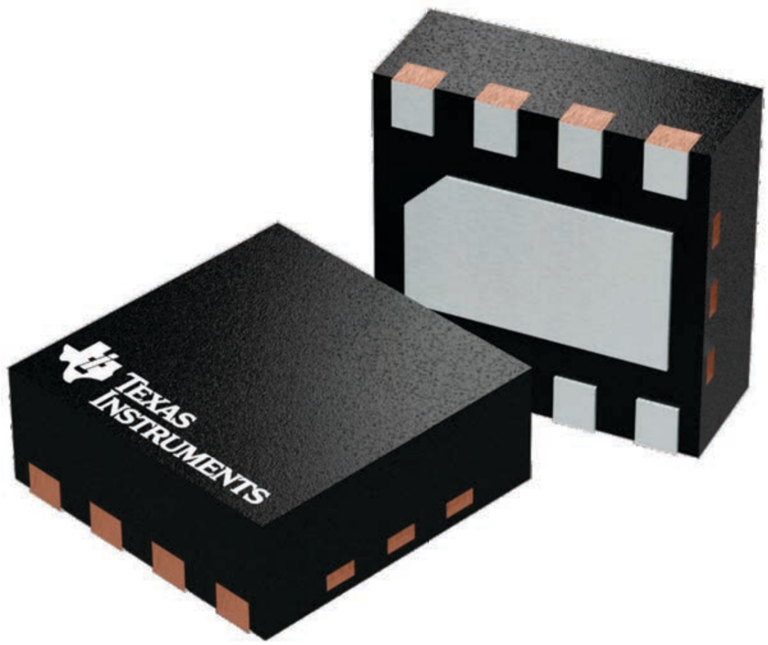
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

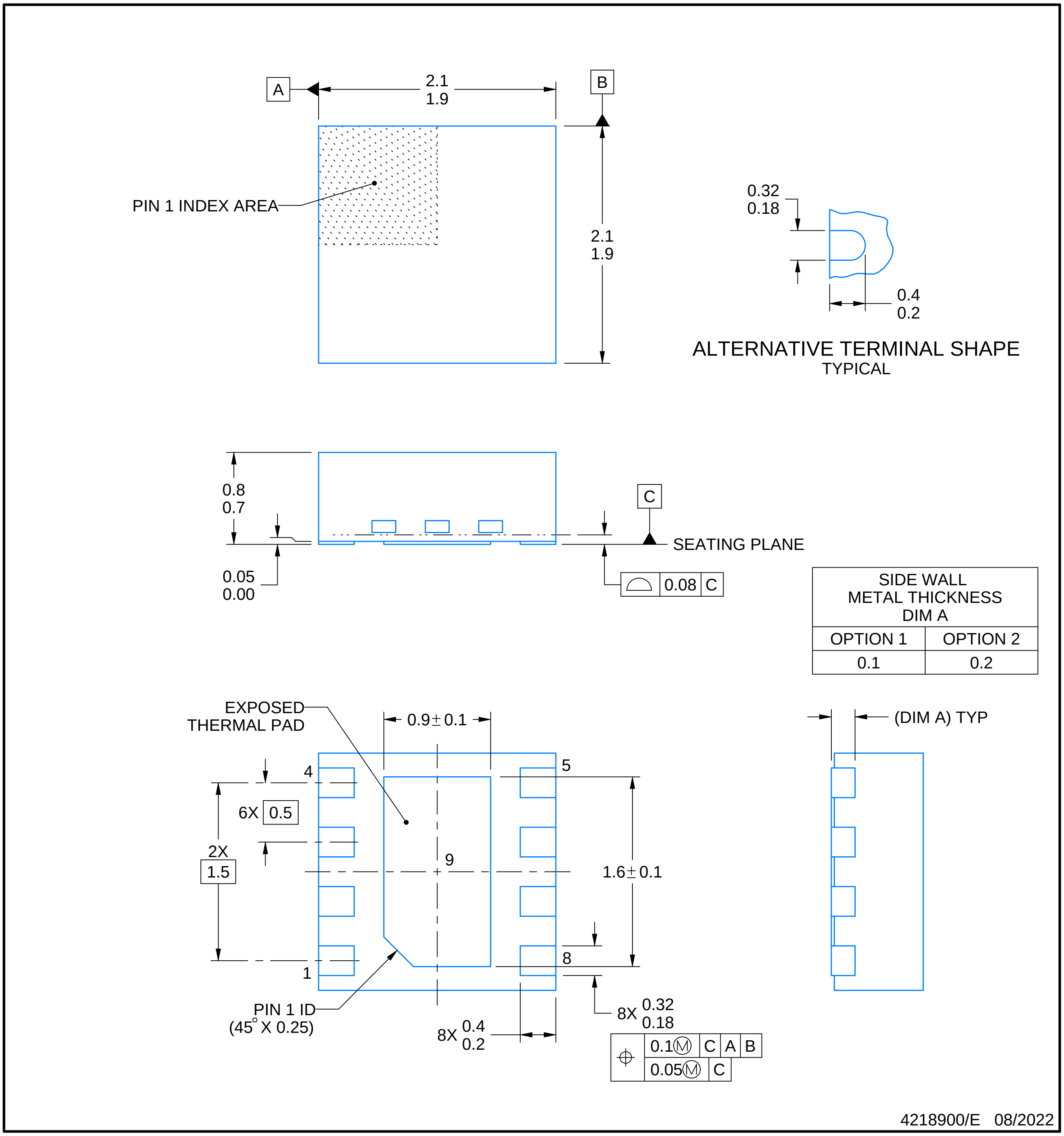
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62080ADSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62080ADSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62080DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62080DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62080DSGT	WSON	DSG	8	250	213.0	191.0	35.0
TPS62080DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS62080DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62081DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62081DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62082DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62082DSGT	WSON	DSG	8	250	213.0	191.0	35.0
TPS62082DSGT	WSON	DSG	8	250	205.0	200.0	33.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



WSON - 0.8 mm max height

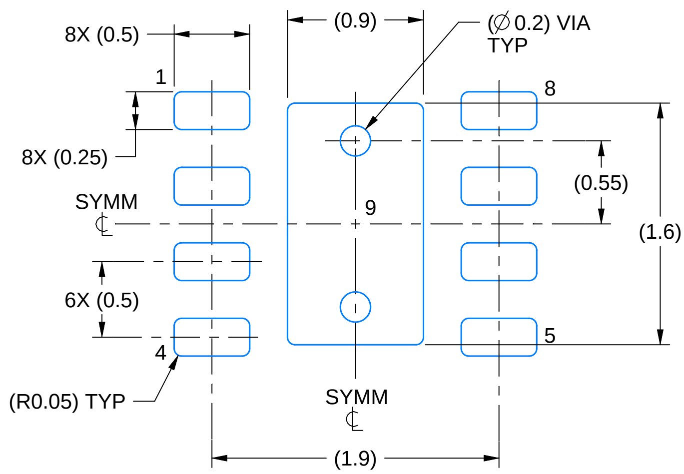
PLASTIC SMALL OUTLINE - NO LEAD



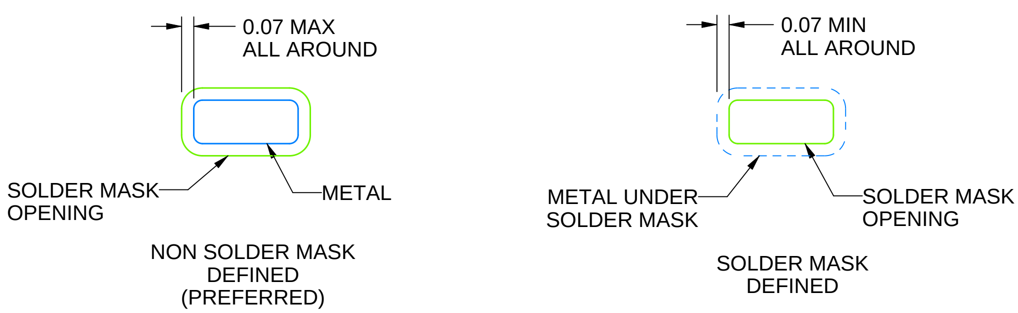
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

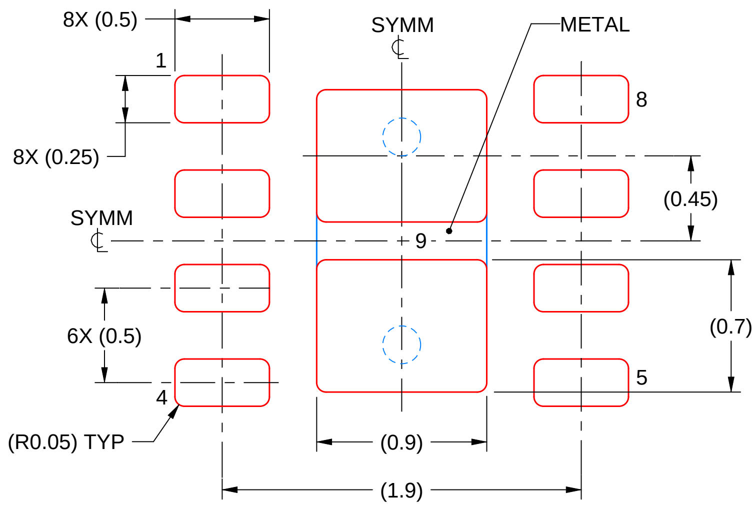


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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