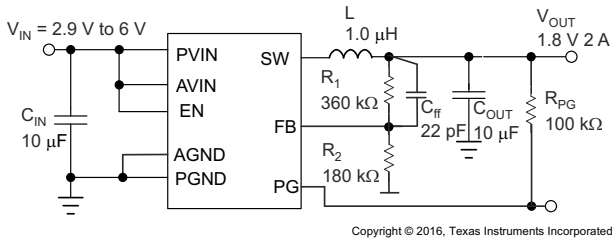
采用 2mm × 2mm SON 封装的 TPS6206x 3MHz、2A 降压转换器

1 特性

- 3MHz 开关频率
- 输入电压范围：2.9V 至 6V
- 效率高达 97%
- 省电模式/3MHz 固定 PWM 模式
- 电源正常输出
- PWM 模式下的输出电压精度为 ±1.5%
- 输出电容器放电功能
- 18μA 典型静态电流
- 100% 占空比，可实现超低压降
- 电压定位
- 时钟抖动
- 运行结温范围：-40°C 至 125°C
- 支持最高 1mm 的解决方案
- 采用 2mm x 2mm x 0.75mm WSON 封装

2 应用

- 负载点 (POL)
- 笔记本电脑、掌上电脑
- 便携式媒体播放器
- DSP 电源



典型应用原理图

3 说明

TPS6206x 是一个高效同步降压直流/直流转换器系列。此类器件可提供高达 2A 的输出电流。

借助于 2.9V 至 6V 的输入电压范围，此器件非常适合用于针对 5V 或者 3.3V 系统电源轨的电源转换。TPS6206x 器件在 3MHz 的固定频率下运行，在轻载电流情况下会进入省电模式，以便在整个负载电流范围内保持高效率。省电模式经过优化，具有低输出电压纹波。对于低噪声应用，TPS62065 可通过拉高 MODE 引脚来强制进入固定频率 PWM 模式。TPS62067 提供了开漏电源正常状态输出。

在关断模式下，流耗减少至 1μA 以下并且内部电路会对输出电容器进行放电。

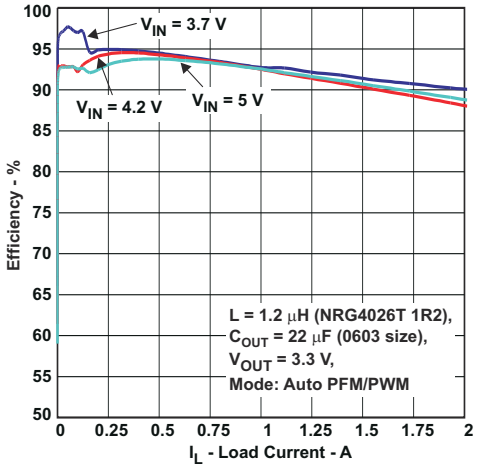
TPS6206x 系列经过了优化，可与微型 1μH 电感器和小型 10μF 输出电容器搭配使用，从而实现超小解决方案尺寸以及高稳压性能。

此类器件采用 2mm x 2mm x 0.75mm 8 引脚 WSON 封装。

器件信息

器件型号	封装 (1)	封装尺寸（标称值）
TPS62065 TPS62067	WSON (8)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



效率与负载电流间的关系

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (November 2016) to Revision E (October 2020) — **Page**

- 更新了整个文档的表、图和交叉参考的编号格式。.....1

Changes from Revision C (September 2015) to Revision D (November 2016) — **Page**

- Changed the conditions statement for *节 7.5*.....5
- Added Note 1 to the Test conditions of I_{SD}, I_{IN}, and I_{LKG} in *节 7.5*.....5
- Changed temperature values From: T_A To: T_J in 图 7-1 and 图 7-3.....7

Changes from Revision B (November 2013) to Revision C (September 2015) — **Page**

- 添加了 *引脚配置和功能* 部分、*ESD 等级* 表、*特性描述* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分.....1

Changes from Revision A (May 2010) to Revision B (November 2013) — **Page**

- Added Thermal Information table and deleted Dissipation Ratings table.....4

Changes from Revision * (March 2010) to Revision A () — **Page**

- 通篇将输入电压范围从“3V 至 6V”更改为“2.9V 至 6V”.....1
- Added equation to "Output Voltage Setting" section.....13
- Changed equation for calculating f_z.....13
- Changed equation for calculating C_{ff}.....13

5 Device Comparison Table

PART NUMBER (2)	OUTPUT VOLTAGE(1)	FUNCTION		MAXIMUM OUTPUT CURRENT
		MODE	POWER GOOD (PG)	
TPS62065	Adjustable	Selectable	No	2 A
TPS62067	Adjustable	Auto PWM/PFM	Yes	2 A

(1) Contact TI for other fixed output voltage options
(2) For the most current package and ordering information, see 节 13 at the end of this document, or see the TI website at www.ti.com.

6 Pin Configuration and Functions

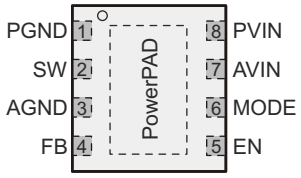


图 6-1. DSG Package 8-Pin WSON Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	3	I	Analog GND supply pin for the control circuit.
AVIN	7	I	Analog V_{IN} power supply for the control circuit. Must be connected to PVIN and input capacitor.
EN	5	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated
FB	4	I	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor
MODE	6	I	**MODE**: MODE pin = High forces the device to operate in fixed frequency PWM mode. MODE pin = Low enables the power save mode with automatic transition from PFM mode to fixed frequency PWM mode. This pin must be terminated.
PG		Open-Drain	**PG**: Power Good Open-Drain output. Connect an external pullup resistor to a rail which is below or equal AV_{IN}.
PGND	1	PWR	GND supply pin for the output stage.
PowerPAD™	—	—	For good thermal performance, this PAD must be soldered to the land pattern on the PCB. This PAD should be used as device GND.
PVIN	8	PWR	V_{IN} power supply pin for the output stage.
SW	2	O	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage(2)	AVIN, PVIN	–0.3	7	V
	EN, MODE, PG, FB	–0.3	V_{IN} +0.3 < 7	
	SW	–0.3	7	
Current (sink)	into PG		1	mA
Current (source)	Peak output	Internally limited		A
Temperature	T_J	–40	125	°C
	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
AV_{IN} , PV_{IN}	Supply voltage	2.9		6	V
	Output current capability			2000	mA
	Output voltage range for adjustable voltage	0.8		V_{IN}	V
L	Effective inductance	0.7	1	1.6	µH
C_{OUT}	Effective output capacitance	4.5	10	22	µF
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS62065 TPS62067 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_J = -40°C to 125°C, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 10 µF 0603, C_{OUT} = 10 µF 0603, L = 1 µH, see the parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.9		6	V
I_Q	Operating quiescent current	I_{OUT} = 0 mA, device operating in PFM mode and device not switching		18		µA
I_{SD}	Shutdown current	EN = GND, current into AVIN and PVIN(1)		0.1	1	µA
V_{UVLO}	Undervoltage lockout threshold	Falling	1.73	1.78	1.83	V
		Rising	1.9	1.95	1.99	
ENABLE, MODE						
V_{IH}	High level input voltage	2.9 V ≤ V_{IN} ≤ 6 V	1		6	V
V_{IL}	Low level input voltage	2.9 V ≤ V_{IN} ≤ 6 V	0		0.4	V
I_{IN}	Input bias current	EN, mode tied to GND or AVIN(1)		0.01	1	µA
POWER GOOD OPEN-DRAIN OUTPUT						
V_{THPG}	Power good threshold voltage	Rising feedback voltage	93%	95%	98%	
		Falling feedback voltage	87%	90%	92%	
V_{OL}	Output low voltage	I_{OUT} = –1mA; must be limited by external pullup resistor (1)			0.3	V
V_H	Output high voltage	Voltage applied to PG pin through external pullup resistor			V_{IN}	V
I_{LKG}	Leakage current into PG pin	$V_{(PG)}$ = 3.6V(1)			100	nA
t_{PGDL}	Internal power good delay time			5		µs
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 3.6 V (1)		120	180	mΩ
		V_{IN} = 5 V(1)		95	150	
$R_{DS(on)}$	Low-side MOSFET on-resistance	V_{IN} = 3.6 V(1)		90	130	mΩ
		V_{IN} = 5 V(1)		75	100	
I_{LIMF}	Forward current limit MOSFET high-side and low-side	2.9 V ≤ V_{IN} ≤ 6 V	2300	2750	3300	mA
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		10		
OSCILLATOR						
f_{SW}	Oscillator frequency	2.9 V ≤ V_{IN} ≤ 6 V	2.6	3	3.4	MHz
OUTPUT						
V_{ref}	Reference voltage			600		mV
$V_{FB(PWM)}$	Feedback voltage PWM mode	PWM operation, MODE = V_{IN} , 2.9 V ≤ V_{IN} ≤ 6 V, 0 mA load	–1.5%	0%	1.5%	
$V_{FB(PFM)}$	Feedback voltage PFM mode, voltage positioning	device in PFM mode, voltage positioning active(2)		1%		
V_{FB}	Load regulation			–0.5		%/A
	Line regulation			0		%/V
$R_{(Discharge)}$	Internal discharge resistor	Activated with EN = GND, 2.9 V ≤ V_{IN} ≤ 6 V, 0.8 ≤ V_{OUT} ≤ 3.6 V	75	200	1450	Ω
t_{START}	Start-up time	Time from active EN to reach 95% of V_{OUT}		500		µs

(1) Maximum value applies for T_J = 85°C

(2) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{ref}. See the parameter measurement information.

7.6 Typical Characteristics

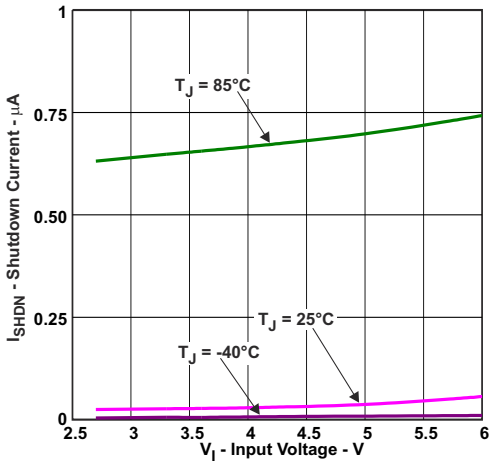


图 7-1. Shutdown Current vs Input Voltage and Ambient Temperature

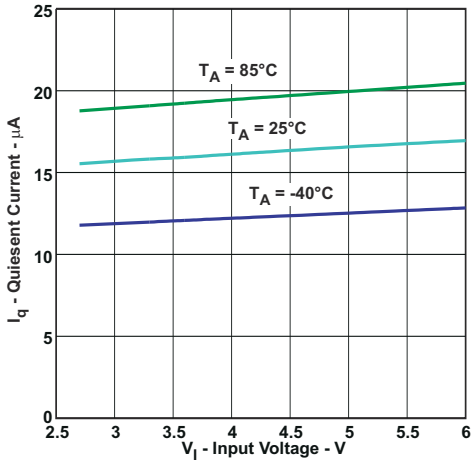


图 7-2. Quiescent Current vs Input Voltage

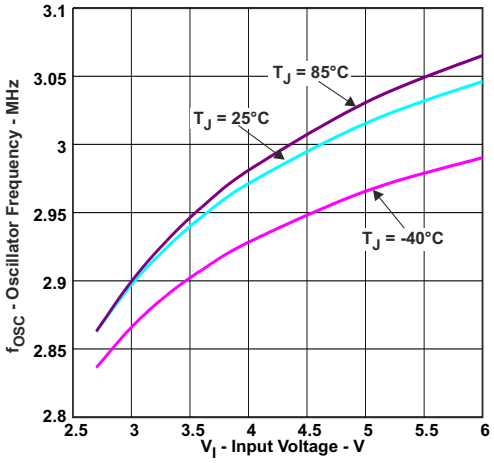


图 7-3. Oscillator Frequency vs Input Voltage

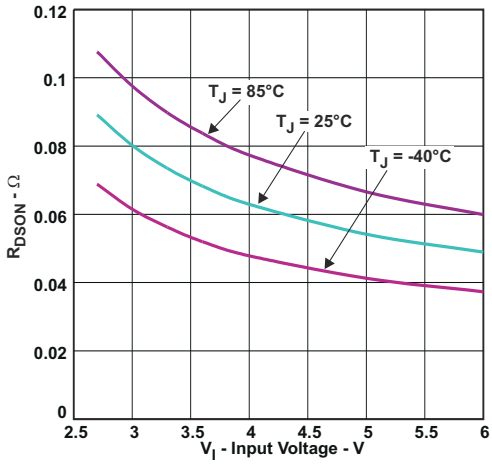


图 7-4. R_{DSON} Low-Side Switch

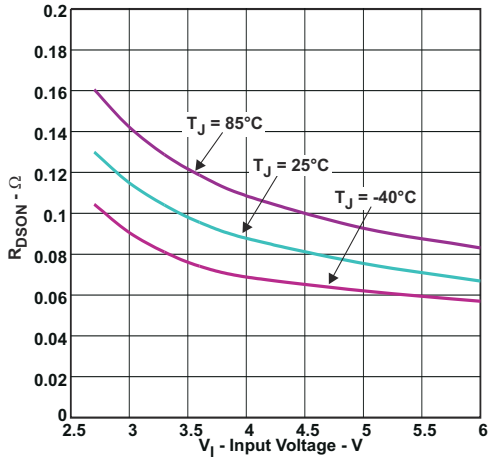


图 7-5. R_{DSON} High-Side Switch

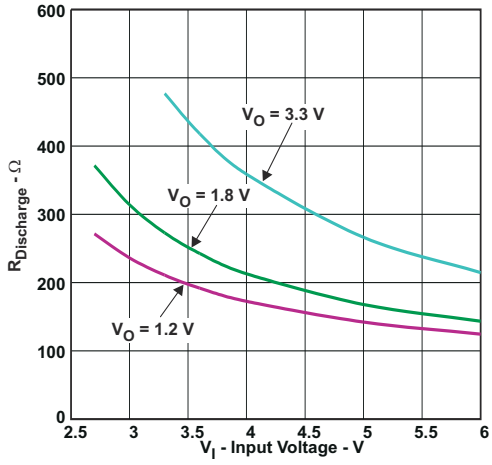


图 7-6. $R_{discharge}$ vs Input Voltage

8 Detailed Description

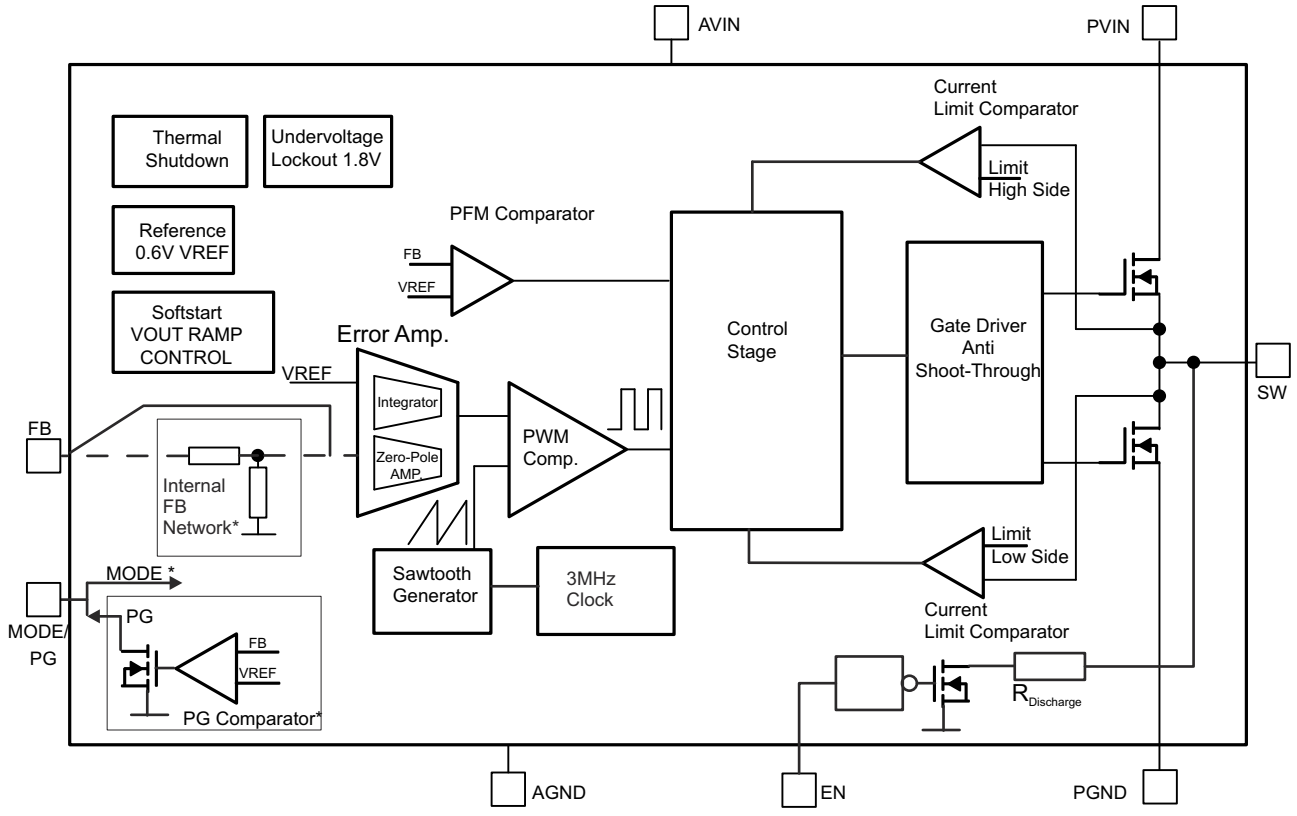
8.1 Overview

The TPS6206x step down converter operates with typically 3-MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converter can automatically enter power save mode and operates then in pulse frequency modulation (PFM) mode.

During PWM operation the converter use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows now from the input capacitor through the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic will turn off the switch. The current limit comparator will also turn off the switch in case the current limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier..

The next cycle will be initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

8.2 Functional Block Diagram



* Function depends on device option

8.3 Feature Description

8.3.1 Mode Selection (TPS62065)

The MODE pin allows mode selection between forced PWM mode and power save mode.

Connecting this pin to GND enables the power save mode with automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

In device options where the MODE pin is replaced with power good output, the power save mode is enabled per default.

8.3.2 Power Good Output (TPS62067)

This function is available in the TPS62067. The power good output is an open-drain output and requires an external pullup resistor. The circuit is active once the device is enabled and AVIN is above the undervoltage lockout threshold V_{UVLO}. It is driven by an internal comparator connected to the FB voltage. The PG output provides a high level once the feedback voltage exceeds typically 95% of its nominal value. The PG output is driven to low level once the feedback voltage falls below typically 90% of its nominal value. The PG output is activated with an internal delay of 5 µs.

The PG open-drain output transistor is turned on immediately with EN = Low level and pulls the output low. The external pullup resistor can be connected to any voltage rail lower or equal the voltage applied to AVIN of the device. The value of the pullup resistor must be carefully selected to limit the current into the PG pin to maximum 1 mA. The external pullup resistor can be connected to VOUT or another voltage rail which does not exceed the V_{IN} level. The current flowing through the pullup resistor impacts the current consumption of the application circuit in shutdown mode.

The shutdown current of the device does not include the current through the external pullup and internal open-drain stage. The PG signal can be used for sequencing various converters or to reset a microcontroller.

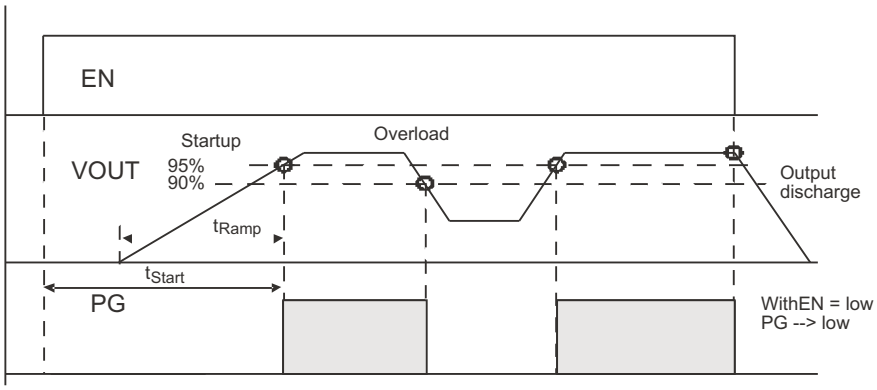


图 8-1. Power Good Output Pg

8.3.3 Enable

The device is enabled by setting EN pin to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltages reaches 95% of its nominal value within t_{START} of typically 500 µs after the device has been enabled. The EN input can be used to control power sequencing in a system with various DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode. In this mode, all circuits are disabled and the SW pin is connected to PGND through an internal resistor to discharge the output.

8.3.4 Clock Dithering

To reduce the noise level of switch frequency harmonics in the higher RF bands, the TPS6206x family has a built-in clock-dithering circuit. The oscillator frequency is slightly modulated with a sub clock causing a clock dither of typically 6 ns.

8.3.5 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling V_{IN} trips the undervoltage lockout threshold V_{UVLO}. The undervoltage lockout threshold V_{UVLO} for falling V_{IN} is typically 1.78 V. The device starts operation once the rising V_{IN} trips undervoltage lockout threshold V_{UVLO} again at typically 1.95 V.

8.3.6 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation with a soft start once the junction temperature falls below the thermal shutdown hysteresis.

8.4 Device Functional Modes

8.4.1 Soft Start

The TPS6206x has an internal soft start circuit that controls the ramp up of the output voltage. Once the converter is enabled and the input voltage is above the undervoltage lockout threshold V_{UVLO} the output voltage ramps up from 5% to 95% of its nominal value within t_{Ramp} of typically 250 µs.

This limits the inrush current in the converter during start-up and prevents possible input voltage drops when a battery or high impedance power source is used.

During soft start, the switch current limit is reduced to 1/3 of its nominal value I_{LIMF} until the output voltage reaches 1/3 of its nominal value. Once the output voltage trips this threshold, the device operates with its nominal current limit I_{LIMF}.

8.4.2 Power Save Mode

At TPS62065 pulling the MODE pin low enables power save mode. In TPS62067 power save mode is enabled per default. If the load current decreases, the converter enters power save mode operation automatically. During power save mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage typically +1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the power save mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of $V_{OUTnominal}$ +1%, the device starts a PFM current pulse. For this the high-side MOSFET switch will turn on and the inductor current ramps up. After the on-time expires the switch will be turned off and the low-side MOSFET switch will be turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typically 18 µA current consumption.

In case the output voltage is still below the PFM comparator threshold, further PFM current pulses will be generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold due to the load current.

The PFM mode is exited and PWM mode entered in case the output current can no longer be supported in PFM mode.

8.4.3 Dynamic Voltage Positioning

This feature reduces the voltage undershoots and overshoots at load steps from light to heavy load and vice versa. It is active in power save mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

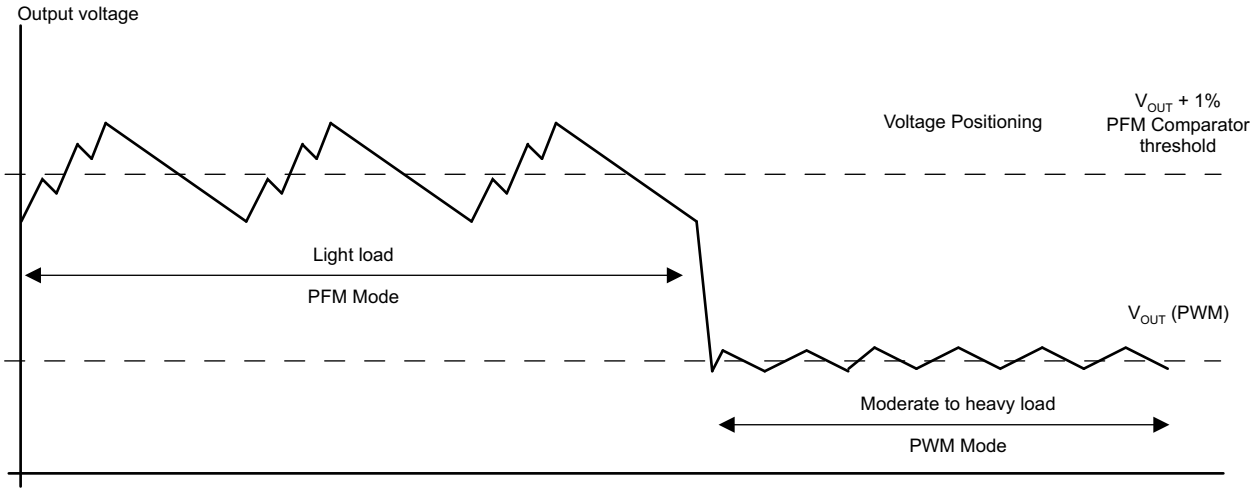


图 8-2. Power Save Mode Operation with Automatic Mode Transition

8.4.4 100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode as the input voltage comes close to the nominal output voltage. To maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing V_{IN} the high-side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_O max + I_O max \times (R_{DS(on)} max + R_L) \quad (1)$$

where

- $I_O$max = maximum output current
- $R_{DS(on)}$max = maximum P-channel switch $R_{DS(on)}$
- R_L = DC resistance of the inductor
- $V_O$max = nominal output voltage plus maximum output voltage tolerance

8.4.5 Internal Current Limit and Fold-Back Current Limit for Short Circuit Protection

During normal operation the high-side and low-side MOSFET switches are protected by its current limits I_{LIMF}. Once the high-side MOSFET switch reaches its current limit, it is turned off and the low-side MOSFET switch is turned on. The high-side MOSFET switch can only turn on again, once the current in the low-side MOSFET switch decreases below its current limit I_{LIMF}. The device is capable to provide peak inductor currents up to its internal current limit$_{ILIMF.}$.

As soon as the switch current limits are hit and the output voltage falls below 1/3 of the nominal output voltage due to overload or short circuit condition, the foldback current limit is enabled. In this case the switch current limit is reduced to 1/3 of the nominal value I_{LIMF}.

Due to the short circuit protection is enabled during start-up, the device does not deliver more than 1/3 of its nominal current limit I_{LIMF} until the output voltage exceeds 1/3 of the nominal output voltage. This needs to be considered when a load is connected to the output of the converter, which acts as a current sink.

8.4.6 Output Capacitor Discharge

With EN = GND, the device enters shutdown mode and all internal circuits are disabled. The SW pin is connected to PGND through an internal resistor to discharge the output capacitor. This feature ensures a startup in a discharged output capacitor once the converter is enabled again and prevents "floating" charge on the output capacitor. The output voltage ramps up monotonic starting from 0 V.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS62065 and TPS62067 are highly efficient synchronous step down DC/DC converters providing up to 2-A output current.

9.2 Typical Application

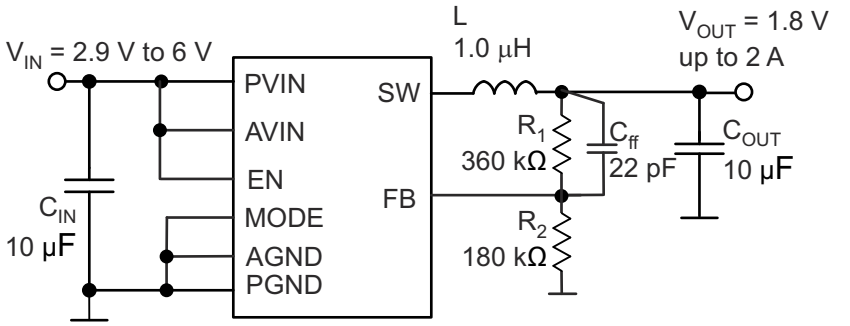


图 9-1. TPS62065 1.8-V Adjustable Output Voltage Configuration

9.2.1 Design Requirements

The device operates over an input voltage range from 2.9 V to 6 V. The output voltage is adjustable using an external feedback divider.

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Setting

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \qquad R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \tag{2}$$

with an internal reference voltage V_{REF} typically 0.6 V.

To minimize the current through the feedback divider network, R_2 should be within the range of 120 kΩ to 360 kΩ. The sum of R_1 and R_2 should not exceed approximately 1 MΩ, to keep the network robust against noise. An external feed-forward capacitor C_{ff} is required for optimum regulation performance. Lower resistor values can be used. R_1 and C_{ff} places a zero in the loop. The right value for C_{ff} can be calculated as:

$$f_z = \frac{1}{2 \times \pi \times R_1 \times C_{ff}} = 25\ \text{kHz} \tag{3}$$

$$C_{ff} = \frac{1}{2 \times \pi \times R_1 \times 25\ \text{kHz}} \tag{4}$$

9.2.2.2 Output Filter Design (Inductor and Output Capacitor)

The internal compensation network of TPS6206x is optimized for a LC output filter with a corner frequency of:

$$f_c = \frac{1}{2 \times \pi \times \sqrt{(1\mu H \times 10\mu F)}} = 50kHz \quad (5)$$

The device operates with nominal inductors of 1 µH to 1.2 µH and with 10 µF to 22 µF small X5R and X7R ceramic capacitors. Refer to the lists of inductors and capacitors. The device is optimized for a 1-µH inductor and 10-µF output capacitor.

9.2.2.2.1 Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

方程式 6 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with 方程式 7. This is recommended because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (6)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (7)$$

where

- f = Switching frequency (3 MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current

A more conservative approach is to select the inductor current rating just for the switch current limit I_{LIMF} of the converter.

The total losses of the coil have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the DC resistance $R_{(DC)}$ and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

表 9-1. List of Inductors

DIMENSIONS (mm^3)	INDUCTANCE (µ H)	INDUCTOR TYPE	SUPPLIER
3.2 × 2.5 × 1 maximum	1	LQM32PN (MLCC)	Murata
3.7 × 4 × 1.8 maximum	1	LQH44 (wire wound)	Murata
4 × 4 × 2.6 maximum	1.2	NRG4026T (wire wound)	Taiyo Yuden
3.5 × 3.7 × 1.8 maximum	1.2	DE3518 (wire wound)	TOKO

9.2.2.2.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS6206x allows the use of tiny ceramic capacitors. TI recommends ceramic capacitors with low ESR values that have the lowest output voltage ripple.

The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies and may not be used. For most applications a nominal 10-µF or 22-µF capacitor is suitable. At small ceramic capacitors, the DC-bias effect decreases the effective capacitance. Therefore a 22-µF capacitor can be used for output voltages higher than 2 V, see list of capacitors.

In case additional ceramic capacitors in the supplied system are connected to the output of the DC/DC converter, the output capacitor C_{OUT} must be decreased in order not to exceed the recommended effective capacitance range. In this case a loop stability analysis must be performed as described later.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSCout} = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (8)$$

9.2.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, TI recommends a 10-µF ceramic capacitor. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or VIN step on the input can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

表 9-2. List of Capacitors

CAPACITANCE	TYPE	SIZE (mm^3)	SUPPLIER
10 µ F	GRM188R60J106M	0603: 1.6 x 0.8 x 0.8	Murata
22 µ F	GRM188R60G226M	0603: 1.6 x 0.8 x 0.8	Murata
22µF	CL10A226MQ8NRNC	0603: 1.6 x 0.8 x 0.8	Samsung
10µF	CL10A106MQ8NRNC	0603: 1.6 x 0.8 x 0.8	Samsung

9.2.2.3 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signal

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that must be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or wrong L-C output filter combinations. As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turnon of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta_{I(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta_{I(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode at medium to high load currents.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot, or ringing; that helps evaluate stability of the converter. Without any ringing, the loop has usually more than 45° of phase margin.

9.2.3 Application Curves

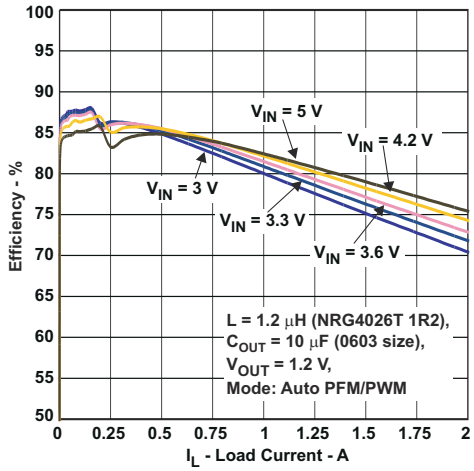


图 9-2. V_{OUT} = 1.2 V, Auto PFM/PWM Mode, Linear Scale

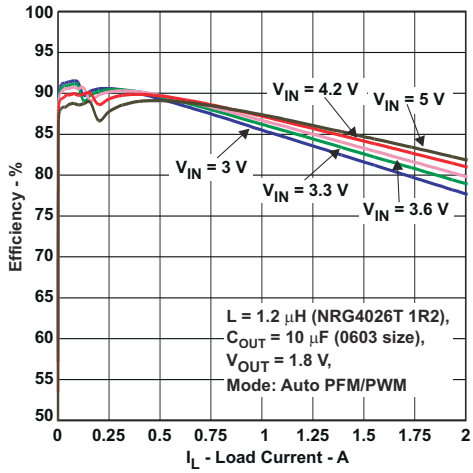


图 9-3. V_{OUT} = 1.8 V, Auto PFM/PWM Mode, Linear Scale

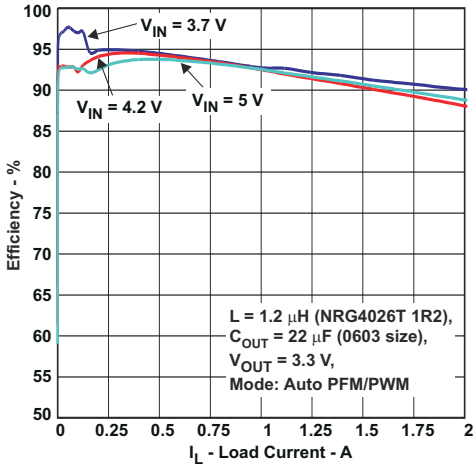


图 9-4. V_{OUT} = 3.3 V, Auto PFM/PWM Mode, Linear Scale

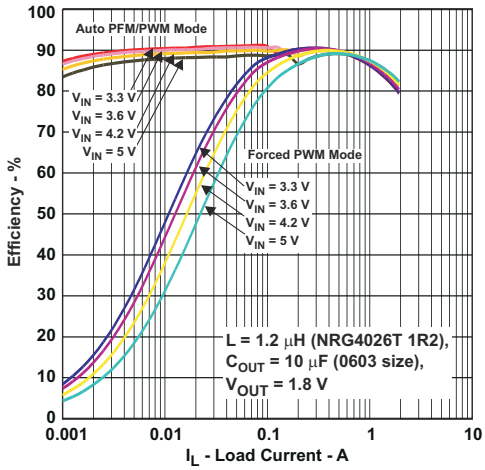


图 9-5. Auto PFM/PWM Mode vs. Forced PWM Mode, Logarithmic Scale

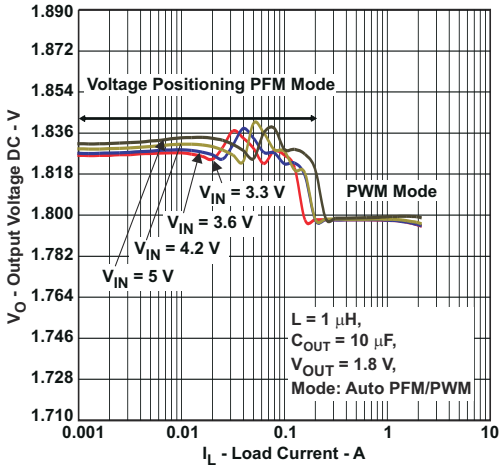


图 9-6. Auto PFM/PWM Mode

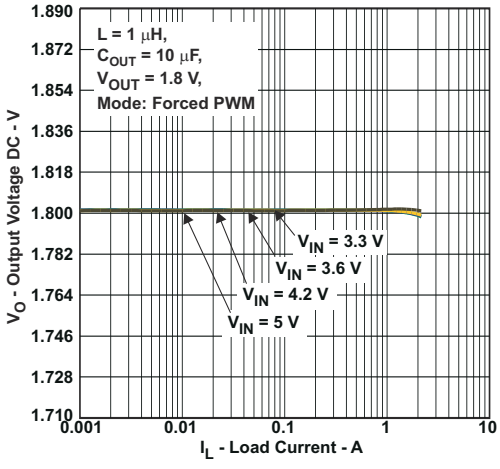


图 9-7. Forced PWM Mode

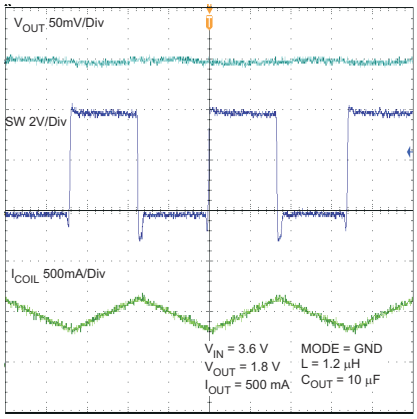


图 9-8. Typical Operation (PWM Mode)

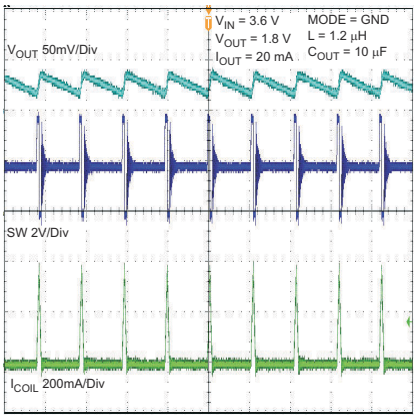


图 9-9. Typical Operation (PFM Mode)

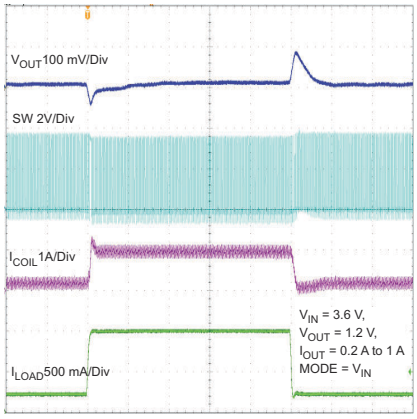


图 9-10. Load Transient Response PWM Mode 0.2 A to 1 A

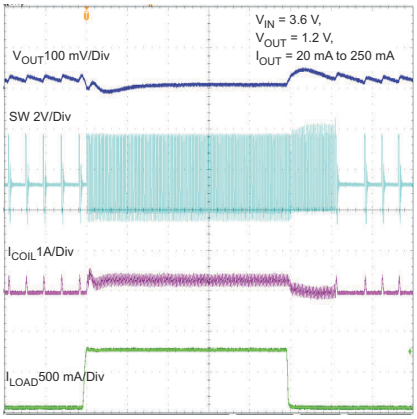


图 9-11. Load Transient PFM Mode 20 mA to 250 mA

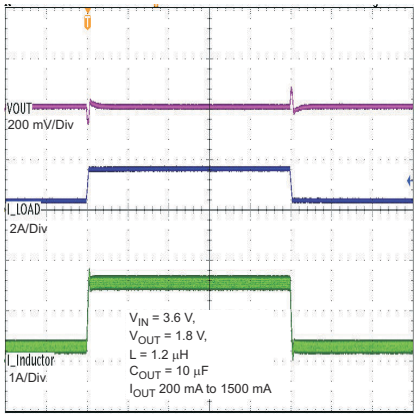


图 9-12. Load Transient Response 200 mA to 1500 mA

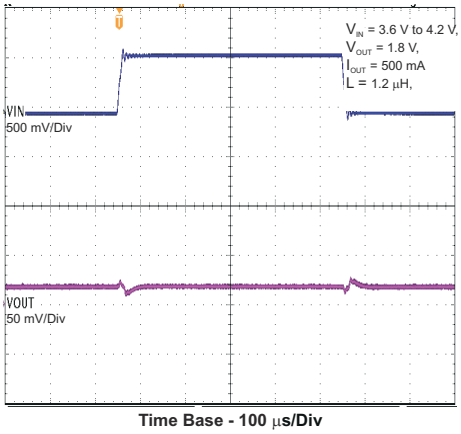


图 9-13. Line Transient Response PWM Mode

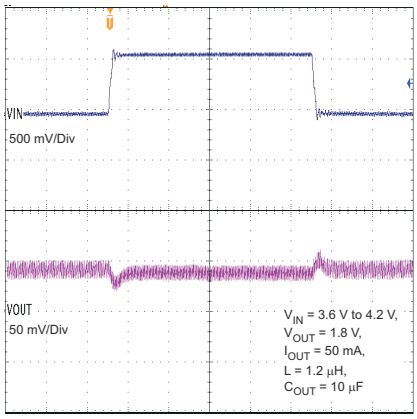


图 9-14. Line Transient PFM Mode

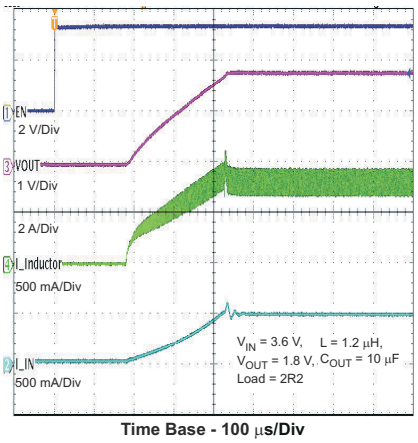


图 9-15. Startup Into Load – V_{OUT} 1.8 V

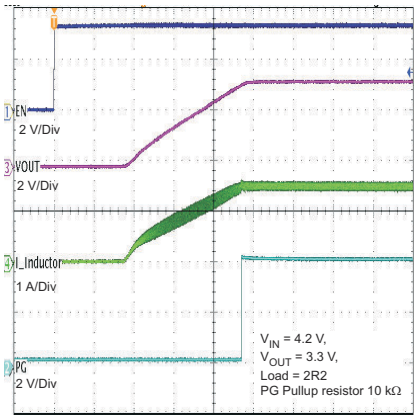


图 9-16. Start-up TPS62067 Into 2.2-Ω Load With Power Good

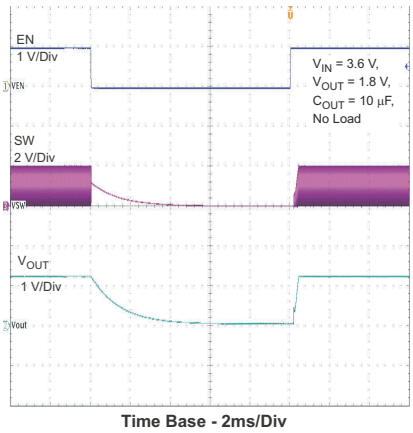


图 9-17. Output Discharge

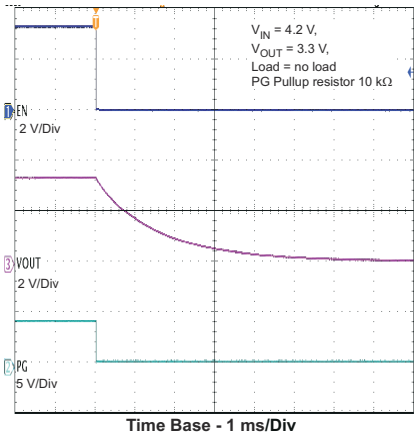


图 9-18. Shutdown TPS62067

9.3 System Example

The TPS62067 provides an open-drain power good output, refer to 节 8.3.2.

9.3.1 TPS62067 Adjustable 1.8-V Output

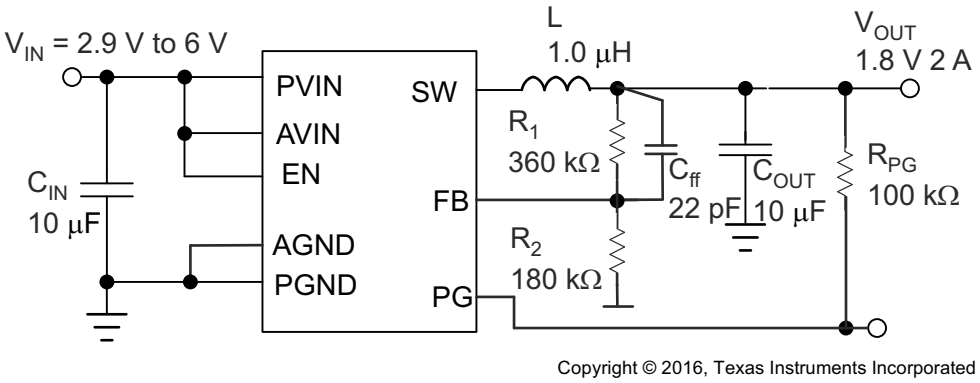


图 9-19. TPS62067 Adjustable 1.8-V Output

10 Power Supply Recommendations

The power supply to the TPS6206x must have a current rating according to the supply voltage, output voltage, and output current of the TPS6206x.

11 Layout

11.1 Layout Guidelines

Take care in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI and thermal problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the AGND and PGND pins of the device to the PowerPAD™ land of the PCB and use this pad as a star point. Use a common power PGND node and a different node for the signal AGND to minimize the effects of ground noise. The FB divider network should be connected right to the output capacitor and the FB line must be routed away from noisy components and traces (for example, SW line).

Due to the small package of this converter and the overall small solution size the thermal performance of the PCB layout is important. To get a good thermal performance, TI recommends a four or more Layer PCB design. The PowerPAD™ of the IC must be soldered on the power pad area on the PCB to get a proper thermal connection. For good thermal performance the PowerPAD™ on the PCB needs to be connected to an inner GND plane with sufficient via connections. Refer to the documentation of the evaluation kit.

11.2 Layout Example

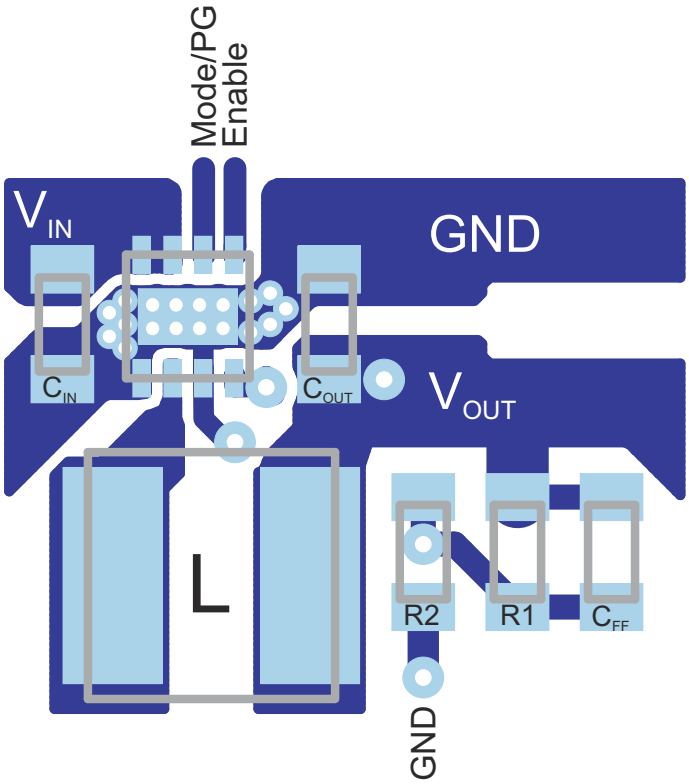


图 11-1. PCB Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62065	Click here	Click here	Click here	Click here	Click here
TPS62067	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62065DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OFA
TPS62065DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFA
TPS62065DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OFA
TPS62065DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFA
TPS62065DSGTG4	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFA
TPS62065DSGTG4.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFA
TPS62067DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ODH
TPS62067DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ODH
TPS62067DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ODH
TPS62067DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ODH
TPS62067DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ODH
TPS62067DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ODH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS62065, TPS62067 :

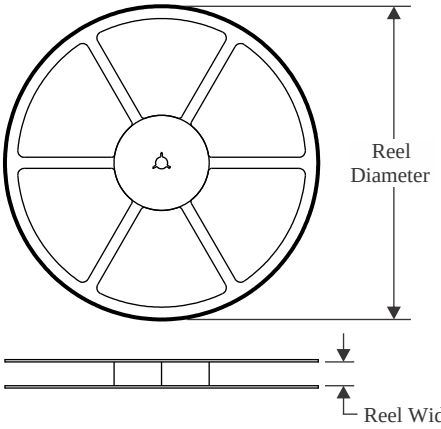
- Automotive : TPS62065-Q1, TPS62067-Q1

NOTE: Qualified Version Definitions:

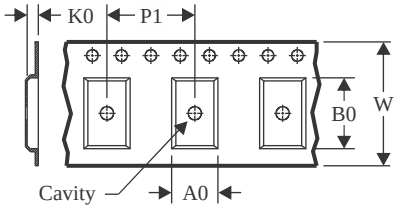
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

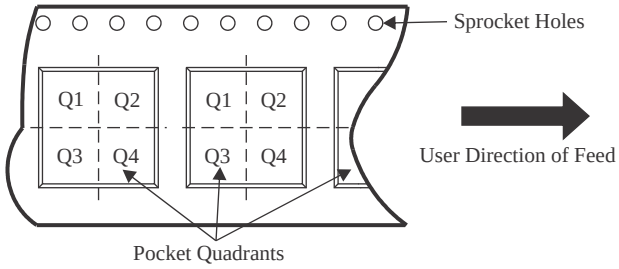


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

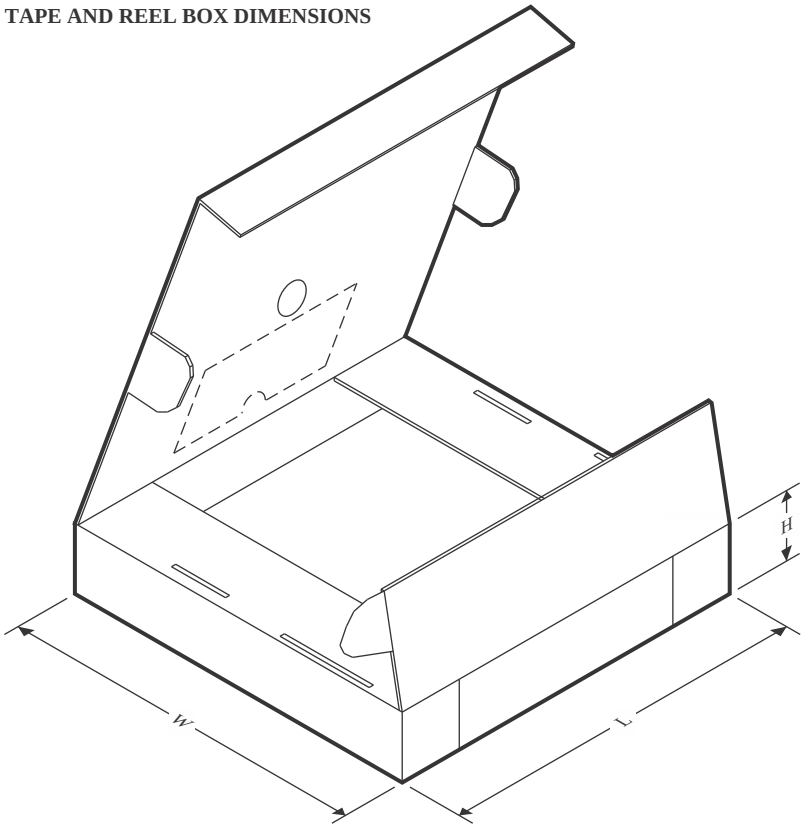
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62065DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62065DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62065DSGTG4	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62067DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62067DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62067DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62065DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62065DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS62065DSGTG4	WSON	DSG	8	250	210.0	185.0	35.0
TPS62067DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62067DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62067DSGT	WSON	DSG	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

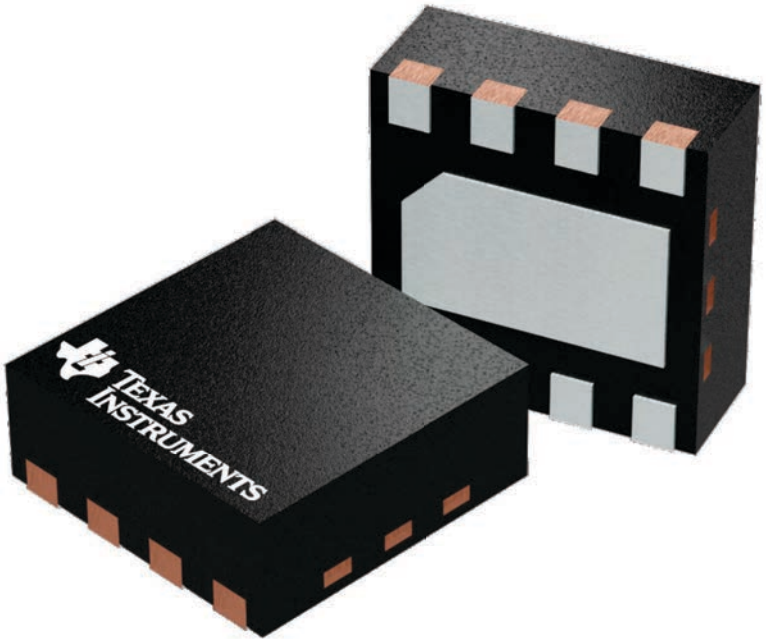
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



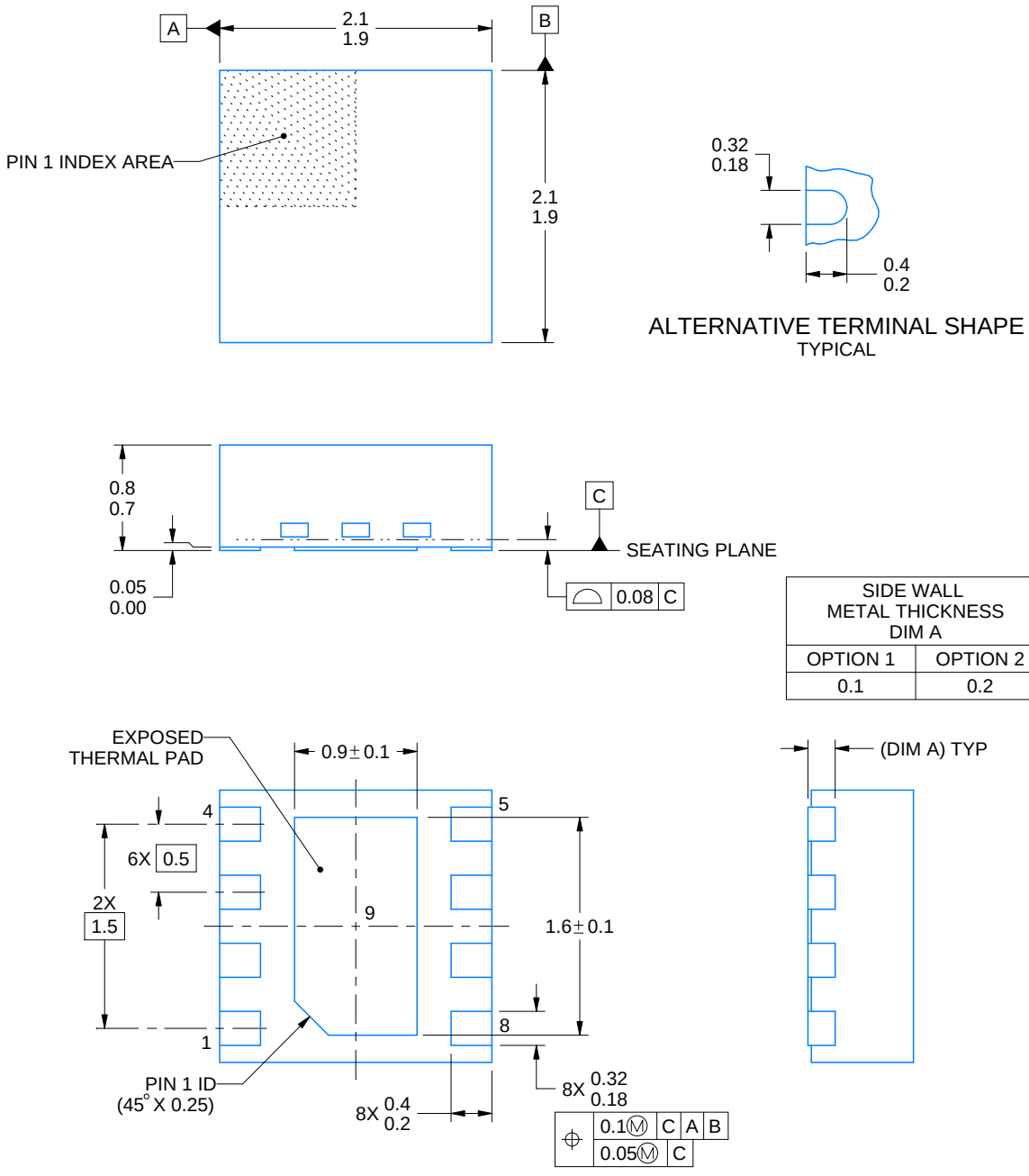
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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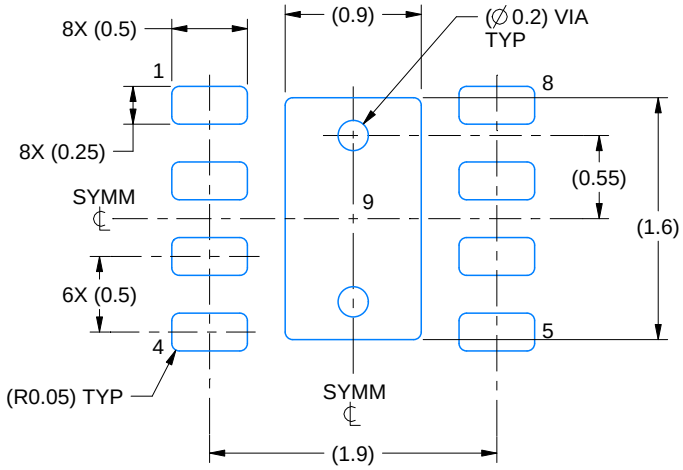
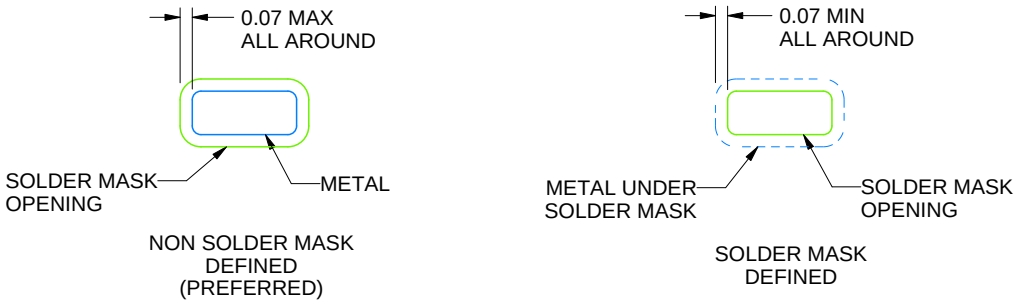
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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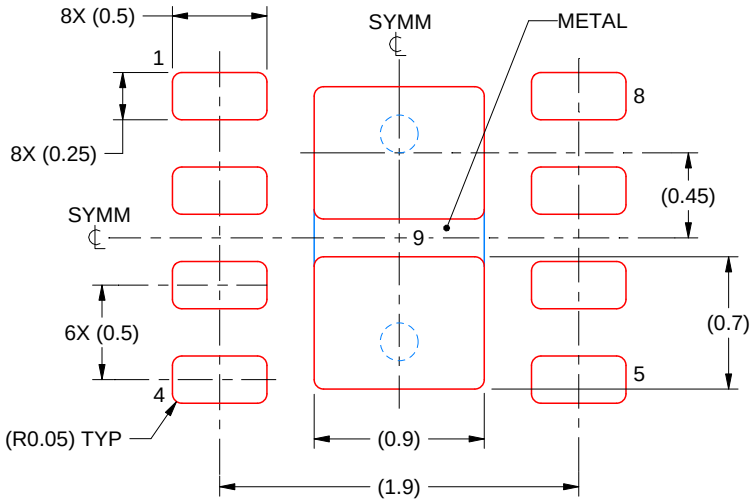
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月