

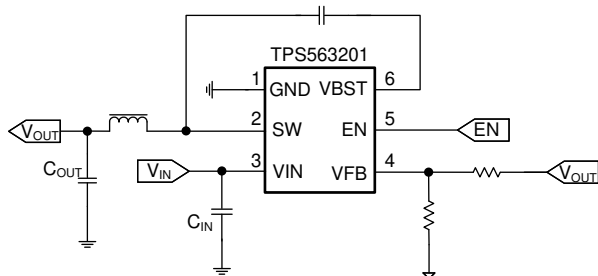
TPS56320x 采用 SOT-23 封装的 4.5V 至 17V 输入、3A 同步降压稳压器

1 特性

- TPS563201 和 TPS563208 3A 转换器集成了 95mΩ 和 57mΩ FET
- D-CAP2™ 控制方案，可提供快速瞬态响应
- 输入电压范围：4.5V 至 17V
- 输出电压范围：0.76V 至 7V
- 脉冲跳跃模式 (TPS563201) 或持续电流模式 (TPS563208)
- 580kHz 开关频率
- 低关断电流 (低于 20μA)
- 2% 反馈电压精度 (25°C)
- 从预偏置输出电压启动
- 逐周期过流限制
- 断续模式过流保护
- 非锁存 UVP 和 TSD 保护
- 固定软启动：1.0ms
- 使用 TPS56320x 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 数字电视电源
- 高清蓝光™光盘播放器
- 网络家庭终端设备
- 数字机顶盒 (STB)
- 安全监控



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简化原理图

3 说明

TPS563201 和 TPS563208 是采用小外形尺寸晶体管 (SOT)-23 封装的简单易用型 3A 同步降压转换器。

这些器件的设计初衷是使用尽可能少的外部元件即可运行，还可以实现低待机电流。

这些开关模式电源 (SMPS) 器件采用 D-CAP2 控制拓扑，从而提供快速瞬态响应，并且在无需外部补偿元件的情况下支持专用聚合物等低等效串联电阻 (ESR) 输出电容器以及超低 ESR 陶瓷电容器。

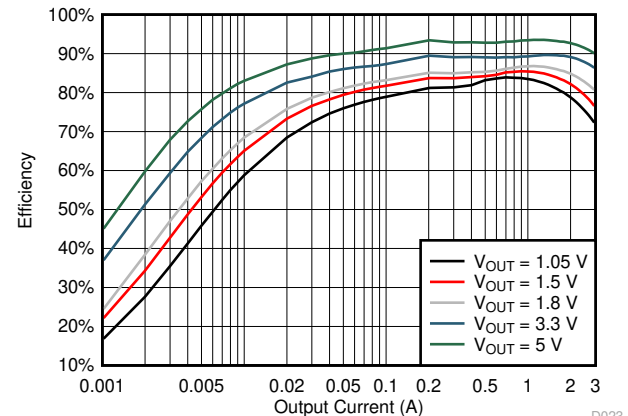
TPS563201 可在脉冲跳跃模式下运行，从而能在轻载运行期间保持高效率。TPS563201 和 TPS563208 采用 6 引脚 1.6mm × 2.9mm SOT (DDC) 封装，额定结温范围为 -40°C 至 125°C。

器件信息

器件型号	模式	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
TPS563201	ECO	DDC (SOT , 6)	1.6mm x 2.9mm
TPS563208	FCCM		

(1) 如需更多信息，请参阅节 10。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



TPS563201 效率

D023



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4 Pin Configuration and Functions

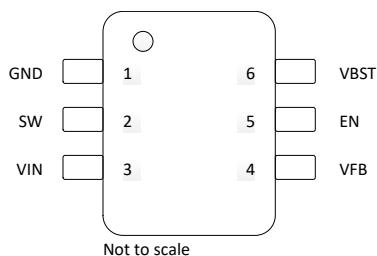


图 4-1. DDC Package 6-Pin SOT Top View

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
GND	1	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 μ F capacitor between VBST and SW pins.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	VIN, EN	– 0.3	19	V
	VBST	– 0.3	25	V
	VBST (10 ns transient)	– 0.3	27	V
	VBST (vs SW)	– 0.3	6	V
	VFB	– 0.3	6	V
	SW	– 2	19	V
	SW (10 ns transient)	– 3.5	21	V
Operating junction temperature, T _J		– 40	150	°C
Storage temperature, T _{stg}		– 55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Supply input voltage range	4.5		17	V
V _I	Input voltage range	VBST		23	V
		VBST (10 ns transient)		26	
		VBST (vs SW)		5.5	
		EN		17	
		VFB		5.5	
		SW		17	
		SW (10 ns transient)		20	
T _J	Operating junction temperature	– 40		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS56320x	UNIT
		DDC (SOT)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{VIN}	Operating – non-switching supply current	V _{IN} current, EN = 5 V, V _{FB} = 0.9 V	TPS563201	120	200	μA
			TPS563208	350	500	
I _{VINSDN}	Shutdown supply current	V _{IN} current, EN = 0 V		8	20	μA
LOGIC THRESHOLD						
V _{ENH}	EN high-level input voltage		1.6			V
V _{ENL}	EN low-level input voltage				0.8	V
R _{EN}	EN pin resistance to GND	V _{EN} = 1.5 V	600	1500	2400	k Ω
I _{EN}	EN pulldown current	V _{EN} = 1.5 V		1		μA
V _{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V _{FBTH}	V _{FB} threshold voltage ⁽¹⁾	V _O = 1.05 V, I _O = 10 mA, Eco-mode operation		774		mV
	V _{FB} threshold voltage	V _O = 1.05 V, continuous mode operation	749	768	787	mV
I _{VFB}	V _{FB} input current	V _{FB} = 0.8 V		0	±0.1	μA
MOSFET						
R _{DS(on)h}	High-side switch resistance	T _A = 25°C, V _{BST} – SW = 5 V		95		m Ω
R _{DS(on)l}	Low-side switch resistance	T _A = 25°C		57		m Ω
CURRENT LIMIT						
I _{ocl}	Current limit	DC current, V _{OUT} = 1.05 V, L ₁ = 1.5 μH	3.3	4.2	5.1	A
THERMAL SHUTDOWN						
T _{SDN}	Thermal shutdown threshold ⁽¹⁾	Shutdown temperature		172		°C
		Hysteresis		37		
ON-TIME TIMER CONTROL						
t _{OFF(MIN)}	Minimum off time	V _{FB} = 0.5 V		220	310	ns
SOFT START						
T _{ss}	Soft-start time	Internal soft-start time		1.0		ms
FREQUENCY						
F _{sw}	Switching frequency	V _{IN} = 12 V, V _O = 3.3 V, I _O = 1 A		580		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V _{UVP}	Output UVP threshold	Hiccup detect (H > L)		65%		
T _{HICCUP_WAIT}	Hiccup on time			1.2		ms
T _{HICCUP_RE}	Hiccup time before restart			10		ms
UVLO						
UVLO	UVLO threshold	Wake up VIN voltage		3.8	4.3	V
		Shutdown VIN voltage		3.3	3.4	
		Hysteresis VIN voltage		0.4		

(1) Not production tested.

5.6 Typical Characteristics

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

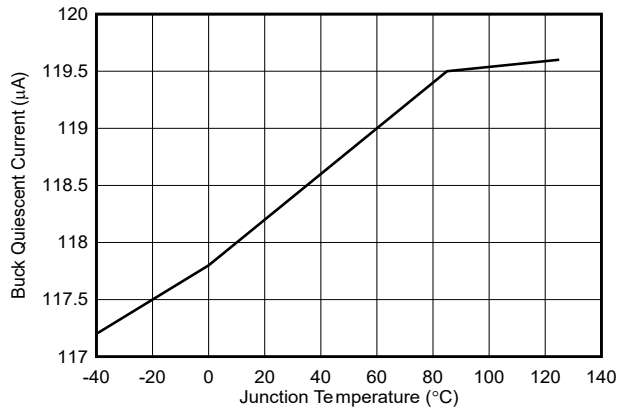


图 5-1. TPS563201 Supply Current vs Junction Temperature

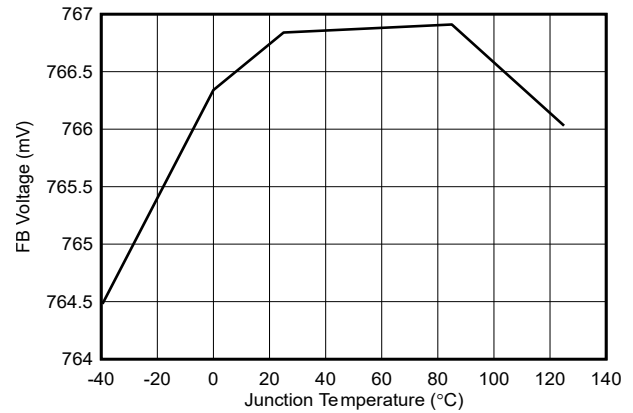


图 5-2. VFB Voltage vs Junction Temperature

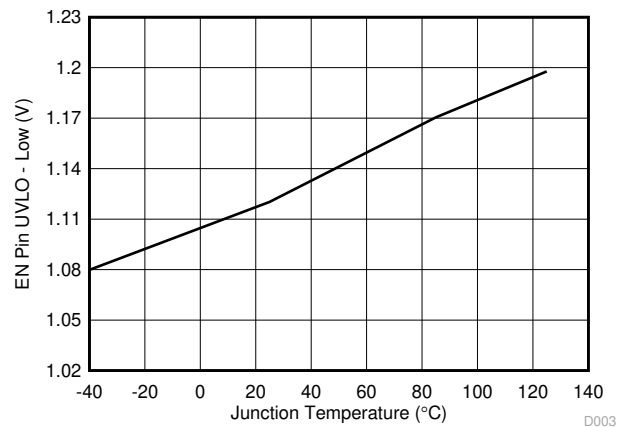


图 5-3. EN Pin UVLO Low Voltage vs Junction Temperature

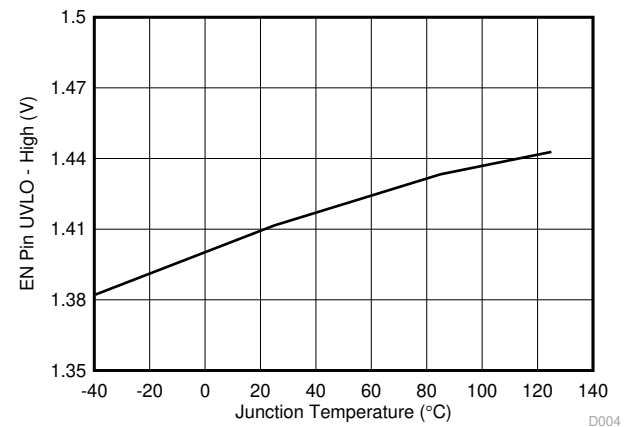


图 5-4. EN Pin UVLO High Voltage vs Junction Temperature

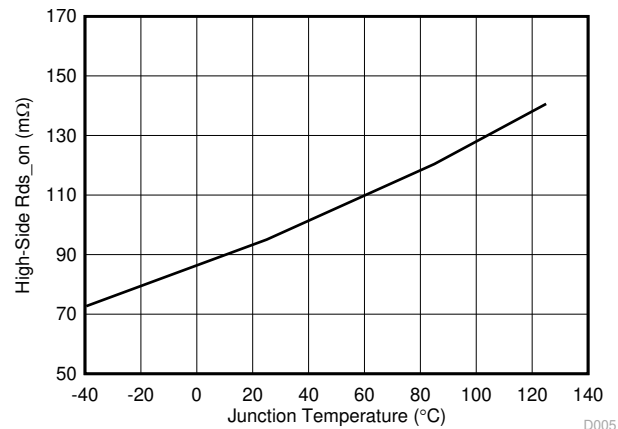


图 5-5. High-Side R_{ds-On} vs Junction Temperature

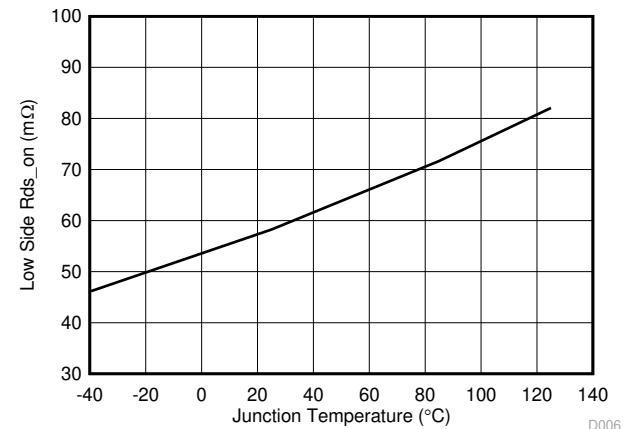


图 5-6. Low-Side R_{ds-On} vs Junction Temperature

5.6 Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

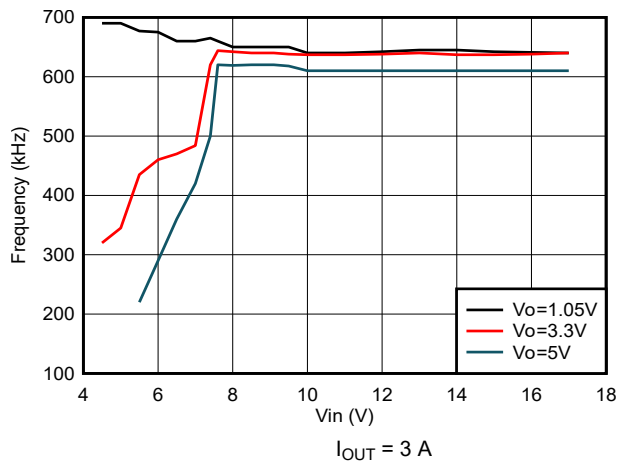


图 5-7. TPS563208 Switching Frequency vs Input Voltage

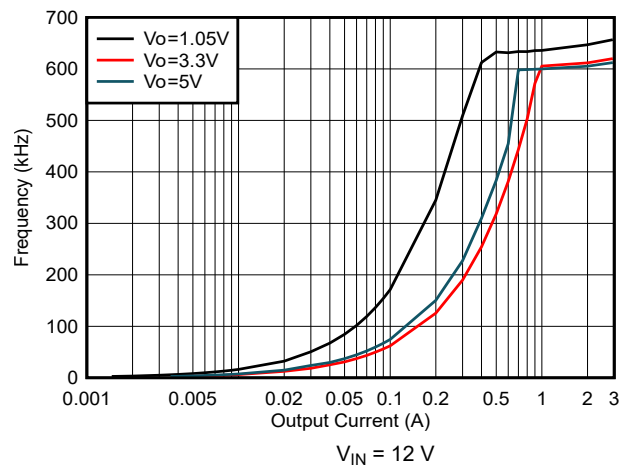


图 5-8. TPS563201 Switching Frequency vs Output Current

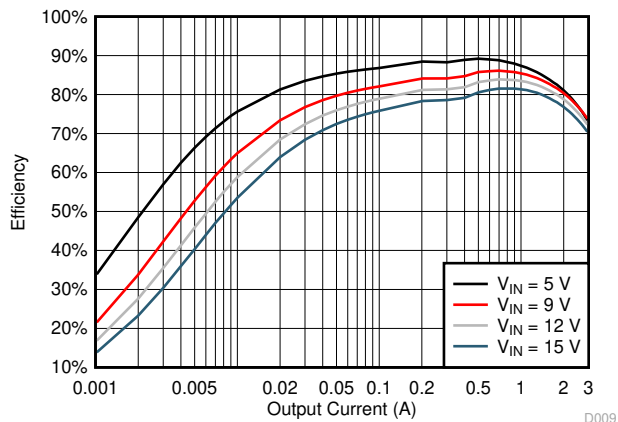


图 5-9. TPS563201 $V_{OUT} = 1.05\text{ V}$ Efficiency, $L = 2.2\text{ }\mu\text{H}$

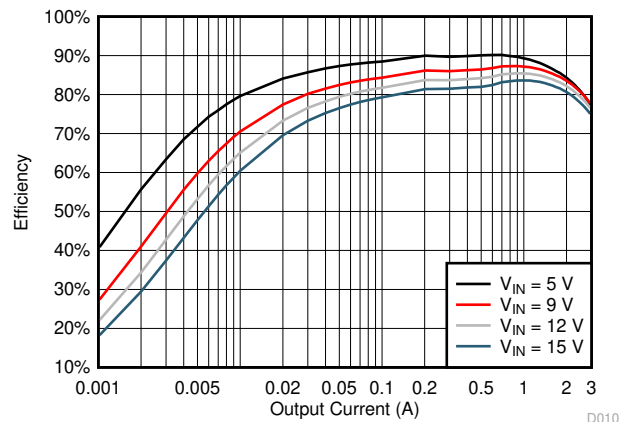


图 5-10. TPS563201 $V_{OUT} = 1.5\text{ V}$ Efficiency, $L = 2.2\text{ }\mu\text{H}$

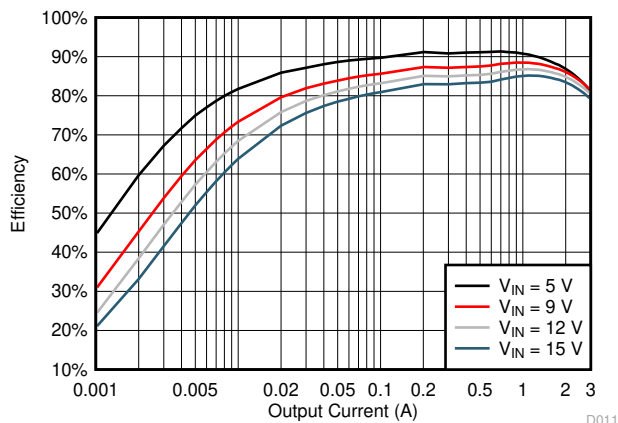


图 5-11. TPS563201 $V_{OUT} = 1.8\text{ V}$ Efficiency, $L = 2.2\text{ }\mu\text{H}$

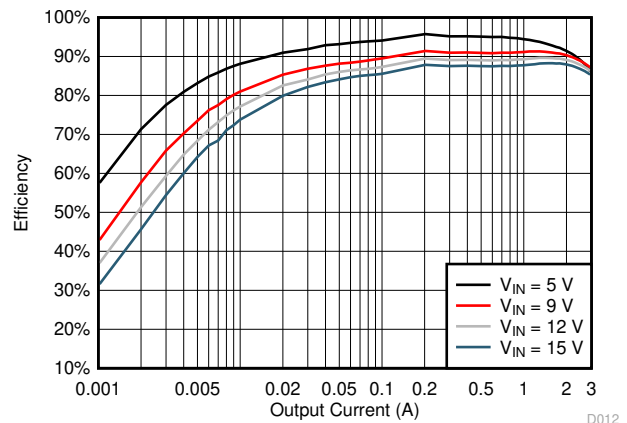


图 5-12. TPS563201 $V_{OUT} = 3.3\text{ V}$ Efficiency, $L = 2.2\text{ }\mu\text{H}$

5.6 Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

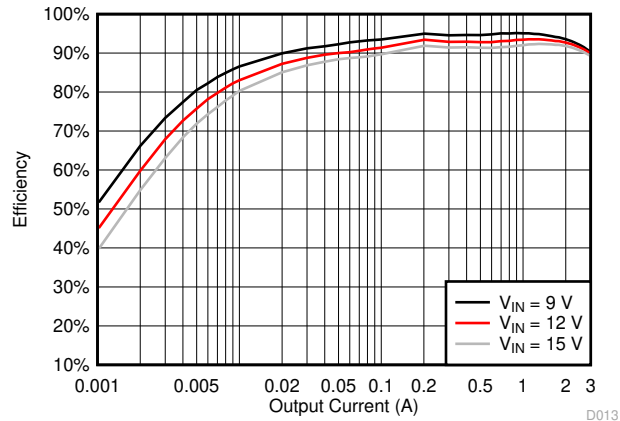


图 5-13. TPS563201 $V_{OUT} = 5\text{ V}$ Efficiency, $L = 3.3\text{ }\mu\text{H}$

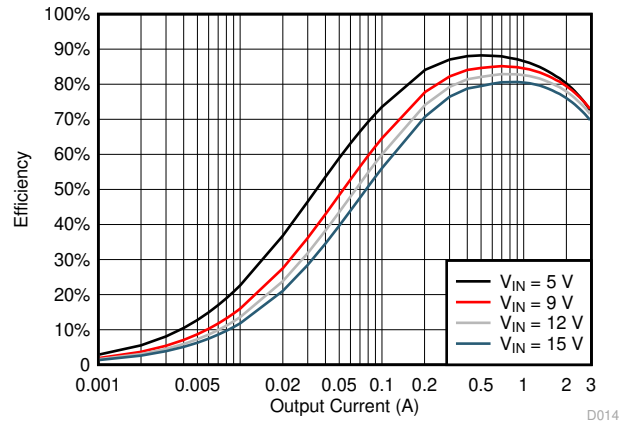


图 5-14. TPS563208 $V_{OUT} = 1.05\text{ V}$ Efficiency, $L = 2.2\text{ }\mu\text{H}$

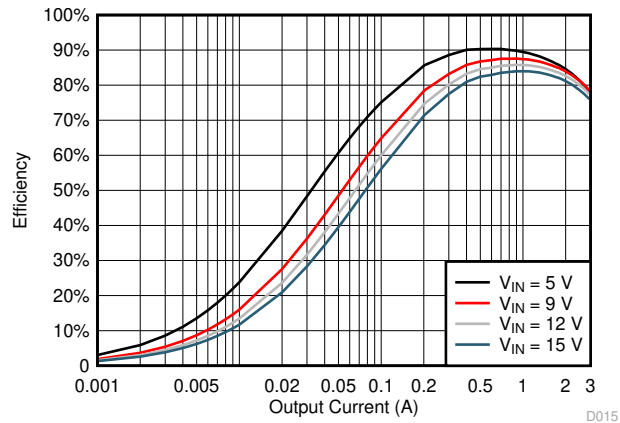


图 5-15. TPS563208 $V_{OUT} = 1.5\text{ V}$ Efficiency, $L = 2.2\text{ }\mu\text{H}$

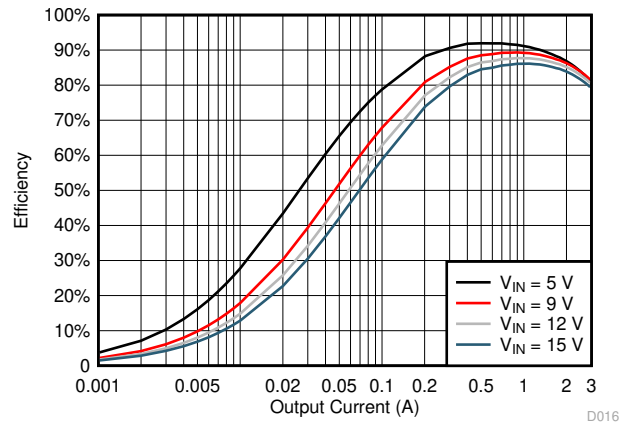


图 5-16. TPS563208 $V_{OUT} = 1.8\text{ V}$ Efficiency, $L = 2.2\text{ }\mu\text{H}$

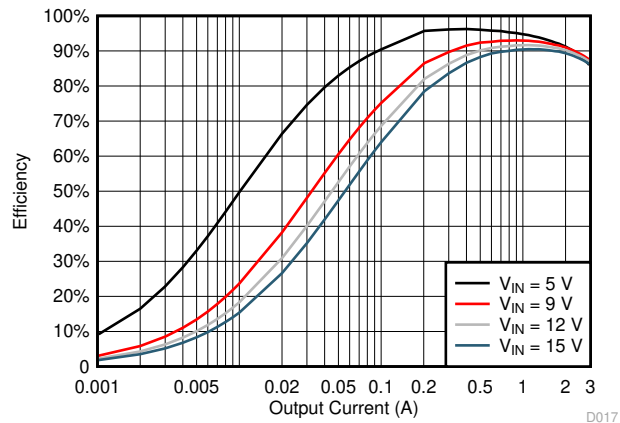


图 5-17. TPS563208 $V_{OUT} = 3.3\text{ V}$ Efficiency, $L = 2.2\text{ }\mu\text{H}$

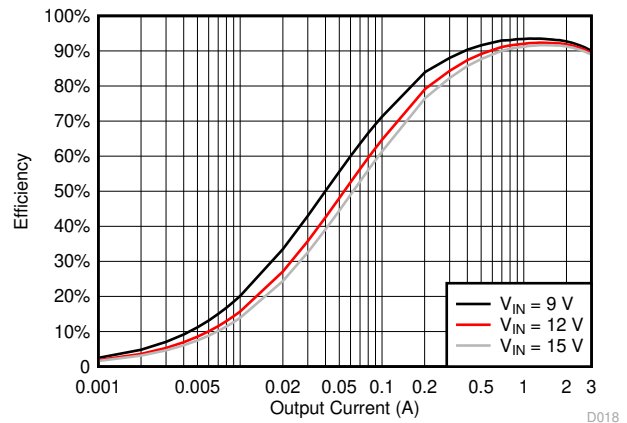


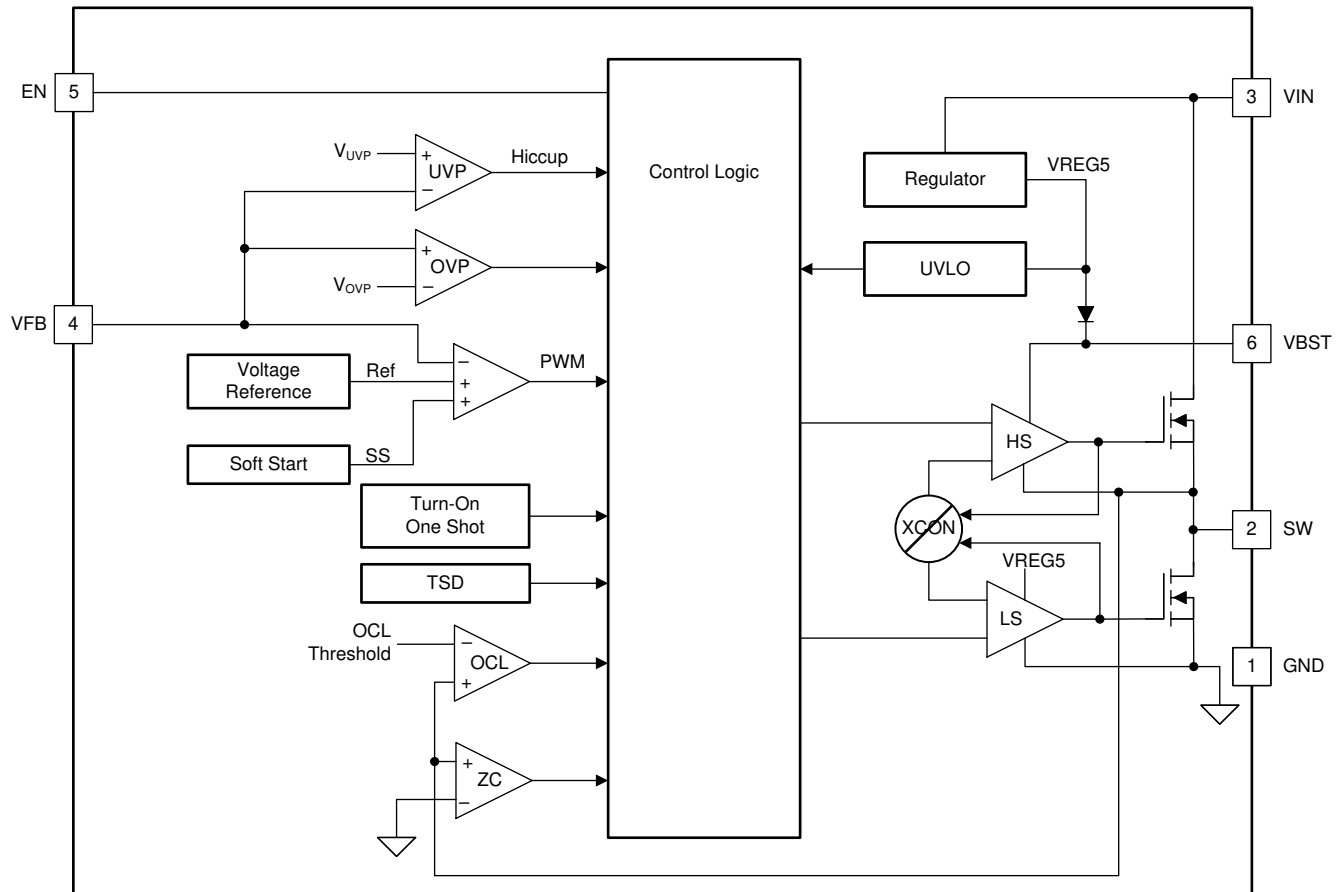
图 5-18. TPS563208 $V_{OUT} = 5\text{ V}$ Efficiency, $L = 3.3\text{ }\mu\text{H}$

6 Detailed Description

6.1 Overview

The TPS563201 and TPS563208 are 3-A synchronous step-down converters. The proprietary D-CAP2 control scheme supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2 control scheme can reduce the output capacitance required to meet a specific level of performance.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS563201 and TPS563208 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 control scheme. The D-CAP2 control scheme combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set proportional to the converter input voltage, V_{IN} , and inversely proportional to the output voltage, V_O , to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 control scheme.

6.3.2 Pulse Skip Control (TPS563201)

The TPS563201 is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in [方程式 1](#).

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

6.3.3 Soft Start and Pre-Biased Soft Start

The TPS563201 and TPS563208 have an internal 1-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB} . This scheme ensures that the converters ramp up smoothly into regulation point.

6.3.4 Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{in} , V_{out} , the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{out} . If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the V_{FB} voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 256 μ s) and re-start after the hiccup time (typically 10 ms).

When the over current condition is removed, the output voltage returns to the regulated value.

6.3.5 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

6.3.6 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 172°C), the device is shut off. This is a non-latch protection.

6.4 Device Functional Modes

6.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS563201 and TPS563208 can operate in the normal switching modes. The TPS563201 and TPS563208 operate at a quasi-fixed frequency of about 580kHz under CCM mode when T_{ON} extension is not triggered. When input voltage $V_{IN} < 7V$ and V_{FB} is lower than internal reference voltage, the switching frequency is allowed to smoothly drop to make T_{ON} extended to keep output voltage and improve the load transient performance. The minimum switching frequency is limited to about 200kHz.

6.4.2 Eco-mode Operation

When the TPS563201 and TPS563208 are in the normal CCM operating mode and the switch current falls to 0 A, the TPS563201 begins operating in pulse skipping Eco-mode. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the V_{FB} voltage falls below the Eco-mode threshold voltage. As the output current decreases, the perceived time between switching pulses increases.

6.4.3 Standby Operation

When the TPS563201 and TPS563208 are operating in either normal CCM or Eco-mode, they may be placed in standby by asserting the EN pin low.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

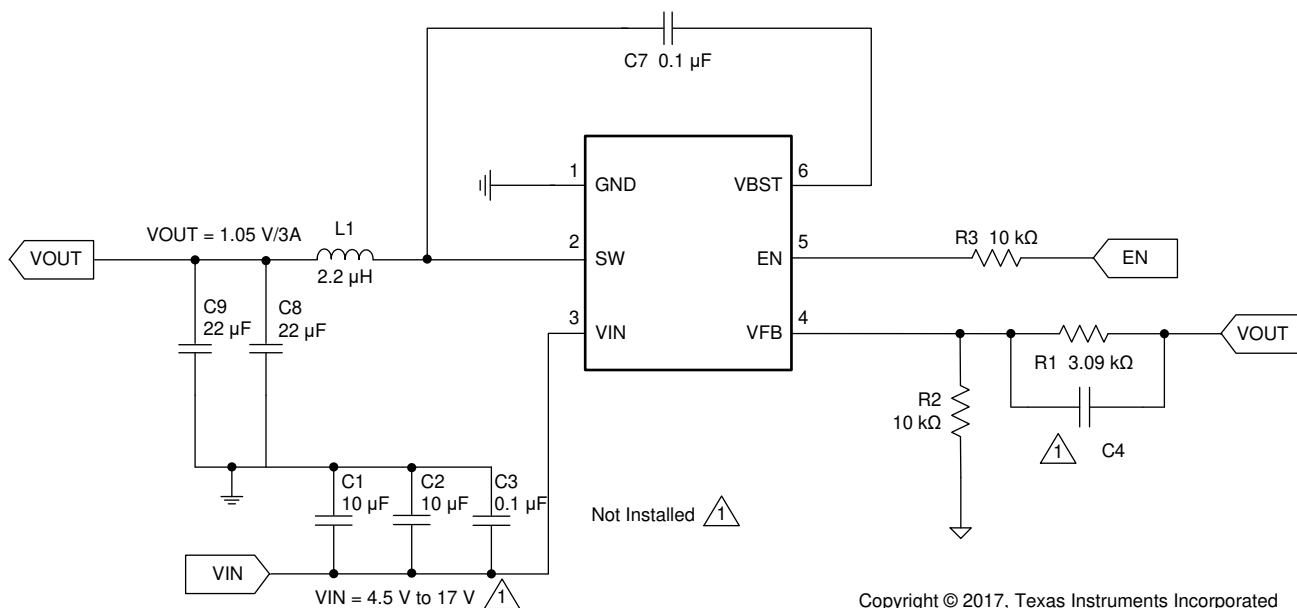
7.1 Application Information

The devices are typical step-down DC-DC converters. The devices are typically used to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for the TPS563201 and TPS563208. Alternately, the WEBENCH software can be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

7.2 Typical Application

The application schematic in 图 7-1 was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

图 7-1 shows the TPS563201 and TPS563208 4.5-V to 17-V input, 1.05-V output converter schematics.



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图 7-1. TPS563201 and TPS563208 1.05-V/3-A Reference Design

7.2.1 Design Requirements

表 7-1 shows the design parameters for this application.

表 7-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 17 V
Output voltage	1.05 V
Transient response, 1.5-A load step	$\Delta V_{out} = \pm 5\%$
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating frequency	580 kHz

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design with WEBENCH® Tools

[Click here](#) to create a custom design using the TPS56320x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using 方程式 2 to calculate V_{OUT} .

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.768 \times \left(1 + \frac{R1}{R2} \right) \quad (2)$$

7.2.2.3 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a – 40 dB per decade rate and the phase drops rapidly. D-CAP2 control scheme introduces a high frequency zero that reduces the gain roll off to – 20 dB per decade and increases the phase to 90° one decade above the zero

frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 方程式 3 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 7-2.

表 7-2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (μH)			C8 + C9 (μF)
			MIN	TYP	MAX	
1	3.09	10.0	1.5	2.2	4.7	20 to 68
1.05	3.74	10.0	1.5	2.2	4.7	20 to 68
1.2	5.76	10.0	1.5	2.2	4.7	20 to 68
1.5	9.53	10.0	1.5	2.2	4.7	20 to 68
1.8	13.7	10.0	1.5	2.2	4.7	20 to 68
2.5	22.6	10.0	2.2	2.2	4.7	20 to 68
3.3	33.2	10.0	2.2	2.2	4.7	20 to 68
5	54.9	10.0	3.3	3.3	4.7	20 to 68
6.5	75	10.0	3.3	3.3	4.7	20 to 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 方程式 4, 方程式 5, and 方程式 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 3.5 A and the calculated RMS current is 3.01 A. The inductor used is a WE 74431122 with a peak current rating of 13 A and an RMS current rating of 9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS563201 and TPS563208 are intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 μF to 68 μF. Use 方程式 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22-μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4 A.

7.2.2.4 Input Capacitor Selection

The TPS563201 and TPS563208 require an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 μF for the decoupling capacitor. An additional 0.1-μF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

7.2.2.5 Bootstrap Capacitor Selection

A 0.1- μ F ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

7.2.3 Application Curves

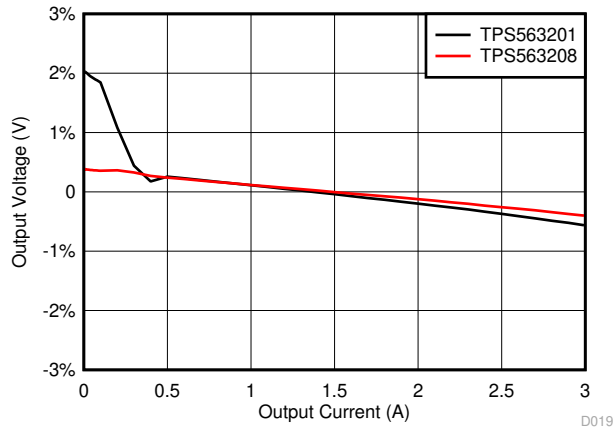


图 7-2. TPS563201 and TPS563208 Load Regulation, $V_{IN} = 5\text{ V}$

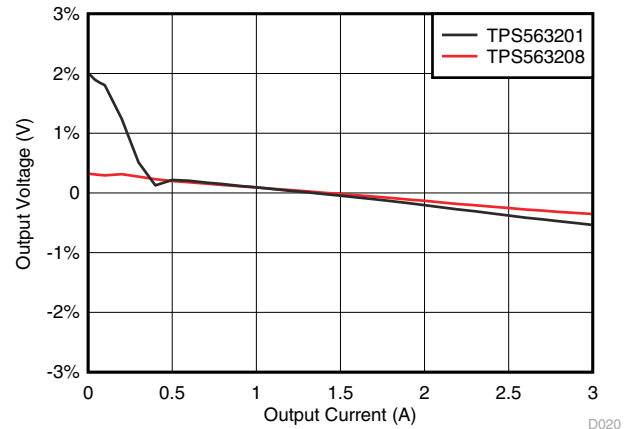
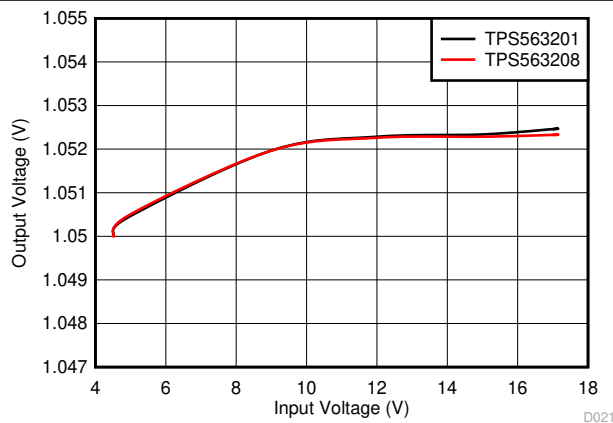


图 7-3. TPS563201 and TPS563208 Load Regulation, $V_{IN} = 12\text{ V}$



I_{OUT} of TPS563201: 1 A
 I_{OUT} of TPS563208: 10 mA

图 7-4. TPS563201 and TPS563208 Line Regulation

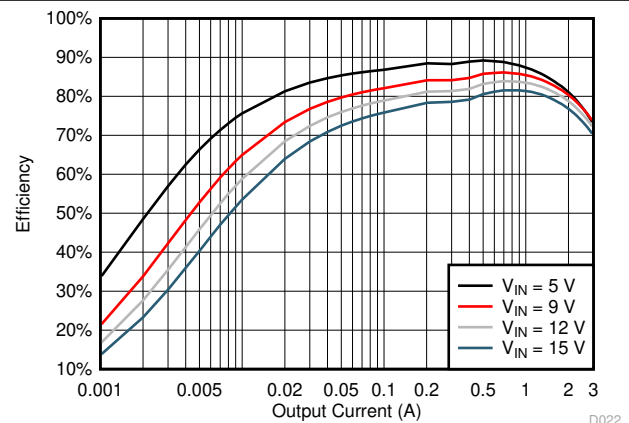


图 7-5. TPS563201 Efficiency

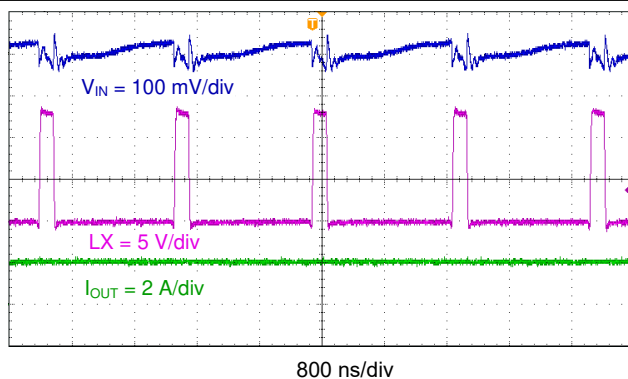


图 7-6. TPS563201 Input Voltage Ripple

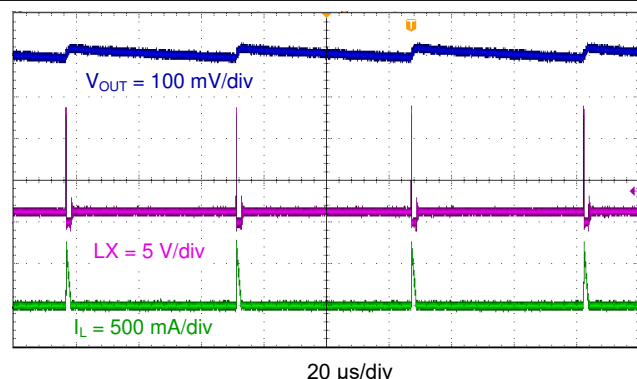


图 7-7. TPS563201 Output Voltage Ripple, 10 mA

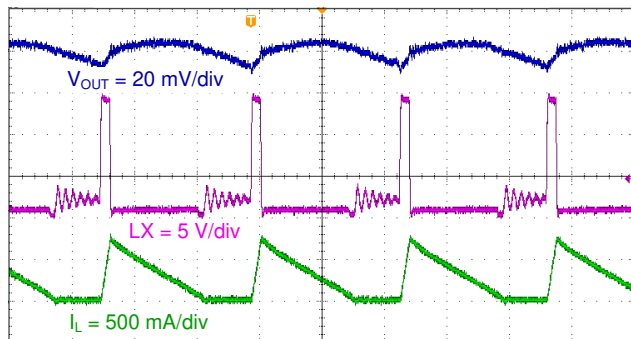


图 7-8. TPS563201 Output Voltage Ripple, $I_{out} = 0.25\text{ A}$

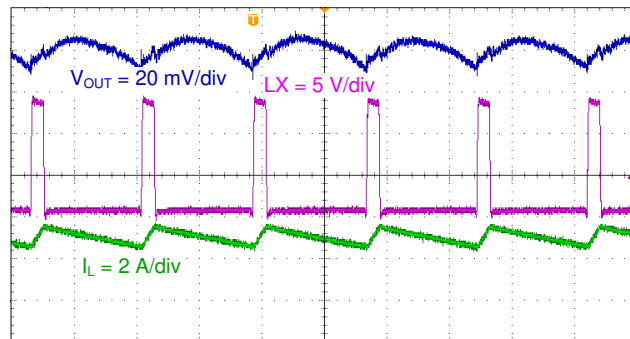


图 7-9. TPS563201 Output Voltage Ripple, $I_{out} = 2\text{ A}$

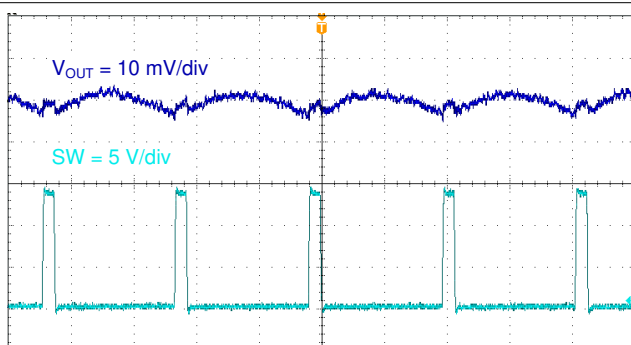


图 7-10. TPS563208 Output Voltage Ripple, $I_{OUT} = 0\text{ A}$

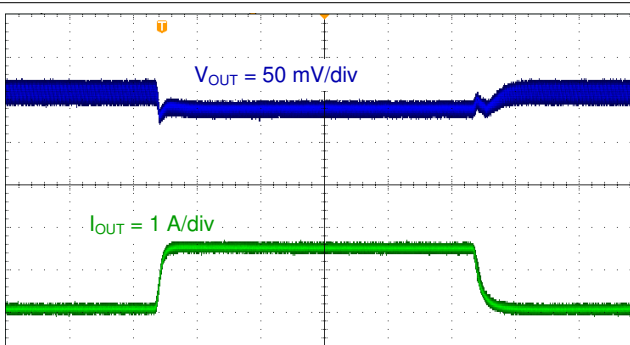


图 7-11. TPS563201 Transient Response, 0.1 to 1.5 A

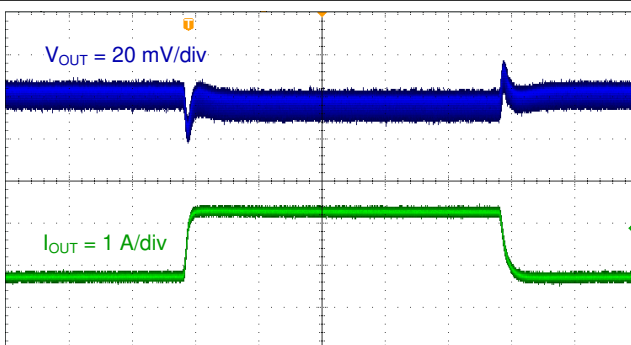


图 7-12. TPS563201 Transient Response, 0.75 to 2.25 A

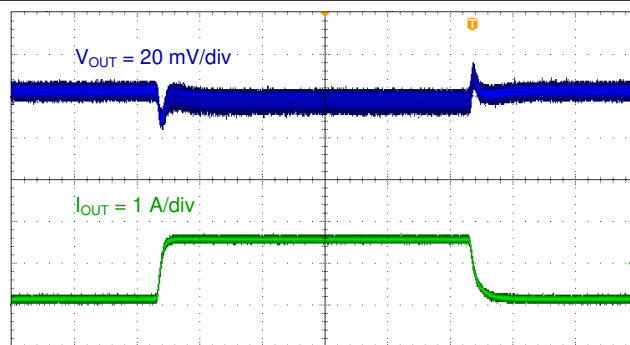


图 7-13. TPS563208 Transient Response 0.1 to 2 A

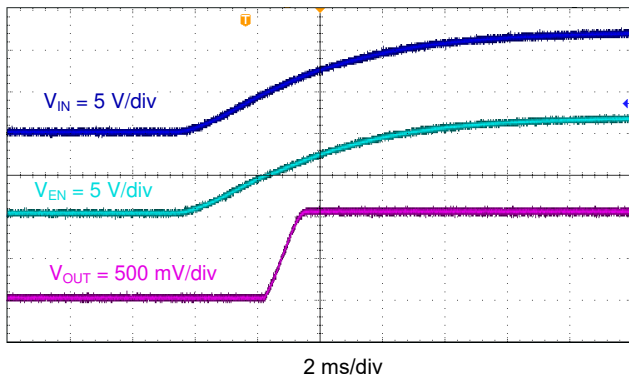


图 7-14. TPS563201 Start Up Relative to V_I

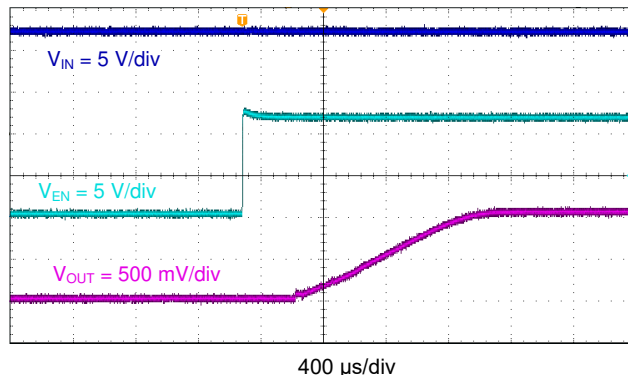


图 7-15. TPS563201 Start-Up Relative to EN

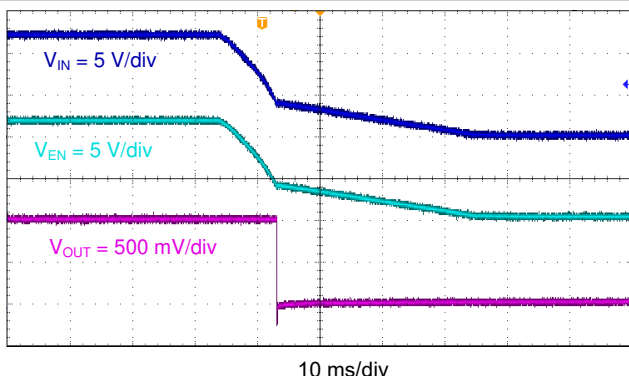


图 7-16. TPS563201 Shutdown Relative to V_I

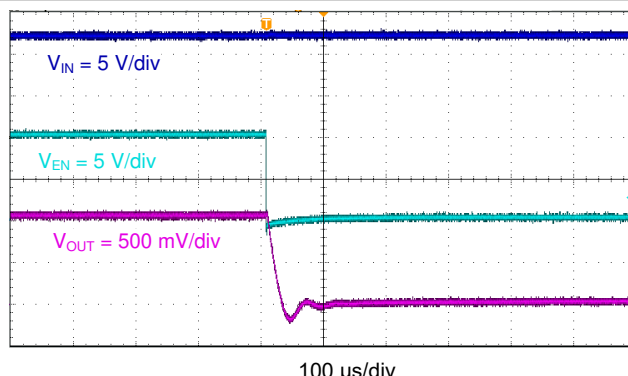


图 7-17. TPS563201 Shutdown Relative to EN

7.3 Power Supply Recommendations

TPS563201 and TPS563208 are designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is $V_O / 0.75$.

7.4 Layout

7.4.1 Layout Guidelines

1. VIN and GND traces must be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor must be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path must be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop must be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node must be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin must be as wide as possible to minimize its trace impedance.

7.4.2 Layout Example

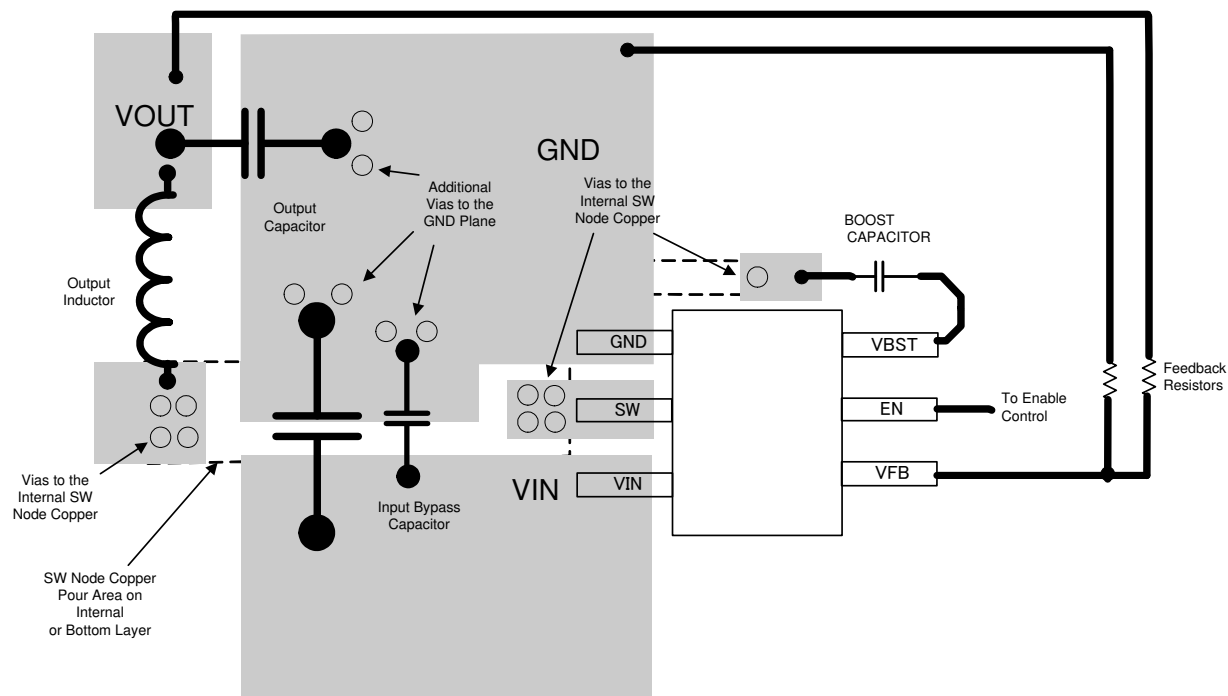


图 7-18. TPS563201 and TPS563208 Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Custom Design with WEBENCH® Tools

[Click here](#) to create a custom design using the TPS56320x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

8.4 Trademarks

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8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

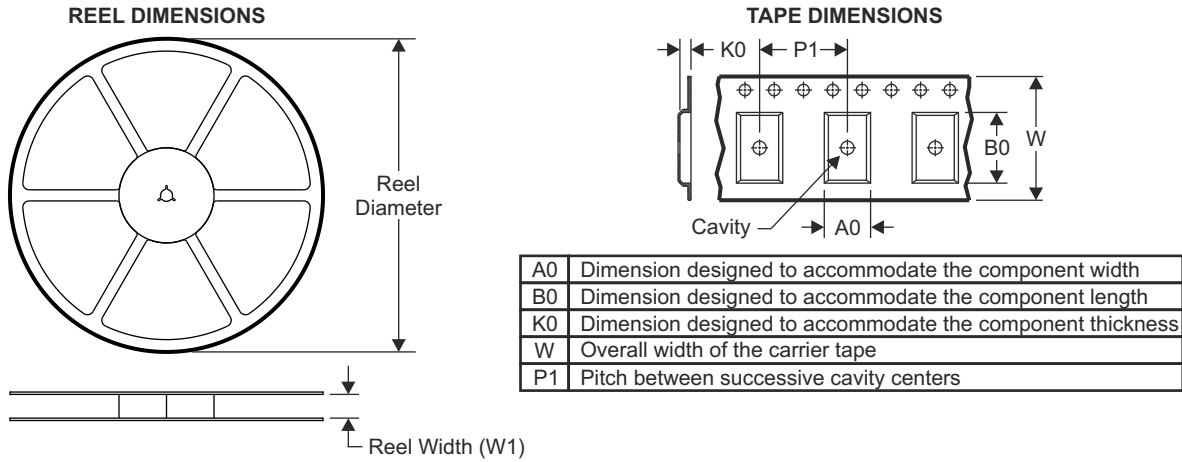
Changes from Revision A (April 2024) to Revision B (September 2024)	Page
• Updated specifications in the <i>Electrical Characteristics</i> table	6
• Updated 图 5-7 and 图 5-8	7
• Updated the <i>Normal Operation</i> description.....	12

Changes from Revision * (December 2015) to Revision A (April 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 将低关断电流从小于 10 μ A 更改为 20 μ A.....	1
• 通篇添加了 WEBENCH 信息.....	1
• 更新了商标信息.....	1
• 更新了 器件信息 表格式.....	1
• Changed VBST (vs SW) and VFB MAX from 6.5 to 6.....	4
• Changed Human-body model (HBM) value from 3000 to 2000.....	4
• Changed VBST (vs SW) MAX from 6.0 to 5.5.....	4
• Updated specifications in the <i>Electrical Characteristics</i> table	6
• Updated 图 5-1 and 图 5-2	7
• Updated the <i>Current Protection</i> section.....	11

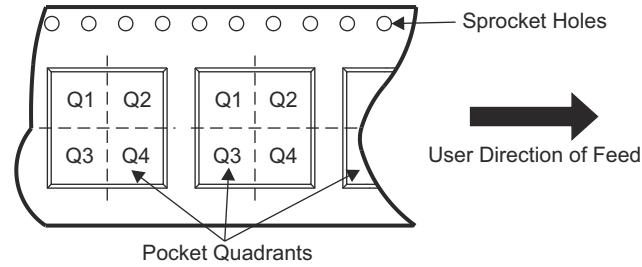
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

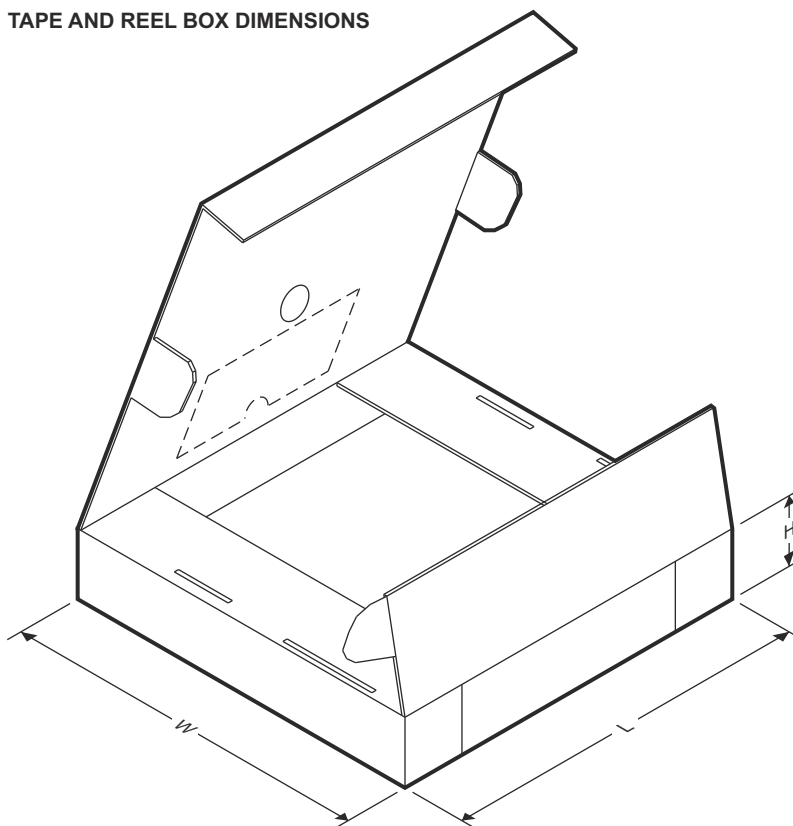


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS563201DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563201DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563201DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563201DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563208DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563208DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563208DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS563201DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS563201DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS563201DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
TPS563201DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
TPS563208DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS563208DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS563208DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0

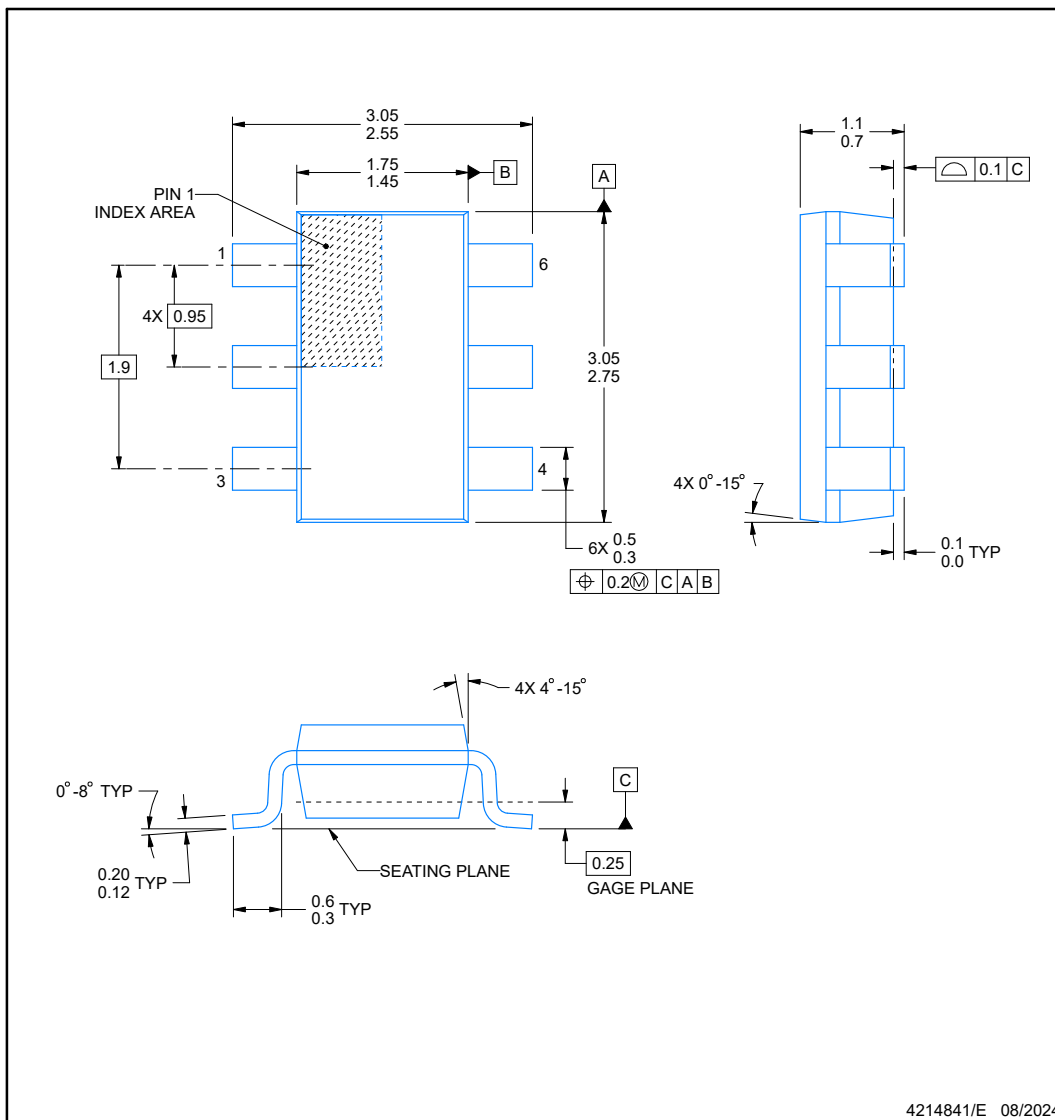


DDC0006A

PACKAGE OUTLINE

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES:

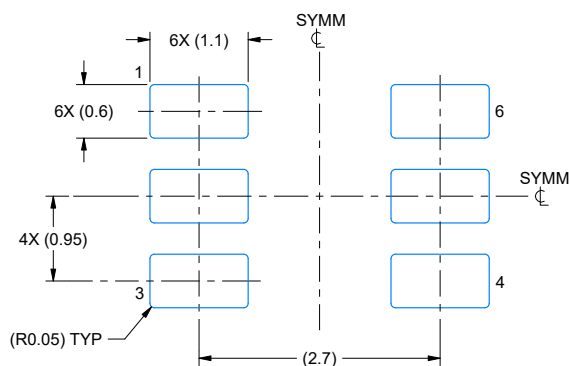
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

EXAMPLE BOARD LAYOUT

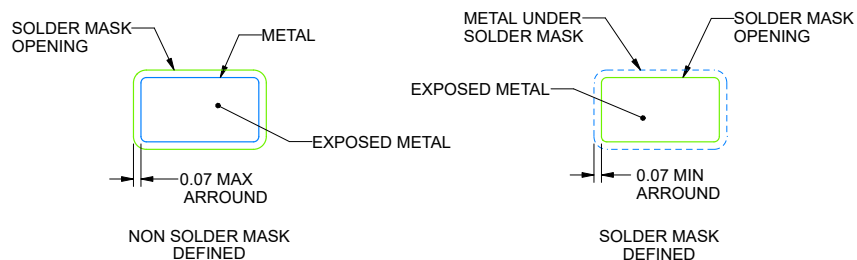
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SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

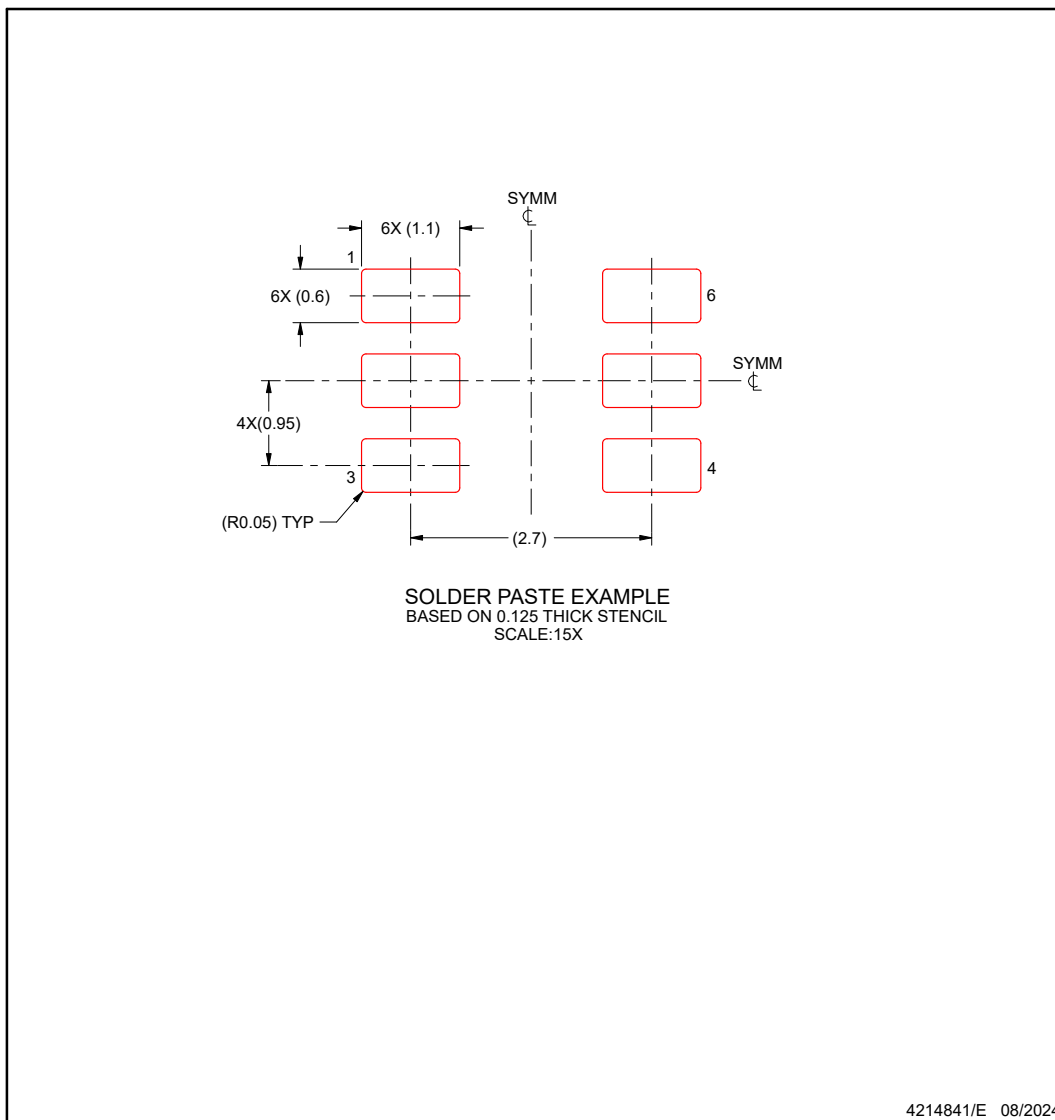
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS563201DDCR	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	Call TI Sn	Level-1-260C-UNLIM	-40 to 125	3201
TPS563201DDCR.A	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3201
TPS563201DDCR.B	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3201
TPS563201DDCT	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	Call TI Sn	Level-1-260C-UNLIM	-40 to 125	3201
TPS563201DDCT.A	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3201
TPS563201DDCT.B	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3201
TPS563208DDCR	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	Call TI Sn	Level-1-260C-UNLIM	-40 to 125	3208
TPS563208DDCR.A	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3208
TPS563208DDCR.B	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3208
TPS563208DDCT	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	Call TI Sn	Level-1-260C-UNLIM	-40 to 125	3208
TPS563208DDCT.A	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3208
TPS563208DDCT.B	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3208

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



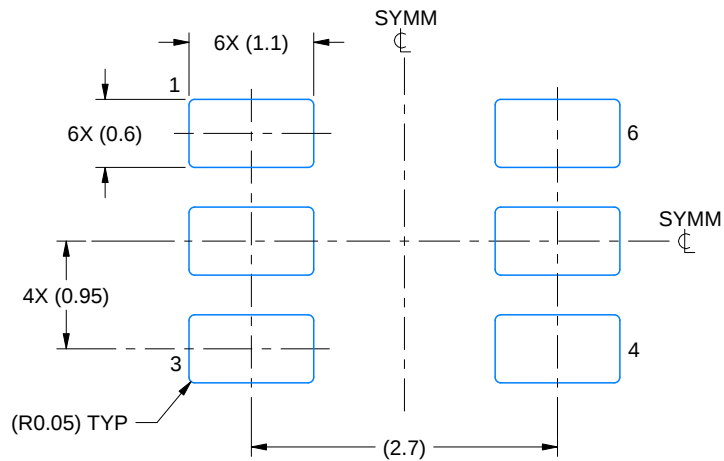
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

EXAMPLE BOARD LAYOUT

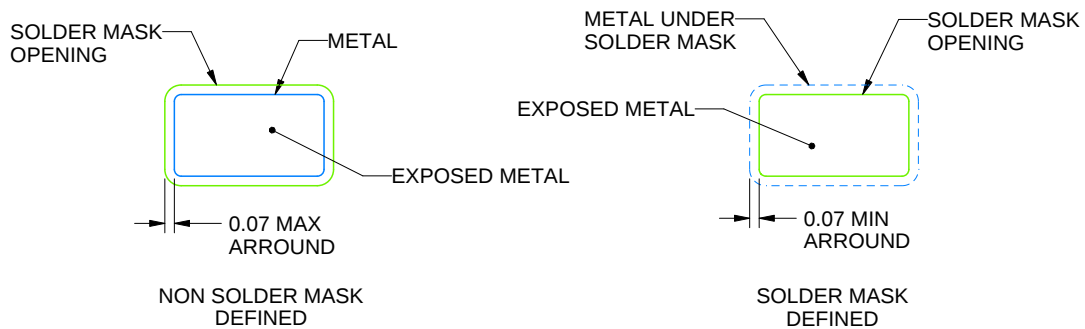
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X

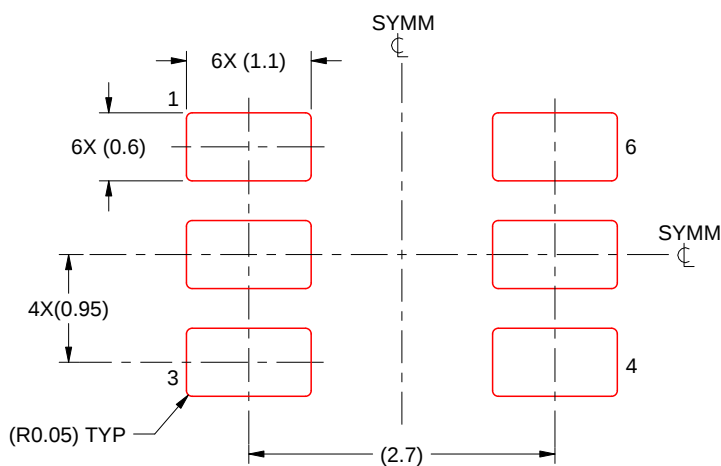


SOLDERMASK DETAILS

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NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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