支持断续模式的 4.5V 至 17 V 输入、8A 同步降压 SWIFT™ 转换器

查询样品: TPS54821

特性

- 集成式 **26 mΩ / 19 mΩ MOSFET**
- 分离电源轨：**1.6 V** 至 **17 V** 的 **PVIN**
- **200 kHz** 至 **1.6 MHz** 开关频率
- 与外部时钟同步
- 不同温度下基准电压为 **0.6 V ±1%**
- **2uA** 的低关断静态电流
- 单调启动至预偏置输出
- 工作结点温度范围：**-40°C** 至 **125°C**
- 可调慢启动/电源时序
- 针对欠压及过压的功率正常输出监控
- 可调输入欠压闭锁
- 提供
- 针对 **SWIFT**的软件工具™ 相关文档，请访问 **http://www.ti.com/swift**

应用

- 数字电视电源
- 机顶盒
- 蓝光 **DVD**
- 家用终端
- 高性能负载点稳压设计

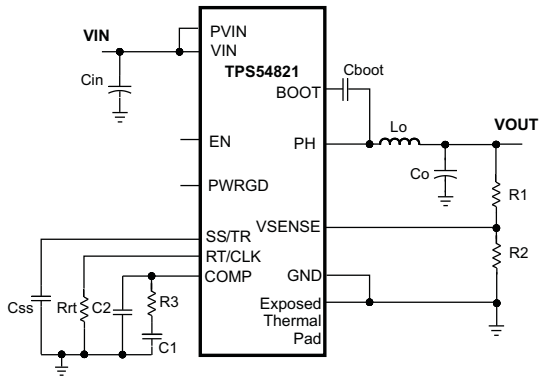
说明

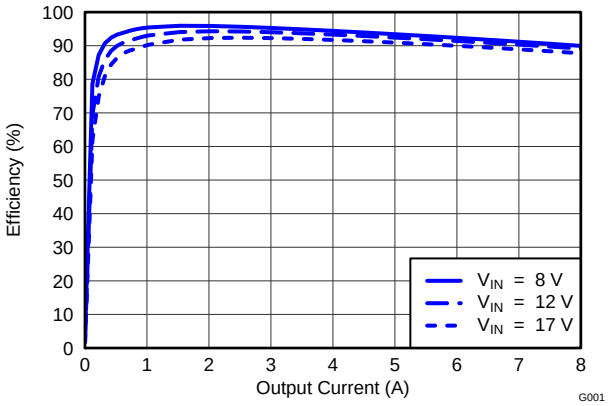
采用耐热性能增强型 3.5 毫米 x 3.5 毫米 QFN 封装的 TPS54821 是一款全功能 17 V、8 A 同步降压转换器。凭借高效率和集成高侧/低侧 MOSFET，此降压器为适应小型设计要求而进行了优化。 通过电流模式控制减少组件数量，并通过选择高开关频率缩小电感器占位面积，从而可进一步节省空间。

输出电压启动斜线上升由 SS/TR 引脚控制，其操作既支持独立电源供电模式又支持跟踪模式。 通过正确配置使能引脚与漏极开路电源状态正常引脚也可实现电源排序。

高侧 FET 的逐周期电流限制可在过载情况下保护器件不受损害，并可通过使用避免电流击穿的低侧源电流限制来增强此功能。 此外，还有一个可关闭低侧 MOSFET 的低侧吸收电流限制以防止过大的反向电流。 在过载电流情况持续时间超过预设时间时，断续保护功能将被触发。 当裸片温度超过热关断温度时，过热断续保护功能将禁用该器件，而在内置热关断断续时间之后，该部件会被重新启用。

简化的电路原理图





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_J	PACKAGE		PART NUMBER
–40°C to 125°C	14 Pin QFN	Small Reel(2)	TPS54821RHLT
		Large Reel(2)	TPS54821RHLR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) See the application section of the datasheet for layout information.

ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input Voltage	VIN	–0.3	20	V
	PVIN	–0.3	20	
	EN	–0.3	6	
	BOOT	–0.3	27	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	6	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	6	
Output Voltage	BOOT-PH	0	7.5	V
	PH	–1	20	
	PH 10ns Transient	–3	20	
Vdiff (GND to exposed thermal pad)		–0.2	0.2	V
Source Current	RT/CLK		±100	µA
	PH		Current Limit	A
Sink Current	PH		Current Limit	A
	PVIN		Current Limit	
	COMP		±200	µA
	PWRGD	–0.1	5	mA
Electrostatic Discharge (HBM) QSS 009-105 (JESD22-A114A)			2	kV
Electrostatic Discharge (CDM) QSS 009-147 (JESD22-C101B.01)			500	V
Operating Junction Temperature		–40	125	°C
Storage Temperature		–65	150	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS54821 QFN 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	47.2	°C/W
θ_{JA}	Junction-to-ambient thermal resistance(3)	32	
θ_{JCtop}	Junction-to-case (top) thermal resistance	64.8	
θ_{JB}	Junction-to-board thermal resistance	14.4	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	14.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.2	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability. See power dissipation estimate in application section of this data sheet for more information.
(3) Test board conditions:
(a) 2.5 inches × 2.5 inches, 4 layers, thickness: 0.062 inch
(b) 2 oz. copper traces located on the top of the PCB
(c) 2 oz. copper ground planes on the 2 internal layers and bottom layer
(d) 4 0.010 inch thermal vias located under the device package

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, VIN = 4.5V to 17V, PVIN = 1.6V to 17V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN AND PVIN PINS)					
PVIN operating input voltage		1.6		17	V
VIN operating input voltage		4.5		17	V
VIN internal UVLO threshold	VIN rising		4.0	4.5	V
VIN internal UVLO hysteresis			150		mV
VIN shutdown supply Current	EN = 0 V		2	5	µA
VIN operating – non switching supply current	VSENSE = 610 mV		600	800	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.21	1.26	V
Enable threshold	Falling	1.10	1.17		
Input current	EN = 1.1 V		1.15		µA
Hysteresis current	EN = 1.3 V		3.3		µA
VOLTAGE REFERENCE					
Voltage reference	0 A ≤ I_{OUT} ≤ 8A	0.594	0.6	0.606	V
MOSFET					
High-side switch resistance	BOOT-PH = 3 V		32	60	mΩ
High-side switch resistance(1)	BOOT-PH = 6 V		26	40	mΩ
Low-side Switch Resistance(1)	VIN = 12 V		19	30	mΩ
ERROR AMPLIFIER					
Error amplifier Transconductance (gm)	–2 µA < I_{COMP} < 2 µA, $V_{(COMP)}$ = 1 V		1300		µMhos
Error amplifier dc gain	VSENSE = 0.6 V	1000	4000		V/V
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV input overdrive		±110		µA
Start switching threshold			0.25		V
COMP to Iswitch gm			21		A/V
CURRENT LIMIT					

(1) Measured at pins

ELECTRICAL CHARACTERISTICS (continued)

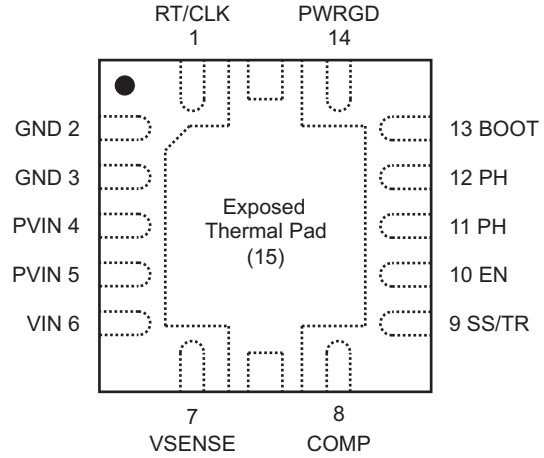
T_J = –40°C to 125°C, VIN = 4.5V to 17V, PVIN = 1.6V to 17V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-side switch current limit threshold		10.5	14.5	17	A
Low-side switch sourcing current limit		9.5	11.5	15	A
Low-side switch sinking current limit		2	3	4	A
Hiccup wait time			512		Cycles
Hiccup time before re-start			16384		Cycles
THERMAL SHUTDOWN					
Thermal shutdown		160	175		°C
Thermal shutdown hysteresis			10		°C
Thermal shutdown hiccup time			16384		Cycles
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Minimum switching frequency	Rrt = 240 kΩ (1%)	160	200	240	kHz
Switching frequency	Rrt = 100 kΩ (1%)	400	480	560	kHz
Maximum switching frequency	Rrt = 29 kΩ (1%)	1440	1600	1760	kHz
Minimum pulse width			20		ns
RT/CLK high threshold				2	V
RT/CLK low threshold		0.78			V
RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with RT resistor in series		66		ns
Switching frequency range (RT mode set point and PLL mode)		200		1600	kHz
PH (PH PIN)					
Minimum on time	Measured at 90% to 90% of VIN, 25°C, I_{PH} = 2A		94	145	ns
Minimum off time	BOOT-PH ≥ 3 V		0		ns
BOOT (BOOT PIN)					
BOOT-PH UVLO			2.1	3	V
SLOW START AND TRACKING (SS/TR PIN)					
SS charge current			2.3		µA
SS/TR to VSENSE matching	$V_{(SS/TR)}$ = 0.4 V		20	60	mV
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE falling (Fault)		92		% Vref
VSENSE rising (Good)			94		% Vref
VSENSE rising (Fault)			106		% Vref
VSENSE falling (Good)			104		% Vref
Output high leakage	VSENSE = Vref, $V_{(PWRGD)}$ = 5.5 V		30	100	nA
Output low	$I_{(PWRGD)}$ = 2 mA			0.3	V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5V at 100 µA		0.6	1	V
Minimum SS/TR voltage for PWRGD				1.4	V

DEVICE INFORMATION

PIN ASSIGNMENTS

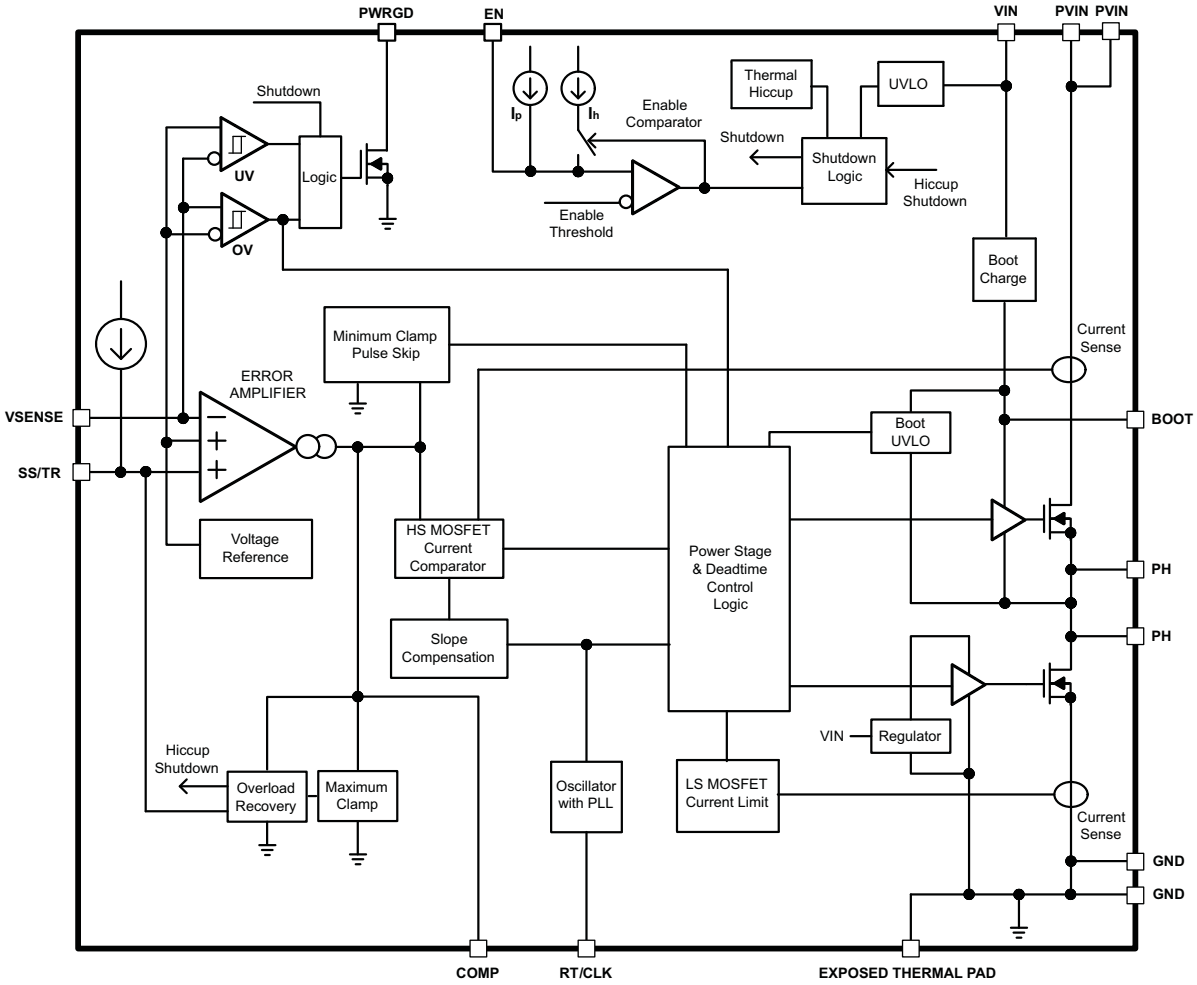
RHL PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
RT/CLK	1	Automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device; In CLK mode, the device synchronizes to an external clock.
GND	2, 3	Return for control circuitry and low-side power MOSFET.
PVIN	4, 5	Power input. Supplies the power switches of the power converter.
VIN	6	Supplies the control circuitry of the power converter.
VSENSE	7	Inverting input of the gm error amplifier.
COMP	8	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
SS/TR	9	Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
EN	10	Enable pin. Float to enable. Adjust the input undervoltage lockout with two resistors.
PH	11, 12	The switch node.
BOOT	13	A bootstrap cap is required between BOOT and PH. The voltage on this cap carries the gate drive voltage for the high-side MOSFET.
PWRGD	14	Power Good fault pin. Asserts low if output voltage is low due to thermal shutdown, dropout, over-voltage, EN shutdown or during slow start.
Exposed Thermal PAD	15	Thermal pad of the package and signal ground and it must be soldered down for proper operation.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

CHARACTERISTIC CURVES

HIGH-SIDE MOSFET ON RESISTANCE vs JUNCTION TEMPERATURE

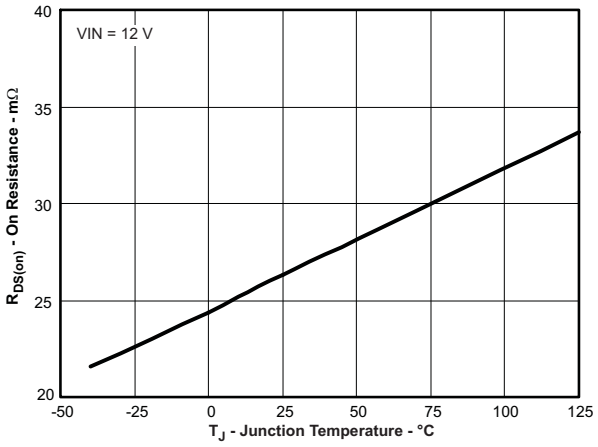


Figure 1.

LOW-SIDE MOSFET ON RESISTANCE vs JUNCTION TEMPERATURE

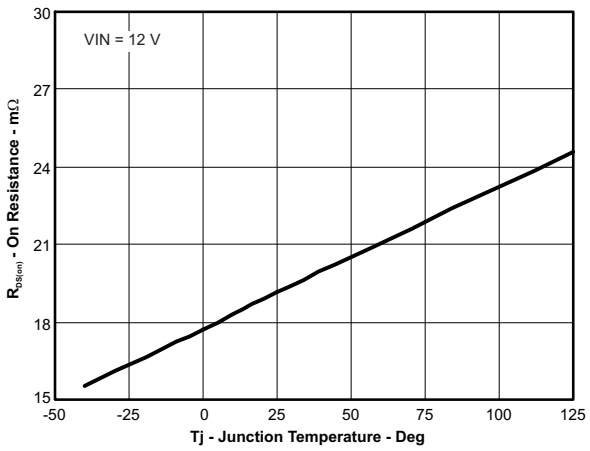


Figure 2.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

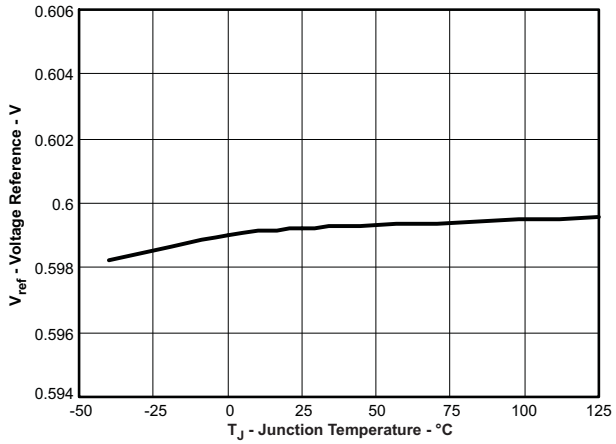


Figure 3.

OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

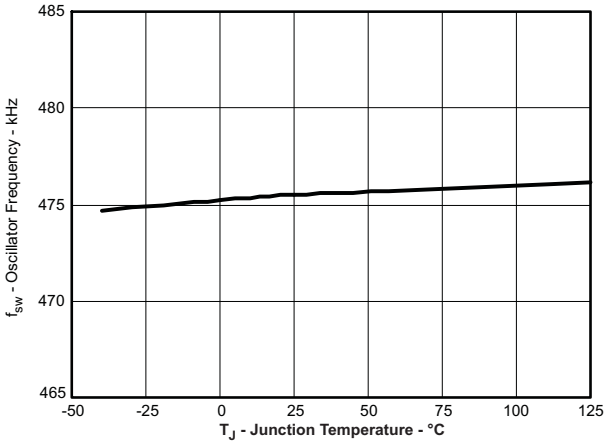


Figure 4.

TYPICAL CHARACTERISTICS (continued)

EN PIN UVLO THRESHOLD vs JUNCTION TEMPERATURE

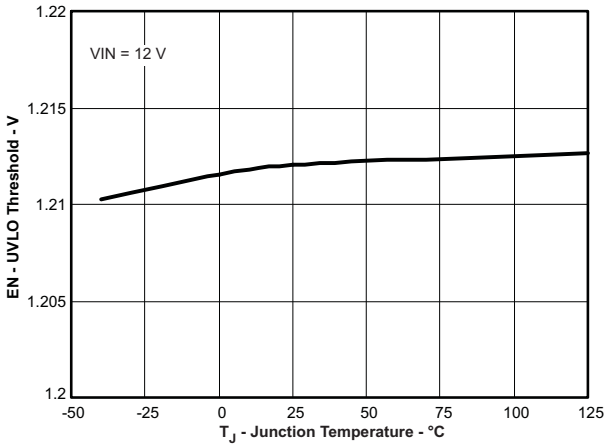


Figure 5.

EN PIN HYSTERESIS CURRENT vs JUNCTION TEMPERATURE

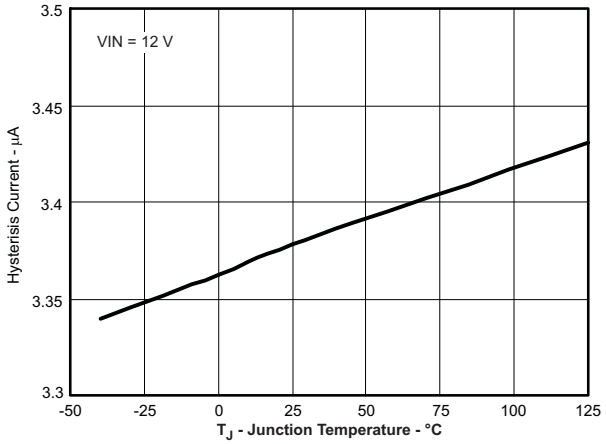


Figure 6.

EN PIN PULLUP CURRENT vs JUNCTION TEMPERATURE

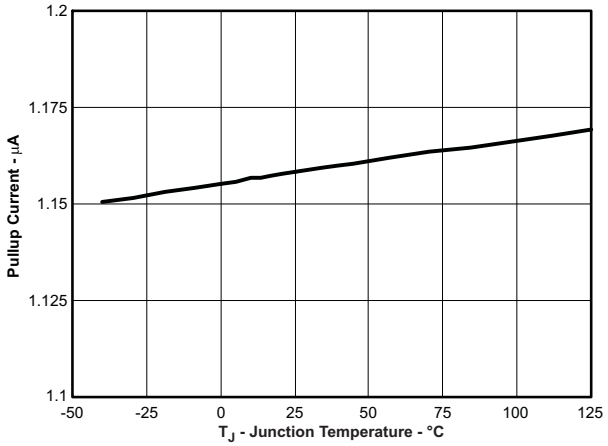


Figure 7.

SHUTDOWN QUIESCENT CURRENT vs INPUT VOLTAGE

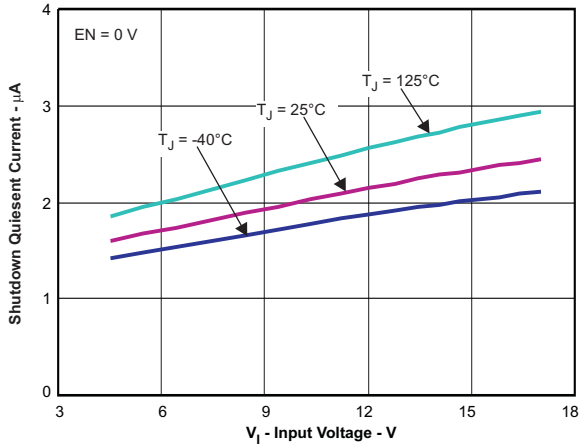


Figure 8.

VIN NON-SWITCHING OPERATING QUIESCENT CURRENT vs INPUT VOLTAGE

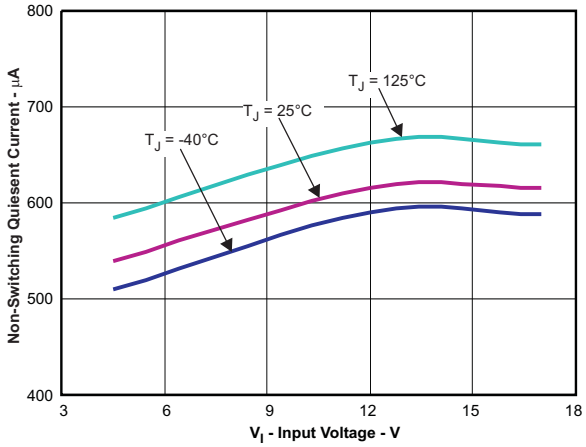


Figure 9.

SLOW START CHARGE CURRENT vs JUNCTION TEMPERATURE

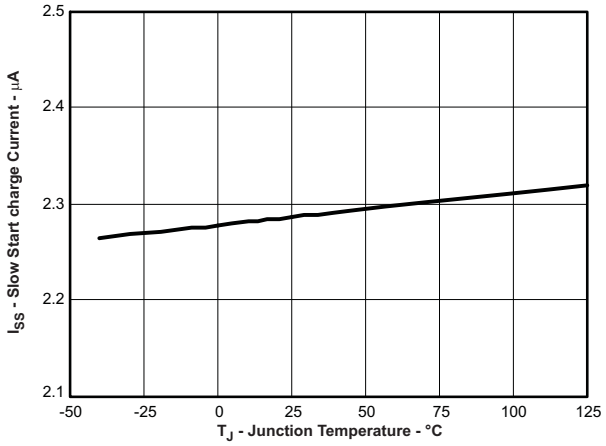


Figure 10.

TYPICAL CHARACTERISTICS (continued)

SS/TR TO VSENSE OFFSET vs JUNCTION TEMPERATURE

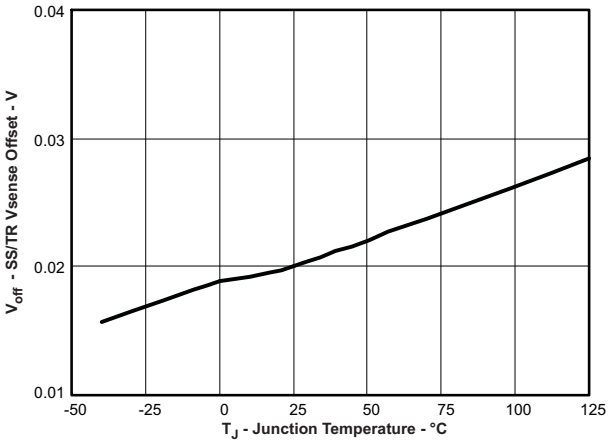


Figure 11.

PWRGD THRESHOLD vs JUNCTION TEMPERATURE

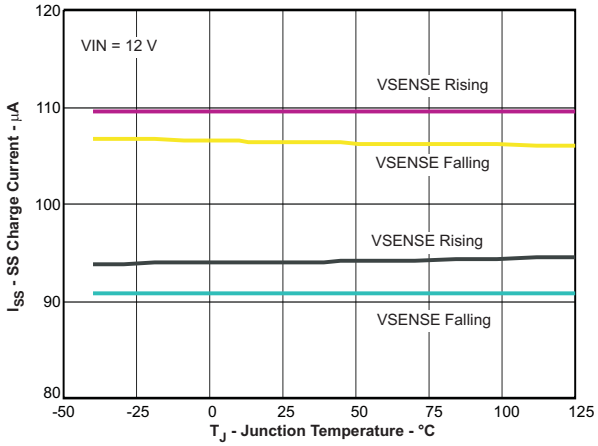


Figure 12.

HIGH-SIDE CURRENT LIMIT THRESHOLD vs INPUT VOLTAGE

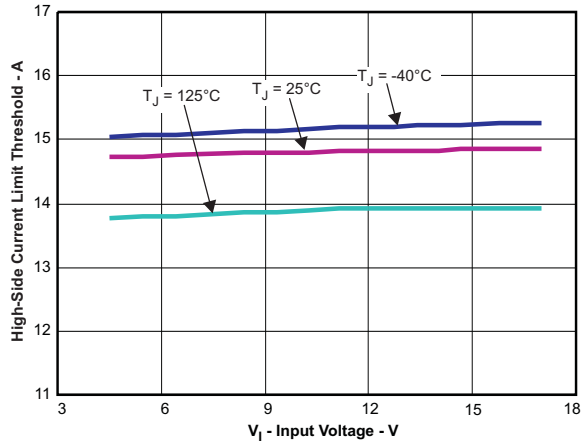


Figure 13.

MINIMUM CONTROLLABLE ON TIME vs JUNCTION TEMPERATURE

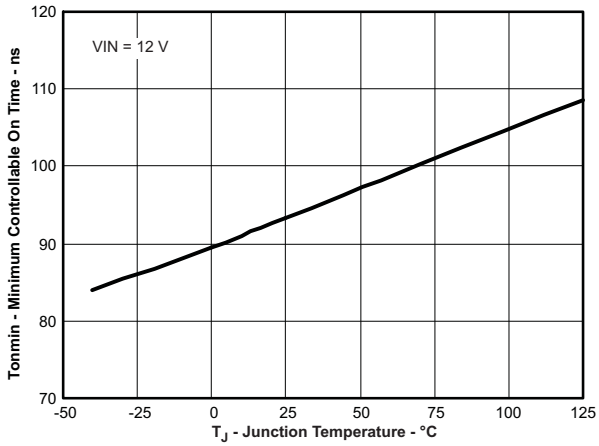


Figure 14.

MINIMUM CONTROLLABLE DUTY RATIO vs JUNCTION TEMPERATURE

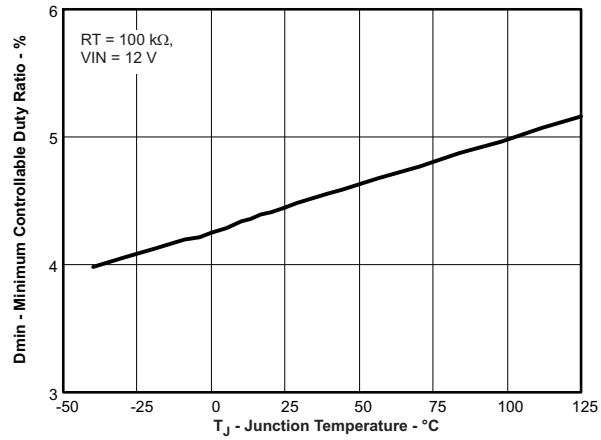


Figure 15.

BOOT-PH UVLO THRESHOLD vs JUNCTION TEMPERATURE

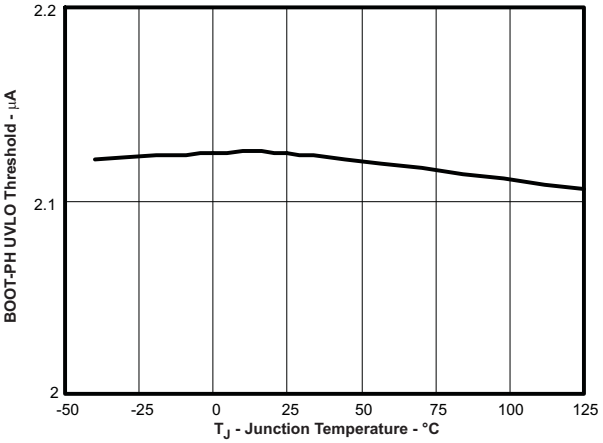


Figure 16.

TYPICAL CHARACTERISTICS (continued)

OVERVIEW

The device is a 17-V, 8-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant frequency, peak current mode control which also simplifies external frequency compensation. The wide switching frequency of 200 kHz to 1600 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device also has an internal phase lock loop (PLL) controlled by the RT/CLK pin that can be used to synchronize the switching cycle to the falling edge of an external system clock.

The device has been designed for safe monotonic startup into pre-biased loads. The default start up is when VIN is typically 4.0V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pull-up current. The total operating current for the device is approximately 600μA when not switching and under no load. When the device is disabled, the supply current is typically less than 2μA.

The integrated MOSFETs allow for high efficiency power supply designs with continuous output currents up to 8 amperes. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The device reduces the external component count by integrating the boot recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by a BOOT to PH UVLO (BOOT-PH UVLO) circuit allowing PH pin to be pulled low to recharge the boot capacitor. The device can operate at 100% duty cycle as long as the boot capacitor voltage is higher than the preset BOOT-PH UVLO threshold which is typically 2.1V. The output voltage can be stepped down to as low as the 0.6V voltage reference (Vref).

The device has a power good comparator (PWRGD) with hysteresis which monitors the output voltage through the VSENSE pin. The PWRGD pin is an open drain MOSFET which is pulled low when the VSENSE pin voltage is less than 92% or greater than 106% of the reference voltage Vref and asserts high when the VSENSE pin voltage is 94% to 104% of the Vref.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider should be coupled to the pin for slow start or critical power supply sequencing requirements.

The device is protected from output overvoltage, overload and thermal fault conditions. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the VSENSE pin voltage is lower than 104% of the Vref. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections which help control the inductor current and avoid current runaway. The device also shuts down if the junction temperature is higher than thermal shutdown trip point. The device is restarted under control of the slow start circuit automatically after the built-in thermal shutdown hiccup time.

DETAILED DESCRIPTION

Fixed Frequency PWM Control

The device uses a adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference which compares to the high-side power switch current. When the power switch current reaches current reference generated by the COMP voltage level the high-side power switch is turned off and the low-side power switch is turned on.

Continuous Current Mode Operation (CCM)

As a synchronous buck converter, the device normally works in CCM (Continuous Conduction Mode) under all load conditions.

VIN and Power VIN Pins (VIN and PVIN)

The device allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the device. The PVIN pin voltage provides the input voltage to the power converter system.

If tied together, the input voltage for VIN and PVIN can range from 4.5 V to 17 V. If using the VIN separately from PVIN, the VIN pin must be between 4.5 V and 17 V, and the PVIN pin can range from as low as 1.6 V to 17 V. A voltage divider connected to the EN pin can adjust the either input voltage UVLO appropriately. Adjusting the input voltage UVLO on the PVIN pin helps to provide consistent power up behavior.

Voltage Reference

The voltage reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit.

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output (VOUT) to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Referring to the application schematic of Figure 29, start with a 10 kΩ for R6 and use Equation 1 to calculate R5. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R5 = \frac{Vo - Vref}{Vref} R6 \quad (1)$$

Where Vref = 0.6V

The minimum output voltage and maximum output voltage can be limited by the minimum on time of the high-side MOSFET and bootstrap voltage (BOOT-PH voltage) respectively. More discussions are located in Minimum Output Voltage and Bootstrap Voltage (BOOT) and Low Dropout Operation.

Safe Start-up into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to sink current until the SS/TR pin voltage is higher than 1.4 V.

Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS/TR pin voltage or the internal 0.6 V voltage reference. The transconductance of the error amplifier is 1300 µA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground.

Slope Compensation

The device adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty cycle range.

Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state.

The EN pin has an internal pull-up current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 150mV.

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN, in split rail applications, then the EN pin can be configured as shown in Figure 17, Figure 18 and Figure 19. When using the external UVLO function it is recommended to set the hysteresis to be greater than 500mV.

The EN pin has a small pull-up current Ip which sets the default state of the pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function since it increases by I_h once the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 2 and Equation 3.

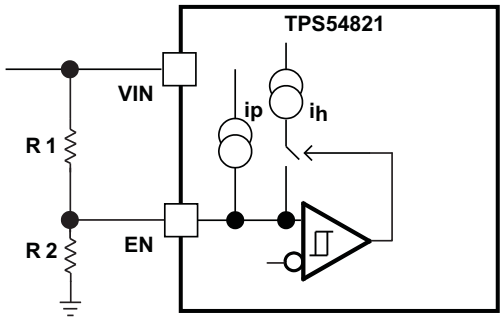


Figure 17. Adjustable VIN Undervoltage Lock Out

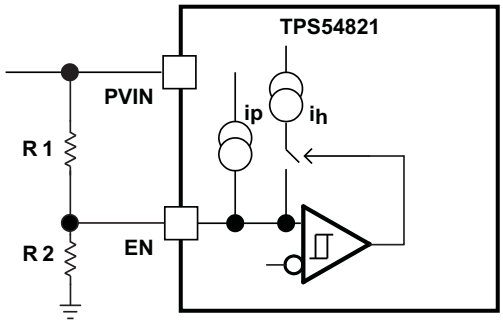


Figure 18. Adjustable PVIN Undervoltage Lock Out, VIN ≥ 4.5V

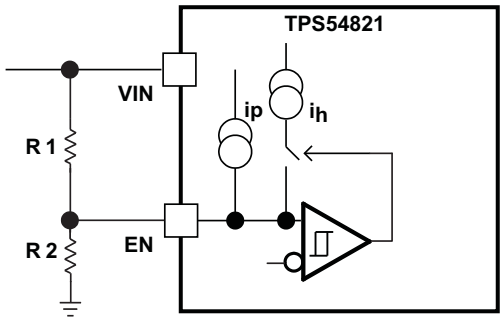


Figure 19. Adjustable VIN and PVIN Undervoltage Lock Out

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (2)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (3)$$

Where I_h = 3.3 µA, I_p = 1.15 µA, $V_{ENRISING}$ = 1.21 V, $V_{ENFALLING}$ = 1.17 V

Adjustable Switching Frequency and Synchronization (RT/CLK)

The RT/CLK pin can be used to set the switching frequency of the device in two modes.

In RT mode, a resistor (RT resistor) is connected between the RT/CLK pin and GND. The switching frequency of the device is adjustable from 200 kHz to 1600 kHz by placing a maximum of 240 kΩ and minimum of 29 kΩ respectively. In CLK mode, an external clock is connected directly to the RT/CLK pin. The device is synchronized to the external clock frequency with PLL.

The CLK mode overrides the RT mode. The device is able to detect the proper mode automatically and switch from the RT mode to CLK mode.

Adjustable Switching Frequency (RT Mode)

To determine the RT resistance for a given switching frequency, use Equation 4 or the curve in Figure 20. To reduce the solution size one would set the switching frequency as high as possible, but tradeoffs of the supply efficiency and minimum controllable on time should be considered.

$$Rrt(k\Omega) = 48000 \cdot Fsw\,(kHz)^{-0.997} - 2 \quad (4)$$

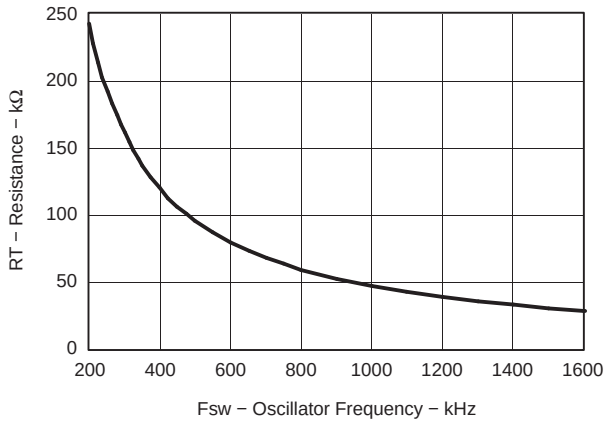


Figure 20. RT Set Resistor vs Switching Frequency

Synchronization (CLK mode)

An internal Phase Locked Loop (PLL) has been implemented to allow synchronization between 200kHz and 1600kHz, and to easily switch from RT mode to CLK mode.

To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.78V and higher than 2.0V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin.

In applications where both RT mode and CLK mode are needed, the device can be configured as shown in Figure 21. Before the external clock is present, the device works in RT mode and the switching frequency is set by RT resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the SYNC pin is pulled above the RT/CLK high threshold (2 V), the device switches from the RT mode to the CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from the CLK mode back to the RT mode because the internal switching frequency drops to 100kHz first before returning to the switching frequency set by RT resistor.

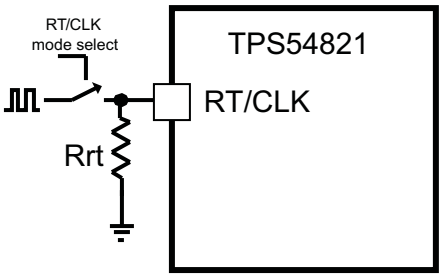


Figure 21. Works with Both RT mode and CLK mode

Slow Start (SS/TR)

The device uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow start time. The device has an internal pull-up current source of 2.3 µA that charges the external slow start capacitor. The calculations for the slow start time (Tss, 10% to 90%) and slow start capacitor (Css) are shown in Equation 5. The voltage reference (Vref) is 0.6 V and the slow start charge current (Iss) is 2.3µA.

$$Tss(ms) = \frac{Css(nF) \times Vref(V)}{Iss(\mu A)} \quad (5)$$

When the input UVLO is triggered, the EN pin is pulled below 1.21V, or a thermal shutdown event occurs the device stops switching and enters low current operation. At the subsequent power up, when the shutdown condition is removed, the device does not start switching until it has discharged its SS/TR pin to ground ensuring proper soft start behavior.

Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the VSENSE pin is between 94% and 104% of the internal voltage reference the PWRGD pin pull-down is de-asserted and the pin floats. It is recommended to use a pull-up resistor between the values of 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD is in a defined state once the VIN input voltage is greater than 1V but with reduced current sinking capability. The PWRGD achieves full current sinking capability once the VIN input voltage is above 4.5 V.

The PWRGD pin is pulled low when VSENSE is lower than 92% or greater than 106% of the nominal internal reference voltage. Also, the PWRGD is pulled low, if the input UVLO or thermal shutdown are asserted, the EN pin is pulled low or the SS/TR pin is below 1.4 V.

Bootstrap Voltage (BOOT) and Low Dropout Operation

The device has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and BOOT-PH voltage is below regulation. The value of this ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve drop out, the device is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than the BOOT-PH UVLO threshold which is typically 2.1 V. When the voltage between BOOT and PH drops below the BOOT-PH UVLO threshold the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged. In applications with split input voltage rails 100% duty cycle operation can be achieved as long as (VIN – PVIN) > 4 V.

Sequencing (SS/TR)

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN and PWRGD pins.

The sequential method is illustrated in Figure 22 using two TPS54821 devices. The power good of the first device is coupled to the EN pin of the second device which enables the second power supply once the primary supply reaches regulation.

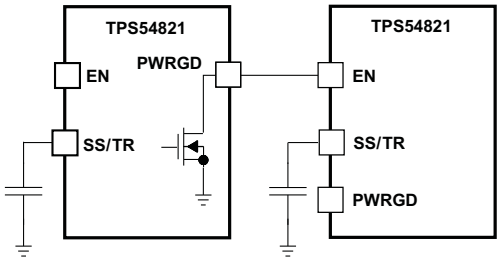


Figure 22. Sequential Start Up Sequence

Figure 23 shows the method implementing ratio-metric sequencing by connecting the SS/TR pins of two devices together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow start time the pull-up current source must be doubled in Equation 5.

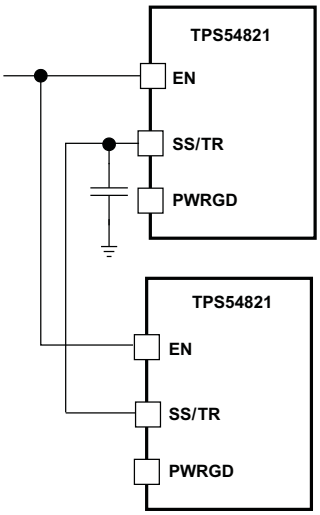


Figure 23. Ratio-metric Start Up Sequence

Ratio-metric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 24 to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 6 and Equation 7, the tracking resistors can be calculated to initiate the Vout2 slightly before, after or at the same time as Vout1. Equation 8 is the voltage difference between Vout1 and Vout2.

To design a ratio-metric start up in which the Vout2 voltage is slightly greater than the Vout1 voltage when Vout2 reaches regulation, use a negative number in Equation 6 and Equation 7 for deltaV. Equation 8 results in a positive number for applications where the Vout2 is slightly lower than Vout1 when Vout2 regulation is achieved. .

The deltaV variable is zero volt for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset (Vssoffset, 29mV) in the slow start circuit and the offset created by the pull-up current source (Iss, 2.3 µA) and tracking resistors, the Vssoffset and Iss are included as variables in the equations.

To ensure proper operation of the device, the calculated R1 value from Equation 6 must be greater than the value calculated in Equation 9.

$$R1 = \frac{Vout2 + \Delta V}{Vref} \times \frac{Vssoffset}{Iss} \quad (6)$$

$$R2 = \frac{Vref \times R1}{Vout2 + \Delta V - Vref} \quad (7)$$

$$\Delta V = Vout1 - Vout2 \quad (8)$$

$$R1 > 2800 \times Vout1 - 180 \times \Delta V \quad (9)$$

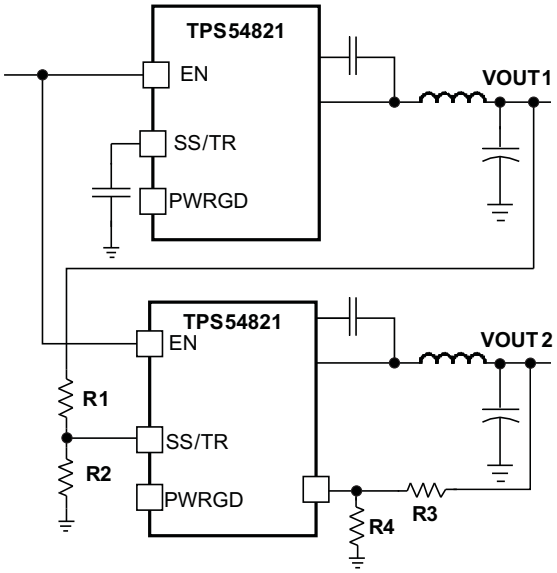


Figure 24. Ratio-metric and Simultaneous Startup Sequence

Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

High-side MOSFET overcurrent protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle by cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference the high-side switch is turned off.

Low-side MOSFET overcurrent protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 512 switching cycles, the device will shut down itself and restart after the hiccup time of 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. Once the junction temperature drops below 165°C typically, the internal thermal hiccup timer will start to count. The device reinitiates the power up sequence after the built-in thermal shutdown hiccup time (16384 cycles) is over.

Small Signal Model for Loop Response

Figure 25 shows an equivalent model for the device control loop which can be modeled in a circuit simulation program to check frequency response and transient responses. The error amplifier is a transconductance amplifier with a gm of 1300µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor Roea (3.07 MΩ) and capacitor Coea (20.7 pF) model the open loop gain and frequency response of the error amplifier. The 1-mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c and c/b show the small signal responses of the power stage and frequency compensation respectively. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

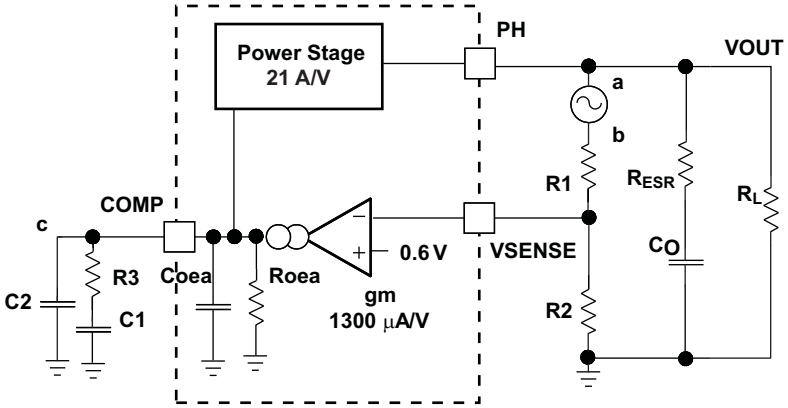


Figure 25. Small Signal Model for Loop Response

Simple Small Signal Model for Peak Current Mode Control

Figure 26 is a simple small signal model that can be used to understand how to design the frequency compensation. The device power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 10 and consists of a dc gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 25) is the power stage transconductance (gm_{ps}) which is 21 A/V for the device. The DC gain of the power stage is the product of gm_{ps} and the load resistance, R_L, as shown in Equation 11 with resistive loads. As the load current increases, the DC gain decreases. This variation with load may seem problematic at first glance, but fortunately the dominant pole moves with load current (see Equation 12). The combined effect is highlighted by the dashed line in Figure 27. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

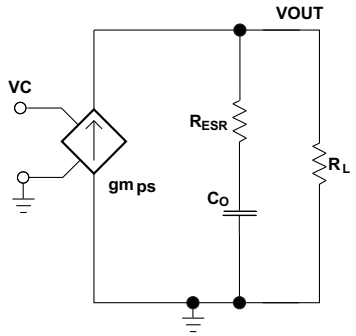


Figure 26. Simplified Small Signal Model for Peak Current Mode Control

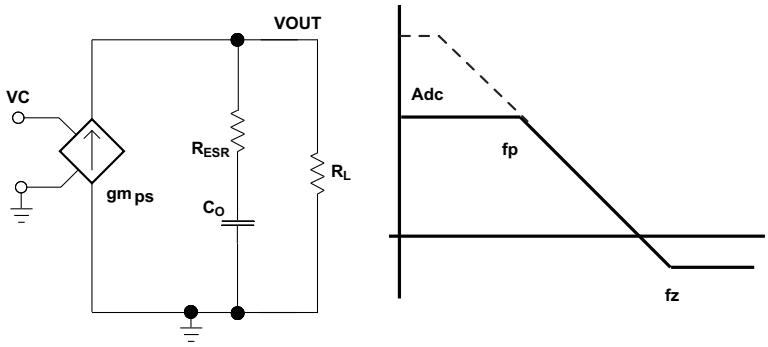


Figure 27. Simplified Frequency Response for Peak Current Mode Control

$$\frac{VOUT}{VC} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \quad (10)$$

$$Adc = gm_{ps} \times R_L \quad (11)$$

$$fp = \frac{1}{C_O \times R_L \times 2\pi} \quad (12)$$

$$fz = \frac{1}{C_O \times R_{ESR} \times 2\pi} \quad (13)$$

Where

gm_{ea} is the GM amplifier gain (1300µA/V)
gm_{ps} is the power stage gain (21A/V).
R_L is the load resistance
C_O is the output capacitance.
R_{ESR} is the equivalent series resistance of the output capacitor.

Small Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used Type II compensation circuits and a Type III frequency compensation circuit, as shown in Figure 28. In Type 2A, one additional high frequency pole, C6, is added to attenuate high frequency noise. In Type III, one additional capacitor, C11, is added to provide a phase boost at the crossover frequency. See *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) for a complete explanation of Type III compensation.

The design guidelines below are provided for advanced users who prefer to compensate using the general method. The below equations only apply to designs whose ESR zero is above the bandwidth of the control loop. This is usually true with ceramic output capacitors. See the Application Information section for a step-by-step design procedure using higher ESR output capacitors with lower ESR zero frequencies.

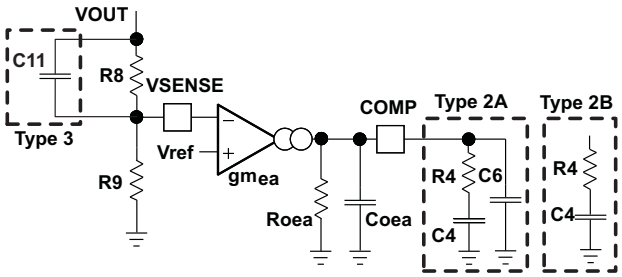


Figure 28. Types of Frequency Compensation

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency, fc. A good starting point is 1/10th of the switching frequency, fsw.
2. R4 can be determined by:

$$R4 = \frac{2\pi \times fc \times VOUT \times Co}{gm_{ea} \times Vref \times gm_{ps}} \quad (14)$$

   Where:

   gm_{ea} is the GM amplifier gain (1300µA/V)
   gm_{ps} is the power stage gain (21A/V)
   Vref is the reference voltage (0.6V)

3. Place a compensation zero at the dominant pole: $\left(fp = \frac{1}{C_O \times R_L \times 2\pi} \right)$
   C4 can be determined by:

$$C4 = \frac{R_L \times Co}{R4} \quad (15)$$

4. C6 is optional. It can be used to cancel the zero from the ESR (Equivalent Series Resistance) of the output capacitor Co.

$$C6 = \frac{R_{ESR} \times Co}{R4} \quad (16)$$

5. Type III compensation can be implemented with the addition of one capacitor, C11. This allows for slightly higher loop bandwidths and higher phase margins. If used, C11 is calculated from Equation 17.

$$C11 = \frac{1}{(2 \cdot \pi \cdot R8 \cdot fc)} \quad (17)$$

APPLICATION INFORMATION

Design Guide – Step-By-Step Design Procedure

This example details the design of a high frequency switching regulator design using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, start with the following known parameters:

Table 1.

Parameter	Value
Output Voltage	3.3 V
Output Current	8 A
Transient Response 4 A load step	ΔVout = 7 %
Input Voltage	12 V nominal, 8 V to 17 V
Output Voltage Ripple	33 mV p-p
Start Input Voltage (Rising Vin)	6.528 V
Stop Input Voltage (Falling Vin)	6.193 V
Switching Frequency	480 kHz

Typical Application Schematic

The application schematic of Figure 29 was developed to meet the requirements above. This circuit is available as the TPS54821EVM-049 evaluation module. The design procedure is given in this section. For more information about Type II and Type III frequency compensation circuits, see Designing Type III Compensation for Current Mode Step-Down Converters (SLVA352) and Design Calculator (SLVC219).

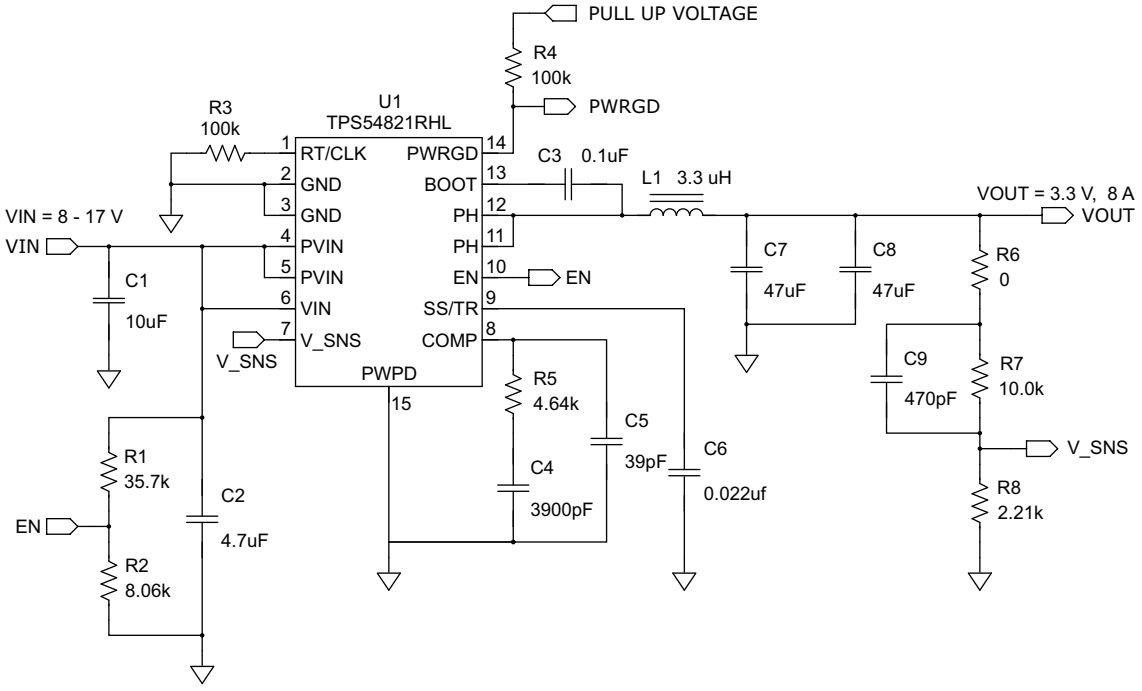


Figure 29. Typical Application Circuit

Operating Frequency

The first step is to decide on a switching frequency for the regulator. There is a trade off between higher and

lower switching frequencies. Higher switching frequencies may produce smaller a solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which hurt the converter's efficiency and thermal performance. In this design, a moderate switching frequency of 480 kHz is selected to achieve both a small solution size and a high efficiency operation.

Output Inductor Selection

To calculate the value of the output inductor, use Equation 18. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, KIND is normally from 0.1 to 0.3 for the majority of applications.

$$L1 = \frac{Vinmax - Vout}{Io \cdot Kind} \cdot \frac{Vout}{Vinmax \cdot fsw} \tag{18}$$

For this design example, use KIND = 0.3 and the minimum inductor value is calculated to be 2.31 µH. For this design, a larger standard value was chosen: 3.3 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 20 and Equation 21.

$$Iripple = \frac{Vinmax - Vout}{L1} \cdot \frac{Vout}{Vinmax \cdot fsw} \tag{19}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \cdot \left(\frac{V_o \cdot (Vinmax - Vo)}{Vinmax \cdot L1 \cdot fsw} \right)^2} \tag{20}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{21}$$

For this design, the RMS inductor current is 8.015 A and the peak inductor current is 8.839 A. The chosen inductor is a Vishay IHLP4040DZER3R3M1series 3.3 µH. It has a saturation current rating of 18.6 A (-20% inductance) and a RMS current rating of 10 A (40° C temperature rise).

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 22 shows the minimum output capacitance necessary to accomplish this.

$$Co > \frac{2 \cdot \Delta Iout}{fsw \cdot \Delta Vout} \tag{22}$$

Where ΔIout is the change in output current, Fsw is the regulators switching frequency and ΔVout is the allowable change in the output voltage. For this example, the transient load response is specified as a 7% change in Vout for a load step of 4 A. For this example, ΔIout = 4 A and ΔVout = 0.07 x 3.3 = 0.231 V. Using these numbers gives a minimum capacitance of 72.2 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 23 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, Vripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. In this case, the maximum output voltage ripple is 33mV. Under this requirement, Equation 23 yields 14.6 µF.

$$Co > \frac{1}{8 \cdot f sw} \cdot \frac{1}{\frac{Voripple}{Iripple}} \tag{23}$$

Equation 24 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 24 indicates the ESR should be less than 17.9 mΩ. In this case, the ceramic caps' ESR is much smaller than 17.9 mΩ.

$$Resr < \frac{Voripple}{Iripple} \tag{24}$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value. For this example, 2 x 47 µF 10 V X5R ceramic capacitor with 3 mΩ of ESR are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation 25 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 25 yields 485mA.

$$Icorms = \frac{Vout \cdot (Vinmax - Vout)}{\sqrt{12} \cdot Vinmax \cdot L1 \cdot f sw} \tag{25}$$

Input Capacitor Selection

The TPS54821 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 4.7 µF of effective capacitance on the PVIN input voltage pins and 4.7 µF on the Vin input voltage pin. In some applications additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54821. The input ripple current can be calculated using Equation 26.

$$Icirms = Iout \cdot \sqrt{\frac{Vout}{Vinmin} \cdot \frac{(Vinmin - Vout)}{Vinmin}} \tag{26}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 25 V voltage rating is required to support the maximum input voltage. For this example, one 10 µF and one 4.7 µF 25 V capacitors in parallel have been selected as the VIN and PVIN inputs are tied together so the TPS54821 may operate from a single supply. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 27. Using the design example values, Ioutmax = 8 A, Cin = 14.7 µF, Fsw=480 kHz, yields an input voltage ripple of 417 mV and a RMS input ripple current of 3.94 A.

$$\Delta Vin = \frac{Ioutmax \cdot 0.25}{Cin \cdot f sw} \tag{27}$$

Slow Start Capacitor Selection

The slow start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54821 reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft start capacitor value can be calculated using Equation 28. For the example circuit, the soft start time is not too critical since the output capacitor value is 2 x 47 µF which does not require much current to charge to 3.3 V. The example circuit has the soft start time set to an arbitrary value of 6 ms which requires a 22 nF capacitor. In TPS54821, Iss is 2.3 uA and Vref is 0.6V.

$$C6(nF) = \frac{Tss(ms) \cdot Iss(\mu A)}{Vref(V)} \tag{28}$$

Bootstrap Capacitor Selection

A 0.1 µF ceramic capacitor must be connected between the BOOT to PH pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10V or higher voltage rating.

Under Voltage Lockout Set Point

The Under Voltage Lock Out (UVLO) can be adjusted using the external voltage divider network of R3 and R4. R3 is connected between VIN and the EN pin of the TPS54821 and R4 is connected between EN and GND . The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 6.528V (UVLO start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 6.190 V (UVLO stop or disable). Equation 2 and Equation 3 can be used to calculate the values for the upper and lower resistor values. For the stop voltages specified the nearest standard resistor value for R3 is 35.7 kΩ and for R4 is 8.06 kΩ.

Output Voltage Feedback Resistor Selection

The resistor divider network R7 and R8 is used to set the output voltage. For the example design, 10 kΩ was selected for R7. Using Equation 29, R8 is calculated as 2.22 kΩ. The nearest standard 1% resistor is 2.21 kΩ.

$$R8 = \frac{R7 \cdot V_{REF}}{V_{OUT} - V_{REF}} \tag{29}$$

Minimum Output Voltage

Due to the internal design of the TPS54821, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.6 V. Above 0.6 V, the output voltage may be limited by the minimum controllable on time. The minimum output voltage in this case is given by Equation 30

$$Voutmin = Ontimemin \cdot Fsmax\left(Vinmax + Ioutmin\left(RDS2min - RDS1min\right)\right) - Ioutmin\left(RL + RDS2min\right)$$

Where:

Voutmin = minimum achievable output voltage

Ontimemin = minimum controllable on-time (135 nsec maximum)

Fsmax = maximum switching frequency including tolerance

Vinmax = maximum input voltage

Ioutmin = minimum load current

RDS1min = minimum high side MOSFET on resistance (36-32 mΩ typical)

RDS2min = minimum low side MOSFET on resistance (19 mΩ typical)

RL = series resistance of output inductor (30)

Compensation Component Selection

There are several possible methods to design closed loop compensation for dc/dc converters. For the ideal current mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at -20 dB/decade above the modulator pole frequency. The power stage phase is 0 degrees at low frequencies and starts to fall one decade above the modulator pole frequency reaching a minimum of -90 degrees one decade above the modulator pole frequency. The modulator pole is a simple pole shown in Equation 31

$$fp\ mod = \frac{Ioutmax}{2\pi \times Vout \times Cout} \tag{31}$$

For the TPS54821 most circuits will have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics will deviate from the ideal approximations. The phase loss of the power stage will now approach -180 degrees, making compensation more difficult. The power stage transfer function can be solved but it is a tedious hand calculation that does not lend itself to simple approximations. It is best to use Pspice or TINA-TI to accurately model the power stage gain and phase so that a reliable compensation circuit can be designed. That is the technique used in this design procedure. Using the pspice model for the TPS54821, apply the values calculated previously to the output filter components of L1, C7 and C8. Set R_{LOAD} to the appropriate value for the current value to be compensate. For this design, L1 = 3.3 µH. C7 and C8 use the derated capacitance value of 37.6 µF, and the ESR is set to 3 mΩ. The R_{LOAD} resistor is 3.3 V / 4 A = .82 Ω. Now the power stage characteristic can be plotted as shown in Figure 30.

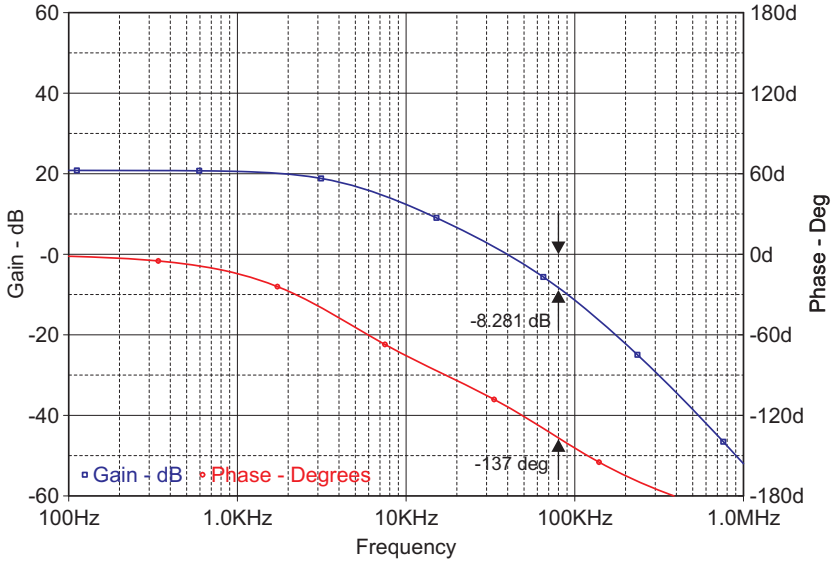


Figure 30. Power Stage Gain and Phase Characteristics

For this design, the intended crossover frequency is 80 kHz. From the power stage gain and phase plots, the gain at 80 kHz is -8.281 dB and the phase is -137 degrees. For 60 degrees of phase margin, additional phase boost from a feed forward capacitor in parallel with the upper resistor of the voltage set point divider will be required. R5 sets the gain of the compensated error amplifier to be equal and opposite the power stage gain at crossover. The required value of R5 can be calculated from Equation 32.

$$R5 = \frac{10^{\frac{-G_{PWRSTG}}{20}}}{gm_{EA}} \cdot \sqrt{\frac{V_{out}}{V_{REF}}} \tag{32}$$

To maximize phase gain, the compensator zero is placed one decade below the crossover frequency of 80 kHz. The required value for C4 is given by Equation 33.

$$C4 = \frac{1}{2 \cdot \pi \cdot R5 \cdot \frac{F_{CO}}{10}} \tag{33}$$

To maximize phase gain the high frequency pole is placed one decade above the crossover frequency of 80 kHz. The required value for C5 can be calculated from Equation 34.

$$C5 = \frac{1}{2 \cdot \pi \cdot R5 \cdot F_P} \tag{34}$$

The feed forward capacitor C9, is used to increase the phase boost at crossover above what is normally available from Type II compensation. It places an additional zero/pole pair located at Equation 35 and Equation 36.

$$F_Z = \frac{1}{2 \cdot \pi \cdot C9 \cdot R7} \tag{35}$$

$$F_P = \frac{1}{2 \cdot \pi \cdot C9 \cdot R7 \,||\, R8} \tag{36}$$

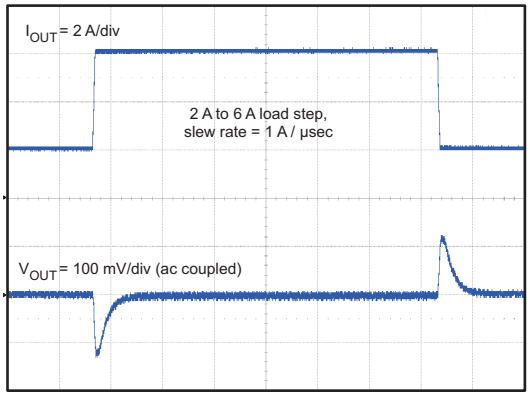
This zero and pole pair is not independent. Once the zero location is chosen, the pole is fixed as well. For optimum performance, the zero and pole should be located symmetrically about the intended crossover frequency. The required value for C9 can calculated from Equation 37.

$$C9 = \frac{1}{2 \cdot \pi \cdot R7 \cdot F_{CO} \cdot \sqrt{\frac{V_{REF}}{V_{OUT}}}} \tag{37}$$

For this design the calculated values for the compensation components are R5 = 4.68 kΩ ,C4 = 4290 pF, C5 = 42.9 pF and C9 = 467 pF. Using standard values, the compensation components are R5 = 4.64 kΩ ,C4 = 3900 pF, C5 = 39 pF and C9 = 470 pF.

Application Curves

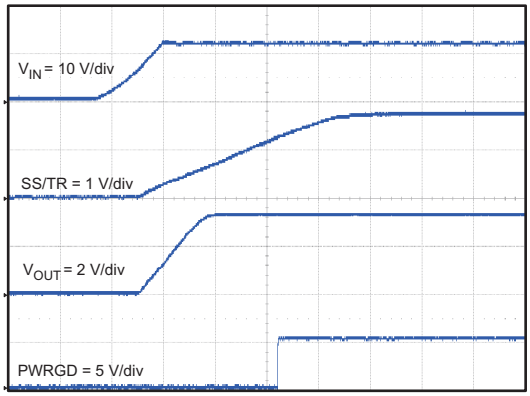
LOAD TRANSIENT



Time = 100 µs/div

Figure 31.

STARTUP with VIN



Time = 5 ms/div

Figure 32.

STARTUP with EN

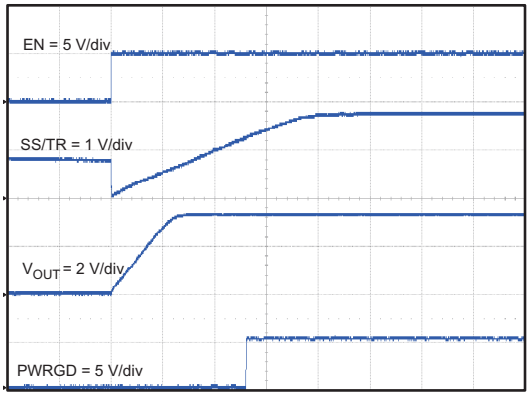


Figure 33.

STARTUP with PRE-BIAS

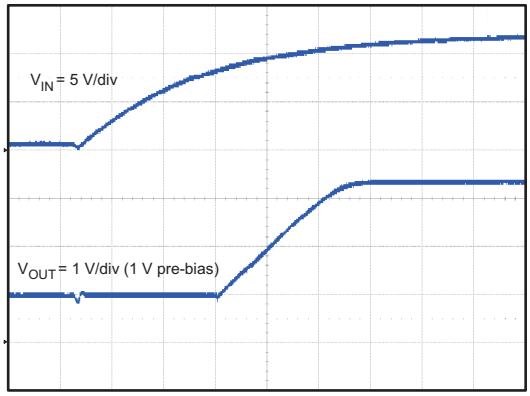


Figure 34.

OUTPUT VOLTAGE RIPPLE with FULL LOAD

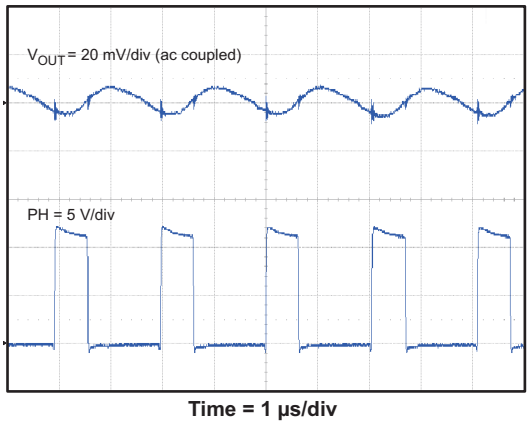


Figure 35.

INPUT VOLTAGE RIPPLE with FULL LOAD

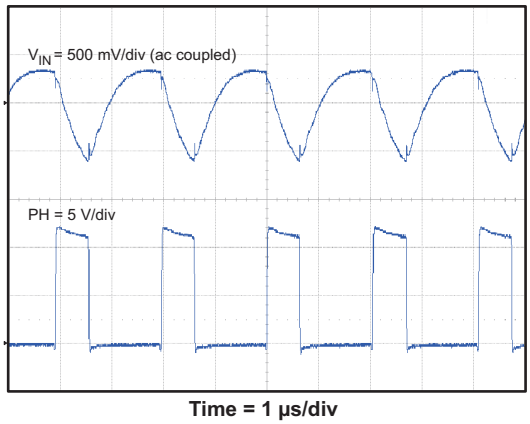


Figure 36.

CLOSED LOOP RESPONSE, I_{OUT} = 4 A

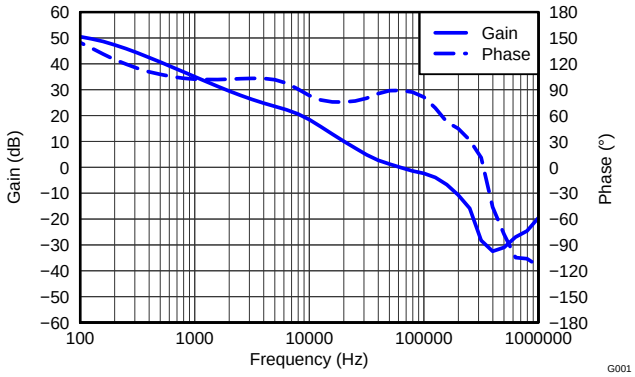


Figure 37.

LINE REGULATION

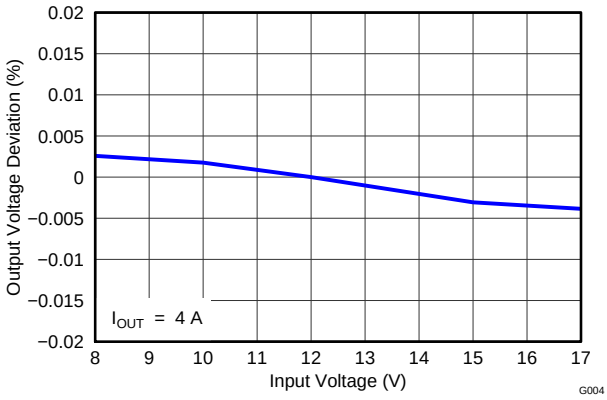


Figure 38.

LOAD REGULATION

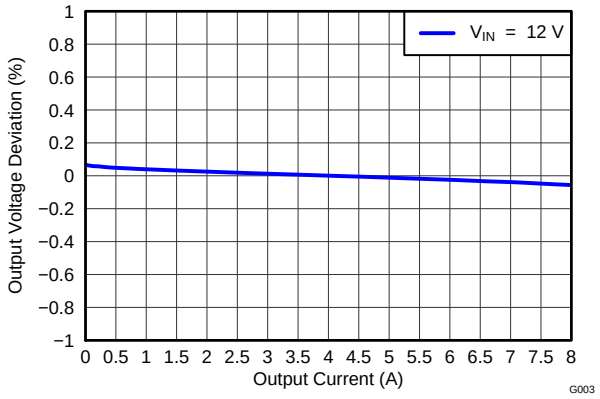


Figure 39.

TRACKING PERFORMANCE

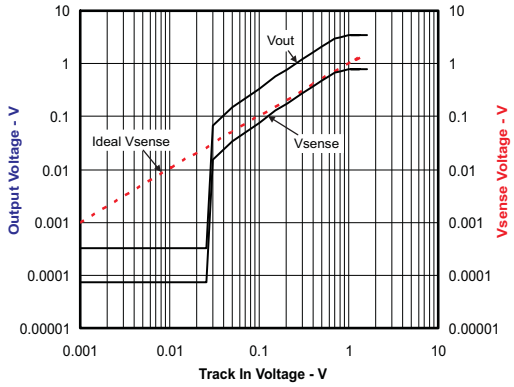


Figure 40.

MAXIMUM AMBIENT TEMPERATURE vs LOAD CURRENT

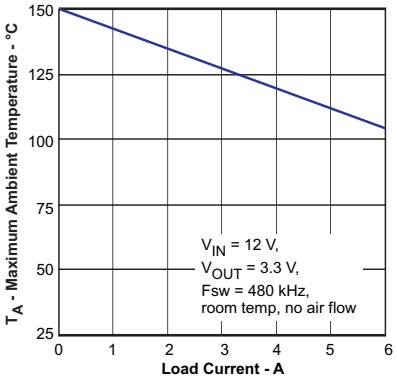


Figure 41.

EFFICIENCY vs LOAD CURRENT

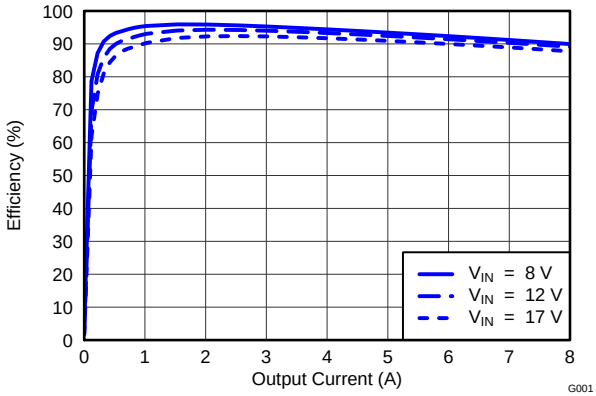


Figure 42.

EFFICIENCY vs OUTPUT CURRENT

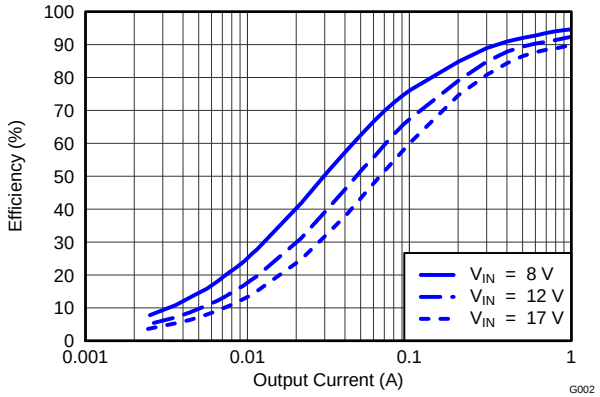


Figure 43.

TPS54821 Hiccup Mode Current Limit

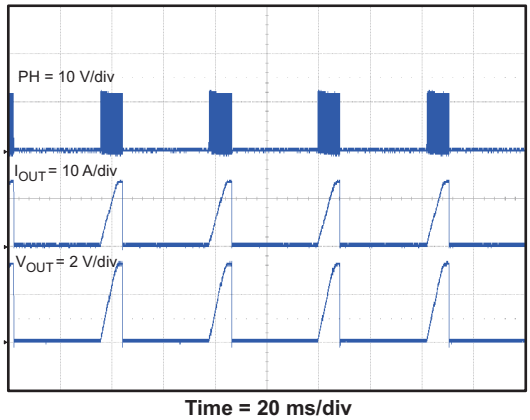


Figure 44.

Fast Transient Considerations

In applications where fast transient responses are important, Type III frequency compensation can be used instead of the traditional Type II frequency compensation.

For more information about Type II and Type III frequency compensation circuits, see *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) and Design Calculator (SLVC219).

PCB Layout Guidelines

Layout is a critical portion of good power supply design. See Figure 45 for a PCB layout example. The top layer contains the main power traces for VIN, VOUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54821 and a large top side area filled with ground. The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS54821 device to provide a thermal path from the exposed thermal pad land to ground. The GND pin should be tied directly to the power pad under the IC and the power pad. For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections. The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric. Make sure to connect this capacitor to the quite analog ground trace rather than the power ground trace of the PVIn bypass capacitor. Since the PH connection is the switching node, the output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components should be grounded to the analog ground path as shown. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

Land pattern and stencil information is provided in the data sheet addendum. The dimension and outline information is for the standard RHL (S-PVQFN-N14) package. There may be slight differences between the provided data and actual lead frame used on the TPS54821RHL package.

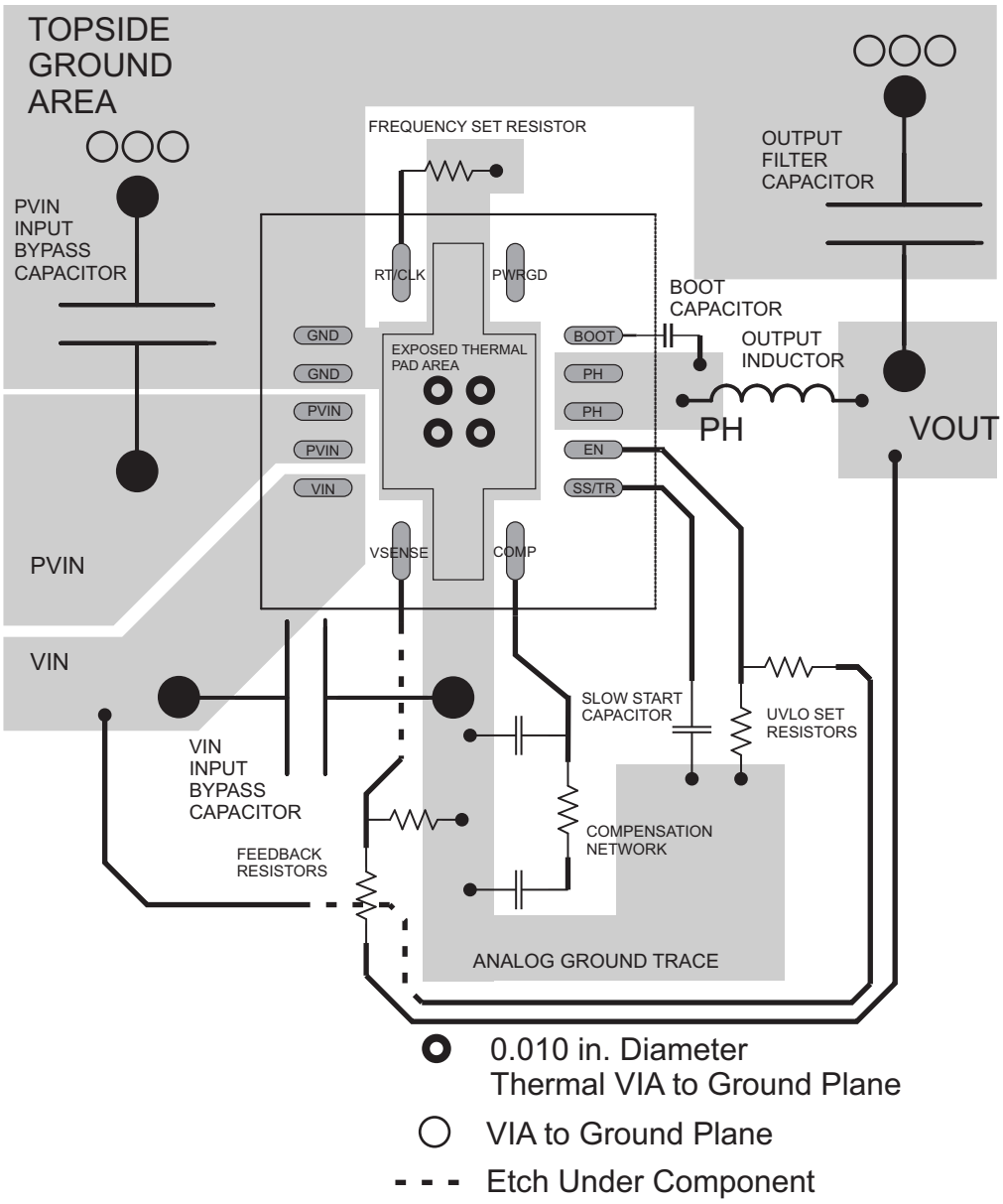


Figure 45. PCB Layout

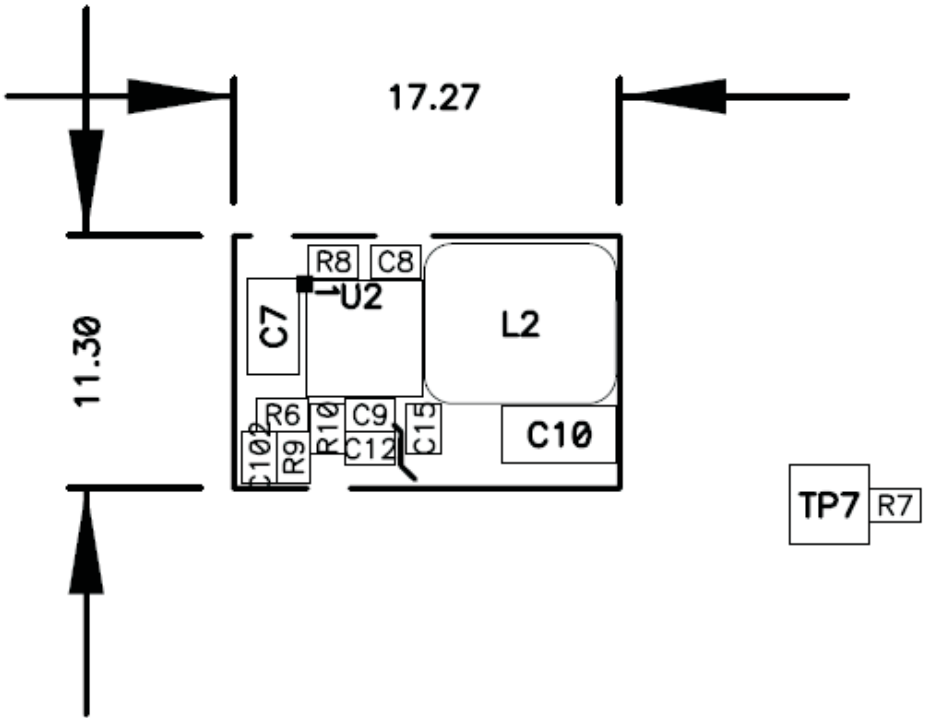


Figure 46. Ultra-Small PCB Layout Using TPS54821 (PMP4854-2)

Estimated Circuit Area

The estimated printed circuit board area for the components used in the design of Figure 29 is 0.58 in^2 (374mm^2). This area does not include test points or connectors.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54821RHLR	Active	Production	VQFN (RHL) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	54821
TPS54821RHLR.A	Active	Production	VQFN (RHL) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	54821
TPS54821RHLR.B	Active	Production	VQFN (RHL) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	54821
TPS54821RHLRG4.A	Active	Production	VQFN (RHL) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	54821
TPS54821RHLRG4.B	Active	Production	VQFN (RHL) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	54821
TPS54821RHLT	Active	Production	VQFN (RHL) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	54821
TPS54821RHLT.A	Active	Production	VQFN (RHL) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	54821
TPS54821RHLT.B	Active	Production	VQFN (RHL) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	54821

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

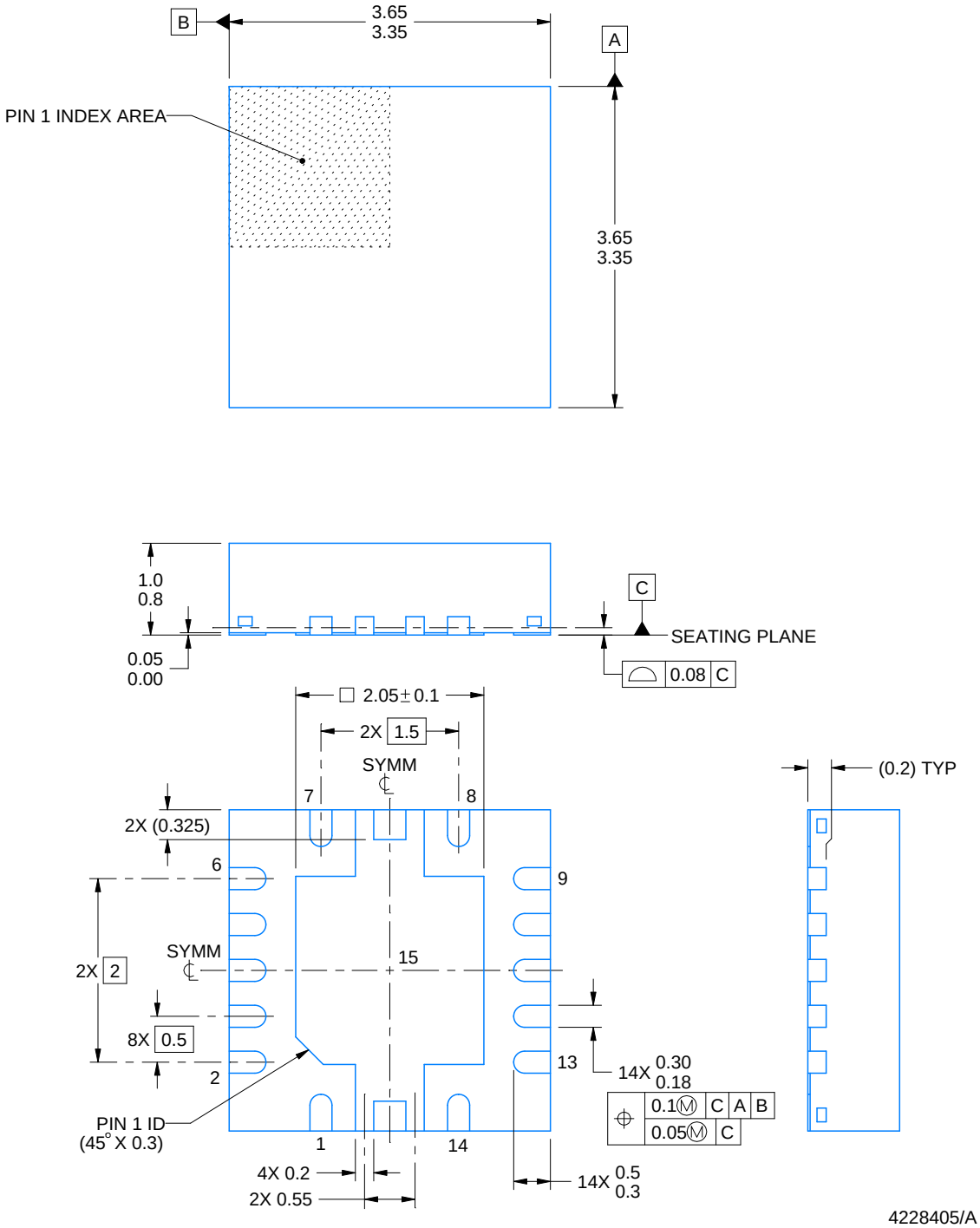
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RHL0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

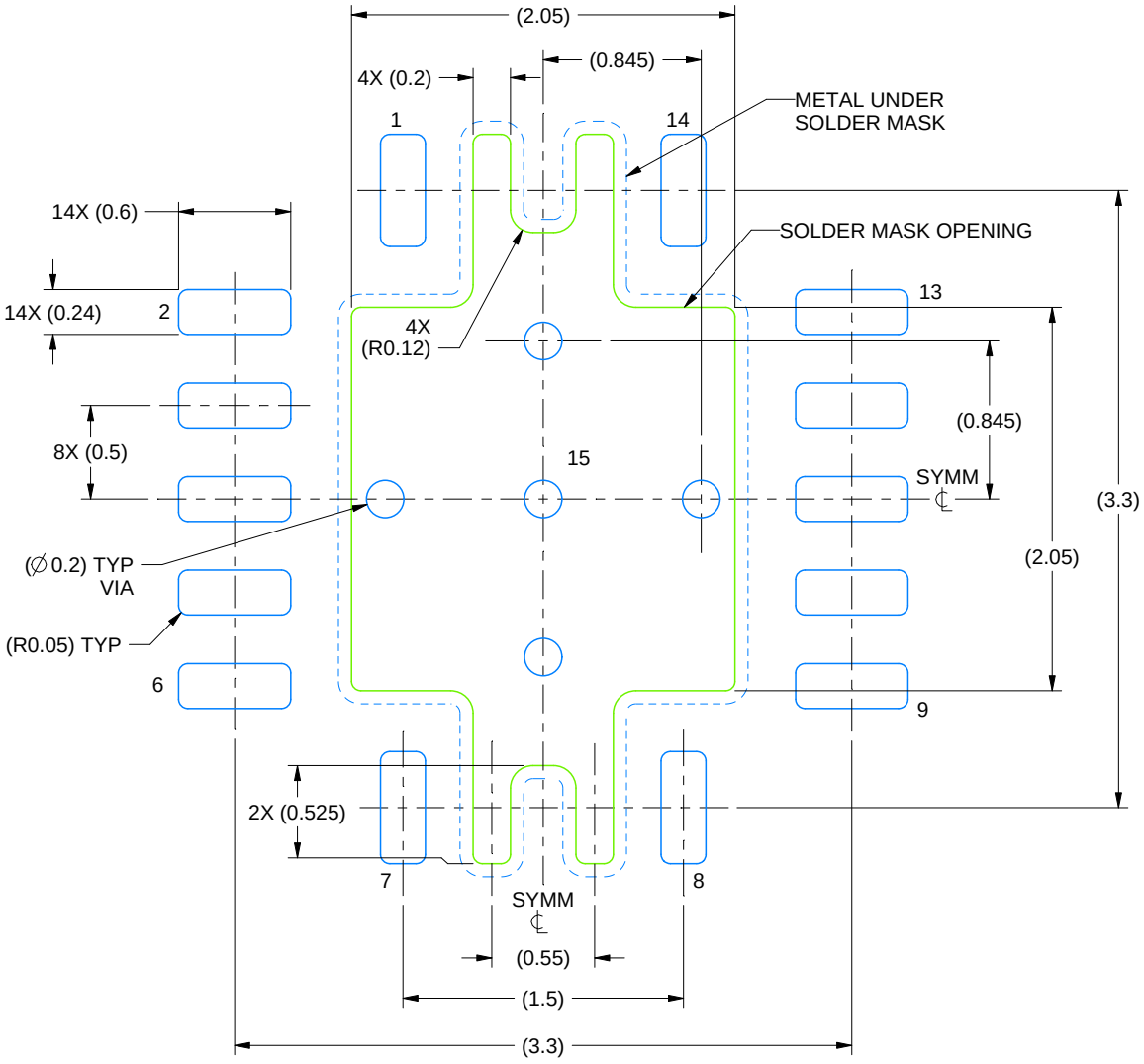
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

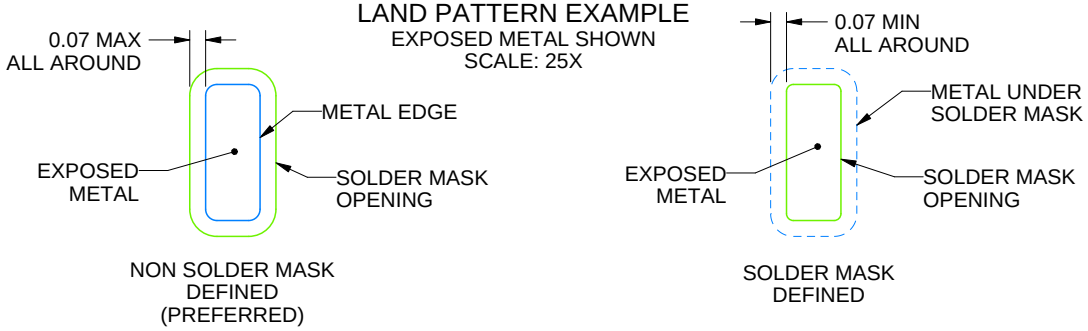
RHL0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

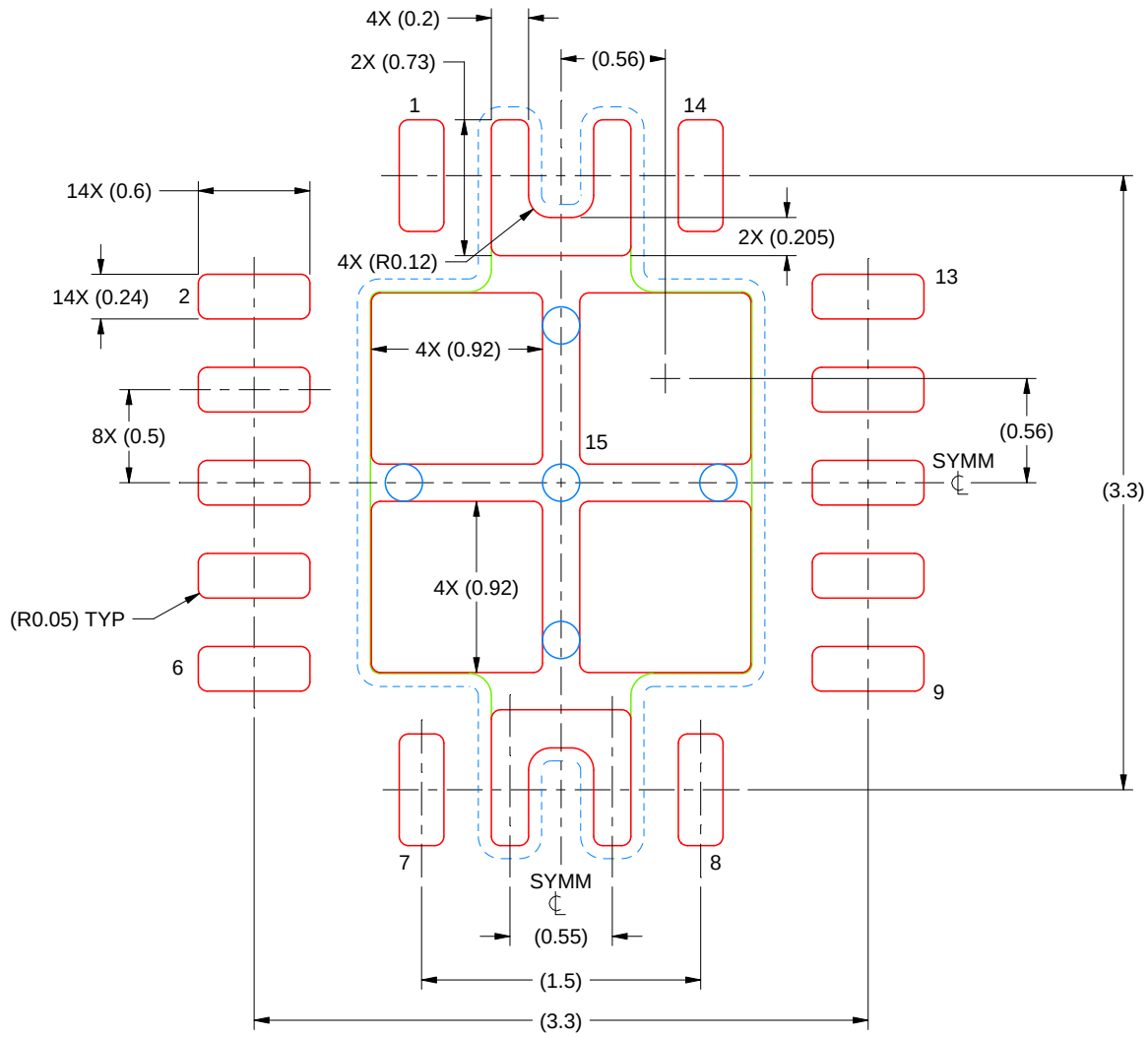


SOLDER MASK DETAILS

4228405/A 01/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
79% PRINTED COVERAGE BY AREA
SCALE: 25X

4228405/A 01/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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