支持软启动和 Eco-Mode™ 的 4.5V 至 42V 输入，3.5A 降压直流 - 直流转换器

查询样片: TPS54341

特性

- 轻负载条件下使用脉冲跳跃实现的高效率 **Eco-mode™**
- **87mΩ** 高侧金属氧化物半导体场效应晶体管 **(MOSFET)**
- **152μA** 静态运行电流和 **2μA** 关断电流
- **100KHz** 至 **2.5MHz** 可调节开关频率
- 同步至外部时钟
- 轻负载条件下使用集成型引导 **(BOOT)** 再充电场效应晶体管 **(FET)** 实现的低压降
- 可调欠压闭锁 **(UVLO)** 电压和滞后
- 欠压 **(UV)** 和过压 **(OV)** 电源正常输出
- 可调软启动和定序
- **0.8V 1%** 内部电压基准
- 带有散热垫的 **10** 引脚小外形尺寸无引线 **(SON)** 封装
- **-40°C** 至 **150°C** T_J 运行范围
- 由 **WEBENCH®** 软件工具支持

应用范围

- 工业自动化和电机控制
- 车辆附件：全球卫星定位 **(GPS)**（请参见 SLVA412），娱乐系统
- **USB** 专用充电端口和电池充电器（请参见 SLVA464）
- **12V** 和 **24V** 工业、汽车和通信电源系统

描述

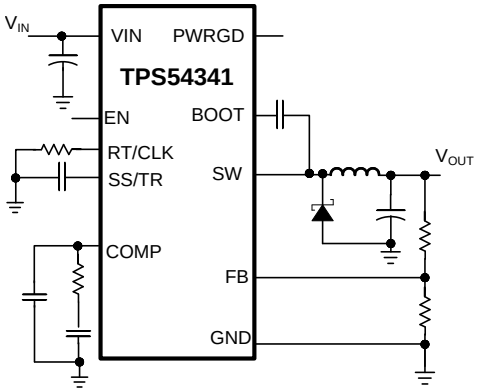
TPS54341 器件是一款 42V 3.5A 降压型稳压器，此稳压器具有一个集成型高侧 MOSFET。 按照 ISO 7637 标准，此器件能够耐受高达 45V 的抛负载脉冲。 电流模式控制提供了简单的外部补偿和灵活的组件选择。 一个低纹波脉冲跳跃模式将无负载输出电源电流减小至 152μA。 当使能引脚被拉至低电平时，关断电源电流被减少至 2μA。

欠压闭锁在内部设定为 4.3V，但可用一个使能引脚上的外部电阻分压器将之提高。 输出电压启动斜坡由软启动引脚控制，该引脚还可被配置用来控制定序/跟踪。 一个开漏电源正常信号表示输出处于标称电压值的 93% 至 106% 之内。

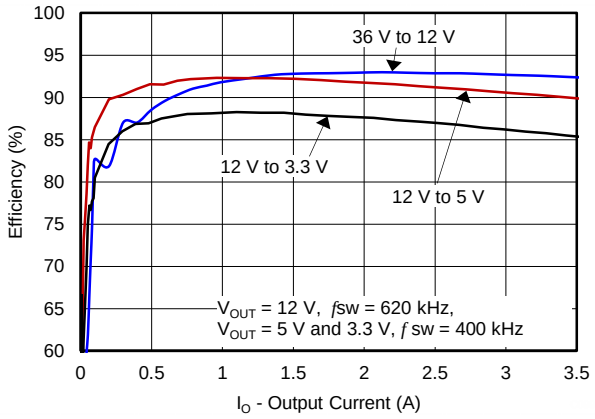
宽可调开关频率范围可针对效率或者外部组件尺寸进行优化。 逐周期电流限制、频率折返和热关断在过载条件下保护内部和外部组件。

TPS54341 器件采用 10 引脚 4mm x 4mm SON 封装。

简化电路原理图



效率与负载电流间的关系



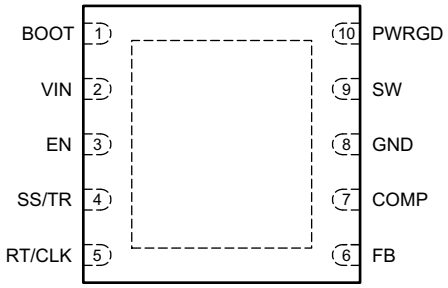
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION

PIN CONFIGURATION

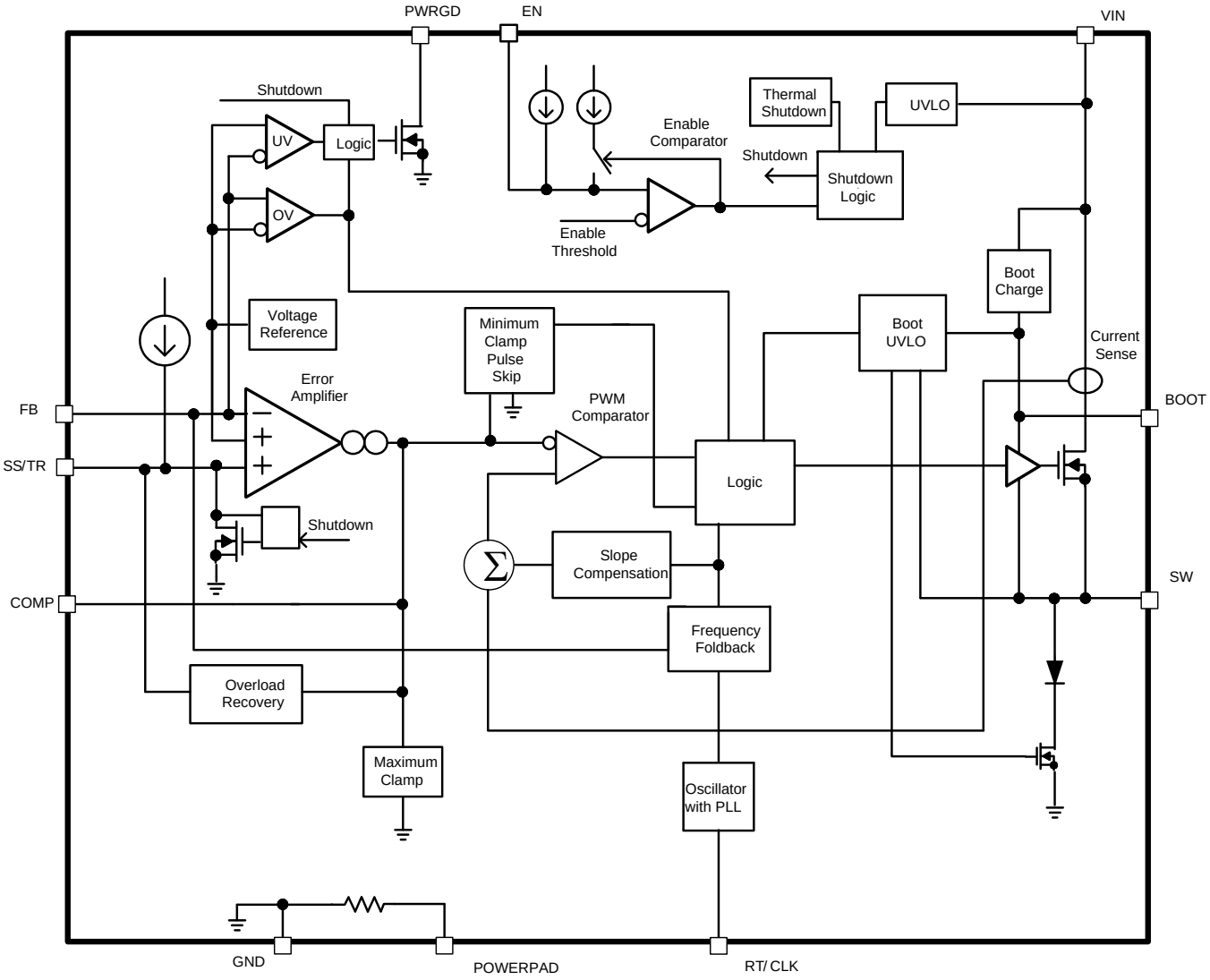
DPR PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and SW. If the voltage on this capacitor is below the minimum required to operate the high-side MOSFET, the gate drive switches off until the capacitor refreshes.
COMP	7	O	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this pin.
EN	3	I	Enable pin, with internal pullup current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors. See the Enable and Adjusting Undervoltage Lockout section.
FB	6	I	Inverting input of the transconductance (gm) error amplifier.
GND	8	–	Ground
PWRGD	10	O	Power Good is an open drain output that asserts low if the output voltage is out of regulation due to thermal shutdown, dropout, over-voltage or EN shut down
RT/CLK	5	I	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high-impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier re-enables and the operating mode returns to resistor frequency programming.
SS/TR	4	I	Soft-start and Tracking. An external capacitor connected to this pin sets the output rise time. Because the voltage on this pin overrides the internal reference, SS/TR can be used for tracking and sequencing.
SW	9	I	The source of the internal high-side power MOSFET and switching node of the converter.
VIN	2	I	Input supply voltage with 4.5-V to 42-V operating range.
Thermal Pad	11	–	The GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage	VIN	–0.3	45	V
	EN	–0.3	8.4	
	BOOT		53	
	FB	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	6	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	3.6	
Output voltage	BOOT-SW		8	V
	SW	–0.6	45	
	SW, 10-ns Transient	–2	45	
Electrostatic Discharge (HBM) QSS 009-105 (JESD22-A114A)			2	kV
Electrostatic Discharge (CDM) QSS 009-147 (JESD22-C101B.01)			500	V
Operating junction temperature		–40	150	°C
Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1) (2)		TPS54341	UNITS
		DPR (10 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance (standard board)	35.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	12.5	
θ_{JCtop}	Junction-to-case(top) thermal resistance	34.1	
θ_{JCbot}	Junction-to-case(bottom) thermal resistance	2.2	
θ_{JB}	Junction-to-board thermal resistance	12.3	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) Power rating at a specific ambient temperature TA should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See power dissipation estimate in application section of this data sheet for more information.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 150°C, VIN = 4.5 to 42 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
	Operating input voltage		4.5		42	V
	Internal undervoltage lockout threshold	Rising	4.1	4.3	4.48	V
	Internal undervoltage lockout threshold hysteresis			325		mV
	Shutdown supply current	EN = 0 V, 25°C, 4.5 V ≤ VIN ≤ 42 V		2.25	4.5	μA
	Operating: nonswitching supply current	FB = 0.9 V, T_A = 25°C		152	200	μA
ENABLE AND UVLO (EN PIN)						
	Enable threshold voltage	No voltage hysteresis, rising and falling	1.1	1.2	1.3	V
	Input current	Enable threshold +50 mV		–4.6		μA
		Enable threshold –50 mV	–0.58	–1.2	–1.8	μA
	Hysteresis current		–2.2	–3.4	–4.5	μA
	Enable to COMP active	V_{IN} = 12 V, T_A = 25°C		540		μs
VOLTAGE REFERENCE						
	Voltage reference		0.792	0.8	0.808	V
HIGH-SIDE MOSFET						
	On-resistance	VIN = 12 V, BOOT-SW = 6 V		87	185	mΩ
ERROR AMPLIFIER						
	Input current			50		nA
	Error amplifier transconductance (gm)	–2 μA < I_{COMP} < 2 μA, V_{COMP} = 1 V		350		μMhos
	Error amplifier transconductance (gm) during soft-start	–2 μA < I_{COMP} < 2 μA, V_{COMP} = 1 V, V_{FB} = 0.4 V		77		μMhos
	Error amplifier DC gain	V_{FB} = 0.8 V		10 000		V/V
	Min unity gain bandwidth			2500		kHz
	Error amplifier source and sink	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±30		μA
	COMP to SW current transconductance			12		A/V
CURRENT LIMIT						
	Current limit threshold	All VIN and temperatures, Open Loop(1)	4.5	5.5	6.8	A
		All temperatures, VIN = 12 V, Open Loop(1)	4.5	5.5	6.3	A
		VIN = 12 V, T_A = 25°C, Open Loop(1)	5.2	5.5	5.9	A
	Current limit threshold delay			60		ns
THERMAL SHUTDOWN						
	Thermal shutdown			176		°C
	Thermal shutdown hysteresis			12		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	Switching frequency range using RT mode		100		2500	kHz
f_{SW}	Switching frequency	R_T = 200 kΩ	450	500	550	kHz
	Switching frequency range using CLK mode		160		2300	kHz
	Minimum CLK input pulse width			15		ns
	RT/CLK high threshold			1.55	2	V
	RT/CLK low threshold		0.5	1.2		V
	RT/CLK falling edge to SW rising edge delay	Measured at 500 kHz with RT resistor in series		55		ns
	PLL lock in time	Measured at 500 kHz		78		μs
SOFT START AND TRACKING (SS/TR PIN)						
	Charge current	$V_{SS/TR}$ = 0.4 V		1.7		μA

(1) Open Loop current limit measured directly at the SW pin and is independent of the inductor value and slope compensation.

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 150°C, VIN = 4.5 to 42 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SS/TR-to-FB matching	$V_{SS/TR}$ = 0.4 V		42		mV
SS/TR-to-reference crossover	98% nominal		1.16		V
SS/TR discharge current (overload)	FB = 0 V, $V_{SS/TR}$ = 0.4 V		354		µA
SS/TR discharge voltage	FB = 0 V		54		mV
POWER GOOD (PWRGD PIN)					
FB threshold for PWRGD low	FB falling		90		%
FB threshold for PWRGD high	FB rising		93		%
FB threshold for PWRGD low	FB rising		108		%
FB threshold for PWRGD high	FB falling		106		%
Hysteresis	FB falling		2.5		%
Output high leakage	V_{PWRGD} = 5.5 V, T_A = 25°C		10		nA
On resistance	I_{PWRGD} = 3 mA, V_{FB} < 0.79 V		45		Ω
Minimum VIN for defined output	V_{PWRGD} < 0.5 V, I_{PWRGD} = 100 µA		0.9	2	V

TYPICAL CHARACTERISTICS

ON RESISTANCE vs JUNCTION TEMPERATURE

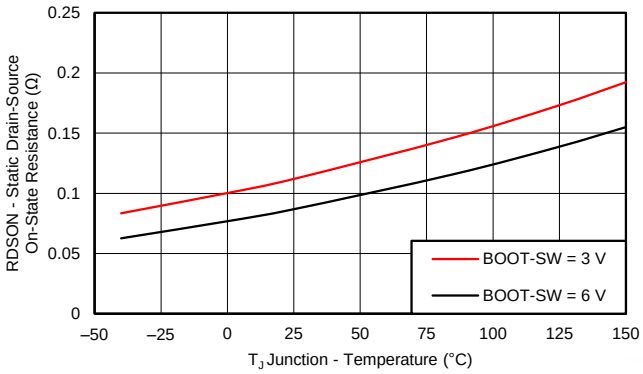


Figure 1.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

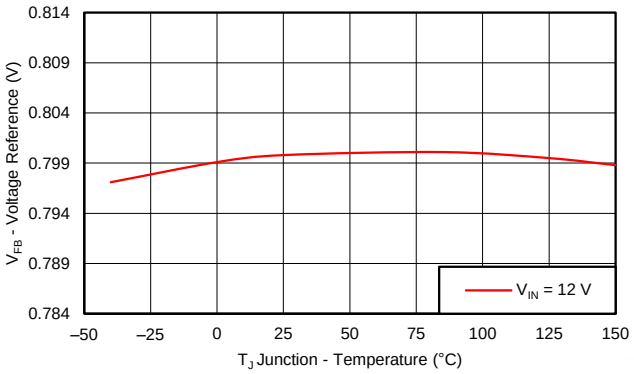


Figure 2.

SWITCH CURRENT LIMIT vs JUNCTION TEMPERATURE

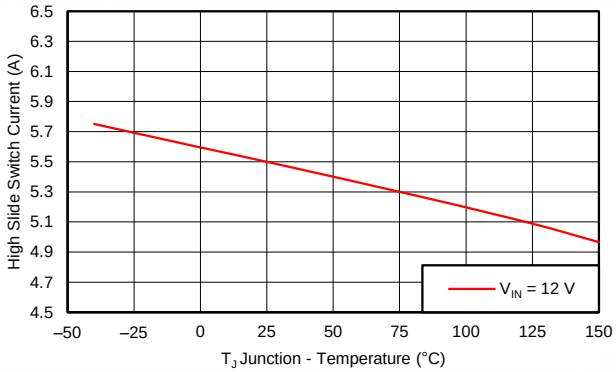


Figure 3.

SWITCH CURRENT LIMIT vs INPUT VOLTAGE

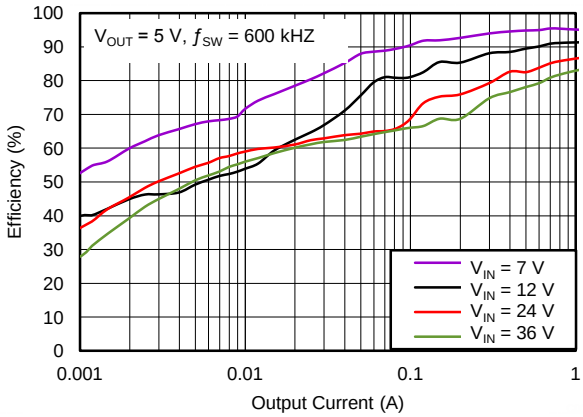


Figure 4.

SWITCHING FREQUENCY vs JUNCTION TEMPERATURE

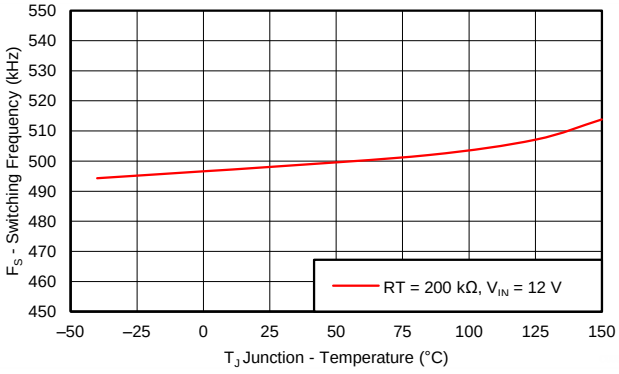


Figure 5.

SWITCHING FREQUENCY vs RT/CLK RESISTANCE LOW FREQUENCY RANGE

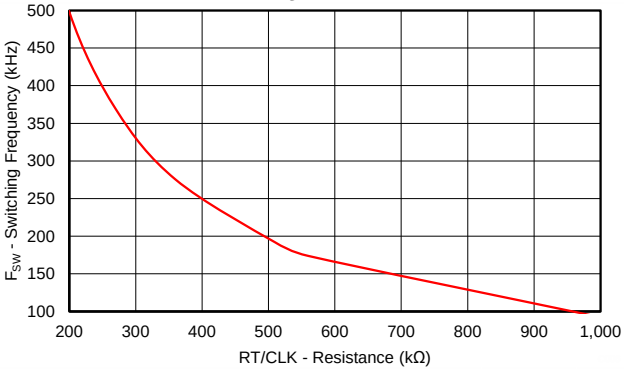


Figure 6.

TYPICAL CHARACTERISTICS (continued)

SWITCHING FREQUENCY vs RT/CLK RESISTANCE HIGH FREQUENCY RANGE

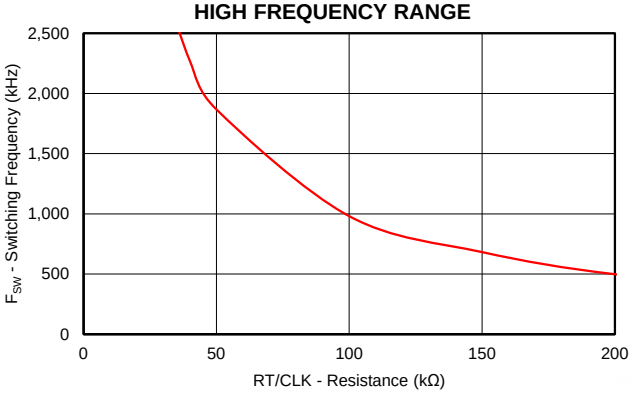


Figure 7.

EA TRANSCONDUCTANCE vs JUNCTION TEMPERATURE

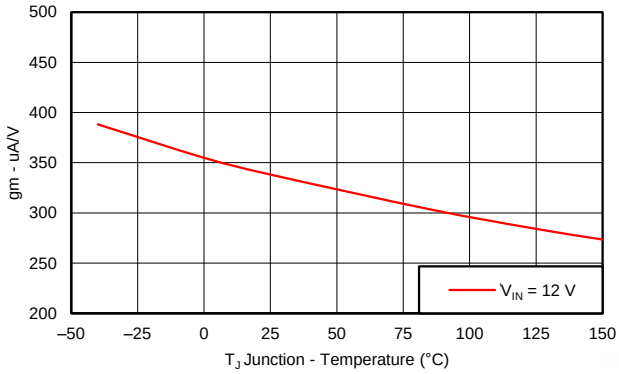


Figure 8.

EA TRANSCONDUCTANCE DURING SOFT-START vs JUNCTION TEMPERATURE

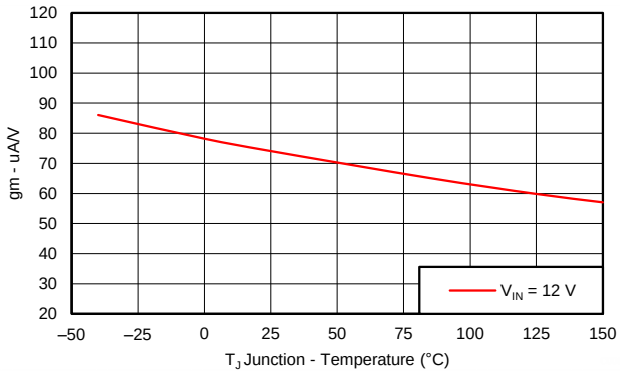


Figure 9.

EN PIN VOLTAGE vs JUNCTION TEMPERATURE

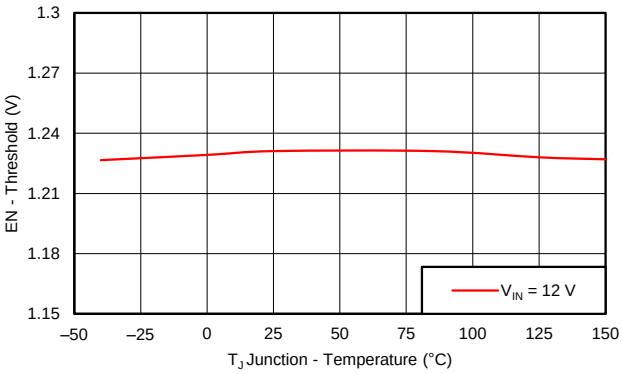


Figure 10.

EN PIN CURRENT vs JUNCTION TEMPERATURE

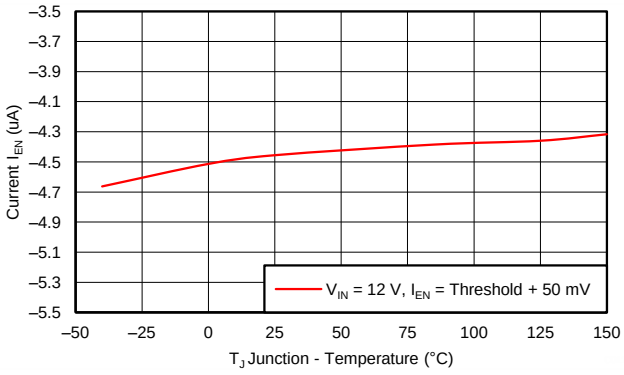


Figure 11.

EN PIN CURRENT vs JUNCTION TEMPERATURE

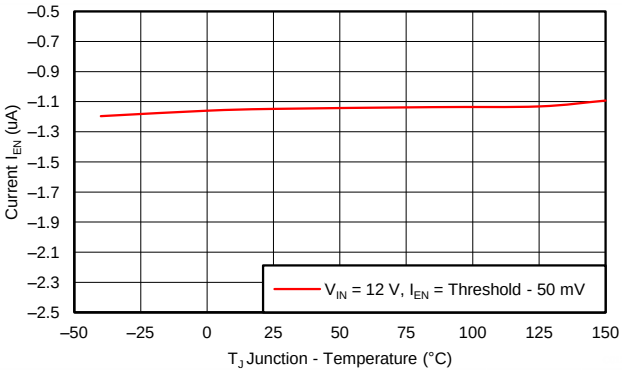


Figure 12.

TYPICAL CHARACTERISTICS (continued)

EN PIN CURRENT HYSTERESIS VS JUNCTION TEMPERATURE

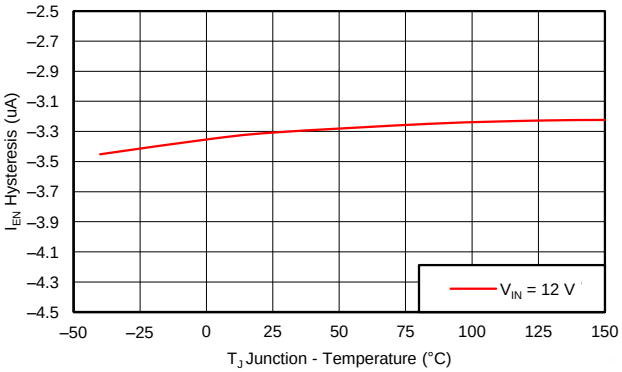


Figure 13.

SWITCHING FREQUENCY VS FB

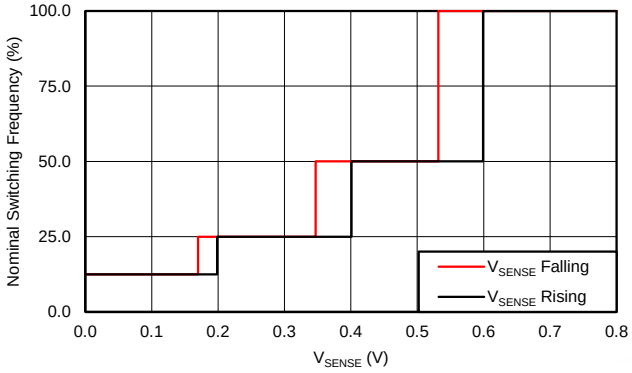


Figure 14.

SHUTDOWN SUPPLY CURRENT VS JUNCTION TEMPERATURE

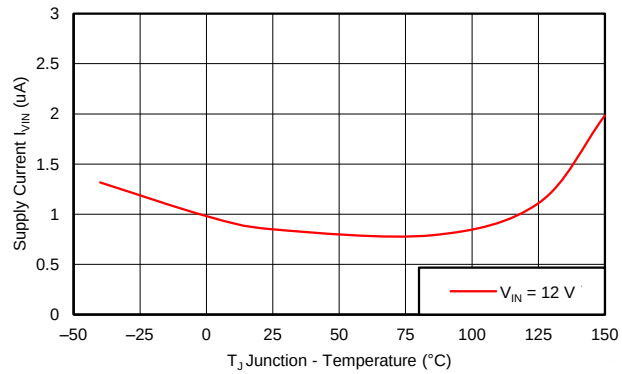


Figure 15.

SHUTDOWN SUPPLY CURRENT VS INPUT VOLTAGE (V_{IN})

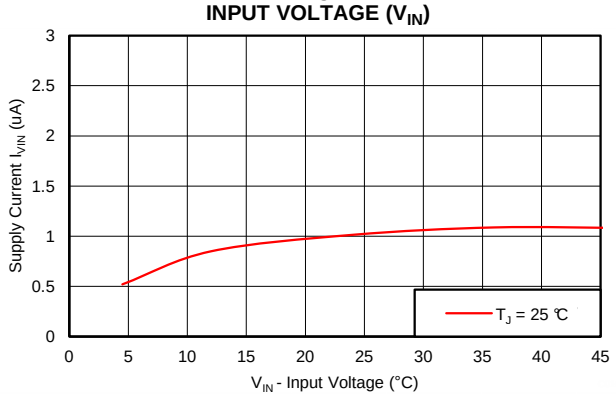


Figure 16.

V_{IN} SUPPLY CURRENT VS JUNCTION TEMPERATURE

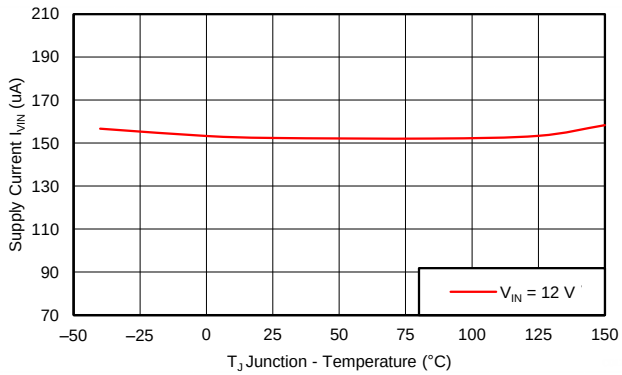


Figure 17.

V_{IN} SUPPLY CURRENT VS INPUT VOLTAGE

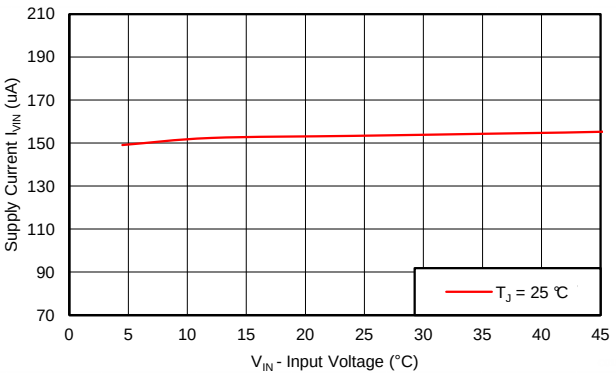


Figure 18.

TYPICAL CHARACTERISTICS (continued)

BOOT-SW UVLO vs JUNCTION TEMPERATURE

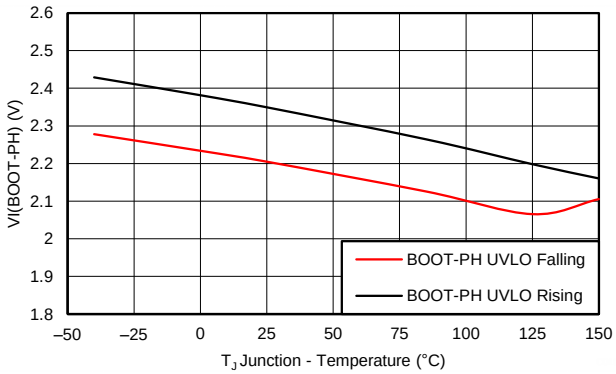


Figure 19.

INPUT VOLTAGE UVLO vs JUNCTION TEMPERATURE

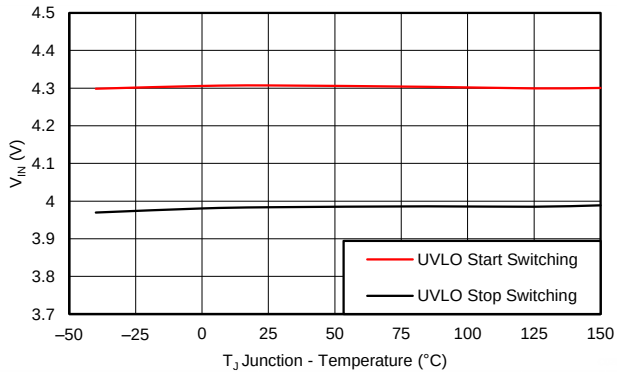


Figure 20.

PWRGD ON RESISTANCE vs JUNCTION TEMPERATURE

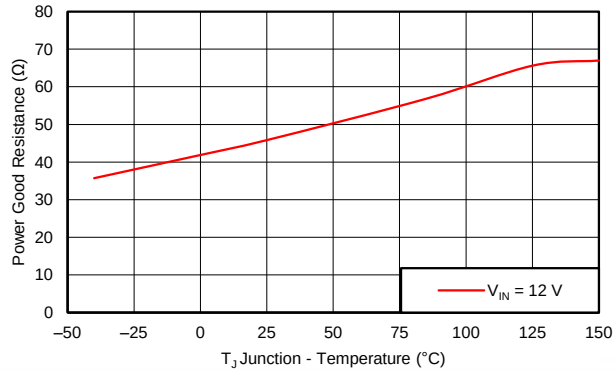


Figure 21.

PWRGD THRESHOLD vs JUNCTION TEMPERATURE

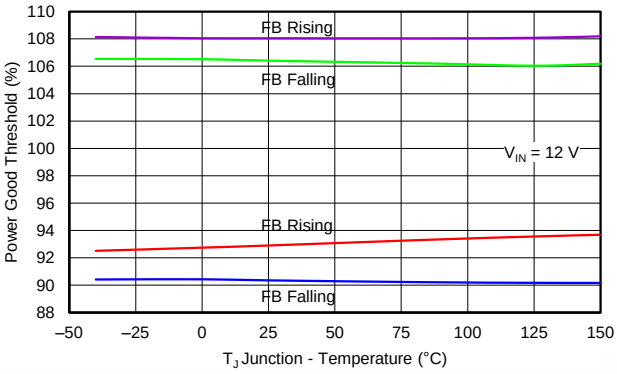


Figure 22.

SS/TR to FB OFFSET vs FB

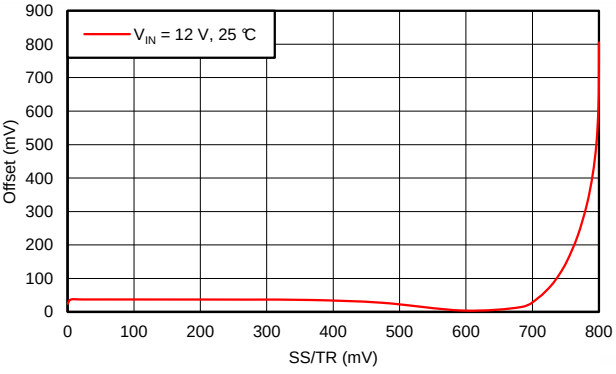


Figure 23.

SS/TR to FB OFFSET vs TEMPERATURE

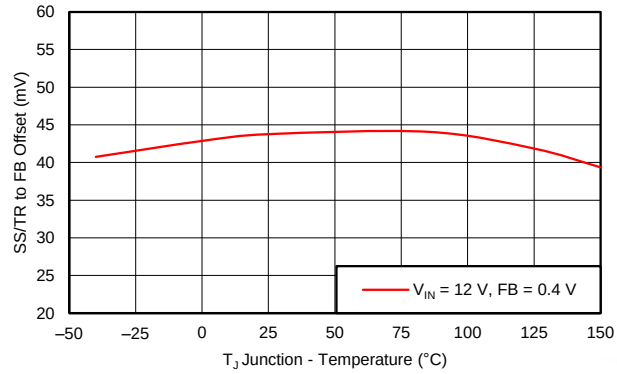


Figure 24.

TYPICAL CHARACTERISTICS (continued)

5-V START and STOP VOLTAGE (see Low Dropout Operation and Bootstrap Voltage (BOOT))

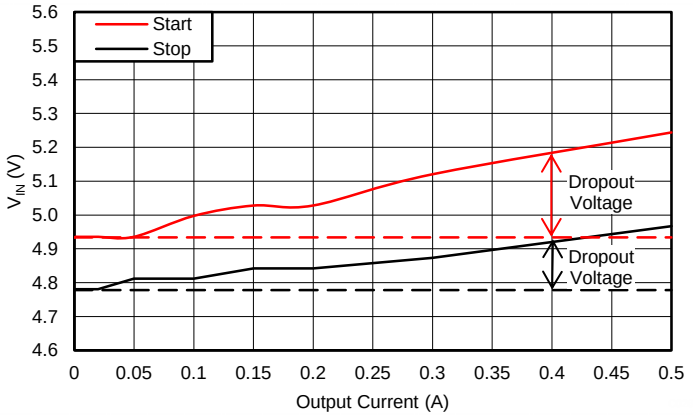


Figure 25.

OVERVIEW

The TPS54341 device is a 42-V 3.5-A, step-down (buck) regulator with an integrated high-side n-channel MOSFET. The device implements constant-frequency current-mode control which reduces output capacitance and simplifies external frequency compensation. The wide switching frequency range of 100 to 2500 kHz allows for either efficiency or size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground connected to the RT/CLK pin. The device has an internal phase-locked loop (PLL) connected to the RT/CLK pin that synchronizes the power switch turn-on to a falling edge of an external clock signal.

The TPS54341 device has a default input-startup voltage of 4.3 V typical. The EN pin adjusts the input-voltage undervoltage-lockout (UVLO) threshold with two external resistors. An internal-pullup current source enables operation when the EN pin is floating. The operating current is 152 μA under a no-load condition when not switching. When the device is disabled, the supply current is 2 μA.

The integrated 87-mΩ high-side MOSFET supports high-efficiency power-supply designs capable of delivering 3.5 A of continuous current to a load. The gate-drive bias voltage for the integrated high-side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to SW pins. The TPS54341 device reduces the external component count by integrating the bootstrap recharge diode. The BOOT pin capacitor voltage is monitored by a UVLO circuit which turns off the high-side MOSFET when the BOOT to SW voltage falls below a preset threshold. An automatic BOOT capacitor recharge circuit allows the TPS54341 device to operate at high duty cycles approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The minimum output voltage is the internal 0.8-V feedback reference.

Output overvoltage transients are minimized by an Overvoltage Protection (OVP) comparator. When the OVP comparator is activated, the high-side MOSFET turns off and remains off until the output voltage is less than 106% of the desired output voltage.

The SS/TR (soft-start/tracking) pin minimizes inrush currents or provides power-supply sequencing during power up. A small value capacitor must be connected to the pin to adjust the soft-start time. A resistor divider can be connected to the pin for critical power-supply sequencing requirements. The SS/TR pin is discharged before the output powers up. This discharging ensures a repeatable restart after an overtemperature fault, UVLO fault, or a disabled condition. When the overload condition is removed, the soft-start circuit controls the recovery from the fault output level to the nominal regulation voltage. A frequency-foldback circuit reduces the switching frequency during startup and overcurrent fault conditions to help maintain control of the inductor current.

DETAILED DESCRIPTION

Fixed Frequency PWM Control

The TPS54341 device uses fixed-frequency peak-current-mode control with adjustable switching frequency. The output voltage is compared through external resistors connected to the FB pin to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn-on of the high-side power switch. The error amplifier output at the COMP pin controls the high-side power switch current. When the high-side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch turns off. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements current limiting by clamping the COMP pin voltage to a maximum level. The pulse skipping Eco-mode is implemented with a minimum voltage clamp on the COMP pin.

Slope Compensation Output Current

The TPS54341 device adds a compensating ramp to the MOSFET switch current-sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty-cycle range.

Pulse Skip Eco-mode

The TPS54341 device operates in a pulse-skipping Eco-mode at light load currents to improve efficiency by reducing switching and gate drive losses. If the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse skipping current threshold, the device enters Eco-mode. The pulse-skipping current threshold is the peak switch-current level corresponding to a nominal COMP voltage of 600 mV.

DETAILED DESCRIPTION (continued)

When in Eco-mode, the COMP pin voltage is clamped at 600 mV and the high-side MOSFET is inhibited. Because the device is not switching, the output voltage begins to decay. The voltage-control loop responds to the falling output voltage by increasing the COMP pin voltage. The high-side MOSFET enables and switching resumes when the error amplifier lifts COMP above the pulse skipping threshold. The output voltage recovers to the regulated value, and COMP eventually falls below the Eco-mode pulse skipping threshold at which time the device again enters Eco-mode. The internal PLL remains operational when in Eco-mode. When operating at light load currents in Eco-mode, the switching transitions occur synchronously with the external clock signal.

During Eco-mode operation, the TPS54341 device senses and controls peak switch current, not the average load current. Therefore the load current at which the device enters Eco-mode is dependent on the output inductor value. The circuit in Figure 46 enters Eco-mode at 30-mA output current. As the load current approaches zero, the device enters a pulse-skip mode during which it draws only 152-µA input quiescent current.

Low Dropout Operation and Bootstrap Voltage (BOOT)

The TPS54341 device provides an integrated bootstrap-voltage regulator. A small capacitor between the BOOT and SW pins provides the gate-drive voltage for the high-side MOSFET. The BOOT capacitor refreshes when the high-side MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended for stable performance over temperature and voltage.

When operating with a low voltage difference from input to output, the high-side MOSFET of the TPS54341 device operates at 100% duty cycle as long as the BOOT to SW pin voltage is greater than 2.1 V. When the voltage from BOOT to SW drops below 2.1 V, the high-side MOSFET turns off and an integrated low-side MOSFET pulls SW low to recharge the BOOT capacitor. To reduce the losses of the small low-side MOSFET at high output voltages, the low-side MOSFET is disabled at 24 V output and re-enabled when the output reaches 21.5 V.

Because the gate-drive current sourced from the BOOT capacitor is small, the high-side MOSFET remains on for many switching cycles before the MOSFET turns off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 100%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low-side diode voltage, and the printed circuit-board resistance.

The start and stop voltage for a typical 5-V output application is shown in Figure 25 where the input voltage is plotted versus load current. The start voltage is defined as the input voltage required to regulate the output within 1% of nominal. The stop voltage is defined as the input voltage at which the output drops by 5% or where switching stops.

During high duty-cycle (low dropout) conditions, inductor current-ripple increases when the BOOT capacitor recharges resulting in an increase in output-voltage ripple. Increased ripple occurs when the off time required to recharge the BOOT capacitor is longer than the high-side off time associated with cycle-by-cycle PWM control.

At heavy loads, the minimum input voltage must increase to ensure a monotonic startup. Equation 1 calculates the minimum input voltage for this condition.

$$V_{OUT(max)} = D_{(max)} \times (V_{IN(min)} - I_{OUT(max)} \times R_{DS(on)} + V_d) - V_d + I_{OUT(max)} \times R_{dc} \quad (1)$$

where

- $D_{(max)} \geq 0.9$
- V_d = forward drop of the catch diode
- VBOOT = $(1.41 \times V_{IN} - 0.554 - V_d \times f_{SW} - 1.847 \times 10^3 \times IB2SW) / (1.41 + f_{SW})$
- $R_{DS(on)} = 1 / (-0.3 \times VB2SW^2 + 3.577 \times VB2SW - 4.246)$
- IB2SW = 100 µA
- VB2SW = VBOOT + V_d

DETAILED DESCRIPTION (continued)

Error Amplifier

A transconductance error amplifier controls the TPS54341 device voltage-regulation loop. The error amplifier compares the FB pin voltage to the lower of the internal soft-start voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 350 µA/V during normal operation. During soft-start operation, the transconductance is reduced to 78 µA/V and the error amplifier is referenced to the internal soft-start voltage.

The frequency compensation components (capacitor, series resistor, and capacitor) are connected between the error amplifier output COMP pin and GND pin.

Adjusting the Output Voltage

The internal voltage reference produces a precise 0.8-V ±1% voltage reference over the operating temperature and voltage range by scaling the output of a bandgap-reference circuit. The output voltage is set by a resistor divider from the output node to the FB pin. Using 1% tolerance or better divider resistors is recommended. Select the low-side resistor R_{LS} for the desired divider current and use Equation 2 to calculate R_{HS}. To improve efficiency at light loads consider using larger value resistors. However, if the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current may become noticeable.

$$R_{HS} = R_{LS} \times \left(\frac{Vout - 0.8V}{0.8\ V} \right) \quad (2)$$

Enable and Adjusting Undervoltage Lockout

The TPS54341 device enables when the VIN pin voltage rises above 4.3 V and the EN pin voltage exceeds the enable threshold of 1.2 V. The TPS54341 device disables when the VIN pin voltage falls below 4 V or when the EN pin voltage is below 1.2 V. The EN pin has an internal pullup-current source, I_1, of 1.2 µA that enables operation of the TPS54341 device when the EN pin floats.

If an application requires a higher undervoltage-lockout (UVLO) threshold, use the circuit shown in Figure 26 to adjust the input-voltage UVLO with two external resistors. When the EN pin voltage exceeds 1.2 V, an additional 3.4 µA of hysteresis current, I_{HYS}, is sourced out of the EN pin. When the EN pin pulls below 1.2 V, the 3.4-µA I_{HYS} current is removed. This additional current facilitates adjustable input-voltage UVLO hysteresis. Use Equation 3 to calculate R_{UVLO1} for the desired UVLO hysteresis voltage. Use Equation 4 to calculate R_{UVLO2} for the desired VIN start voltage.

In applications designed to start at relatively low input voltages (that is, from 4.5 o 9 V) and withstand high input voltages (for example, 40 V), the EN pin can experience a voltage greater than the absolute maximum voltage of 8.4 V during the high-input voltage condition. To avoid exceeding this voltage when using the EN resistors, the EN pin is clamped internally with a 5.8-V Zener diode capable of sinking up to 150 µA.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (3)$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} \quad (4)$$

DETAILED DESCRIPTION (continued)

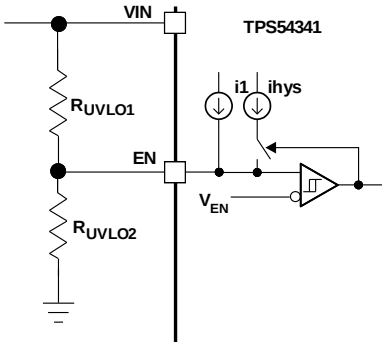


Figure 26. Adjustable UVLO

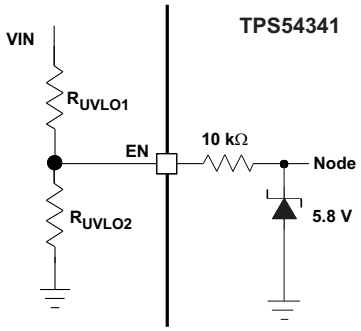


Figure 27. Internal EN Pin Clamp

Soft-Start/Tracking Pin (SS/TR)

The TPS54341 device effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage of the power-supply and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a soft-start time. The TPS54341 device has an internal pullup-current source of 1.7 µA that charges the external soft-start capacitor. The calculations for the soft-start time (10% to 90%) are shown in Equation 5. The voltage reference (V_{REF}) is 0.8 V and the soft-start current (I_{SS}) is 1.7 µA. The soft-start capacitor should remain lower than 0.47 µF and greater than 0.47 nF.

$$C_{SS}\ (nF) = \frac{T_{SS}\ (ms) \times I_{SS}\ (\mu A)}{V_{REF}\ (V) \times 0.8} \quad (5)$$

At power up, the TPS54341 device does not start switching until the soft-start pin discharges to less than 54 mV to ensure a proper power-up, see Figure 28.

Also, during normal operation, the TPS54341 device stops switching and the SS/TR must discharge to 54 mV, when the VIN UVLO is exceeded, the EN pin pulls below 1.2 V, otherwise a thermal shutdown event occurs.

The FB voltage follows the SS/TR pin voltage with a 42-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% on the internal reference voltage the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference (see Figure 23). The SS/TR voltage ramps linearly until clamped at 2.7 V typically as shown in Figure 28.

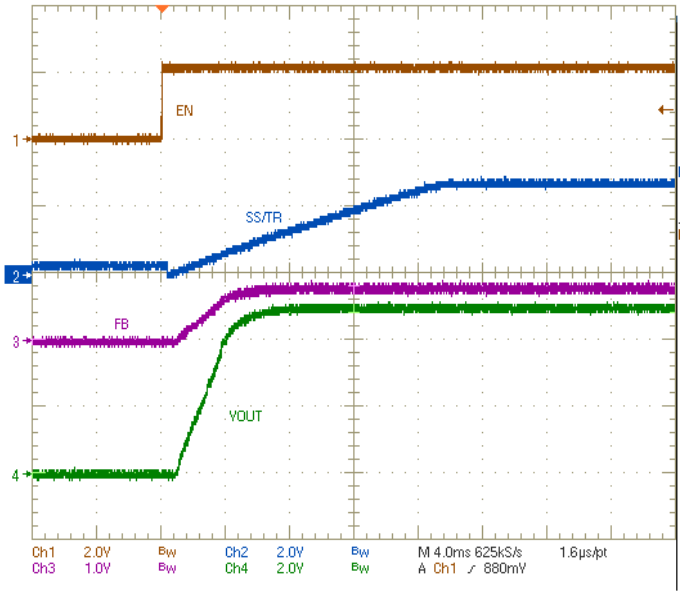


Figure 28. Operation of SS/TR Pin When Starting

DETAILED DESCRIPTION (continued)

Sequencing

Many of the common power-supply sequencing methods are implemented using the SS/TR, EN, and PWRGD pins. The sequential method is implemented using an open-drain output of a power-on reset pin of another device. The sequential method is illustrated in Figure 29 using two TPS54341 devices. The power good is connected to the EN pin on the TPS54341 device which enables the second power supply once the primary supply reaches regulation. If needed, a 1-nF ceramic capacitor on the EN pin of the second power supply provides a 1-ms startup delay. Figure 30 shows the results of Figure 29.

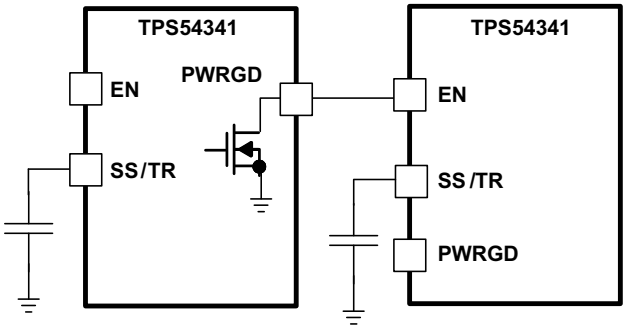


Figure 29. Schematic for Sequential Startup Sequence

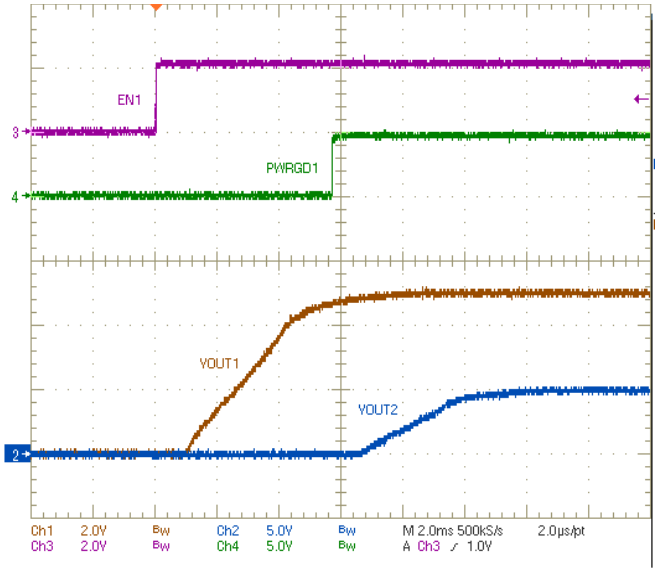


Figure 30. Sequential Startup Using EN and PWRGD

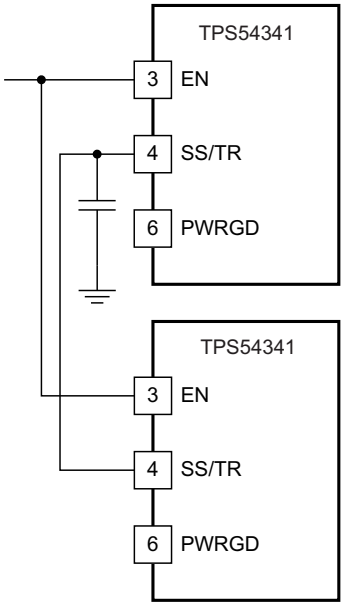


Figure 31. Schematic for Ratiometric Startup Sequence

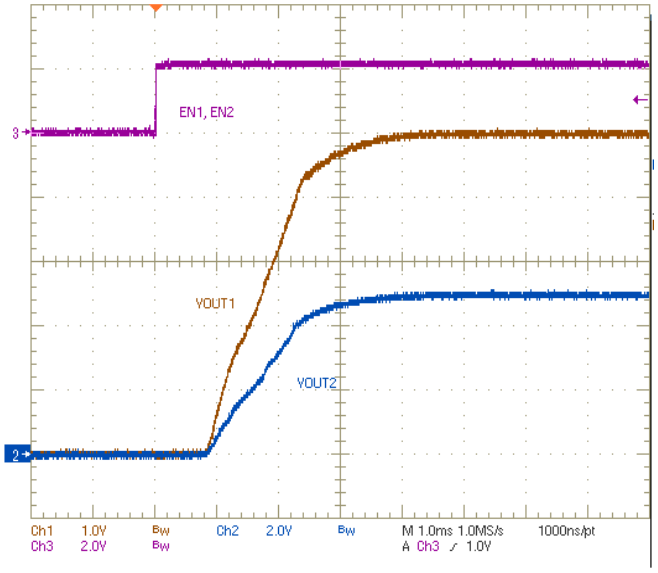


Figure 32. Ratiometric Startup Using Coupled SS/TR pins

Figure 31 shows a method for ratiometric start-up sequence by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start time the pullup current source must be doubled in Equation 5. Figure 32 shows the results of Figure 31.

DETAILED DESCRIPTION (continued)

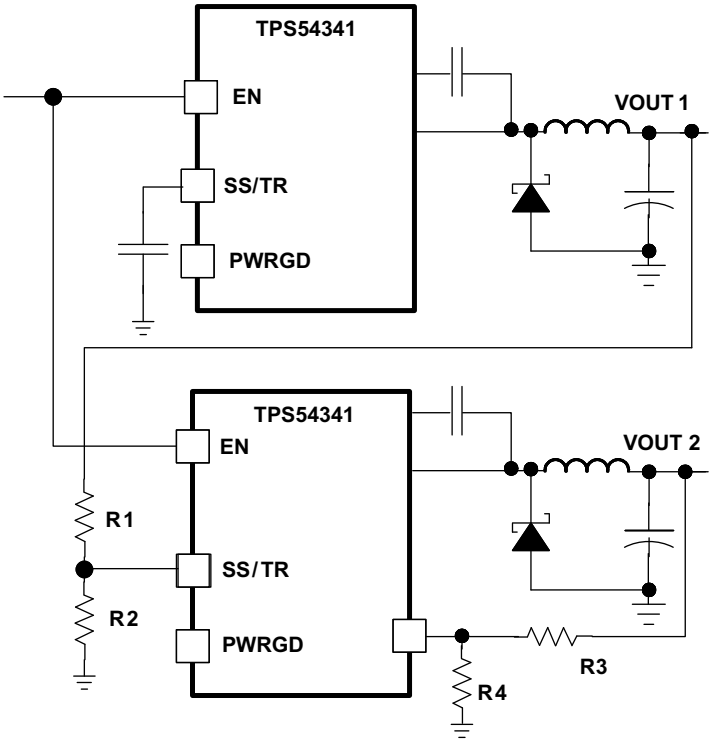


Figure 33. Schematic for Ratiometric and Simultaneous Startup Sequence

Ratiometric and simultaneous power-supply sequencing is implemented by connecting the resistor network of R1 and R2 shown in Figure 33 to the output of the power supply that must be tracked or another voltage reference source. Using Equation 6 and Equation 7, calculate the tracking resistors to initiate the V_{OUT2} slightly before, after, or at the same time as V_{OUT1}. Equation 8 is the voltage difference between V_{OUT1} and V_{OUT2} at the 95% of nominal output regulation.

The ΔV variable is 0 V for simultaneous sequencing. To minimize the effect of the inherent SS/TR to FB offset ($V_{SSoffset}$) in the soft-start circuit and the offset created by the pullup-current source (I_{SS}) and tracking resistors, the $V_{SSoffset}$ and I_{SS} are included as variables in the equations.

To design a ratiometric start-up in which the V_{OUT2} voltage is slightly greater than the V_{OUT1} voltage when V_{OUT2} reaches regulation, use a negative number in Equation 6 through Equation 8 for ΔV. Equation 8 results in a positive number for applications which the V_{OUT2} is slightly lower than V_{OUT1} when V_{OUT2} regulation is achieved.

Because the SS/TR pin must be pulled below 54 mV before starting after an EN, UVLO, or thermal shutdown fault, careful selection of the tracking resistors is required to ensure the device restarts after a fault. The calculated R1 value from Equation 6 must be greater than the value calculated in Equation 9 to ensure the device recovers from a fault.

As the SS/TR voltage becomes more than 85% of the nominal reference voltage, the $V_{SSoffset}$ becomes larger as the soft-start circuits gradually hands-off the regulation reference to the internal voltage reference. The SS/TR pin voltage must be greater than 1.5 V for a complete handoff to the internal voltage reference.

$$R1 = \frac{V_{OUT2} + \Delta V}{V_{REF}} \times \frac{V_{SSoffset}}{I_{SS}} \quad (6)$$

$$R2 = \frac{V_{REF} \times R1}{V_{OUT2} + \Delta V - V_{REF}} \quad (7)$$

$$\Delta V = V_{OUT1} - V_{OUT2} \quad (8)$$

$$R1 > 2800 \times V_{OUT1} - 180 \times \Delta V \quad (9)$$

DETAILED DESCRIPTION (continued)

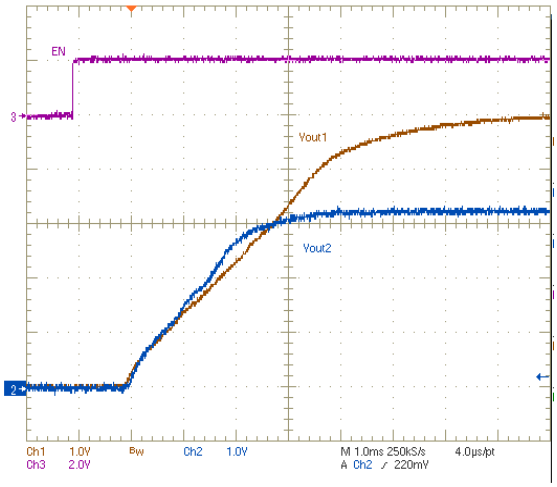


Figure 34. Ratiometric Startup With Tracking Resistors

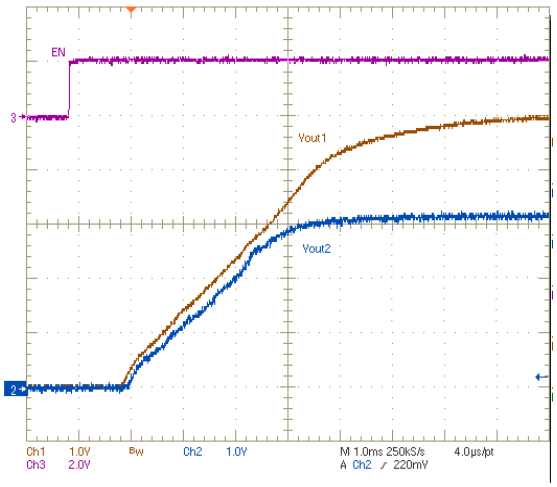


Figure 35. Ratiometric Startup With Tracking Resistors

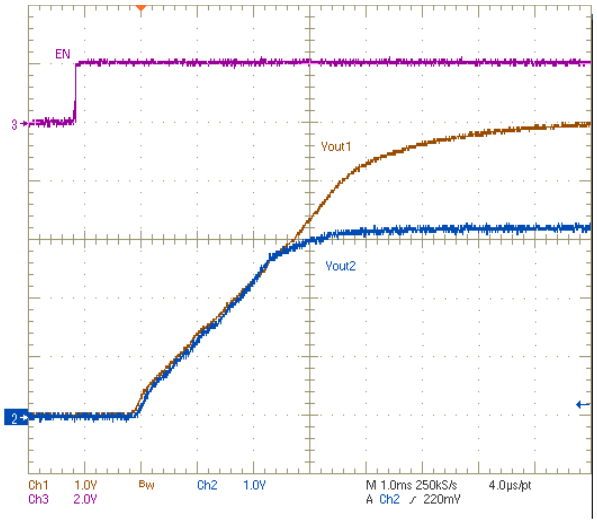


Figure 36. Simultaneous Startup With Tracking Resistor

Constant Switching Frequency and Timing Resistor (RT/CLK) Pin)

The switching frequency of the TPS54341 device is adjustable over a wide range from 100 to 2500 kHz by placing a resistor between the RT/CLK pin and GND pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 10 or Equation 11 or the curves in Figure 5 and Figure 6. To reduce the solution size, one typically sets the switching frequency as high as possible. Tradeoffs of the conversion efficiency, maximum input voltage, and minimum controllable on time must be considered. The minimum controllable on time is typically 135 ns which limits the maximum operating frequency in applications with high input-to-output step-down ratios. The maximum switching frequency is also limited by the frequency-foldback circuit. A more detailed discussion of the maximum switching frequency is provided in the next section.

$$\mathrm{RT}\ (\mathrm{k\Omega}) = \frac{92417}{f_{\mathrm{SW}}\ (\mathrm{kHz})^{0.991}} \tag{10}$$

$$f_{\mathrm{SW}}\ (\mathrm{kHz}) = \frac{101756}{\mathrm{RT}\ (\mathrm{k\Omega})^{1.008}} \tag{11}$$

DETAILED DESCRIPTION (continued)

Accurate Current Limit Operation and Maximum Switching Frequency

The TPS54341 device implements peak-current-mode control in which the COMP pin voltage controls the peak current of the high-side MOSFET. A signal proportional to the high-side switch current and the COMP pin voltage are compared each cycle. When the peak switch current intersects the COMP control voltage, the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier increases switch current by driving the COMP pin high. The error amplifier output clamps internally at a level which sets the peak switch current limit. The TPS54341 device provides an accurate current limit threshold with a typical current limit delay of 60 ns. With smaller inductor values, the delay results in a higher peak inductor current. The relationship between the inductor value and the peak inductor current is shown in Figure 37.

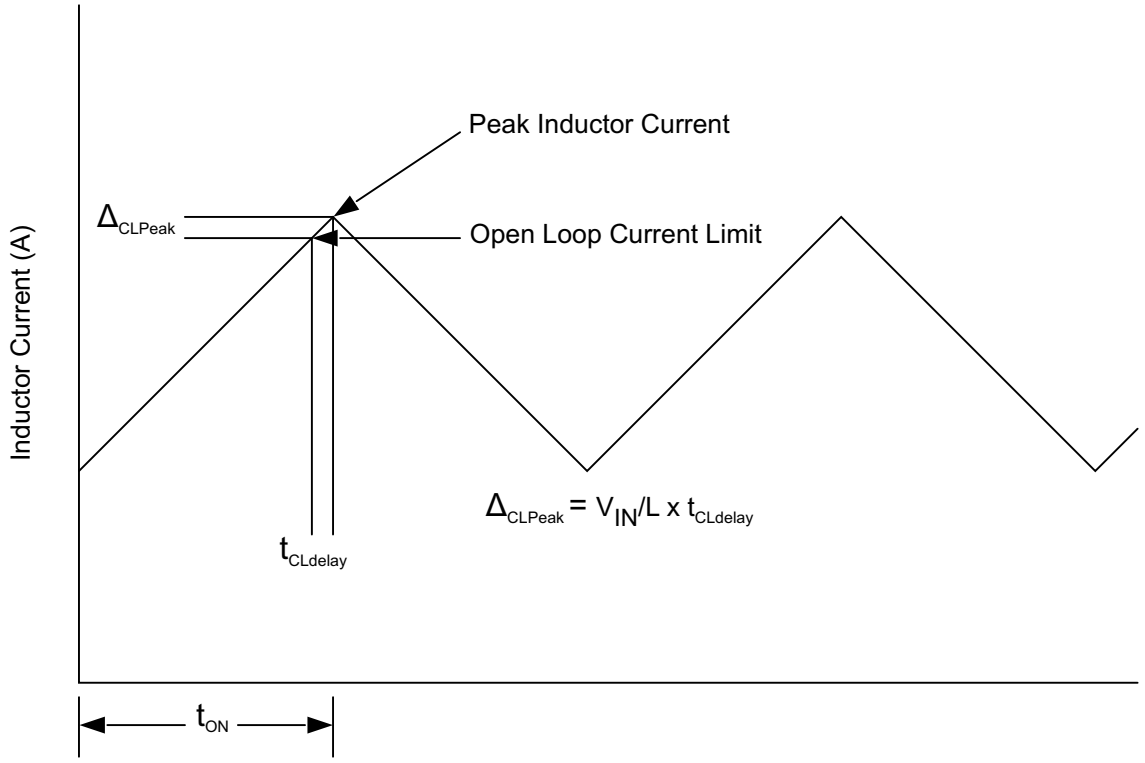


Figure 37. Current Limit Delay

To protect the converter in overload conditions at higher switching frequencies and input voltages, the TPS54341 device implements a frequency foldback. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V. The TPS54341 device uses a digital frequency foldback to enable synchronization to an external clock during normal startup and fault conditions. During short-circuit events, the inductor current can exceed the peak current-limit because of the high input voltage and the minimum controllable on time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off time. The frequency foldback effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency-foldback ratio of 8, there is a maximum frequency at which frequency-foldback protection controls the inductor current. Equation 13 calculates the maximum switching frequency at which the inductor current remains under control when V_{OUT} is forced to $V_{OUT(SC)}$. The selected operating frequency should not exceed the calculated value.

Equation 12 calculates the maximum switching-frequency limitation set by the minimum controllable on time and the input-to-output step-down ratio. Setting the switching frequency above this value causes the regulator to skip switching pulses to achieve the low duty cycle required to regulate the output voltage at maximum input voltage.

DETAILED DESCRIPTION (continued)

$$f_{SW(max\,skip)} = \frac{1}{t_{ON}} \times \left(\frac{I_O \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_O \times R_{DS(on)} + V_d} \right) \quad (12)$$

$$f_{SW(shift)} = \frac{f_{DIV}}{t_{ON}} \times \left(\frac{I_{CL} \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_{CL} \times R_{DS(on)} + V_d} \right) \quad (13)$$

where (for Equation 12 and Equation 13)

- I_O = output current
- I_{CL} = current limit
- R_{dc} = inductor resistance
- V_{IN} = maximum input voltage
- V_{OUT} = output voltage
- $V_{OUT(SC)}$ = output voltage during short
- V_d = diode voltage drop
- $R_{DS(on)}$ = switch on resistance
- t_{ON} = controllable on time
- f_{DIV}, frequency divide equals (1, 2, 4, or 8)

Synchronization to RT/CLK Pin

The RT/CLK pin can receive a frequency synchronization signal from an external system clock. To implement this synchronization feature connect a square wave to the RT/CLK pin through either circuit network shown in Figure 38. The square wave applied to the RT/CLK pin must switch lower than 0.5 V and higher than 2 V, and must have a pulsewidth greater than 15 ns. The synchronization frequency range is 160 to 2300 kHz. The rising edge of the SW synchronizes to the falling edge of RT/CLK pin signal. Design the external synchronization circuit such that the default-frequency set resistor connects from the RT/CLK pin to ground when the synchronization signal is off. When using a low-impedance signal source, the frequency-set resistor connects in parallel with an AC-coupling capacitor to a termination resistor (for example, 50 Ω) as shown in Figure 38. The two resistors in the series provide the default frequency-setting resistance when the signal source is turned off. The sum of the resistance sets the switching frequency close to the external CLK frequency. AC-coupling the synchronization signal the synchronization signal through a 10-pF ceramic capacitor to RT/CLK pin is recommended.

The first time the RT/CLK pulls above the PLL threshold the TPS54341 device switches from the RT-resistor free-running frequency mode to the PLL-synchronized mode. The internal 0.5-V voltage source is removed and the RT/CLK pin becomes high impedance as the PLL begins to lock onto the external signal. The switching frequency can be higher or lower than the frequency set with the RT/CLK resistor. The device transitions from the resistor mode to the PLL mode and locks onto the external clock frequency within 78 µs. During the transition from the PLL mode to the resistor-programmed mode, the switching frequency falls to 150 kHz and then increases or decreases to the resistor-programmed frequency when the 0.5-V bias voltage is reapplied to the RT/CLK resistor.

DETAILED DESCRIPTION (continued)

The switching frequency is divided by 8, 4, 2, and 1 as the FB pin voltage ramps from 0 to 0.8 V. The device implements a digital frequency foldback which enables synchronization to an external clock during normal startup and fault conditions. Figure 39, Figure 40 and Figure 41 show the device synchronized to an external system clock in continuous conduction mode (CCM), discontinuous conduction (DCM), and pulse skip mode (Eco-Mode).

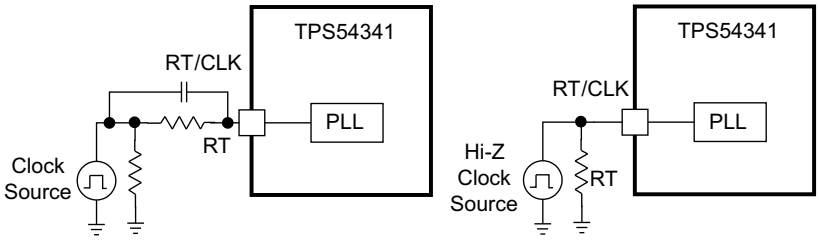


Figure 38. Synchronizing to a System Clock

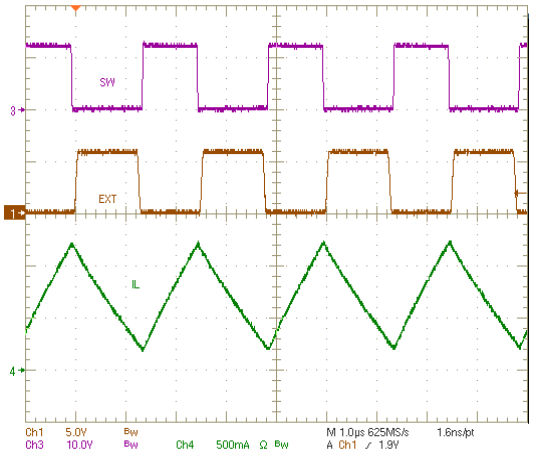


Figure 39. Plot of Synchronizing in CCM

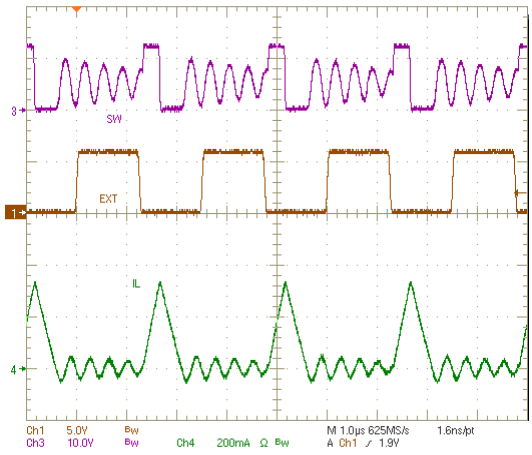


Figure 40. Plot of Synchronizing in DCM

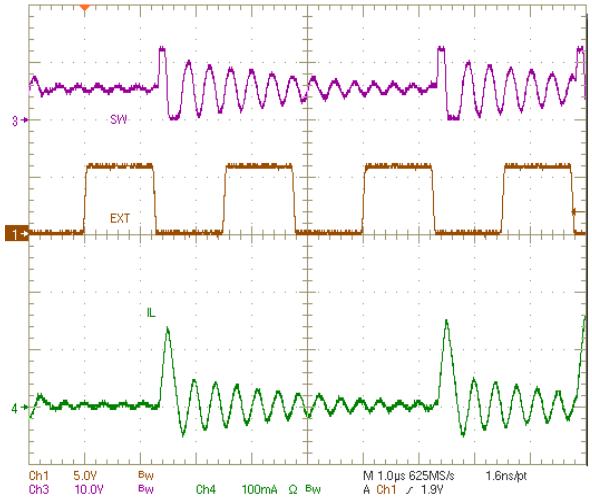


Figure 41. Plot of Synchronizing in Eco-mode

DETAILED DESCRIPTION (continued)

Power Good (PWRGD Pin)

The PWRGD pin is an open-drain output. Once the FB pin is between 93% and 106% of the internal voltage reference the PWRGD pin is de-asserted and the pin floats. A pull-up resistor of 1 kΩ to a voltage source that is 5.5 V or less is recommended. A higher pull-up resistance reduces the amount of current drawn from the pull up voltage source when the PWRGD pin is asserted low. A lower pullup resistance reduces the switching noise seen on the PWRGD signal. The PWRGD is in a defined state once the VIN input voltage is greater than 2 V but with reduced current sinking capability. The PWRGD will achieve full current sinking capability as VIN input voltage approaches 3 V.

The PWRGD pin is pulled low when the FB is lower than 90% or greater than 108% of the nominal internal reference voltage. Also, the PWRGD is pulled low, if the UVLO or thermal shutdown are asserted or the EN pin pulled low.

Overvoltage Protection

The TPS54341 device incorporates an output overvoltage-protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low-output capacitance. For example, when the power-supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier increases to a maximum voltage corresponding to the peak current-limit threshold. When the overload condition is removed, the regulator output rises and the error amplifier output transitions to the normal operating level. In some applications, the power-supply output voltage increases faster than the response of the error amplifier output resulting in an output overshoot.

The OVP feature minimizes output overshoot when using a low-value output capacitor by comparing the FB pin voltage to the rising OVP threshold which is nominally 108% of the internal voltage reference. If the FB pin voltage is greater than the rising OVP threshold, the high-side MOSFET disables immediately to minimize output overshoot. When the FB voltage drops below the falling OVP threshold which is nominally 106% of the internal voltage reference, the high-side MOSFET resumes normal operation.

Thermal Shutdown

The TPS54341 device provides an internal thermal shutdown to protect the device when the junction temperature exceeds 176°C. The high-side MOSFET stops switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature falls below 164°C, the device reinitiates the power-up sequence controlled by discharging the SS/TR pin.

Small-Signal Model for Loop Response

Figure 42 shows a simplified equivalent model for the TPS54341 control loop which is simulated to check the frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm_{EA} of 350 µA/V. The error amplifier is modeled using an ideal voltage-controlled current source. The resistor R_O and capacitor C_o model the open-loop gain and frequency response of the amplifier. The 1-mV AC-voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting c/a provides the small signal response of the frequency compensation. Plotting a/b provides the small signal response of the overall loop. The dynamic loop response is evaluated by replacing R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis. This equivalent model is only valid for CCM operation.

DETAILED DESCRIPTION (continued)

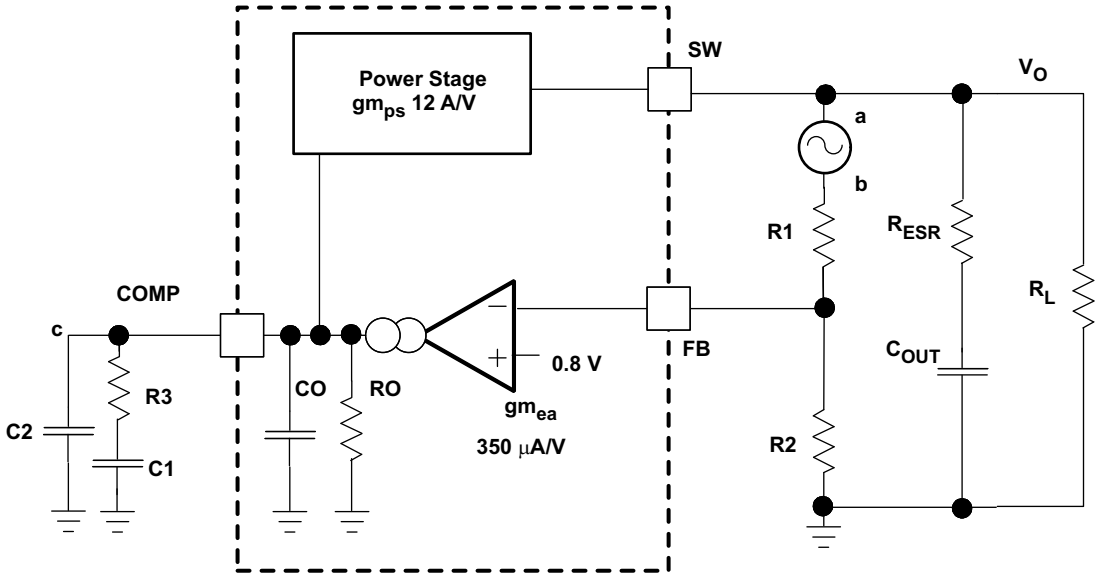


Figure 42. Small-Signal Model for Loop Response

Simple Small-Signal Model for Peak-Current-Mode Control

Figure 43 describes a simple small-signal model used to design the frequency compensation. The TPS54341 power stage is approximated by a voltage-controlled current source (duty-cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 14 and consists of a DC gain, one dominant pole, and one equivalent-series-resistor (ESR) zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 42) is the power stage transconductance, gm_{PS}. The gm_{PS} for the TPS54341 device is 16 A/V. The low-frequency gain of the power stage is the product of the transconductance and the load resistance as shown in Equation 15.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load seems problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 16). The combined effect is highlighted by the dashed line in the right half of Figure 43. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same with varying load conditions. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high-ESR aluminum-electrolytic capacitors can reduce the number frequency compensation components required to stabilize the overall loop because the phase margin increases by the ESR zero of the output capacitor (see FUNCTIONAL BLOCK DIAGRAM).

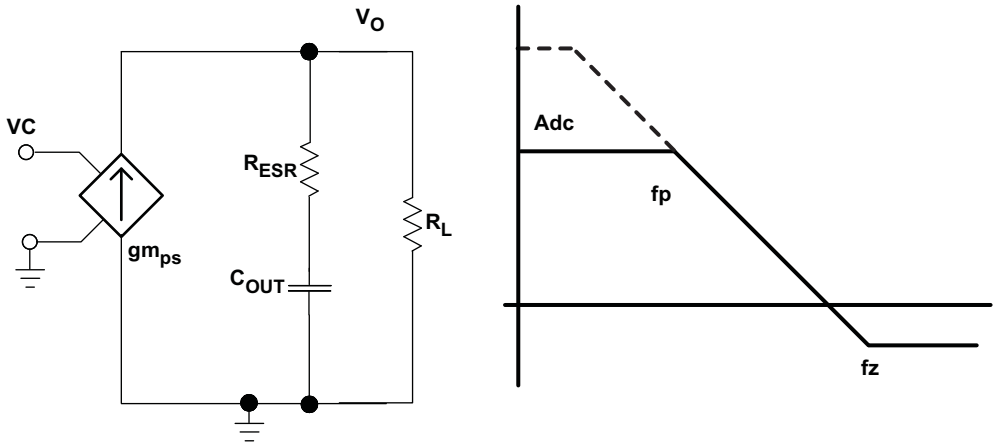


Figure 43. Simple Small-Signal Model and Frequency Response for Peak-Current-Mode Control

DETAILED DESCRIPTION (continued)

$$\frac{V_{OUT}}{VC} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (14)$$

$$Adc = gm_{ps} \times R_L \quad (15)$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (16)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (17)$$

Small Signal Model for Frequency Compensation

The TPS54341 device uses a transconductance amplifier for the error amplifier and supports three of the commonly-used frequency compensation circuits. Compensation circuits Type 2A, Type 2B, and Type 1 are shown in Figure 44. Type 2 circuits are typically implemented in high bandwidth power-supply designs using low-ESR output capacitors. The Type 1 circuit is used with power-supply designs with high-ESR aluminum-electrolytic or tantalum capacitors. Equation 18 and Equation 19 relate the frequency response of the amplifier to the small signal model in Figure 44. The open-loop gain and bandwidth are modeled using the R_O and C_O shown in Figure 44. See the APPLICATION INFORMATION section for a design example using a Type 2A network with a low-ESR output capacitor.

Equation 18 through Equation 27 are provided as a reference. An alternative is to use WEBENCH software tools to create a design based on the power-supply requirements (go to www.ti.com/WEBENCH for more information).

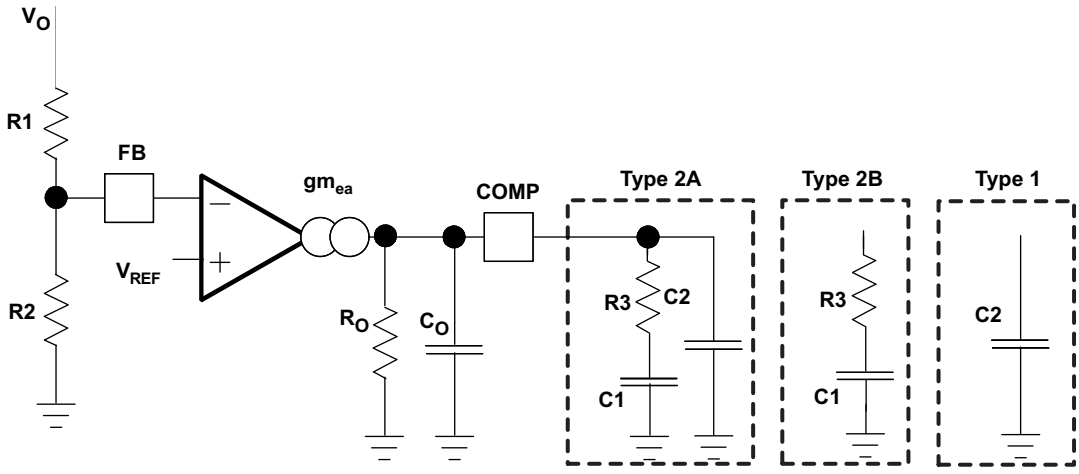


Figure 44. Types of Frequency Compensation

DETAILED DESCRIPTION (continued)

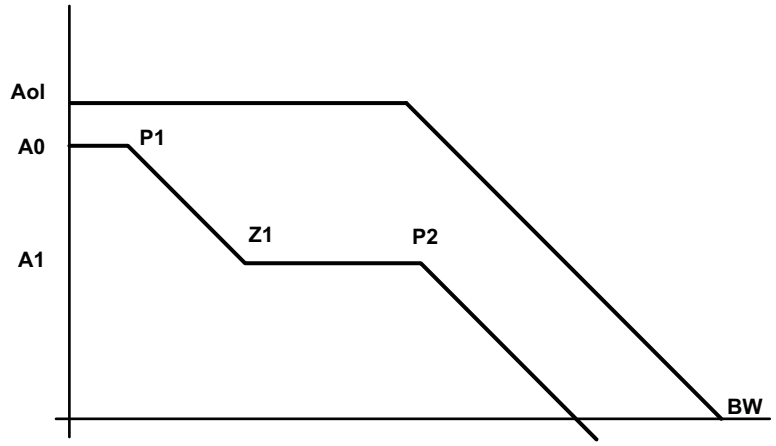


Figure 45. Frequency Response of the Type 2A and Type 2B Frequency Compensation

$$R_O = \frac{AoI(V/V)}{gm_{ea}} \quad (18)$$

$$C_O = \frac{gm_{ea}}{2\pi \times BW\ (Hz)} \quad (19)$$

$$EA = A0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \quad (20)$$

$$A0 = gm_{ea} \times R_O \times \frac{R2}{R1 + R2} \quad (21)$$

$$A1 = gm_{ea} \times R_O \| R3 \times \frac{R2}{R1 + R2} \quad (22)$$

$$P1 = \frac{1}{2\pi \times Ro \times C1} \quad (23)$$

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \quad (24)$$

$$P2 = \frac{1}{2\pi \times R3 \| R_O \times (C2 + C_O)} \text{ Type 2A} \quad (25)$$

$$P2 = \frac{1}{2\pi \times R3 \| R_O \times C_O} \text{ Type 2B} \quad (26)$$

$$P2 = \frac{1}{2\pi \times R_O \times (C2 + C_O)} \text{ Type 1} \quad (27)$$

APPLICATION INFORMATION

Design Guide — Step-By-Step Design Procedure

This guide illustrates the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These requirements are typically determined at the system level. The necessary calculations can be done using WEBENCH or the excel spreadsheet (SLVC452) located on the product. This design starts from the following known parameters.

Output Voltage	3.3 V
Transient Response 0.875 A to 2.625 A load step	ΔV_{OUT} = 4 %
Maximum Output Current	3.5 A
Input Voltage	12 V nominal 6 V to 42 V
Output Voltage Ripple	0.5% of V_{OUT}
Start Input Voltage (rising VIN)	5.75 V
Stop Input Voltage (falling VIN)	4.5 V

Selecting the Switching Frequency

The first step is to choose a switching frequency for the regulator. Typically, the designer uses the highest switching frequency possible because this produces the smallest solution size. High switching frequency allows for lower value inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage, the output voltage and the frequency-foldback protection.

Equation 12 and Equation 13 must be used to calculate the upper limit of the switching frequency for the regulator. Choose the lower value result from the two equations. Switching frequencies higher than these values results in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on time, t_{onmin}, is 135 ns for the TPS54341 device. For this example, the output voltage is 3.3 V and the maximum input voltage is 42 V, which allows for a maximum switch frequency up to 712 kHz to avoid pulse skipping from Equation 12. To ensure overcurrent runaway is not a concern during short circuits use Equation 13 to determine the maximum switching frequency for frequency foldback protection. With a maximum input voltage of 42 V, assuming a diode voltage of 0.7 V, inductor resistance of 21 mΩ, switch resistance of 87 mΩ, a current-limit value of 4.7 A and short circuit output voltage of 0.1 V, the maximum switching frequency is 1260 kHz.

For this design, a lower switching frequency of 600 kHz is chosen to operate comfortably below the calculated maximums. To determine the timing resistance for a given switching frequency, use Equation 10 or the curve in Figure 6. The switching frequency is set by resistor R_3 shown in Figure 46. For 600 kHz operation, the closest standard value resistor is 162 kΩ.

$$f_{SW(maxskip)} = \frac{1}{135ns} \times \left(\frac{3.5\ A \times 21\ m\Omega + 3.3\ V + 0.7\ V}{42\ V - 3.5\ A \times 87\ m\Omega + 0.7\ V} \right) = 712\ kHz \quad (28)$$

$$f_{SW(shift)} = \frac{8}{135\ ns} \times \left(\frac{4.7\ A \times 21\ m\Omega + 0.1\ V + 0.7\ V}{42\ V - 4.7\ A \times 87\ m\Omega + 0.7\ V} \right) = 1260\ kHz \quad (29)$$

$$RT\ (k\Omega) = \frac{92417}{600\ (kHz)^{0.991}} = 163\ k\Omega \quad (30)$$

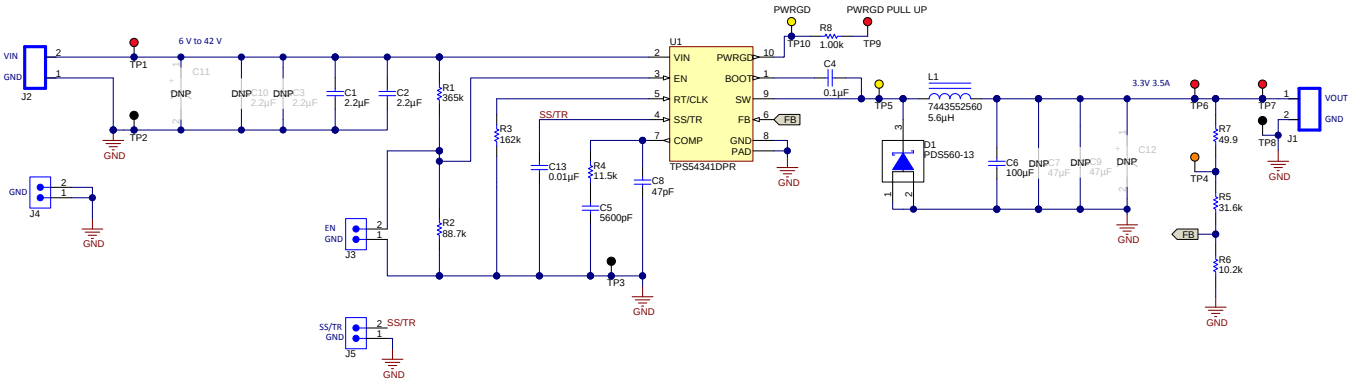


Figure 46. 3.3-V Output TPS54341 Design Example

Output Inductor Selection (L_O)

To calculate the minimum value of the output inductor, use Equation 31.

K_{IND} is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer, however, the following guidelines may be used.

For designs using low ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 may be desirable. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results. Because the inductor ripple current is part of the current mode PWM control system, the inductor ripple current should always be greater than 150 mA for stable PWM operation. In a wide input voltage regulator, it is best to choose relatively large inductor ripple current. This provides sufficienct ripple current with the input voltage at the minimum.

For this design example, K_{IND} = 0.3 and the minimum inductor value is calculated to be 4.8 µH. The nearest standard value is 5.6 µH. It is important that the RMS current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found from Equation 33 and Equation 34. For this design, the RMS inductor current is 3.5 A and the peak inductor current is 3.95 A. The chosen inductor is a WE 7443552560, which has a saturation current rating of 7.5 A and an RMS current rating of 6.7 A.

As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. Selecting higher ripple currents will increase the output voltage ripple of the regulator but allow for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative design approach is to choose an inductor with a saturation current rating equal to or greater than the switch current limit of the TPS54341 device which is nominally 5.5 A.

$$L_{O(min)} = \frac{V_{IN(max)} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} = \frac{42\ V - 3.3\ V}{3.5\ A \times 0.3} \times \frac{3.3\ V}{42\ V \times 600\ kHz} = 4.8\ \mu H \quad (31)$$

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_O \times f_{SW}} = \frac{3.3\ V \times (42\ V - 3.3\ V)}{42\ V \times 5.6\ \mu H \times 600\ kHz} = 0.905\ A \quad (32)$$

$$I_{L(rms)} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_O \times f_{SW}} \right)^2} = \sqrt{(3.5\ A)^2 + \frac{1}{12} \times \left(\frac{3.3\ V \times (42\ V - 3.3\ V)}{42\ V \times 5.6\ \mu H \times 600\ kHz} \right)^2} = 3.5\ A \quad (33)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 3.5\ A + \frac{0.905\ A}{2} = 3.95\ A \quad (34)$$

Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the increased load current until the regulator responds to the load step. The regulator does not respond immediately to a large, fast increase in the load current such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to sense the change in output voltage and adjust the peak switch current in response to the higher load. The output capacitance must be large enough to supply the difference in current for two clock cycles to maintain the output voltage within the specified range. Equation 35 shows the minimum output capacitance necessary, where ΔI_{OUT} is the change in output current, $f$sw is the regulators switching frequency and ΔV_{OUT} is the allowable change in the output voltage. For this example, the transient load response is specified as a 4% change in V_{OUT} for a load step from 0.875 A to 2.625 A. Therefore, ΔI_{OUT} is 2.625 A – 0.875 A = 1.75 A and ΔV_{OUT} = 0.04 × 3.3 = 0.13 V. Using these numbers gives a minimum capacitance of 44.9 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be included in load step calculations.

The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high to low load current. The catch diode of the regulator can not sink current so energy stored in the inductor can produce an output voltage overshoot when the load current rapidly decreases. A typical load step response is shown in Figure 47. The excess energy absorbed in the output capacitor will increase the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 36 calculates the minimum capacitance required to keep the output voltage overshoot to a desired value, where L_O is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_f is the peak output voltage, and V_I is the initial voltage. For this example, the worst case load step will be from 2.625 A to 0.875 A. The output voltage increases during this load transition and the stated maximum in our specification is 4 % of the output voltage. This makes V_f = 1.04 × 3.3 = 3.432. V_I is the initial capacitor voltage which is the nominal output voltage of 3.3 V. Using these numbers in Equation 36 yields a minimum capacitance of 38.6 µF.

Equation 37 calculates the minimum output capacitance needed to meet the output voltage ripple specification, where $f$sw is the switching frequency, $V_{ORIPPLE}$ is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. Equation 37 yields 11.4 µF.

Equation 38 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 38 indicates the ESR should be less than 18 mΩ.

The most stringent criteria for the output capacitor is 44.9 µF required to maintain the output voltage within regulation tolerance during a load transient.

Capacitance de-ratings for aging, temperature and dc bias increases this minimum value. For this example, a 100-µF ceramic capacitor with 5 mΩ of ESR is used. The derated capacitance is 70 µF, well above the minimum required capacitance of 44.9 µF.

Capacitors are generally rated for a maximum ripple current that can be filtered without degrading capacitor reliability. Some capacitor data sheets specify the Root Mean Square (RMS) value of the maximum ripple current. Equation 39 can be used to calculate the RMS ripple current that the output capacitor must support. For this example, Equation 39 yields 261 mA.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} = \frac{2 \times 1.75\ A}{600\ kHz \times 0.13\ V} = 44.9\ \mu F \quad (35)$$

$$C_{OUT} > L_O \times \frac{\left((I_{OH})^2 - (I_{OL})^2\right)}{\left((V_f)^2 - (V_l)^2\right)} = 5.6\ \mu H \times \frac{\left(2.625\ A^2 - 0.875\ A^2\right)}{\left(3.432\ V^2 - 3.3\ V^2\right)} = 38.6\ \mu F \quad (36)$$

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{ORIPPLE}}{I_{RIPPLE}}\right)} = \frac{1}{8 \times 600\ kHz} \times \frac{1}{\left(\frac{16.5\ mV}{0.905\ A}\right)} = 11.4\ \mu F \quad (37)$$

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} = \frac{16.5\ mV}{0.905\ A} = 18\ m\Omega \quad (38)$$

$$I_{COUT(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L_O \times f_{SW}} = \frac{3.3\ V \times (42\ V - 3.3\ V)}{\sqrt{12} \times 42\ V \times 5.6\ \mu H \times 600\ kHz} = 261\ mA \quad (39)$$

Catch Diode

The TPS54341 device requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(max)}$. The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 42 V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the TPS54341 device.

For the example design, the PDS560 Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the PDS560 is 0.55 V at 3.5 A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the AC losses of the diode must be taken into account. The AC losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 40 is used to calculate the total power dissipation, including conduction losses and AC losses of the diode.

The PDS560 diode has a junction capacitance of 90 pF at 42 V input voltage. Using Equation 40, the total loss in the diode is 2.27 W.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{\left(V_{IN(max)} - V_{OUT}\right) \times I_{OUT} \times Vfd}{V_{IN(max)}} + \frac{C_j \times f_{SW} \times \left(V_{IN} + Vfd\right)^2}{2} =$$

$$\frac{(42\ V - 3.3\ V) \times 3.5\ A \times 0.55\ V}{42\ V} + \frac{90\ pF \times 600\ kHz \times (42\ V + 0.55\ V)^2}{2} = 2.27\ W \quad (40)$$

Input Capacitor

The TPS54341 device requires a high-quality ceramic-type X5R or X7R input-decoupling capacitor with at least 3 µF of effective capacitance. Some applications will benefit from additional bulk capacitance. The effective capacitance includes any loss of capacitance due to dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54341 device. The input ripple current can be calculated using Equation 41.

The value of a ceramic capacitor varies significantly with temperature and the dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is more stable over temperature. X5R and X7R ceramic dielectrics are usually selected for switching regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with consideration for the dc bias. The effective value of a capacitor decreases as the dc bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 42 V voltage rating is required to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V, or 100 V. For this example, two 2.2-µF 100-V capacitors in parallel are used. Table 1 shows several choices of high voltage capacitors.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 42. Using the design example values, I_{OUT} = 3.5 A, C_{IN} = 4.4 µF, f_{SW} = 600 kHz, yields an input voltage ripple of 331 mV and a rms input ripple current of 1.74 A.

$$I_{CI(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} = 3.5\ A \sqrt{\frac{3.3\ V}{6\ V} \times \frac{\left(6\ V - 3.3\ V\right)}{6\ V}} = 1.74\ A \tag{41}$$

$$\Delta V_{IN} = \frac{I_{OUT} \times 0.25}{C_{IN} \times f_{SW}} = \frac{3.5\ A \times 0.25}{4.4\ \mu F \times 600\ kHz} = 331\ mV \tag{42}$$

Table 1. Capacitor Types

VENDOR	VALUE (µF)	EIA Size	VOLTAGE (V)	DIALECTRIC	COMMENTS
Murata	1 to 2.2	1210	100	X7R	GRM32 series
	1 to 4.7		50		
	1	1206	100		GRM31 series
	1 to 2.2		50		
Vishay	1 to 1.8	2220	50		VJ X7R series
	1 to 1.2		100		
	1 to 3.9	2225	50		
	1 to 1.8		100		
TDK	1 to 2.2	1812	100		C series C4532
	1.5 to 6.8		50		
	1 to 2.2	1210	100		C series C3225
	1 to 3.3		50		
AVX	1 to 4.7	1210	50		X7R dielectric series
	1		100		
	1 to 4.7	1812	50		
	1 to 2.2		100		

Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time it will take for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54341 device reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The slow-start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Equation 43 can be used to find the minimum slow-start time, T_{SS}, necessary to charge the output capacitor, C_{OUT}, from 10% to 90% of the output voltage, V_{OUT}, with an average slow-start current of I_{SSavg}. In the example, to charge the effective output capacitance of 70 µF up to 3.3 V with an average current of 1 A requires a 0.2-ms slow-start time.

Once the slow-start time is known, the slow-start capacitor value can be calculated using Equation 5. For the example circuit, the slow-start time is not too critical because the output capacitor value is 100 µF which does not require much current to charge to 3.3 V. The example circuit has the slow-start time set to an arbitrary value of 3.5 ms which requires a 9.3-nF slow-start capacitor calculated by Equation 44. For this design, the next larger standard value of 10 nF is used.

$$T_{SS} > \frac{C_{OUT} \times V_{OUT} \times 0.8}{I_{SSavg}} \tag{43}$$

$$C_{SS}\ (nF) = \frac{T_{SS}\ (ms) \times I_{SS}\ (\mu A)}{V_{REF}\ (V) \times 0.8} = 3.5\ ms \times \frac{1.7\ \mu A}{(0.8\ V \times 0.8)} = 9.3\ nF \tag{44}$$

Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT and SW pins for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor must have a 10 V or higher voltage rating.

Undervoltage Lockout Set Point

The Undervoltage Lockout (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54341 device. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.75 V (UVLO start). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.5 V (UVLO stop).

Programmable UVLO threshold voltages are set using the resistor divider of R_{UVLO1} and R_{UVLO2} between VIN and ground connected to the EN pin. Equation 3 and Equation 4 calculate the resistance values necessary. For the example application, a 365 kΩ between Vin and EN (R_{UVLO1}) and a 88.7 kΩ between EN and ground (R_{UVLO2}) are required to produce the 8-V and 6.25-V start and stop voltages.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} = \frac{5.75\ V - 4.5\ V}{3.4\ \mu A} = 368\ k\Omega \tag{45}$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} = \frac{1.2\ V}{\frac{5.75\ V - 1.2\ V}{365\ k\Omega} + 1.2\ \mu A} = 87.8\ k\Omega \tag{46}$$

Output Voltage and Feedback Resistors Selection

The voltage divider of R5 and R6 sets the output voltage. For the example design, 10.2 kΩ was selected for R6. Using Equation 2, R5 is calculated as 31.9 kΩ. The nearest standard 1% resistor is 31.6 kΩ. Due to the input current of the FB pin, the current flowing through the feedback network should be greater than 1 µA to maintain the output voltage accuracy. This requirement is satisfied if the value of R6 is less than 800 kΩ. Choosing higher resistor values decreases quiescent current and improves efficiency at low output currents but may also introduce noise immunity problems.

$$R_{HS} = R_{LS} \times \frac{V_{OUT} - 0.8\ V}{0.8\ V} = 10.2\ k\Omega \times \left(\frac{3.3\ V - 0.8\ V}{0.8\ V}\right) = 31.9\ k\Omega \quad (47)$$

Compensation

There are several methods to design compensation for DC-DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Because the slope compensation is ignored, the actual crossover frequency will be lower than the crossover frequency used in the calculations. This method assumes the crossover frequency is between the modulator pole and the ESR zero and the ESR zero is at least ten-times greater the modulator pole.

To get started, the modulator pole, $f_{p(mod)}$, and the ESR zero, f_{z1} must be calculated using Equation 48 and Equation 49. For C_{OUT}, use a derated value of 70 µF. Use equations Equation 50 and Equation 51 to estimate a starting point for the crossover frequency, f_{co}. For the example design, $f_{p(mod)}$ is 2411 Hz and $f_{z(mod)}$ is 455 kHz. Equation 49 is the geometric mean of the modulator pole and the ESR zero and Equation 51 is the mean of modulator pole and the switching frequency. Equation 50 yields 33.1 kHz and Equation 51 gives 26.9 kHz. Use the lower value of Equation 50 or Equation 51 for an initial crossover frequency. For this example, the target $f$co is 26.9 kHz.

Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

$$f_{P(mod)} = \frac{I_{OUT(max)}}{2 \times \pi \times V_{OUT} \times C_{OUT}} = \frac{3.5\ A}{2 \times \pi \times 3.3\ V \times 70\ \mu F} = 2411\ Hz \quad (48)$$

$$f_{Z(mod)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} = \frac{1}{2 \times \pi \times 5\ m\Omega \times 70\ \mu F} = 455\ kHz \quad (49)$$

$$f_{co} = \sqrt{f_{p(mod)} \times f_{z(mod)}} = \sqrt{2411\ Hz \times 455\ kHz} = 33.1\ kHz \quad (50)$$

$$f_{co} = \sqrt{f_{p(mod)} \times \frac{f_{SW}}{2}} = \sqrt{2411\ Hz \times \frac{600\ kHz}{2}} = 26.9\ kHz \quad (51)$$

To determine the compensation resistor, R4, use Equation 52. Assume the power stage transconductance, gmps, is 12 A/V. The output voltage, V_O, reference voltage, V_{REF}, and amplifier transconductance, gmea, are 5 V, 0.8 V and 350 µA/V, respectively. R4 is calculated to be 11.6 kΩ and a standard value of 11.5 kΩ is selected. Use Equation 53 to set the compensation zero to the modulator pole frequency. Equation 53 yields 5740 pF for compensating capacitor C5. 5600 pF is used for this design.

$$R4 = \left(\frac{2 \times \pi \times f_{co} \times C_{OUT}}{gm_{ps}}\right) \times \left(\frac{V_{OUT}}{V_{REF} \times gm_{ea}}\right) = \left(\frac{2 \times \pi \times 26.9\ kHz \times 70\ \mu F}{12\ A/V}\right) \times \left(\frac{3.3\ V}{0.8\ V \times 350\ \mu A/V}\right) = 11.6\ k\Omega \quad (52)$$

$$C5 = \frac{1}{2 \times \pi \times R4 \times f_{p(mod)}} = \frac{1}{2 \times \pi \times 11.5\ k\Omega \times 2411\ Hz} = 5740\ pF \quad (53)$$

A compensation pole can be implemented if desired by adding capacitor C8 in parallel with the series combination of R4 and C5. Use the larger value calculated from Equation 54 and Equation 55 for C8 to set the compensation pole. The selected value of C8 is 47 pF for this design example.

$$C8 = \frac{C_{OUT} \text{ x } R_{ESR}}{R4} = \frac{70\ \mu F \text{ x } 5\ m\Omega}{11.5\ k\Omega} = 30.4\ pF \quad (54)$$

$$C8 = \frac{1}{R4 \times f_{sw} \times \pi} = \frac{1}{11.5\ k\Omega \times 600\ kHz \times \pi} = 46.1\ pF \quad (55)$$

Discontinuous Conduction Mode and Eco-mode Boundary

With an input voltage of 12 V, the power supply enters discontinuous conduction mode when the output current is less than 340 mA. The power supply enters Eco-mode when the output current is lower than 30 mA. The input current draw is 260 µA with no load.

APPLICATION CURVES

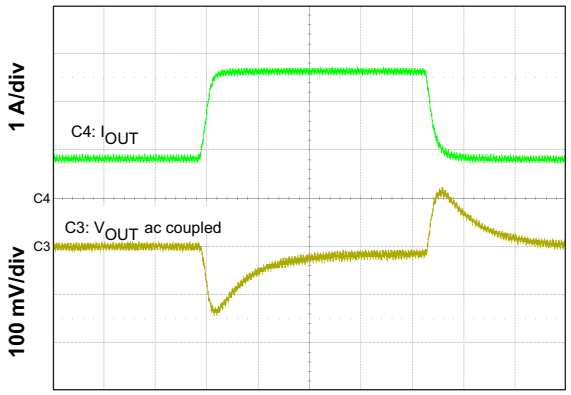


Figure 47. Load Transient

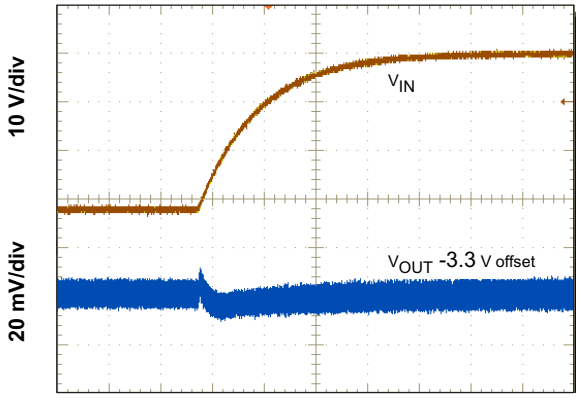


Figure 48. Line Transient (8 V to 40 V)

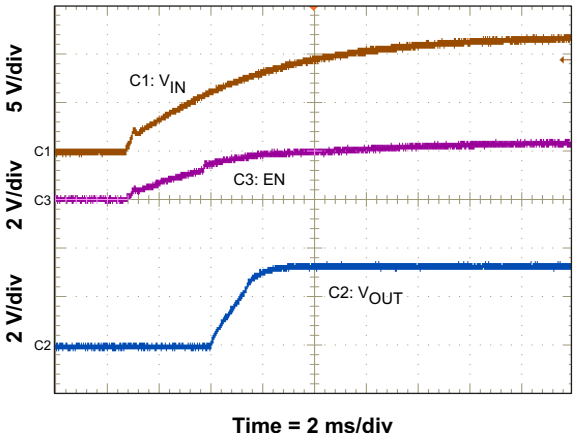


Figure 49. Startup With VIN

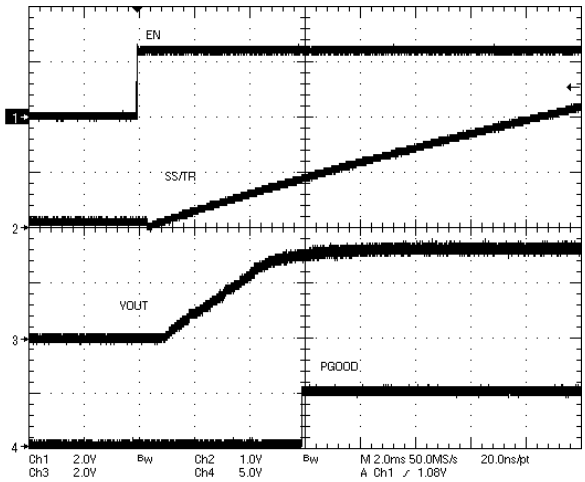


Figure 50. Startup With EN

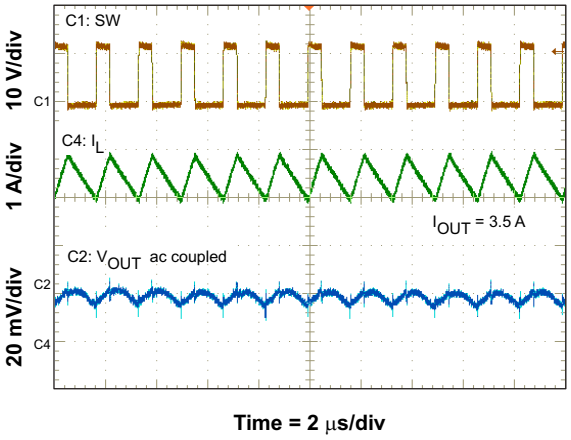


Figure 51. Output Ripple CCM

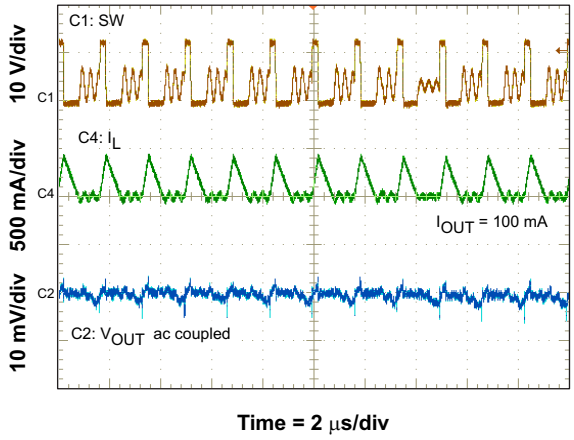


Figure 52. Output Ripple DCM

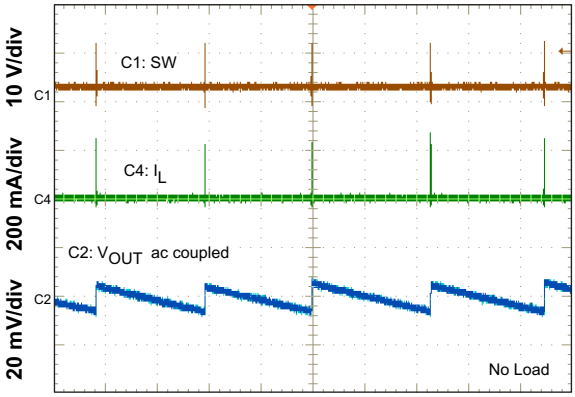


Figure 53. Output Ripple PSM

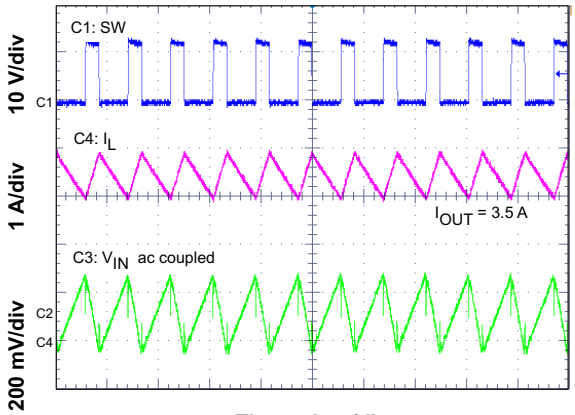


Figure 54. Input Ripple CCM

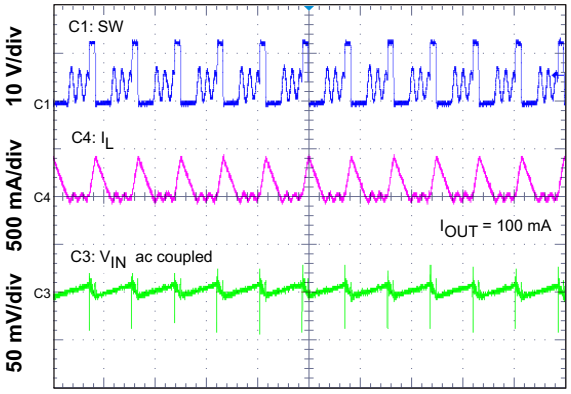


Figure 55. Input Ripple DCM

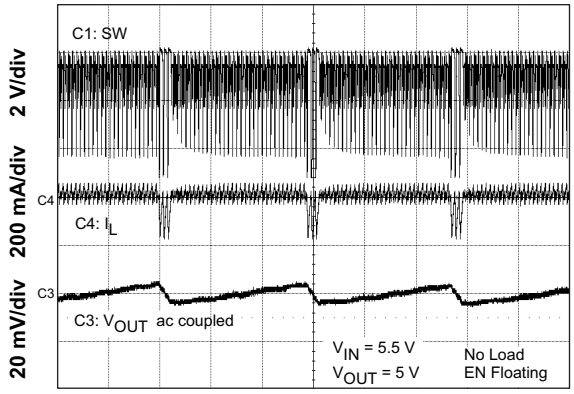


Figure 56. Low Dropout Operation

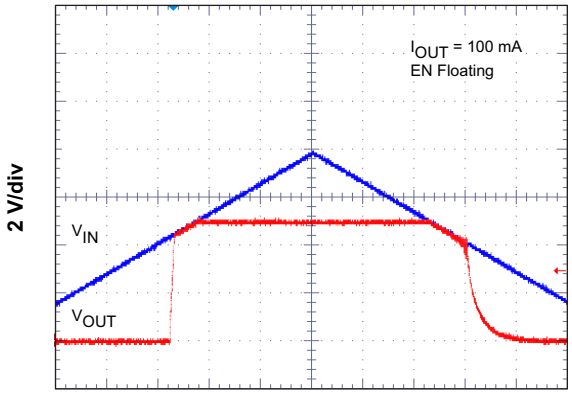


Figure 57. Low Dropout Operation

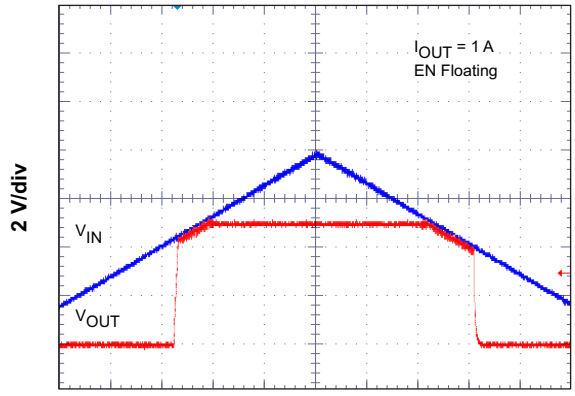


Figure 58. Low Dropout Operation

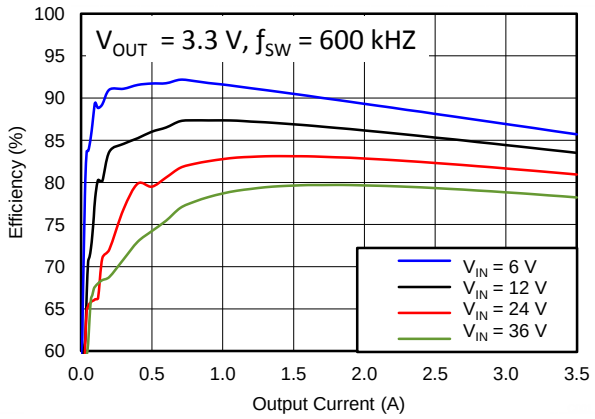


Figure 59. Efficiency Versus Load Current

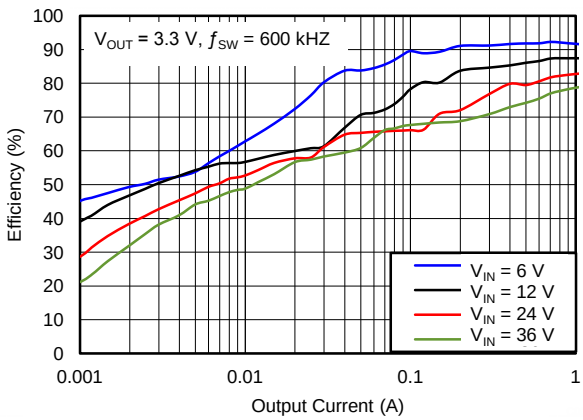


Figure 60. Light Load Efficiency

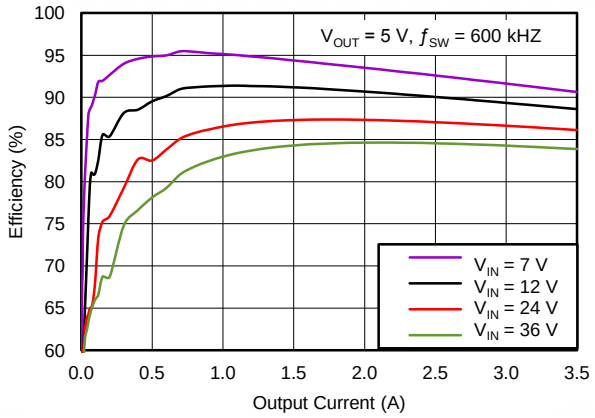


Figure 61. Efficiency Versus Load Current

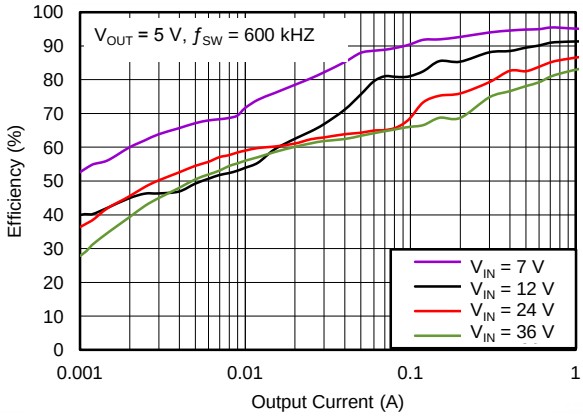


Figure 62. Light Load Efficiency

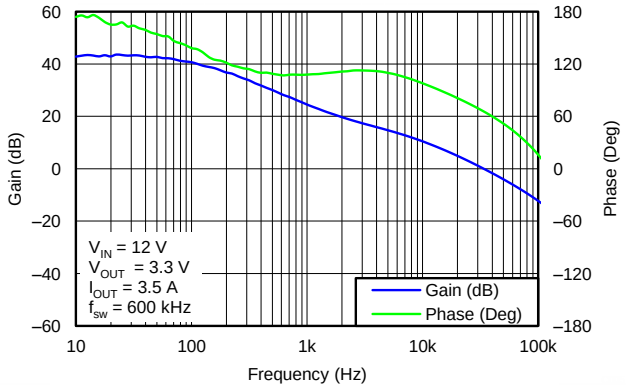


Figure 63. Overall Loop Frequency Response

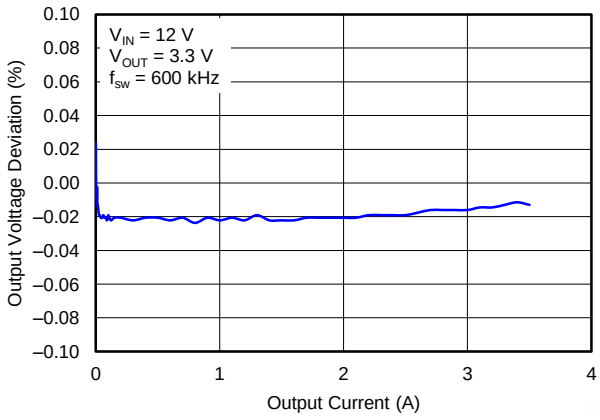


Figure 64. Regulation Versus Load Current

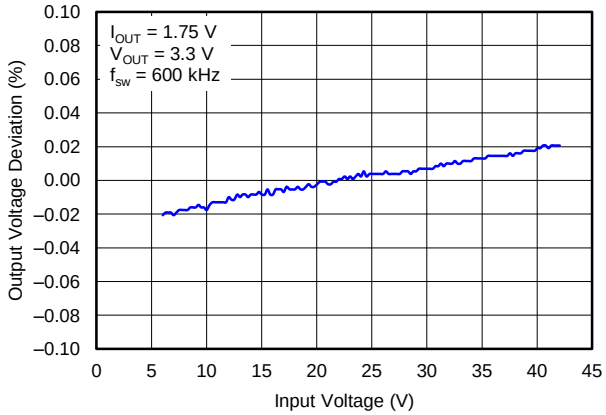


Figure 65. Regulation Versus Input Voltage

Power Dissipation Estimate

The following formulas show how to estimate the TPS54341 power dissipation under continuous conduction mode (CCM) operation. These equations should not be used if the device is operating in discontinuous conduction mode (DCM).

The power dissipation of the IC includes conduction loss (P_{COND}), switching loss (P_{SW}), gate drive loss (P_{GD}) and supply current (P_Q). Example calculations are shown with the 12 V typical input voltage of the design example.

$$P_{COND} = (I_{OUT})^2 \times R_{DS(on)} \times \left(\frac{V_{OUT}}{V_{IN}} \right) = 3.5\ A^2 \times 87\ m\Omega \times \frac{3.3\ V}{12\ V} = 0.31\ W \quad (56)$$

$$P_{SW} = V_{IN} \times f_{SW} \times I_{OUT} \times t_{rise} = 12\ V \times 600\ kHz \times 3.5\ A \times 4.9\ ns = 0.123\ W \quad (57)$$

$$P_{GD} = V_{IN} \times Q_G \times f_{SW} = 12\ V \times 3nC \times 600\ kHz = 0.022\ W \quad (58)$$

$$P_Q = V_{IN} \times I_Q = 12\ V \times 146\ \mu A = 0.0018\ W \quad (59)$$

Where:

- I_{OUT} is the output current (A).
- $R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω).
- V_{OUT} is the output voltage (V).
- V_{IN} is the input voltage (V).
- f_{SW} is the switching frequency (Hz).
- t_{rise} is the SW pin voltage rise time and can be estimated by trise = V_{IN} × 0.16 ns/V + 3 ns
- Q_G is the total gate charge of the internal MOSFET
- I_Q is the operating nonswitching supply current

Therefore,

$$P_{TOT} = P_{COND} + P_{SW} + P_{GD} + P_Q = 0.31\ W + 0.123\ W + 0.022\ W + 0.0018\ W = 0.457\ W \quad (60)$$

For given T_A,

$$T_J = T_A + R_{TH} \times P_{TOT} \quad (61)$$

For given $T_{J(MAX)}$ = 150°C

$$T_{A(max)} = T_{J(max)} - R_{TH} \times P_{TOT} \quad (62)$$

Where:

- P_{TOT} is the total device power dissipation (W).
- T_A is the ambient temperature (°C).
- T_J is the junction temperature (°C).
- R_{TH} is the thermal resistance (°C/W).
- $T_{J(MAX)}$ is maximum junction temperature (°C).
- $T_{A(MAX)}$ is maximum ambient temperature (°C).

There will be additional power losses in the regulator circuit due to the inductor ac and dc losses, the catch diode and PCB trace resistance impacting the overall efficiency of the regulator.

Layout

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade performance. To reduce parasitic effects, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. See Figure 66 for a PCB layout example. The GND pin should be tied directly to the power pad under the IC and the power pad.

The power pad should be connected to internal PCB ground planes using multiple vias directly under the IC. The SW pin should be routed to the cathode of the catch diode and to the output inductor. Because the SW connection is the switching node, the catch diode and output inductor should be located close to the SW pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

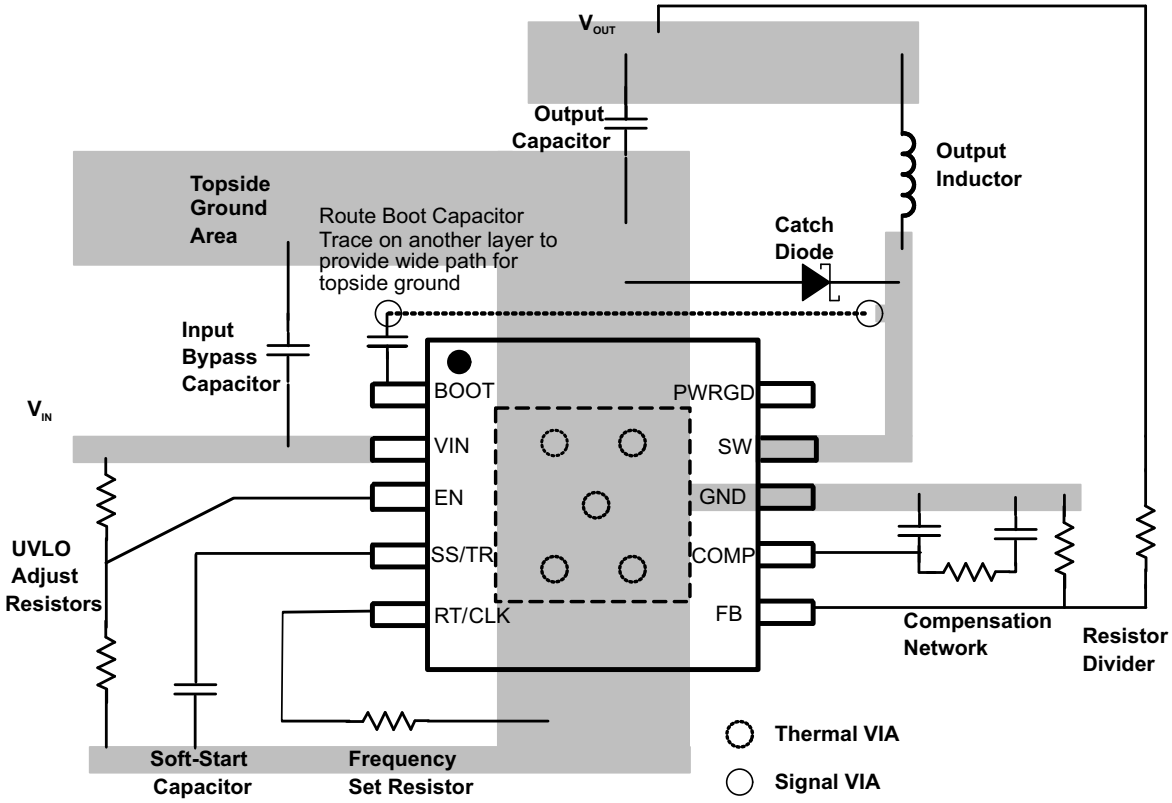


Figure 66. PCB Layout Example

Estimated Circuit Area

Boxing in the components in the design of Figure 46 the estimated printed circuit board area is 1.025 in^2 (661 mm^2). This area does not include test points or connectors.

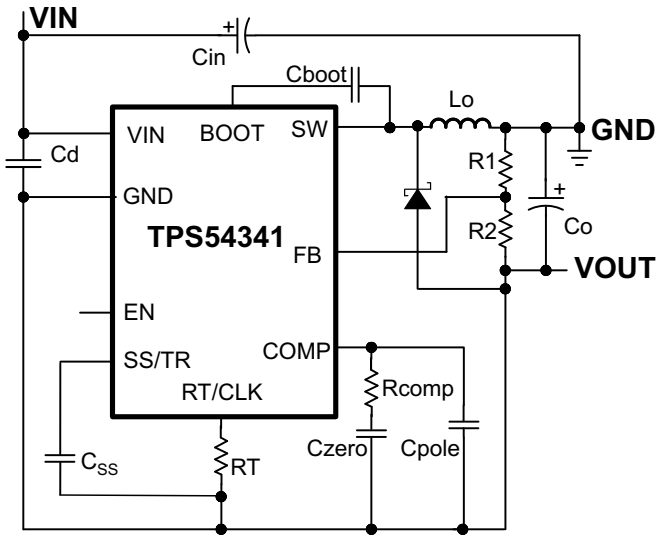


Figure 67. TPS54341 Inverting Power Supply Based on the Application Note, SLVA317

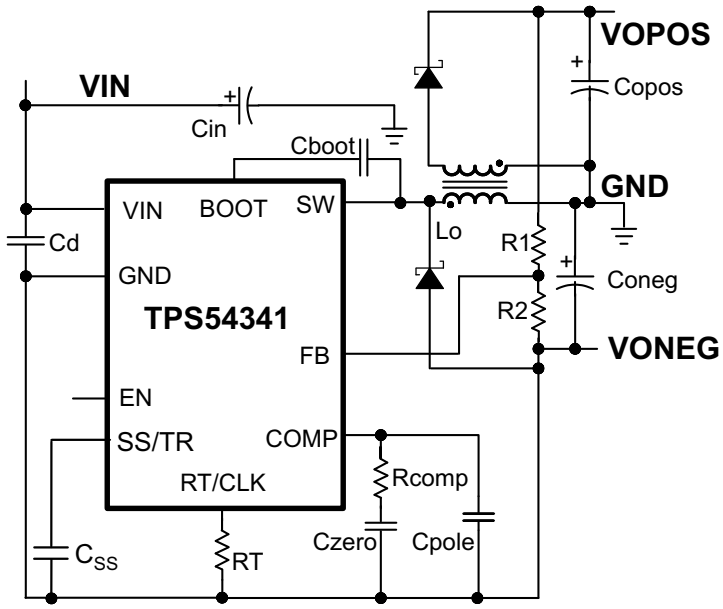


Figure 68. TPS54341 Split Rail Power Supply Based on the Application Note, SLVA369

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54341DPRR	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54341
TPS54341DPRR.A	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54341
TPS54341DPRR.B	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54341
TPS54341DPRRG4	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54341
TPS54341DPRRG4.A	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54341
TPS54341DPRRG4.B	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54341
TPS54341DPRT	Active	Production	WSON (DPR) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54341
TPS54341DPRT.A	Active	Production	WSON (DPR) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54341
TPS54341DPRT.B	Active	Production	WSON (DPR) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54341

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

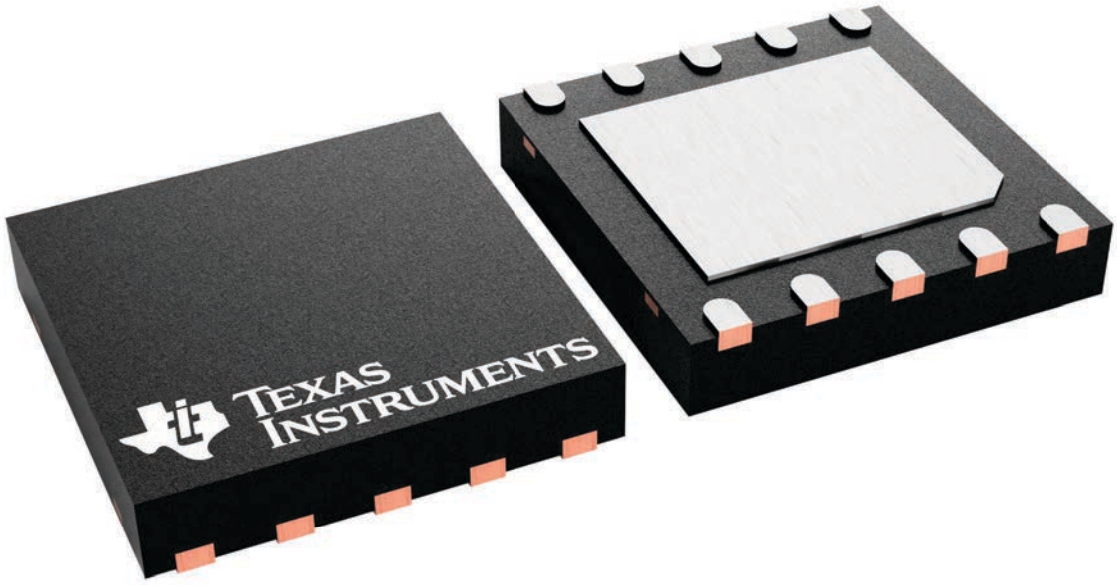
DPR 10

WSON - 0.8 mm max height

4 x 4, 0.8 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



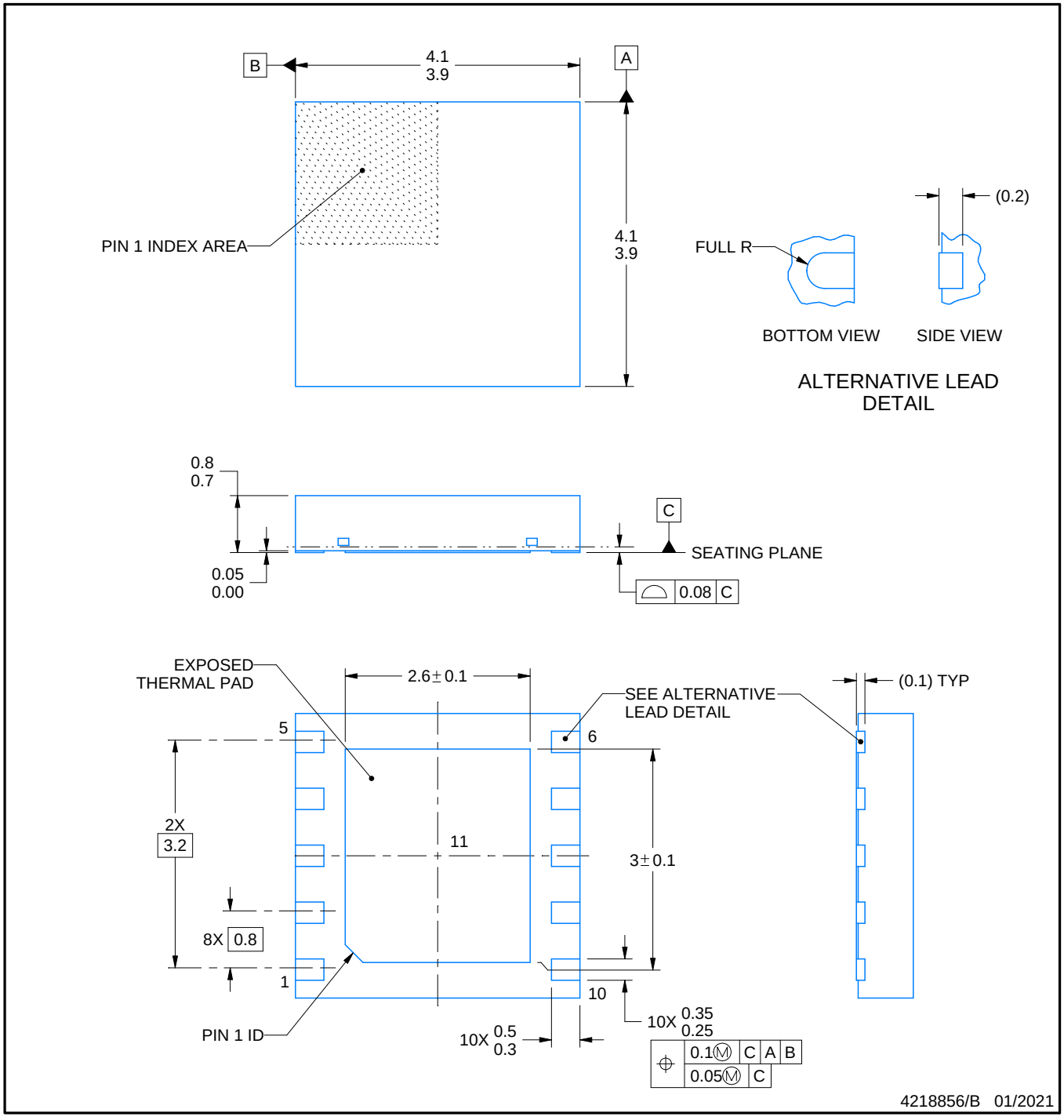
4232220/A

PACKAGE OUTLINE

DPR0010A

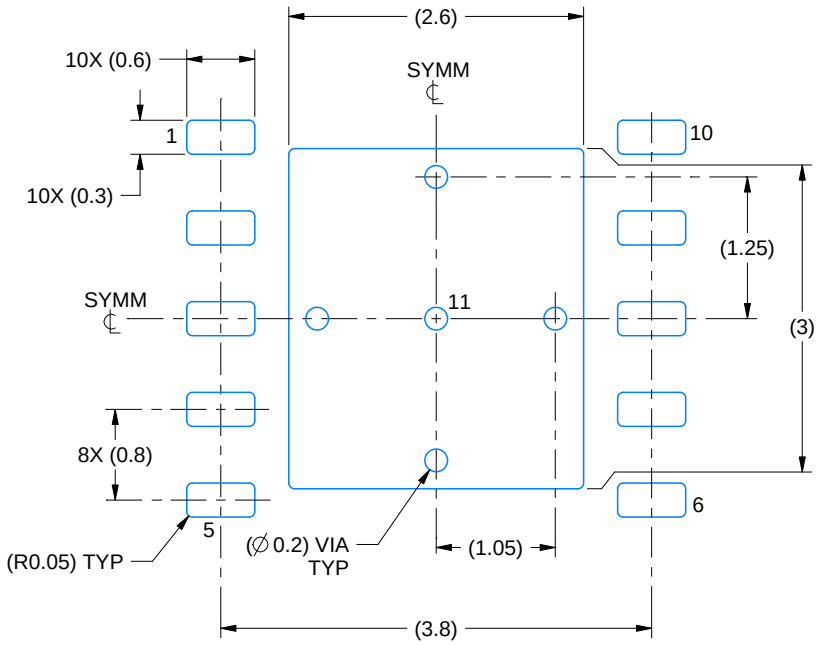
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

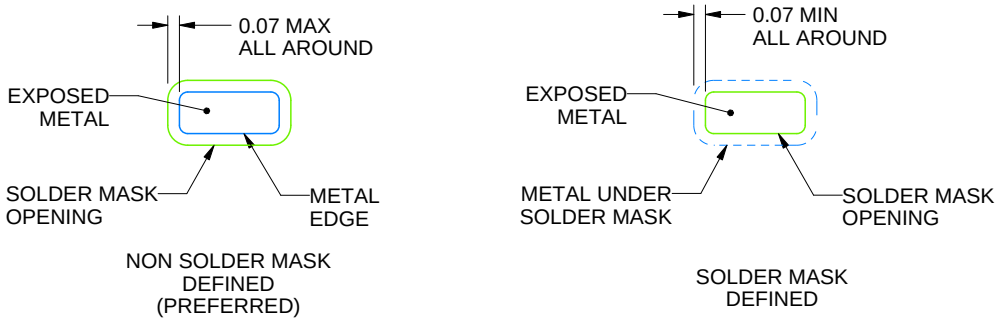


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

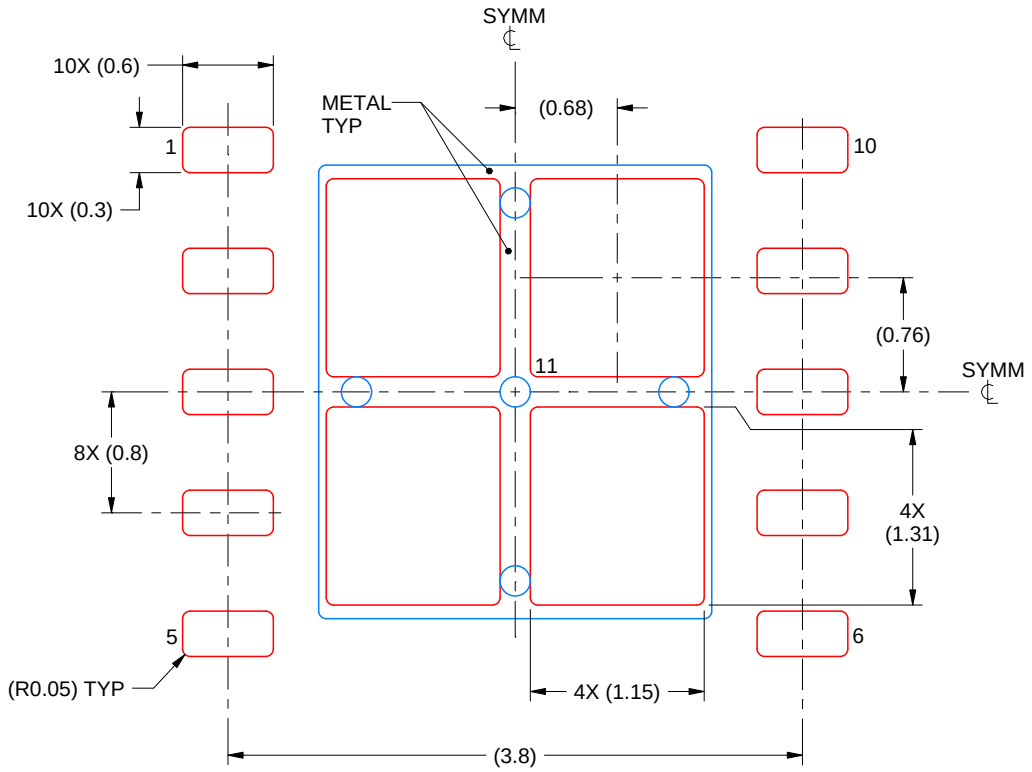


SOLDER MASK DETAILS

4218856/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218856/B 01/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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