固定频率 **99%** 占空比峰值电流模式笔记本系统功率控制器

查询样品: **TPS51220A-Q1**

特性

- 符合汽车应用要求
- 输入电压范围：**4.5V** 至 **32V**
- 输出电压范围：**1V** 至 **12V**
- 可选轻载操作
  （连续**/** 自动跳过 **/ Out-Of-Audio™** 跳过）
- 可编程降压补偿
- 电压伺服可调节软启动
- **200kHz** 至 **1MHz** 固定频率 **PWM**
- 可选电流**/ D-CAP™** 模式架构
- 通道间的 **180°** 相移
- 电阻或电感器 **DCR** 电流感应
- 自适应零交叉电路
- 每个通道的电源良好输出
- **OCL/OVP/UVP/UVLO** 保护
  （**OVP** 禁用选项）
- 热关断（非锁闭）
- 输出放电功能（禁用选项）
- 闭锁电流超过 **100mA**，符合 **JESD78 I** 类标准
- 集成自举 **MOSFET** 开关
- **QFN-32 (RTV)** 封装

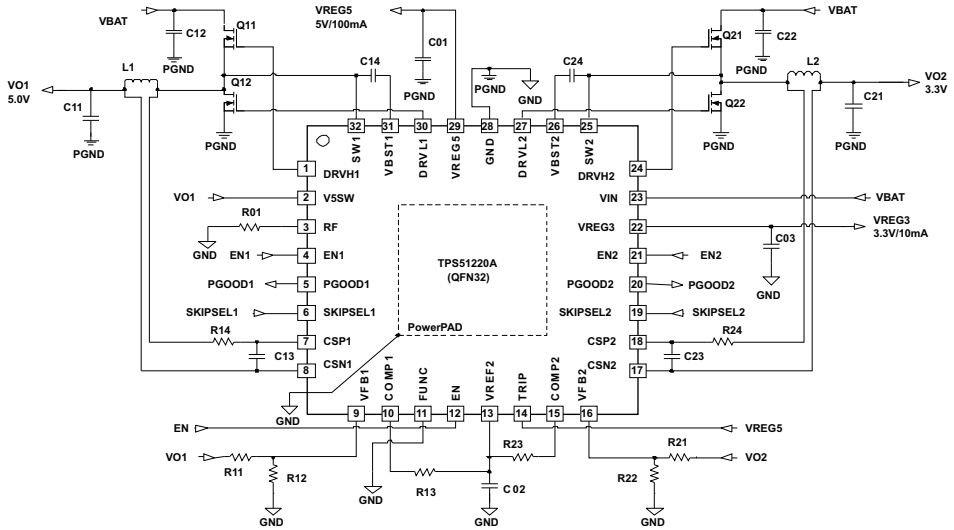
应用

- **I/O** 总线
- 液晶电视、多媒体框架产品 **(MFP)** 的负载点

说明

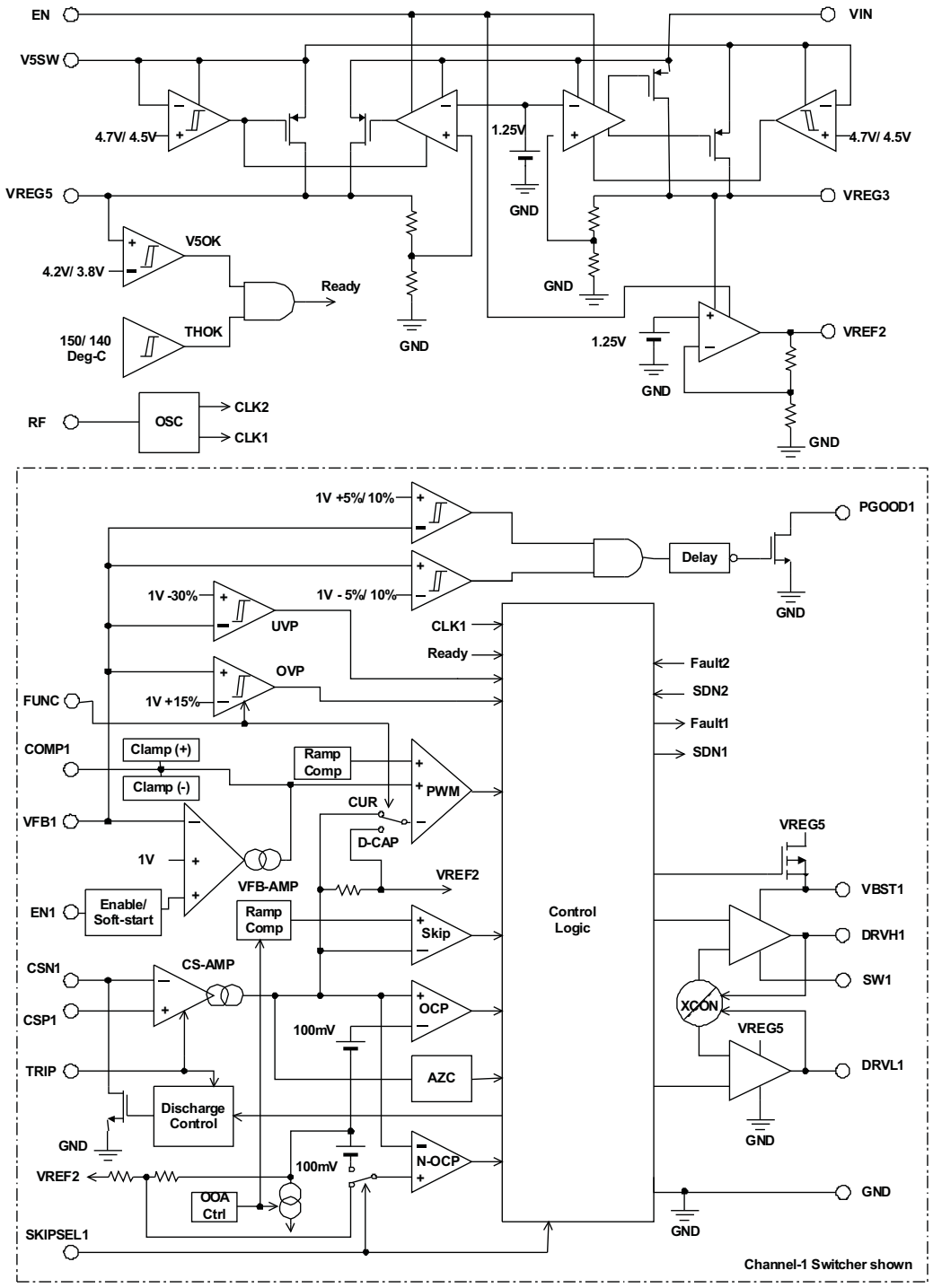
TPS51220A-Q1 是一个带有两个 LDO 的双路同步降压稳压器控制器 它针对 5V/3.3V 系统控制器进行过优化，使设计者能够经济高效地完善 2 节电池到 4 节电池的笔记本系统电源。 TPS51220A-Q1 支持高效、快速瞬态响应和 99% 的工作占空比。 它支持 4.5V 到 32V 的电源输入电压以及 1V 到 12V 的输出电压。可以根据应用来选择两种类型的控制方案。 峰值电流模式支持较低 ESR 电容器及输出精度的稳定运行。 D-CAP 模式支持快速瞬态响应。高占空比 (99%) 运行和宽输入/输出电压范围支持小型移动 PC 和各种其它应用的灵活设计。 固定频率可通过电阻在 200 kHz 到 1 MHz 之间进行调节，而每个通道运行 180° 相移。 TPS51220A-Q1 可以与外部时钟同步，交错比可通过其自身占空比调节。 TPS51220A-Q1 采用 32 引脚 5×5/4×4 QFN 封装，可适应 –40°C 到 105°C 的环境。

典型应用电路



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		TPS51220A-Q1	UNIT
Input voltage range (2)	VIN	–0.3 to 34	V
	VBST1, VBST2	–0.3 to 39	
	VBST1, VBST2(3)	–0.3 to 7	
	SW1, SW2	–7 to 34	
	CSP1, CSP2, CSN1, CSN2	–1 to 13.5	
	EN, EN1, EN2, VFB1, VFB2, TRIP, SKIPSEL1, SKIPSEL2, FUNC	–0.3 to 7	
	V5SW	–1 to 7	
	V5SW (to VREG5)(4)	–7 to 7	
Output voltage range(2)	DRVH1, DRVH2	–7 to 39	V
	DRVH1, DRVH2 (3)	–0.3 to 7	V
	DRVL1, DRVL2, COMP1, COMP2, VREG5, RF, VREF2, PGOOD1, PGOOD2	–0.3 to 7	V
	VREG3	–0.3 to 3.6	V
T_J Junction temperature		150	°C
T_{stg} Storage temperature		–55 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the corresponding SW terminal.
(4) When EN is high and V5SW is grounded, or voltage is applied to V5SW when EN is low.

DISSIPATION RATINGS (2 oz. Trace and Copper Pad with Solder)

PACKAGE	T_A < 25°C POWER RATING (W)	DERATING FACTOR ABOVE T_A = 25°C (mW/°C)	T_A = 105°C POWER RATING (W)
32-pin RTV	1.7	17	0.34

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage	VIN	4.5		32	V
	V5SW	–0.8		6	
I/O voltage	VBST1, VBST2	–0.1		37	V
	DRVH1, DRVH2	–4.		37	
	DRVH1, DRVH2 (wrt SW1, 2)	–0.1		6	
	DRVH1, DRVH2 (negative overshoot -6 V for t < 20% duration of the switching period)	-6		37	
	SW1, SW2	–4.		32	
	SW1, SW2 (negative overshoot -6 V for t < 20% duration of the switching period)	-6		32	
	CSP1, CSP2, CSN1, CSN2	–0.8		13	
	EN, EN1, EN2, VFB1, VFB2, TRIP, DRVL1, DRVL2, COMP1, COMP2, VREG5, RF, VREF2, PGOOD1, PGOOD2, SKIPSEL1, SKIPSEL2, FUNC	–0.1		6	
	VREG3	–0.1		3.5	
T_A Operating free-air temperature		–40		105	°C

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	QFN – RTV	Reel of 3000	TPS51220ATRTVRQ1	51220AT

(1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or see the TI website at www.ti.com.

ESD RATINGS TABLE

PARAMTER		VALUE	UNIT
ESD	Human Body Model (HBM)	2000	V
	Charged-Device Model	500	V
	Machine Model (MM)	100	V

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, EN = 3.3V, VIN = 12V, V5SW = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{VINSDN}	VIN shutdown current	VIN shutdown current, T_A = 25°C, No Load, EN = 0V, V5SW = 0 V			7	15	µA
$I_{VINSTBY}$	VIN Standby Current	VIN standby current, T_A = 25°C, No Load, EN1 = EN2 = V5SW = 0 V			80	120	µA
$I_{VBATSTBY}$	VBAT Standby Current	Vbat standby current, T_A = 25°C, No Load SKIPSEL2 = 2V, EN2 = open, EN1 = V5SW = 0V(1)			500		µA
I_{V5SW}	V5SW Supply Current	V5SW current, T_A = 25°C, No Load, ENx = 5V, VFBx = 1.05 V	TRIP = 5 V		0.8		mA
			TRIP = 0 V		0.9		mA
VREF2 OUTPUT							
V_{VREF2}	VREF2 Output Voltage	$I_{(VREF2)}$ < ±10 µA, T_A = 25°C		1.98	2.00	2.02	V
		$I_{(VREF2)}$ < ±100 µA, 4.5V < VIN < 32 V		1.97	2.00	2.03	
VREG3 OUTPUT							
V_{VREG3}	VREG3 Output Voltage	V5SW = 0 V, $I_{(VREG3)}$ = 0 mA, T_A = 25°C		3.279	3.313	3.347	V
		V5SW = 0 V, 0 mA < $I_{(VREG3)}$ < 10 mA, 5.5 V < VIN < 32 V		3.135	3.300	3.400	
I_{VREG3}	VREG3 Output Current	VREG3 = 3 V		10	15	20	mA
VREG5 OUTPUT							
V_{VREG5}	VREG5 Output Voltage	V5SW = 0 V, $I_{(VREG5)}$ = 0 mA, T_A = 25°C		4.99	5.04	5.09	V
		V5SW = 0 V, 0 mA < $I_{(VREG5)}$ < 100 mA, 6 V < VIN < 32 V		4.90	5.03	5.15	
		V5SW = 0 V, 0 mA < $I_{(VREG5)}$ < 100 mA, 5.5 V < VIN < 32 V		4.50	5.03	5.15	V
I_{VREG5}	VREG5 Output Current	V5SW = 0 V, VREG5 = 4.5 V		100	150	200	mA
		V5SW = 5 V, VREG5 = 4.5 V		200	300	400	
V_{THV5SW}	Switchover Threshold	Turning on		4.55	4.7	4.83	V
		Hysteresis		0.15	0.20	0.25	
t_{dV5SW}	Switchover Delay	Turning on			7.7		ms
R_{V5SW}	5V SW On-Ressitance	$I_{(VREG5)}$ = 100 mA			0.5		Ω
OUTPUT							
V_{VFB}	VFB Regulation Voltage Tolerance	T_A = 25°C, No Load		0.9925	1.000	1.0075	V
		T_A = –40°C to 105°C , No Load		0.990	1.000	1.010	
I_{VFB}	VFB Input Current	VFBx = 1.05 V, COMPx = 1.8 V, T_A = 25°C		–50		50	nA
R_{DISCHG}	CSNx Discharge Resistance	ENx = 0 V, CSNx = 0.5 V, T_A = 25°C			20	40	Ω

(1) Specified by design. Detail external condition follows application circuit of 图 57.

ELECTRICAL CHARACTERISTICS (接下页)

over operating free-air temperature range, EN = 3.3V, VIN = 12V, V5SW = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VOLTAGE TRANSCONDUCTANCE AMPLIFIER							
g_{Mv}	Gain	T_A = 25°C			500		µS
V_{ID}	Differential Input Voltage Range			–30		30	mV
$I_{COMPSINK}$	COMP Maximum Sink Current	COMPx = 1.8 V	T_A = 0 to 105°C	27	33		µA
			T_A = –40 to 105°C	22	33		µA
$I_{COMPSRC}$	COMP Maximum Source Current	COMPx = 1.8 V			–33	–43	µA
V_{COMP}	COMP Clamp Voltage			2.18	2.22	2.26	V
V_{COMPN}	COMP Negative Clamp Voltage			1.73	1.77	1.81	V
CURRENT AMPLIFIER							
G_C	Gain	TRIP = 0V/2V, CSNx = 5V, T_A = 25°C (2)			3.333		
		TRIP = 3.3V/5V, CSNx = 5V, T_A = 25°C(2)			1.667		
V_{IC}	Common mode Input Voltage Range			0		13	V
V_{ID}	Differential Input Voltage Range	T_A = 25°C		–75		75	mV
POWERGOOD							
V_{THPG}	PG threshold	PG in from lower		92.5%	95%	97.5%	
		PG in from higher		102.5%	105%	107.5%	
		PG hysteresis			5%		
I_{PG}	PG sink current	PGOOD = 0.5 V			5		mA
$I_{PG(LK)}$	PG leak current	PGOOD = 5 V			0	1	µA
t_{PGDLY}	PGOOD delay	Delay for PG in		0.8	1.0	1.2	ms
SOFTSTART							
t_{SSDYL}	Soft Start Delay	Delay for Soft Start, ENx = Hi to SS-ramp starts			200		µs
t_{SS}	Soft Start Time	Internal Soft Start			960		µs
FREQUENCY AND DUTY CONTROL							
f_{SW}	Switching Frequency	R_F = 330 kΩ		273	303	333	kHz
V_{THRF}	RF Threshold	Lo to Hi		0.7	1.3	2	V
		Hysteresis			0.2		V
f_{SYNC}	Sync Input Frequency Range(2)			200		1000	kHz
$t_{ON(min)}$	Minimum On Time	$V_{(DRVH)}$ = 90% to 10%, No Load, CCM/ OOA(2)			120		ns
		$V_{(DRVH)}$ = 90% to 10%, No Load, Auto-skip			160	250	ns
$t_{OFF(min)}$	Minimum Off Time	$V_{(DRVH)}$ = 10% to 90%, No Load			290	400	ns
t_D	Dead time	DRVH-off to DRVL-on		10	30	50	ns
		DRVL-off to DRVH-on		30	40	70	ns
V_{DTH}	DRVH-off threshold	DRVH to GND (2)			1		V
V_{DTL}	DRVL-off threshold	DRVL to GND(2)			1		V

(2) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (接下页)

over operating free-air temperature range, EN = 3.3V, VIN = 12V, V5SW = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT SENSE							
$V_{OCL-ULV}$	Current limit threshold (ultra-low voltage)	TRIP=0V/ 2V, 2V<CSNx<12.6V	RTV package, T_A = 0 to 105°C	28	31	35	mV
			RSN package , T_A = 0 to 105°C	28	31	34	
			T_A = –40 to 105°C	27	31	37	
		TRIP=0V/ 2V, 0.95V<CSNx<12.6V	T_A = 0 to 105°C	27	31	36	
			T_A = –40 to 105°C	25	31	42	
V_{OCL-LV}	Current limit threshold (low voltage)	TRIP=3.3V/ 5V, 2V<CSNx<12.6V	T_A = 0 to 105°C	56	60	65	mV
			T_A = –40 to 105°C	55	60	68	
		TRIP=3.3V/ 5V, 0.95V<CSNx<12.6V	T_A = 0 to 105°C	55	60	67	
			T_A = –40 to 105°C	54	60	72	
V_{ZCAJ}	Auto-Zero cross adjustable offset range	0.95V < CSNx < 12.6V, Auto-skip	Positive		5		mV
			Negative		–5		
V_{ZC}	Zero cross detection comparator Offset	0.95V < CSNx < 12.6V, OOA		–5	0	4	mV
$V_{OCLN-ULV}$	Negative current limit threshold (ultra-low voltage)	TRIP = 0V/2V, 0.95V < CSNx < 12.6V	T_A = 0 to 105°C	–23	–31	–40	mV
			T_A = –40 to 105°C	–22	–31	–44	
$V_{OCLN-LV}$	Negative current limit threshold (low voltage)	TRIP = 3.3V/5V, 0.95V < CSNx < 12.6V	T_A = 0 to 105°C	–50	–60	–73	
			T_A = –40 to 105°C	–49	–60	–77	
OUTPUT DRIVERS							
R_{DRVH}	DRVH resistance	Source, $V_{(VBST-DRVH)}$ = 0.1 V			1.7	5	Ω
		Sink, $V_{(DRVH-SW)}$ = 0.1 V			1	3	
R_{DRVL}	DRVL resistance	Source, $V_{(VREG5-DRVL)}$ = 0.1 V			1.3	4	Ω
		Sink, $V_{(DRVL-GND)}$ = 0.1 V			0.7	2	
UVP, OVP AND UVLO							
V_{OVP}	OVP Trip Threshold	OVP detect		110%	115%	120%	
t_{OVPDLY}	OVP Prop Delay				1.5		µs
V_{UVP}	UVP Trip Threshold	UVP detect		65%	70%	73%	
t_{UVPDLY}	UVP Delay			0.8	1	1.2	ms
V_{UVREF2}	VREF2 UVLO Threshold	Wake up		1.7	1.8	1.9	V
		Hysteresis		75	100	125	mV
V_{UVREG3}	VREG3 UVLO Threshold	Wake up		3	3.1	3.2	V
		Hysteresis		0.10	0.15	0.20	
V_{UVREG5}	VREG5 UVLO Threshold	Wake up		4.1	4.2	4.3	V
		Hysteresis		0.35	0.40	0.44	V

ELECTRICAL CHARACTERISTICS (接下页)

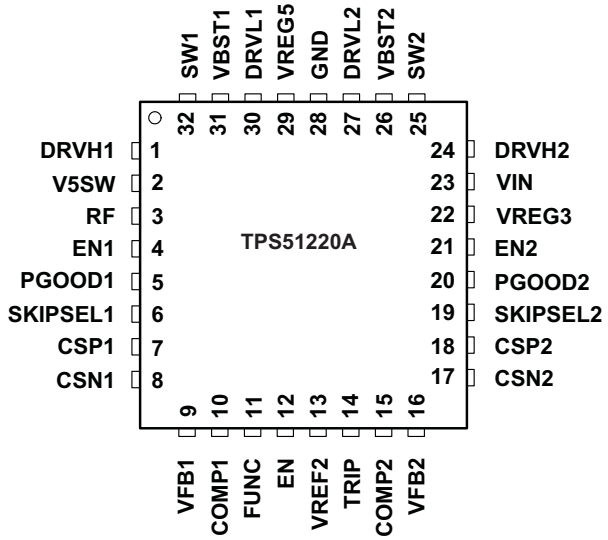
over operating free-air temperature range, EN = 3.3V, VIN = 12V, V5SW = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERFACE AND LOGIC THRESHOLD						
V_{EN}	EN Threshold	Wake up	0.8	1	1.2	V
		Hysteresis	0.1	0.2	0.3	
I_{ENLK}	EN leak current	EN = 0 V, or EN = 3.3 V	-1		1	µA
V_{EN12}	EN1/EN2 Threshold	Wake up	0.45	0.50	0.55	V
		Hysteresis	0.1	0.2	0.3	
V_{EN12SS}	EN1/EN2 SS Start Threshold	SS-ramp start threshold at external soft start		1		V
$V_{EN12SSEND}$	EN1/EN2 SS End Threshold	SS-End threshold at external soft start (3)		2		V
I_{EN12}	EN1/EN2 Source Current	VEN1/EN2 = 0V	1.6	2	2.4	µA
$V_{SKIPSEL}$	SKIPSEL1/SKIPSEL2 Setting Voltage	Continuous			1.5	V
		Auto Skip	1.9		2.1	
		OOA Skip (min 1/8 Fsw)	3.2		3.4	
		OOA Skip (min 1/16 Fsw)	3.8			
V_{TRIP}	TRIP Setting Voltage	$V_{(OCL-ULV)}$, Discharge ON			1.5	V
		$V_{(OCL-ULV)}$, Discharge OFF	1.9		2.1	
		$V_{(OCL-LV)}$, Discharge OFF	3.2		3.4	
		$V_{(OCL-LV)}$, Discharge ON	3.8			
V_{FUNC}	FUNC Setting Voltage	Current mode, OVP enable			1.5	V
		D-CAP mode, OVP disable	1.9		2.1	
		D-CAP mode, OVP enable	3.2		3.4	
		Current mode, OVP disable	3.8			
I_{TRIP}	TRIP Input Current	TRIP = 0 V	–1		1	µA
		TRIP = 5 V	–1		1	
$I_{SKIPSEL}$	SKIPSEL Input Current	SKIPSELx = 0 V	–0.5		0.5	µA
		SKIPSELx = 5 V	–0.5		0.5	
BOOT STRAP SW						
V_{FBST}	Forward Voltage	$V_{VREG5-VBST}$, I_F = 10 mA, T_A = 25°C		0.10	0.20	V
I_{BSTLK}	VBST Leakage Current	V_{VBST} = 37 V, V_{SW} = 32 V		0.01	1.5	µA
THERMAL SHUTDOWN						
T_{SDN}	Thermal SDN Threshold	Shutdown temperature (3)		150		°C
		Hysteresis (3)		10		

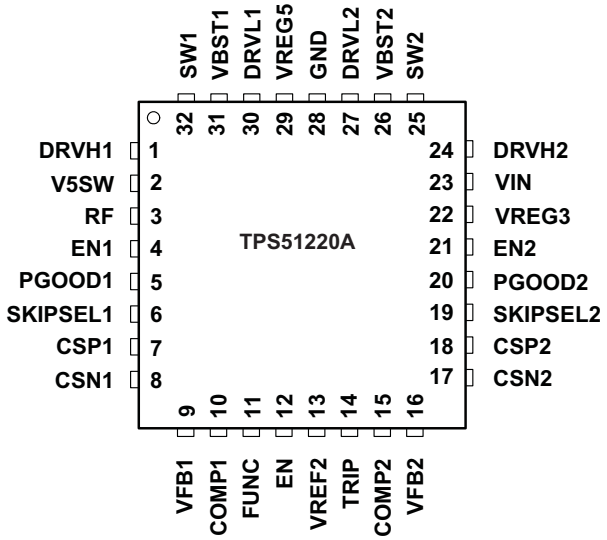
(3) Specified by design. Not production tested.

DEVICE INFORMATION

RSN PACKAGE
(TOP VIEW)



RTV PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
DRVH1	1	O	High-side MOSFET gate driver outputs. Source 1.7 Ω, sink 1.0 Ω, SW-node referenced floating driver. Drive voltage corresponds to VBST to SW voltage.
DRVH2	24		
SW2	25	I/O	High-side MOSFET gate driver returns.
SW1	32		
VREG3	22	O	Always alive 3.3 V, 10 mA low dropout linear regulator output. Bypass to (signal) GND with more than 1-µF ceramic capacitance. Runs from VIN supply or from VREG5 when it is switched over to V5SW input.
EN1	4	I	Channel 1 and channel 2 SMPS Enable Pins. When turning on, apply greater than 0.55 V and less than 6 V, or leave floating. Connect to GND to disable. Adjustable soft-start capacitance to be attached here.
EN2	21		
PGOOD1	5	O	Powergood window comparator outputs for channel 1 and channel 2. The recommended applied voltage should be less than 6 V, and the recommended pull-up resistance value is from 100 kΩ to 1 MΩ.
PGOOD2	20		
SKIPSEL1	6	I	Skip mode selection pin. GND: Continuous conduction mode VREF2: Auto Skip VREG3: OOA Auto Skip, maximum 7 skips (suitable for f_{SW} < 400kHz) VREG5: OOA Auto Skip, maximum 15 skips (suitable for equal to or greater than 400kHz)
SKIPSEL2	19		
CSP1	7	I/O	Current sense comparator inputs (+). An RC network with high quality X5R or X7R ceramic capacitor should be used to extract voltage drop across DCR. 0.1-µF is a good value to start the design. See the current sensing scheme section for more details.
CSP2	18		
CSN1	8	I	Current sense comparator inputs (–). See the current sensing scheme section. Used as power supply for the current sense circuit for 5V or higher output voltage setting. Also, used for output discharge terminal.
CSN2	17		
VFB1	9	I	SMPS voltage feedback Inputs. Connect the feedback resistors divider, and should be referred to (signal) GND.
VFB2	16		
COMP1	10	I	Loop compensation pin for current mode (error amplifier output). Connect R (and C if required) from this pin to VREF2 for proper loop compensation with current mode operation. Ramp compensation adjustable pin for D-CAP mode, connect R from this pin to VREF2. 10 kΩ is a good value to start the design. 6 kΩ to 20 kΩ can be chosen. See the D-CAP MODE section for more details.
COMP2	15		
RF	3	I/O	Frequency setting pin. Connect a frequency setting resistor to (signal) GND. Connect to an external clock for synchronization.

PIN FUNCTIONS (接下页)

PIN		I/O	DESCRIPTION
NAME	NO.		
FUNC	11	I	Control architecture and OVP functions selection pin. GND: Current mode, OVP enable VREF2: D-CAP mode, OVP disable VREG3: D-CAP mode, OVP enable VREG5: Current mode, OVP disable
VREF2	13	O	2-V reference output. Bypass to (signal) GND with 0.22-μF of ceramic capacitance.
TRIP	14	I	Overcurrent trip level and discharge mode selection pin. GND: $V_{(OCL-ULV)}$, discharge on VREF2: $V_{(OCL-ULV)}$, discharge off VREG3: $V_{(OCL-LV)}$, discharge off VREG5: $V_{(OCL-LV)}$, discharge on
EN	12	I	VREF2 and VREG5 linear regulators enable pin. When turning on, apply greater than 1.2 V and less than 6 V. Connect to GND to disable.
VBST1	31	I	Supply inputs for high-side N-channel FET driver (boot strap terminal). Connect a capacitor (0.1-μF or greater is recommended) from this pin to respective SW terminal. Additional SB diode from VREG5 to this pin is an optional.
VBST2	26		
DRVL1	30	O	Low-side MOSFET gate driver outputs. Source 1.3 Ω, sink 0.7 Ω, and GND referenced driver.
DRVL2	27		
V5SW	2	I	VREG5 switchover power supply input pin. When EN1 is high, PGOOD1 indicates GOOD and V5SW voltage is higher than 4.83 V, switch-over function is enabled. Note: When switch-over is enabled, VREG5 output voltage is approximately equal to the V5SW input voltage.
VREG5	29	O	5-V, 100-mA low dropout linear regulator output. Bypass to (power) GND using a 10-μF ceramic capacitor. Runs from VIN supply. Internally connected to VBST and DRVL. Shuts off with EN. Switches over to V5SW when 4.83 V or above is provided. Note: When switch-over (see above V5SW) is enabled, VREG5 output voltage is approximately equal to V5SW input voltage.
VIN	23	I	Supply input for 5-V and 3.3-V linear regulator. Typically connected to VBAT.
GND	28	–	Ground

TYPICAL CHARACTERISTICS

INPUT VOLTAGE SHUTDOWN CURRENT vs INPUT VOLTAGE

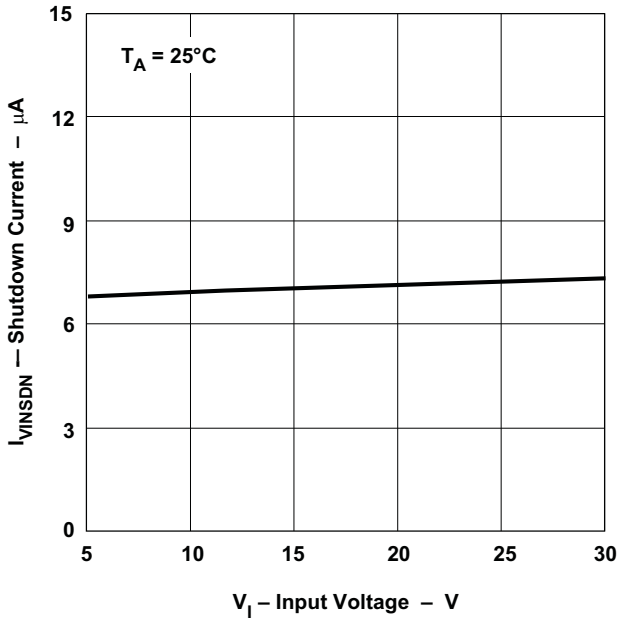


图 1.

INPUT VOLTAGE SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

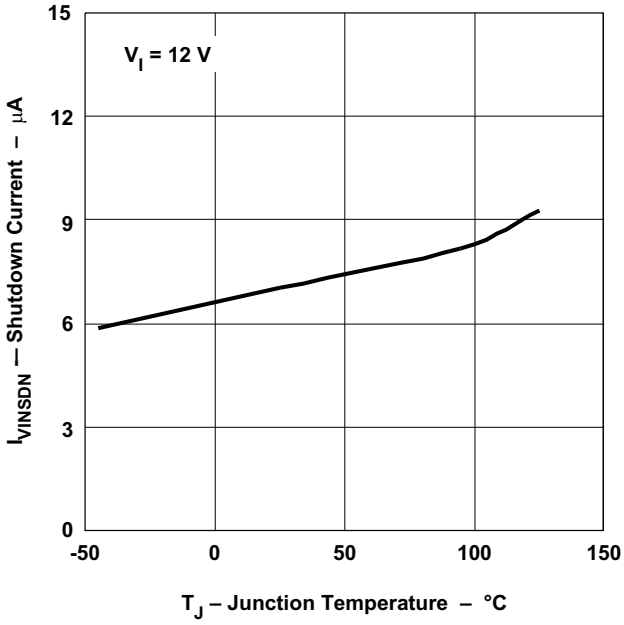


图 2.

INPUT VOLTAGE STANDBY CURRENT vs JUNCTION TEMPERATURE

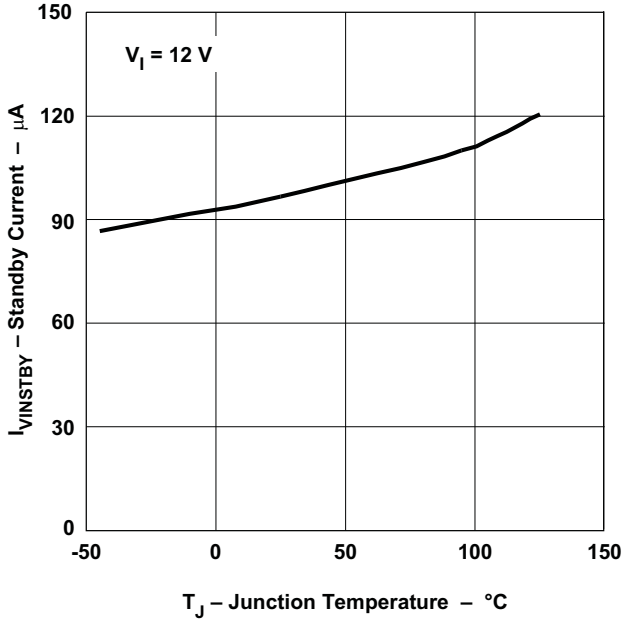


图 3.

INPUT VOLTAGE STANDBY CURRENT vs INPUT VOLTAGE

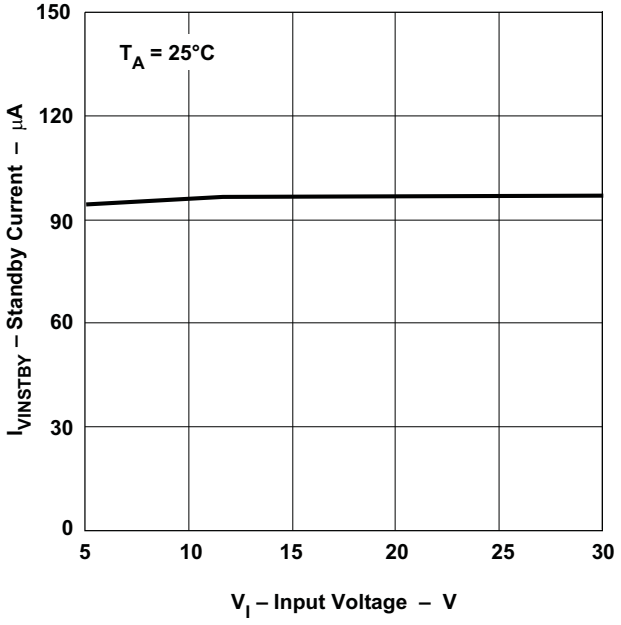


图 4.

TYPICAL CHARACTERISTICS (接下页)

NO LOAD BATTERY CURRENT vs INPUT VOLTAGE

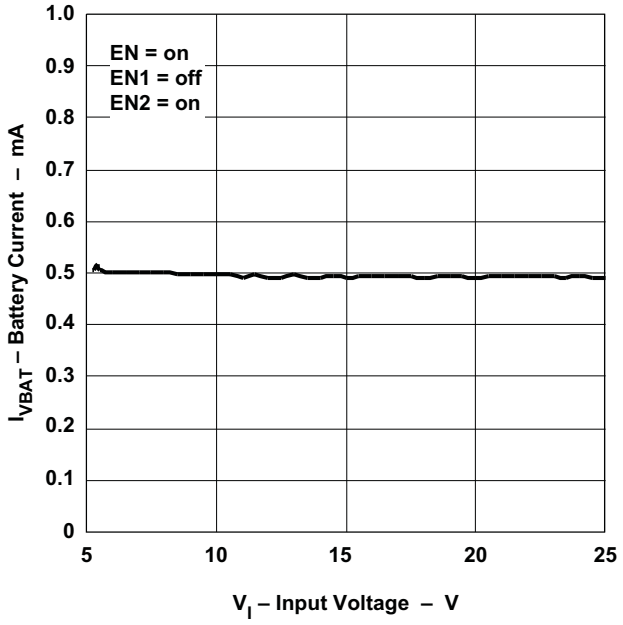


图 5.

NO LOAD BATTERY CURRENT vs INPUT VOLTAGE

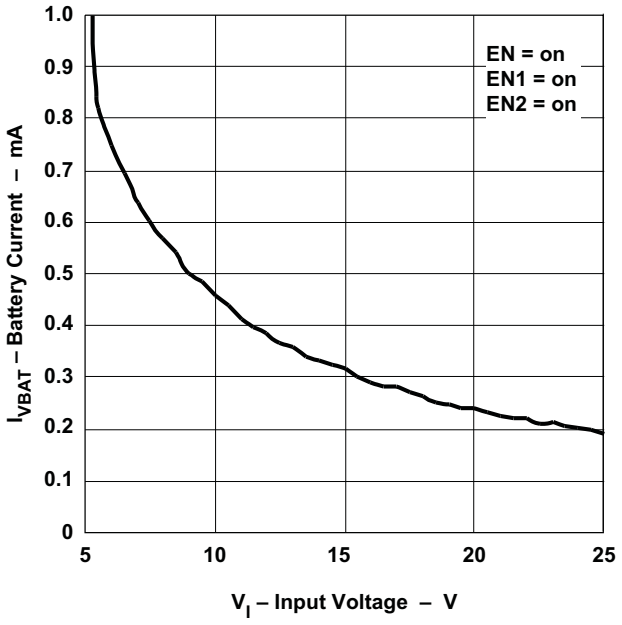


图 6.

BATTERY CURRENT vs INPUT VOLTAGE

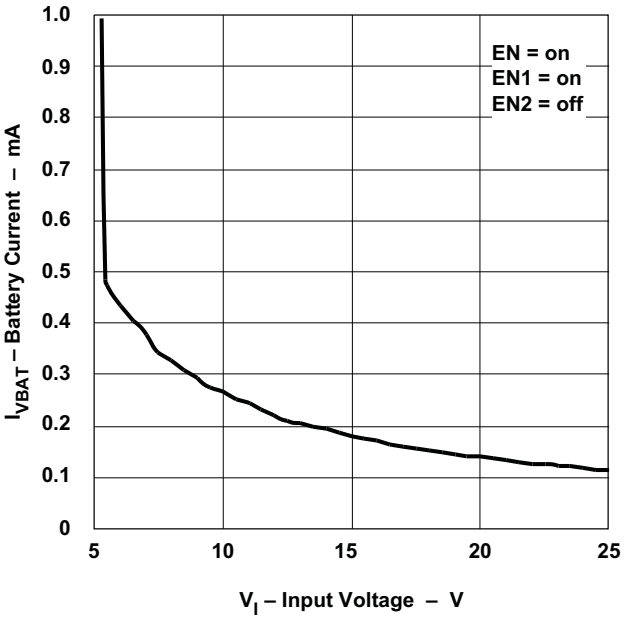


图 7.

VREF2 OUTPUT VOLTAGE vs OUTPUT CURRENT

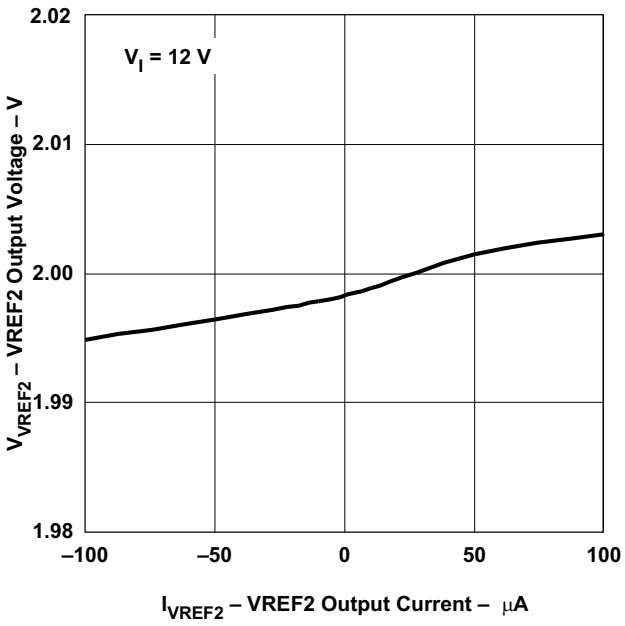


图 8.

TYPICAL CHARACTERISTICS (接下页)

VREG3 OUTPUT VOLTAGE vs OUTPUT CURRENT

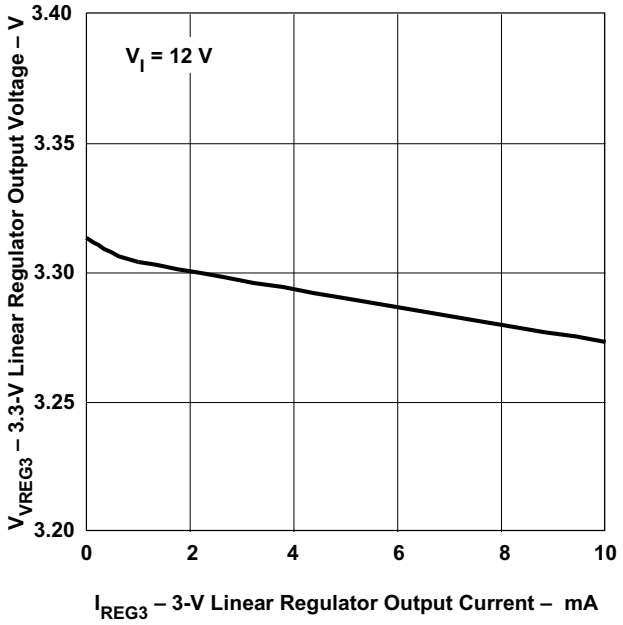


图 9.

VREG5 OUTPUT VOLTAGE vs OUTPUT CURRENT

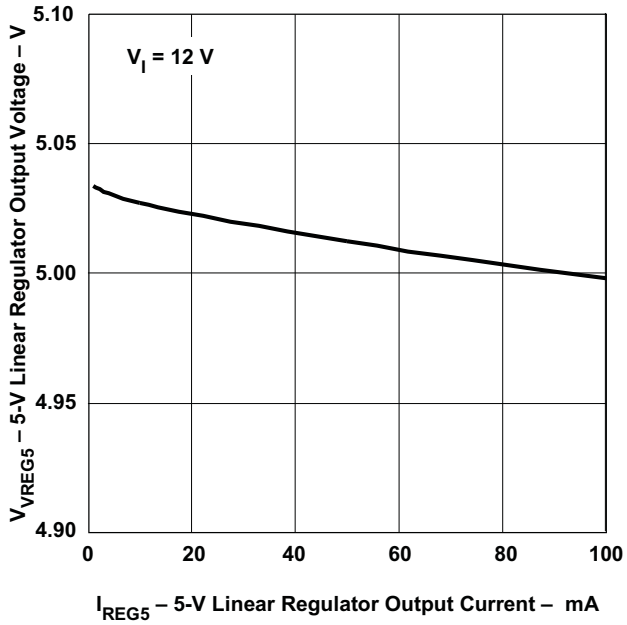


图 10.

SWITCHING FREQUENCY vs JUNCTION TEMPERATURE

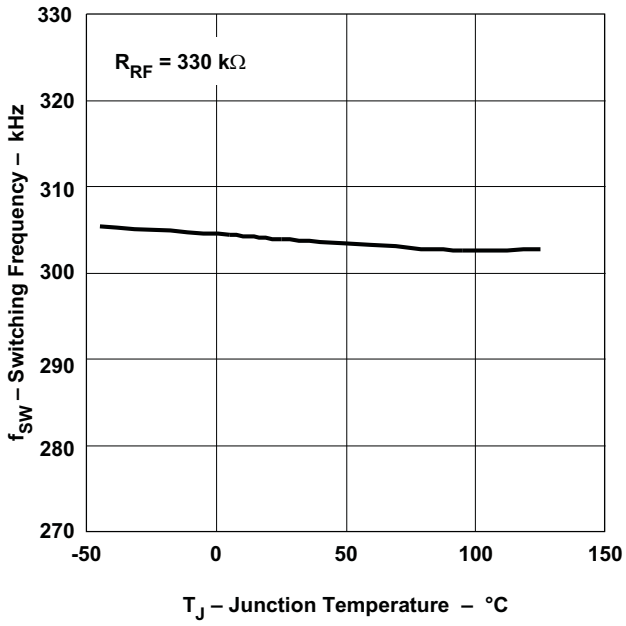


图 11.

FORWARD VOLTAGE OF BOOST SW vs JUNCTION TEMPERATURE

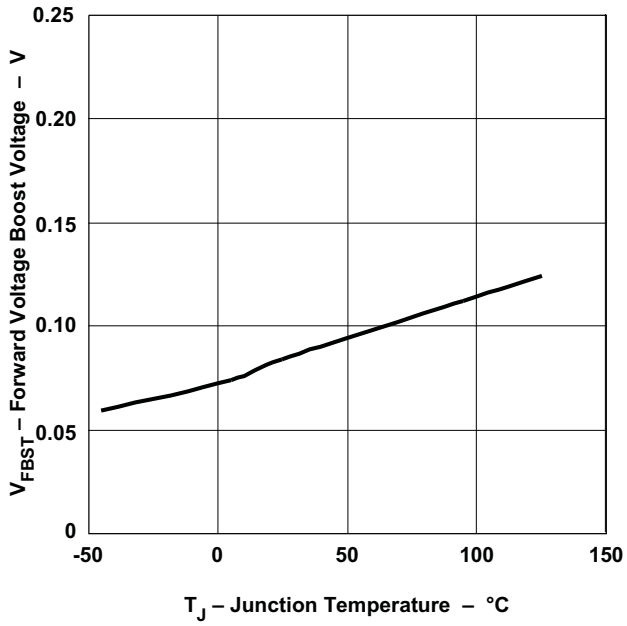


图 12.

TYPICAL CHARACTERISTICS (接下页)

OVP/UVP THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

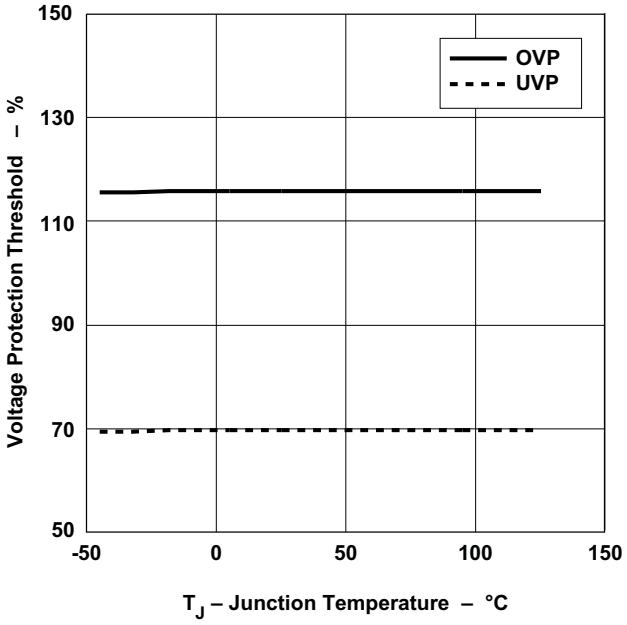


图 13.

VBST LEAKAGE CURRENT vs JUNCTION TEMPERATURE

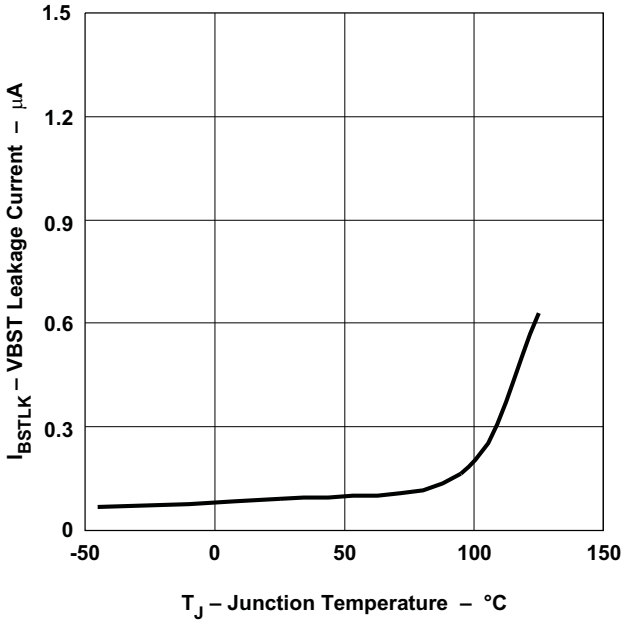


图 14.

CURRENT LIMIT THRESHOLD vs JUNCTION TEMPERATURE

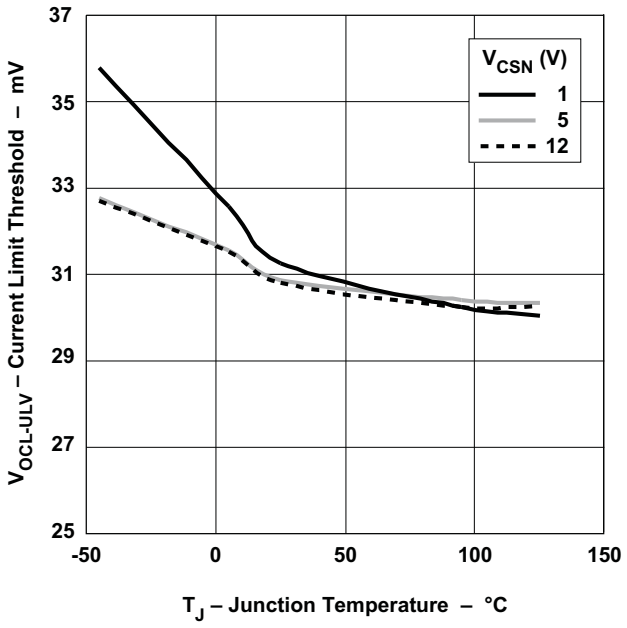


图 15.

CURRENT LIMIT THRESHOLD vs JUNCTION TEMPERATURE

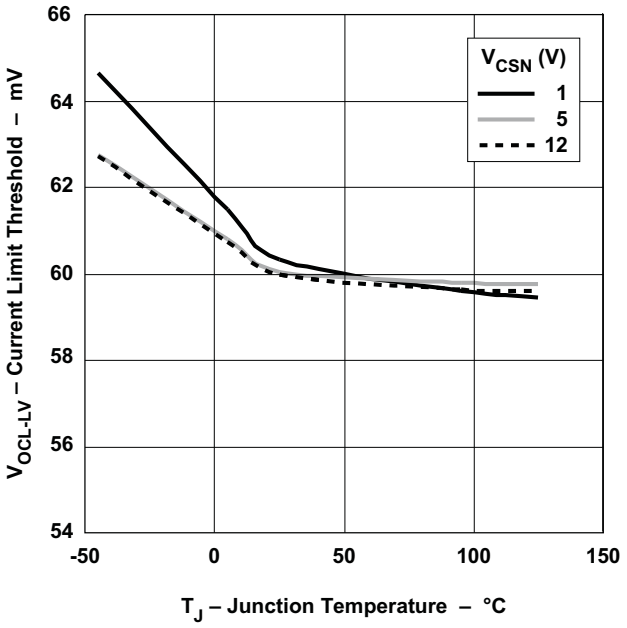


图 16.

TYPICAL CHARACTERISTICS (接下页)

5-V OUTPUT VOLTAGE vs INPUT VOLTAGE

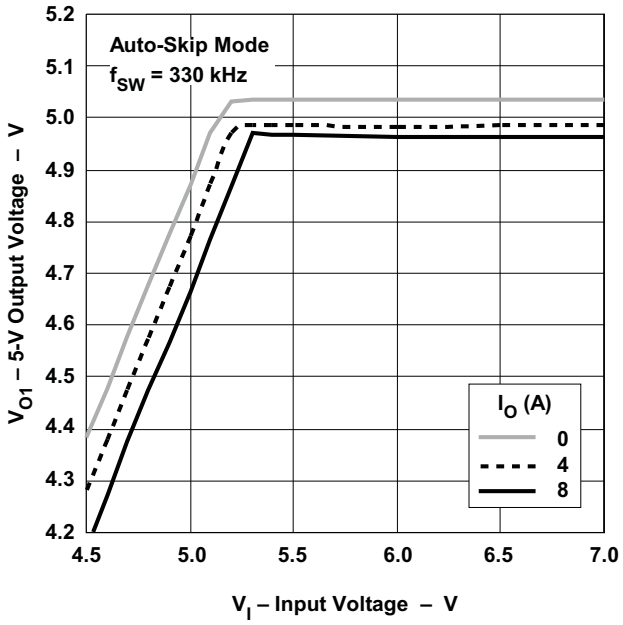


图 17.

3.3-V OUTPUT VOLTAGE vs INPUT VOLTAGE

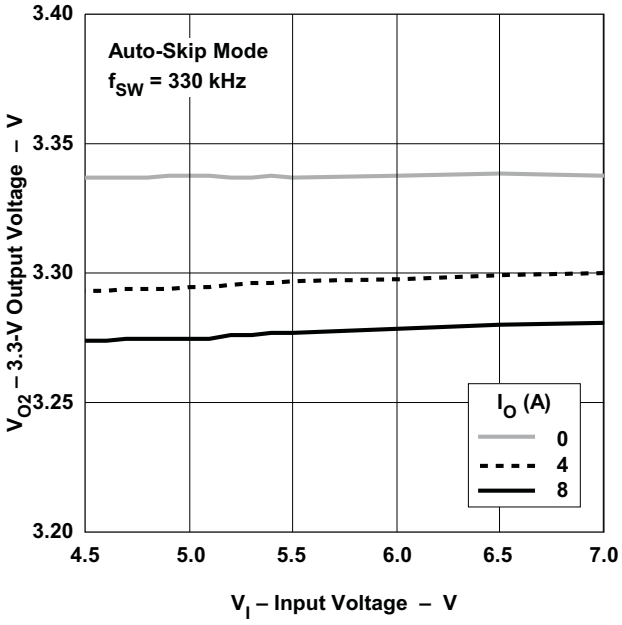


图 18.

5-V EFFICIENCY vs OUTPUT CURRENT

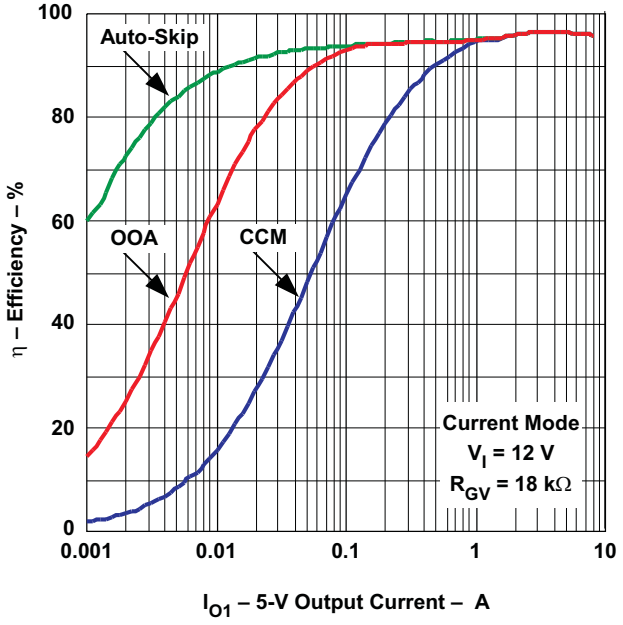


图 19.

5-V EFFICIENCY vs OUTPUT CURRENT

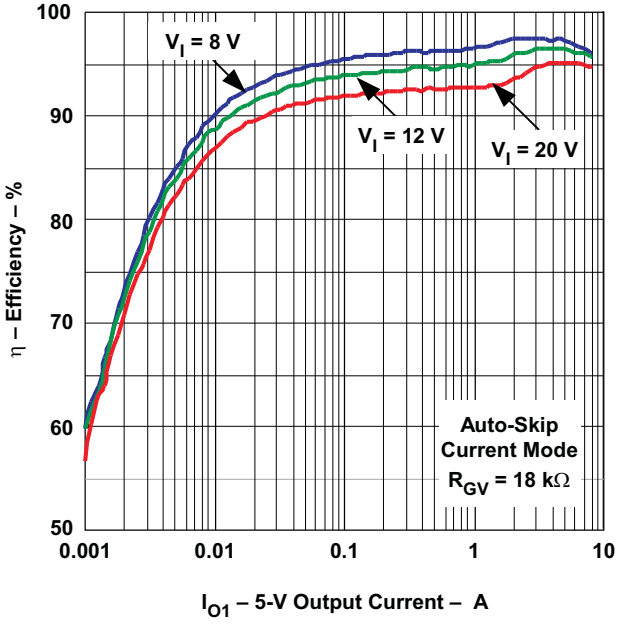


图 20.

TYPICAL CHARACTERISTICS (接下页)

3.3-V EFFICIENCY vs OUTPUT CURRENT

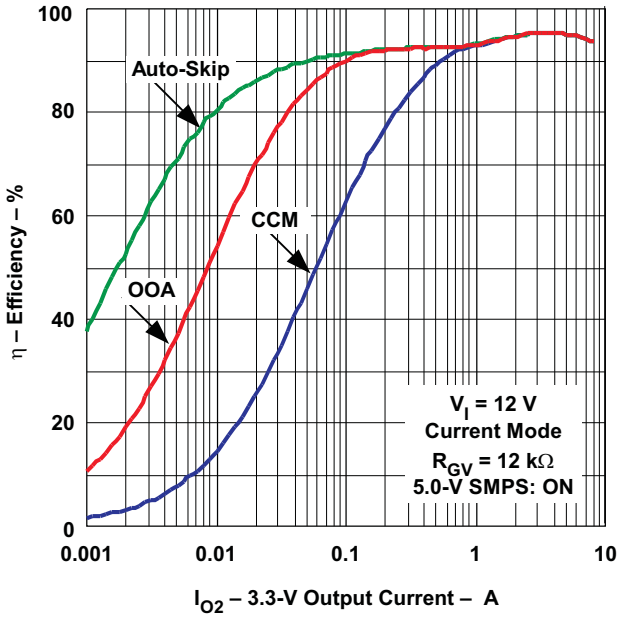


图 21.

3.3-V EFFICIENCY vs OUTPUT CURRENT

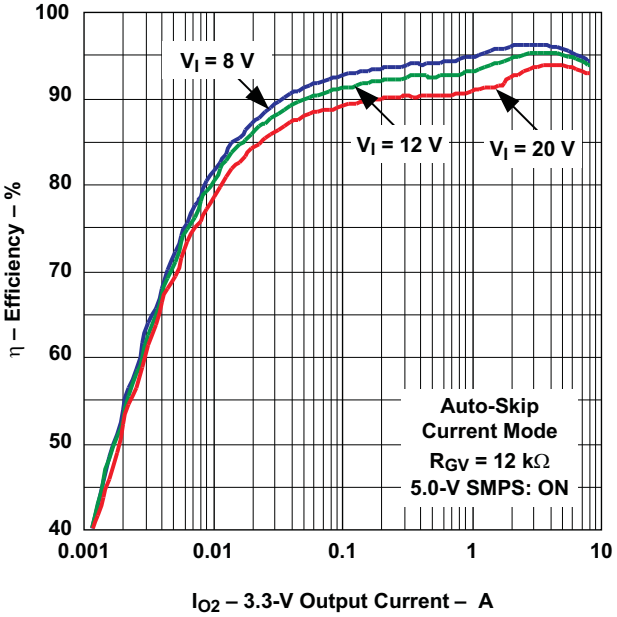


图 22.

5-V SWITCHING FREQUENCY vs OUTPUT CURRENT

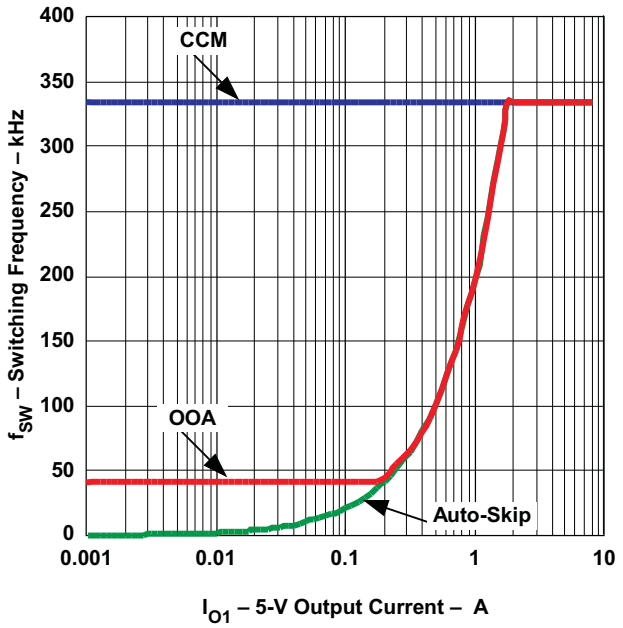


图 23.

3.3-V SWITCHING FREQUENCY vs OUTPUT CURRENT

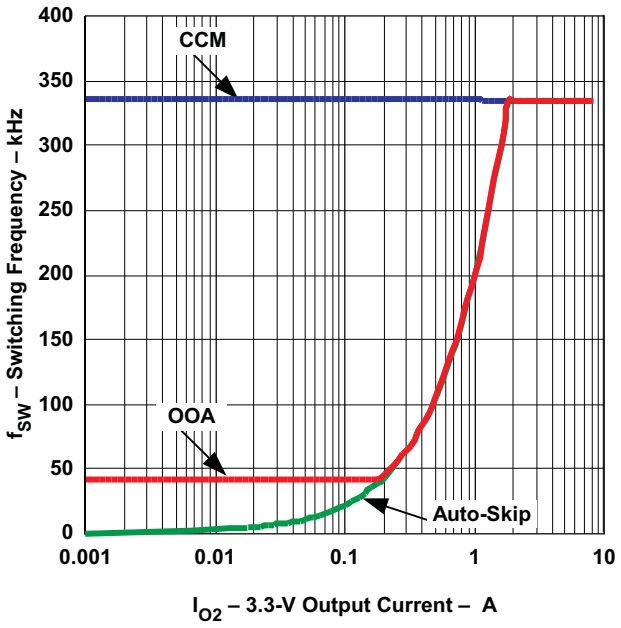


图 24.

TYPICAL CHARACTERISTICS (接下页)

5-V OUTPUT VOLTAGE
vs
OUTPUT CURRENT

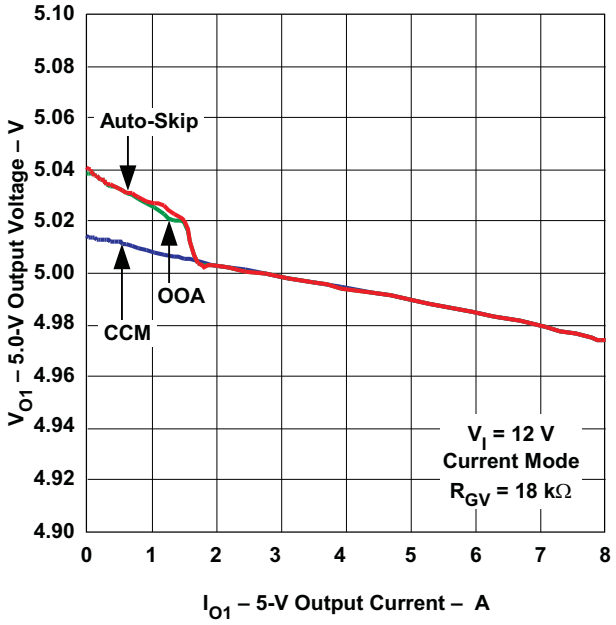


图 25.

3.3-V OUTPUT VOLTAGE
vs
OUTPUT CURRENT

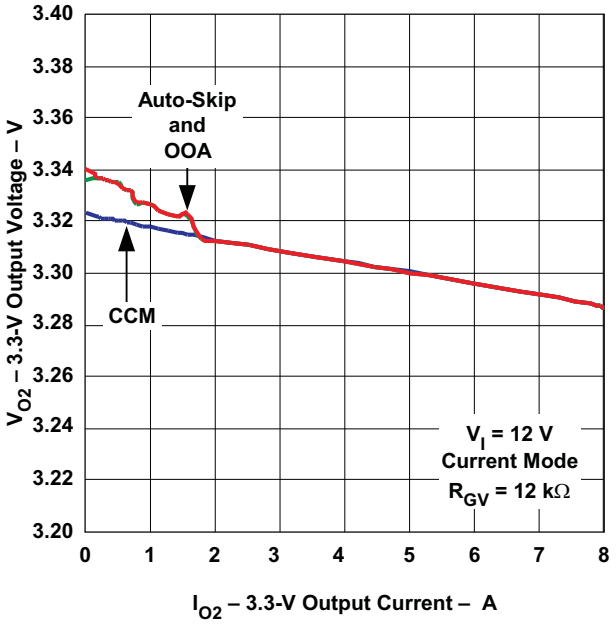


图 26.

5-V OUTPUT VOLTAGE
vs
OUTPUT CURRENT

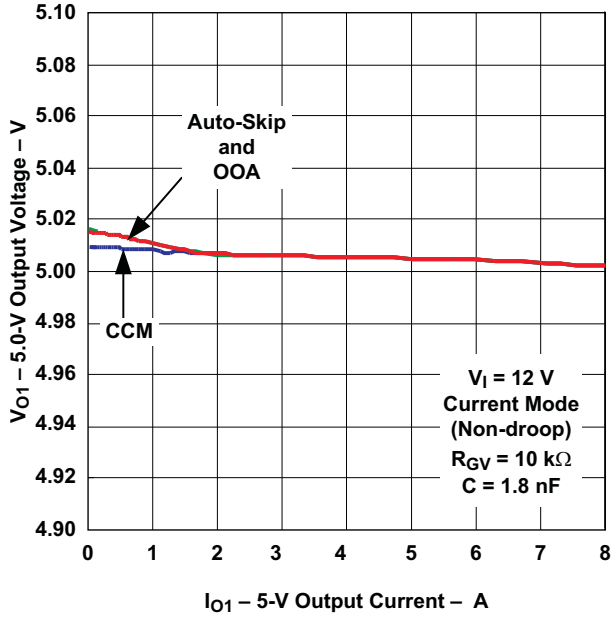


图 27.

3.3-V OUTPUT VOLTAGE
vs
OUTPUT CURRENT

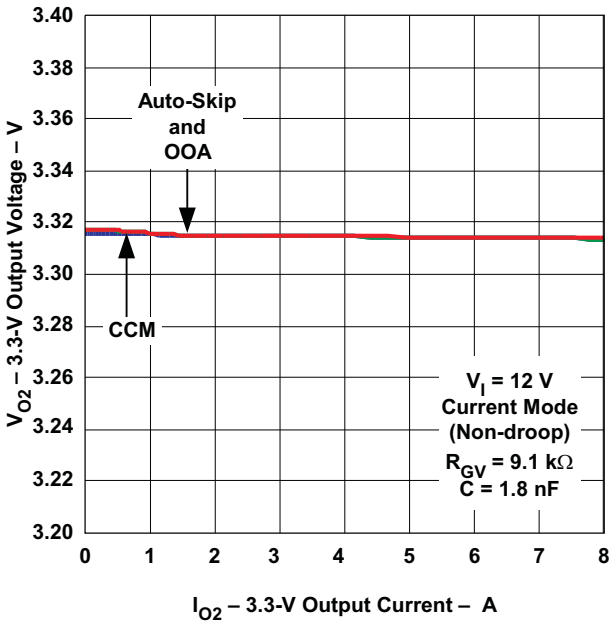


图 28.

TYPICAL CHARACTERISTICS (接下页)

5-V OUTPUT VOLTAGE vs OUTPUT CURRENT

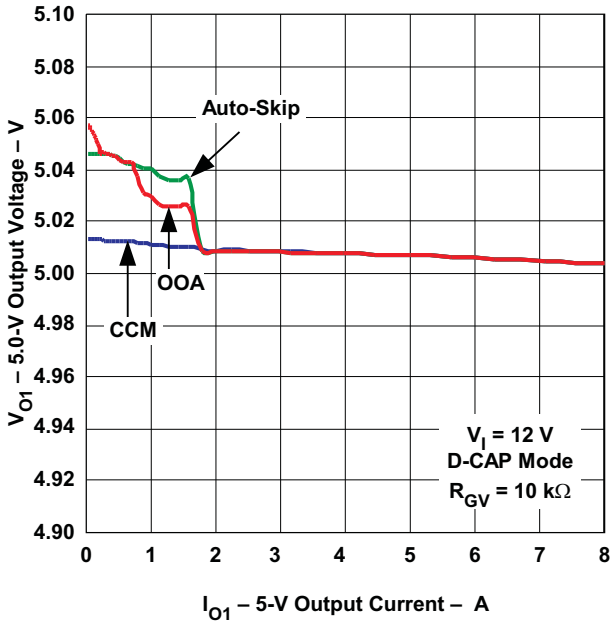


图 29.

3.3-V OUTPUT VOLTAGE vs OUTPUT CURRENT

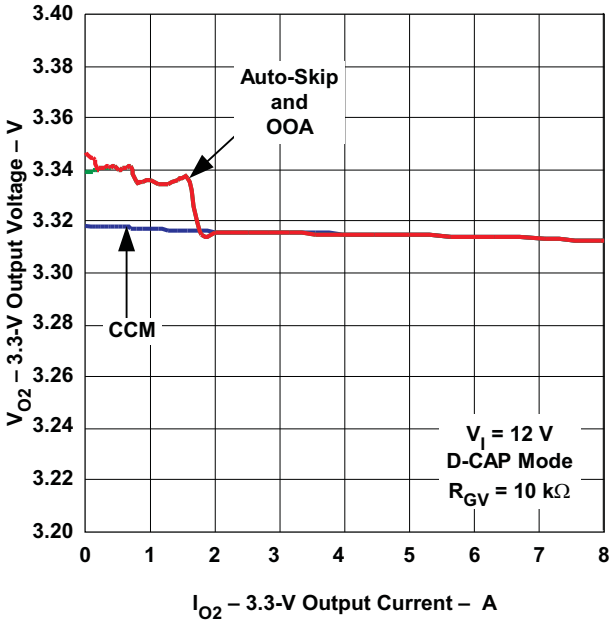


图 30.

5.0-V BODE-PLOT – GAIN AND PHASE vs FREQUENCY

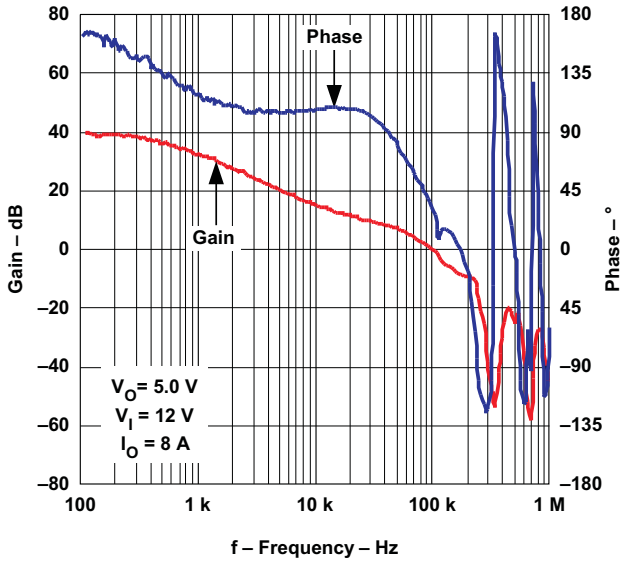


图 31.

3.3-V BODE-PLOT – GAIN AND PHASE vs FREQUENCY

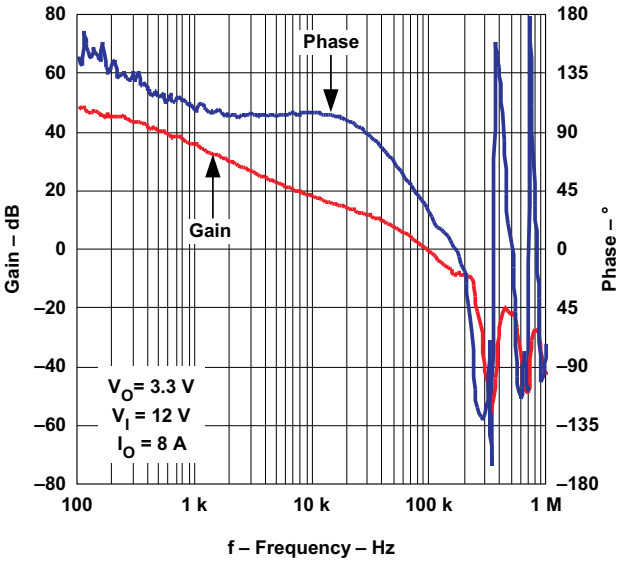


图 32.

TYPICAL CHARACTERISTICS (接下页)

5.0-V SWITCH-OVER WAVEFORMS

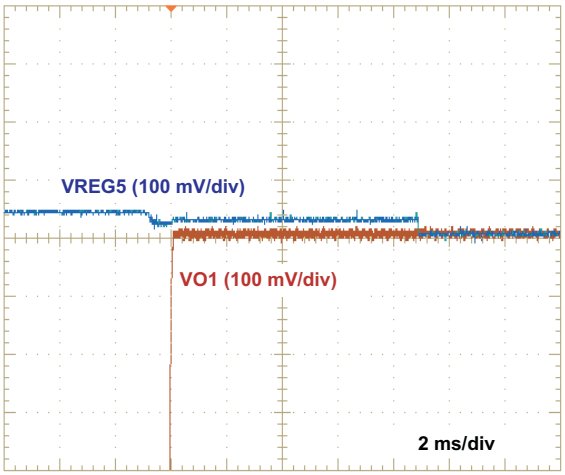


图 33.

TYPICAL CHARACTERISTICS

5.0-V START-UP WAVEFORMS

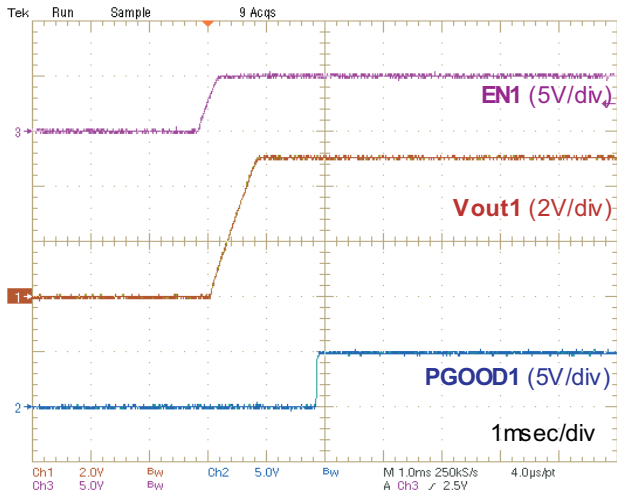


图 34.

3.3-V START-UP WAVEFORMS

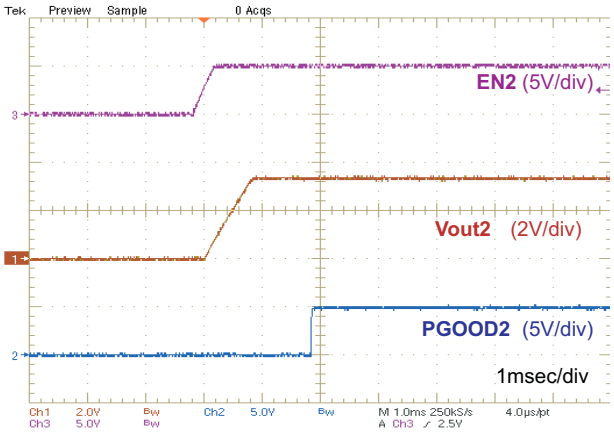


图 35.

5.0-V SOFT-STOP WAVEFORMS

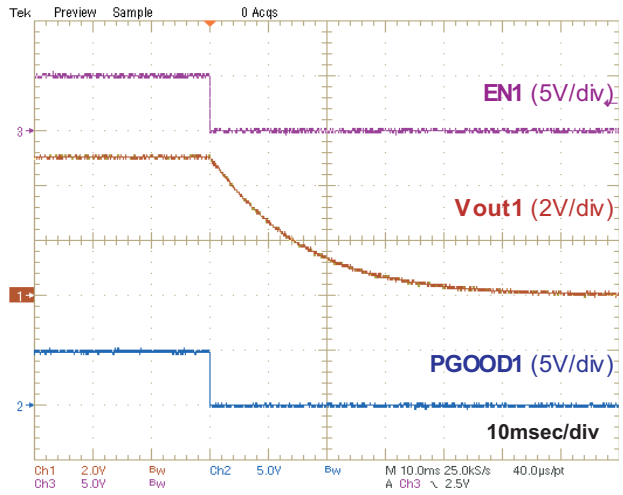


图 36.

3.3-V SOFT-STOP WAVEFORMS

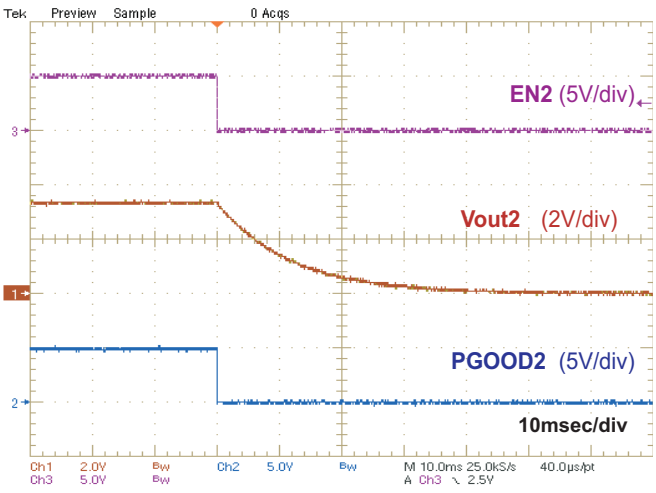


图 37.

TYPICAL CHARACTERISTICS (接下页)

5.0-V LOAD TRANSIENT RESPONSE

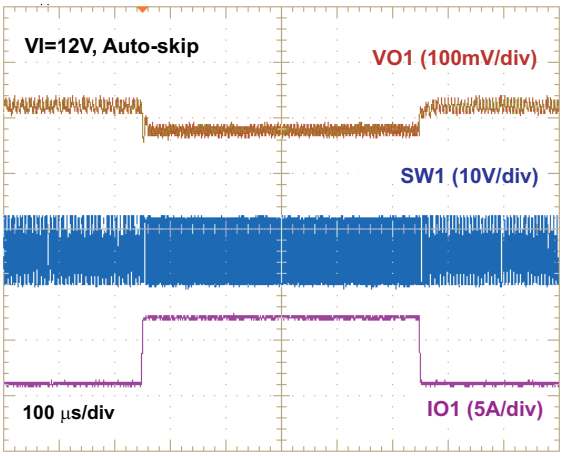


图 38.

3.3-V LOAD TRANSIENT RESPONSE

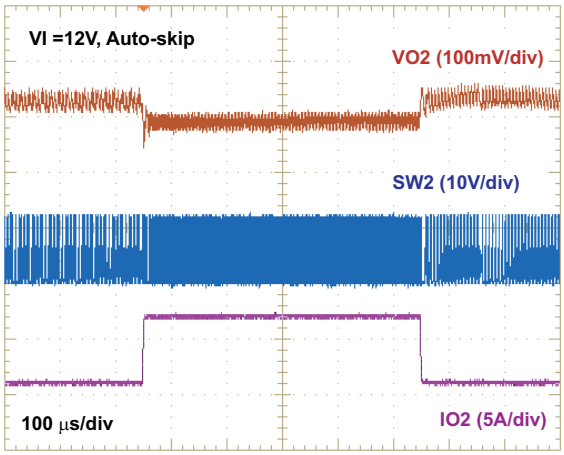


图 39.

DETAILED DESCRIPTION

ENABLE AND SOFT START

When EN is *Low*, the TPS51220A-Q1 is in the shutdown state. Only the 3.3-V LDO stays alive, and consumes 7 µA (typically). When EN becomes *High*, the TPS51220A-Q1 is in the standby state. The 2-V reference and the 5-V LDO become enabled, and consume about 80 µA with no load condition, and are ready to turn on SMPS channels. Each SMPS channel is turned on when ENx becomes *High*. After ENx is set to high, the TPS51220A-Q1 begins the softstart sequence, and ramps up the output voltage from zero to the target voltage in 0.96 ms. However, if a slower soft-start is required, an external capacitor can be tied from the ENx pin to GND. In this case, the TPS51220A-Q1 charges the external capacitor with the integrated 2-µA current source. An approximate external soft-start time would be $t_{EX\text{-}SS} = C_{EX} / I_{EN12}$, which means the time from ENx = 1 V to ENx = 2 V. The recommend capacitance is more than 2.2 nF.

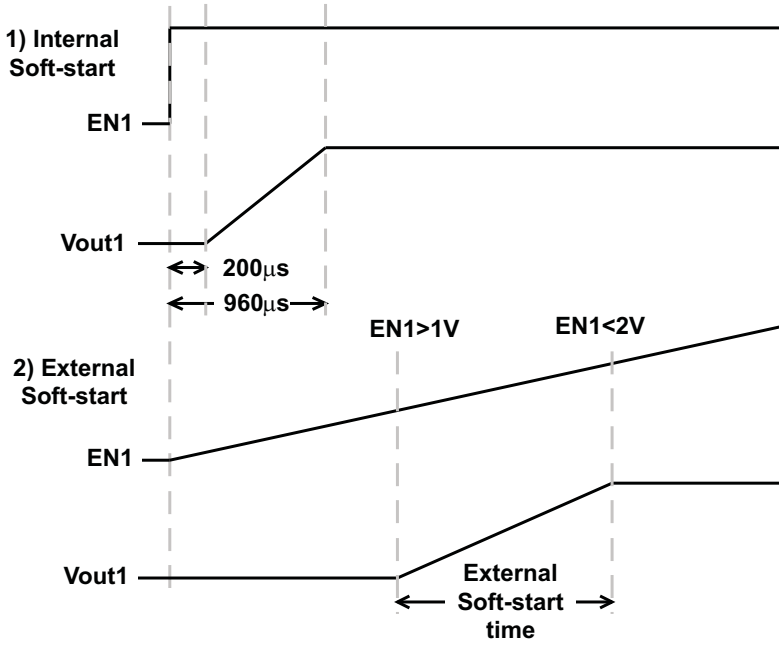


图 40. Enable and Soft-start Timing

表 1. Enable Logic States

EN	EN1	EN2	VREG3	VREF2	VREG5	CH1	CH2
GND	Don't Care	Don't Care	**ON**	Off	Off	Off	Off
Hi	Lo	Lo	**ON**	**ON**	**ON**	Off	Off
Hi	Hi	Lo	**ON**	**ON**	**ON**	**ON**	Off
Hi	Lo	Hi	**ON**	**ON**	**ON**	Off	**ON**
Hi	Hi	Hi	**ON**	**ON**	**ON**	**ON**	**ON**

PRE-BIASED START-UP

The TPS51220A-Q1 supports a pre-biased start up by preventing negative inductor current during soft-start when the output capacitor holds some charge. The initial DRVH signal waits until the voltage feedback signal becomes greater than the internal reference ramping up by the soft-start function. After that, the start-up occurs in the same way the soft-start condition fully discharges, regardless of the SKIPSELx selection.

3.3-V, 10-mA LDO (VREG3)

A 3.3-V, 10-mA, linear regulator is integrated in the TPS51220A-Q1. This LDO services some of the analog circuit in the device and provides a handy standby supply for 3.3-V *Always On* voltage in the notebook system. Apply a 2.2-µF (at least 1-µF), high quality X5R or X7R ceramic capacitor from VREG3 to (signal) GND in adjacent to the device.

2-V, 100-µA Sink/Source Reference (VREF2)

This voltage is used for the reference of the loop compensation network. Apply a 0.22-µF (at least 0.1-µF), high-quality X5R or X7R ceramic capacitor from VREF2 to (signal) GND in adjacent to the device.

5.0-V, 100-mA LDO (VREG5)

A 5.0-V, 100-mA, linear regulator is integrated in the TPS51220A-Q1. This LDO services the main analog supply rail and provides the current for gate drivers until switch-over function becomes enable. Apply a 10-µF (at least 4.7-µF), high-quality X5R or X7R ceramic capacitor from VREG5 to (power) GND in adjacent to the device.

VREG5 SWITCHOVER

When EN1 is high, PGOOD1 indicates *GOOD* and a voltage of more than 4.83 V is applied to V5SW, the internal 5V-LDO is shut off and the VREG5 is shorted to V5SW by an internal MOSFET after an 7.7-ms delay. When the V5SW voltage becomes lower than 4.65 V, EN1 becomes low, or PGOOD1 indicates *BAD*, the internal switch is turned off, and the internal 5V-LDO resumes immediately.

BASIC PWM OPERATIONS

The main control loop of the SMPS is designed as a fixed frequency, pulse width modulation (PWM) controller. It supports two control schemes; a peak current mode and a proprietary D-CAP mode. Current mode achieves stable operation with any type of output capacitors, including low ESR capacitor(s) such as ceramic or specialty polymer capacitors. D-CAP mode does not require an external compensation circuit, and is suitable for relatively larger ESR capacitor(s) configuration. These control schemes are selected with FUNC pin. See 表 4.

CURRENT MODE

The current mode scheme uses the output voltage information and the inductor current information to regulate the output voltage. The output voltage information is sensed by VFBx pin. The signal is compared with the internal 1-V reference and the voltage difference is amplified by a transconductance amplifier (VFB-AMP). The inductor current information is sensed by CSPx and CSNx pins. The voltage difference is amplified by another transconductance amplifier (CS-AMP). The output of the VFB-AMP indicates the target peak inductor current. If the output voltage decreases, the TPS51220A-Q1 increases the target inductor current to raise the output voltage. Alternatively, if the output voltage rises, the TPS51220A-Q1 decreases the target inductor current to reduce the output voltage.

At the beginning of each clock cycle, the high-side MOSFET is turned on, or becomes ‘ON’ state. The high-side MOSFET is turned off, or becomes *OFF* state, after the inductor current becomes the target value which is determined by the combination value of the output of the VFB-AMP and a ramp compensation signal. The ramp compensation signal is used to prevent sub-harmonic oscillation of the inductor current control loop. The high-side MOSFET is turned on again at the next clock cycle. By repeating the operation in this manner, the controller regulates the output voltage. The synchronous low-side or the *rectifying* MOSFET is turned on each *OFF* state to keep the conduction loss minimum.

D-CAP™ MODE

With the D-CAP mode operation, the PWM comparator compares VREF2 with the combination value of the COMP voltage, VFB-AMP output, and the ramp compensation signal. When the both signals are equal at the peak of the voltage sense signal, the comparator provides the *OFF* signal to the high-side MOSFET driver. Because the compensation network is implemented on the part and the output waveform itself is used as the error signal, external circuit is simplified. Another advantage is its inherent fast transient response. A trade-off is a sufficient amount of ESR required in the output capacitor. The D-CAP™ mode is suitable for relatively larger output ripple voltage application. The inductor current information is used for the overcurrent protection and light load operation.

PWM FREQUENCY CONTROL

The TPS51220A-Q1 has a fixed frequency control scheme with 180° phase shift. The switching frequency can be determined by an external resistor which is connected between RF pin and GND, and can be calculated using 公式 1.

$$f_{sw}\left[kHz\right] = \frac{1 \times 10^{5}}{RF\left[k\Omega\right]} \quad (1)$$

TPS51220A-Q1 can also synchronize to more than 2.5 V amplitude external clock by applying the signal to the RF pin. The set timing of channel 1 initiates at the raising edge (1.3 V typ) of the clock and channel 2 initiates at the falling edge (1.1 V typ). Therefore, the 50% duty signal makes both channels 180° phase shift.

When the external clock synchronization is selected, the following conditions are required.

- Remove RF resistor
- Add clock signal before EN1 or EN2 turning on

The TPS51220A-Q1 does NOT support switching frequency change on-the-fly. (neither from the switching frequency set by the RF resistor to the external clock, nor vice versa)

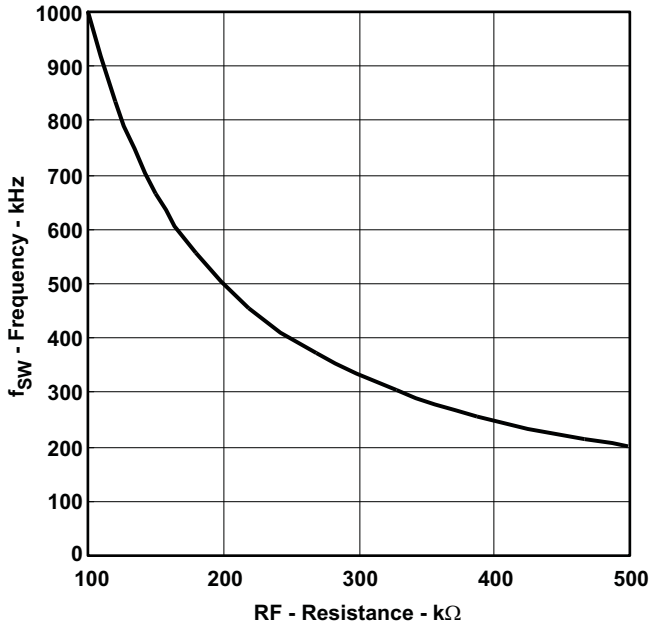


图 41. Switching Frequency vs RF

180 Degrees Phase Shift and Blanking Time

The two channels of the SMPS operate 180 degrees phase shift. This scheme helps in reducing the input RMS current. As a result, the device provides the benefits of saving the number and power loss of the input bulk capacitors. To minimize interaction between the two channels caused by switching noise, blanking time is implemented. The loop comparator output is masked during the blanking time to avoid false turning off the channel.

There are two cases where the inter-channel communication can take place:

1. One channel's switching node falling edge is close to another channel's switching node rising edge.
2. One channel's switching node falling edge is close to another channel's switching node falling edge.

In both cases, the TPS51220A-Q1 shows jitter inherent to the blanking time. Since the device is a fixed frequency controller, the rising edge of the switching node is settled at the clock cycle. Consequently, jitter is observed at a period of switching node falling edge. This jitter does not represent small signal instability. In fact,

jittering is a normal action of control loop against timing deviation caused by any accidental event such as noise, or the blanking time, adjusting back to the regulation point. A small amount of jittering does not harm the voltage regulation. However; if the user wants a further reduction of jitter, using the external clock synchronization provides adjustable phase shift between channels to avoid overlapping of switching events. See the *PWM Frequency Control* section.

LIGHT LOAD OPERATION

The TPS51220A-Q1 automatically reduces switching frequency at light load conditions to maintain high efficiency if *Auto Skip* or *Out-of-Audio™* mode is selected by SKIPSELx. This reduction of frequency is achieved by skipping pulses. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its *peak* reaches a predetermined current, $I_{LL(PEAK)}$, which indicates the boundary between heavy-load and light-load conditions. Once the top MOSFET is turned on, the TPS51220A-Q1 does not allow it to be turned off until it reaches $I_{LL(PEAK)}$. This eventually causes an overvoltage condition to the output and pulse skipping. From the next pulse after zero-crossing is detected, $I_{LL(PEAK)}$ is limited by the ramp-down signal $I_{LL(PEAK)RAMP}$, which starts from 25% of the overcurrent limit setting ($I_{OCL(PEAK)}$: (see the *Current Protection* section) toward 5% of $I_{OCL(PEAK)}$ over one switching cycle to prevent causing large ripple. The transition load point to the light load operation $I_{LL(DC)}$ can be calculated in 公式 2.

$$I_{LL(DC)} = I_{LL(PEAK)} - 0.5 \times I_{IND(RIPPLE)} \quad (2)$$

$$I_{IND(RIPPLE)} = \frac{1}{L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- f_{SW} is the PWM switching frequency which is determined by RF resistor setting or external clock (3)

$$I_{LL(PEAK)RAMP} = (0.2 - 0.13 \times t \times f_{SW}) \times I_{OCL(PEAK)} \quad (4)$$

Switching frequency versus output current in the light load condition is a function of L, f, V_{IN} and V_{OUT}, but it decreases almost proportionally to the output current from the $I_{LL(DC)}$, as described in 公式 2; while maintaining the switching synchronization with the clock. Due to the synchronization, the switching waveform in boundary load condition (close to $I_{LL(DC)}$) appears as a sub-harmonic oscillation; however, it is the intended operation.

If SKIPSELx is tied to GND, the TPS51220A-Q1 works on a constant frequency of f_{SW} regardless its load current.

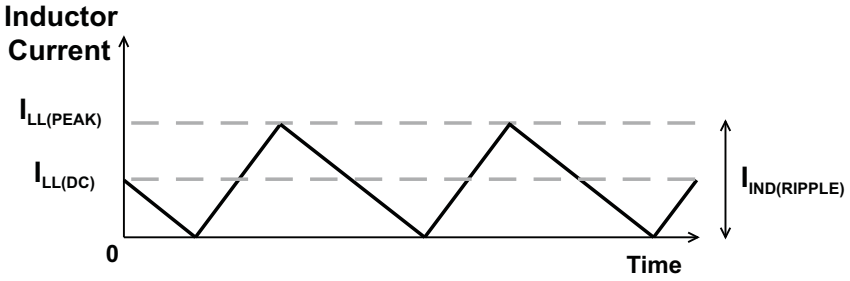


图 42. Boundary Between Pulse Skipping and CCM

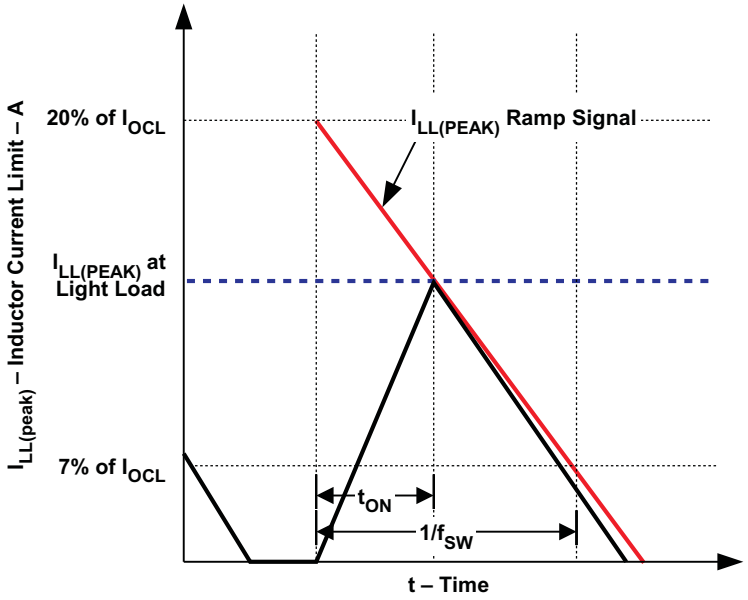


图 43. Inductor Current Limit at Pulse Skipping

表 2. Skip Mode Selection

SKIPSELx	GND	VREF2	VREG3	VREG5
OPERATING MODE	Continuous Conduction	Auto Skip	OOA Skip (maximum 7 skips, for <400 kHz)	OOA Skip (maximum 15 skips, for equal to or greater than 400kHz)

OUT OF AUDIO SKIP OPERATION

Out-Of-Audio™ (OOA) light-load mode is a unique control feature that keeps the switching frequency above acoustic audible frequencies toward virtually no load condition while maintaining state-of-the-art high conversion efficiency. When OOA is selected, the switching frequency is kept higher than audible frequency range in any load condition. The TPS51220A-Q1 automatically reduced switching frequency at light-load conditions. The OOA control circuit monitors the states of both MOSFETs and forces an *ON* state if the predetermined number of pulses are skipped. The high-side MOSFET is turned on before the output voltage declines down to the target value, so that eventually an overvoltage condition is caused. The OOA control circuit detects this overvoltage condition and begins modulating the skip-mode on time to keep the output voltage.

The TPS51220A-Q1 supports a wide-switching frequency range, therefore, the OOA skip mode has two selections. See 表 2. When the 300-kHz switching frequency is selected, a maximum of seven (7) skips (SKIPSEL=3.3 V) makes the lowest frequency at 37.5 kHz. If a 15-skip maximum is chosen, it becomes 18.8 kHz, hence the maximum 7 skip is suitable for less than 400 kHz, and the maximum 15 skip is 400 kHz or greater.

99% DUTY CYCLE OPERATION

In a low-dropout condition such as 5-V input to 5-V output, the basic control loop attempts to maintain 100% of the high-side MOSFET *ON*. However, with the N-channel MOSFET used for the top switch, it is not possible to use the 100% on-cycle to charge the boot strap capacitor. When high duty is required, the TPS51220A-Q1 extends the ON period (by skipping a maximum of three clock cycles and reducing the switching frequency to 25% of the steady state value) and asserts the OFF state after extended ON.

HIGH-SIDE DRIVER

The high-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance, which is 1.7Ω for VBSTx to DRVHx, and 1Ω for DRVHx to SWx. When configured as a floating driver, 5 V of bias voltage is delivered from VREG5 supply. The instantaneous drive current is supplied by the flying capacitor between VBSTx and SWx pins. The average drive current is equal to the gate charge at Vgs = 5V times switching frequency. This gate drive current as well as the low-side gate drive current times 5 V makes the driving power which needs to be dissipated mainly from TPS51220A-Q1 package. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on.

LOW-SIDE DRIVER

The low-side driver is designed to drive high-current low-$R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance, which are 1.3Ω for VREG5 to DRVLx and 0.7Ω for DRVLx to GND. The 5-V bias voltage is delivered from VREG5 supply. The instantaneous drive current is supplied by an input capacitor connected between VREG5 and GND. The average drive current is also calculated by the gate charge at Vgs = 5 V times switching frequency.

CURRENT SENSING SCHEME

In order to provide both good accuracy and cost effective solution, the TPS51220A-Q1 supports external resistor sensing and inductor DCR sensing. An RC network with high quality X5R or X7R ceramic capacitor should be used to extract voltage drop across DCR. 0.1µF is a good value to start the design. CSPx and CSNx should be connected to positive and negative terminal of the sensing device respectively. TPS51220A-Q1 has an internal current amplifier. The gain of the current amplifier, *Gc*, is selected by TRIP terminal. In any setting, the output signal of the current amplifier becomes 100mV at the OCL setting point. This means that the current sensing amplifier normalize the current information signal based on the OCL setting. Attaching a RC network recommended even with a resistor sensing scheme to get an accurate current sensing; see the external parts selection session for detailed configurations.

ADAPTIVE ZERO CROSSING

TPS51220A-Q1 has an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the ZC comparator and delay time of the ZC detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

CURRENT PROTECTION

TPS51220A-Q1 has cycle-by-cycle overcurrent limiting control. If the inductor current becomes larger than the overcurrent trip level, TPS51220A-Q1 turns off high-side MOSFET, turns on low-side MOSFET and waits for the next clock cycle.

$I_{OCL(PEAK)}$ sets peak level of the inductor current. Thus, the dc load current at overcurrent threshold, $I_{OCL(DC)}$, can be calculated as follows;

$$I_{OCL(DC)} = I_{OCL(PEAK)} - 0.5 \times I_{IND(RIPPLE)} \quad (5)$$

$$I_{OCL(PEAK)} = \frac{V_{OCL}}{R_{SENSE}}$$

where

- R_{SENSE} is resistance of current sensing device
- $V_{(OCL)}$ is the overcurrent trip threshold voltage which is determined by TRIP pin voltages as shown in 表 3 (6)

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down, and it ultimately crosses the undervoltage protection threshold and shutdown.

表 3. OCL Trip and Discharge Selection

TRIP	GND	VREF2	VREG3	VREG5
$V_{(OCL)}$ (OCL TRIP VOLTAGE)	$V_{(OCL-ULV)}$ (ULTRA-LOW VOLTAGE)		$V_{(OCL-LV)}$ (LOW VOLTAGE)	
DISCHARGE	Enable	Disable	Disable	Enable

POWERGOOD

The TPS51220A-Q1 has powergood output for both switcher channels. The powergood function is activated after softstart has finished. If the output voltage becomes within ±5% of the target value, internal comparators detect power good state and the powergood signal becomes high after 1ms internal delay. If the output voltage goes outside of ±10% of the target value, the powergood signal becomes low after 1.5µs internal delay. Apply voltage should be less than 6V and the recommended pull-up resistance value is from 100kΩ to 1MΩ.

OUTPUT DISCHARGE CONTROL

The TPS51220A-Q1 discharges output when ENx is low. The TPS51220A-Q1 discharges outputs using an internal MOSFET which is connected to CSNx and GND. The current capability of these MOSFETs is limited to discharge the output capacitor slowly. If ENx becomes high during discharge, MOSFETs are turning off, and some output voltage remains. SMPS changes over to soft-start. The PWM initiates after the target voltage overtakes the remaining output voltage. This function can be disabled as shown in 表 3.

OVERVOLTAGE/UNDERVOLTAGE PROTECTION

TPS51220A-Q1 monitors the output voltage to detect overvoltage and undervoltage. When the output voltage becomes 15% higher than the target value, the OVP comparator output goes high and the circuit latches as the high-side MOSFET driver OFF and the low-side MOSFET driver ON, and shuts off another channel.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, TPS51220A-Q1 latches OFF both high-side and low-side MOSFETs, and shuts off another channel. This UVP function is enabled after soft-start has completed. OVP function can be disabled as shown in 表 4. The procedures for restarting from these protection states are:

1. toggle EN
2. toggle EN1 and EN2 or
3. once hit UVLO

表 4. FUNC Logic States

FUNC	GND	VREF2	VREG3	VREG5
OVP	Enable	Disable	Enable	Disable
CONTROL SCHEME	Current mode	D-CAP mode	D-CAP mode	Current mode

UVLO PROTECTION

The TPS51220A-Q1 has undervoltage lockout protections (UVLO) for VREG5, VREG3 and VREF2. When the voltage is lower than UVLO threshold voltage, TPS51220A-Q1 shuts off each output as shown in表 5. This is non-latch protection.

表 5. UVLO Protection

	CH1/ CH2	VREG5	VREG3	VREF2
VREG5 UVLO	Off	—	On	On
VREG3 UVLO	Off	Off	—	Off
VREF2 UVLO	Off	Off	On	—

THERMAL SHUTDOWN

The TPS51220A-Q1 monitors the device temperature. If the temperature exceeds the threshold value, TPS51220A-Q1 shuts off both SMPS and 5V-LDO, and decreases the VREG3 current limitation to 5 mA (typically). This is non-latch protection.

APPLICATION INFORMATION

EXTERNAL PARTS SELECTION

A buck converter using the TPS51220A-Q1 consists of linear circuits and a switching modulator. 图 44 and 图 45 show basic scheme.

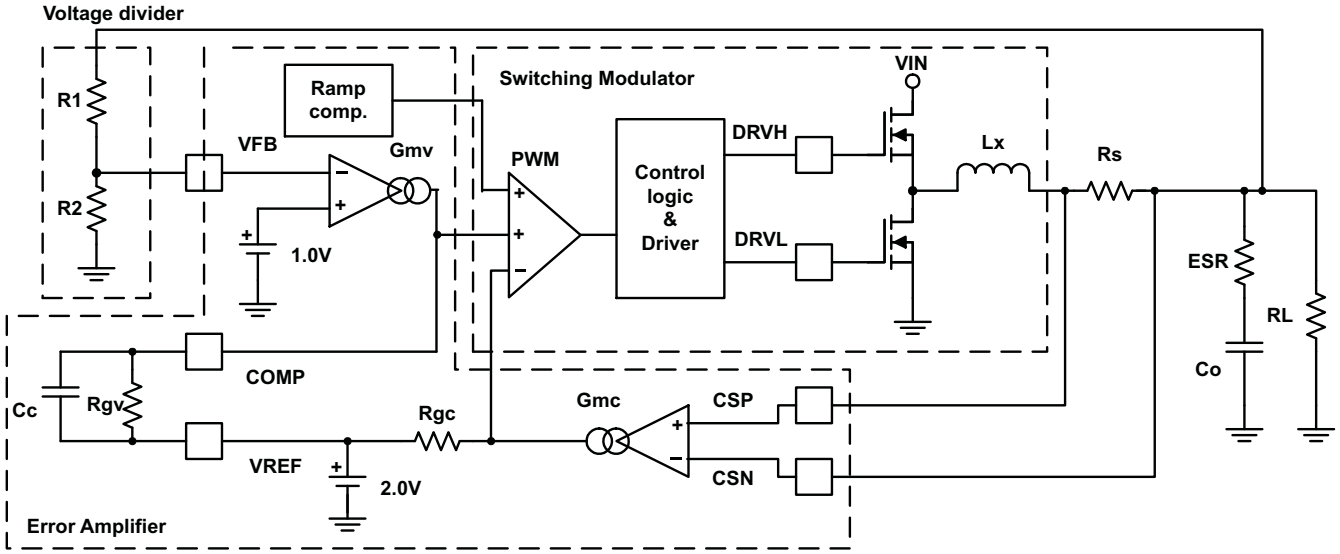


图 44. Simplified Current Mode Functional Blocks

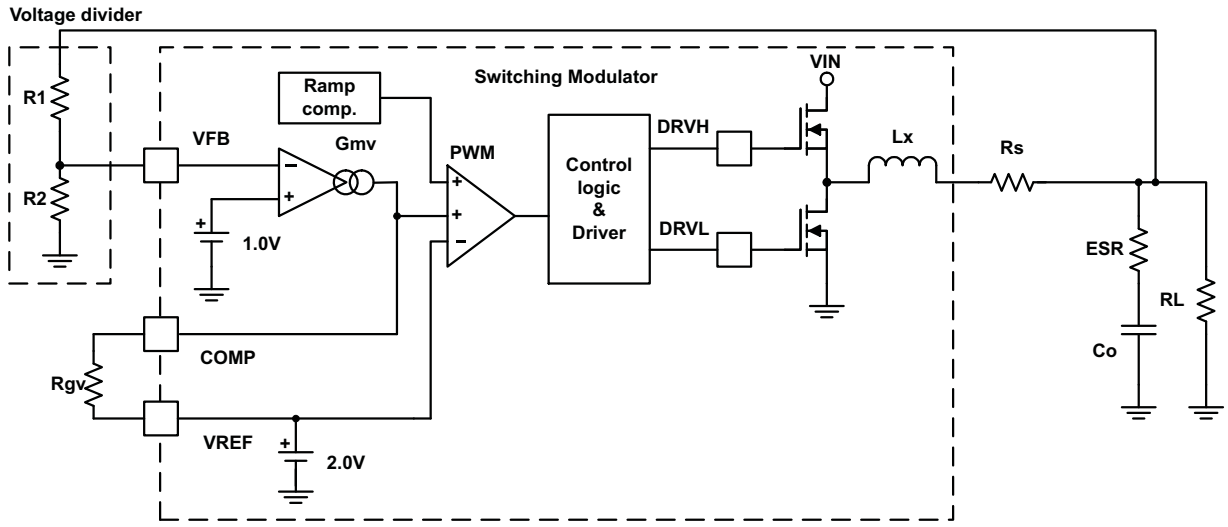


图 45. Simplified D-CAP Mode Functional Blocks

The external components can be selected by following manner.

1. **Determine output voltage dividing resistors.** (R1 and R2: shown in 图 44) using 公式 7 .

$$R1 = \left(V_{OUT} - 1.0\right) \times R2 \quad (7)$$

For D-CAP mode, recommended R2 value is from 10kΩ to 20kΩ.

2. **Determine switching frequency.** Higher frequency allows smaller output capacitances, however, degrade efficiency due to increase of switching loss. Frequency setting resistor for RF-pin can be calculated by;

$$RF[k\Omega] = \frac{1 \times 10^5}{f_{sw}\,[kHz]} \quad (8)$$

3. **Choose the inductor.** The inductance value should be determined to give the ripple current of approximately 25% to 50% of maximum output current. Recommended ripple current rate is about 30% to 40% at the typical input voltage condition, next equation uses 33%.

$$L = \frac{1}{0.33 \times I_{OUT(MAX)} \times f_{SW}} \times \frac{(V_{IN(TYP)} - V_{OUT}) \times V_{OUT}}{V_{IN(TYP)}} \quad (9)$$

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

4. Determine the OCL trip voltage threshold, $V_{(OCL)}$, and select the sensing resistor.

The OCL trip voltage threshold is determined by TRIP pin setting. To use a larger value improves the S/N ratio. Determine the sensing resistor using next equation. $I_{OCL(PEAK)}$ should be approximately 1.5 × $I_{OUT(MAX)}$ to 1.7 × $I_{OUT(MAX)}$.

$$R_{SENSE} = \frac{V_{OCL}}{I_{OCL(PEAK)}} \quad (10)$$

5. **Determine Rgv.** Rgv should be determined from preferable droop compensation value and is given by next equation based on the typical number of Gmv = 500µS.

$$Rgv = 0.1 \times \frac{I_{OUT(MAX)}}{I_{OCL(PEAK)}} \times V_{OUT} \times \frac{1}{Gmv \times Vdroop} \quad (11)$$

$$Rgv[k\Omega] = 200 \times \frac{I_{OUT(MAX)}}{I_{OCL(PEAK)}} \times \frac{V_{OUT}[V]}{Vdroop[mV]} \quad (12)$$

If no-droop is preferred, attach a series RC network circuit instead of single resistor. Series resistance is determined using 公式 12 . Series capacitance can be arbitrarily chosen to meet the RC time constant, but should be kept under 1/10 of f_o. For D-CAP mode, Rgv is used for adjusting ramp compensation. 10kΩ is a good value to start design with. 6kΩ to 20kΩ can be chosen.

6. Determine output capacitance *Co* to achieve a stable operation using the next equation. The 0 dB frequency, f_o, should be kept under 1/3 of the switching frequency.

$$f_0 = \frac{5}{\pi} \times I_{OCL(PEAK)} \times \frac{1}{V_{OUT}} \times \frac{Gmv \times Rgv}{Co} < \frac{fsw}{3} \quad (13)$$

$$Co > \frac{15}{\pi} \times I_{OCL(PEAK)} \times \frac{1}{V_{OUT}} \times \frac{Gmv \times Rgv}{fsw} \quad (14)$$

For D-CAP mode, f_o is determined by the output capacitor's characteristics as below.

$$f_0 = \frac{1}{2\pi \times ESR \times Co} < \frac{fsw}{3} \quad (15)$$

$$Co > \frac{3}{2\pi \times ESR \times fsw} \quad (16)$$

For better jitter performance, a sufficient amount of feedback signal is required at VFBx pin. The recommended signal level is approximately 30mV per t_{sw} (switching period) of the ramping up rate, and more than 4 mV of peak-to-peak voltage.

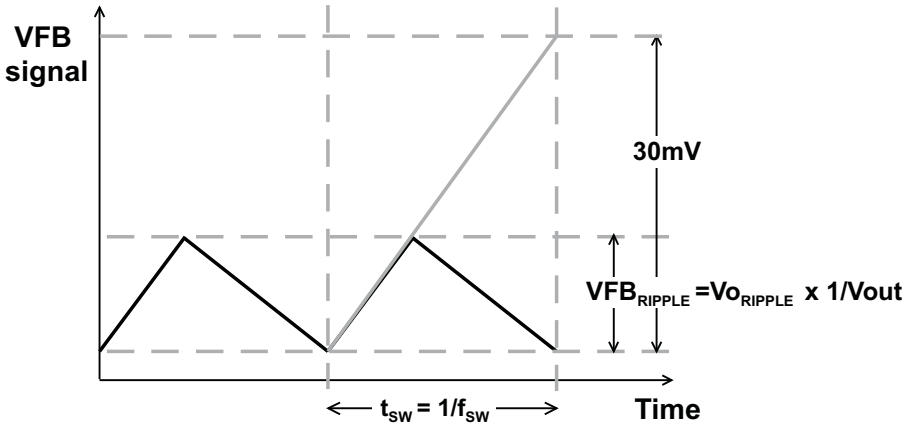


图 46. Required voltage feedback ramp signal

7. **Calculate Cc.** The purpose of this capacitance is to cancel zero caused by *ESR* of the output capacitor. If ceramic capacitor(s) is used, there is no need for Cc. If a combination of different capacitors is used, attach a RC network circuit instead of single capacitance to cancel zeros and poles caused by the output capacitors. With single capacitance, Cc is given in 公式 17.

$$Cc = Co \times \frac{ESR}{Rgv} \tag{17}$$

For D-CAP mode, basically Cc is not needed.

8. **Choose MOSFETs** Generally, the on resistance affects efficiency at high load conditions as conduction loss. For a low output voltage application, the duty ratio is not high enough so that the on resistance of high-side MOSFET does not affect efficiency; however, switching speed (t_r and t_f) affects efficiency as switching loss. As for low-side MOSFET, the switching loss is usually not a main portion of the total loss.

RESISTOR CURRENT SENSING

For more accurate current sensing with an external resistor, the following technique is recommended. Adding an RC filter to cancel the parasitic inductance of resistor, this filter value is calculated using 公式 18.

$$Cx \times Rx = \frac{Lx}{Rs} \tag{18}$$

This equation means time-constant of Cx and Rx should match the one of Lx (ESL) and Rs.

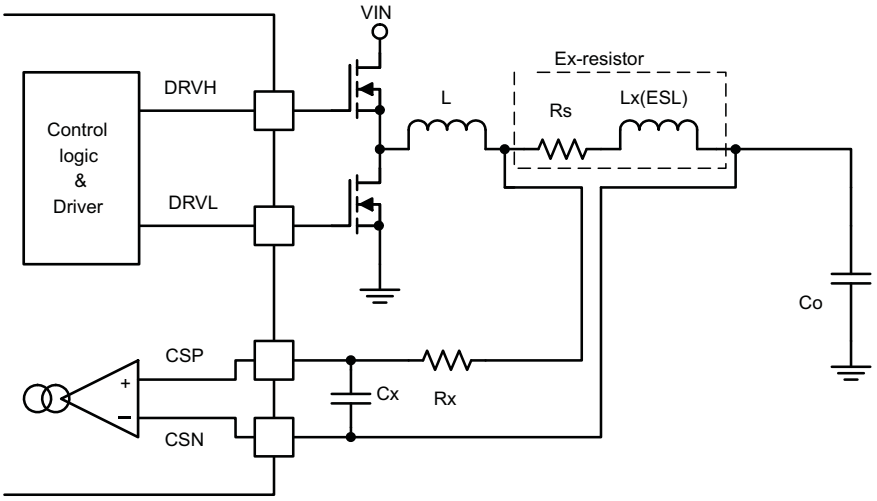


图 47. External Resistor Current Sensing

INDUCTOR DCR CURRENT SENSING

To use inductor DCR as current sensing resistor (Rs), the configuration needs to change as below. However, the equation that must be satisfied is the same as the one for the resistor sensing.

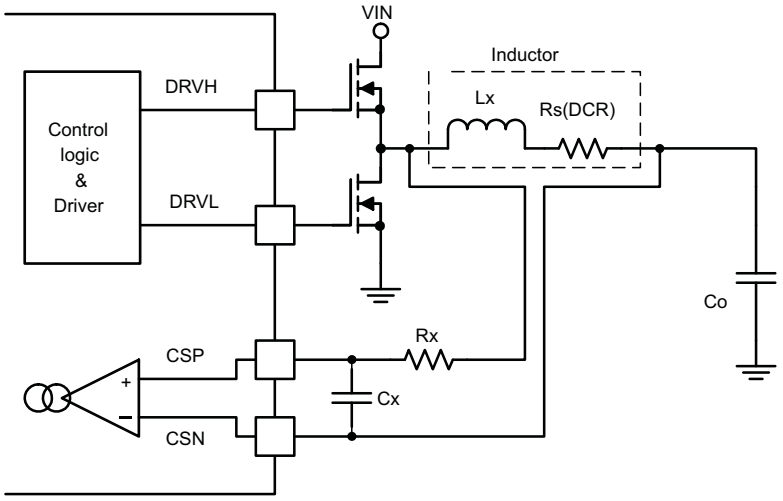


图 48. Inductor DCR Current Sensing

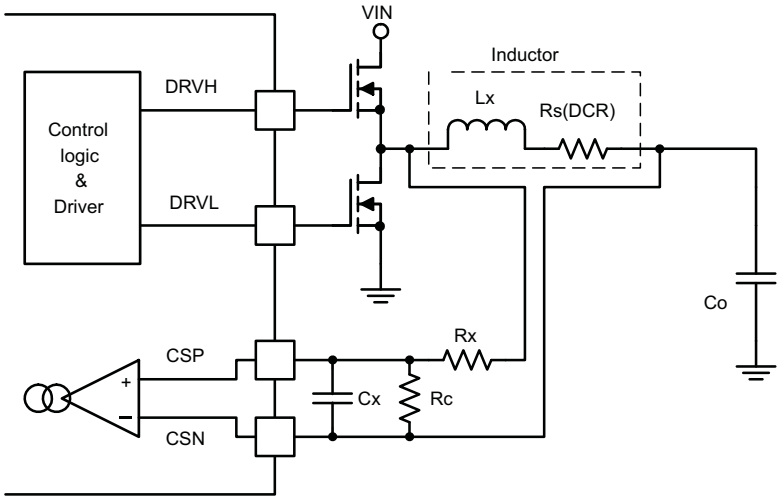


图 49. Inductor DCR Current Sensing With Voltage Divider

TPS51220A-Q1 has fixed $V_{(OCL)}$ point (60 mV or 31 mV). In order to adjust for DCR, a voltage divider can be configured a described in 图 49.

For Rx, Rc and Cx can be calculated as shown below, and overcurrent limitation value can be calculated as follows:

$$Cx \times (Rx // Rc) = \frac{Lx}{Rs} \tag{19}$$

$$I_{OCL(PEAK)} = V_{OCL} \times \frac{1}{Rs} \times \frac{Rx + Rc}{Rc} \tag{20}$$

图 50 shows the compensation technique for the temperature drifts of the inductor DCR value. This scheme assumes the temperature rise at the thermistor (R_{NTC}) is directly proportional to the temperature rise at the inductor.

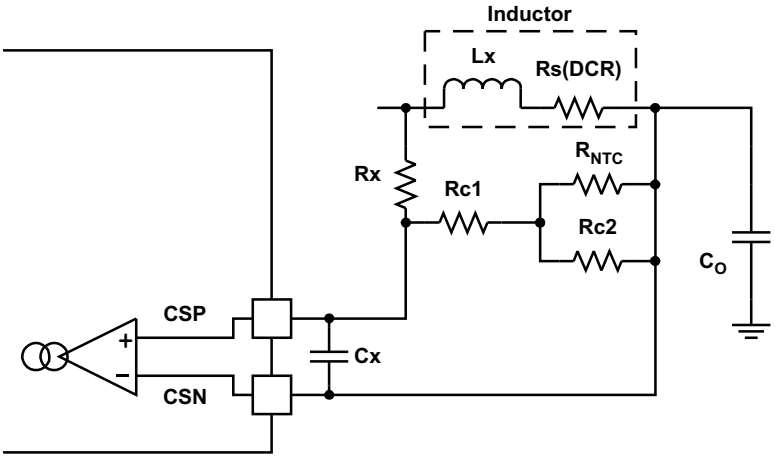


图 50. Inductor DCR Current Sensing With Temperature Compensate

LAYOUT CONSIDERATIONS

Certain points must be considered before starting a PCB layout work using the TPS51220A-Q1.

Placement

- Place RC network for CSP1 and CSP2 close to the device pins.
- Place bypass capacitors for VREG5, VREG3 and VREF2 close to the device pins.
- Place frequency-setting resistor close to the device pin.
- Place the compensation circuits for COMP1 and COMP2 close to the device pins.
- Place the voltage setting resistors close to the device pins, especially when D-CAP mode is chosen.

Routing (sensitive analog portion)

- Use separate traces for; see 图 51
  - Output voltage sensing from current sensing (negative-side)
  - Output voltage sensing from V5SW input (when V_{OUT} = 5V)
  - Current sensing (positive-side) from switch-node

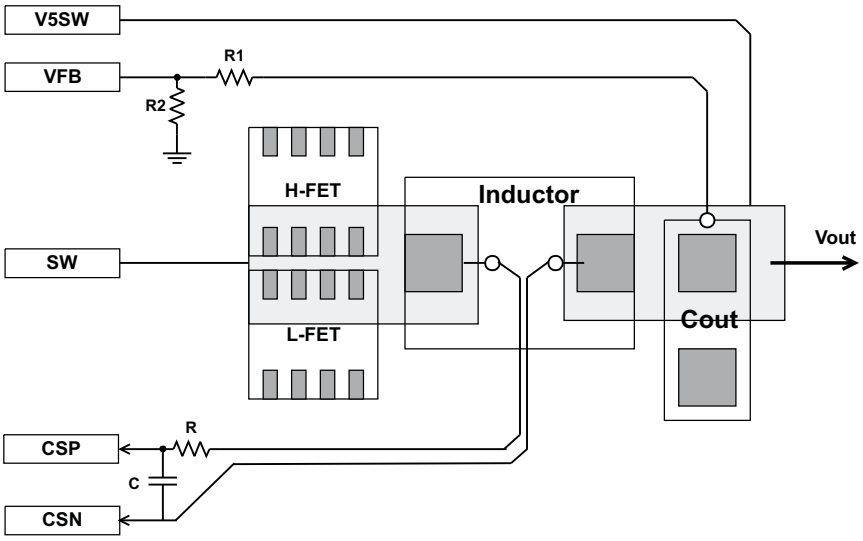


图 51. Sensing Trace Routings

- Use Kelvin sensing traces from the solder pads of the current sensing device (inductor or resistor) to current

sensing comparator inputs (CSPx and CSNx). (See 图 52)

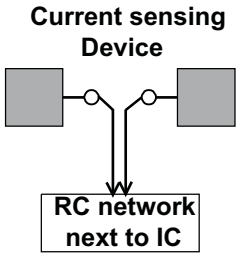


图 52. Current Sensing Traces

- Use small copper space for VFBx. These are short and narrow traces to avoid noise coupling
- Connect VFB resistor trace to the positive node of the output capacitor.
- Use signal GND for VREF2 and VREG3 capacitors, RF and VFB resistors, and the other sensitive analog components. Placing a signal GND plane (underneath the IC, and fully covered peripheral components) on the internal layer for shielding purpose is recommended. (See 图 53)
- Use a thermal land for PowerPAD™. Five or more vias, with 0.33-mm (13-mils) diameter connected from the thermal land to the internal GND plane, should be used to help dissipation. Do NOT connect the GND-pin to this thermal land on the surface layer, underneath the package.

Routing (power portion)

- Use wider/shorter traces of DRVL for low-side gate drivers to reduce stray inductance.
- Use the parallel traces of SW and DRVH for high-side MOSFET gate drive, and keep them away from DRVL.
- Connect SW trace to source terminal of the high-side MOSFET.
- Use power GND for VREG5, VIN and V_{OUT} capacitors and low-side MOSFETs. Power GND and signal GND should be connected near the device GND terminal. (See 图 53)

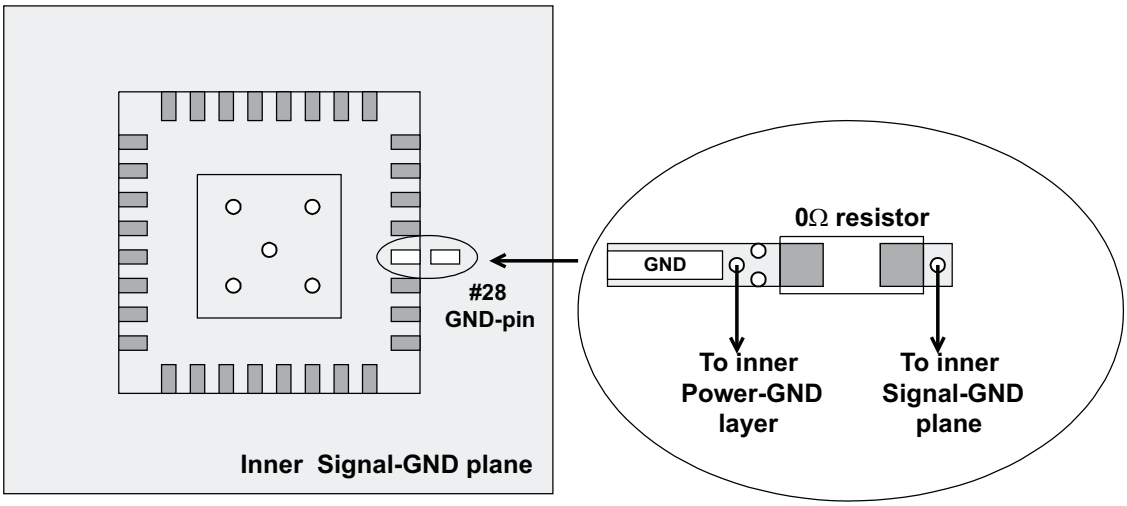


图 53. GND Layout Example

APPLICATION CIRCUITS

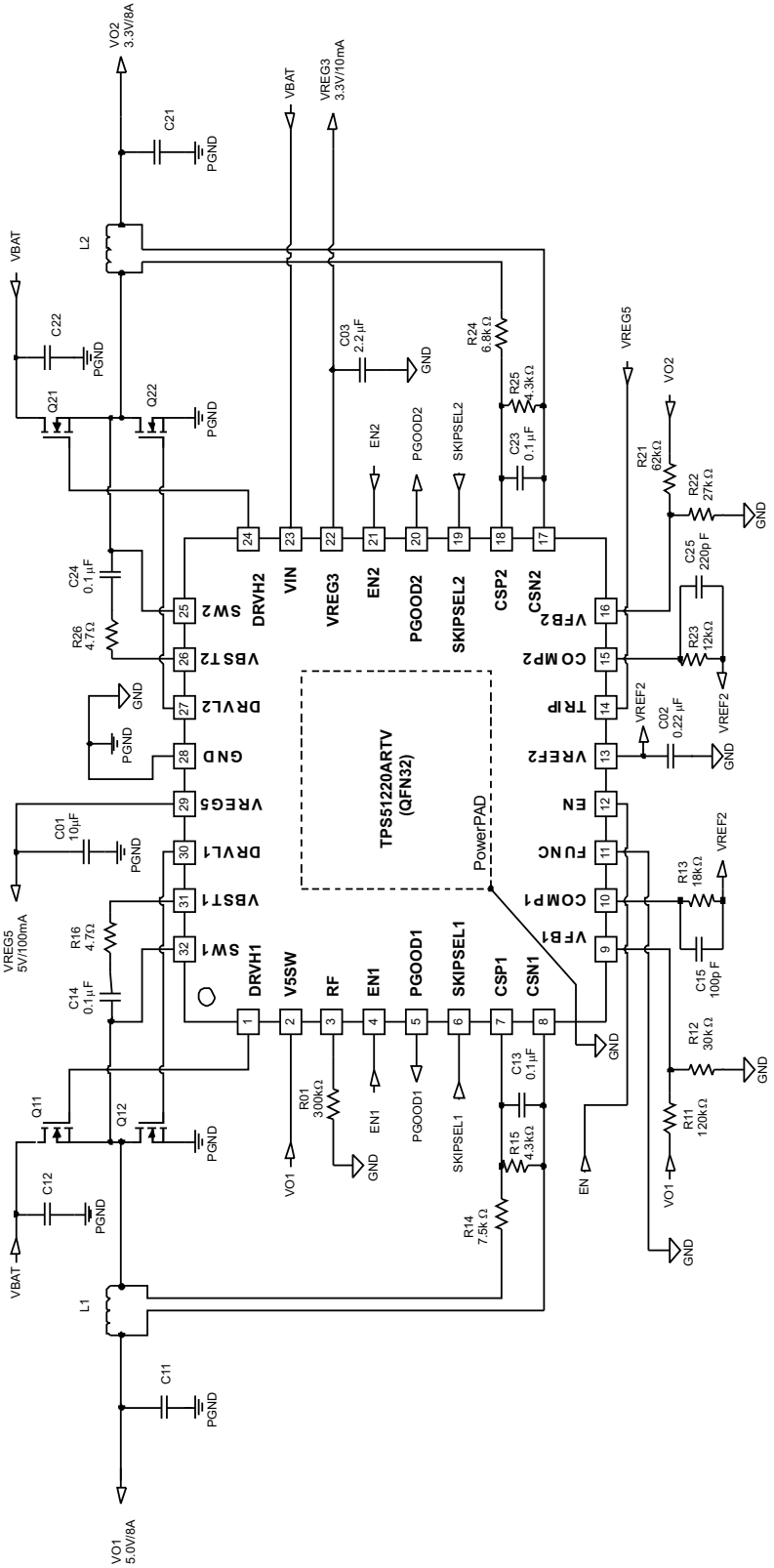


图 54. Current Mode, DCR Sensing, 5-V/8-A, 3.3-V/8-A, 330-kHz

表 6. Current Mode, DCR Sensing, 5-V/8-A, 3.3-V/8-A, 330-kHz

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C11	2 × 330 µF, 6.3 V, 18 mΩ	Sanyo	6TPE330MIL
C12	2 × 10 µF, 25 V	Murata	GRM32DR71E106K
C21	470 µF, 4.0V, 15 mΩ	Sanyo	4TPE470MFL
C22	2 × 10 µF, 25 V	Murata	GRM32DR71E106K
L1	3.3 µH, 10.7 A, 10.5 mΩ	TOKO	FDV1040-3R3M
L2	3.3 µH, 10.7 A, 10.5 mΩ	TOKO	FDV1040-3R3M
Q11, Q21	30-V, 12 A, 10.5 mΩ	Fairchild	FDMS8692
Q12, Q22	30 V, 18 A, 5.4 mΩ	Fairchild	FDMS8672AS

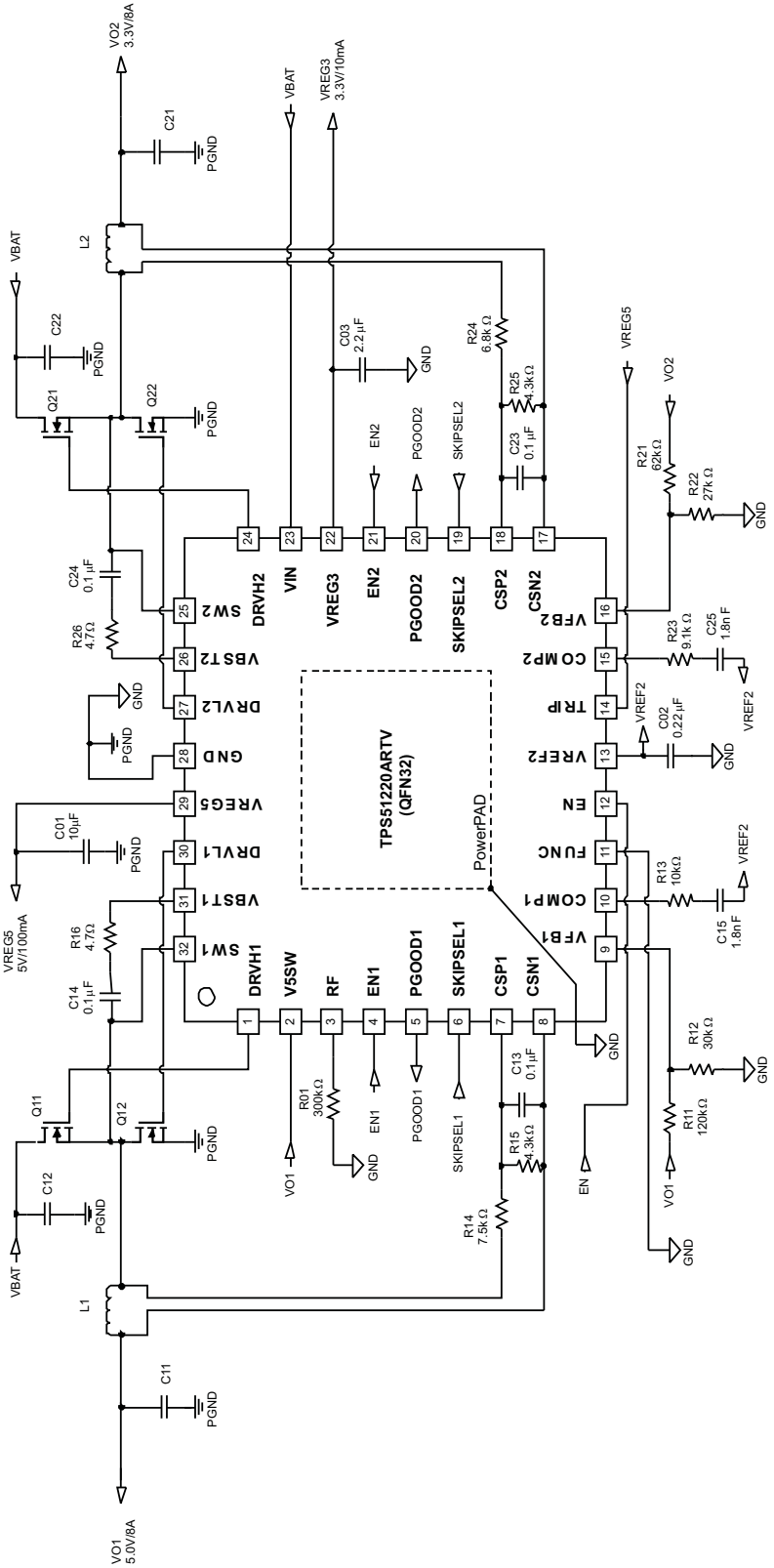


图 55. Current Mode (Non-Droop), DCR Sensing, 5-V/8-A, 3.3-V/8-A, 330-kHz

表 7. Current Mode (Non-droop), DCR Sensing, 5-V/8-A, 3.3-V/8-A, 330-kHz

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C11	2 x 330 µF, 6.3 V 18 mΩ	Sanyo	6TPE330MIL
C12	2 x 10 µF, 25 V	Murata	GRM32DR71E106K
C21	470 µF, 4.0V, 15 mΩ	Sanyo	4TPE470MFL
C22	2 x 10 µF, 25 V	Murata	GRM32DR71E106K
L1	3.3 µH, 10.7 A, 10.5 mΩ	TOKO	FDV1040-3R3M
L2	3.3 µH, 10.7 A, 10.5 mΩ	TOKO	FDV1040-3R3M
Q11, Q21	30-V, 12-A, 10.5 mΩ	Fairchild	FDMS8692
Q12, Q22	30-V, 18-A, 5.4 mΩ	Fairchild	FDMS8672AS

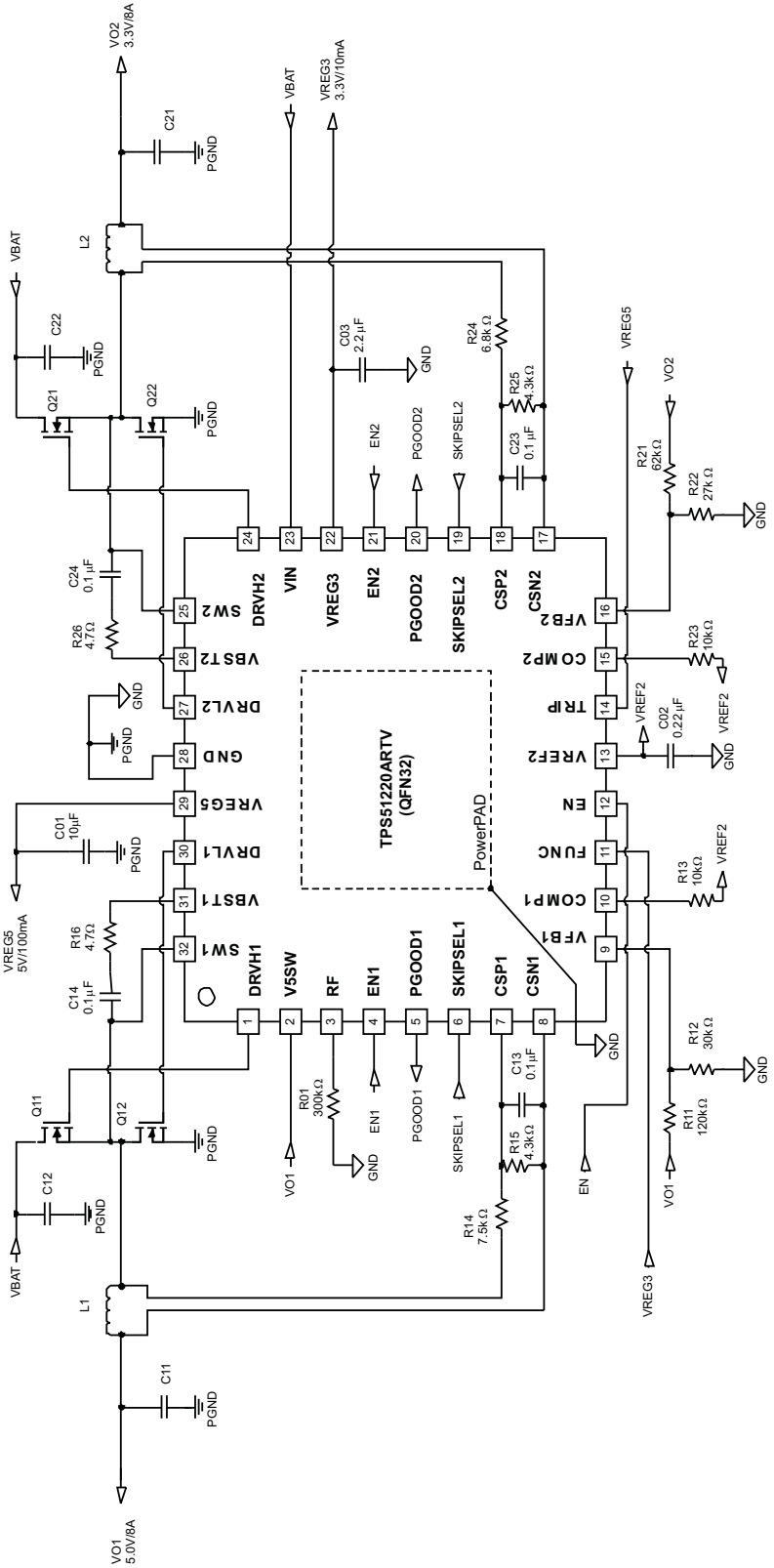


图 56. D-CAP Mode, DCR Sensing, 5-V/8-A, 3.3-V/8-A, 330-kHz

表 8. D-CAP Mode, DCR Sensing, 5-V/ 8-A, 3.3-V/8-A, 330-kHz

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C11	2 x 330 µF, 6.3 V, 18 mΩ	Sanyo	6TPE330MIL
C12	2 x 10 µF, 25 V	Murata	GRM32DR71E106K
C21	470 µF, 4.0V, 15 mΩ	Sanyo	4TPE470MFL
C22	2 x 10 µF, 25 V	Murata	GRM32DR71E106K
L1	3.3 µH, 10.7 A, 10.5 mΩ	TOKO	FDV1040-3R3M
L2	3.3 µH, 10.7 A, 10.5 mΩ	TOKO	FDV1040-3R3M
Q11, Q21	30 V, 12 A, 10.5 mΩ	Fairchild	FDMS8692
Q12, Q22	30 V, 18 A, 5.4 mΩ	Fairchild	FDMS8672AS

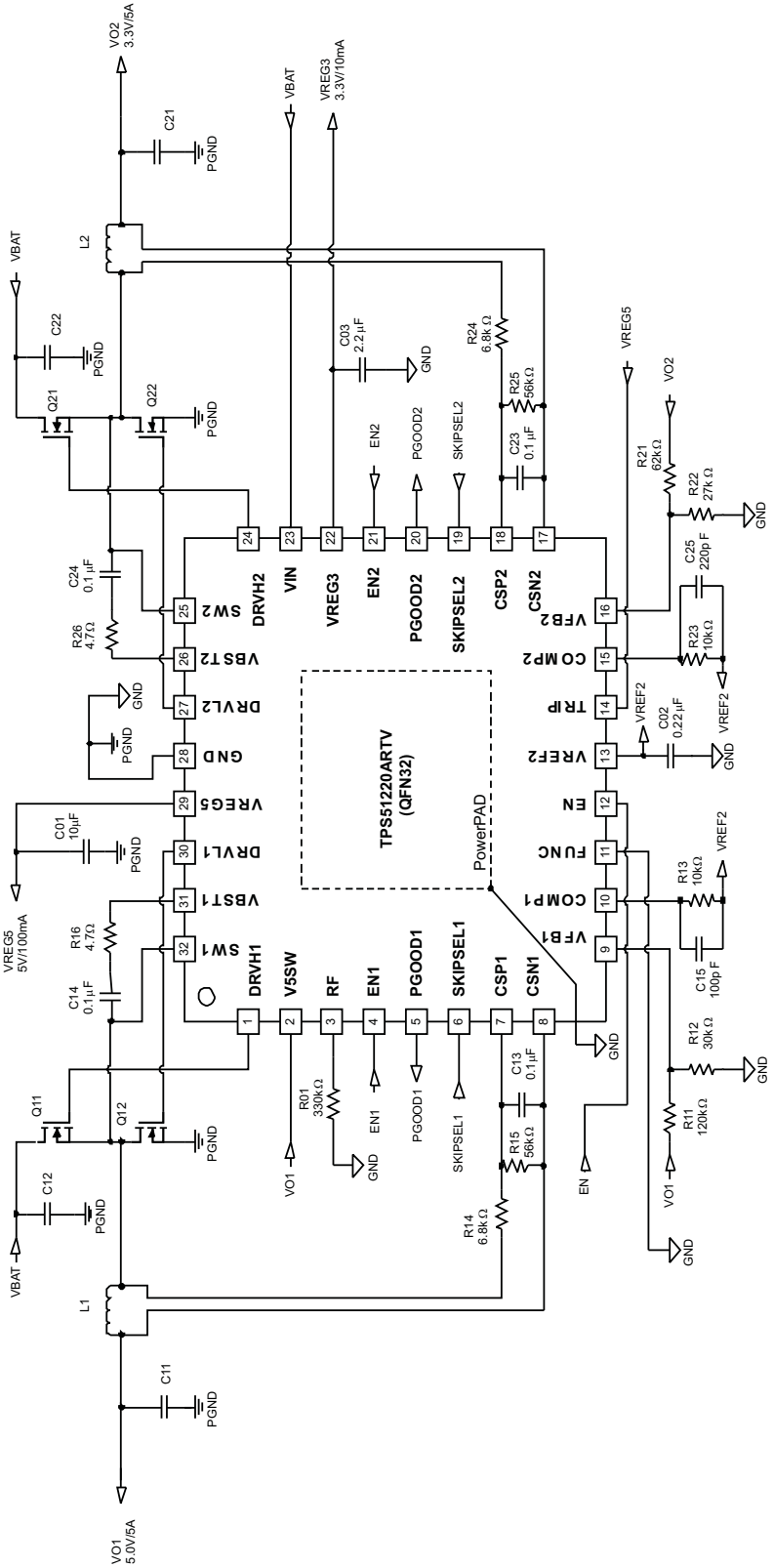


图 57. Current Mode, DCR Sensing, 5-V/5-A, 3.3-V/5-A, 300-kHz

表 9. Current Mode, DCR Sensing, 5-V/5-A, 3.3-V/5-A, 300-kHz

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C11	2 × 120 µF, 6.3V, 15 mΩ	Panasonic	EEFCX0J121R
C12	2 × 10 µF, 25 V	Murata	GRM32DR71E106K
C21	2 × 220 µF, 4.0 V, 15 mΩ	Panasonic	EEFCX0G221R
C22	2 × 10 µF, 25 V	Murata	GRM32DR71E106K
L1	4.0 µH, 10.3 A, 6.6 mΩ	Sumida	CEP125-4R0MC-H
L2	4.0 µH, 10.3 A, 6.6 mΩ	Sumida	CEP125-4R0MC-H
Q11, Q21	30 V, 13.6 A, 9.5 mΩ	IR	IRF7821
Q12, Q22	30 V, 13.8 A, 5.8 mΩ	IR	IRF8113

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS51220ATRTVRQ1	Active	Production	WQFN (RTV) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 51220AT
TPS51220ATRTVRQ1.B	Active	Production	WQFN (RTV) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 51220AT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

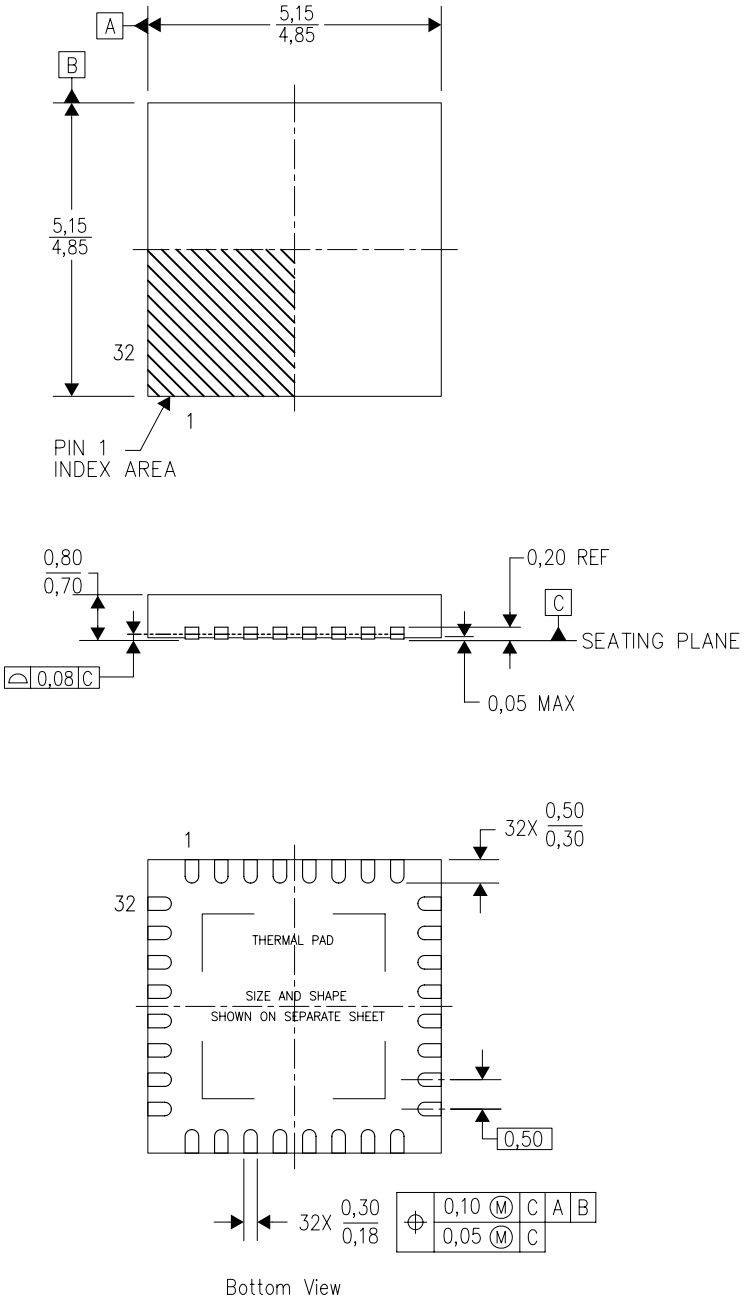
OTHER QUALIFIED VERSIONS OF TPS51220A-Q1 :

- Catalog : TPS51220A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4206245/C 10/11

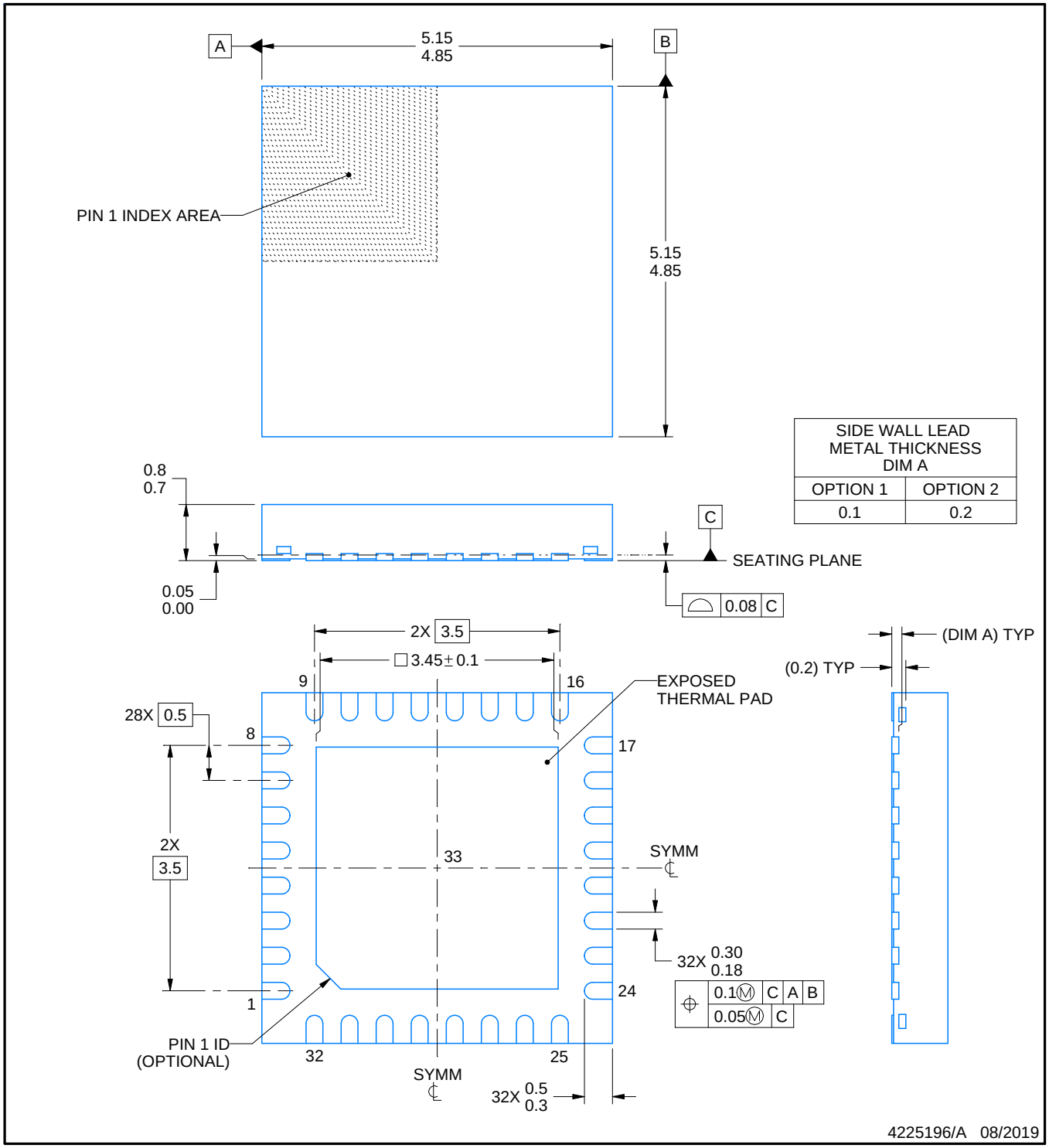
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

RTV0032E

PACKAGE OUTLINE

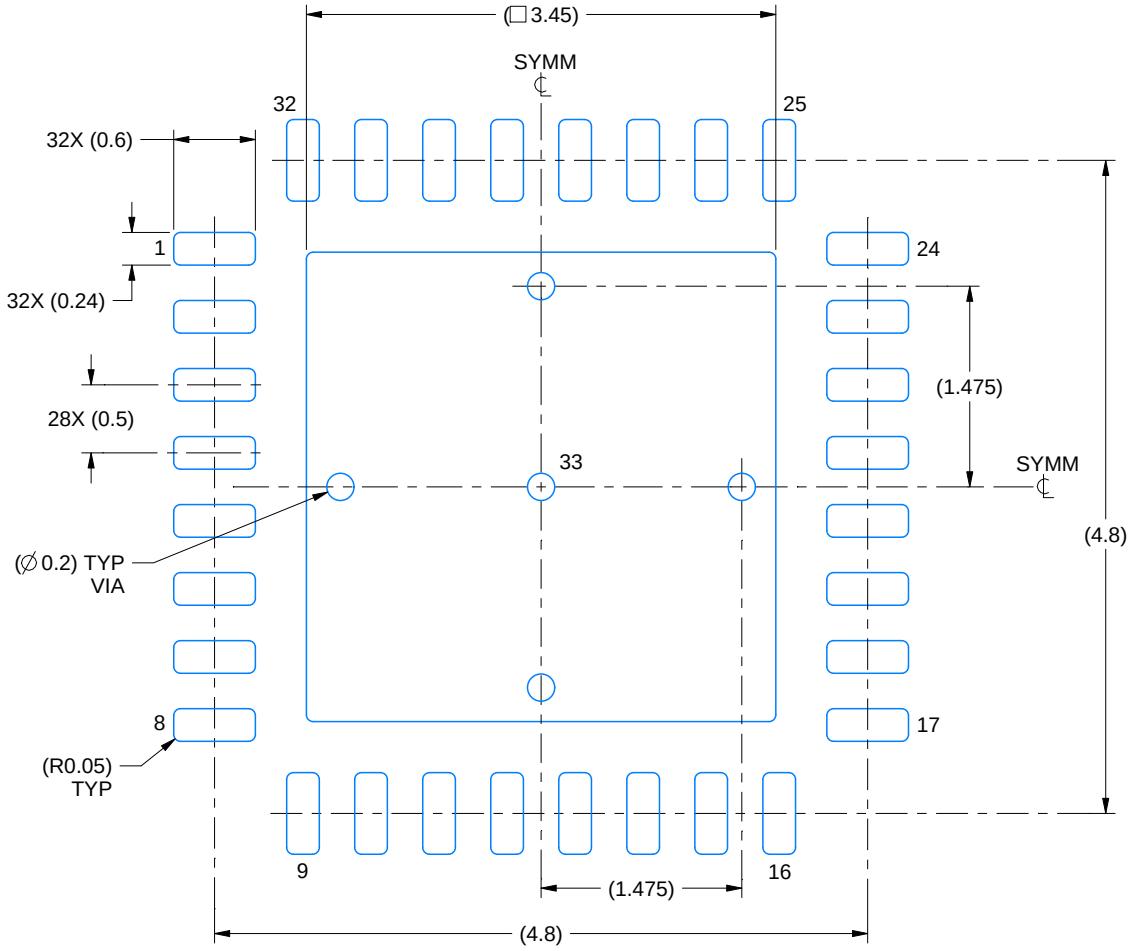
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

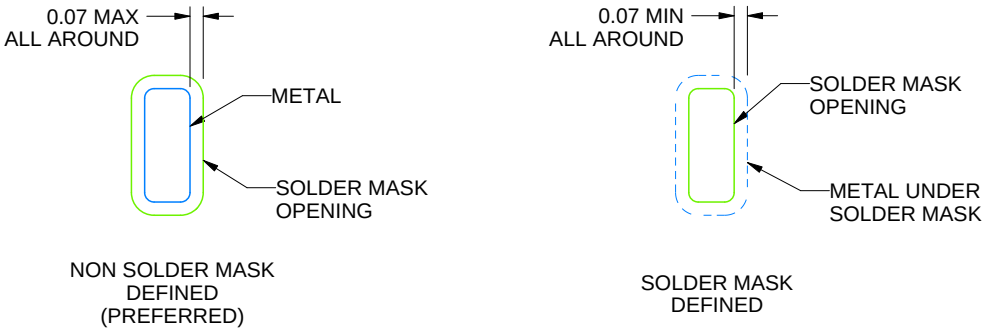


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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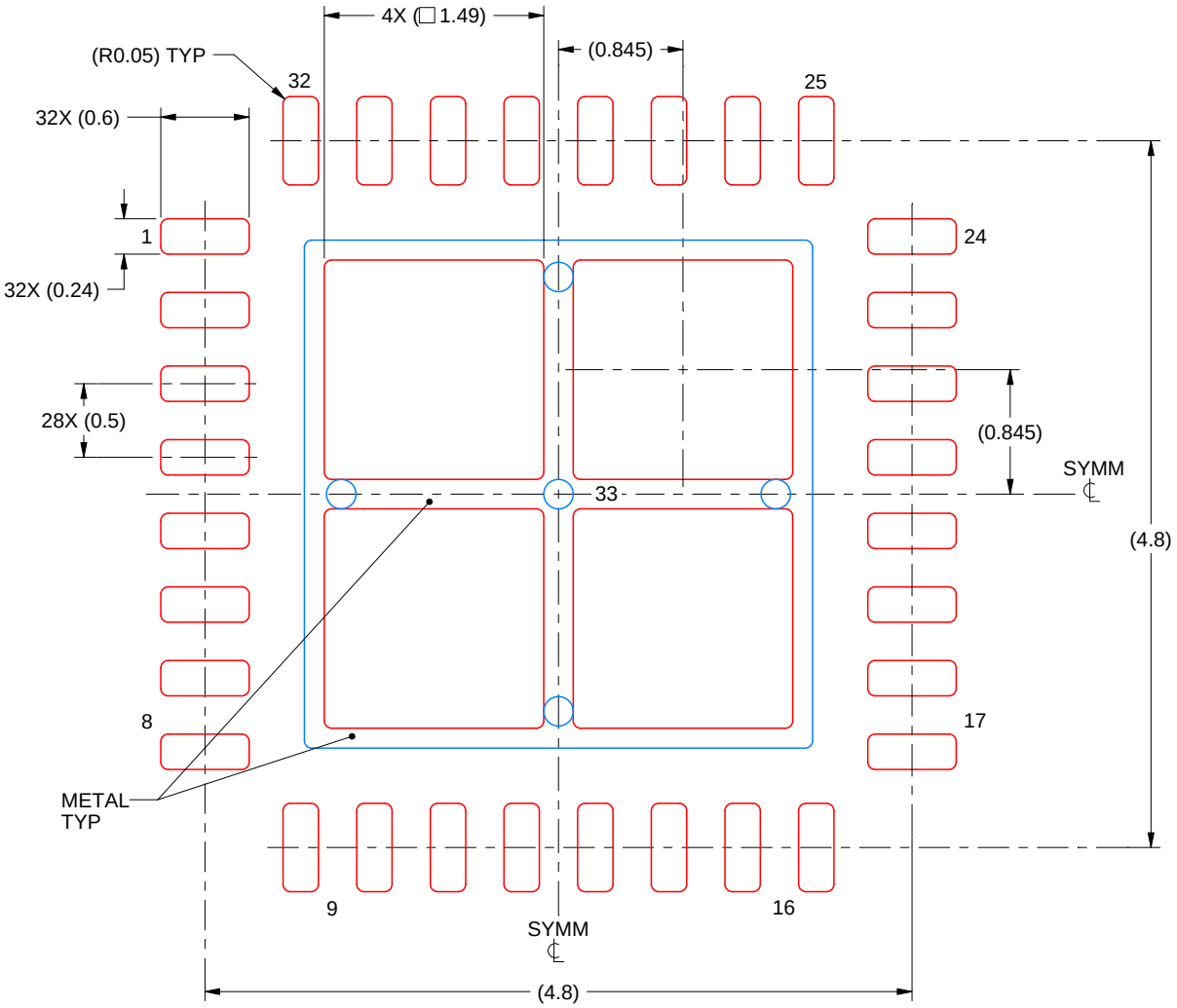
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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