具有电压前馈功能的 TPS40077 4.5V 至 28V 输入、电压模式、同步降压控制器

1 特性

- 在 4.5V 至 28V 输入范围内运行
- 固定频率高达 1MHz 的可编程电压模式控制器
- 预测性栅极驱动反跨导电路
- <1% 内部 700mV 基准电压
- 用于高侧和同步 N 沟道金属氧化物半导体场效应晶体管 (MOSFET) 的内部栅极驱动输出
- 16 引脚 PowerPAD™封装
- 热关断保护
- 与预偏置功能兼容
- 功率级关断功能
- 可编程高侧感应短路保护

2 应用

- 电源模块
- 网络/电信
- PCI Express
- 工业
- 服务器

3 说明

TPS40077 是一款中压、宽输入电压（4.5V 至 28V）同步降压控制器，可以为多种用户可编程功能的设计提供灵活性，包括软启动、欠压锁定 (UVLO)、工作频率、电压前馈以及高侧 FET 检测短路保护。

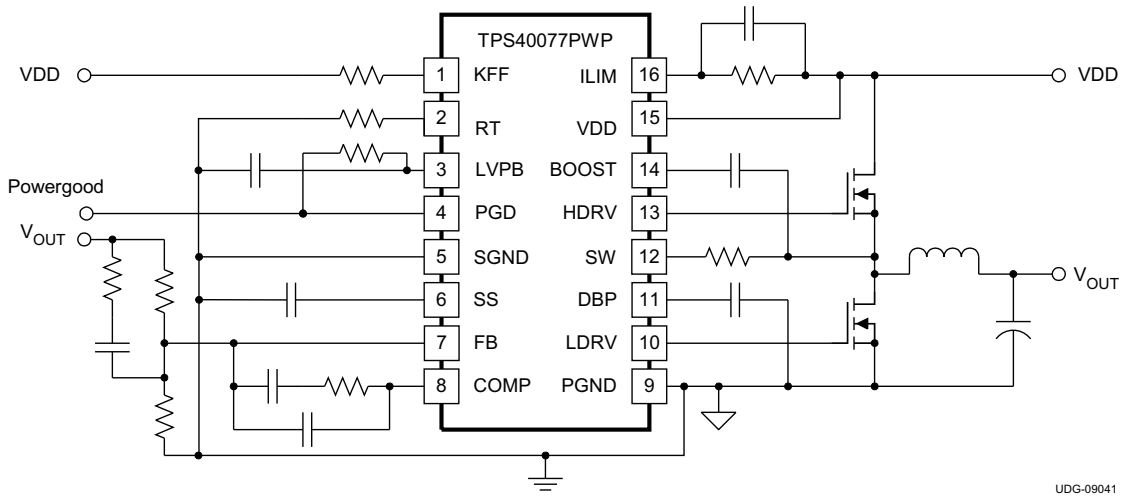
TPS40077 使用第二代预测性栅极驱动器来驱动外部 N 沟道 MOSFET，以便最大限度降低低侧 FET 的体二极管的导电能力，并最大限度提高效率。其支持预偏置输出，方式是在闭环软启动所需的电压大于预偏置电压之前，禁止打开低侧 FET。电压前馈功能可在发生输入瞬变时即时响应，并在宽输入电压工作范围内提供恒定的 PWM 增益以降低补偿要求。可编程的短路保护提供了故障电流限制和断续恢复功能，可最大限度降低输出短路时的功率耗散。16 引脚 PowerPAD 封装带来良好的热性能和紧凑的外形。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS40077	HTSSOP (16)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化应用示意图



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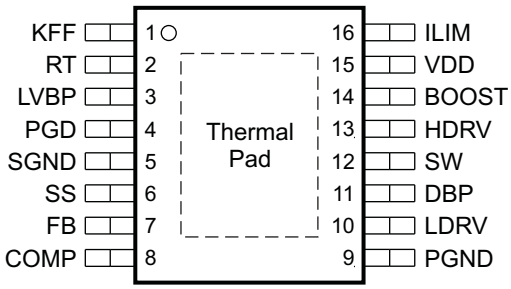
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (April 2009) to Revision E	Page
• 添加了*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分；编辑性更改	1
• Deleted Ordering Information table	3
• Moved Package Dissipation Ratings table to *Power Dissipation*	16

5 Pin Configuration and Functions

16-Pin HTSSOP with PowerPAD
PWP PACKAGE(1)
(TOP VIEW)



P0047-01

(1) For more information on the PWP package, see the *PowerPAD Thermally Enhanced Package* technical brief (SLMA002).

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	KFF	I	A resistor connected from this pin to VIN programs the amount of feed-forward voltage. The current fed into this pin is internally divided by 25 and used to control the slope of the PWM ramp and program UVLO. Nominal voltage at this pin is maintained at 400 mV.
2	RT	I	A resistor is connected from this pin to ground to set the internal oscillator and switching frequency.
3	LVBP	O	4.2-V reference used for internal device logic only. This pin should be bypassed by a 0.1-μF ceramic capacitor. External loads that are less than 1 mA and electrically quiet may be applied.
4	PGD	O	This is an open-drain output that pulls to ground when soft start is active, or when the FB pin is outside a ±10% band around VREF.
5	SGND	—	Signal ground reference for the device. Low-level quiet circuitry around the IC should connect to this pin. This pin should be connected to the thermal pad under the IC, and that thermal pad should connect to the PGND pin. Do not allow power currents to flow in the thermal pad or in the SGND part of the ground for best results.
6	SS	I	Soft-start programming pin. A capacitor connected from this pin to GND programs the soft-start time. The capacitor is charged with an internal current source of 12 μA. The resulting voltage ramp on the SS pin is used as a second noninverting input to the error amplifier. The voltage at this error amplifier input is approximately 1 V less than that on the SS pin. Output voltage regulation is controlled by the SS voltage ramp until the voltage on the SS pin reaches the internal offset voltage of 1 V plus the internal reference voltage of 700 mV. If SS is pulled below 225 mV, the device goes into a shutdown state where the power FETSs are turned off and the prebias circuitry is reset. If the programmed UVLO voltage is below 6 V, connect a 330-kΩ resistor in parallel with the SS capacitor. Also provides timing for fault recovery attempts.
7	FB	I	Inverting input to the error amplifier. In normal operation, the voltage on this pin is equal to the internal reference voltage, 0.7 V.
8	COMP	O	Output of the error amplifier, input to the PWM comparator. A feedback network is connected from this pin to the FB pin to compensate the overall loop. The COMP pin is internally clamped to 3.4 V.
9	PGND	—	Power ground reference for the device. There should be a low-impedance path from this pin to the source(s) of the lower MOSFET(s).
10	LDRV	O	Gate drive for the N-channel synchronous rectifier. This pin switches from DBP (MOSFET on) to ground (MOSFET off). For proper operation, the total gate charge of the MOSFET connected to LDRV should be less than 50 nC.
11	DBP	O	8-V reference used for the gate drive of the N-channel synchronous rectifier. This pin should be bypassed to ground with a 1-μF ceramic capacitor.
12	SW	I	This pin is connected to the switched node of the converter. It is used for short-circuit sensing and gate-drive timing information and is the return for the high-side driver. A 1.5-Ω resistor is required in series with this pin for protection against substrate current issues.
13	HDRV	O	Floating gate drive for the high-side N-channel MOSFET. This pin switches from BOOST (MOSFET on) to SW (MOSFET off).

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
14	BOOST	I	The peak voltage on BOOST is equal to the SW node voltage plus the voltage present at DBP less the bootstrap diode drop. This drop can be 1.4 V for the internal bootstrap diode or 300 mV for an external Schottky diode. The voltage differential between this pin and SW is the available drive voltage for the high-side FET.
15	VDD	I	Supply voltage for the device.
16	ILIM	I	Short-circuit-protection programming pin. This pin is used to set the short circuit detection threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor connected from this pin to VDD. The voltage on this pin is compared to the voltage drop ($V_{VDD} – V_{SW}$) across the high side N-channel MOSFET during conduction. Just prior to the beginning of a switching cycle, this pin is pulled to approximately VDD/2 and released when SW is within 2 V of V_{DD} or after a timeout (the precondition time), whichever occurs first. Placing a capacitor across the resistor from ILIM to VDD allows the ILIM threshold to decrease during the switch-on time, effectively programming the ILIM blanking time. See *Application Information*.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage, V_{VDD}	VDD, ILIM		30	V
	COMP, FB, KFF, PGD, LVBP	–0.3	6	
	SW	–0.3	40	
	SW, transient (<50 ns)		–2.5	
Output voltage, V_{OUT}	COMP, KFF, RT, SS	–0.3	6	V
	VBOOST		50	
	DBP		10.5	
	LVBP		6	
Output current source, I_{OUT} (LDRV, HDRV)			1.5	A
Output current sink, I_{OUT}	LDRV, HDRV		2	A
	KFF		10	
Output current	RT		1	mA
	LVBP		1.5	
Lead temperature, 1.6 mm (1/16 inch) from case (10 s)			260	°C
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Input voltage	4.5		28	V
T_A	Operating free-air temperature	–40		85	°C

6.4 Electrical Characteristics

T_A = –40°C to 85°C, V_{IN} = 12 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 300 µA, f_{SW} = 500 kHz, and all parameters at zero power dissipation (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VDD}	Input voltage range, VIN		4.5		28	V
I_{VDD}	Quiescent current	Output drivers not switching		2.5	3.5	mA
V_{LVBP}	Output voltage	$T_A = T_J$ = 25°C	3.9	4.2	4.5	V
OSCILLATOR/RAMP GENERATOR						
f_{OSC}	Accuracy		450	500	550	kHz
V_{RAMP}	PWM ramp voltage(1)	$V_{PEAK} – V_{VAL}$		2		V
V_{RT}	RT voltage		2.23	2.4	2.58	V
t_{ON}	Minimum output pulse time(1)	C_{HDRV} = 0 nF			150	ns
	Maximum duty cycle	V_{FB} = 0 V, 100 kHz ≤ f_{SW} ≤ 500 kHz	84%		93%	
		V_{FB} = 0 V, f_{SW} = 1 MHz	76%		93%	
V_{KFF}	Feed-forward voltage		0.35	0.4	0.45	V
I_{KFF}	Feed-forward current operating range(1)		20		1100	µA
SOFT START						
I_{SS}	Charge current		7	12	17	µA
t_{DSCH}	Discharge time	C_{SS} = 3.9 nF	25		75	µs
t_{SS}	Soft-start time	C_{SS} = 3.9 nF, V_{SS} rising from 0.7 V to 1.6 V	210	290	500	µs
V_{SSSD}	Turnon threshold		310	365	420	mV
	Shutdown threshold		225	275	325	
V_{SSSDH}	Shutdown threshold hysteresis		35		150	mV
V_{DBP}	Output voltage	V_{DD} > 10 V	7	8	9	V
		V_{DD} = 4.5 V, I_{OUT} = 25 mA	4	4.3		
ERROR AMPLIFIER						
V_{FB}	Feedback regulation voltage total variation	T_J = 25°C	0.698	0.7	0.704	V
		0°C ≤ T_J ≤ 85°C	0.69	0.7	0.707	
		–40°C ≤ T_J ≤ 85°C	0.69	0.7	0.715	
V_{SS}	Soft-start offset from VSS(1)	Offset from V_{SS} to error amplifier		1		V
G_{BW}	Gain bandwidth(1)		5	10		MHz
A_{VOL}	Open-loop gain		50			dB
I_{SRC}	Output source current		2.5	4.5		mA
I_{SINK}	Output sink current		2.5	6		mA
I_{BIAS}	Input bias current	V_{FB} = 0.7 V	–250		0	nA
SHORT-CIRCUIT CURRENT PROTECTION						
I_{ILIM}	Current sink into current limit		80	105	125	µA
$V_{ILIM(ofst)}$	Current limit offset voltage ($V_{SW} – V_{ILIM}$)	V_{ILIM} = 11.5 V, V_{VDD} = 12 V	–75	–50	–30	mV
t_{HSC}	Minimum HDRV pulse duration	During short circuit		135	225	ns
	Propagation delay to output(1)			50		ns
t_{BLANK}	Blanking time(1)			50		ns
t_{OFF}	Off time during a fault (SS cycle times)			7		Cycles
V_{SW}	Switching level to end precondition ($V_{VDD} – V_{SW}$)(1)			2		V
t_{PC}	Precondition time(1)				100	ns
V_{ILIM}	Current limit precondition voltage threshold(1)			6.8		V

(1) Ensured by design. Not production tested.

Electrical Characteristics (continued)

T_A = –40°C to 85°C, V_{IN} = 12 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 300 μA, f_{SW} = 500 kHz, and all parameters at zero power dissipation (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS						
t_{HFALL}	High-side driver fall time (HDRV – SW)(1)	C_{HDRV} = 2200 pF		36		ns
t_{HRISE}	High-side driver rise time (HDRV – SW)(1)			48		ns
t_{HFALL}	High-side driver fall time (HDRV – SW)(1)	C_{HDRV} = 2200 pF, V_{VDD} = 4.5 V, 0.2 V ≤ V_{SS} ≤ 4 V		72		ns
t_{HRISE}	High-side driver rise time (HDRV – SW)(1)			96		ns
t_{LFALL}	Low-side driver fall time(1)	C_{LDRV} = 2200 pF		24		ns
t_{LRISE}	Low-side driver rise time(1)			48		ns
t_{LFALL}	Low-side driver fall time(1)	C_{LDRV} = 2200 pF, V_{VDD} = 4.5 V, 0.2 V ≤ V_{SS} ≤ 4 V		48		ns
t_{LRISE}	Low-side driver rise time(1)			96		ns
V_{OH}	High-level output voltage, HDRV (V_{BOOST} – V_{HDRV})	I_{HDRV} = –0.01 A		0.7	1	V
		I_{HDRV} = –0.1 A		0.95	1.3	
V_{OL}	Low-level output voltage, HDRV (V_{HDRV} – V_{SW})	I_{HDRV} = 0.01A		0.06	0.1	V
		I_{HDRV} = 0.1 A		0.65	1	
V_{OH}	High-level output voltage, LDRV (V_{DBP} – V_{LDRV})	I_{LDRV}= –0.01A		0.65	1	V
		I_{LDRV} = –0.1 A		0.875	1.2	
V_{OL}	Low-level output voltage, LDRV	I_{LDRV} = 0.01 A		0.03	0.05	V
		I_{LDRV} = 0.1 A		0.3	0.5	
V_{BOOST}	Output voltage	V_{DD} = 12 V	15.2	17		V
UVLO						
V_{UVLO}	Programmable UVLO threshold voltage	R_{KFF} = 90.9 kΩ, turn-on, V_{VDD} rising	6.2	7.2	8.2	V
	Programmable UVLO hysteresis	R_{KFF} = 90.9 kΩ	1.1	1.55	2	V
	Fixed UVLO threshold voltage	Turn-on, V_{VDD} rising	4.15	4.3	4.45	V
	Fixed UVLO hysteresis		275	365		mV
POWER GOOD						
V_{PG}	Power-good voltage	I_{PG} = 1 mA		370	500	mV
V_{OH}	High-level output voltage, FB			770		mV
V_{OL}	Low-level output voltage, FB			630		mV
THERMAL SHUTDOWN						
	Shutdown temperature threshold(1)			165		°C
	Hysteresis(1)			15		°C

6.5 Typical Characteristics

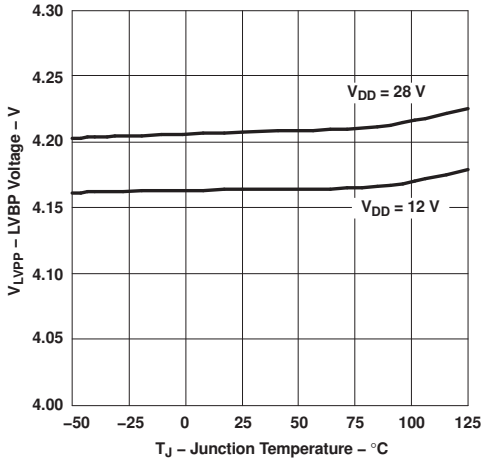


Figure 1. LVBP Voltage vs Junction Temperature

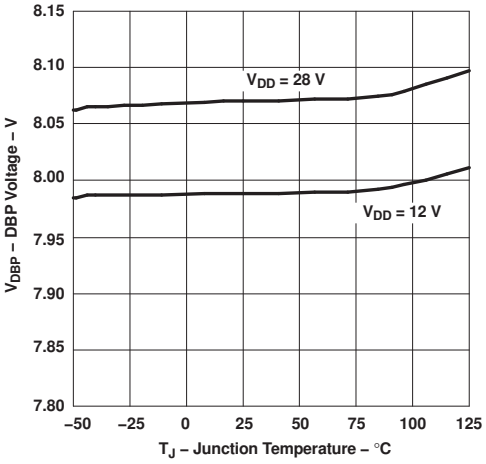


Figure 2. DBP Voltage vs Junction Temperature

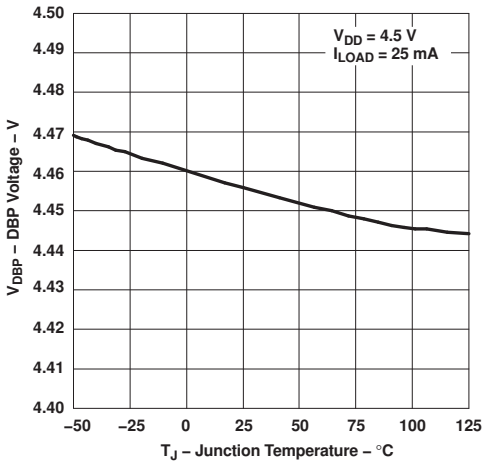


Figure 3. DBP Voltage vs Junction Temperature

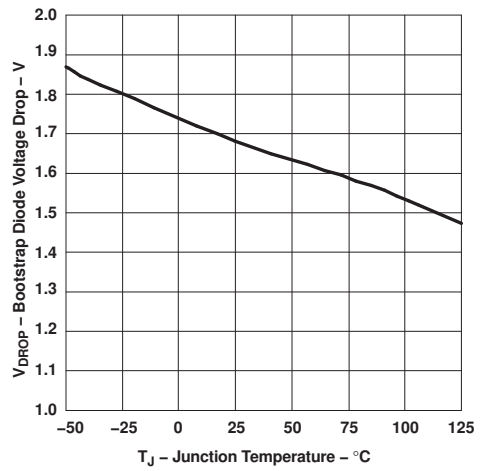


Figure 4. Bootstrap Diode Voltage vs Junction Temperature

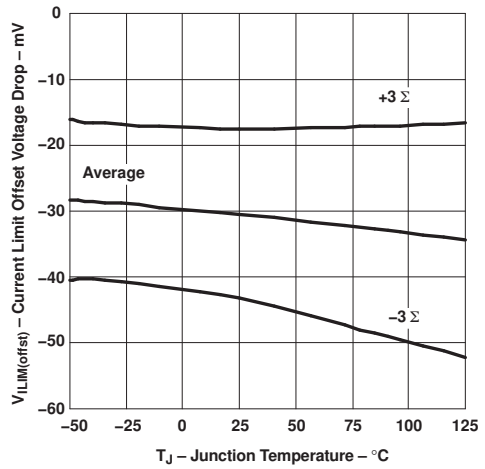


Figure 5. Current Limit Offset Voltage vs Junction Temperature

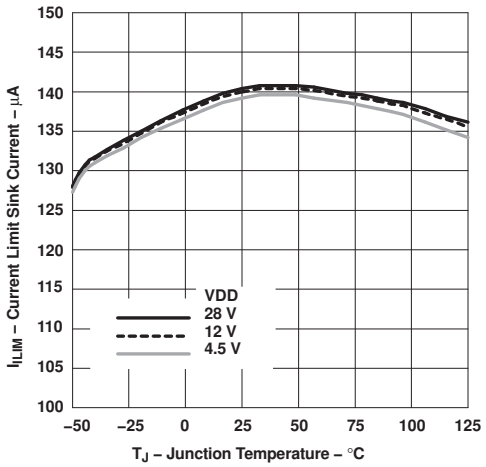


Figure 6. Current Limit Sink Current vs Junction Temperature

Typical Characteristics (continued)

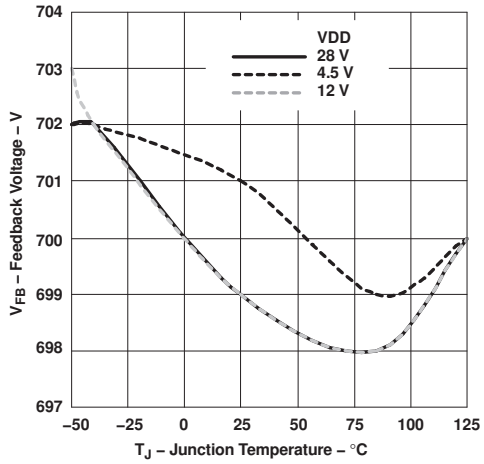


Figure 7. Feedback Regulation Voltage vs Junction Temperature

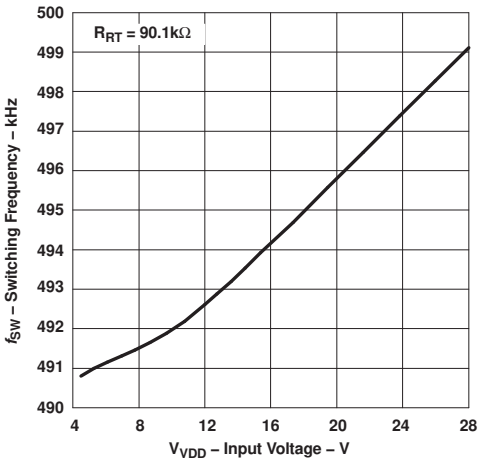


Figure 8. Switching Frequency vs Input Voltage

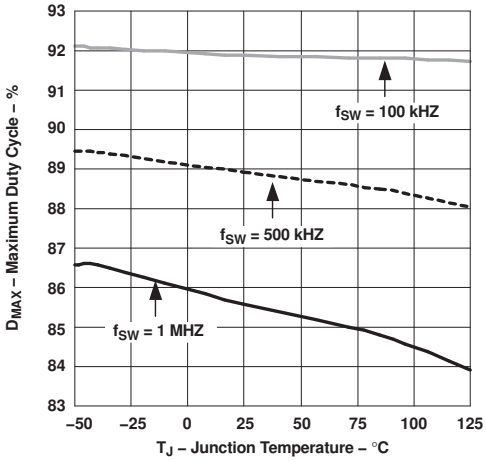


Figure 9. Maximum Duty Cycle vs Junction Temperature

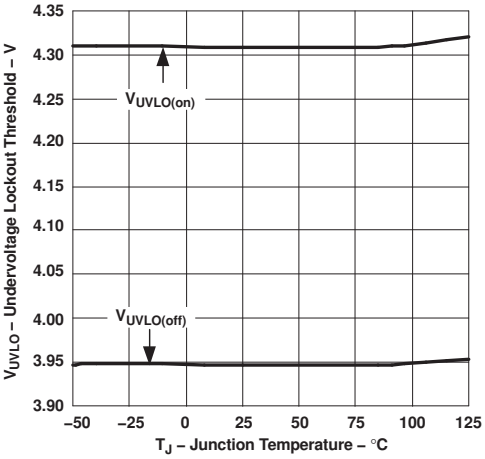


Figure 10. Undervoltage Lockout vs Junction Temperature

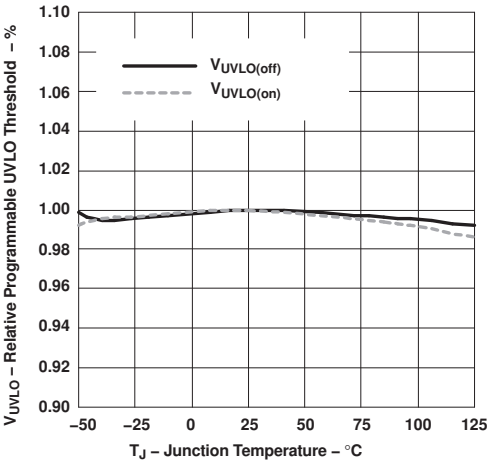


Figure 11. Programmable UVLO Threshold vs Junction Temperature

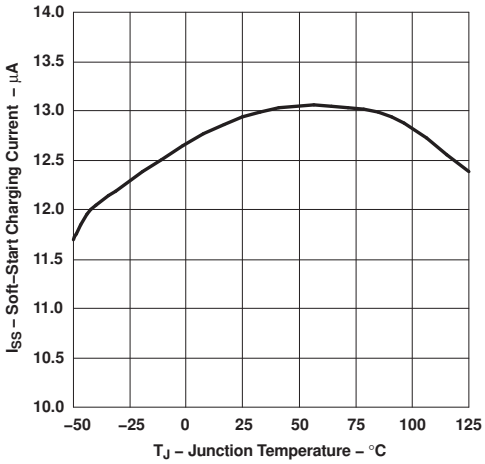


Figure 12. Soft-Start Charging Current vs Junction Temperature

Typical Characteristics (continued)

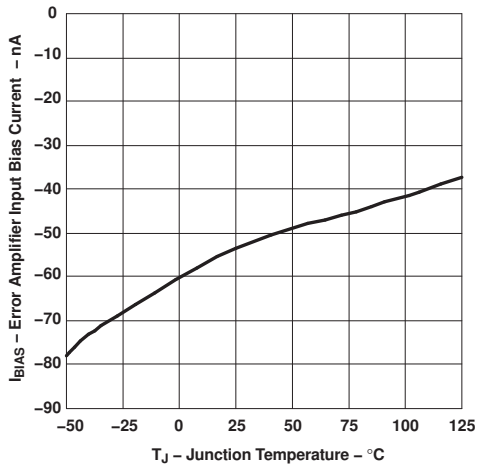


Figure 13. Error Amplifier Input Bias Current vs Junction Temperature

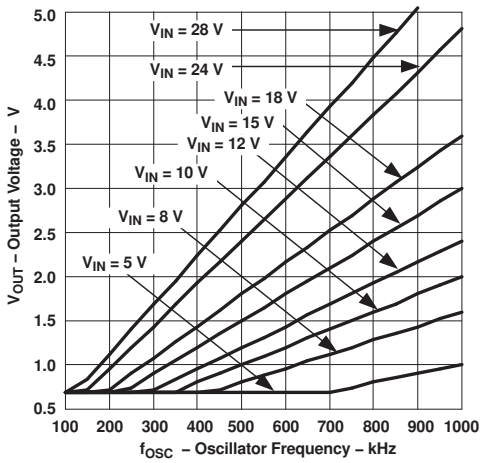


Figure 14. Minimum Output Voltage vs Frequency

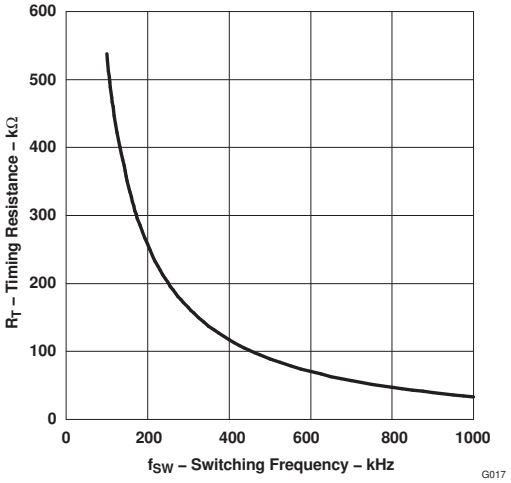


Figure 15. Switching Frequency vs Timing Resistance

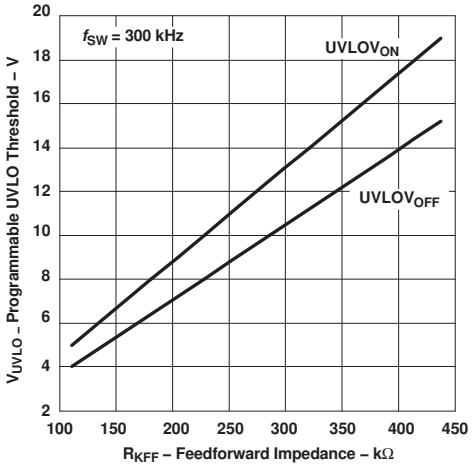


Figure 16. Undervoltage Lockout Threshold vs Feed-Forward Impedance

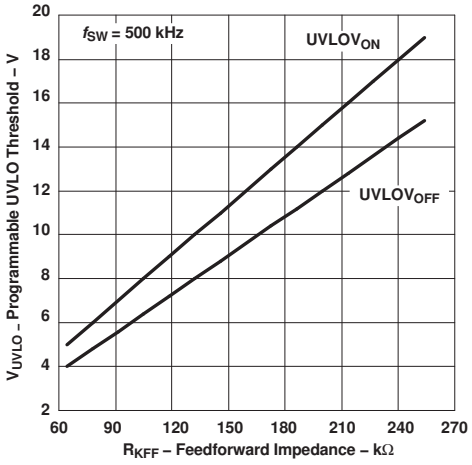


Figure 17. Undervoltage Lockout Threshold vs Feed-Forward Impedance

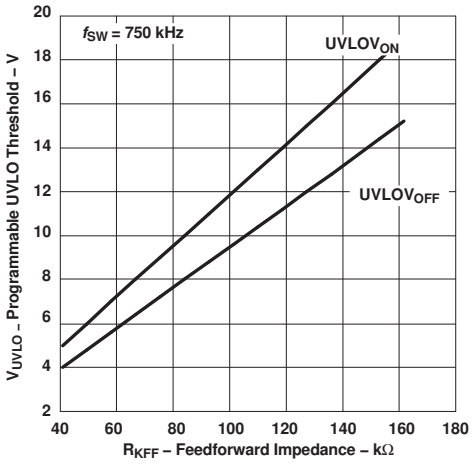


Figure 18. Undervoltage Lockout Threshold vs Feed-Forward Impedance

Typical Characteristics (continued)

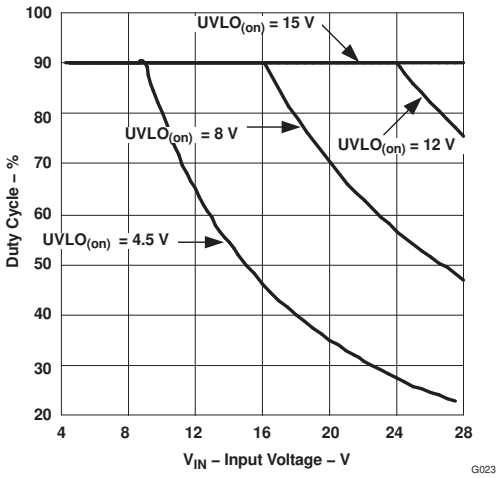


Figure 19. Typical Maximum Duty Cycle vs Input Voltage

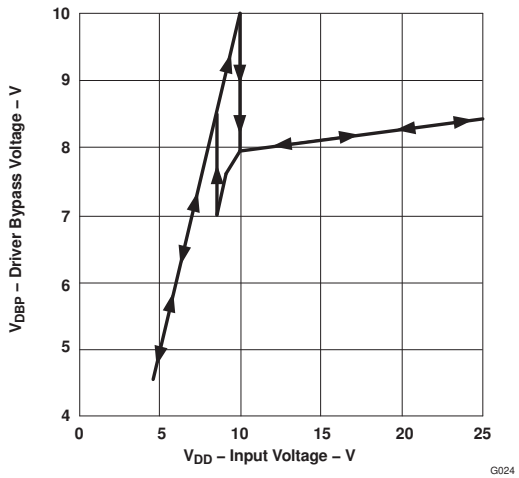


Figure 20. DBP Voltage vs Input Voltage

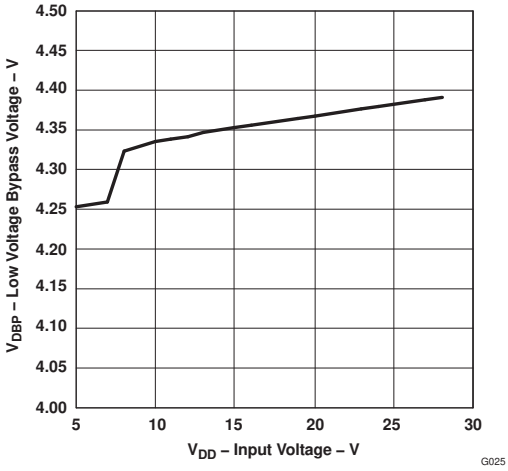


Figure 21. Input Voltage vs Low-Voltage Bypass Voltage

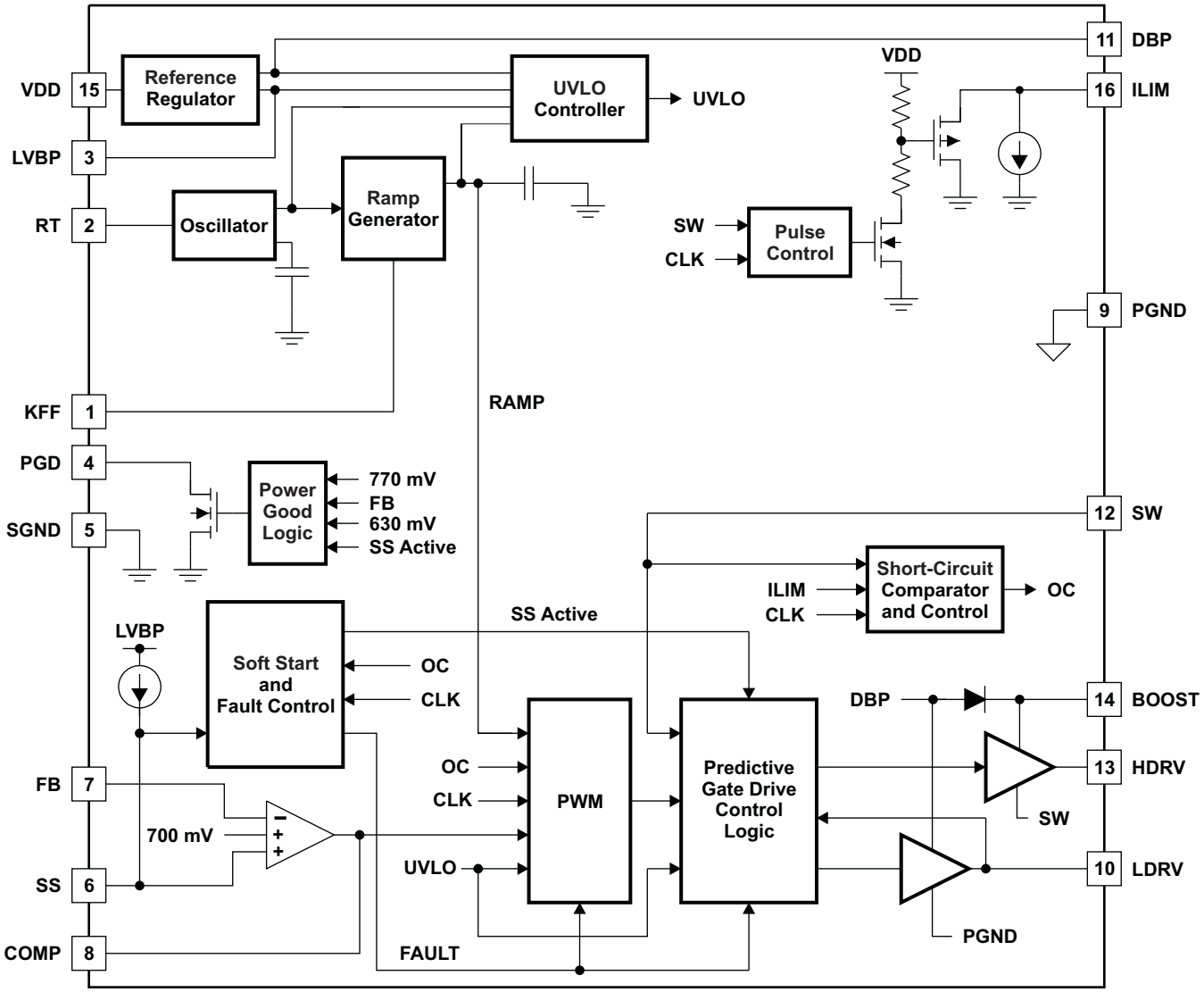
7 Detailed Description

7.1 Overview

The TPS40077 allows the user to construct synchronous voltage-mode buck converters with inputs ranging from 4.5 V to 28 V and outputs as low as 700 mV. Predictive Gate Drive circuitry optimizes switching delays for increased efficiency and improved converter output-power capability. Voltage feed forward is employed to ease loop compensation for wide-input-range designs and provide better line transient response.

The TPS40077 incorporates circuitry to allow start-up into a preexisting output voltage without sinking current from the source of the preexisting output voltage. This avoids damaging sensitive loads at start-up. An integrated power-good indicator is available for logic (open-drain) output of the condition of the output of the converter.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Minimum Pulse Duration

The TPS40077 devices have limitations on the minimum pulse duration that can be used to design a converter. Reliable operation is assured for nominal pulse durations of 150 ns and above. This places some restrictions on the conversion ratio that can be achieved at a given switching frequency. Figure 14 shows minimum output voltage for a given input voltage and frequency.

7.3.2 Slew Rate Limit On VDD

The regulator that supplies power for the drivers on the TPS40077 requires a limited rising slew rate on VDD for proper operation if the input voltage is above 10 V. If the slew rate is too great, this regulator can overshoot and damage to the part can occur. To ensure that the part operates properly, limit the slew rate to no more than 0.12 V/µs as the voltage at VDD crosses 8 V. If necessary, an R-C filter can be used on the VDD pin of the device. Connect the resistor from the VDD pin to the input supply of the converter. Connect the capacitor from the VDD pin to PGND. There should not be excessive (more than a 200-mV) voltage drop across the resistor in normal operation. This places some constraints on the R-C values that can be used. Figure 22 is a schematic fragment that shows the connection of the R-C slew rate limit circuit. Equation 1 and Equation 2 give values for R and C that limit the slew rate in the worst-case condition.

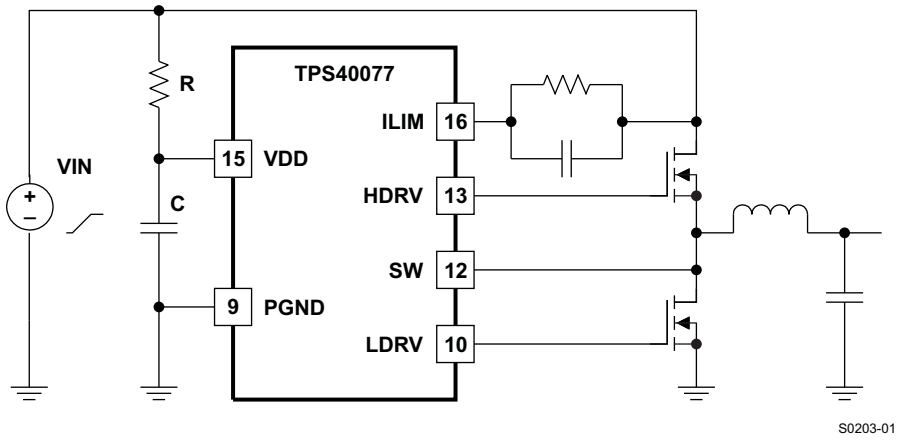


Figure 22. Limiting the Slew Rate

$$C > \frac{V_{IN} - 8\ V}{R \times SR} \qquad (1)$$

$$R < \frac{0.2\ V}{f_{SW} \times Q_{g(TOT)} + I_{DD}}$$

where

- V_{VIN} is the final value of the input voltage ramp
- f_{SW} is the switching frequency
- $Q_{g(TOT)}$ is the combined total gate charge for both upper and lower MOSFETs (from MOSFET data sheet)
- I_{DD} is the TPS40077 input current (3.5 mA maximum)
- SR is the maximum allowed slew rate [12 $\times 10^4$] (V/s) (2)

Feature Description (continued)

7.3.3 Setting The Switching Frequency (Programming The Clock Oscillator)

The TPS40077 has independent clock oscillator and PWM ramp generator circuits. The clock oscillator serves as the master clock to the ramp generator circuit. Connecting a single resistor from RT to ground sets the switching frequency of the clock oscillator. The clock frequency is related to R_T with Equation 3.

$$R_T = \left(\frac{1}{f_{SW}(kHz) \times 17.82 \times 10^{-6}} - 23 \right) k\Omega \quad (3)$$

7.3.4 Loop Compensation

Voltage-mode, buck-type converters are typically compensated using Type III networks. Because the TPS40077 uses voltage feed-forward control, the gain of the voltage feed-forward circuit must be included in the PWM gain. The gain of the voltage feed-forward circuit, combined with the PWM circuit and power stage for the TPS40077 is Equation 4.

$$K_{PWM} \cong V_{UVLO(on)} \quad (4)$$

The remainder of the loop compensation is performed as in a normal buck converter. Note that the voltage feed-forward circuitry removes the input voltage term from the expression for PWM gain. PWM gain is strictly a function of the programmed start-up voltage.

7.3.5 Shutdown and Sequencing

The TPS40077 can be shut down by pulling the SS pin below 250 mV. In this state, both of the output drivers are in the low-output state, turning off both of the power FETs. This places the output of the converter in a high-impedance state. When shutting down the converter, a crisp pulldown of the SS pin is preferred to a slow pulldown. A slow pulldown could allow the output to be pulled low, possibly sinking current from the load. As a general rule of thumb, the fall time of SS when shutting down the converter should be no more than 1/10th of the control loop crossover frequency. An example of a shutdown interface is shown in Figure 23.

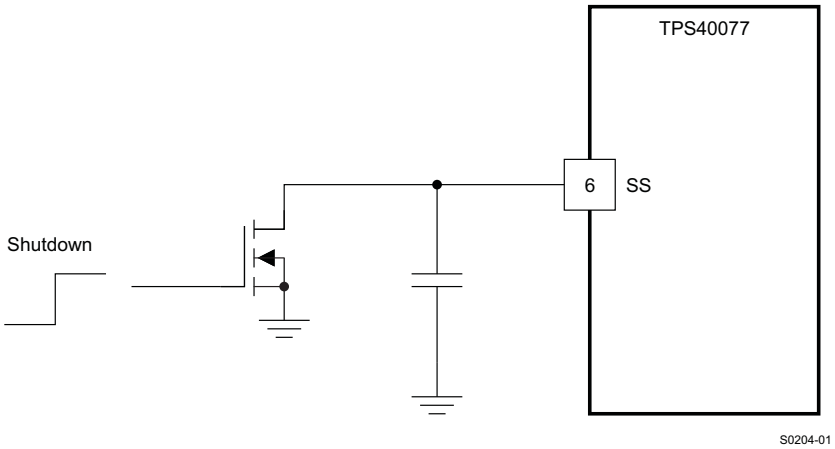


Figure 23. TPS40077 Shutdown

In a similar manner, power supplies based on the TPS40077 can be sequenced by connecting the PGD pin of the first supply to come up to the SS pin of the second supply as shown in Figure 24.

Feature Description (continued)

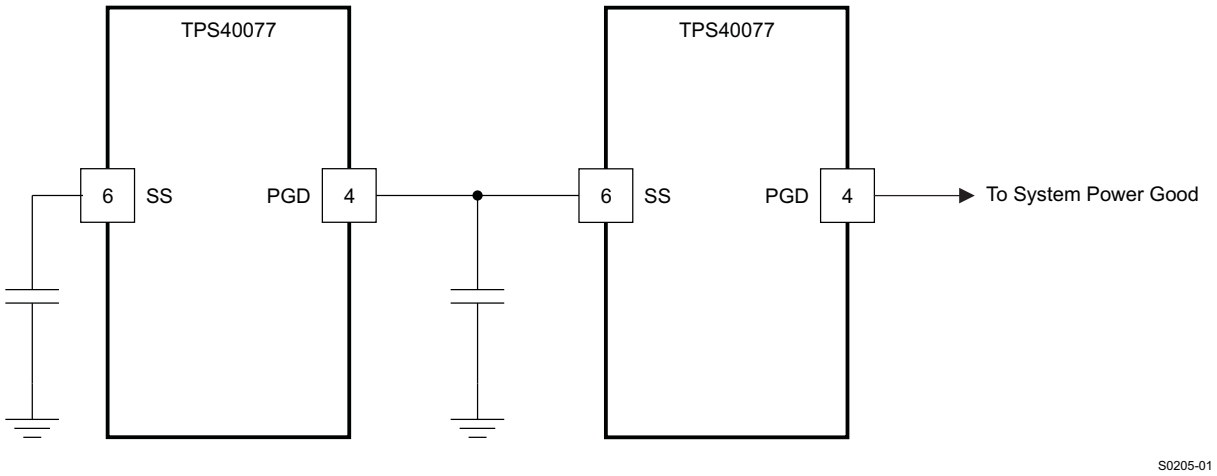


Figure 24. TPS40077 Sequencing

7.3.6 Boost and LVBP Bypass Capacitance

The BOOST capacitance provides a local, low-impedance flying source for the high-side driver. The BOOST capacitor should be a good-quality, high-frequency capacitor. A capacitor with a minimum value of 100-nF is suggested.

The LVBP pin must provide energy for both the synchronous MOSFET and the high-side MOSFET (via the BOOST capacitor). The suggested value for this capacitor is 1-μF ceramic, minimum.

7.3.7 Internal Regulators

The internal regulators are linear regulators that provide controlled voltages from which the drivers and the internal circuitry operate. The DBP pin is connected to a nominal 8-V regulator that provides power for the driver circuits. This regulator has two modes of operation. At V_{DD} voltages below 8.5 V, the regulator is in a low-dropout mode of operation and tries to provide as little impedance as possible from VDD to DBP. Above 10 V at V_{DD}, the regulator regulates DBP to 8 V. Between these two voltages, the regulator remains in the state it was in when V_{DD} entered this region (see Figure 20). Small amounts of current can be drawn from this pin for other circuit functions, as long as power dissipation in the controller device remains at acceptable levels and junction temperature does not exceed 125°C.

The LVBP pin is connected to another internal regulator that provides 4.2 V (nom) for the operation of low-voltage circuitry in the controller. This pin can be used for other circuit purposes, but extreme care must be taken to ensure that no extra noise is coupled onto this pin; otherwise, controller performance suffers. Current draw is not to exceed 1 mA. See Figure 21 for typical output voltage at this pin.

7.3.8 Power Dissipation

The power dissipation in the TPS40077 is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Qg, of the external MOSFETs. Driver power (neglecting external gate resistance) can be calculated with Equation 5.

$$P_D = Q_g \times V_{DR} \times f_{SW} \quad \text{(Watts/driver)} \tag{5}$$

where

V_{DR} is the driver output voltage

The total power dissipation in the TPS40077, assuming the same MOSFET is selected for both the high-side and synchronous rectifier, is described in Equation 6 or Equation 7.

$$P_T = \left(\frac{2 \times P_D}{V_{DR}} + I_Q \right) \times V_{IN} \quad \text{(Watts)} \tag{6}$$

Feature Description (continued)

or

$$P_T = \left(2 \times Q_g \times f_{SW} + I_Q\right) \times V_{IN} \quad \text{(Watts)}$$

where I_Q is the quiescent operating current (neglecting drivers) (7)

The maximum power capability of the TPS40077 PowerPAD package is dependent on the layout as well as air flow. The thermal impedance from junction to air, assuming 2-oz. copper trace and thermal pad with solder and no air flow, is 37°C/W. See the application report titled *PowerPAD Thermally Enhanced Package* (SLMA002) for detailed information on PowerPAD package mounting and usage.

The maximum allowable package power dissipation is related to ambient temperature by Equation 8. For θ_{JA}, see Table 1.

$$P_T = \frac{T_J - T_A}{\theta_{JA}} \quad \text{(Watts)} \tag{8}$$

Table 1. Package Dissipation Ratings

	THERMAL IMPEDANCE, JUNCTION-TO-AMBIENT(1)	T_A = 25°C POWER RATING	T_A = 85°C POWER RATING
Natural convection	37°C/W	2.7 W	1.08 W
150 LFM airflow	30°C/W	3.33 W	1.33 W
250 LFM airflow	28°C/W	3.57 W	1.42 W
500 LFM airflow	26°C/W	3.84 W	1.52 W

(1) For more information on the board and the methods used to determine ratings, see the *PowerPAD Thermally Enhanced Package* application report (SLMA002).

Substituting Equation 8 into Equation 7 and solving for f_{SW} yields the maximum operating frequency for the TPS40077. The result is described in Equation 9.

$$f_{SW} = \frac{\left(\left[\frac{(T_J - T_A)}{(\theta_{JA} \times V_{DD})}\right] - I_Q\right)}{\left(2 \times Q_g\right)} \quad \text{(Hz)} \tag{9}$$

7.3.9 Boost Diode

The TPS40077 series has internal diodes to charge the boost capacitor connected from SW to BOOST. The drop across these diodes is rather large, 1.4 V nominal, at room temperature. If this drop is too large for a particular application, an external diode may be connected from DBP (anode) to BOOST (cathode). This provides significantly improved gate drive for the high-side FET, especially at lower input voltages.

7.3.10 Synchronous Rectifier Control

Table 2 describes the state of the rectifier MOSFET control under various operating conditions.

Table 2. Synchronous Rectifier MOSFET States

SYNCHRONOUS RECTIFIER OPERATION DURING			
SOFT-START	NORMAL	FAULT (FAULT RECOVERY IS SAME AS SOFT-START)	OVERVOLTAGE
Off until first high-side pulse is detected, then on when high-side MOSFET is off	Turns off at the start of a new cycle. Turns on when the high-side MOSFET is turned off	OFF	Turns OFF only at start of next cycle only if the pulse width modulator duty cycle is greater than zero. Otherwise, stays ON

For proper operation, the total gate charge of the MOSFET connected to LDRV must be less than 50 nC.

7.4 Programming

7.4.1 Programming The Ramp Generator Circuit and UVLO

The ramp generator circuit provides the actual ramp used by the PWM comparator. The ramp generator provides voltage feed-forward control by varying the PWM ramp slope with line voltage, while maintaining a constant ramp magnitude. Varying the PWM ramp directly with line voltage provides excellent response to line variations, because the PWM is not required to wait for loop delays before changing the duty cycle. (See Figure 25).

The PWM ramp must reach approximately 1 V in amplitude during a clock cycle, or the PWM is not allowed to start. The PWM ramp time is programmed via a single resistor (R_{KFF}) connected from KFF VDD. R_{KFF}, V_{START}, and R_T are related by (approximately) Equation 10.

$$R_{KFF} = 0.131 \times R_T \times V_{UVLO(on)} - 1.61 \times 10^{-3} \times V_{UVLO(on)}^{2} + 1.886 \times V_{UVLO} - 1.363 - 0.02 \times R_T - 4.87 \times 10^{-5} \times R_T^2 \quad (10)$$

where

- R_T and R_{KFF} are in kΩ
- $V_{UVLO(on)}$ is in V

This yields typical numbers for the programmed start-up voltage. The minimum and maximum values may vary up to ±15% from this number. Figure 16 through Figure 18 show the typical relationship of $V_{UVLO(on)}$, $V_{UVLO(off)}$ and R_{KFF} at three common frequencies.

The programmable UVLO circuit incorporates 20% hysteresis from the start voltage to the shutdown voltage. For example, if the start-up voltage is programmed to be 10 V, the controller starts when V_{DD} reaches 10 V and shuts down when V_{DD} falls below 8 V. The maximum duty cycle begins to decrease as the input voltage rises to twice the start-up voltage. Below this point, the maximum duty cycle is as specified in the *Electrical Characteristics*. Note that with this scheme, the theoretical maximum output voltage that the converter can produce is approximately two times the programmed start-up voltage. For design, set the programmed start-up voltage equal to or greater than the desired output voltage divided by maximum duty cycle (85% for frequencies 500 kHz and below). For example, a 5-V output converter should not have a programmed start-up voltage below 5.9 V. Figure 25 shows the theoretical maximum duty cycle (typical) for various programmed start-up voltages.

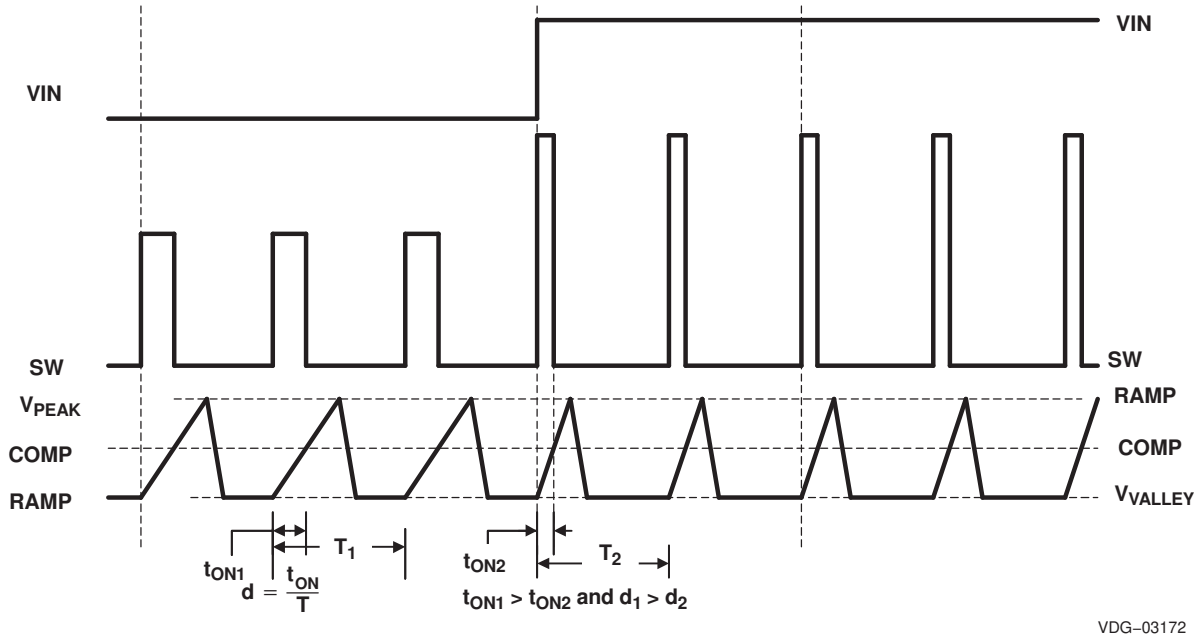


Figure 25. Voltage Feed-Forward and PWM Duty Cycle Waveforms

Programming (continued)

7.4.2 Programming Soft Start

TPS40077 uses a closed-loop approach to ensure a controlled ramp on the output during start-up. Soft start is programmed by connecting an external capacitor (C_{SS}) from the SS pin to GND. This capacitor is charged by a fixed current, generating a ramp signal. The voltage on SS is level-shifted down approximately 1 V and fed into a separate noninverting input to the error amplifier. The loop is closed on the lower of the level-shifted SS voltage or the 700-mV internal reference voltage. Once the level-shifted SS voltage rises above the internal reference voltage, output-voltage regulation is based on the internal reference. To ensure a controlled ramp-up of the output voltage, the soft-start time should be greater than the L-C_{OUT} time constant or Equation 11.

$$t_{START} \geq 2\pi \times \sqrt{L \times C_{OUT}} \tag{11}$$

Note that there is a direct correlation between t_{START} and the input current required during start-up. The lower t_{START} is, the higher the input current required during start-up, because the output capacitance must be charged faster. For a desired soft-start time, the soft-start capacitance, C_{SS}, can be found from Equation 12.

$$C_{SS} = t_{SS} \times \frac{I_{SS}}{V_{FB}} \tag{12}$$

7.4.3 Programming Short-Circuit Protection

The TPS40077 uses a two-tier approach for short-circuit protection. The first tier is a pulse-by-pulse protection scheme. Short-circuit protection is implemented on the high-side MOSFET by sensing the voltage drop across the MOSFET when its gate is driven high. The MOSFET voltage is compared to the voltage dropped across a resistor (R_{ILIM}) connected from V_{VDD} to the ILIM pin when driven by a constant-current sink. If the voltage drop across the MOSFET exceeds the voltage drop across the ILIM resistor, the switching pulse is immediately terminated. The MOSFET remains off until the next switching cycle is initiated. This is illustrated in Figure 26.

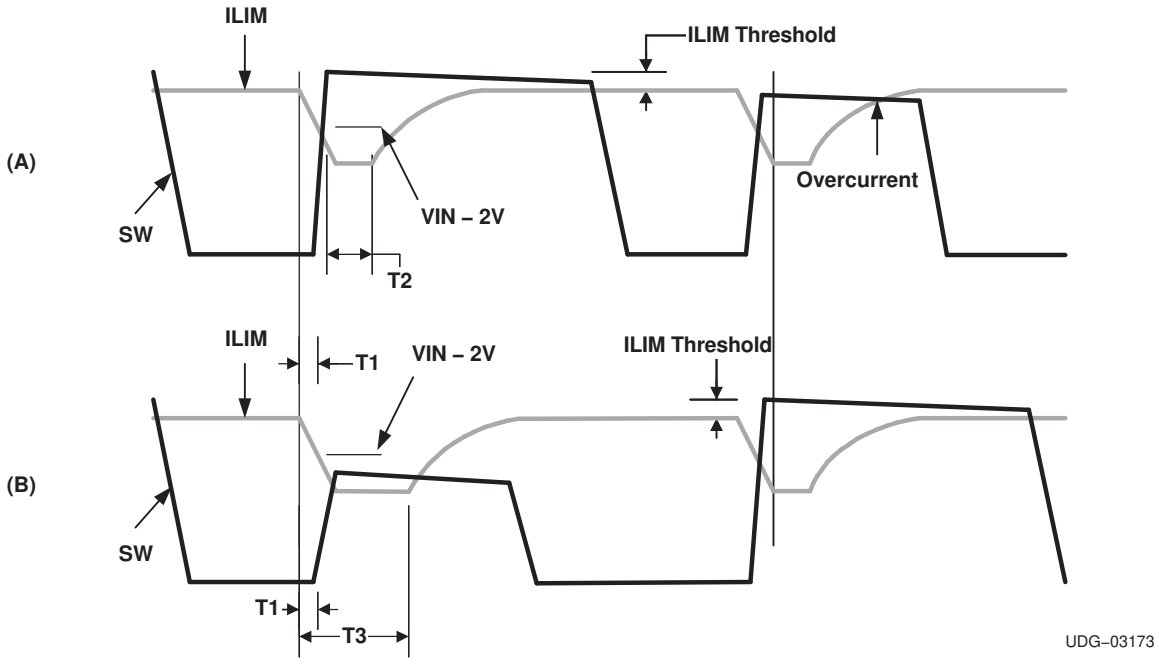


Figure 26. Switching and Current-Limit Waveforms and Timing Relationship

Programming (continued)

In addition, just prior to the high-side MOSFET turning on, the ILIM pin is pulled down to approximately half of V_{VDD}. The ILIM pin is allowed to return to its nominal value after one of two events occurs. If the SW node rises to within approximately 2 V of V_{VDD}, the device allows ILIM to go back to its nominal value. This is illustrated in Figure 26(A). T1 is the delay time from the internal PWM signal being asserted and the rise of SW. This includes a driver delay of 50 ns, typical. T2 is the reaction time of the sensing circuit that allows ILIM to start to return to its nominal value, typically 20 ns. The second event that can cause ILIM to return to its nominal value is for an internal timeout to expire. This is illustrated in Figure 26(B) as T3. Here SW never rises to V_{VDD} – 2 V, for whatever reason, and the internal timer times out, releasing the ILIM pin.

Prior to ILIM starting back to its nominal value, overcurrent sensing is not enabled. In normal operation, this ensures that the SW node is at a higher voltage than ILIM when overcurrent sensing starts, avoiding false trips while allowing for a quicker blanking delay than would ordinarily be possible. Placing a capacitor across R_{ILIM} sets an exponential approach to the normal voltage at the ILIM pin. This exponential decay of the overcurrent threshold can be used to compensate for ringing on the SW node after its rising edge and to help compensate for slower-turnon FETs. Choosing the proper capacitance requires care. If the capacitance is too large, the voltage at ILIM does not approach the desired overcurrent level quickly enough, resulting in an apparent shift in overcurrent threshold as pulse duration changes. As a general rule, it is best to make the time constant of the R-C at the ILIM pin 0.2 times or less of the nominal pulse duration of the converter as shown in Equation 17.

Also, the comparator that uses ILIM and SW to determine if an overcurrent condition exists has a clamp on its SW input. This clamp makes the SW node never appear to fall more than 1.4 V (approximately, could be as much as 2 V at –40°C) below V_{VDD}. When ILIM is more than 1.4 V below V_{VDD}, the overcurrent circuit is effectively disabled.

The second-tier protection incorporates a fault counter. The fault counter is incremented on each cycle with an overcurrent pulse and decremented on a clock cycle without an overcurrent pulse. When the counter reaches seven (7), a fault condition is declared by the controller. When this happens, the outputs are placed in a state defined in Table 2. Seven soft-start cycles are initiated (without activity on the HDRV and LDRV outputs) and the PWM is disabled during this period. The counter is decremented on each soft-start cycle. When the counter is decremented to zero, the PWM is re-enabled and the controller attempts to restart. If the fault has been removed, the output starts up normally. If the output is still present, the counter counts seven overcurrent pulses and re-enters the second-tier fault mode. Refer to Figure 27 for typical fault-protection waveforms.

In Equation 13, the minimum short-circuit limit setpoint ($I_{SCP(min)}$) depends on t_{START}, C_{OUT}, V_{OUT}, ripple current in the inductor (I_{RIPPLE}), and the load current at turnon (I_{LOAD}).

$$I_{SCP(min)} > \left(\frac{C_{OUT} \times V_{OUT}}{t_{START}}\right) + I_{LOAD} + \left(\frac{I_{RIPPLE}}{2}\right) \tag{13}$$

The short-circuit limit programming resistor (R_{ILIM}) is calculated from Equation 14.

$$R_{ILIM} = \frac{I_{SCP} \times R_{DS(onMAX)} + V_{ILIM\ (offset)}}{I_{ILIM}}\ \Omega$$

where

- I_{ILIM} is the current into the ILIM pin (110 μA, typical)
- $V_{ILIM(offset)}$ is the offset voltage of the ILIM comparator (–50 mV, typical)
- I_{SCP} is the short-circuit protection current

(14)

To find the range of the overcurrent values, use Equation 15 and Equation 16.

$$I_{SCP(max)} = \frac{1.09 \times I_{ILIM(max)} \times R_{ILIM} - 0.09 \times R_{VDD} \times I_{R_{VDD}} - 0.045\ V + 75\ mV}{R_{DS(ON)min}}\ (A) \tag{15}$$

$$I_{SCP(min)} = \frac{1.09 \times I_{ILIM(min)} \times R_{ILIM} - 0.09 \times R_{VDD} \times I_{R_{VDD}} - 0.045\ V + 30\ mV}{R_{DS(ON)max}}\ (A) \tag{16}$$

Programming (continued)

The TPS40077 provides short-circuit protection only. Therefore, it is recommended that the minimum short-circuit protection level be placed at least 20% above the maximum output current required from the converter. The maximum output of the converter should be the steady state maximum output plus any transient specification that may exist.

The ILIM capacitor maximum value can be found from Equation 17.

$$C_{ILIM(max)} = \frac{V_{OUT} \times 0.2}{V_{IN} \times R_{ILIM} \times f_{SW}} \text{ (Farads)} \quad (17)$$

Note that this is a recommended maximum value. If a smaller value can be used, it should be. For most applications, consider using half the maximum value above.

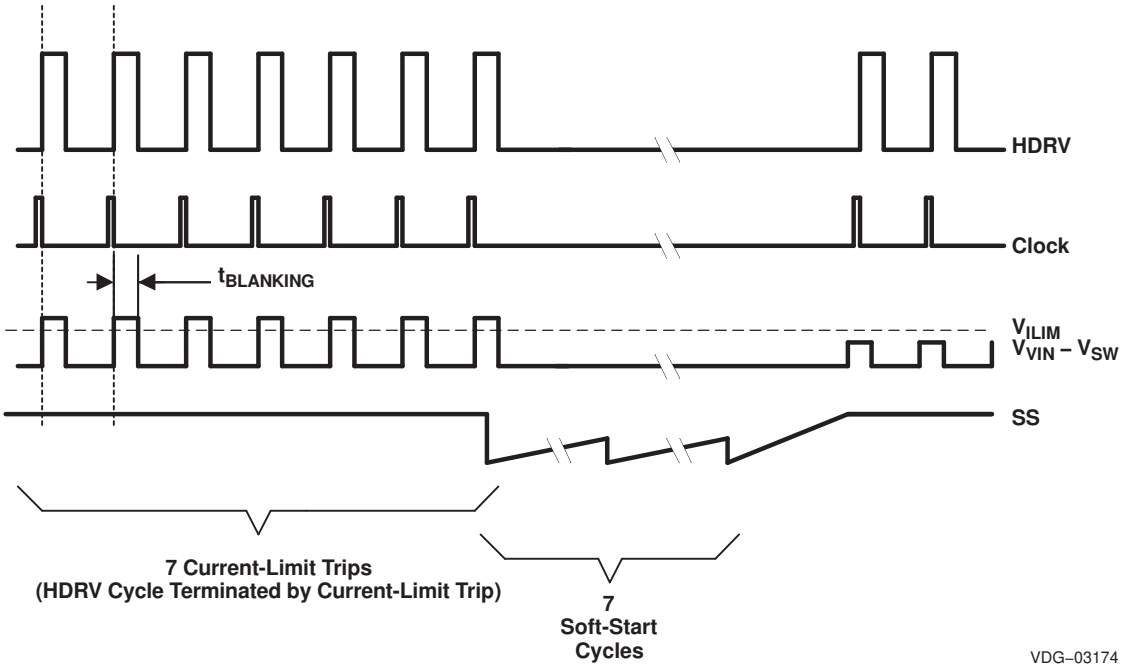


Figure 27. Typical Fault Protection Waveforms

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS40077 allows the user to construct synchronous voltage-mode buck converters with inputs ranging from 4.5 V to 28 V and outputs as low as 700 mV. Predictive Gate Drive circuitry optimizes switching delays for increased efficiency and improved converter output-power capability. Voltage feed-forward is employed to ease loop compensation for wide-input-range designs and provide better line transient response.

The TPS40077 incorporates circuitry to allow startup into a preexisting output voltage without sinking current from the source of the preexisting output voltage. This avoids damaging sensitive loads at start-up. An integrated power-good indicator is available for logic (open-drain) output of the condition of the output of the converter.

8.2 Typical Applications

8.2.1 Buck Regulator 8-V to 16-V Input, 1.8-V Output at 10 A

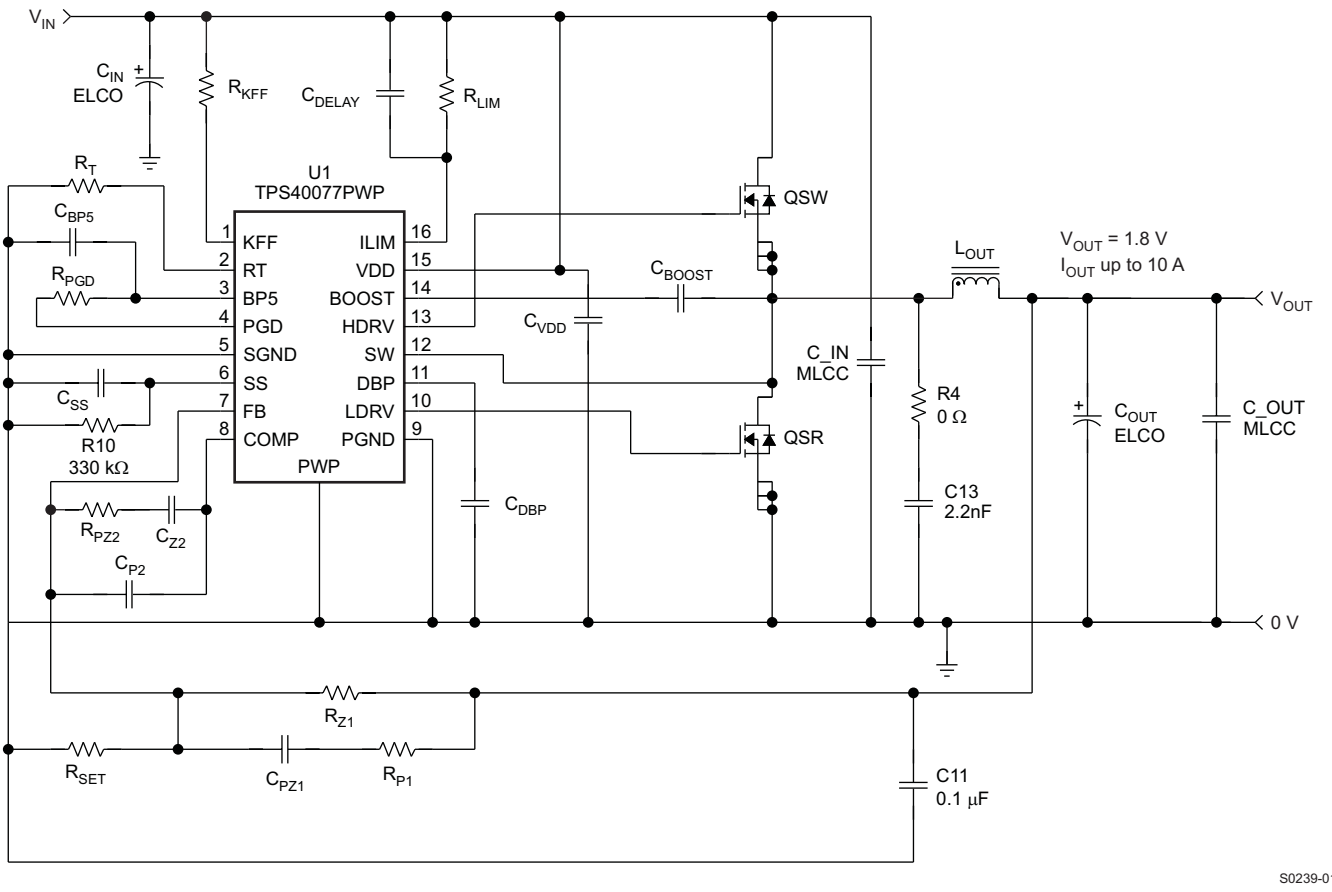


Figure 28. Schematic Diagram

8.2.1.1 Design Requirements

Table 3 lists the design specifications and Table 4 lists the bill of materials for this buck regulator application example.

Typical Applications (continued)

Table 3. Characteristics

PARAMETER		NOTES AND CONDITIONS	MIN	NOM	MAX	UNITS
INPUT CHARACTERSTICS						
V_{IN}	Input voltage		8	12	16	V
I_{IN}	Input current	V_{IN} = NOM, I_{OUT} = MAX		1.8	2	A
	No-load input current	V_{IN} = NOM, I_{OUT} = 0 A		62.6	3.6	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = MIN to MAX	5.4	6	6.6	V
V_{IN_ONV}	Input ONV	I_{OUT} = MIN to MAX	6.3	7	7.7	V
OUTPUT CHARACTERSTICS						
V_{OUT}	Output voltage	V_{IN} = NOM, I_{OUT} = NOM	1.75	1.8	1.85	V
	Line regulation(1)	V_{IN} = MIN to MAX, I_{OUT} = NOM			0.5%	
	Load regulation(1)	V_{IN} = NOM, I_{OUT} = MIN to MAX			0.5%	
V_{OUT_ripple}	Output voltage ripple	V_{IN} = NOM, I_{OUT} = MAX			100	mVpp
I_{OUT}	Output current	V_{IN} = MIN to MAX	0	5	10	A
I_{OCP}	Output overcurrent inception point	V_{IN} = NOM, V_{OUT} = V_{OUT} – 5%	12.25	19.4	34	A
V_{OVP}	Output OVP	I_{OUT} = MIN to MAX	NA	NA	NA	
Transient response						
ΔI	Load step	I_{OUT_Max} to 0.2 × I_{OUT_Max}		8		A
	Load slew rate			10		A/μs
	Overshoot			200		mV
	Settling time			1		ms
SYSTEM CHARACTERSTICS						
f_{SW}	Switching frequency		240	300	360	kHz
η_{pk}	Peak efficiency	V_{IN} = NOM, I_{OUT} = MIN to MAX		90%		
η	Full-load efficiency	V_{IN} = NOM, I_{OUT} = MAX		90%		
T_{op}	Operating temperature range	V_{IN} = MIN to MAX, I_{OUT} = MIN to MAX	–40	25	85	°C
MECHANICAL CHARACTERSTICS						
L	Width			2		Inches
				5.08		cm
W	Length			3		Inches
				7.62		cm
h	Component height			0.41		Inch
				1.04		cm

(1) Voltage accuracy is dependent on resistor tolerance and reference accuracy. Line and load regulation are calculated with respect to the actual set point voltage.

Table 4. Bill of Materials

REFDES	COUNT	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
C1	1	470 μF	Capacitor, aluminum, 470-μF, 25-V, 20%	0.457 x 0.406	EEVFK1E471P	Panasonic
C2, C10	2	0.1 μF	Capacitor, ceramic, 25-V, X7R, 20%	0603	Std	Vishay
C3	1	15 nF	Capacitor, ceramic, 25-V, X7R 20%	0603	Std	Vishay
C4	1	47 pF	Capacitor, ceramic, 25-V, X7R, 20%	0603	Std	Vishay
C5	1	1.8 nF	Capacitor, ceramic, 25-V, X7R 20%	0603	Std	Vishay
C6	1	680 pF	Capacitor, ceramic, 25-V, X7R 20%	0603	Std	Vishay
C7	1	51 pF	Capacitor, ceramic, 25-V, COG 20%	0603	Std	Vishay
C8, C11	2	0.1 μF	Capacitor, ceramic, 25-V, X7R, 20%	0603	Std	Vishay

Table 4. Bill of Materials (continued)

REFDES	COUNT	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
C9	1	1 μF	Capacitor, ceramic, 25-V, X7R, 20%	0805	Std	Vishay
C12, C14, C15	3	22 μF	Capacitor, ceramic, 22-μF, 16-V, X5R, 20%	1812	C4532X5R1C226MT	TDK
C13	1	2.2 nF	Capacitor, ceramic, 25-V, X7R, 20%	0603	Std	Vishay
C16	1	470 μF	Capacitor, aluminum, SM, 6.3-V, 300-mΩ (FC series)	8 × 10	Std	Panasonic
C17	1	47 μF	Capacitor, ceramic, 47-uF, 6.3-V, X5R, 20%	1812	C4532X5R0J476MT	TDK
D1	1	BAT54	Diode, Schottky, 200-mA, 30-V	SOT23	BAT54	Vishay
J1, J2	2	ED1609-ND	Terminal block, 2-pin, 15-A, 5,1-mm	0.40 × 0.35	ED1609	OST
J3	1	PTC36SAAN	Header, 2-pin, 100-mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
L1	1	2.5 μH	Inductor, SMT, 2.5 μH, 16.5-A, 3.4-mΩ	0.515 × 0.516	MLC1550-252ML	Coilcraft
Q1	1	Si7860DP	MOSFET, N-channel, 30-V, 18-A, 8.0-mΩ	PWRPAK S0-8	Si7860DP	Vishay
Q2	1	Si7336ADP	MOSFET, N-channel, 30-V, 18-A, 40-mΩ	PWRPAK S0-8	Si7886ADP	Vishay
Q3	1	FDV301N	MOSFET, N-channel, 25-V, 220-mA, 5-Ω	SOT23	FDV301N	Fairchild
R1	1	10 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R2, R6	2	165 kΩ	Resistor, Chip, 1/16-W, 20%	0603	Std	Std
R3	1	32.4 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R4, R11	2	0 Ω	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R5	1	21.5 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R7	1	51 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R8	1	3.3 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R9	1	1.8 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R10	1	330 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R12	1	51 Ω	Resistor, chip, 1/16-W, 20%	0603	Std	Std
R13	1	1 kΩ	Resistor, chip, 1/16-W, 20%	0603	Std	Std
U1	1	TPS40077PWP	IC, Texas Instruments	PWP16	TPS40077PWP	TI

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Power Train Components

8.2.1.2.1.1 Output Inductor, LOUT

The output inductor is one of the most important components to select. It stores the energy necessary to keep the output regulated when the switch FET is turned off. The value of the output inductor dictates the peak and RMS currents in the converter. These currents are important when selecting other components. Equation 18 can be used to calculate a value for LOUT for this module which operates at a switching frequency (f) of 300 kHz.

$$LOUT = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{V_{IN(max)} - V_{OUT}}{f_s \times I_{RIPPLE}} \quad (18)$$

I_{RIPPLE} is the allowable ripple in the inductor. Select I_{RIPPLE} to be between 20% and 30% of maximum I_{OUT}. For this design, I_{RIPPLE} of 2.5 A was selected. Calculated LOUT is 2.13 μH. A standard inductor with value of 2.5 μH was chosen. This will reduce I_{RIPPLE} by about 17% to 2.07 A.

This I_{RIPPLE} value can be used calculate the rms and peak current flowing in LOUT with Equation 19. Note that this peak current is also seen by the switching FET and synchronous rectifier.

$$I_{LOUT\_RMS} = \sqrt{I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12}} = 10.02\ A \tag{19}$$

The power loss from the selected inductor DCR is 357 mW. The ac core loss for this Coilcraft inductor may be found from the Coilcraft Web site, where there is a loss calculator. The loss is 179 mW calculated with Equation 20.

$$I_{PK} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 11.03\ A \tag{20}$$

The inductor is selected with a saturation current higher than this current plus the current that is developed charging the output capacitance during the soft-start interval.

8.2.1.2.1.2 Output Capacitor, COUT, ELCO and MLCC

Several parameters must be considered when selecting the output capacitor. The capacitance value should be selected based on the output overshoot, V_{OVER}, and undershoot, V_{UNDER}, during a transient load, I_{STEP}, on the converter. The equivalent series resistance (ESR) is chosen to allow the converter to meet the output ripple specification, V_{RIPPLE}. The voltage rating must be greater than the maximum output voltage. Another parameter to consider is equivalent series inductance, which is important in fast-transient load situations. Also, size and technology can be factors when choosing the output capacitor. In this design, a large-capacitance electrolytic type capacitor, COUT ELCO, is used to meet the overshoot and undershoot specifications. Its ESR is chosen to meet the output ripple specification. Smaller multiple-layer ceramic capacitors, COUT MLCC, are used to filter high-frequency noise.

The minimum required capacitance and maximum ESR can be calculated using Equation 21, Equation 22, and Equation 23.

$$COUT = \frac{LOUT \times I_{STEP}^2}{2 \times V_{UNDER} \times D_{max} \times (V_{IN} - V_{OUT})} \tag{21}$$

$$COUT = \frac{LOUT \times I_{STEP}^2}{2 \times V_{OVER} \times V_{OUT}} \tag{22}$$

$$ESR = \frac{V_{RIPPLE}}{I_{RIPPLE}} \tag{23}$$

The capacitance for COUT should be greater than 444 μF, and its ESR should be less than 12 mΩ. The 470-μF/6.3-V capacitor from Panasonic's FC series was chosen. Its ESR is 160 mΩ. MLCCs of 47 μF and 22 μF/16 V are also added in parallel to achieve the required ESR and to reduce high-frequency noise.

8.2.1.2.1.3 Input Capacitor, CIN ELCO and MLCC

The input capacitor is selected to handle the ripple current of the buck stage. Also, a relatively large capacitance is used to keep the ripple voltage on the supply line low. This is especially important where the supply line has high impedance. It is recommended however, that the supply-line impedance be kept as low as possible.

The input-capacitor ripple current can be calculated using Equation 24.

$$I_{CAP(RMS)} = \sqrt{\left[\left(I_{OUT} - I_{IN(AVG)}\right)^2 + \frac{I_{RIPPLE}^2}{12}\right] \times D + I_{IN(AVG)}^2 \times (1 - D)} \tag{24}$$

$I_{IN(AVG)}$ is the average input current. This is calculated simply by multiplying the output dc current by the duty cycle. The ripple current in the input capacitor is 3.3 A. An 1812 MLCC using X5R material has a typical dissipation factor of 5%. For a 22-μF capacitor at 300 kHz, the ESR is approximately 4 mΩ. Two capacitors are used in parallel, so the power dissipation in each capacitor is less than 11 mW.

A 470-μF/16-V electrolytic is added to maintain the voltage on the input rail.

8.2.1.2.1.4 Switching MOSFET, QSW

The following key parameters must be met by the selected MOSFET.

- Drain source voltage, V_{ds}, must be able to withstand the input voltage plus spikes that may be on the switching node. For this design a V_{ds} rating of 30 volts is recommended.
- Drain current, I_D, at 25°C, must be greater than that calculated using Equation 25.

$$I_{QSW(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN(MIN)}} \times \left[I_{OUT(MAX)}^{2} + \frac{I_{RIPPLE}^{2}}{12} \right]} \tag{25}$$

- With the parameters specified, the calculation of $I_{QSW(RMS)}$ should be greater than 5 A.
- Gate source voltage, V_{gs}, must be able to withstand the gate voltage from the control IC. For the TPS40077, this is 11 V.

Once the above boundary parameters are defined, the next step in selecting the switching MOSFET is to select the key performance parameters. Efficiency is the performance characteristic which drives the other selection criteria. Target efficiency for this design is 90%. Based on 1.8-V output and 10 A, this equates to a power loss in the converter of 1.8 W. Based on this figure, a target of 0.6 W dissipated in the switching FET was chosen.

Equation 26 through Equation 29 can be used to calculate the power loss, P_{QSW}, in the switching MOSFET.

$$P_{QSW} = P_{CON} + P_{SW} + P_{GATE} \tag{26}$$

$$P_{CON} = R_{DS(on)} \times I_{QSW(RMS)}^{2} = R_{DS(on)} \times \frac{V_{OUT}}{V_{IN}} \times \left[I_{out}^{2} + \frac{I_{RIPPLE}^{2}}{12} \right] \tag{27}$$

$$P_{SW} = V_{IN} \times f_S \times \left[\frac{\left(I_{OUT} + \frac{I_{RIPPLE}}{2} \right) \times \left(Q_{gs1} + Q_{gd} \right)}{I_g} + \frac{Q_{OSS(SW)} + Q_{OSS(SR)}}{12} \right] \tag{28}$$

$$P_{GATE} = Q_{g(TOT)} \times V_g \times f_{SW} \tag{29}$$

where

P_{CON} = conduction losses
P_{SW} = switching losses
P_{GATE} = gate-drive losses
Q_{gd} = drain-source charge or Miller charge
Q_{gs1} = gate-source post-threshold charge
I_g = gate-drive current
$Q_{OSS(SW)}$ = switching MOSFET output charge
$Q_{OSS(SR)}$ = synchronous MOSFET output charge
$Q_{g(TOT)}$ = total gate charge from zero volts to the gate voltage
V_g = gate voltage

If the total estimated loss is split evenly between conduction and switching losses, Equation 27 and Equation 28 yield preliminary values for $R_{DS(on)}$ and (Q_{gs1} + Q_{gd}). Note output losses due to Q_{OSS} and gate losses have been ignored here. Once a MOSFET is selected, these parameters can be added.

The switching MOSFET for this design should have an $R_{DS(on)}$ of less than 8 mΩ. The sum of Q_{gd} and Q_{gs} should be approximately 4 nC.

It may not always be possible to get a MOSFET which meets both these criteria, so a compromise may be necessary. Also, by selecting different MOSFETs close to these criteria and calculating power loss, the final selection can be made. It was found that the Si7860DP MOSFET from Vishay semiconductor gave reasonable results. This device has an $R_{DS(on)}$ of 8 mΩ and a (Q_{gs1} + Q_{gd}) of 5 nC. The estimated conduction losses are 0.115 W and the switching losses are 0.276 W. This gives a total estimated power loss of 0.391 W versus 0.6 W for our initial boundary condition. Note this does not include gate losses of approximately 71 mW and output losses of 20 mW.

8.2.1.2.1.5 Rectifier MOSFET, QSR

Similar criteria to the foregoing can be used for the rectifier MOSFET. There is one significant difference: due to the body diode conducting, the rectifier MOSFET switches with zero voltage across its drain and source, so effectively with zero switching losses. However, there are some losses in the body diode. These are minimized by reducing the delay time between the transition from the switching MOSFET turnoff to rectifier MOSFET turnon and vice-versa. The TPS40077 incorporates TI's proprietary Predictive Gate Drive circuitry (PGD), which helps reduce these delays to around 10 ns.

To calculate the losses in the rectifier MOSFET, use Equation 30 through Equation 33.

$$P_{QSR} = P_{CON} + P_{BD} + P_{GATE} \tag{30}$$

$$P_{CON} = R_{DS(on)} \times \left[1 - \frac{V_{OUT}}{V_{IN}} - \left(t_1 + t_2\right) \times f_S\right] \times \left[I_{out}^{\ 2} + \frac{I_{RIPPLE}^{\ 2}}{12}\right] \tag{31}$$

$$P_{BD} = V_f \times I_{OUT} \times \left(t_1 + t_2\right) \times f_S \tag{32}$$

$$P_{GATE} = Q_{g(TOTAL)} \times V_g \times \times f_S$$

where

- P_{BD} = body diode losses
- t_1 = body diode conduction prior to turnon of channel = 12 ns for PGD
- t_2 = body diode conduction after turnoff of channel = 12 ns for PGD
- V_f = body diode forward voltage (33)

Estimating the body diode losses based on a forward voltage of 1 V gives 0.072 W. The gate losses are unknown at this time, so assume 0.1-W gate losses. This leaves 0.428 W for conduction losses. Using this figure, a target $R_{DS(on)}$ of 5 mΩ was calculated.

The Si7336ADP from Vishay was chosen. Using the parameters from its data sheet, the actual expected power losses are calculated. Conduction loss is 0.317 W, body diode loss is 0.072 W, and the gate loss is 0.136W. This totals 0.525 W associated with the rectifier MOSFET.

Two other criteria should be verified before finalizing on the rectifier MOSFET. One is the requirement to ensure that predictive gate drive functions correctly. The turnoff delay of the Si7336ADP is 97 ns. The minimum turnoff delay of the Si7860DP is 25 ns. Together these devices meet the 130-ns requirement.

Secondly, the ratio between C_{gs} and C_{gd} should be greater than 1. The Si7336ADP easily meets this criterion. This helps reduce the risk of dv/dt-induced turnon of the rectifier MOSFET. If this is likely to be a problem, a small resistor may be added in series with the boost capacitor, CBOOST.

8.2.1.2.1.6 Timing Resistor, R_T

The timing resistor is calculated using Equation 34.

$$R_T = \frac{1}{f_S \times 17.82 \times 10^{-6}} - 23 \tag{34}$$

This gives a resistor value of 165 kΩ. The nominal frequency using this resistor is 300 kHz.

8.2.1.2.1.7 Feed-Forward and UVLO Resistor, R_{KFF}

A resistor connected to the KFF pin of the IC feeds into the ramp generator. This resistor provides current into the ramp generator proportional to the input voltage. The ramp is then adjusted to compensate for different input voltages. This provides the voltage feed-forward feature of the TPS40077.

The same resistor also sets the undervoltage lockout point. The input start voltage should be used to calculate a value for R_{KFF}. For this module, the minimum input voltage is 8 V; however, due to tolerances in the IC, a start voltage of 10% less than the minimum input voltage is selected. The start voltage for R_{KFF} calculation is 7.2 V. Using Equation 35, R_{KFF} can be selected.

$$R_{KFF} = 0.131 \times R_T \times V_{UVLO(on)} - 1.61 \times 10^{-3} \times V_{UVLO(on)}^{2} + 1.886 \times V_{UVLO} - 1.363 - 0.02 \times R_T - 4.87 \times 10^{-5} \times R_T^{2}$$

where

- R_{KFF} and R_T are in kΩ (35)

Equation 35 gives an R_{KFF} value of 156 kΩ. The closest lower standard value of 154 kΩ should be selected. This gives a minimum start voltage of 7.1 V.

8.2.1.2.1.8 Soft-Start Capacitor, CSS

It is good practice to limit the rise time of the output voltage. This helps prevent output overshoot and possible damage to the load. The selection of the soft-start time is arbitrary. It must meet one condition: it should be greater than the time constant of the output filter, LOUT and COUT. This time is given by Equation 36.

$$t_{START} \geq 2\pi \times \sqrt{LOUT \times COUT} \tag{36}$$

The soft-start time must be greater than 0.23 ms. A time of 0.75 ms was chosen. This time also helps limit the initial input current during start-up so that the peak current plus the capacitor start-up current is less than the minimum short-circuit current. The value of CSS can be calculated using Equation 37.

$$C_{SS} = \frac{I_{SS}}{V_{FB}} \times t_{START} \tag{37}$$

A standard 15-nF MLCC capacitor was chosen. The calculated start time using this capacitor is 0.875 ms.

8.2.1.2.1.9 Short-Circuit Protection, R_{ILIM} and C_{ILIM}

Short-circuit protection is programmed using the R_{ILIM} resistor. Selection of this resistor depends on the $R_{DS(on)}$ of the switching MOSFET selected and the required short-circuit current trip point, I_{SCP}. The minimum I_{SCP} is limited by the inductor peak current, the output voltage, the output capacitor, and the soft-start time. Their relationship is given by Equation 38. A short-circuit current trip point greater than that calculated by Equation 38 should be used.

$$I_{SCP} \geq \frac{COUT \times V_{OUT}}{t_{START}} + I_{PK} \tag{38}$$

The minimum short-circuit current trip point for this design is 12.25 A. This value is used in Equation 39 to calculate the minimum R_{ILIM} value.

$$R_{ILIM} = \frac{I_{SCP} \times R_{DS(on)MAX} + V_{ILIM(Max)}}{I_{LIM(Min)}} \tag{39}$$

R_{ILIM} is calculated to be 1.17 kΩ, and a 1.2-kΩ resistor is used to verify that the short-circuit current requirements are met. The minimum and maximum short-circuit current can be calculated using Equation 40 and Equation 41.

$$I_{SCP(MIN)} = \frac{I_{ILIM(MIN)} \times R_{ILIM(MIN)} - V_{ILIM(MAX)}}{R_{DS(on)MAX}} \tag{40}$$

$$I_{SCP(MAX)} = \frac{I_{ILIM(MAX)} \times R_{ILIM(MAX)} - V_{ILIM(MIN)}}{R_{DS(on)MIN}} \tag{41}$$

where: $V_{ILIM(MAX)}$ and $V_{ILIM(MIN)}$ are maximum and minimum voltages across the high side FET when it is turned on, taking into account temperature variations.

The minimum I_{SCP} is 12.25 A, and the maximum is 34 A.

It is also recommended to add a small capacitor, C_{ILIM}, across R_{ILIM}. The value of this capacitor should be about half the value calculated in Equation 42.

$$C_{ILIM(Max)} = \frac{V_{OUT} \times 0.2}{V_{IN} \times R_{ILIM} \times f_S} \quad (42)$$

This equation yields a maximum C_{ILIM} as 55 pF. A smaller value of 27 pF is chosen is chosen.

8.2.1.2.1.10 Boost Voltage, CBOOST and DBOOST (Optional)

To be able to drive an N-channel MOSFET in the switch location of a buck converter, a capacitor charge pump or boost circuit is required. The TPS40077 contains the elements for this boost circuit. The designer must only add a capacitor, CBOOST, from the switch node of the buck power stage to the BOOST pin of the IC. Selection of this capacitor is based on the total gate charge of the switching MOSFET and the allowable ripple on the boost voltage, ΔV_{BOOST}. A ripple of 0.2 V is assumed for this design. Using these two parameters and Equation 43, the minimum value for CBOOST can be calculated.

$$CBOOST > \frac{Q_{g(TOTAL)}}{\Delta V_{BOOST}} \quad (43)$$

The total gate charge of the switching MOSFET is 23 nC. A minimum CBOOST of 0.092 µF is required. A 0.1 µF capacitor was chosen. This capacitor must be able to withstand the maximum input voltage plus the maximum voltage on DBP. This is 13.2 V plus 9.0 V, which is 22.2 V. A 50-V capacitor is used.

To reduce losses in the TPS40077 and to increase the available gate voltage for the switching MOSFET, an external diode can be added between the DBP pin and the BOOST pin of the IC. A small-signal Schottky diode should be used here, such as the BAT54.

8.2.1.2.1.11 Closing the Feedback Loop, R_{Z1}, R_{P1}, R_{PZ2}, R_{SET1}, R_{SET2}, C_{Z2}, C_{P2}, and C_{PZ1}

A graphical method is used to select the compensation components. This is a standard feed-forward buck converter. Its PWM gain is given by Equation 44.

$$K_{PWM} \cong \frac{V_{UVLO}}{1\ V} \quad (44)$$

The ramp voltage is 1 V at the UVLO voltage. Because of the feed-forward compensation, the programmed UVLO voltage is the voltage that sets the PWM gain.

The gain of the output LC filter is given by Equation 45.

$$K_{LC} = \frac{1 + s \times ESR \times COUT}{1 + s \times \frac{LOUT}{ROUT} + s^2 \times LOUT \times COUT} \quad (45)$$

The PWM and LC gain is Equation 46.

$$G_c(s) = K_{PWM} \times K_{LC} \times \frac{V_{UVLO}}{1\ V} \times \frac{1 + s \times ESR \times COUT}{1 + s \times \frac{LOUT}{ROUT} + s^2 \times LOUT \times COUT} \quad (46)$$

To plot this on a Bode plot, the dc gain must be expressed in dB. The dc gain is equal to KPWM. To express this in dB, take its logarithm and multiply by 20. For this converter, the dc gain is Equation 47.

$$DCGAIN = 20 \times \log\left[\frac{V_{UVLO}}{V_{RAMP}}\right] = 20 \times \log(7) = 16.9\ dB \quad (47)$$

Also, the pole and zero frequencies should be calculated. A double pole is associated with the LC and a zero is associated with the ESR of the output capacitor. The frequencies where these occur can be calculated using Equation 48 and Equation 49.

$$f_{LC\_Pole} = \frac{1}{2\pi \times \sqrt{LOUT \times COUT}} = 4.3\ kHz \quad (48)$$

$$f_{ESR\_Zero} = \frac{1}{2\pi \times ESR \times COUT} = 2.1\ kHz \quad (49)$$

These are shown in the Bode plot of Figure 29.

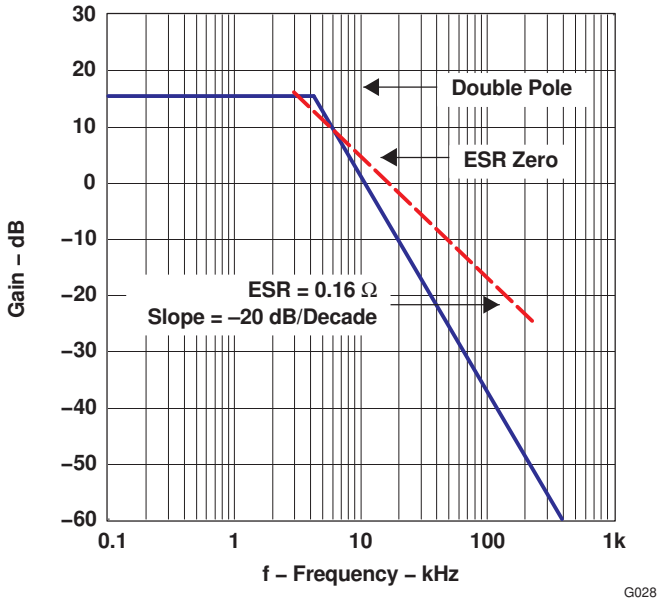


Figure 29. PWM and LC Filter Gain

The next step is to establish the required compensation gain to achieve the desired overall system response. The target response is to have the crossover frequency between 1/9 and 1/5 times the switching frequency, in order to have a phase margin greater than 45° and a gain margin greater than 6 dB.

A type-III compensation network, shown in Figure 30, was used for this design. This network gives the best overall flexibility for compensating the converter.

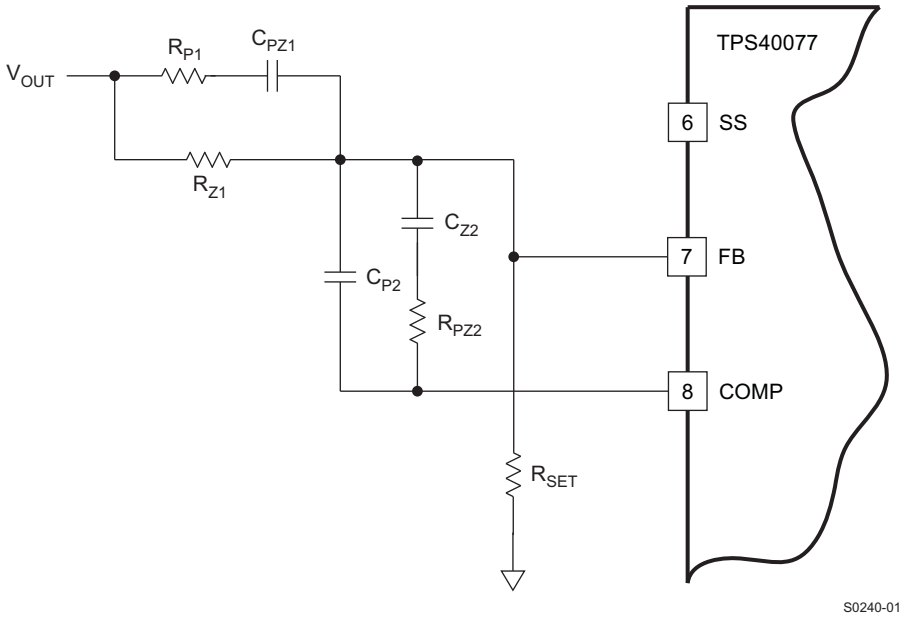


Figure 30. Type-III Compensation With the TPS40077

A typical Bode plot for this type of compensation network is shown in Figure 31.

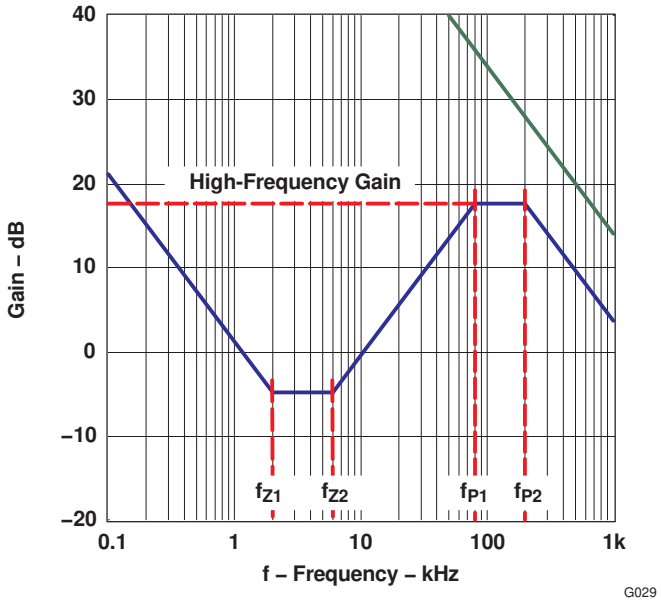


Figure 31. Type-III Compensation Typical Bode Plot

The high-frequency gain and the break (pole and zero) frequencies are calculated using Equation 50 through Equation 55.

$$VOUT = VREF \times \frac{R_{Z1} + R_{SET}}{R_{SET}} \tag{50}$$

$$GAIN = R_{PZ2} \times \frac{R_{Z1} + R_{P1}}{R_{Z1} \times R_{P1}} \tag{51}$$

$$f_{P1} = \frac{1}{2\pi \times R_{P1} \times C_{PZ1}} \tag{52}$$

$$f_{P2} = \frac{C_{P2} + C_{Z2}}{2\pi \times R_{PZ2} \times C_{P2} \times C_{Z2}} \approx \frac{1}{2\pi \times R_{PZ2} \times C_{P2}} \tag{53}$$

$$f_{Z1} = \frac{1}{2\pi \times R_{Z1} \times C_{PZ1}} \tag{54}$$

$$f_{Z2} = \frac{1}{2\pi \times \left(R_{PZ2} + R_{P1}\right) \times C_{Z2}} \approx \frac{1}{2\pi \times R_{PZ2} \times C_{Z2}} \tag{55}$$

Looking at the PWM and LC bode plot, there are a few things which must be done to achieve stability.

1. Place two zeros close to the double pole, e.g., $f_{Z1} = f_{Z2} = 4.3$ kHz
2. Place both poles well above the crossover frequency. The crossover frequency was selected as one sixth the switching frequency, $f_{co1} = 50$ kHz, $f_{P1} = 66$ kHz
3. Place the second pole at three times f_{co1}. This ensures that the overall system gain falls off quickly to give good gain margin, $f_{p2} = 150$ kHz
4. The high-frequency gain should be sufficient to ensure 0 dB at the required crossover frequency, GAIN = –1 × gain of PWM and LC at the crossover frequency, GAIN = 16.9 dB

Using these values and Equation 50 through Equation 55, the Rs and Cs around the compensation network can be calculated.

1. Set $R_{Z1} = 51$ kΩ
2. Calculate R_{SET} using Equation 50, $R_{SET} = 32.4$ kΩ
3. Using Equation 54 and $f_{z1} = 4.3$ kHz, C_{PZ1} can be calculated to be 726 pF, C_{PZ1}= 680 pF

4. f_{P1} and Equation 52 yields R_{P1} to be a standard value of 3.3 kΩ.
5. The required gain of 16.9 dB and Equation 51 sets the value for R_{PZ2}. R_{PZ2} = 21.5 kΩ.
6. C_{Z2} is calculated using Equation 55 and the desired frequency for the second zero, C_{Z2} = 1.7 nF, or using standard values, 1.8 nF.
7. Finally, C_{P2} is calculated using the second pole frequency and Equation 53; C_{P2} = 47 pF.

Using these values, the simulated results are 57° of phase margin at 54 kHz.

8.2.1.3 Application Curves

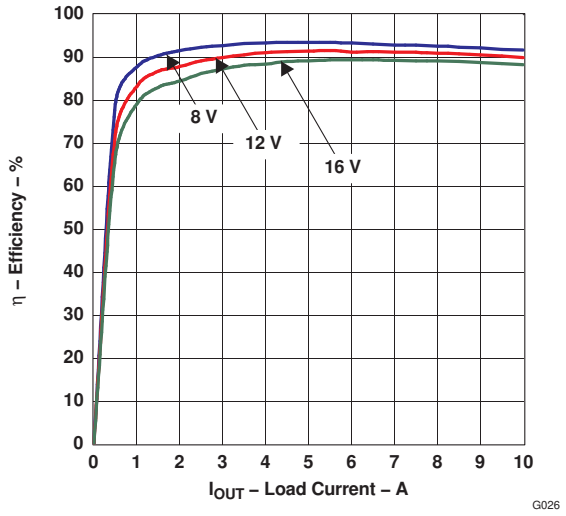


Figure 32. Module Efficiency, 8 V, 12 V, and 16 V In, 0 to 10 A Out

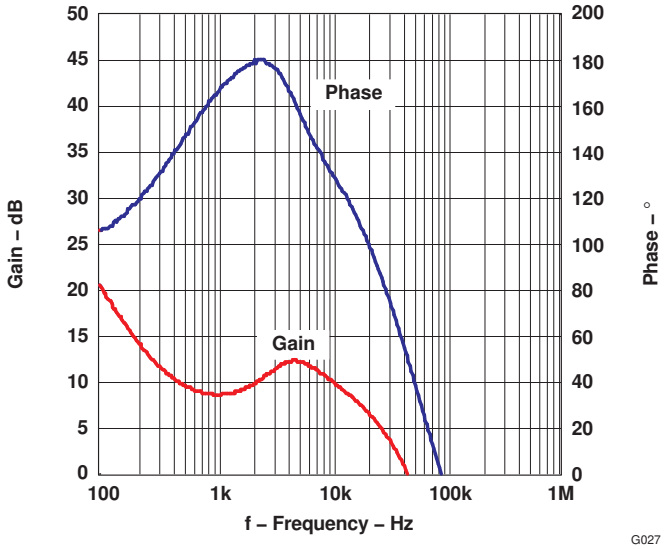


Figure 33. Bode Plot Showing 57° Phase Margin at Crossover Frequency of 54 kHz

8.3 Additional System Examples

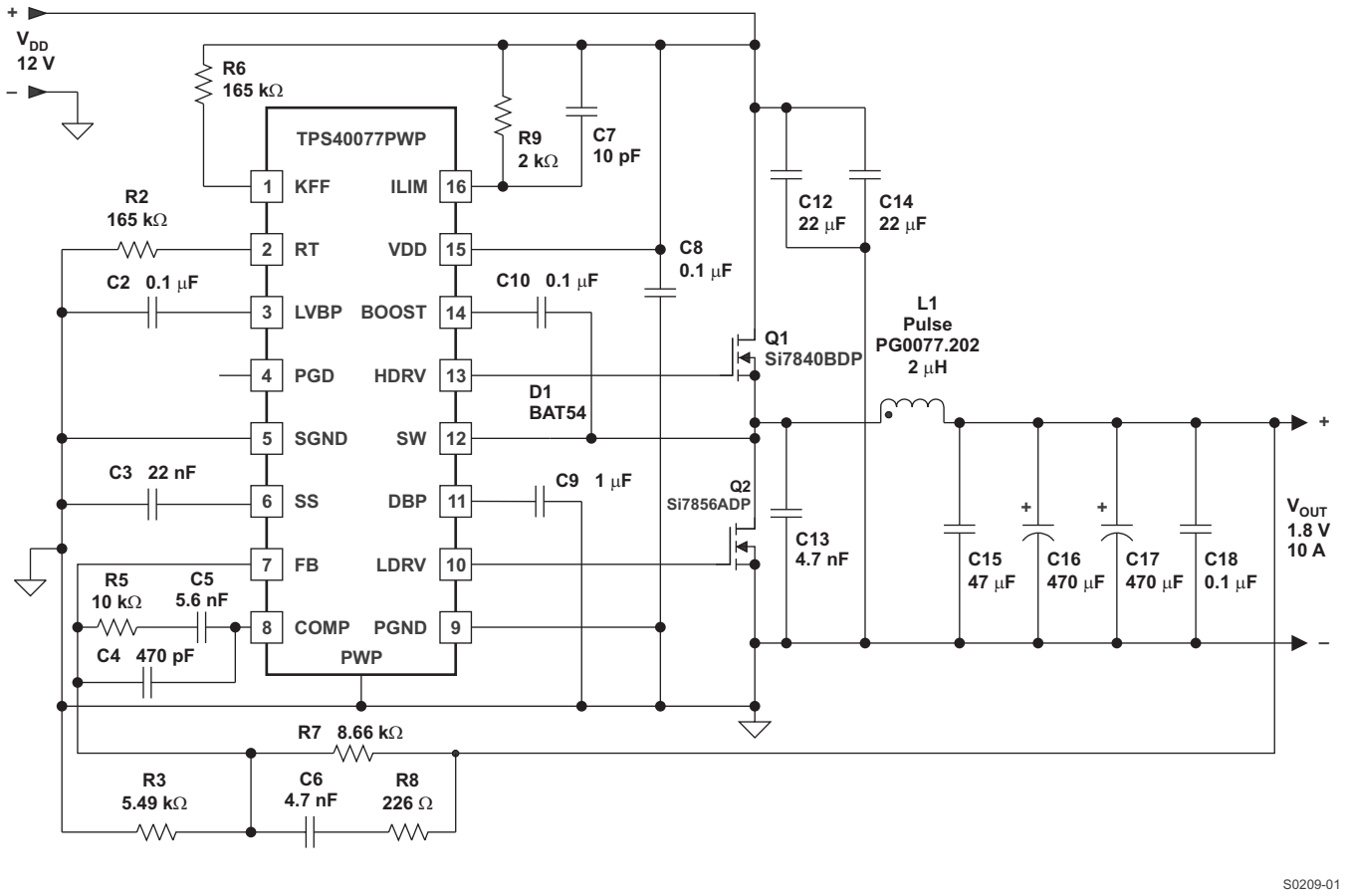
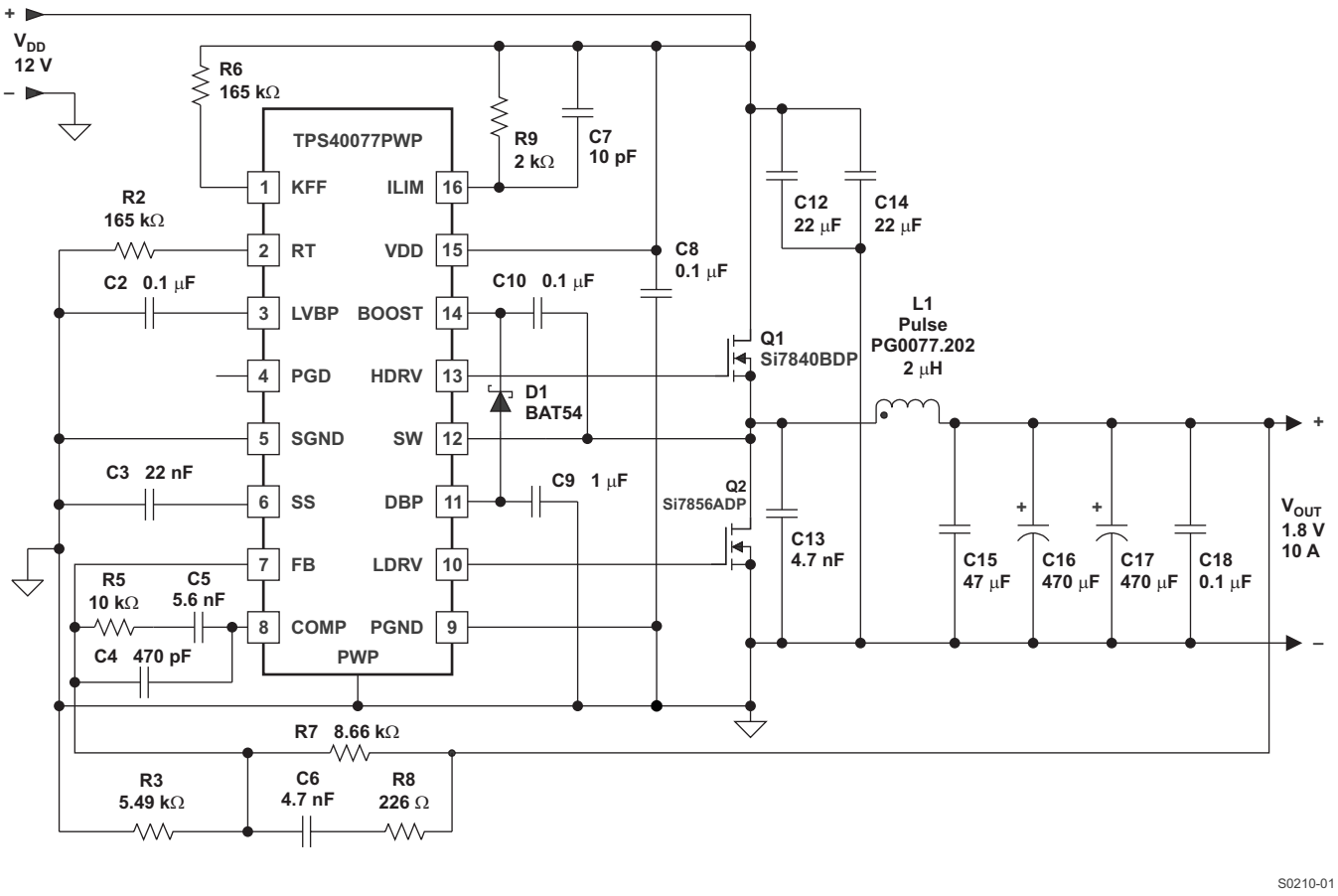


Figure 34. 300 kHz, 12 V to 1.8 V

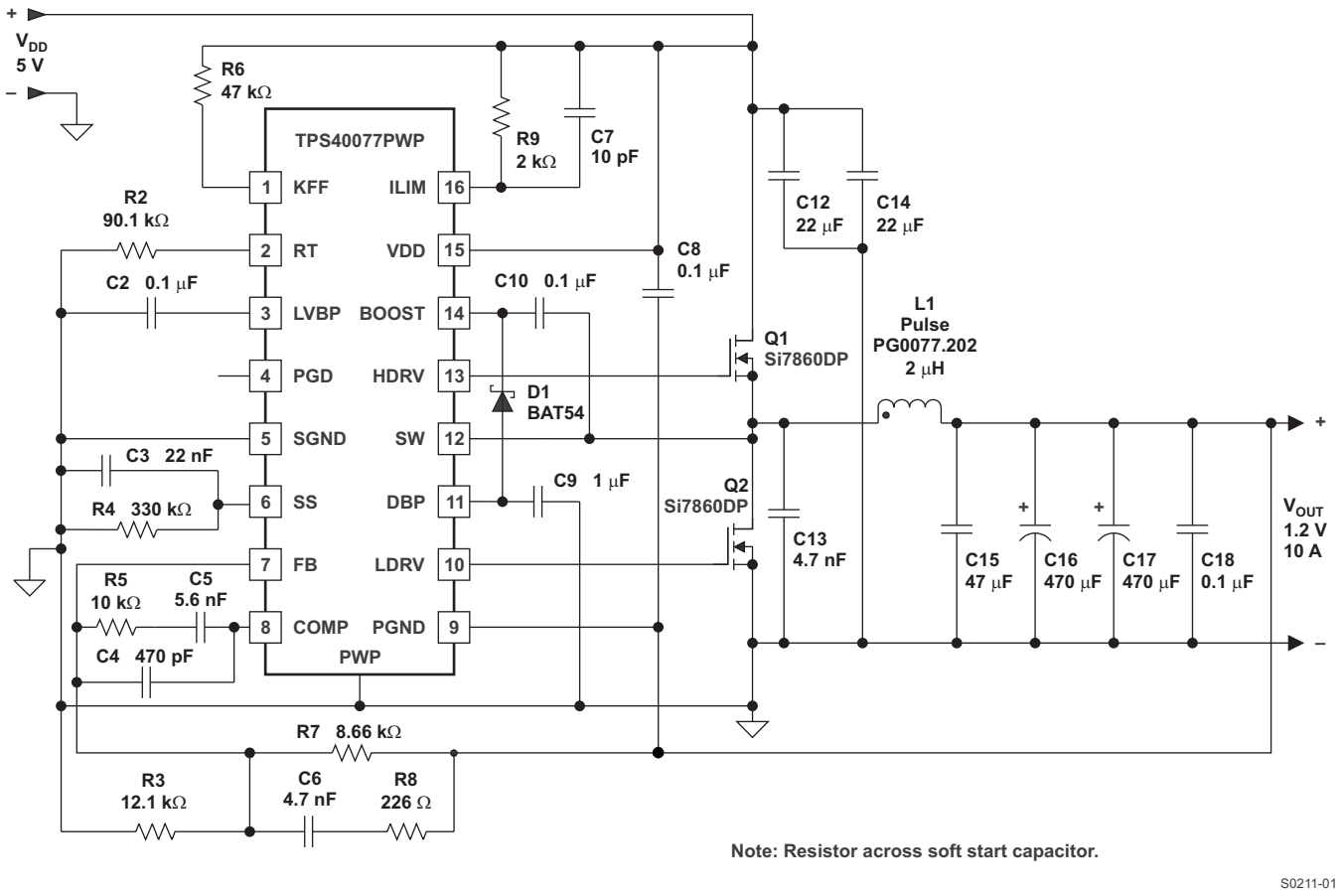
Additional System Examples (continued)



See *Boost Diode*.

Figure 35. 300 kHz, 12 V to 1.8 V With Improved High-Side Gate Drive

Additional System Examples (continued)



See *Boost Diode*.

Figure 36. 500 kHz, 5 V to 1.2 V With Improved High-Side Gate Drive

9 Layout

9.1 Layout Guidelines

The TPS40077 provides separate signal ground (SGND) and power ground (PGND) pins. Take care to properly separation of the circuit grounds. Each ground must consist of a plane to minimize its impedance, if possible. The high-power *noisy* circuits such as the output, synchronous rectifier, MOSFET driver decoupling capacitor (DBP), and the input capacitor should be connected to PGND plane.

Connect sensitive nodes such as the FB resistor divider and RT to the SGND plane. The SGND plane must only make a single-point connection to the PGND plane. TI recommends that the SGND pin be tied to the copper area for the thermal pad underneath the chip. Tie the PGND to the thermal-pad copper area as well, and make the connection to the power circuit ground from the PGND pin. Reference the output voltage divider to the SGND pin.

Component placement must ensure that bypass capacitors (LVPB and DBP) are located as close as possible to their respective power and ground pins. Also, sensitive circuits such as FB, RT and ILIM should not be located near high-dv/dt nodes such as HDRV, LDRV, BOOST, and the switch node (SW). Failure to follow careful layout practices results in suboptimal operation. More detailed information can be found in the TPS40077EVM user's guide (SLVU192).

10 器件和文档支持

10.1 器件支持

10.1.1 第三方产品免责声明

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10.2 文档支持

10.2.1 相关文档

请参阅如下相关文档：

- *《PowerPAD 耐热增强型封装》*，SLMA002
- *《TPS40190 低引脚数同步降压控制器》*，SLUS658
- *《具有高级排序功能和输出裕量的 TPS40100 中端输入同步控制器》*，SLUS601
- *《具有电压前馈功能的 TPS40075 中端输入同步降压控制器》*，SLUS676
- *《TPS40057 宽输入同步降压控制器》*，SLUS593
- *《使用 TPS40077EVM 12V 输入、1.8V 输出、10A 同步降压转换器》*，SLVU192

10.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.5 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

10.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

10.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS40077PWP	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40077
TPS40077PWP.A	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40077
TPS40077PWPR	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40077
TPS40077PWPR.A	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40077
TPS40077PWPRG4	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40077

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

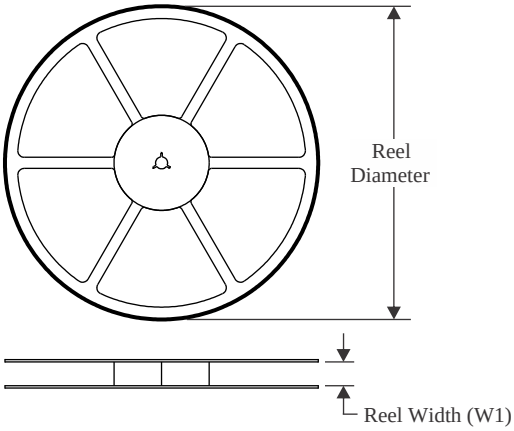
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

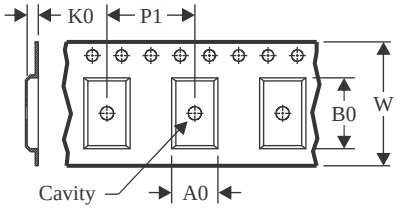
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

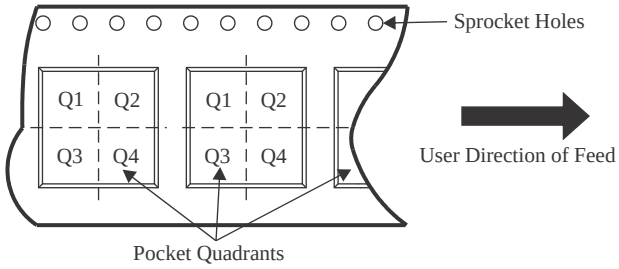


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

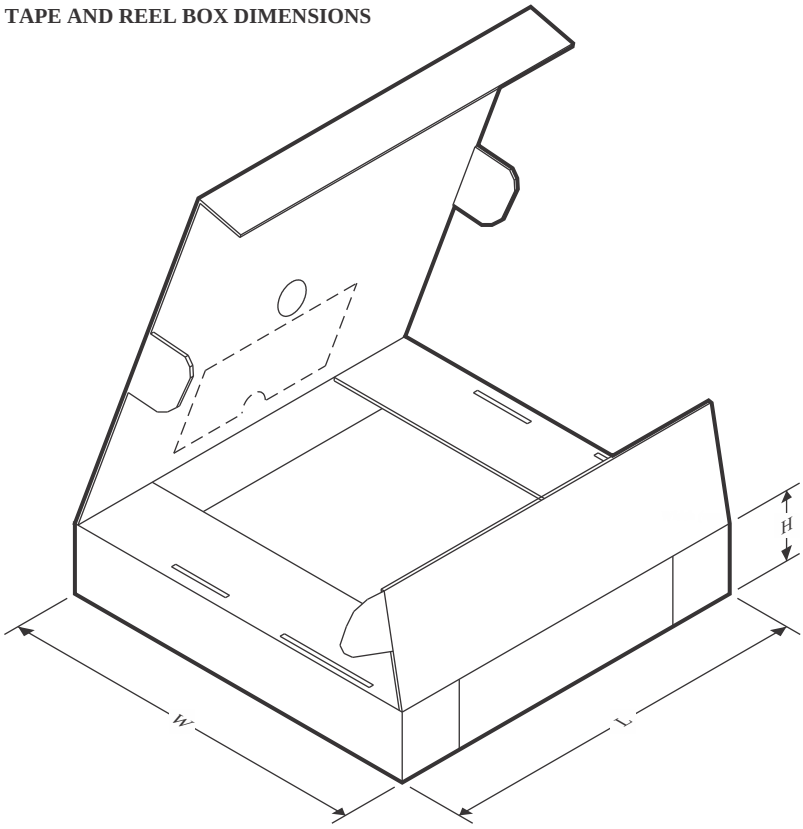
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40077PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

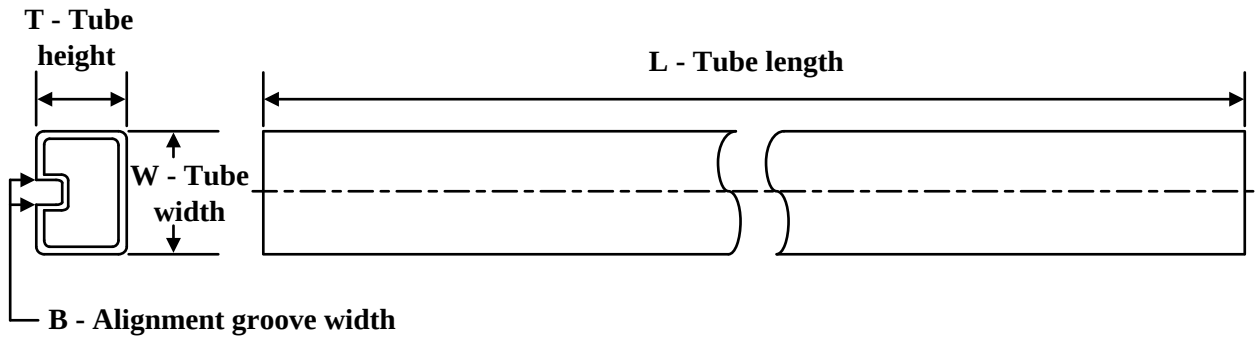
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40077PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0

TUBE

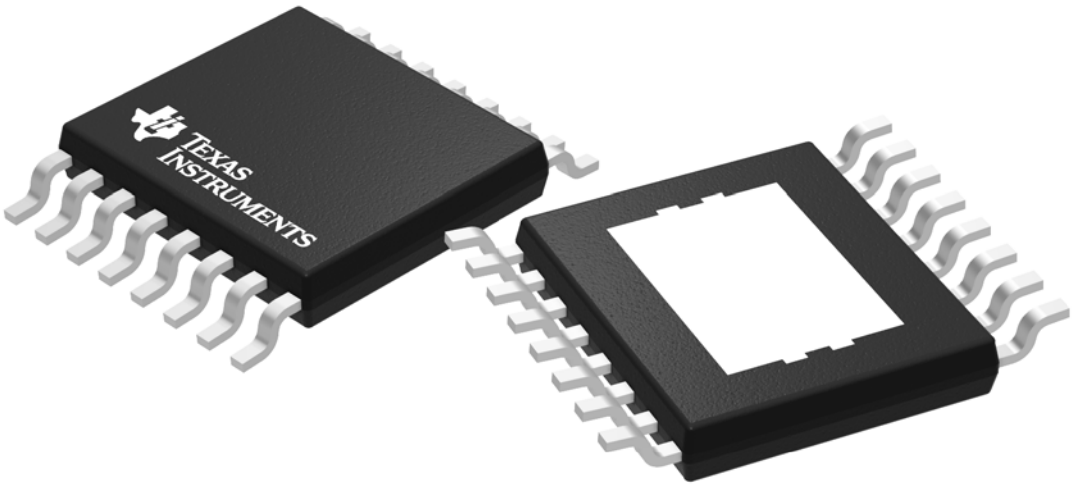


*All dimensions are nominal

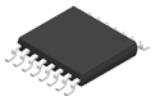
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS40077PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS40077PWP.A	PWP	HTSSOP	16	90	530	10.2	3600	3.5

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

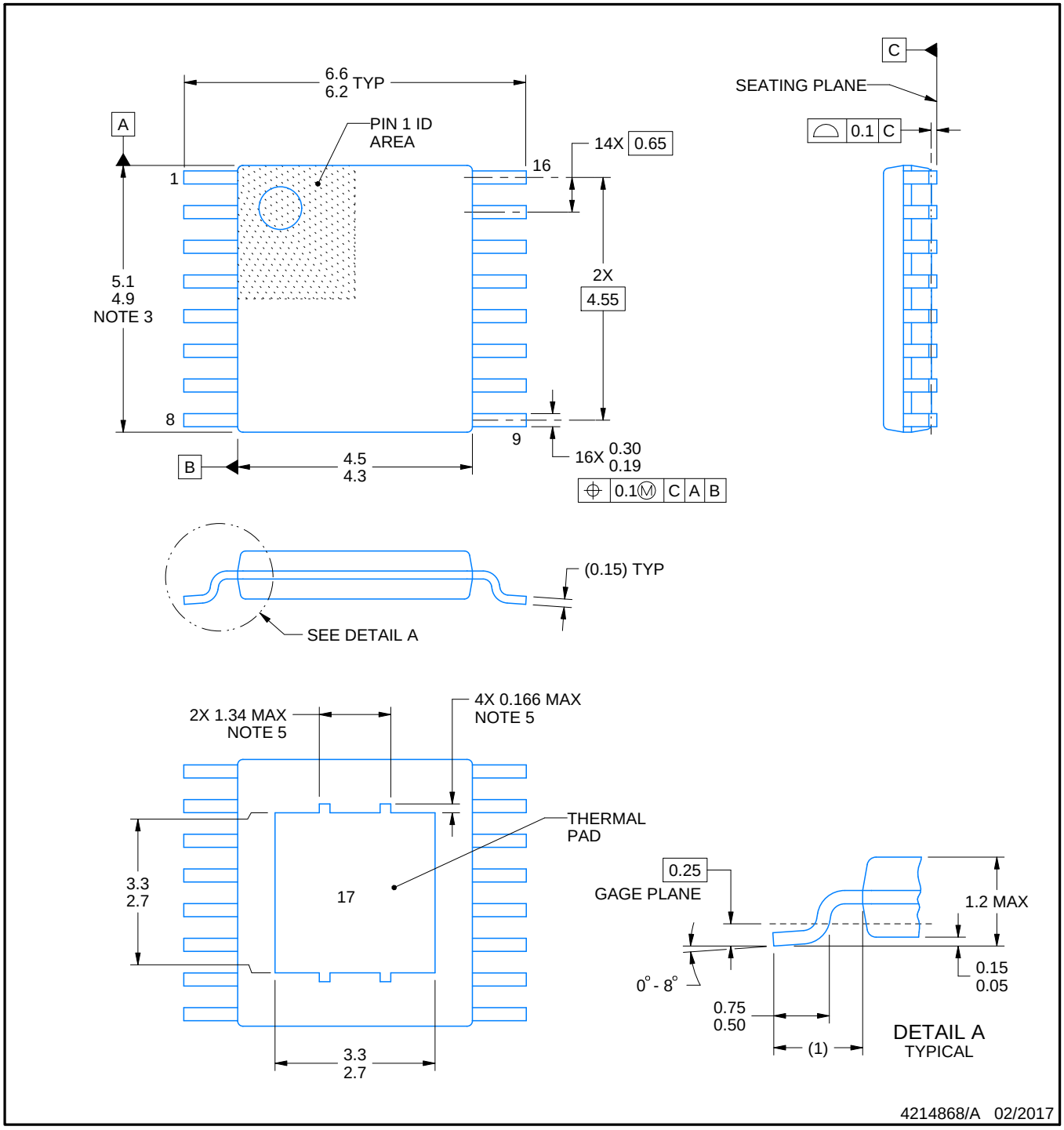


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

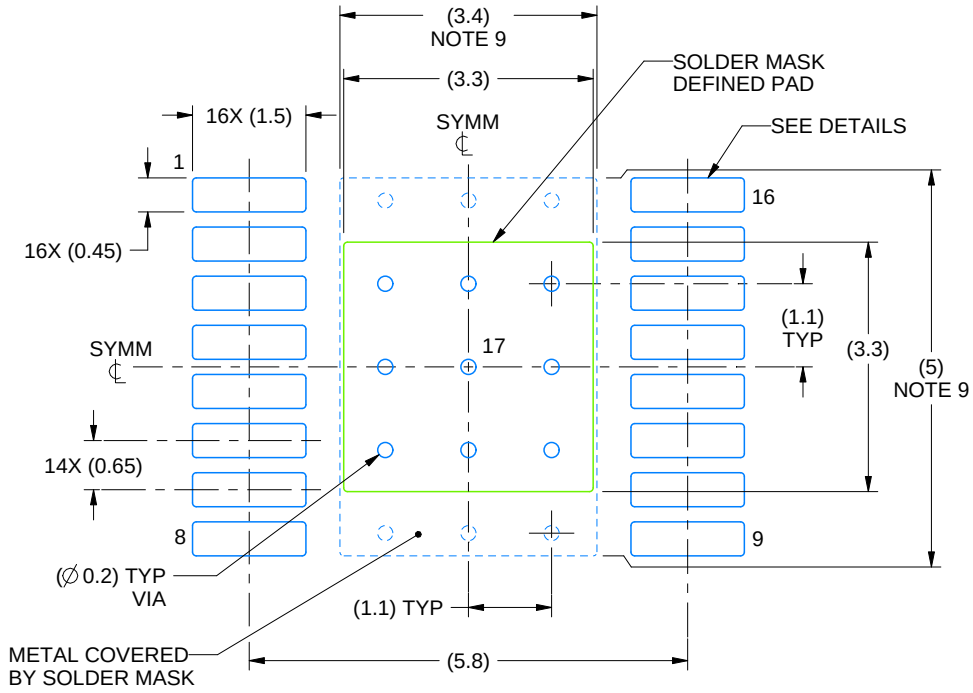
PLASTIC SMALL OUTLINE



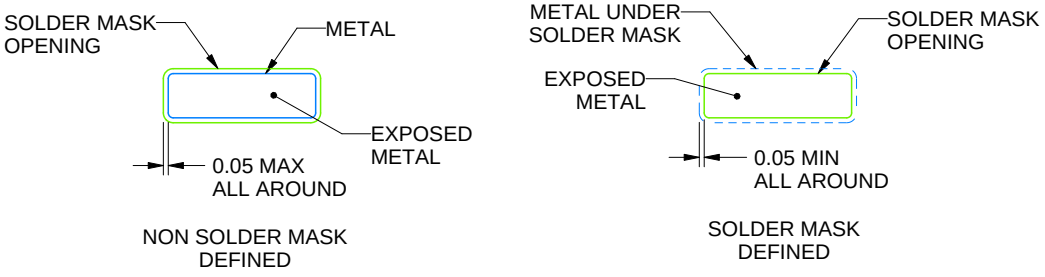
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

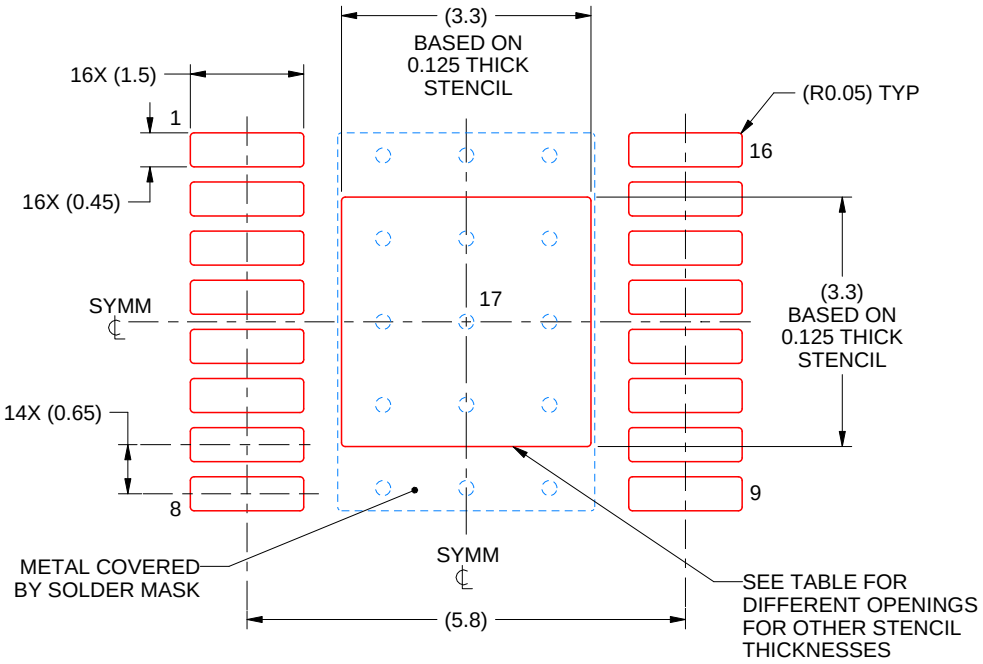


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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