TPS386596 Quad Reset Supervisor With Manual Reset Input

1 Features

- Four Channel Voltage Detector
- Threshold Accuracy: 0.25% (typ)
- Fixed 50-ms $\overline{\text{RESET}}$ Delay Time
- Active-Low Manual Reset Input
- Very Low Quiescent Current: 7 µA (Typical)
- SVS-1: Fixed Threshold for Monitoring 3.3 V
- SVS-2/3/4: Adjustable Threshold Down to 0.4 V
- Open-Drain $\overline{\text{RESET}}$ Output
- Space-Saving, 8-pin MSOP Package

2 Applications

- Notebook/Desktop Computers
- Industrial Equipment
- Telecom, Networking Infrastructure
- Server, Storage Equipment
- DSP and Microcontroller Applications
- FPGA/ASIC Applications

3 Description

The TPS386596 device monitors four power rails and asserts the $\overline{\text{RESET}}$ signal when any of the SENSE inputs drop below the respective thresholds. SVS-1 can be used to monitor a 3.3-V nominal power supply with no external components required. SVS-2, SVS-3, and SVS-4 are adjustable using external resistors and can be used to monitor any power-supply voltage higher than 0.4 V. All SENSE inputs have a threshold accuracy of 0.25% (typical). The TPS386596L33 also has an active-low manual reset ($\overline{\text{MR}}$) that can assert the $\overline{\text{RESET}}$ signal as desired by the application. The open-drain, active-low $\overline{\text{RESET}}$ output deasserts after a fixed 50-ms delay.

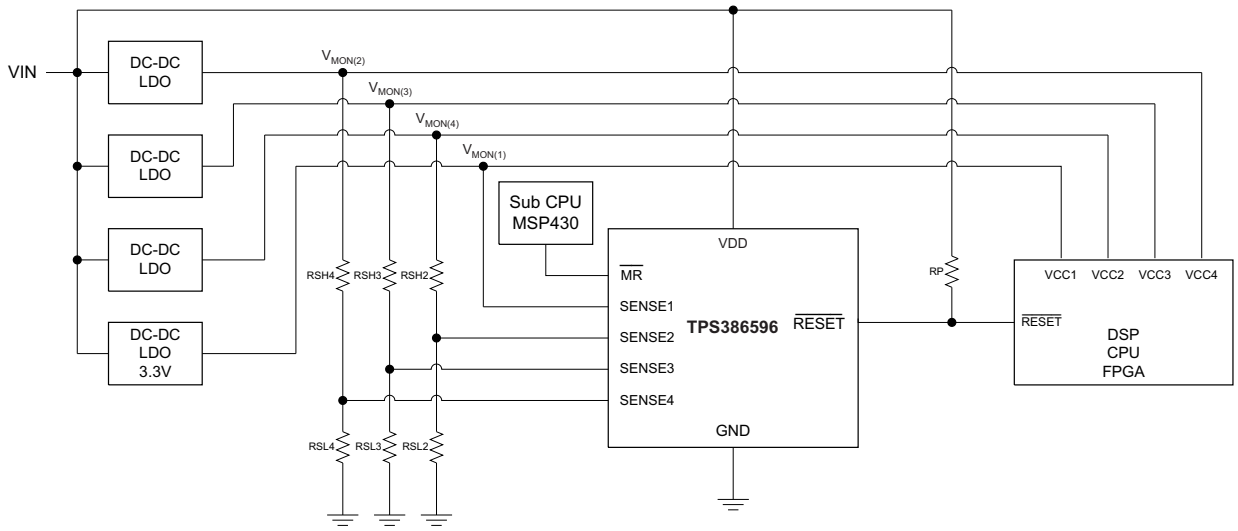
The TPS386596 has a low quiescent current of 7 µA (typical) and is available in a space-saving, 8-pin MSOP package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS386596	VSSOP (8)	5.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TPS386596 Typical Application Circuit



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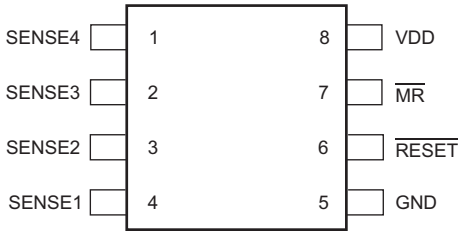
4 Revision History

Changes from Original (July 2010) to Revision A **Page**

- Changed references to *TPS386596L33* to *TPS386596* throughout document ... 1
- Changed *Pin Configuration and Functions* section; updated table format and pin drawing ... 3
- Changed "free-air temperature" to "junction temperature" in *Absolute Maximum Ratings* condition statement ... 4
- Changed *Absolute Maximum Ratings* table; moved ESD ratings to separate table ... 4
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4
- Changed *Thermal Information* table; updated thermal resistance values ... 4
- Changed *Electrical Characteristics* table; moved timing and switching parameters (t_W, t_D) to separate tables ... 5
- Changed input voltage range notation from V_{VCC} to V_{DD} throughout *Electrical Characteristics* table ... 5
- Changed supply current notation from I_{VCC} to I_{DD} in *Electrical Characteristics* table ... 5
- Changed *VCC* notation in *Functional Block Diagram* to *VDD* ... 10
- Deleted *Immunity to SENSE Pin Voltage Transients* section; rewrote content and added to *Voltage Monitoring* section ... 11
- Changed *Sense Inputs* section title to *Undervoltage Detection* ... 12
- Changed title and graphic for Figure 14 ... 12

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION	
NAME	NO.			
GND	5	—	Ground	
MR	7	I	Manual reset input with internal 100-kΩ pullup to VDD and 50-ns deglitch. Logic low level of this pin asserts RESET.	
RESET	6	O	RESET is an open-drain output pin. When RESET is asserted, this pin remains in a low-impedance state. When RESET is deasserted, this pin goes to a high-impedance state after 50 ms. A pullup resistor to VDD or another voltage source is required.	
SENSE1	4	I	Monitor voltage input for Supply 1	When the voltage at this terminal drops the threshold voltage (VIT1= 2.9 V), RESET is asserted.
SENSE2	3	I	Monitor voltage input for Supply 2	When the voltage at this terminal drops the threshold voltage (VIT2= 0.4 V), RESET is asserted.
SENSE3	2	I	Monitor voltage input for Supply 3	When the voltage at this terminal drops the threshold voltage (VIT3= 0.4 V), RESET is asserted.
SENSE4	1	I	Monitor voltage input for Supply 4	When the voltage at this terminal drops the threshold voltage (VIT4= 0.4 V), RESET is asserted.
VDD	8	I	Supply voltage. Connecting a 0.1-µF ceramic capacitor close to this pin is recommended.	

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted).(1) (2)

		MIN	MAX	UNIT
Voltage	Input, V_{DD}	–0.3	7	V
	$V_{\overline{MR}}$, V_{SENSE1}, V_{SENSE2}, V_{SENSE3}, V_{SENSE4}, $V_{\overline{RESET}}$	–0.3	7	V
Current	$\overline{RESET}$ pin		5	mA
Power dissipation	Continuous total	See *Thermal Information*		
Temperature	Operating virtual junction, T_J	–40	150	°C
	Operating ambient, T_A	–40	125	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted).

	MIN	NOM	MAX	UNIT
V_{DD}	1.8		6.5	V
V_{SENSE} (1)	0		V_{DD}	V
V_{MR}	0		V_{DD}	V
$V_{\overline{RESET}}$	0		6.5	V
$R_{PULL-UP}$	6.5	100	10,000	kΩ
T_J	–40	25	125	°C

(1) All sense inputs.

6.4 Thermal Information

THERMAL METRIC(1)		TPS386596 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	174	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	92.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to 125°C. 1.8 V < V_{DD} < 6.5 V, R $\overline{\text{RESET}}$ = 100 kΩ to V_{DD}, C $\overline{\text{RESET}}$ = 50 pF to GND, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input supply		1.8		6.5	V
I_{DD}	Supply current (current into VDD pin)	V_{CC} = 3.3 V, $\overline{\text{RESET}}$ not asserted		7	19	µA
		V_{CC} = 6.5 V, $\overline{\text{RESET}}$ not asserted		7.5	22	µA
	Power-on reset voltage(1) (2)	$V_{OL(max)}$ = 0.2 V, I $\overline{\text{RESET}}$ = 15 µA			0.9	V
V_{ITn}	Negative-going input threshold accuracy	SENSE1	2.87	2.90	2.93	V
		SENSE2, SENSE3, SENSE4	396	400	404	mV
V_{HYS}	Hysteresis (positive-going) on V_{ITn}	SENSE1		25	72	mV
		SENSE2, SENSE3, SENSE4		3.5	10	mV
I_{SENSE1}	Input current at SENSE1	VSENSE1 = 3.3 V	2.2	2.75	3.3	µA
I_{SENSEn}	Input current at SENSEn pin, n = 2, 3, 4	VSENSEn = 0.42 V	–25		25	nA
t_d	$\overline{\text{RESET}}$ delay time		30	50	70	ms
V_{IL}	$\overline{\text{MR}}$ logic low input		0		$0.3V_{DD}$	V
V_{IH}	$\overline{\text{MR}}$ logic high input		$0.7V_{DD}$			V
R_{MR_Pullup}	Internal pullup resistor on $\overline{\text{MR}}$ pin to V_{DD}			100		kΩ
V_{OL}	Low-level $\overline{\text{RESET}}$ output voltage	I_{OL} = 1 mA			0.4	V
		SENSEn = 0 V, 1.3 V < V_{DD} < 1.8 V, I_{OL} = 0.4 mA(1)			0.3	
I_{LKG}	$\overline{\text{RESET}}$ leakage current	V $\overline{\text{RESET}}$ = 6.5 V, $\overline{\text{RESET}}$ not asserted	–300		300	nA
C_{IN}	Input pin capacitance			5		pF

(1) These specifications are out of recommended V_{DD} range and only define $\overline{\text{RESET}}$ output performance during V_{DD} ramp up.
(2) The lowest supply voltage (V_{DD}) at which $\overline{\text{RESET}}$ becomes active. $t_{RISE(VDD)}$ ≥ 15 µs/V.

6.6 Timing Requirements

Over the operating temperature range of T_J = –40°C to 125°C. 1.8 V < V_{DD} < 6.5 V, R $\overline{\text{RESET}}$ = 100 kΩ to V_{DD}, C $\overline{\text{RESET}}$ = 50 pF to GND, unless otherwise noted. Typical values are at T_J = 25°C.

			MIN	NOM	MAX	UNIT
t_W	Input pulse width to SENSEn and $\overline{\text{MR}}$ pins	SENSEm: 1.05 V_{IT} ≥ 0.95 V_{IT}		4		µs
		$\overline{\text{MR}}$: 0.7 V_{DD} ≥ 0.3 V_{DD}		50		ns

6.7 Switching Characteristics

Over the operating temperature range of T_J = –40°C to 125°C. 1.8 V < V_{DD} < 6.5 V, R $\overline{\text{RESET}}$ = 100 kΩ to V_{DD}, C $\overline{\text{RESET}}$ = 50 pF to GND, unless otherwise noted. Typical values are at T_J = 25°C.

		MIN	TYP	MAX	UNIT
t_D	$\overline{\text{RESET}}$ delay time	30	50	70	ms

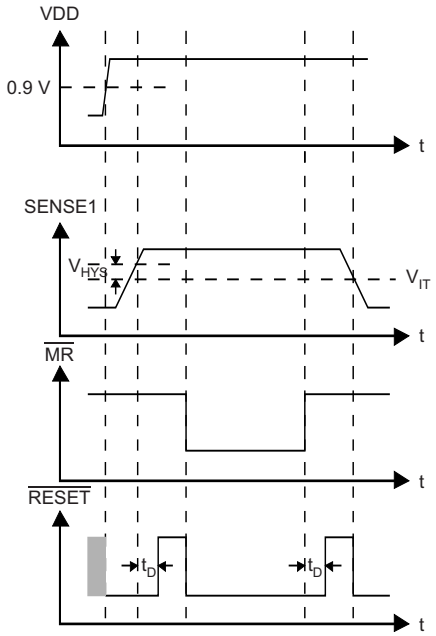


Figure 1. Timing Diagram

6.8 Typical Characteristics

At T_A = 25°C, and V_{DD} = 3.3 V, unless otherwise noted.

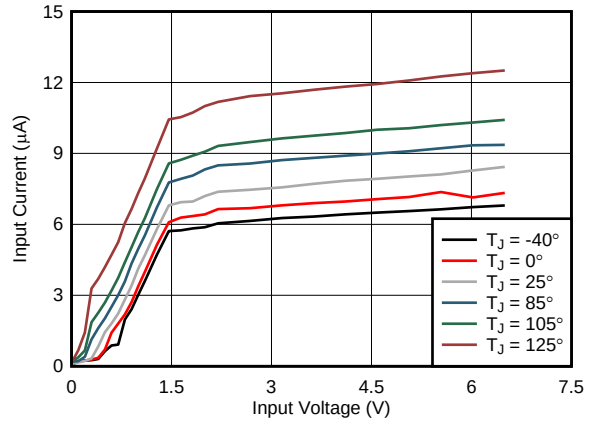


Figure 2. Supply Current vs Supply Voltage

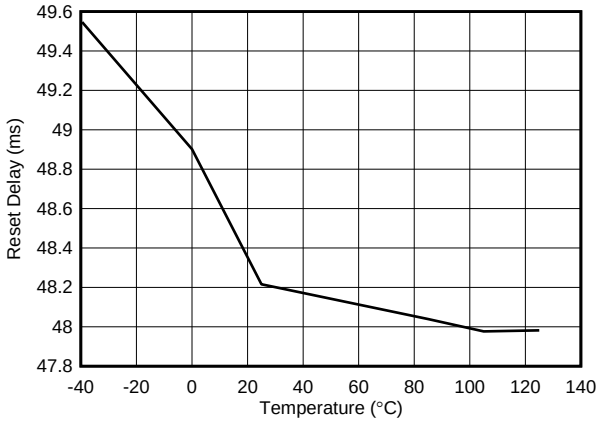


Figure 3. Reset Delay vs Temperature

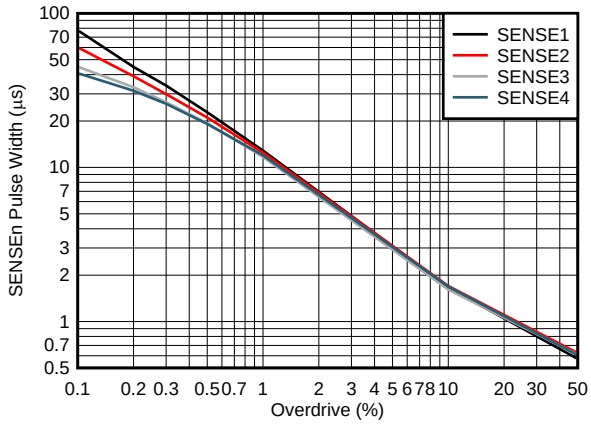


Figure 4. SENSEn Minimum Pulse Width vs SENSEn Threshold Overdrive Voltage

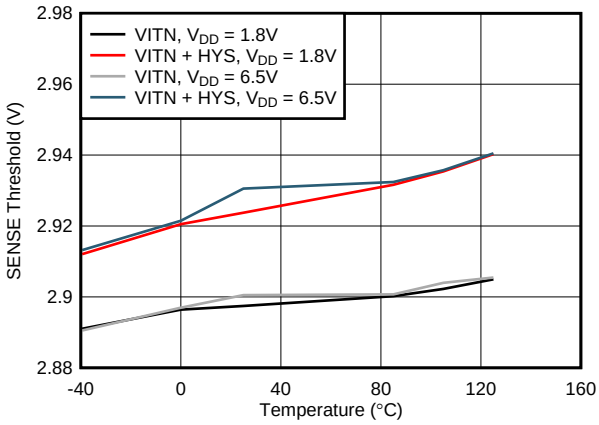


Figure 5. SENSE1 Threshold and Hysteresis vs Temperature

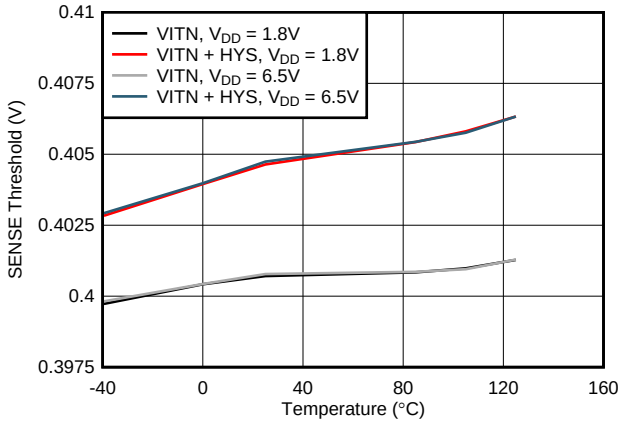


Figure 6. SENSE2 Threshold and Hysteresis vs Temperature

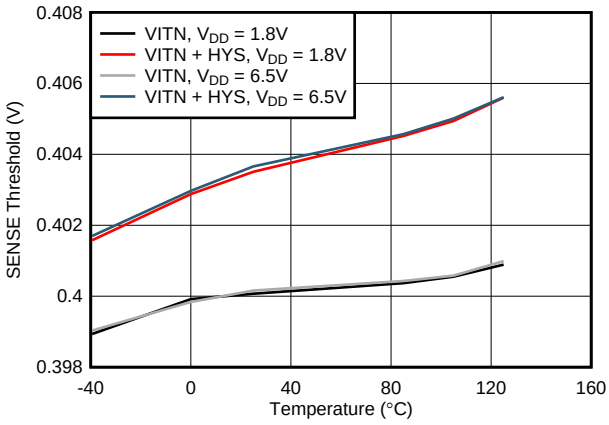


Figure 7. SENSE3 Threshold and Hysteresis vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, and V_{DD} = 3.3 V, unless otherwise noted.

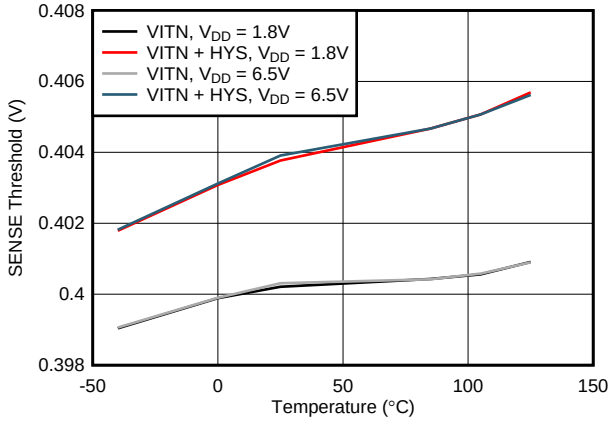


Figure 8. SENSE4 Threshold and Hysteresis vs Temperature

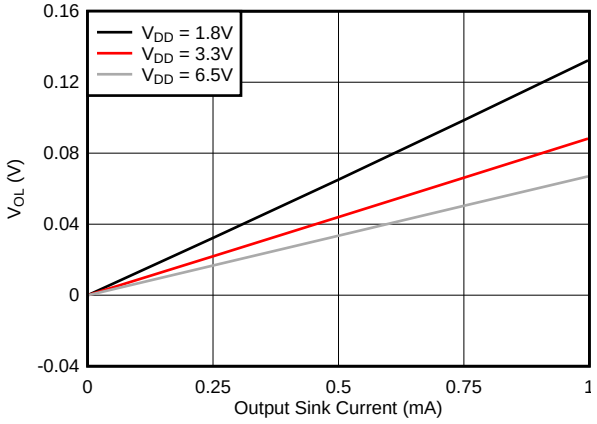


Figure 9. Output Voltage Low vs Output Current

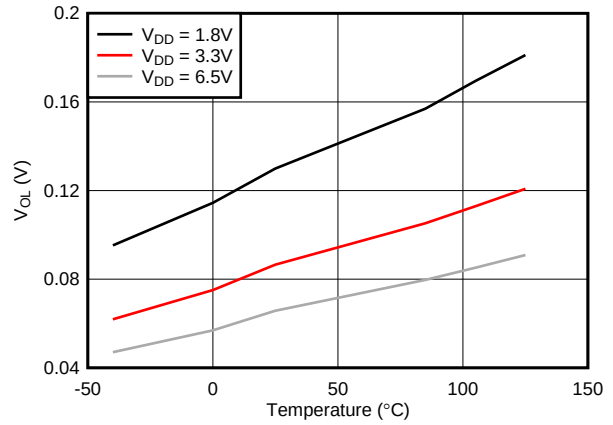


Figure 10. Output Voltage Low at 1 mA vs Temperature

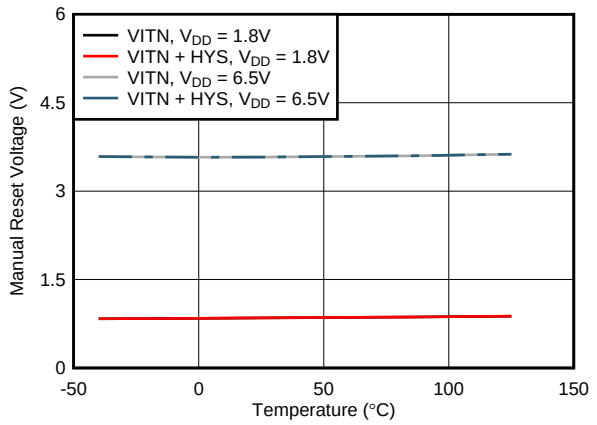


Figure 11. $\overline{MR}$ Threshold vs Temperature

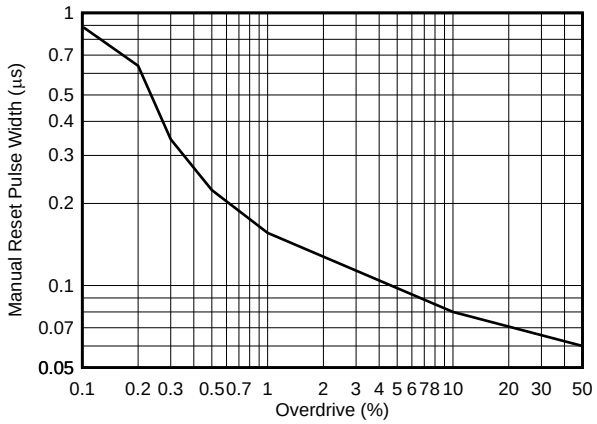
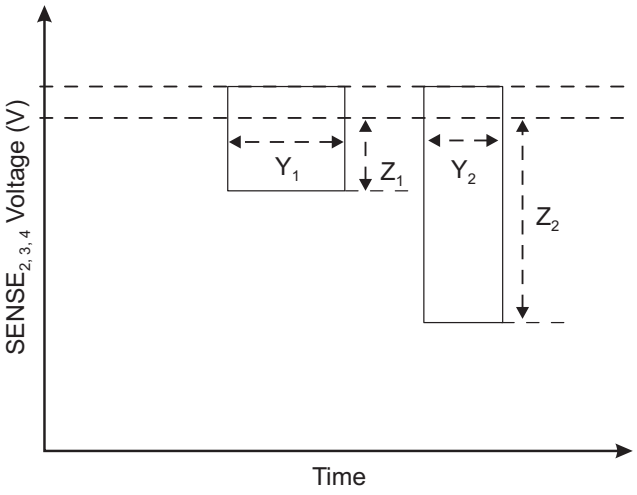


Figure 12. $\overline{MR}$ Minimum Pulse Width vs $\overline{MR}$ Threshold Overdrive Voltage

7 Parameter Measurement Information



$X_1 = (Z_1/0.4) * 100(\%)$
$X_2 = (Z_2/0.4) * 100(\%)$

$X_1 = X_2$ are overdrive (%) values calculated from actual $SENSE_{2, 3, 4}$ voltage amplitudes measured as Z_1 and Z_2.

Y_N is the minimum pulse width that gives $\overline{RESET}$ transition. Greater Z_N produces shorter Y_N.

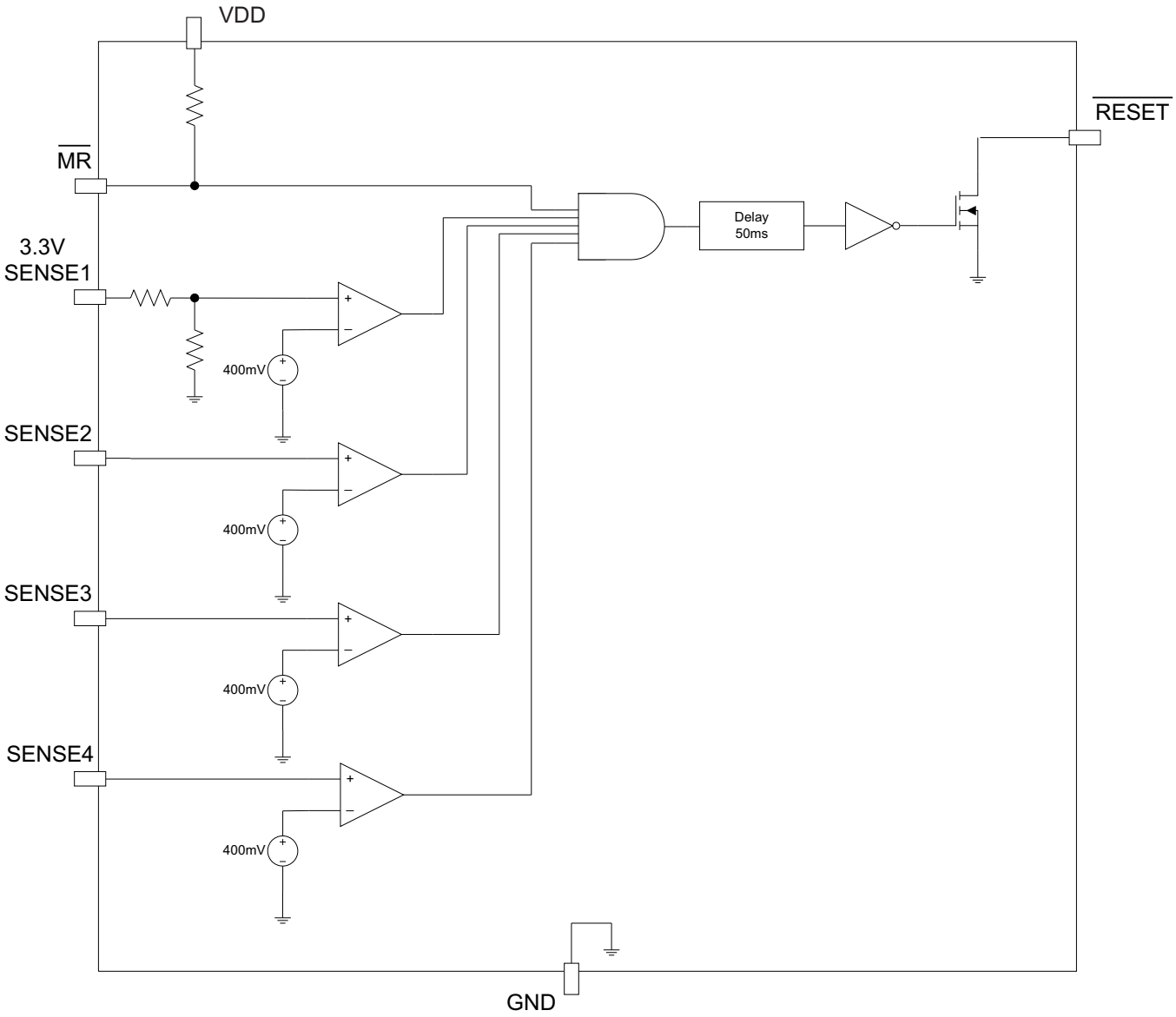
Figure 13. Overdrive Measurement Method: Measurement Technique for Immunity to SENSE Pin Voltage Transient

8 Detailed Description

8.1 Overview

The TPS386596L33 multi-channel reset supervisor provides a complete single reset function for a four power supply system. The design of the SVS is based on the TPS386000 quad supervisor device series. The TPS386596 is designed to assert the $\overline{\text{RESET}}$ signal following the logic in Table 1. The $\overline{\text{RESET}}$ output remains asserted for a 50-ms delay time (t_d) after the event of reset release. The SENSE1 input has a fixed voltage threshold designed to monitor a 3.3-V nominal supply. The trip point, V_{IT1}, for SENSE1 is 2.90 V (typical). Each of the remaining SENSEn inputs (n = 2, 3, 4) can be set to any voltage threshold greater than 0.4 V using an external resistor divider. An active-low manual reset ($\overline{\text{MR}}$) input is also provided for asserting the $\overline{\text{RESET}}$ signal as desired by the system, regardless of the voltage on any of the SENSE pins.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Voltage Monitoring

Each SENSEn (n = 2, 3, 4) pin can be set to monitor any voltage threshold greater than 0.4 V using an external resistor divider. The SENSE1 pin is designed to monitor a 3.3-V supply with a 2.9-V threshold. A broad range of voltage thresholds can be supported, allowing these devices to be used in a wide array of applications.

The TPS386596 is relatively immune to short negative transients on the SENSEn pin. Sensitivity to transients depends on threshold overdrive, as shown in the typical performance graph *TPS386596 SENSEn Minimum Pulse Width vs SENSEn Threshold Overdrive Voltage* (Figure 4).

8.3.2 Manual Reset

The manual reset $\overline{MR}$ input allows external logic signal from processors, other logic circuits, and/or discrete sensors to initiate a reset. The typical application of a TPS386596 has its $\overline{RESET}$ output connected to processor. A logic low at $\overline{MR}$ causes $\overline{RESET}$ to assert. After $\overline{MR}$ returns to a logic high and SENSEn are above the respective voltage thresholds, $\overline{RESET}$ is released after a fixed 50-ms reset delay time. An internal 100-kΩ pullup to VDD is integrated on the $\overline{MR}$ input. There is also an internal 50-ns (typical) deglitch circuit.

8.3.3 Reset Output

In a typical application of the TPS386596, the $\overline{RESET}$ output is connected to the reset input of a processor (DSP, MCU, CPU, FPGA, ASIC, and so forth) or connected to the enable input of voltage regulators (DC-DC, LDO, and so forth).

The TPS386596 provides an open-drain reset output. Pullup resistors must be used to hold this line high when $\overline{RESET}$ is not asserted. By connecting a pullup resistor to the proper voltage rail (up to 6.5 V), the $\overline{RESET}$ output can be connected to other devices at the proper interface voltage level. The pullup resistor should be no smaller than 10 kΩ due to the finite impedance of the output transistor.

The $\overline{RESET}$ output is defined for V_{DD} > 0.9 V. To ensure that the target processor is properly reset, the V_{DD} supply input should be fed by the power rail and be available as early as possible in the application.

Table 1 shows a truth table of how the $\overline{RESET}$ output is asserted or released. Figure 1 provides a timing diagram that shows how $\overline{RESET}$ is asserted and deasserted in relation to $\overline{MR}$ and the SENSEn inputs. Once the conditions are met, the transitions from the asserted state to the release state are performed after a fixed 50-ms delay time.

8.4 Device Functional Modes

Table 1 shows the device functional modes.

Table 1. $\overline{RESET}$ Truth Table

CONDITION		OUTPUT	
$\overline{MR}$ = L	SENSEn < VITn	$\overline{RESET}$ = L	Reset asserted
$\overline{MR}$ = L	SENSEn > VITn	$\overline{RESET}$ = L	Reset asserted
$\overline{MR}$ = H	SENSE1 < VIT1 OR SENSE2 < VIT2 OR SENSE3 < VIT3 OR SENSE4 < VIT4	$\overline{RESET}$ = L	Reset asserted
$\overline{MR}$ = H	SENSE1 > VIT1 AND SENSE2 > VIT2 AND SENSE3 > VIT3 AND SENSE4 > VIT4	$\overline{RESET}$ = H	**Reset released**

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Undervoltage Detection

The SENSEn inputs provide terminals at which the system voltages can be monitored. If the voltage at any one of the SENSEn pins drops the respective V_{ITn}, then the $\overline{\text{RESET}}$ output is asserted. The comparators have a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ transitions.

It is good analog design practice to use a 1-nF to 10-nF bypass capacitor at the SENSEn input to ground, to reduce sensitivity to transients, layout parasitics, and interference between power rails monitored by this device.

A typical connection of resistor dividers is show in Figure 14. SENSE1 is used to monitor a 3.3-V nominal power-supply voltage with a trip point equal to 2.90 V, and the remaining SENSEn (n = 2, 3, 4) inputs can be used to monitor voltage rails down to 0.4 V. Threshold voltages can be calculated using the following equations.

$$V_{MON(2)} = (1 + RS2H/RS2L) \times 0.4\ (V) \quad (1)$$

$$V_{MON(3)} = (1 + RS3H/RS3L) \times 0.4\ (V) \quad (2)$$

$$V_{MON(4)} = (1 + RS4H/RS4L) \times 0.4\ (V) \quad (3)$$

9.2 Typical Application

Figure 14 shows a typical application for the TPS386956.

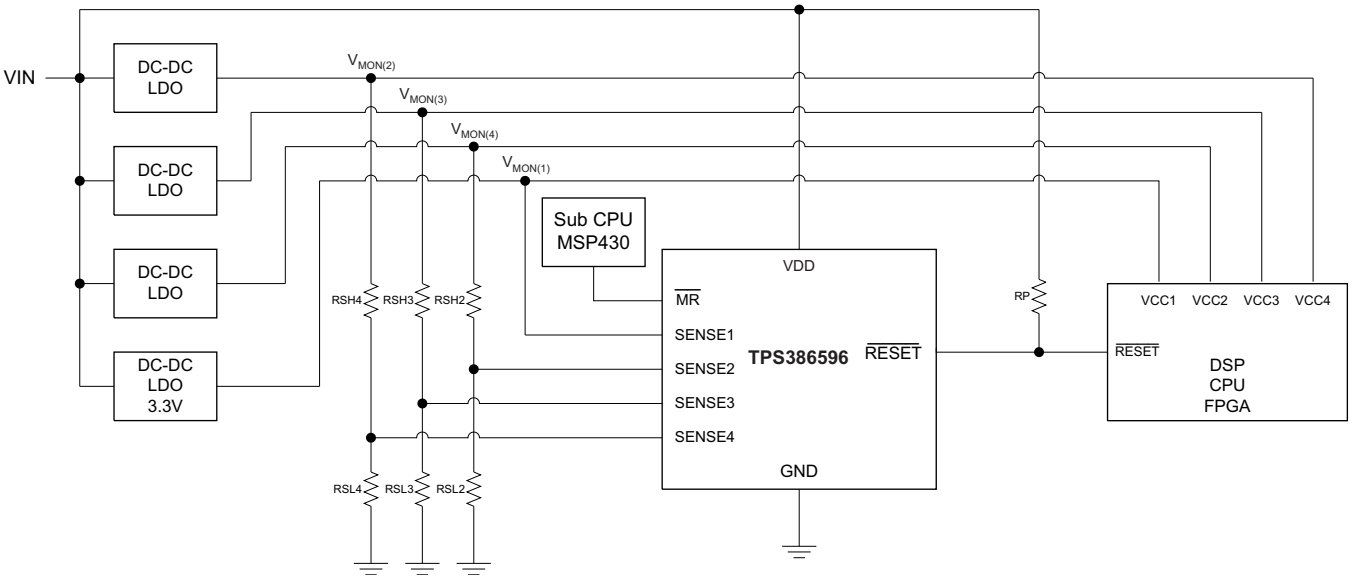


Figure 14. Typical Application Circuit

Typical Application (continued)

9.2.1 Design Requirements

This design is intended to monitor the voltage rails for an FPGA. Table 2 summarizes the design requirements.

Table 2. Design Requirements

PARAMETER	DESIGN REQUIREMENT
V_{DD}	5 V
$V_{MON(1)}$	3.3 V –10%
$V_{MON(2)}$	1.5 V –5%
$V_{MON(3)}$	1.2 V –5%
$V_{MON(4)}$	1 V –5%

9.2.2 Detailed Design Procedure

Select the pullup resistors to be 100 kΩ to ensure that $V_{OL} \leq 0.4$ V.

Select RSnL = 10 kΩ for all channels to ensure DC accuracy.

Use Equation 1 through Equation 3 to determine the values of RSnH and RS4M. Using standard 1% resistors, Table 3 shows the results:

Table 3. Design Results

RESISTOR	VALUE (kΩ)
RS1H	32.4
RS2H	25.5
RS3H	18.7
RS4H	14.3
RS4M	1

9.2.3 Application Curves

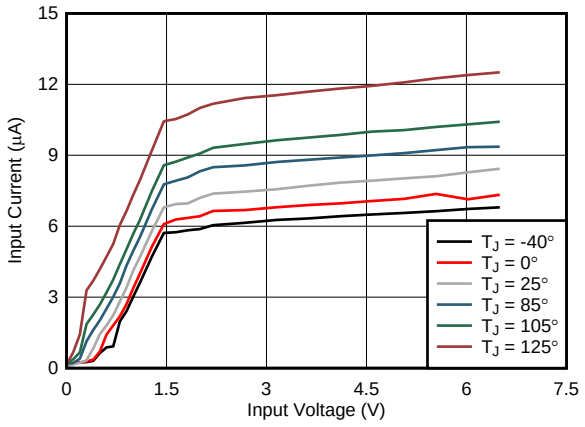


Figure 15. Supply Current vs Supply Voltage

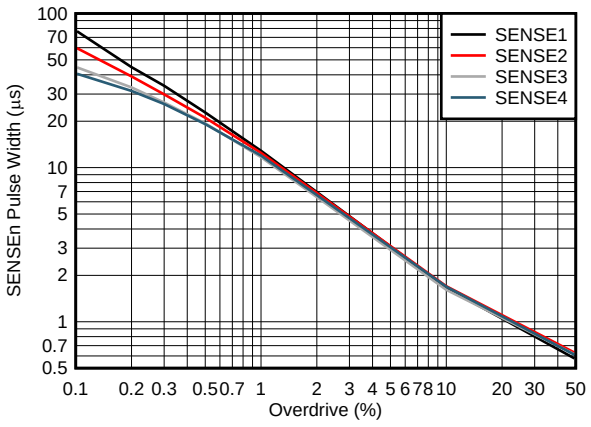


Figure 16. SENSEn Minimum Pulse Width vs SENSEn Threshold Overdrive Voltage

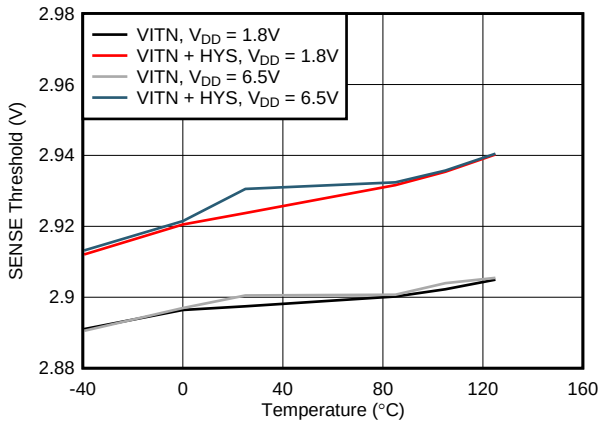


Figure 17. SENSE1 Threshold and Hysteresis vs Temperature

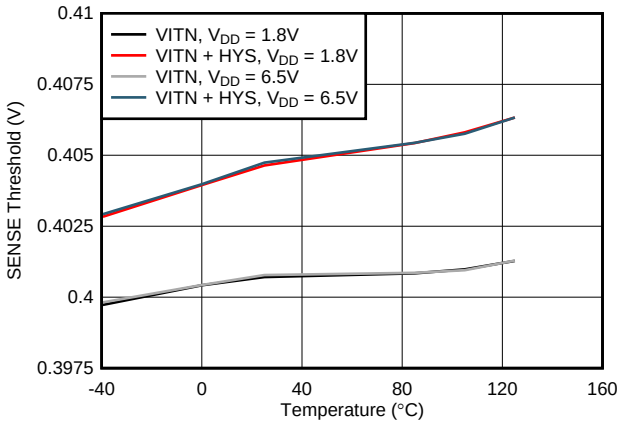


Figure 18. SENSE2 Threshold and Hysteresis vs Temperature

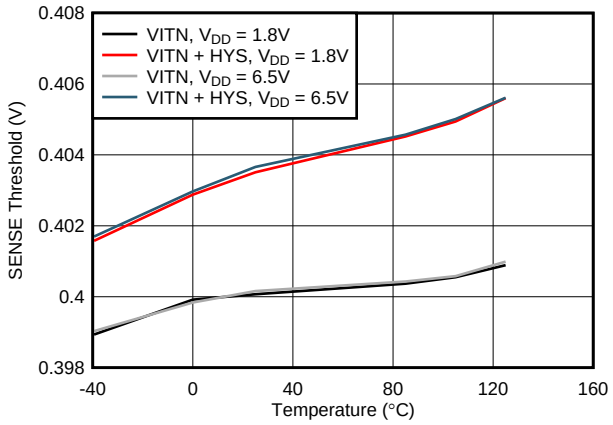


Figure 19. SENSE3 Threshold and Hysteresis vs Temperature

10 Power Supply Recommendations

The TPS386596 can operate from a 1.8-V to a 6.5-V input supply. A 0.1-µF capacitor placed next to the VDD pin to the GND node is highly recommended. This power supply should not be less than 1.8 V in normal operation to ensure that the internal UVLO circuit does not assert reset.

11 Layout

11.1 Layout Guidelines

Follow these guidelines to lay out the printed-circuit-board (PCB) that is used for the TPS386596.

- Avoid long traces from the SENSE pin to the resistor divider. Instead, run the long traces from the RSnH to $V_{MON(n)}$.
- Place the V_{DD} decoupling capacitor (C_{VDD}) close to the device.
- Avoid using long traces for the V_{DD} supply node. The V_{DD} capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum V_{DD} voltage.

11.2 Layout Example

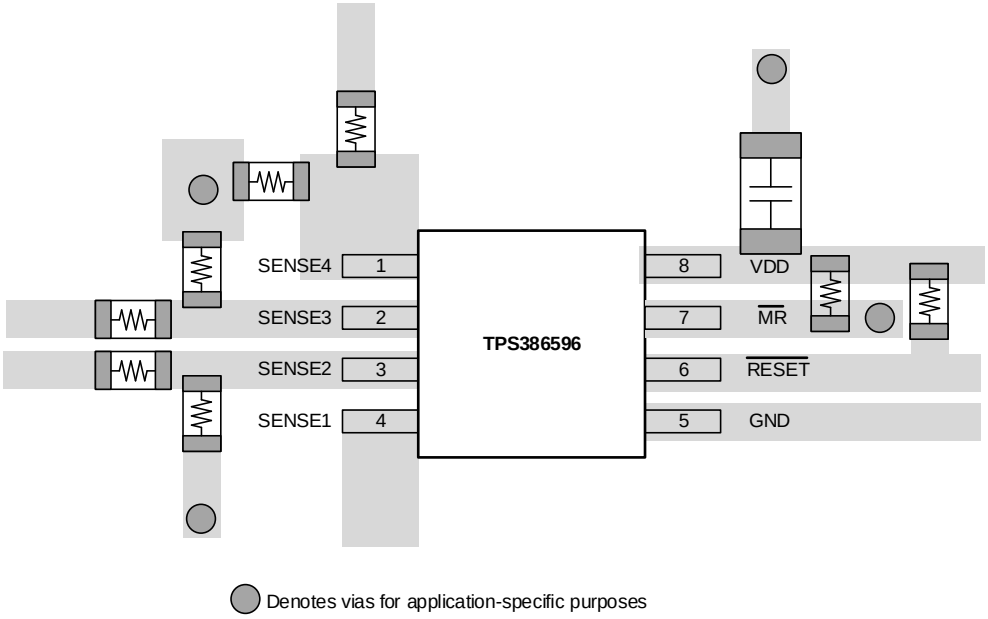


Figure 20. Example Layout (DGK Package)

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS386596 is available through the device product folders under *Simulation Models*.

12.1.2 Device Nomenclature

Table 4. Device Nomenclature(1)

PRODUCT	DESCRIPTION
TPS386596**xxx** ***yyy*** **z**	**xxx** is device voltage option (for example, L33 = 3.3 V option) **yyy** is package designator **z** is package quantity

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS386596L33DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PMXQ
TPS386596L33DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PMXQ
TPS386596L33DGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PMXQ
TPS386596L33DGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PMXQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

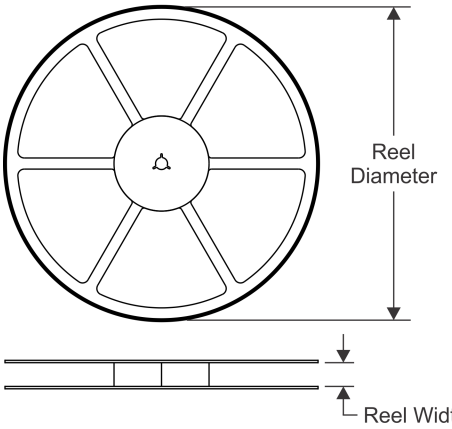
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

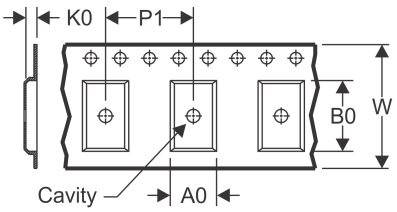
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

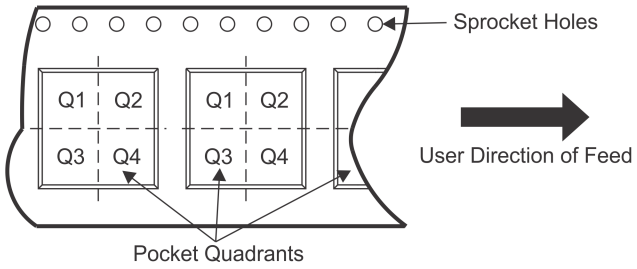


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

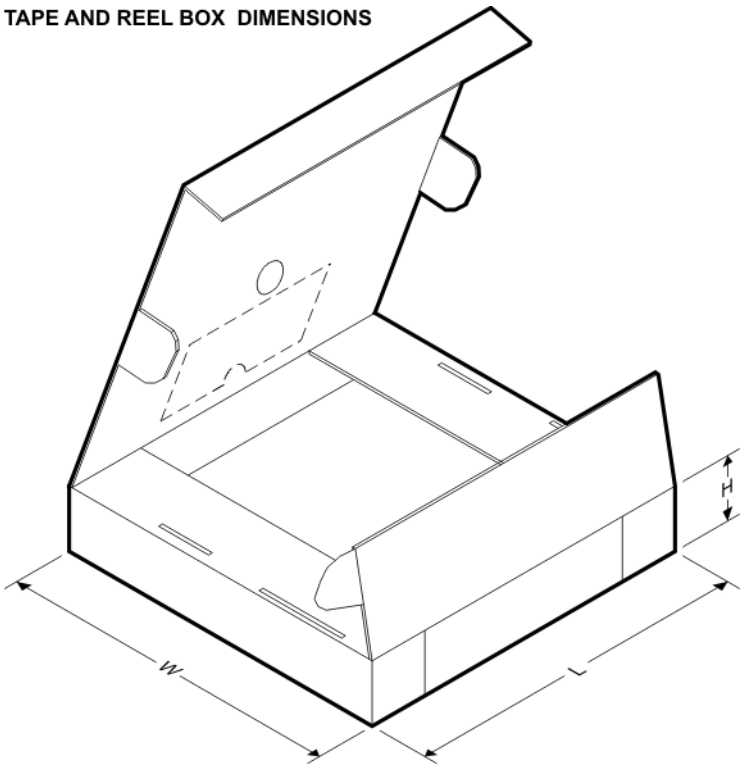
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS386596L33DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS386596L33DGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

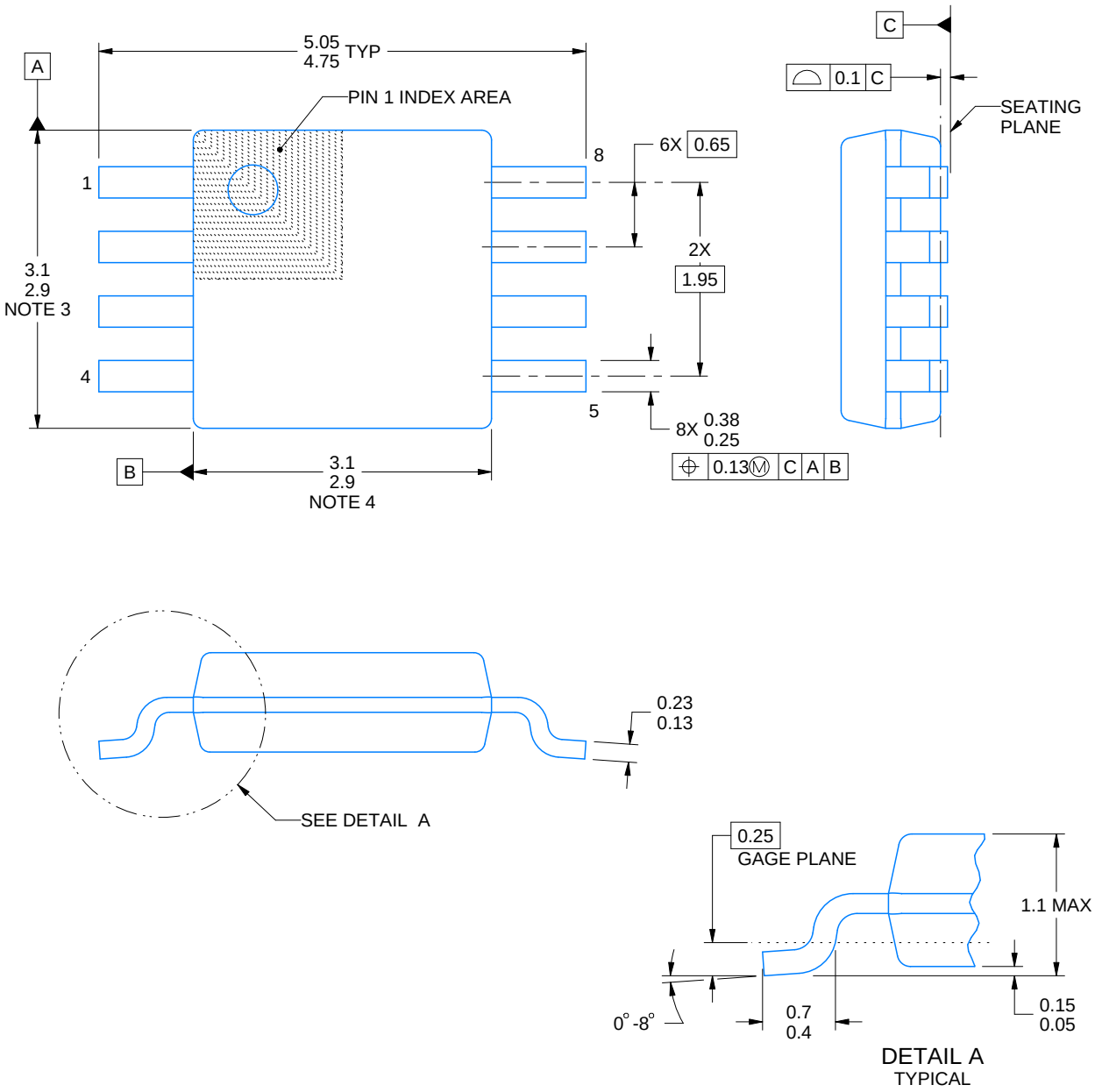
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS386596L33DGKR	VSSOP	DGK	8	2500	367.0	367.0	38.0
TPS386596L33DGKT	VSSOP	DGK	8	250	213.0	191.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

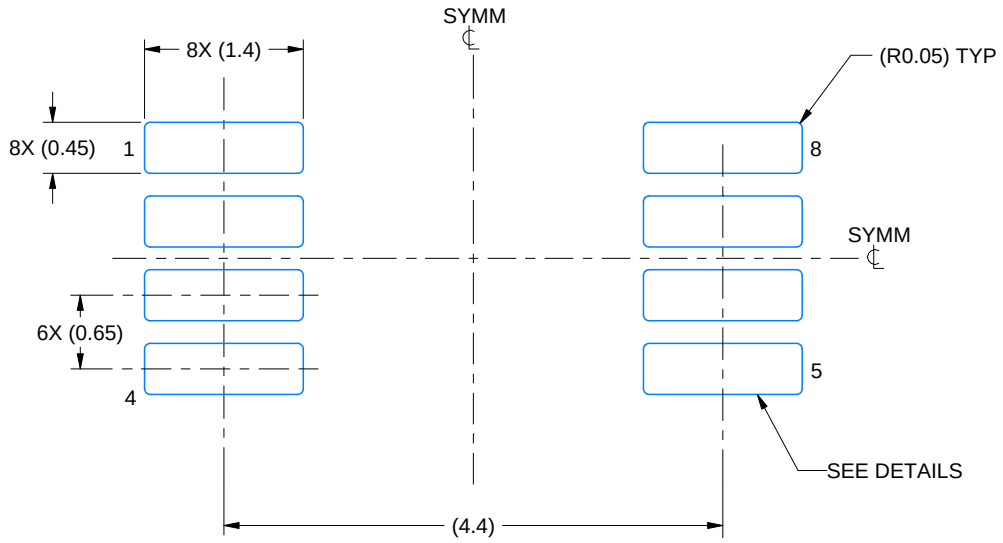
SMALL OUTLINE PACKAGE



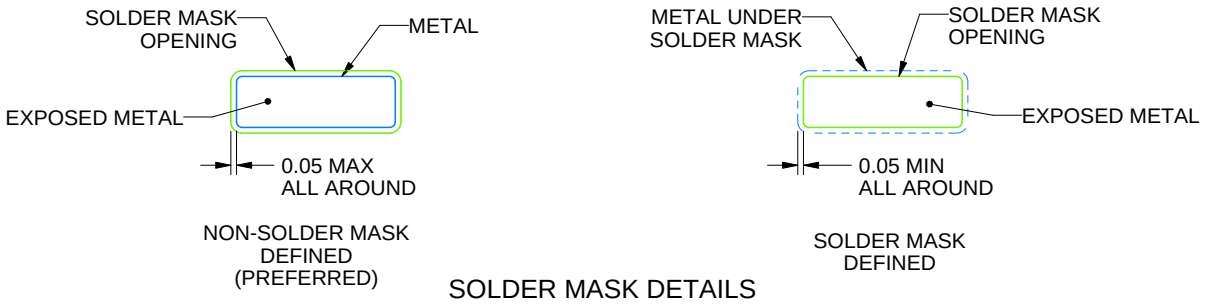
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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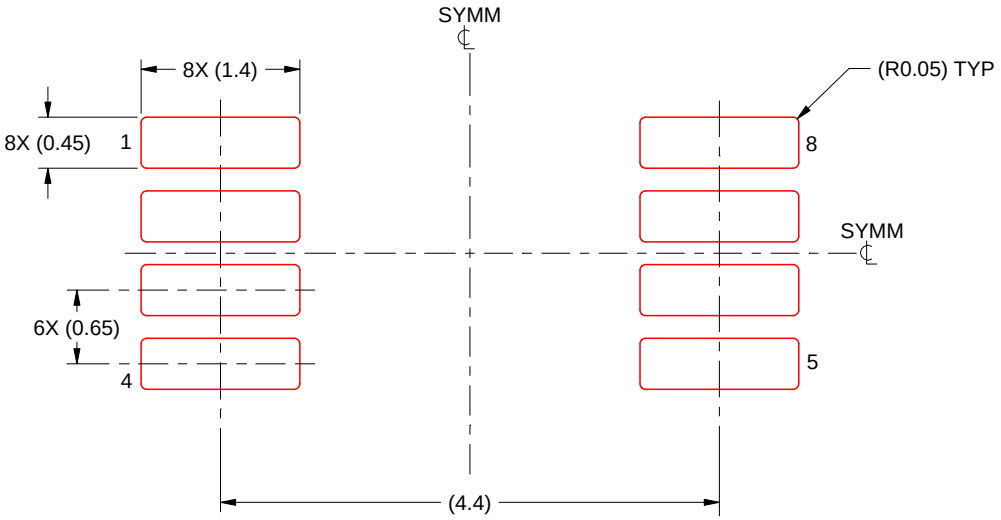
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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