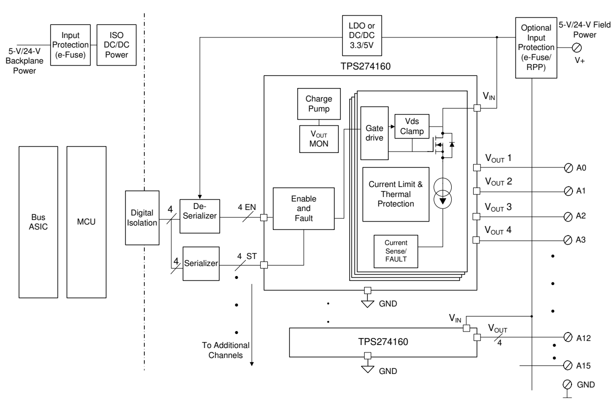
TPS274160x 160mΩ 四通道智能高侧开关

1 特性

- 四通道 160mΩ 智能高侧开关
- 宽直流工作电压范围：5V 至 36V
  - 50V 绝对最大电压
- 精确可调节电流限制范围（250mA 至 4A）
- 智能诊断功能
  - TPS274160A：开漏故障输出
  - TPS274160B：模拟电流感应
  - 关闭状态下开路负载或对电源短路检测
- 强大的保护特性
  - 短路保护
  - 电感负载反激式钳位
  - 欠压锁定 (UVLO) 保护
  - 接地失效保护
- VS 和 OUT 引脚提供出色 ESD 保护
  - ±8/±15kV IEC 61000-4-2 ESD 接触/空气放电
- 采用小型 28 引脚无引线 QFN 封装
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档

2 应用

- 数字输出模块
- 独立远程 I/O
- 电机驱动器
- 电磁阀或阀驱动器



应用示例

3 说明

TPS274160 器件是一款智能高侧开关，通过四个集成式 160mΩ NMOS 功率 FET 和一个电荷泵来驱动栅极。该器件提供强大的保护和诊断功能，可以驱动各种电感、容性和电阻性负载，例如低瓦数灯泡、LED、继电器、电磁阀、加热器和子模块。该器件可通过并行通道实现灵活的多通道输出配置，并采用超小型 WQFN 封装，可在空间受限的应用中使用。

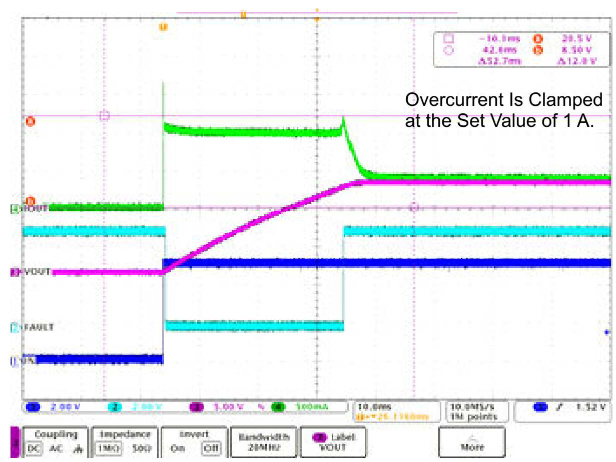
该器件具有短路和过热保护功能，可在故障期间安全地关闭输出。该器件还支持从外部调节电流限值。这一特性通过减小驱动大容性负载时的浪涌电流并尽可能降低过载电流，可提高系统的可靠性，从而消除系统欠压的情况。

该器件还集成了诊断功能，例如输出电流监控（B 版本）和开路负载检测，从而使模块更加智能并实现预测性维护功能。

器件信息

器件型号	封装[1]	封装尺寸
TPS274160A	WQFN (28)	4mm x 5mm
TPS274160B	WQFN (28)	4mm x 5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



驱动具有可调节电流限制的电容性负载

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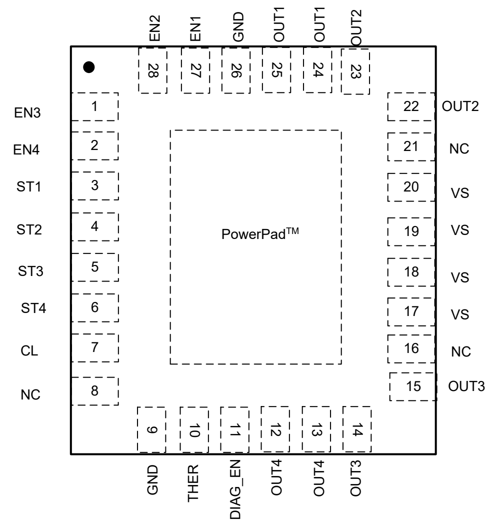
4 Revision History

Changes from Revision * (May 2020) to Revision A (November 2020)	Page
• 更新了整个文档的表、图和交叉参考的编号格式	1
• 将数据表状态从“预告信息”更改为“量产数据”	1

5 Device Comparison Table

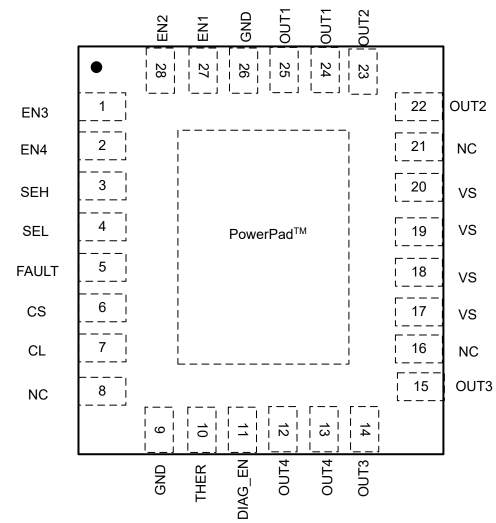
PART NO.	FAULT REPORTING MODE
TPS274160**A**	Open-drain digital output
TPS274160**B**	Current-sense analog output

6 Pin Configuration and Functions



NC – No internal connection

图 6-1. RLH Package 28-Pin WQFN With Exposed Thermal Pad TPS274160A Top View



NC – No internal connection

图 6-2. RLH Package 28-Pin WQFN With Exposed Thermal Pad TPS274160B Top View

表 6-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS274160			
	Version A	Version B		
CL	7	7	O	Adjustable current limit. Connect to device GND if external current limit is not used.
CS	—	6	O	Current-sense output.
DIAG_EN	11	11	I	Enable-disable pin for diagnostics; internal pulldown.
FAULT	—	5	O	Global fault report with open-drain structure, ORed logic for quad-channel fault conditions.
GND	9,26	9, 26	—	Ground pin.
EN1	27	27	I	Input control for channel 1 activation; internal pulldown.
EN2	28	28	I	Input control for channel 2 activation; internal pulldown.
EN3	1	1	I	Input control for channel 3 activation; internal pulldown.
EN4	2	2	I	Input control for channel 4 activation; internal pulldown.
NC	8, 21, 16	8, 21, 16	—	No internal connection.
ST1	3	—	O	Open-drain diagnostic status output for channel 1.
ST2	4	—	O	Open-drain diagnostic status output for channel 2.
ST3	5	—	O	Open-drain diagnostic status output for channel 3.
ST4	6	—	O	Open-drain diagnostic status output for channel 4.
SEH	—	3	I	CS channel-selection high bit; internal pulldown.
SEL	—	4	I	CS channel-selection low bit; internal pulldown.
THER	10	10	I	Thermal shutdown behavior control, latch off or auto-retry; internal pulldown.
OUT1	24, 25	24, 25	O	Output of the channel 1 high side-switch, connect to the load.
OUT2	22, 23	22, 23	O	Output of the channel 2 high side-switch, connect to the load.

表 6-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	TPS274160			
	Version A	Version B		
OUT3	14, 15	14, 15	O	Output of the channel 3 high side-switch, connect to the load.
OUT4	12, 13	12, 13	O	Output of the channel 4 high side-switch, connect to the load.
VS	17, 18, 19, 20	17, 18, 19, 20	I	Power supply.
Thermal pad	—	—	—	Connect to device GND or leave floating

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Input Voltage on Supply pin (3)			50	V
Reverse polarity voltage (4)		–36		V
Current on GND pin	t < 2 minutes	–100	250	mA
Voltage on ENx, DIAG_EN, SEL, SEH, and THER pins		–0.3	7	V
Current on ENx, DIAG_EN, SEL, SEH, and THER pins		–10	—	mA
Voltage on $\overline{STx}$ or $\overline{FAULT}$ pins		–0.3	7	V
Current on $\overline{STx}$ or $\overline{FAULT}$ pins		–30	10	mA
Voltage on CS pin		–2.7	7	V
Current on CS pin		—	30	mA
Voltage on CL pin		–0.3	7	V
Current on CL pin		—	6	mA
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Maximum voltage including long transients < 400 ms.
(4) Reverse polarity condition:time t < 180s, reverse current < $I_{R(2)}$, ENx = 0 V, GND pin 1-kΩ resistor in parallel with diode.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD1)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except VS and VOUTx	±2000	V
$V_{(ESD2)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	VS and VOUTx with respect to GND	±5000	V
$V_{(ESD3)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	All pins	±750	V
$V_{(ESD4)}$	Electrostatic discharge	Contact/Air discharge, per IEC 61000-4-2 (3)	VS, OUTx	±8/±15	kV
$V_{(surge)}$	Transient surge	Surge protection with 42 Ω, per IEC 61000-4-5; 1.2/50 μs (3)	VS, OUTx	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Tested with the application circuit and supply voltage of 24 V DC and always ON, EN Inputs High → Output High (ON)

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VS}	Continuous DC Supply operating voltage (1)	5	36	V
	Voltage on ENx, DIAG EN, SEL, SEH, and THER pins	0	5	V
	Voltage on ST and FAULT pins	0	5	V
I_{nom}	Nominal DC load current per channel (all channels on)	0	1.35	A
T_A	Operating ambient temperature range	–40	125	°C

(1) Transients up to the absolute maximum is allowed

7.4 Thermal Information

THERMAL METRIC(1)		TPS274160 RLH(QFN) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

(5 V ≤ Vs ≤ 36 V; −40°C ≤ T_J ≤ 125°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VS(uvr)}$	Undervoltage turnon	VS voltage rising, $V_{VS} > V_{VS(uvr)}$, device turns on.	3.5	3.7	4	V
$V_{VS(uvf)}$	Undervoltage shutdown	VS voltage falling, $V_{VS} < V_{VS(uvf)}$ device shuts off.	3	3.2	3.4	V
$V_{VS(uv,hys)}$	Undervoltage shutdown, hysteresis			0.5		V
I_{qd}	Device quiescent current, diagnostics enabled	V_{VS} < 30 V, ENx = 5 V, DIAG_EN = H/L, Ioutx = 0 A, current limit = 2 A, all channels on			6.2	mA
I_{off}	Standby current	V_{VS} < 30 V, ENx = DIAG_EN = OUTx = THER = 0 V, T_J = 25°C			1.4	µA
		V_{VS} < 30 V, ENx = DIAG_EN = OUTx = THER = 0 V, T_J = 125°C			5	
$I_{off(diag)}$	Standby current with diagnostic enabled	V_{VS} < 30 V, ENx = 0 V, DIAG_EN = 5 V, $V_{VS} - V_{OUTx} > V_{ol(off)}$, not in open-load mode			5	mA
$t_{off(deg)}$	Standby mode deglitch time(1)	EN from high to low, if elapsed time > $t_{off(deg)}$, the device enters into standby mode.	10	12.5	15	ms
$I_{out(leak)}$	Output leakage current in off-state	V_{VS} < 30 V, ENx = DIAG_EN = OUTx = 0, T_J = 25°C			0.5	µA
		V_{VS} < 30 V, ENx = DIAG_EN = OUTx = 0, T_J < 125°C			8	µA
$r_{DS(on)}$	On-state resistance	V_{VS} ≥ 5V, T_J = 25°C		160		mΩ
		V_{VS} ≥ 5 V, T_J = 125°C			260	
$\Delta r_{DS(on)}$	Percentage Difference in On-state resistance between channels ($r_{DS(on)CHx} - r_{DS(on)CHy}$) (1)	V_{VS} ≥ 5V, T_J = 25°C			6	%
$I_{cl(int)}$	Internal current limit	Internal current limit value, CL pin connected to GND	8		14	A

7.5 Electrical Characteristics (continued)

(5 V ⩽ Vs ⩽ 36 V; −40°C ⩽ T_J ⩽ 125°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{cl(TSD)}$	Current limit during thermal shutdown	Internal current limit value under thermal shutdown		6.5		A
		External current limit value under thermal shutdown. The percentage of the external current limit setting value		70%		
$V_{ds(clamp)}$	Source-to-drain body diode voltage		50		70	V
V_F	Drain−source diode voltage	EN = 0, Iout = −0.15 A.	0.3	0.7	0.9	V
$I_{R(1)}$	Continuous reverse current from source to drain	t < 60 s, V_{VS} = 24 V, ENx = 0 V, T_J = 25°C, single channel reversed current to supply		2.5		A
$I_{R(2)}$	Continuous reverse current from source to drain	t < 60 s, V_{VS} = 24 V, ENx = 0 V, GND pin 1-kΩ resistor in parallel with diode. T_J = 25°C. Reverse-current condition, All channels reversed		2.0		A
V_{IH}	Logic high-level voltage		2			V
V_{IL}	Logic low-level voltage				0.8	V
$R_{(logic,pd)}$	Logic-pin pulldown resistor	DIAG_EN V_{VS} = V_{DIAG_EN}=5V	200	275	350	kΩ
$R_{(logic,pd)}$	Logic-pin pulldown resistor	ENx, SEL, SEH, THER pins, V_{VS} = V_{ENx}= V_{SEL}=V_{SEH}=V_{THER}=5V	100	175	250	kΩ
$I_{gnd(loss)}$	Output leakage current under GND loss condition	V_{VS} = 24 V			20	µA
$V_{ol(off)}$	Open load detection threshold	ENx = 0 V, when V_{VS} – V_{OUTx}> $V_{ol(off)}$, duration longer than $t_{ol(off)}$, then open load is detected, off state	1.6		2.6	V
$t_{ol(off)}$	Open-load detection threshold deglitch time	ENx =0V, when V_{VS} – V_{OUTx}> $V_{ol(off)}$, duration longer than $t_{ol(off)}$, then open load is detected, off state	300	560	800	µs
$I_{ol(off)}$	Off-state output sink current	ENx = 0 V, DIAG_EN= 5 V, V_{VS} – V_{OUTx} = 24 V, T_J = 125°C, open load			100	µA
$V_{OL(STx)}$	Status low-output voltage	I_{STx} = 2 mA, version A only			0.2	V
$V_{OL(FAULT)}$	Fault low-output voltage	I_{FAULT} = 2 mA, version B only			0.2	V
$t_{cl(deg)}$	Deglitch time when current limit occurs(1)	ENx = DIAG_EN = 5 V, the deglitch time from current limit toggling to FAULT, STx, CS report.	80		180	µs
T_{SD}	Thermal shutdown threshold		160	175		°C
$T_{SD(rst)}$	Thermal shutdown status reset threshold			155		°C
T_{sw}	Thermal swing shutdown threshold			60		°C
T_{hys}	Hysteresis for resetting the thermal shutdown or thermal swing			10		°C
K_{CS}	Current sense ratio (Ver. B only)			300		
K_{CL}	Current limit ratio			2500		
$V_{CL(th)}$	Current limit internal threshold voltage(1) (2)			0.8		V
dK_{CS} / K_{CS}	Current sense accuracy, (I_{CS} × K_{CS} – I_{OUT}) /I_{OUT} × 100	V_{VS} = 24 V, Ioutx ⩾ 5 mA (Version B)	-50		50	%
dK_{CS} / K_{CS}	Current sense accuracy, (I_{CS} × K_{CS} – I_{OUT}) /I_{OUT} × 100	V_{VS} = 24 V, Ioutx ⩾ 25 mA (Version B)	-10		10	%
dK_{CS} / K_{CS}	Current sense accuracy, (I_{CS} × K_{CS} – I_{OUT}) /I_{OUT} × 100	V_{VS} = 24 V, Ioutx ⩾ 50 mA (Version B)	-5		5	%
dK_{CS} / K_{CS}	Current sense accuracy, (I_{CS} × K_{CS} – I_{OUT}) /I_{OUT} × 100	V_{VS} = 24 V, Ioutx ⩾ 100 mA (Version B)	-3		3	%

7.5 Electrical Characteristics (continued)

(5 V ⩽ Vs ⩽ 36 V; −40°C ⩽ T_J ⩽ 125°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dK_{CS} / K_{CS}	Current sense accuracy, (I_{CS} × K_{CS} – I_{OUT}) /I_{OUT} × 100	V_{VS} = 24 V, Ioutx ⩾ 0.5 A (Version B)	-2		2	%
dK_{CL} / K_{CL}	External current limit accuracy, (I_{OUT} – I_{CL} × K_{CL} –) × 100 / I_{CL} × K_{CL}	V_{VS} = 24 V, Ilimit ⩾ 0.25 A	-20		20	%
dK_{CL} / K_{CL}	External current limit accuracy, (I_{OUT} – I_{CL} × K_{CL} –) × 100 / I_{CL} × K_{CL}	V_{VS} = 24 V, 2 A ⩽ Ilimit ⩽ 7 A	-15		15	%
$V_{CS(lin)}$	Current-sense voltage linear range[1]	V_{VS} ⩾ 6.5 V	0		4	V
		5 V ⩽ V_{VS} < 6.5 V	0		Vs – 2.5	
$I_{OUTx(lin)}$	Output-current linear range[1]	V_{VS} ⩾ 6.5 V, Vcs,lin ⩽ 4 V	0		2.2	A
		5 V ⩽ V_{VS} < 6.5 V, $V_{cs,lin}$ ⩽ V_{VS} – 2.5 V	0		2.2	
$V_{CS(H)}$	Current sense pin output voltage	V_{VS} ⩾ 7 V, fault mode	4.5		6.5	V
		5 V ⩽ V_{VS} < 7 V, fault mode	Min(Vs - 2, 4.5)		6.5	V
$I_{CS(H)}$	Current-sense pin output current available in fault mode	Vcs = 4.5 V, V_{VS} > 7 V	15			mA
$I_{CS(leak)}$	Current-sense leakage current in disabled mode	DIAG_EN = 0 V, TJ =125ºC			0.5	µA

(1) Value specified by design, not subject to production test.
(2) Vcl,th tolerance is included in the dK_{CL} / K_{CL} tolerance.

7.6 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d,on}$	Turnon delay time	Vs = 24 V, DIAG_EN = 5 V, Ioutx = 0.5 A, IN rising edge to 10% of Voutx	20	50	90	µs
$t_{d,off}$	Turnoff delay time	Vs = 24 V, DIAG_EN = 5 V, Ioutx = 0.5 A, IN falling edge to 90% of Voutx	20	50	90	µs
$t_{d,rise}$	Channel turnon time	V_S = 24 V, DIAG_EN = 5 V, Ioutx = 0.5 A 50% of EN to 90% of VOUT	90	120	150	µs
$t_{d,fall}$	Channel Turnoff time	V_S = 24 V, DIAG_EN = 5 V, Ioutx = 0.5 A 50% of EN to 10% of VOUT	90	120	150	µs
dV/dton	Turnon slew rate	Vs = 24 V, DIAG_EN = 5 V, Ioutx = 0.5 A, Voutx from 10% to 90%	0.1	0.3	0.55	V/µs
dV/dtoff	Turnoff slew rate	Vs = 24 V, DIAG_EN = 5 V, Ioutx = 0.5 A, Voutx from 90% to 10%	0.1	0.3	0.55	V/µs
$t_{d,match}$	$t_{d,rise}$ – $t_{d,fall}$	Vs = 24 V, Iload= 0.5A. $t_{d, rise}$ is the IN rising edge to Vout = 90%. $t_{d, fall}$ is the IN falling edge to Vout = 10%.	– 50		50	µs
$t_{cs,off1}$	CS settling time from DIAG_EN disabled	Vs = 24 V, ENx = 5 V, Ioutx = 0.5 A. current limit = 2 A. DIAG_EN falling edge to 10% of Vcs.			20	µs
$t_{cs,on1}$	CS settling time from DIAG_EN enabled	Vs = 24 V, ENx = 5 V, Ioutx = 0.5 A. current limit is 2A. DIAG_EN rising edge to 90% of Vcs.			20	µs
$t_{cs,off2}$	CS settling time from IN falling edge	Vs = 24 V, DIAG_EN = 5 V, Ioutx = 0.5 A. current limit = 2 A. EN falling edge to 10% of Vcs			100	µs
$t_{cs,on2}$	CS settling time from IN rising edge	Vs = 24 V, DIAG_EN = 5 V, Ioutx = 0.5 A. current limit = 2 A. EN rising edge to 90% of Vcs			150	µs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SEx}	Multi-sense transition delay from channel to channel	DIAG_EN = 5 V, current sense output delay when multi-sense pins SEL and SEH transition from channel to channel			50	μs

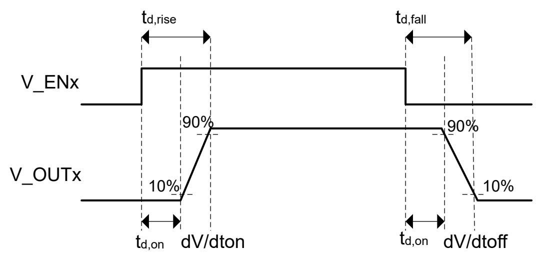


图 7-1. Output Delay Characteristics

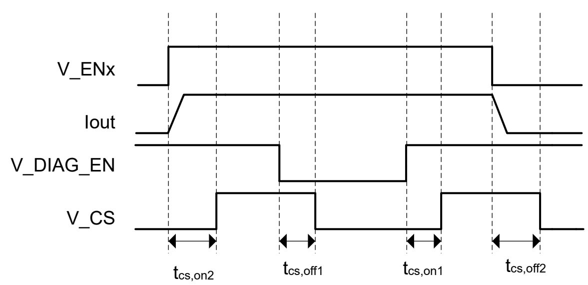


图 7-2. CS Delay Characteristics

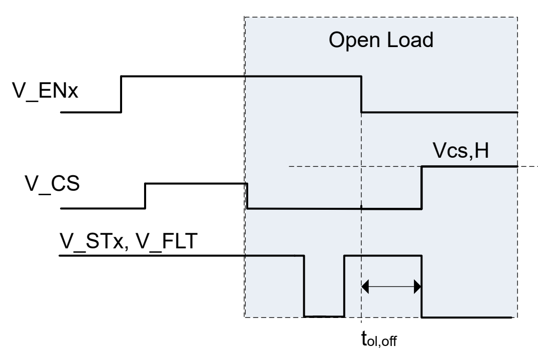


图 7-3. Open-Load Blanking-Time Characteristics

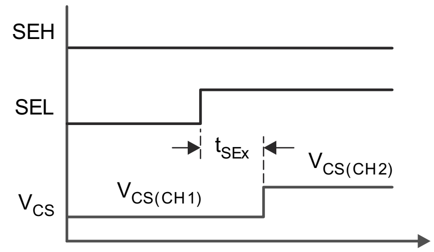


图 7-4. Multi-Sense Transition Delay

7.7 Typical Characteristics

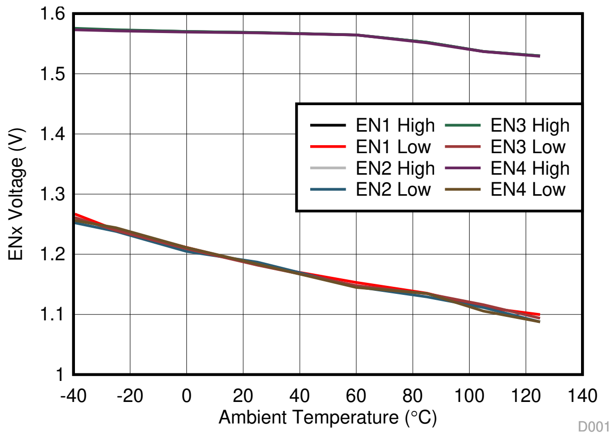


图 7-5. ENx Voltage Threshold

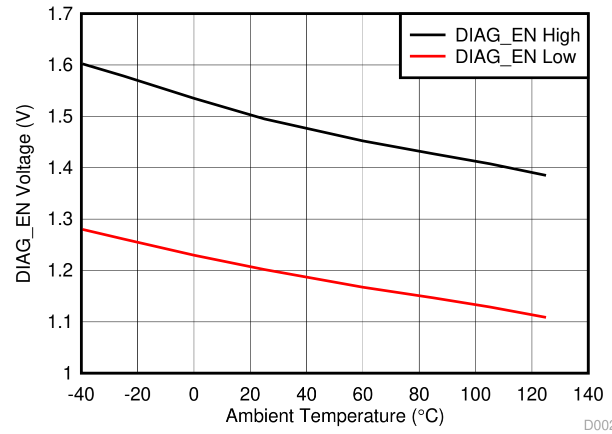


图 7-6. DIAG_EN Voltage Threshold

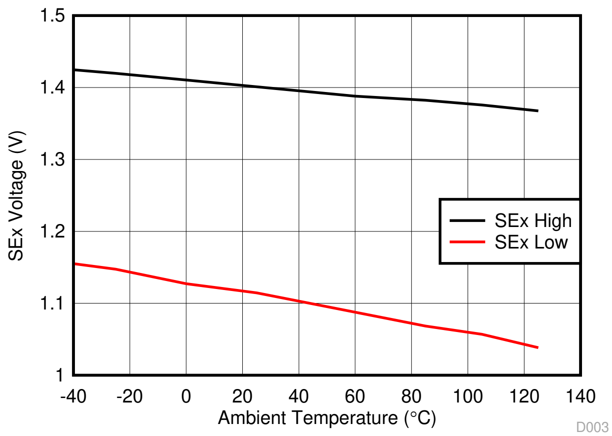


图 7-7. SEx Voltage Threshold

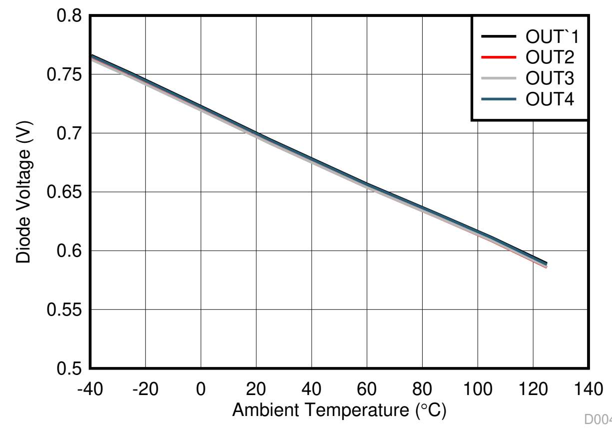


图 7-8. Body-Diode Forward Voltage

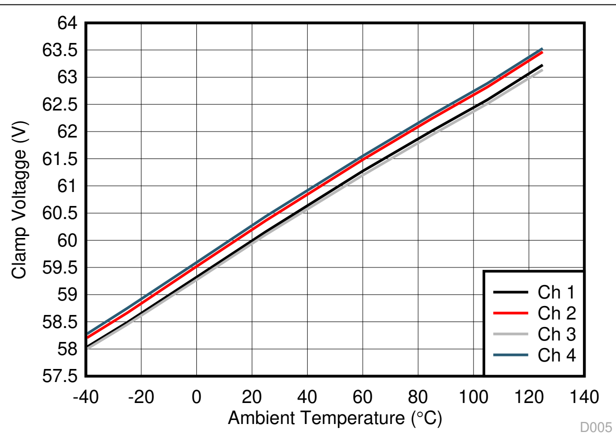


图 7-9. Drain-to-Source Clamp Voltage

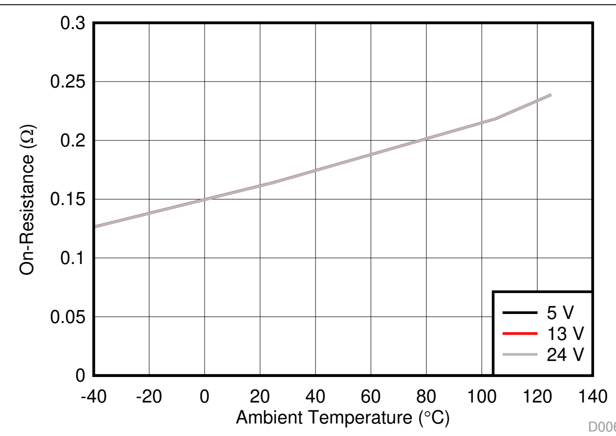


图 7-10. Channel-1 FET On-Resistance

7.7 Typical Characteristics (continued)

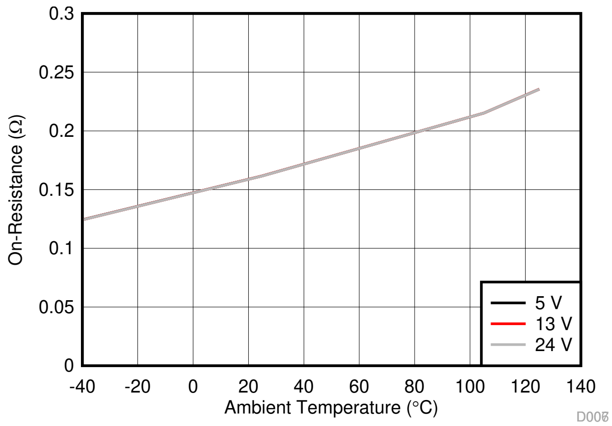


图 7-11. Channel-2 FET On-Resistance

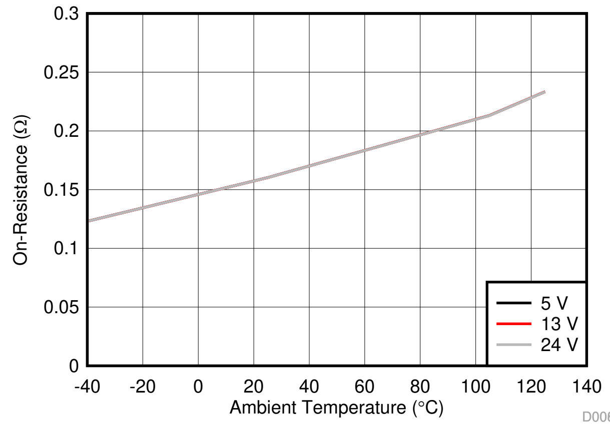


图 7-12. Channel-3 FET On-Resistanc

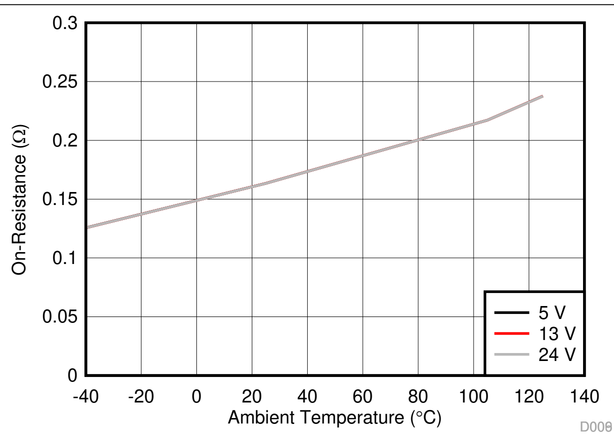


图 7-13. Channel-4 FET On-Resistanc

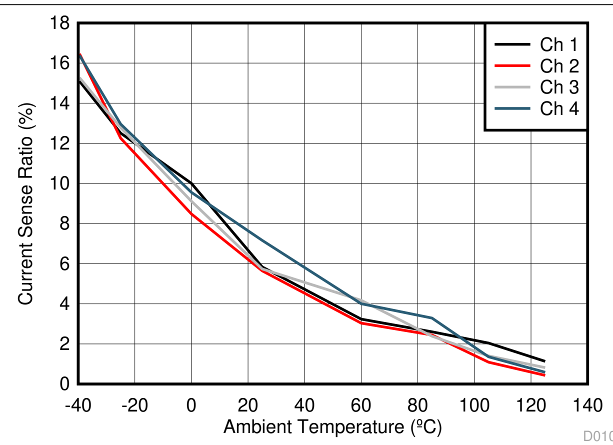


图 7-14. Current-Sense Ratio at 5 mA

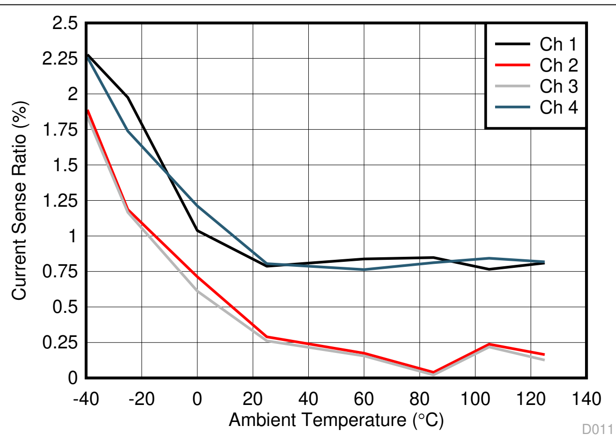


图 7-15. Current-Sense Ratio at 25 mA

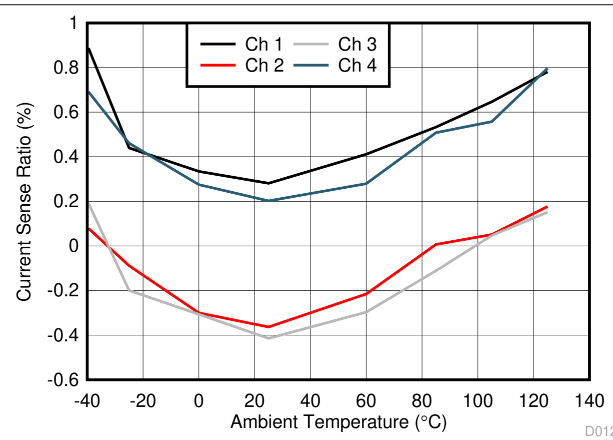


图 7-16. Current-Sense Ratio at 50 mA

7.7 Typical Characteristics (continued)

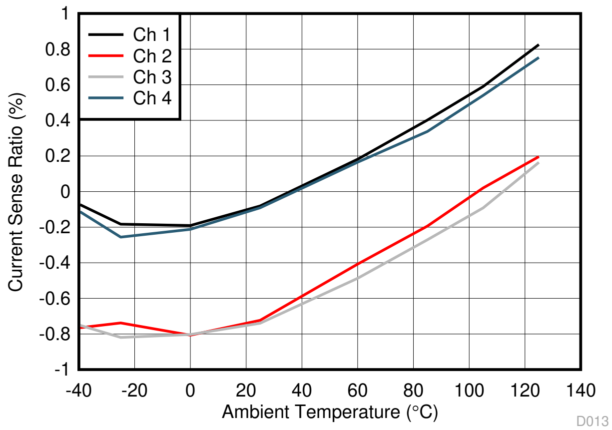


图 7-17. Current-Sense Ratio at 100 mA

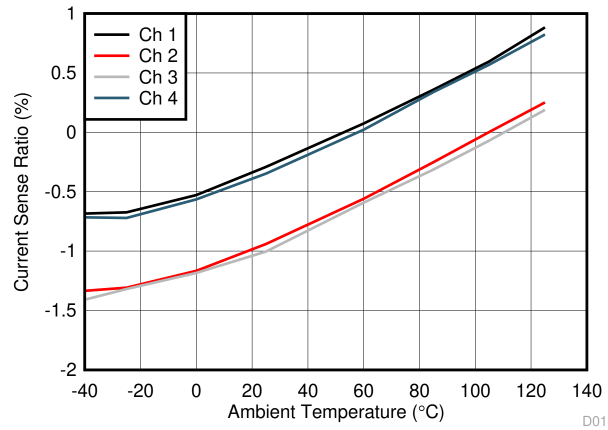


图 7-18. Current-Sense Ratio at 500 mA

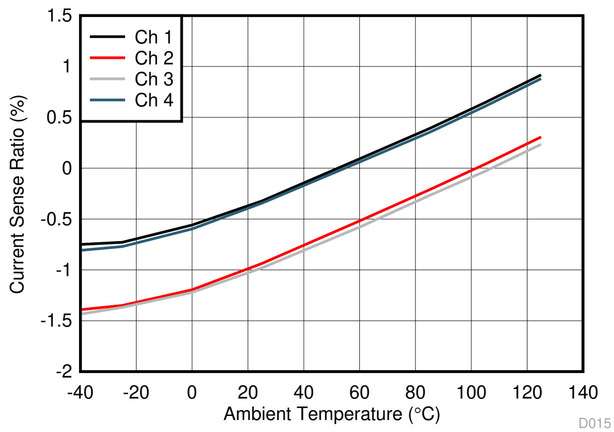


图 7-19. Current-Sense Ratio at 1 A

8 Detailed Description

8.1 Overview

The TPS274160 device is a quad-channel smart high-side switch, with an internal charge pump and NMOS power FETs. The TPS274160 device integrates fault diagnostics and a high-accuracy current-sense feature that enable intelligent control of the load. The adjustable current-limit function greatly improves the reliability of whole system. There are two versions of the device. The TPA274160A contains open drain digital output for diagnostic reporting. The TPS274160B device implements a high accuracy current sense analog output.

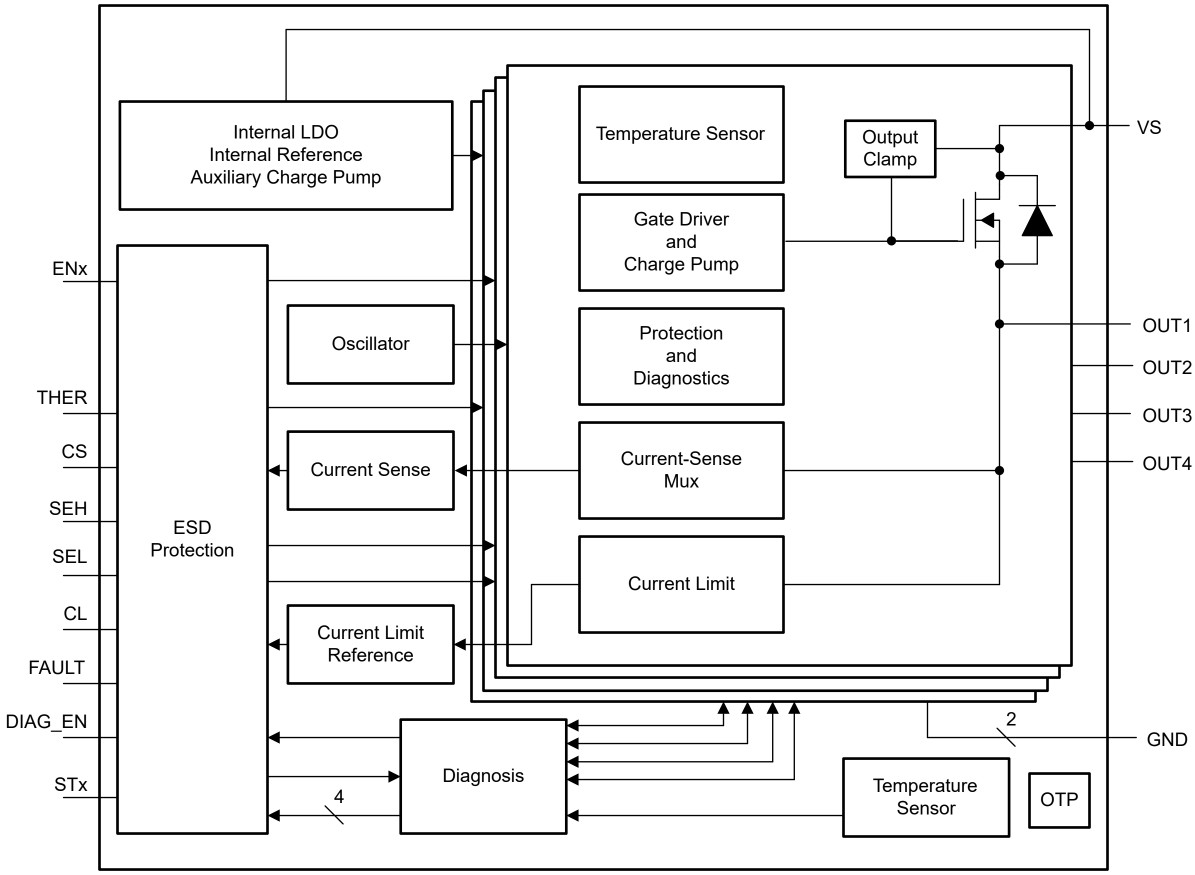
TPS274160A device implements the digital fault report with an open-drain structure. When a fault occurs, the device pulls $\overline{STx}$ down to GND. A 3.3- or 5-V external pullup is required to match the microcontroller supply level. The digital status of each channel can report individually, or globally by connecting the $\overline{STx}$ pins together.

The TPS274160B device integrates a high-accuracy current sense circuit that enables precise load current sensing without the need for on-board calibration. The integrated current mirror (selectable one-channel at a time) can source a fraction (1 / $K_{(CS)}$) of the load current. The mirrored current flows into the CS-pin resistor to become a voltage signal. $K_{(CS)}$ is a near-constant value across temperature and supply voltage. A wide linear region from 0 V to 4 V allows a better real-time load-current monitoring. The CS pin can also report a fault with pullup voltage of $V_{CS(H)}$.

The external high-accuracy current limit allows setting the current-limit value by applications. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The device can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage. Besides, the device also implements an internal current limit with a fixed value.

The TPS274160 device integrates active clamp between the drain and the source of the FETs. This clamp ensures that the device is protected during switch off cycle of inductive loads like relays, solenoids and valves. During the inductive load turn-off, the energy of the power supply and the load are dissipated on the high-side switch. The device also optimizes the switching-off slew rate when the clamp is active, which helps the system design by keeping the effects of transient power dissipation and EMI to a minimum.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Pin Current and Voltage Conventions

Note that throughout the data sheet, the current directions on the respective pins are as shown by the arrows in 图 8-1. All voltages are measured relative to the ground plane.

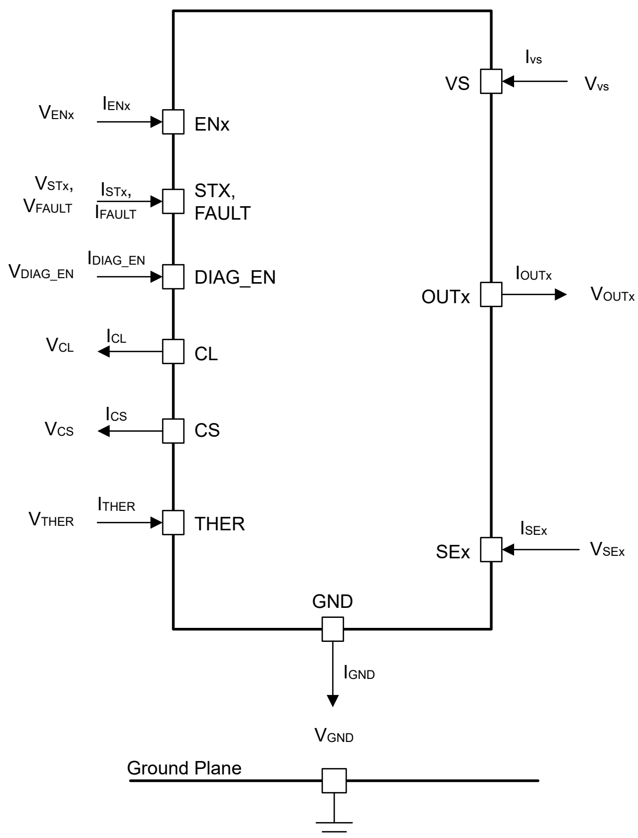


图 8-1. Voltage and Current Conventions

8.3.2 Accurate Current Sense

High-accuracy current sense is implemented in the TPS274160B device. This feature enables continuous current monitoring and accurate load diagnostic without extensive calibration.

The integrated current mirror sources 1 / $K_{(CS)}$ of the load current, and the mirrored current flows into the external current sense resistor to become a voltage signal. The current mirror is shared by the four channels. $K_{(CS)}$ is the ratio of the output current and the sense current. It is a constant value across the temperature and supply voltage. Each device is calibrated accurately during production, so post-calibration is not required. See 图 8-2 for more details.

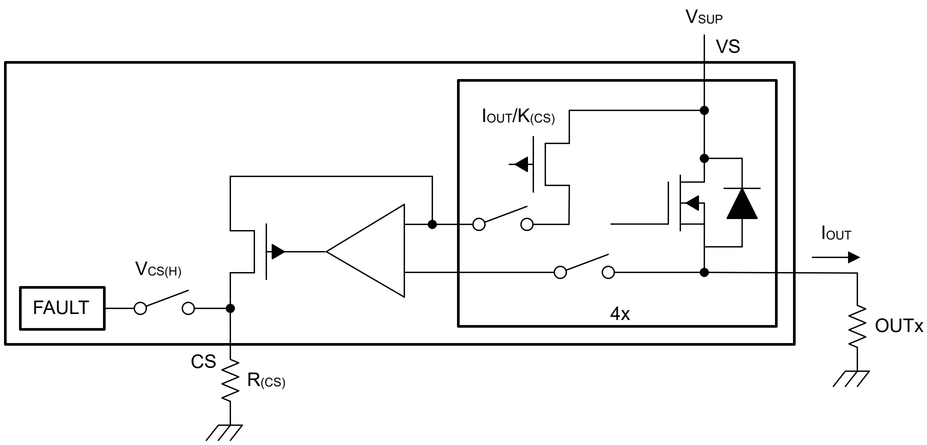


图 8-2. Current-Sense Block Diagram

When a fault occurs, the CS pin also works as a fault report with a pullup voltage, $V_{CS(H)}$. See 图 8-3 for more details.

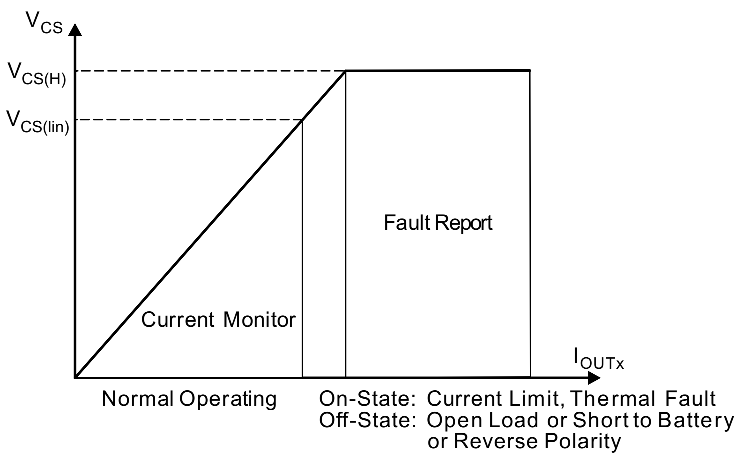


图 8-3. Current-Sense Output-Voltage Curve

Use 方程式 1 to calculate $R_{(CS)}$.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUTx}} \tag{1}$$

Take the following points into consideration when calculating $R_{(CS)}$.

- Ensure V_{CS} is within the current-sense linear region (V_{CS}, $I_{OUTx(lin)}$) across the full range of the load current. Check $R_{(CS)}$ with 方程式 2.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} \le \frac{V_{CS(lin)}}{I_{CS}} \tag{2}$$

- In fault mode, ensure I_{CS} is within the source capacity of the CS pin ($I_{CS(H)}$). Check $R_{(CS)}$ with 方程式 3.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} \ge \frac{V_{CS(H,min)}}{I_{CS(H,min)}} \tag{3}$$

8.3.3 Adjustable Current Limit

A high-accuracy current limit allows high reliability of the design. It protects the load and the power supply from overstressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When a current-limit threshold is hit, a closed loop activates immediately. The output current is clamped at the set value, and a fault is reported out. The device heats up due to the high power dissipation on the power FET. If thermal shutdown occurs, the current limit is set to $I_{CL(TSD)}$ to reduce the power dissipation on the power FET. See 图 8-4 for more details.

The device has two current-limit thresholds.

- Internal current limit – The internal current limit is fixed at $I_{CL(int)}$. Tie the CL pin directly to the device GND for large-transient-current applications.
- External adjustable current limit – An external resistor is used to set the current-limit threshold. Use the 方程式 4 to calculate the $R_{(CL)}$. $V_{CL(th)}$ is the internal band-gap voltage. $K_{(CL)}$ is the ratio of the output current and the current-limit set value. It is constant across the temperature and supply voltage. The external adjustable current limit allows the flexibility to set the current limit value by applications.

$$I_{CL} = \frac{V_{CL(th)}}{R_{(CL)}} = \frac{I_{OUT}}{K_{(CL)}}$$

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} \quad (4)$$

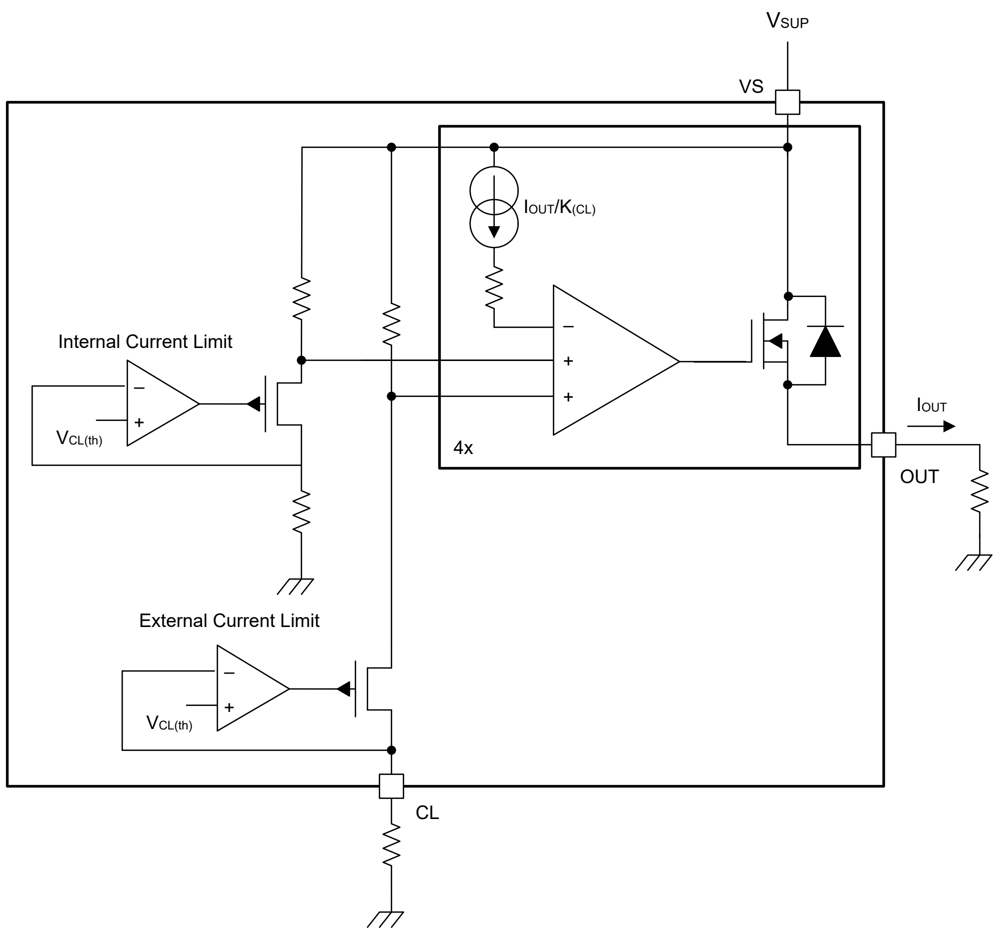


图 8-4. Current-Limit Block Diargam

Note that if using a GND network which causes a level shift between the device GND and board GND, the CL pin must be connected with device GND.

For better protection from a hard short-to-GND condition (when the ENx pins are enabled, a short to GND occurs suddenly), the device implements a fast-trip protection to turn off the related channel before the current-limit closed loop is set up. The fast-trip response time is less than 1 μs, typically. With this fast response, the device can achieve better inrush current-suppression performance.

8.3.4 Inductive-Load Turn-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

$$V_{DS(clamp)} = V_{VS} - V_{OUT} \tag{5}$$

During the period of demagnetization (t_{decay}), the power FET is turned on for inductance-energy dissipation. The inductive load energy is dissipated in the high-side switch. Total energy includes the energy of the power supply ($E_{(VS)}$) and the energy of the load ($E_{(load)}$). If resistance is in series with inductance, some of the load energy is dissipated on the resistance.

$$E_{(HSS)} = E_{(VS)} + E_{(load)} = E_{(VS)} + E_{(L)} - E_{(R)} \tag{6}$$

When an inductive load switches off, $E_{(HSS)}$ causes a high thermal stress on the device.. The upper limit of the power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

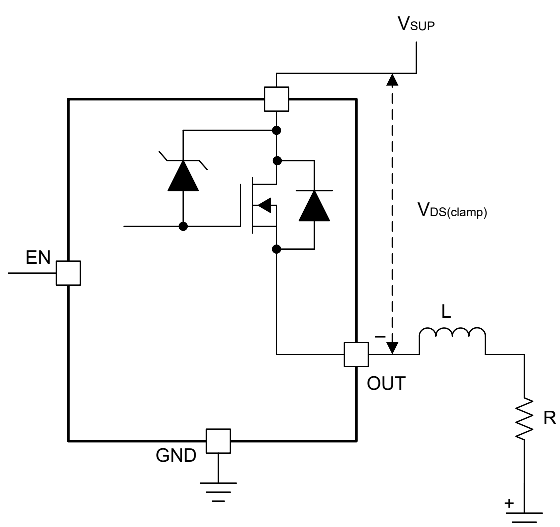


图 8-5. Drain-to-Source Clamping Structure

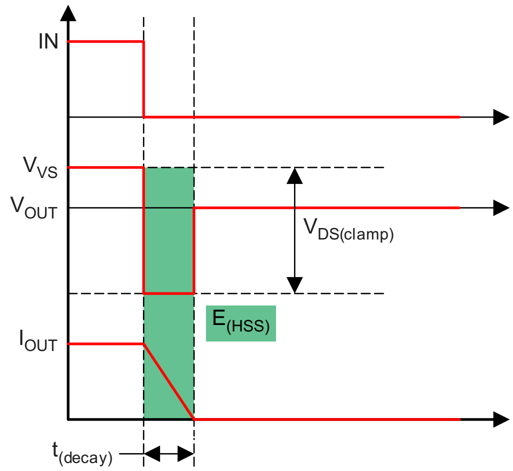


图 8-6. Inductive Load Switching-Off Diagram, note EN pin waveform referred to as IN

From the perspective of the high-side switch, $E_{(HSS)}$ equals the integration value during the demagnetization period.

$$E_{(HSS)} = \int_0^{t_{(decay)}} V_{DS(clamp)} \times I_{OUT}(t)\,dt$$

$$t_{(decay)} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)$$

$$E_{(HSS)} = L \times \frac{V_{VS} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(max)} - |V_{OUT}|\ \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \tag{7}$$

When R approximately equals 0, $E_{(HSD)}$ can be given simply as:

$$E_{(HSS)} = \frac{1}{2} \times L \times I^2_{OUT(max)} \frac{V_{VS} + |V_{OUT}|}{|V_{OUT}|} \tag{8}$$

图 8-7 is a waveform of the device driving an inductive load. Channel 1 is the EN signal (blue), channel 2 is the supply voltage V_{VS} (cyan), channel 3 is the output voltage V_{OUT} (magenta), channel 4 is the output current I_{OUT}(green), and channel M is the measured power dissipation $E_{(HSS)}$.

On the waveform, the duration of V_{OUT} from V_{VS} to (V_{VS} – $V_{DS(clamp)}$) is around 120 µs. The device optimizes the switch-off slew rate when the clamp is active. As shown in 图 8-7, the controlled slew rate is around 0.5 V/µs.

The 图 8-8 plots the maximum inductive energy (E_{AS}) that can be discharged safely by the device a function of the inductor load current in a single pulse in a single channel at one time. If the stored energy in the inductor at the particular load current is higher, then an external clamp will be required.

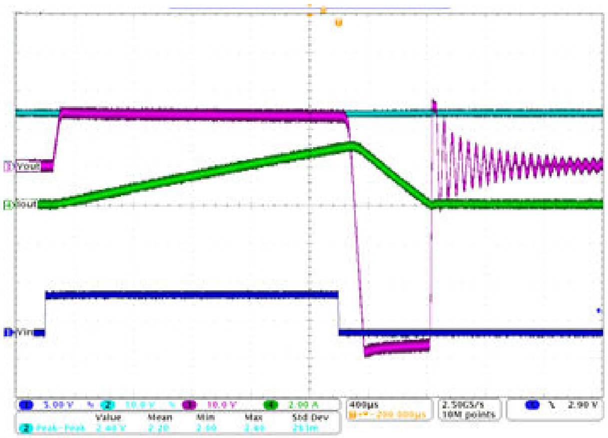


图 8-7. Inductive Load Switching-Off Waveform

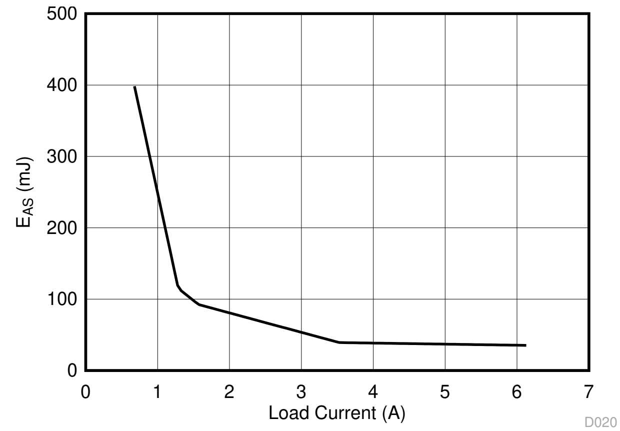


图 8-8. Maximum Energy Dissipation (E_{AS}) Allowed T_{J_start} = 125°C - Single Pulse, One Channel

Note that for PWM-controlled inductive loads, it is recommended to add the external freewheeling circuitry shown in 图 8-9 to protect the device from repetitive power stressing. The TVS clamp is used to achieve the fast decay. See 图 8-9 for more details.

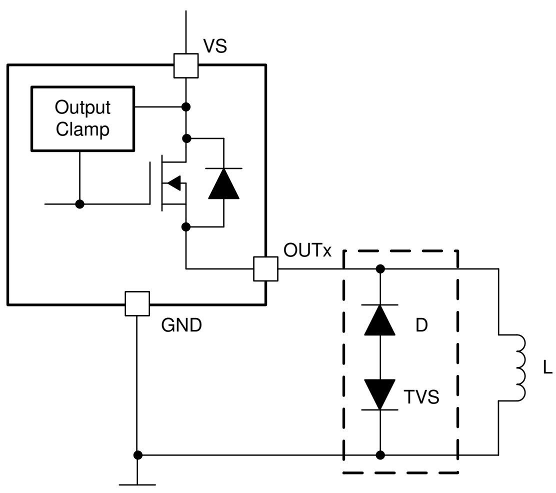


图 8-9. Protection With External Circuitry

8.3.5 Fault Detection and Reporting

8.3.5.1 Diagnostic Enable Function

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the MCU can use GPIOs to set DIAG_EN high to enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG_EN and ENx low.

8.3.5.2 Multiplexing of Current Sense

For version B, SEL and SEH are two pins to multiplex the shared current-sense function among the four channels. See 表 8-1 for more details.

表 8-1. Diagnosis Configuration Table

DIAG_EN	ENx	SEH	SEL	CS ACTIVATED CHANNEL	CS, $\overline{FAULT}$, $\overline{STx}$	PROTECTIONS AND DIAGNOSTICS
L	H	—	—	—	High impedance	Diagnostics disabled, full protection
	L					Diagnostics disabled, no protection
H	—	0	0	Channel 1	See 表 8-2	See Table 8-2
		0	1	Channel 2		
		1	0	Channel 3		
		1	1	Channel 4		

8.3.5.3 Fault Table

表 8-2 applies when the DIAG_EN pin is enabled.

表 8-2. Fault Table

CONDITIONS	ENx	OUTx	THER	CRITERION	$\overline{STx}$ (VER. A)	CS (VER. B)	$\overline{FAULT}$ (VER. B)	FAULT RECOVERY
Normal	L	L	—	—	H	0	H	—
	H	H	—	—	H	In linear region	H	—
Overlaod, short to ground	H	L	—	Current limit triggered	L	$V_{CS(H)}$	L	Auto
Open load(1), short to supply, reverse polarity	L	H	—	V_{VS} – V_{OUTx} < $V_{(ol,off)}$	L	$V_{CS(H)}$	L	Auto
Thermal shutdown	H	—	L	T_{SD} triggered	L	$V_{CS(H)}$	L	Output auto-retry. Fault recovers when T_J < $T_{(SD,rst)}$ or when ENx toggles.
			H					Output latch off. Fault recovers when ENx toggles.
Thermal swing	H	—	—	T_{SW} triggered	L	$V_{CS(H)}$	L	Auto

(1) An external pullup is required for open-load detection.

8.3.5.4 $\overline{STx}$ and $\overline{FAULT}$ Reporting

For version A, four individual $\overline{STx}$ pins report the fault conditions, each pin for its respective channel. When a fault condition occurs, it pulls $\overline{STx}$ down to GND. A 3.3- or 5-V external pullup is required to match the supply level of the microcontroller. The digital status of each channel can be reported individually, or globally by connecting all the $\overline{STx}$ pins together.

For version B, a global $\overline{FAULT}$ pin is used to monitor the global fault condition among all the channels. When a fault condition occurs on any channel, the $\overline{FAULT}$ pin is pulled down to GND. A 3.3-V or 5-V external pullup is required to match the supply level of the microcontroller.

After the $\overline{FAULT}$ report, the microcontroller can check and identify the channel in fault status by multiplexed current sensing. The CS pin also works as a fault report with an internal pullup voltage, $V_{CS(H)}$.

8.3.6 Full Diagnostics

8.3.6.1 Short-to-GND and Overload Detection

When a channel is on, a short to GND or overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The microcontroller can handle the overcurrent by turning off the switch. The device heats up if no actions are taken. If a thermal shutdown occurs, the current limit is $I_{CL(TSD)}$ to keep the power stressing on the power FET to a minimum. The device automatically recovers when the fault condition is removed.

8.3.6.2 Open-Load Detection

8.3.6.2.1 Channel On

When a channel is on and an open-load event occurs, it can be detected as an ultra-low V_{CS} voltage at the CS pin and handled by the micro-controller. The high-accuracy current sense in the low current range, enables the open-load detection at very low current thresholds. Note that the detection is not reported on the $\overline{STx}$ or $\overline{FAULT}$ pins. The microcontroller must proactively multiplex the SEL and SEH pins to detect the channel-on open-load fault.

8.3.6.2.2 Channel Off

When a channel is off, if a load is connected, the output is pulled down to GND. But if an open load occurs, the output voltage is close to the supply voltage (V_{VS} – V_{OUTx}< $V_{(ol,off)}$), and the fault is reported out.

There is always a leakage current $I_{(ol,off)}$ present on the output due to internal logic control path or external humidity, corrosion, and so forth. Thus, TI recommends an external pullup resistor to offset the leakage current when an open load is detected. The recommended pullup resistance is 20 kΩ.

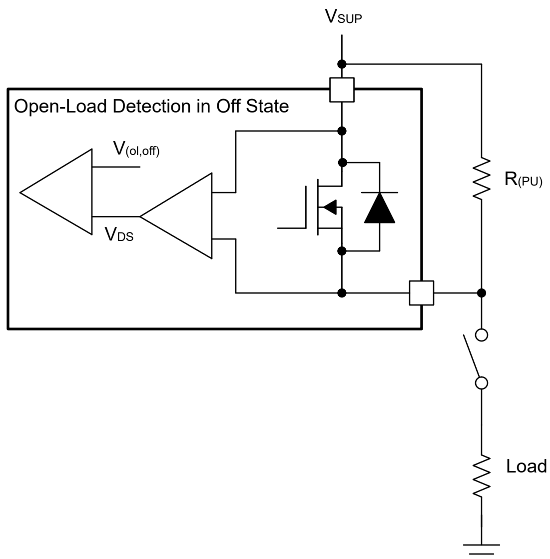


图 8-10. Open-Load Detection in Off-State

8.3.6.3 Short-to-Supply Detection

Short-to-supply has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state. See 表 8-2 for more details.

In the on-state, reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case occurs in the off-state.

- If V_{OUTx} – V_{VS} < $V_{(F)}$ (body diode forward voltage), no reverse current occurs.
- If V_{OUTx} – V_{VS} > $V_{(F)}$, reverse current occurs. The current must be limited to less than $I_{R(1)}$. Setting an ENx pin high can minimize the power stress on its channel. Also, for external reverse protection, see Reverse-Current Protection for more details.

8.3.6.4 Input Reverse Polarity Detection

Reverse polarity detection has the same detection mechanism and behavior as open-load detection both in the on-state and off-state. See 表 8-2 for more details.

In the on-state, the reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case occurs in the off-state. The reverse current must be limited to less than $I_{R(2)}$.

Set the related ENx pin high to keep the power dissipation to a minimum. For external reverse-blocking circuitry, see Reverse-Current Protection for more details.

8.3.6.5 Thermal Fault Detection

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing). Respective temperature sensors are integrated close to each power FET, so the thermal fault is reported by each channel. This arrangement can help the device keep the cross-channel effect to a minimum when some channels are in a thermal fault condition.

8.3.6.5.1 Thermal Shutdown

Thermal shutdown is active when the absolute temperature $T_J > T_{(SD)}$. When thefrmal shutdown occurs, the respective output turns off. The THER pin is used to configure the behavior after the thermal shutdown occurs.

- When the THER pin is low, thermal shutdown operates in the auto-retry mode. The output automatically recovers when $T_J < T_{(SD)} - T_{(hys)}$, but the current is limited to $I_{CL(TSD)}$ to avoid repetitive thermal shutdown. The thermal shutdown fault signal is cleared when $T_J < T_{(SD,rst)}$ or after toggling the related ENx pin.
- When the THER pin is high, thermal shutdown operates in the latch mode. The output latches off when thermal shutdown occurs. When the THER pin goes from high to low, thermal shutdown changes to auto-retry mode. The thermal shutdown fault signal is cleared after toggling the related ENx pin.

Thermal swing activates when the power FET temperature is increasing sharply, that is, when $\Delta T = T_{(FET)} - T_{(Logic)} > T_{(sw)}$, then the output turns off. The output automatically recovers and the fault signal clears when $\Delta T = T_{(FET)} - T_{(Logic)} < T_{(sw)} - T_{(hys)}$. Thermal swing function improves the device reliability when subjected to repetitive fast thermal variation. As shown in 图 8-11, multiple thermal swings are triggered before thermal shutdown occurs.

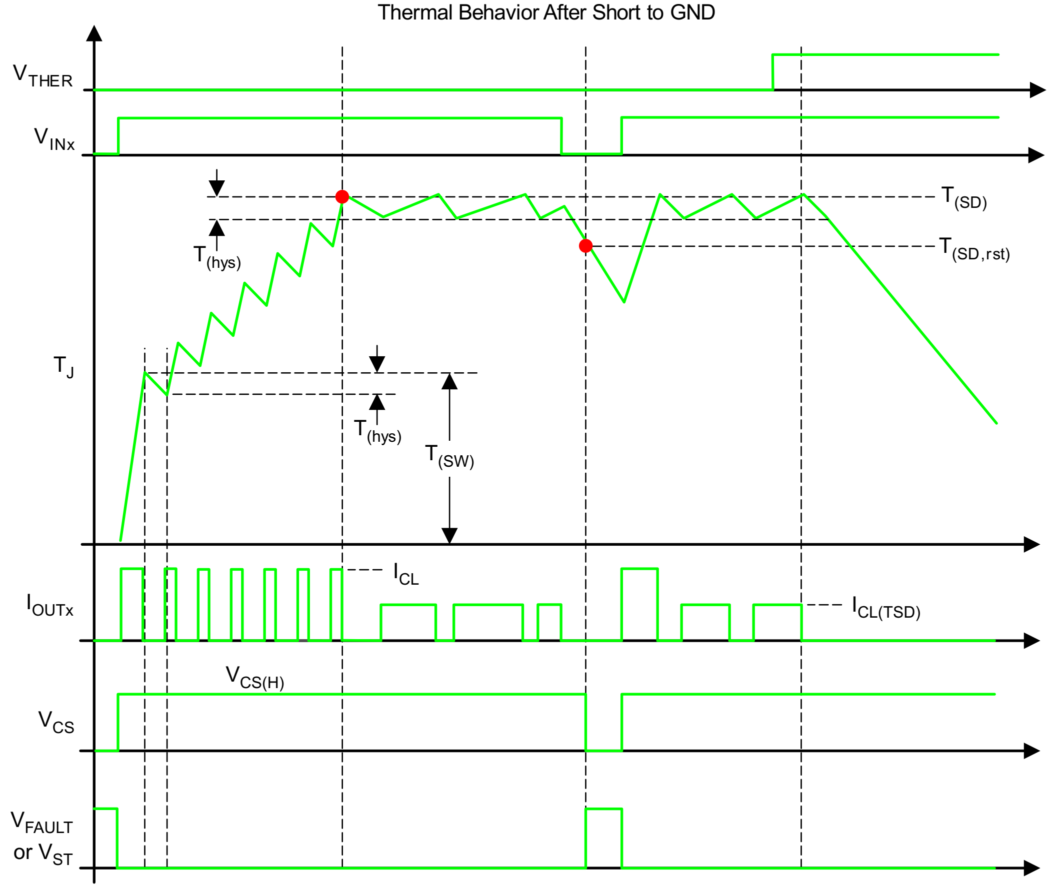


图 8-11. Thermal Behavior Diagram

8.3.7 Full Protections

8.3.7.1 UVLO Protection

The device monitors the supply voltage V_{VS}, to prevent unpredicted behaviors when V_{VS} is too low. When V_{VS} falls down to $V_{VS(uvf)}$, the device shuts down. When V_{VS} rises up to $V_{VS(uvr)}$, the device turns on.

8.3.7.2 Loss-of-GND Protection

When loss of GND occurs, output is shut down regardless of whether the ENx pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND.

8.3.7.3 Protection for Loss of Power Supply

When loss of supply occurs, the output is shut down regardless of whether the ENx pin is high or low. For a resistive or a capacitive load, loss of supply has no risk. But for a charged inductive load, the current is driven from all the I/O pins to maintain the inductance current. To protect the system in this condition, TI recommends two types of external protections: the GND network or the external free-wheeling diode. In addition, the recommended components per the application diagram needs to be implemented for protection.

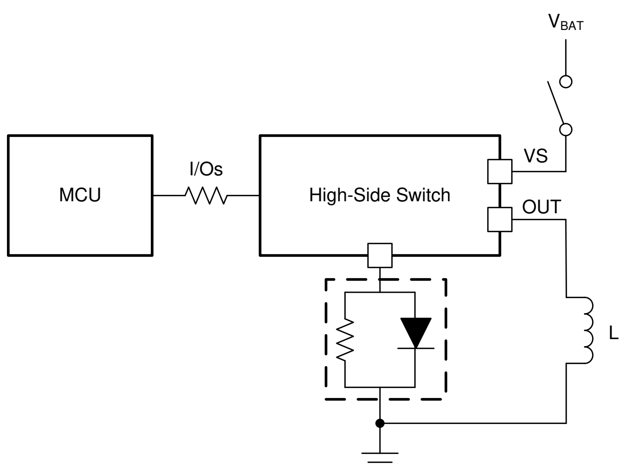


图 8-12. Protection for Loss of Power Supply, Method 1

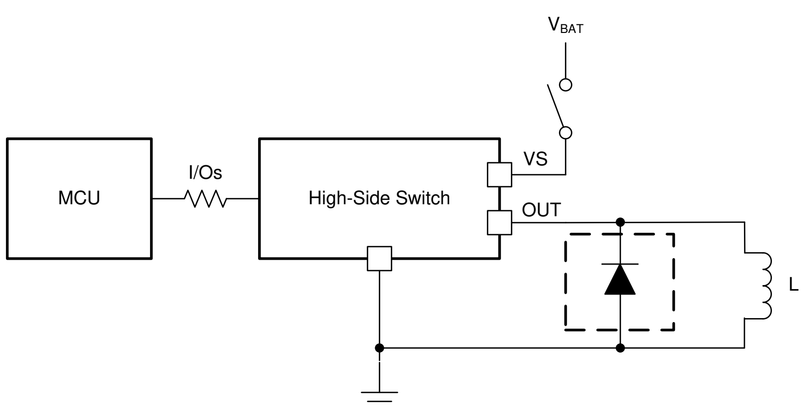


图 8-13. Protection for Loss of Power Supply, Method 2

8.3.7.4 Reverse-Current Protection

Reverse current occurs in two conditions: short to supply and reverse polarity.

- When a short to the supply occurs, there is only reverse current through the body diode. $I_{R(1)}$ specifies the limit of the reverse current.

- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. $I_{R(2)}$ specifies the limit of the reverse current.

To protect the device, TI recommends two types of external circuitry.

- Adding a blocking diode. Both the IC and load are protected when in reverse polarity.

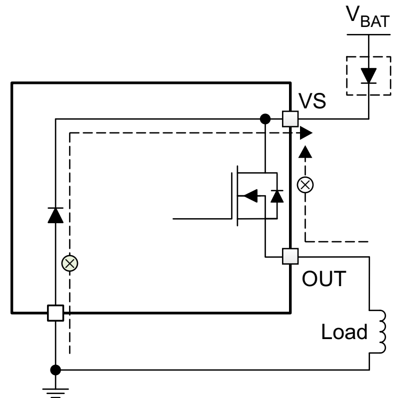


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图 8-14. Reverse-Current External Protection, Method 1

- Adding a GND network. The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended selection are 1-kΩ resistor in parallel with an > 100-mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices. The reverse current protection diode in the GND network forward voltage should be less than 0.6 V in any circumstances. In addition a minimum resistance of 4.7 K is recommended on the I/O pins.

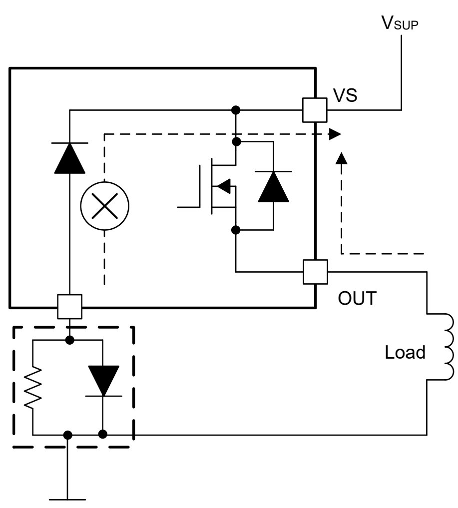


图 8-15. Reverse-Current External Protection, Method 2

8.3.7.5 MCU I/O Protection

In some severe conditions, such as the high voltage transients or the loss of supply with inductive loads, a negative pulse occurs on the GND pin This pulse can cause damage on the connected microcontroller. TI recommends serial resistors to protect the microcontroller, for example, 4.7-kΩ when using a 3.3-V microcontroller and 10-kΩ for a 5-V microcontroller.

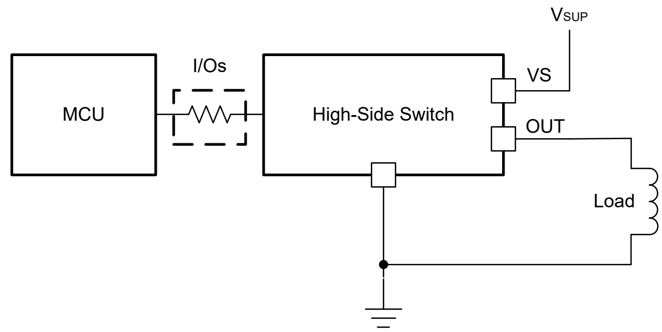


图 8-16. MCU I/O External Protection

8.4 Device Functional Modes

8.4.1 Working Modes

The device has three working modes, the normal mode, the standby mode, and the standby mode with diagnostics.

Note that IN must be low for t > $t_{(off,deg)}$ to enter the standby mode, where $t_{(off,deg)}$ is the standby mode deglitch time used to avoid false triggering. 图 8-17 shows a working-mode diagram.

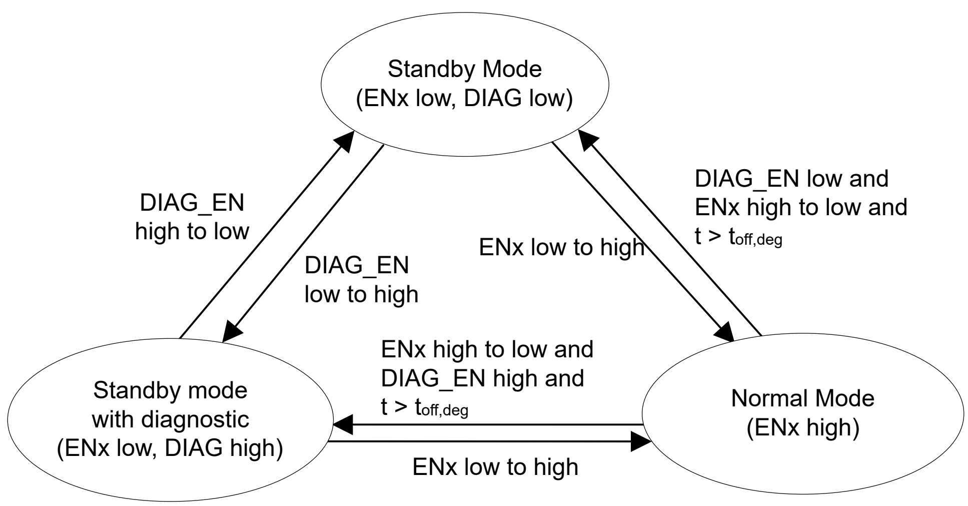


图 8-17. Working Modes

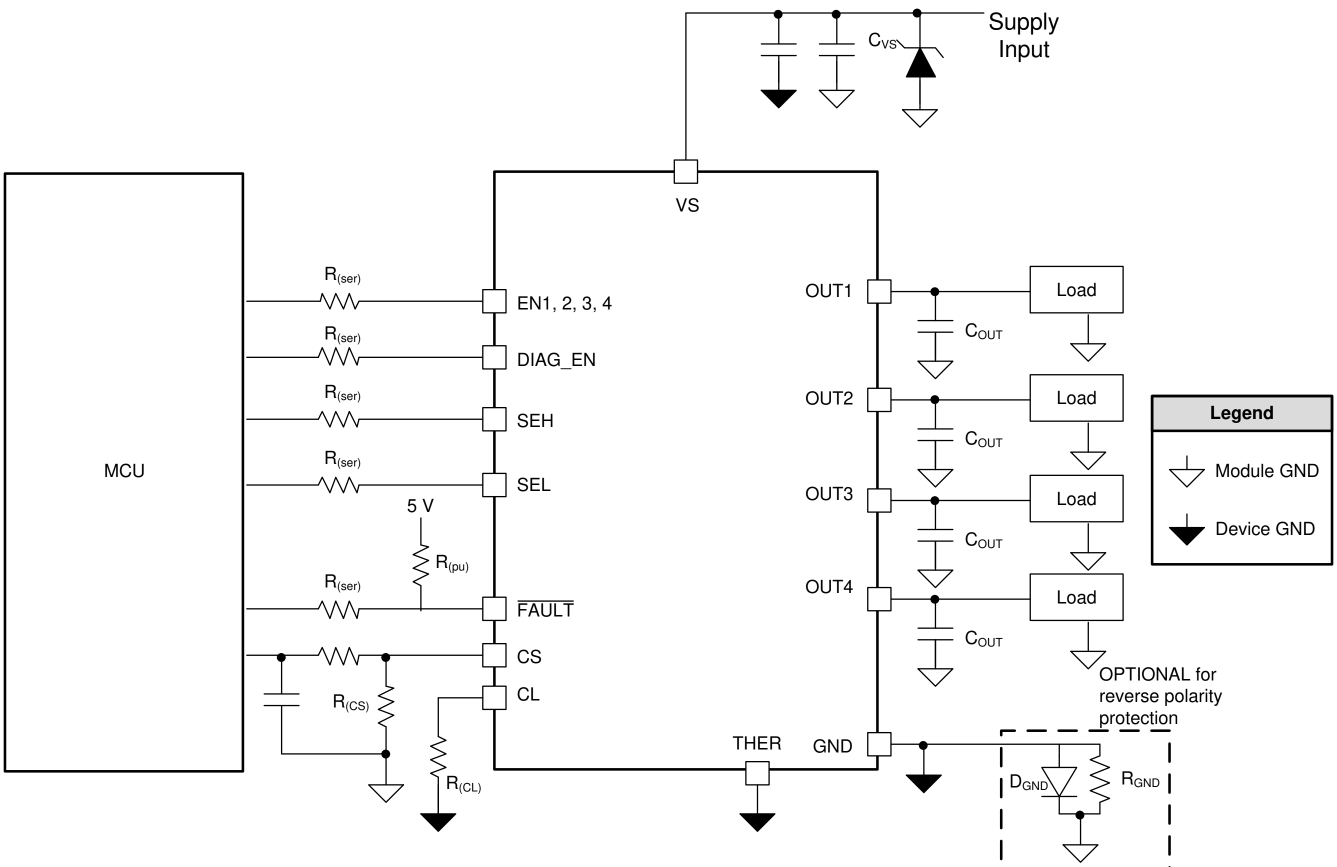
9 Application and Implementation

Note

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

图 9-1 shows the schematic of a typical application of the . It includes all standard external components. This section of the datasheet discusses the considerations in implementing commonly required application functionality.



With the ground protection network, the device ground will be offset relative to the microcontroller ground.

图 9-1. System Diagram

表 9-1. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
$R_{(ser)}$	10 kΩ	Protect microcontroller and device I/O pins
$R_{(CS)}$	1 kΩ	Translate the sense current into sense voltage
C_{SNS}	100 pF - 10 nF	Low-pass filter for the ADC input
R_{GND}	1 kΩ	Stabilize GND potential during turn-off of inductive load
D_{GND}	BAS21 Diode	Protects device during reverse supply condition
$R_{(CL)}$	1-kΩ typical	Set current limiting value, short to IC GND to set the current limit to the internal setting.

表 9-1. Recommended External Components (continued)

COMPONENT	TYPICAL VALUE	PURPOSE
C_{VS}	10 nF to Device GND and 100 nF to module GND	Filtering of voltage transients (for example, surge)
Z_{VS}	TVS to module GND	Clamp voltage spikes at the input.
C_{OUT}	22 nF	Filtering of voltage transients (for example, ESD)

9.2 Typical Application

The following figure shows example of a typical application based on the TPS274160B device. The loads can be varied and be different on each channel.

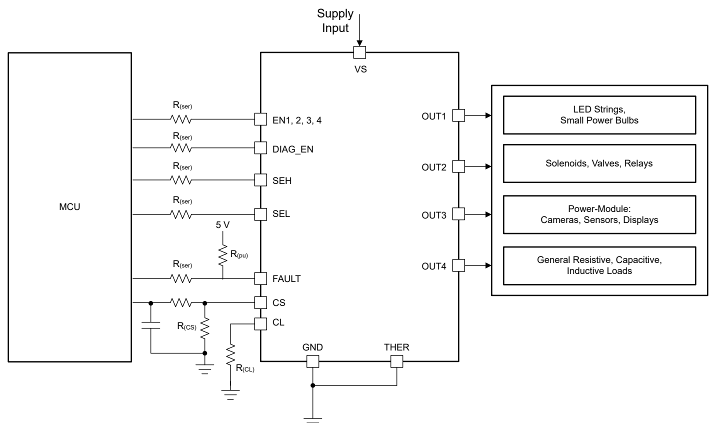


图 9-2. Typical Application Diagram.

9.2.1 Design Requirements

- V_{VS} = 24-V nominal
- Load range is from 0.1 A to 1 A for each channel
- Current sense for fault monitoring
- Expected current-limit value of 2.5 A
- Automatic recovery mode when thermal shutdown occurs
- Full diagnostics with 5-V MCU

9.2.2 Detailed Design Procedure

To keep the 1-A nominal current in the 0 to 4-V current-sense range, calculate the $R_{(CS)}$ resistor using 方程式 9. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUT}} = \frac{4 \times 300}{1} = 1200\ \Omega \tag{9}$$

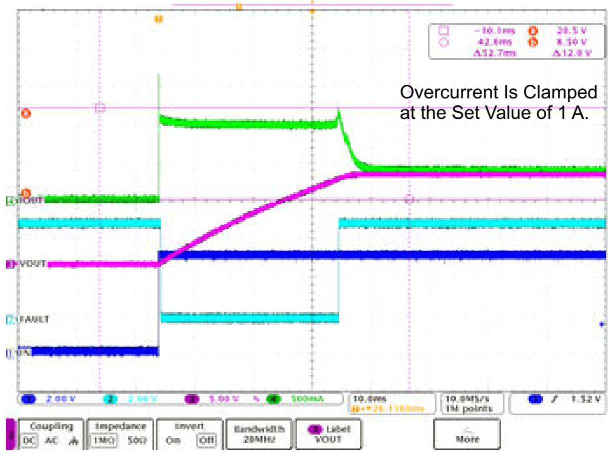
To set the adjustable current limit value at 2.5-A, calculate $R_{(CL)}$ using 方程式 10.

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} = \frac{0.8 \times 2500}{2.5} = 800\ \Omega \tag{10}$$

TI recommends $R_{(ser)}$ = 10 kΩ for 5-V MCU, and $R_{(pu)}$ = 10 kΩ as the pullup resistor.

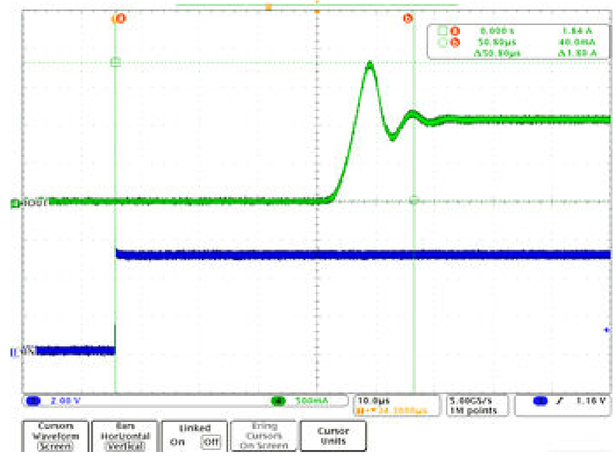
9.3 Capacitive Load Drive and Application Curves

In this application example we show the case of driving a large capacitive load at the input of a sensor hub supply node. The input capacitance is a 2.3-mF capacitor and is charged to a 12-V supply voltage . The nominal total load current at the node is 0.4 A and the current limit is set to 1 A and chosen to be well in excess of the peak load current. 图 9-3 shows a test example of soft-start when driving the large capacitive load. 图 9-4 shows an expanded waveform of the output current.



V_S = 12 V	ENx = ↑	Current limit = 1 A
Load current = 0.4 A	C_L = 2.3 mF	CH1 = ENx
CH2 = $\overline{FAULT}$	CH3 = output voltage	CH4 = output current

图 9-3. Driving a Capacitive Load With Adjustable Current Limit



V_{VS} = 12 V	ENx = ↑	Current limit = 1 A
Load current = 0.4 A	C_L = 2.3 mF	CH1 = ENx
CH2 = $\overline{FAULT}$	CH3 = output voltage	CH4 = output current

图 9-4. Driving a Capacitive Load, Expanded Waveform

10 Power Supply Recommendations

The TPS274160 device is designed to operate with a 12-V or 24-V nominal DC supply input. The DC supply voltage range should be within the range specified in the *Recommended Operating Conditions*. The device is also designed to withstand voltage transients beyond this range at the supply input pin up to the absolute maximum voltage specifications.

11 Layout

11.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. The WQFN package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

11.2 Layout Examples

11.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

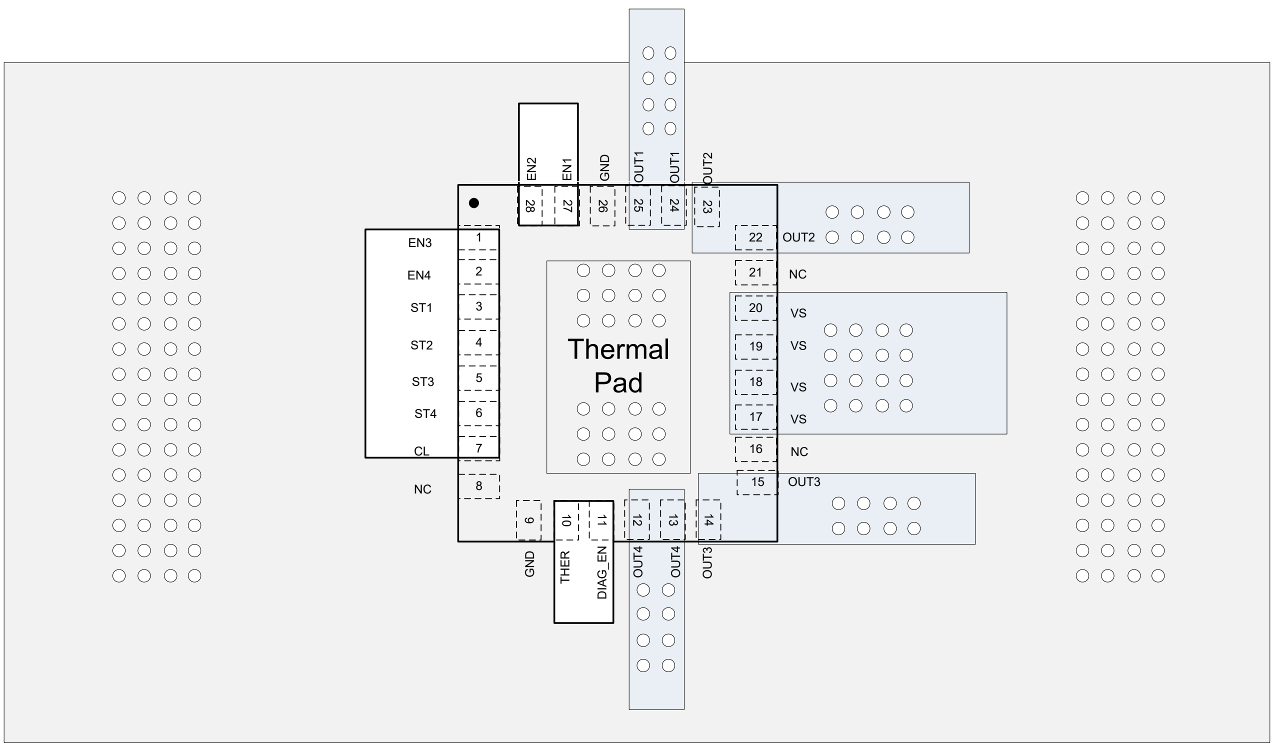


图 11-1. Layout Example Without a GND Network

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

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12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS274160ARLHR	Active	Production	WQFN (RLH) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	274160A
TPS274160ARLHR.A	Active	Production	WQFN (RLH) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	274160A
TPS274160ARLHRG4	Active	Production	WQFN (RLH) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	274160A
TPS274160ARLHRG4.A	Active	Production	WQFN (RLH) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	274160A
TPS274160BRLHR	Active	Production	WQFN (RLH) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	274160B
TPS274160BRLHR.A	Active	Production	WQFN (RLH) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	274160B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

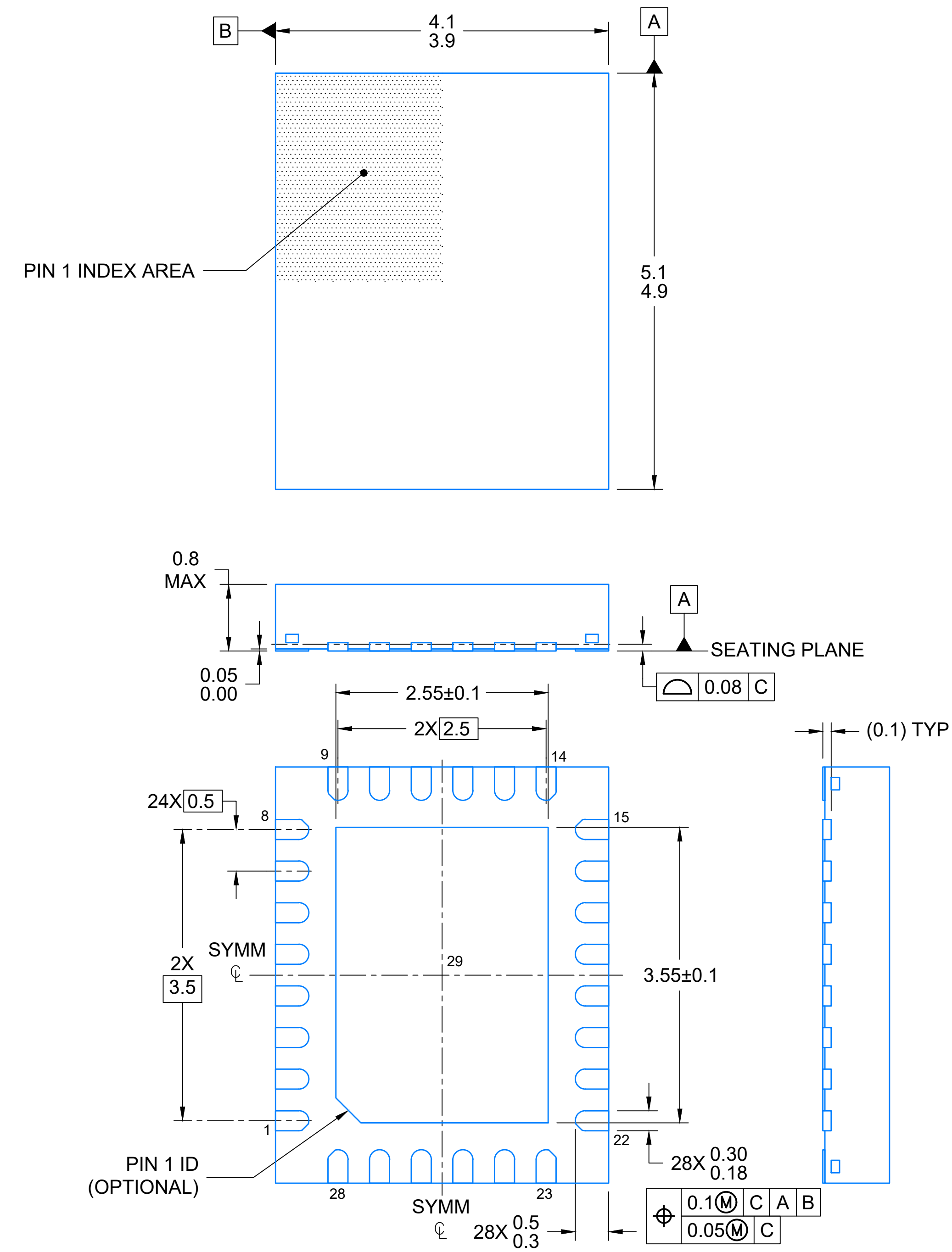
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

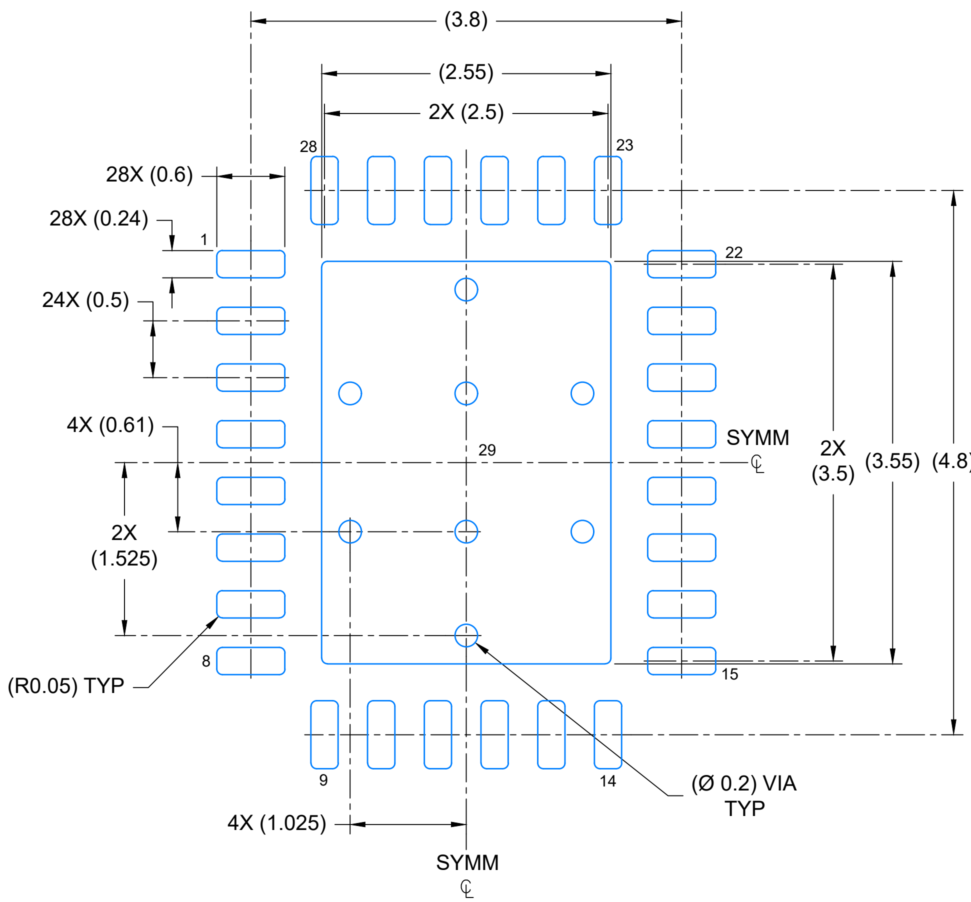
PLASTIC QUAD FLATPACK- NO LEAD



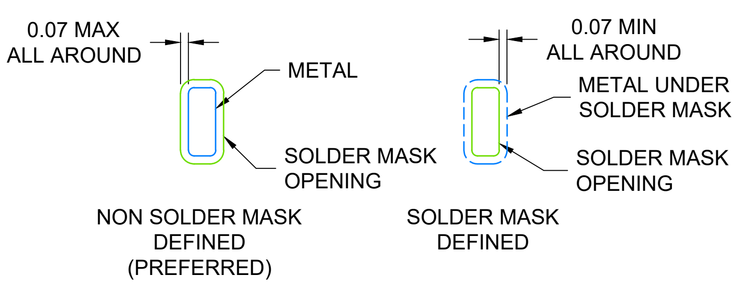
4224734/A 12/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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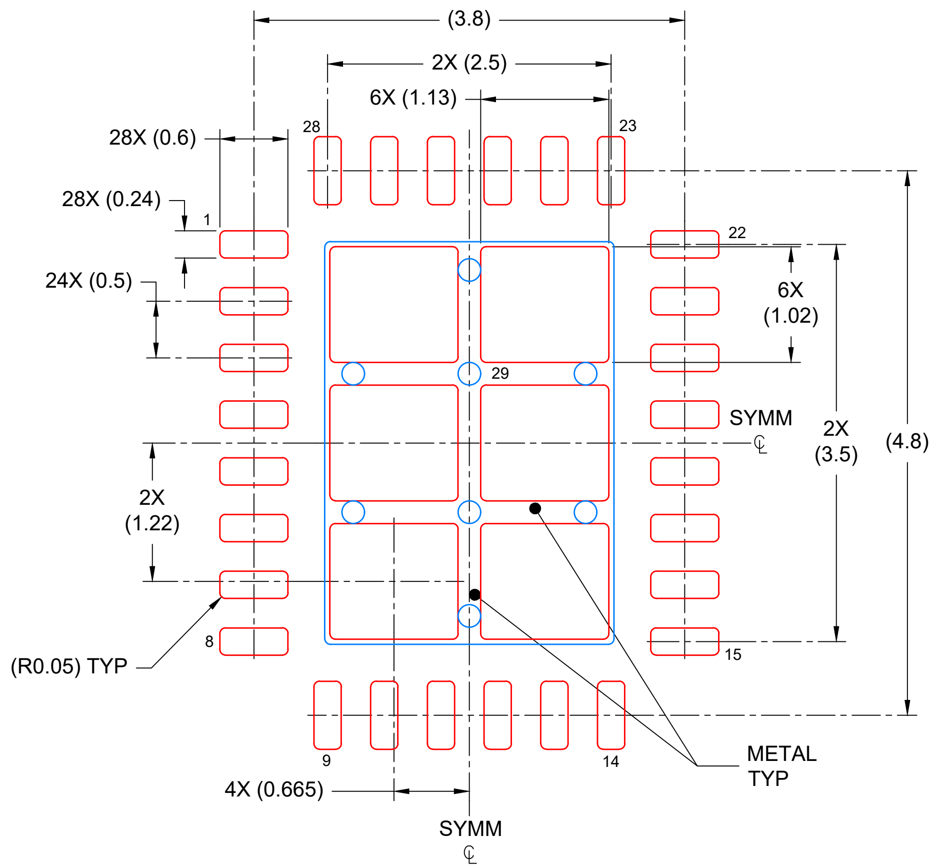
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
76% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.