

支持可调转换率、快速瞬态隔离和滞后控制的 1.2V - 8V, 3A 聚合物薄膜场效应晶体管 (PFET) 负载开关

查询样品: [TPS27082L](#)

特性

- 低导通电阻, 高电流 **PFET**
 - $V_{GS} = -4.5V$ 时, $R_{导通} = 32m\Omega$ (典型值)
 - $V_{GS} = -3.0V$ 时, $R_{导通} = 44m\Omega$ (典型值)
 - $V_{GS} = -1.8V$ 时, $R_{导通} = 85m\Omega$ (典型值)
 - $V_{GS} = -1.5V$ 时, $R_{导通} = 97m\Omega$ (典型值)
 - $V_{GS} = -1.2V$ 时, $R_{导通} = 155m\Omega$ (典型值)
- 可调接通和关闭转换率
 - $V_{IN} = 5V$ 时, 缺省最小输出上升时间为 **10 μ s**
- 可配置接通和关闭转换率
- 支持 **1.2V** 到高达 **8V** 的宽范围 V_{IN}
- 出色的关闭隔离, 即使在快速输入瞬态下也是如此
- 支持可调滞后的 **1.0V** 至 **8V** 的 **NMOS** 控制逻辑接口
- 完全不受静电放电 (**ESD**) 的影响 (所有引脚)
 - 人体模型 (**HBM**) **2kV**, 充电器件模型 (**CDM**) **500V**
- 极低的导通状态静态电流 (低至 **1.2 μ A**)
- 极低的关闭状态泄露电流 (典型值为 **100nA**)
- 采用 **2.9mm x 1.6mm x 0.75mm** 小外形尺寸晶体管 (**SOT**)-23 (**DDC**) 封装

应用范围

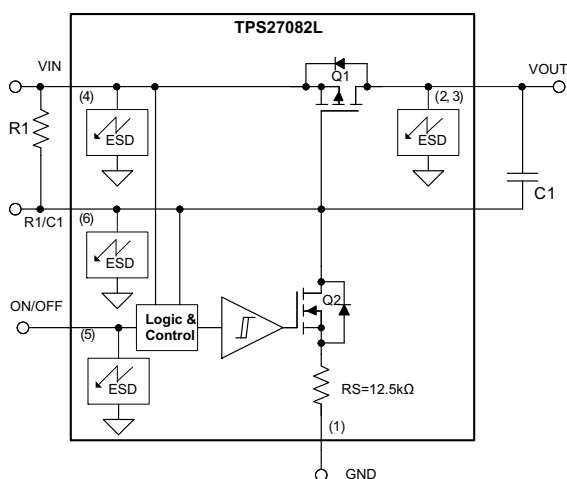
- 高侧负载开关
- 涌入电流控制
- 电源排序和控制
- 待机电源隔离
- 便携式电源开关

说明

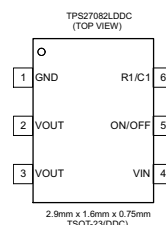
TPS27082L 集成电路 (IC) 是一款高侧负载开关, 此器件在微小的薄型小外形尺寸晶体管 (TSOT)-23 封装内集成了一个功率 PFET 和一个控制电路。TPS27082L 需要极低的导通状态静态电流并提供极低的关闭状态泄露电流, 从而优化了系统功效。

TPS27082L 导通/关闭逻辑接口特有滞后功能, 从而提供了一个稳健耐用的逻辑接口, 即使在非常嘈杂的运行条件下也是如此。TPS27082L 导通/关闭接口支持与低至 1V 的低压通用输入输出接口 (GPIO) 的直接对接。在无需外部电平位移器的情况下, TPS27082L 可将导通/关闭逻辑信号的电平位移至 V_{IN} 的电平。

TPS27082L 特有一个创新型关闭隔离电路, 此电路在负载开关处于关闭状态时可防止 V_{IN} 引脚上的 PMOS 在有可能具有快速瞬态的应用中被开启。



简化方框图 & 应用图



TPS27082L 封装 (DDC)

组件表 (典型应用)

组件	说明
R1	电平位移上拉电阻器
C1	可选 ⁽¹⁾

(1) 负载浪涌电流 (转换率) 控制需要此选项。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾⁽²⁾

T _J	PART NUMBER	PACKAGE		TOP-SIDE MARKING
–40°C to 125°C	TPS27082LDDCR	6-Pin Thin SOT	Reel of 3000	BU_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Contact factory for details and availability for PREVIEW devices, minimum order quantity may apply.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾⁽³⁾

Specified at T_J = –40°C to 125°C (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
V _{INmax} , V _{OUTmax}	V _{IN} , V _{OUT} pin maximum voltage with respect to GND pin	–0.1	8	V
V _{ON/OFF}	ON/OFF control voltage	–0.3	8	V
I _{Q1-ON}	Max continuous drain current of Q1		3	A
	Max pulsed drain current of Q1 ⁽⁴⁾		9.5	
P _D	Max power dissipation at T _A = 25°C, T _J = 150°C ⁽⁴⁾		1190	mW
All pins	ESD Rating – HBM		2000	V
	ESD Rating – CDM		500	V
T _A	Operating free-air ambient temperature range	–40	125 ⁽⁵⁾	°C
T _{J-max}	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Operating at the absolute T_{J-max} of 150°C can affect reliability – for higher reliability it is recommended to ensure T_J < 125°C
- (3) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance.
- (4) Pulse Width < 300µs, Duty Cycle < 2%
- (5) T_{J-max} limits and other related conditions apply. Refer to SOA charts, [Figure 8](#) through [Figure 13](#)

DISSIPATION RATINGS⁽¹⁾⁽²⁾⁽³⁾

BOARD	PACKAGE	θ _{JC}	θ _{JA} ⁽⁴⁾	T _A < 25°C	T _A = 70°C	T _A = 85°C	T _A = 105°C	DERATING FACTOR ABOVE T _A = 25°C
High-K (JEDEC 51-7)	6-Pin TSOT (DDC)	43°C/W	105°C/W	1190 mW	760 mW	619 mW	428 mW	9.55 mW/°C

- (1) Maximum dissipation values for retaining a maximum allowable device junction temperature of 150°C
- (2) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance
- (3) Package thermal data based on a 76x114x1.6mm, 4-layer board with 2-oz Copper on outer layers
- (4) Operating at the absolute T_{J-max} of 150°C can affect reliability; T_J ≤ 125°C is recommended

ELECTRICAL CHARACTERISTICS

Full temperature range spans $T_J = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A =T _J = 25°C			FULL TEMP RANGE ⁽¹⁾		UNIT
			MIN	TYP	MAX	MIN	MAX	
OFF CHARACTERISTICS								
BV _{IN}	VIN breakdown voltage	V _{ON/OFF} = 0 V, VGS(Q1) = 0 V, ID(Q1) = 250 μA	-8		-8		V	
I _{FIN}	VIN pin total forward leakage current ⁽²⁾	VIN = 8 V, ON/OFF = 0 V, RL = 2.5 Ω	0.15		30		μA	
		VIN = 5 V, ON/OFF = 0 V, RL = 2.5 Ω	0.04		12			
ON CHARACTERISTICS ⁽³⁾								
V _{T+} (VIH)	Positive going ON/OFF threshold voltage ⁽⁴⁾	VIN = 5.0 V, R1 = 125 kΩ ⁽¹⁾ , RL = 2.5 Ω			1.0		V	
		VIN = 5.0 V, R1 = 1 MΩ, RL = 2.5 Ω			1.0			
V _{T-} (VIL)	Negative going ON/OFF threshold voltage ⁽⁴⁾	VIN = 5.0 V, ID(Q1) < 175 μA, R1 =125 kΩ ⁽¹⁾			400		mV	
		VIN = 5.0 V, ID(Q1) < 175 μA, R1 = 1 MΩ			270			
ΔV _T (V _{T+} -V _{T-})	ON/OFF input logic hysteresis ⁽⁴⁾	VIN = 5.0 V, R1 = 125 kΩ ⁽¹⁾			600		V	
		VIN = 5.0 V, R1 = 1 MΩ			730			
R _{Q1(ON)}	Q1 Channel ON resistance ⁽⁵⁾	VGS _{Q1} = -4.5V, ID = 3.0 A	32	52	64		mΩ	
		VGS1 _{Q1} = -3.0V, ID =2 .5 A	44	66	84			
		VGS1 _{Q1} = -2.5V, ID = 2.5 A	50	76	92			
		VGS _{Q1} = -1.8V, ID = 2.0 A	82	113	147			
		VGS _{Q1} = -1.5V, ID = 1.0 A	97	150	173			
		VGS _{Q1} = -1.2V, ID = 0.50 A	155	250	260			
RGND _{ON}	R1/C1 pin to GND pin resistance when Q2 is ON	V _{ON/OFF} = 1.8 V	12.5	14.2	14.5		kΩ	
Q1 DRAIN-SOURCE DIODE PARAMETERS ⁽¹⁾⁽³⁾⁽⁶⁾								
IF _{SD}	Source-drain diode peak forward current	VF _{SD(Q1)} = 0.8V, VON/OFF = 0 V	1.0				A	
VF _{SD}	Source-drain diode forward voltage	IF _{SD(Q1)} = -0.6A, VON/OFF = 0 V			1.0		V	

(1) Specified by design only

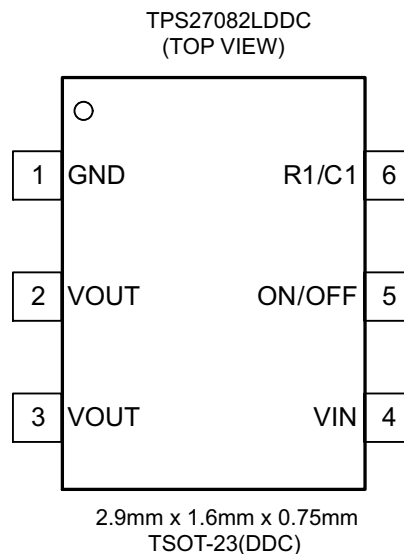
(2) Refer to I_{FVIN} plots for more information

(3) Pulse width $< 300\mu\text{s}$, Duty cycle $< 2\%$

(4) Refer to charts for more information on V_{T+}/V_{T-} thresholds

(5) Refer to SOA charts for operating current information

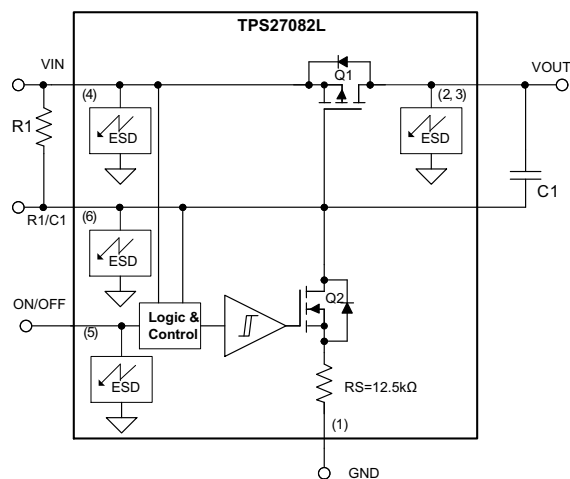
(6) Not rated for continuous current operation



TPS27082LD and TPS27082LDRV PINOUT

PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
GND	1	Connect to the system GND
VOUT	2, 3	Drain Terminal of Power PFET (Q1) – If required, connect a slew control capacitor between pins VOUT and R1/C1
VIN	4	Source Terminal of Power PFET (Q1) – connect a pull-up resistor between the pins VIN and R1/C1
ON/OFF	5	Active high enable – when driven with a high impedance driver, connect an external pull down resistor to GND
R1/C1	6	Gate Terminal of Power PFET (Q1)



Typical Application Diagram

APPLICATION INFORMATION

The TPS27082L IC is a high side load switch that integrates a Power PFET and its control circuit in a tiny TSOT-23 package. TPS27082L supports up to 8V supply input and up to 3A of load current. The TPS27082L can be used in a variety of applications. Figure 1 shows a general application of TPS27082L to control capacitive load inrush current.

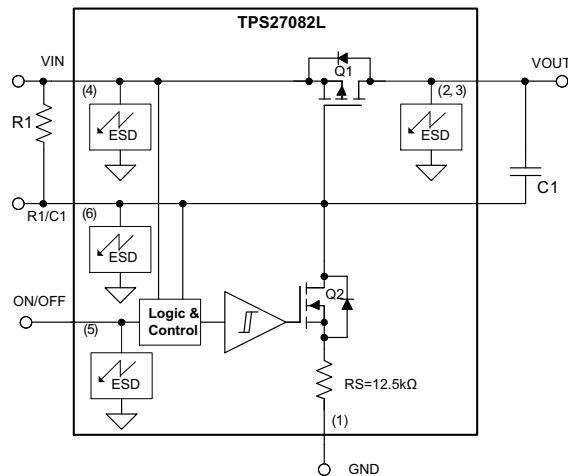


Figure 1. Typical Application Diagram

Configuring Q1 ON resistance

V_{GS-Q1} , Gate-Source voltage, of PMOS transistor Q1 sets its ON resistance $R_{Q1(ON)}$. Connecting a high value pull up resistor R1 maximizes ON state V_{GS-Q1} and thus minimizes the VIN to VOUT voltage drop. Use the following equation for calculating V_{GS-Q1} :

$$V_{GS-Q1} = -VIN \times \frac{R1}{R1 + 12.5 \text{ k}\Omega} \quad (1)$$

e.g. $R1 = 125 \text{ k}\Omega$, $VIN = 5 \text{ V}$ sets $V_{GS-Q1} = -4.5 \text{ V}$

NOTE

It is recommended to keep $R1 \geq 125 \text{ k}\Omega$. Higher value resistor R1 reduces ON-state quiescent current, increases turn-OFF delay, while reducing ON/OFF negative going threshold voltage V_{T-} .

Configuring Turn-ON slew rate

Switching a large capacitive load CL instantaneously results in a load inrush current given by the following equation:

$$I_{inrush} = C_{load} \times \frac{dv}{dt} = C_{load} \times \frac{V_{OUT_{final}} - V_{OUT_{initial}}}{V_{out} \text{ Slew Rate}} \quad (2)$$

An uncontrolled fast rising ON/OFF logic input may result in a high slew rate (dv/dt) at the output thus leading to a higher load inrush current. To control the inrush current connect a capacitor C1 as shown in the Figure 1. Use the following approximate empirical equation to configure the TPS27082L slew rate to a specific value.

$$t_{rise} = \frac{50 \times 10^3 \times C1}{VIN^{2/3}} \text{ sec} \quad (3)$$

Where t_{rise} is the time delta starting from the ON/OFF signal's rising edge to charge up the load capacitor CL from 10% to 90% of VIN voltage.

Table 1. Capacitor C1 Selection for Standard Output Rise Time

t_{rise} (μ Sec) (Typical)	C1 (F) R1 = 125 k Ω				
	VIN=7V	VIN=5V	VIN=3.3V	VIN=1.8V	VIN=1.2V
5	0	0	0	0	0
50	3.46n	2.77n	2.10n	1.41n	1.08n
100	6.91n	5.54n	4.21n	2.82n	2.16n
250	17.3n	13.8n	10.5n	7.05n	5.40n
470	32.5n	26.0n	19.8n	13.3n	10.1n
1000	69.1n	55.4n	42.1n	28.2n	21.6n

Note: The t_{rise} equation and the capacitor C1 values recommended in the table above are under typical conditions and are accurate to within $\pm 20\%$. Ensure $R1 > 125k\Omega$; and select a closest standard valued capacitor C1.

Configuring Turn-OFF delay

TPS27082L PMOS turn-OFF delay from the falling edge of ON/OFF logic signal depends upon the component values of resistor R1 and capacitor C1. Lower values of resistor R1 ensures quicker turn-OFF.

$$t_{off} > (R1 \times C1 \text{ sec}) \quad (4)$$

OFF Isolation Under VIN Transients

TPS27082L architecture helps isolate fast transients at the VIN when PFET is in the OFF state. Best transient isolation is achieved when an external capacitor C1 is not connected across VOUT and R1/C1 pins. When a capacitor C1 is present the VIN to VOUT coupling is capacitive and is set by the C1 to CL capacitance ratio. TPS27082L architecture prevents direct conduction through PFET.

Low Voltage ON/OFF Interface

To turn ON the load switch apply a voltage $> 1.0V$ at the ON/OFF pin. The TPS27082L features hysteresis at its ON/OFF input. The turn-ON and turn-OFF thresholds are dependent upon the value of resistor R1. Refer to the [ELECTRICAL CHARACTERISTICS](#) Table and [Figure 14](#) for details on the positive and negative going ON/OFF thresholds.

In applications where ON/OFF signal is not available connect ON/OFF pin to the VIN pin. The TPS27082L will turn ON and OFF in sync with the input supply connected to VIN.

On-chip Power Dissipation

Use below approximate equation to calculate TPS27082L's on-chip power dissipation P_D :

$$PD = I_{DQ1}^2 \times R_{Q1(ON)} \quad (5)$$

Where, I_{DQ1} is the DC current flowing through the transistor Q1. Refer to the [ELECTRICAL CHARACTERISTICS](#) Table and the [Figure 16](#) through [Figure 22](#) to estimate $R_{Q1(ON)}$ for various values of V_{GSQ1} .

Note: MOS switches can get extremely hot when operated in saturation region. As a general guideline, to avoid transistors Q1 going into saturation region set $V_{GS} > V_{DS} + 1.0V$. E.g. $V_{GS} > 1.5V$ and $V_{DS} < 200mV$ ensures switching region.

Thermal Reliability

For higher reliability it is recommended to limit TPS27082L IC's die junction temperature to less than $125^\circ C$. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate maximum on-chip power dissipation to restrict the die junction temperature target to safe limits:

$$PD_{(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}} \quad (6)$$

Where $T_{J(MAX)}$ is the target maximum junction temperature, T_A is the operating ambient temperature, and θ_{JA} is the package junction to ambient thermal resistance.

Improving Package Thermal Performance

The package θ_{JA} value under standard conditions on a High-K board is available in the Dissipation Rating Table. θ_{JA} value depends upon the PC board layout. An external heat sink and/or a cooling mechanism like a cold air fan can help reduce θ_{JA} and thus improving device thermal capability. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

APPLICATION EXAMPLES

TFT LCD Module Inrush Current Control

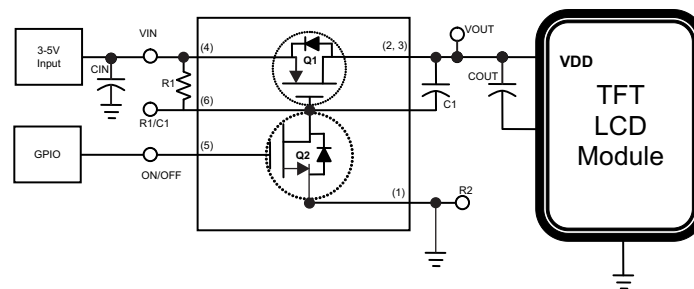


Figure 2. Inrush Current Control Using TPS27082L

LCD panels require inrush current control to prevent permanent system damages during turn-ON and turn-OFF events.

Standby Power Isolation

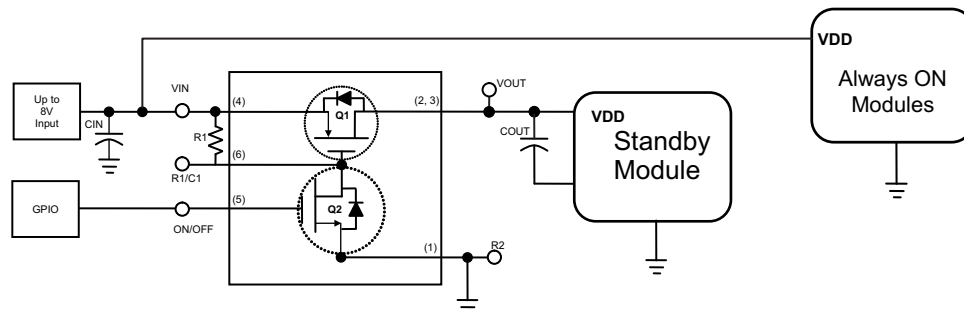


Figure 3. boost

Many applications have some always ON modules to support various core functions. However, some modules are selectively powered ON or OFF to save power and multiplexing of various on board resources. Such modules that are selectively turned ON or OFF require standby power generation. In such applications TPS27082L requires only a single pull-up resistor. In this configuration the VOUT voltage rise time is approximately 250ns when VIN = 5V.

Boost Regulator with True Shutdown

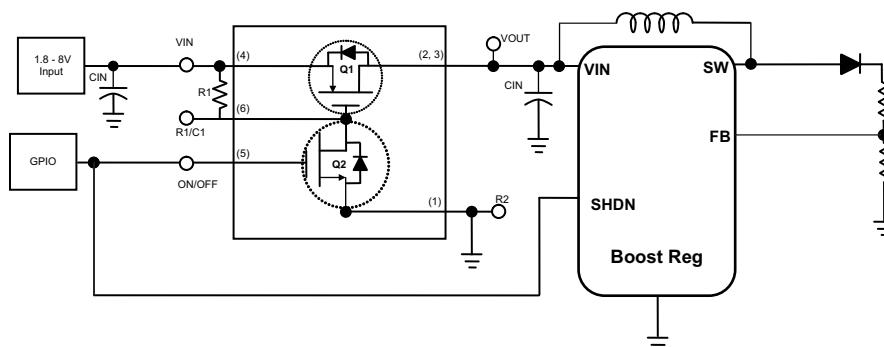


Figure 4. True Shutdown Using TPS27082L

The most common boost regulator topology provides a current leakage path through inductor and diode into the feedback resistor even when the regulator is shut down. Adding a TPS27082L in the input side power path prevents this leakage current and thus providing a true shutdown.

Single Module Multiple Power Supply Sequencing

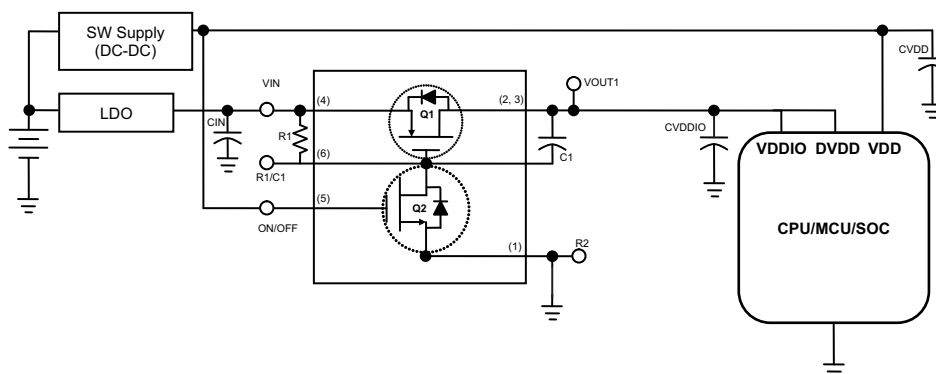


Figure 5. Power Sequencing Using TPS27082L, Example 1

Most modern SOC and CPUs require multiple voltage inputs for its Analog, Digital cores and IO interfaces. These ICs require that these supplies be applied simultaneously or in a certain sequence. TPS27082L when configured, as shown in Figure 5, with the VOUT1 rise time adjusted appropriately through resistor R2 and capacitor C1, will delay the early arriving LDO output to match up with late arriving DC-DC output and thus achieving power sequencing.

Multiple Modules Interdependent Power Supply Sequencing

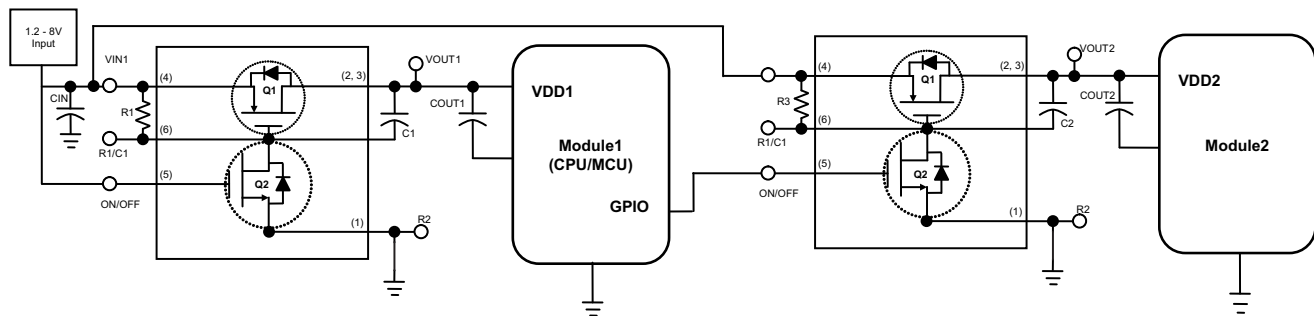


Figure 6. Power Sequencing Using TPS27082L, Example 2

For system integrity reasons a certain power sequencing may be required among various modules. As shown in [Figure 6](#), Module 2 will power up only after Module 1 is powered up and the Module 1 GPIO output is enabled to turn ON Module 2. TPS27082L when used as shown in [Figure 6](#) will not only sequence the Module 2 power, but also it will help prevent inrush current into the power path of Module 1 and 2.

Multiple Modules Interdependent Supply Sequencing without a GPIO Input

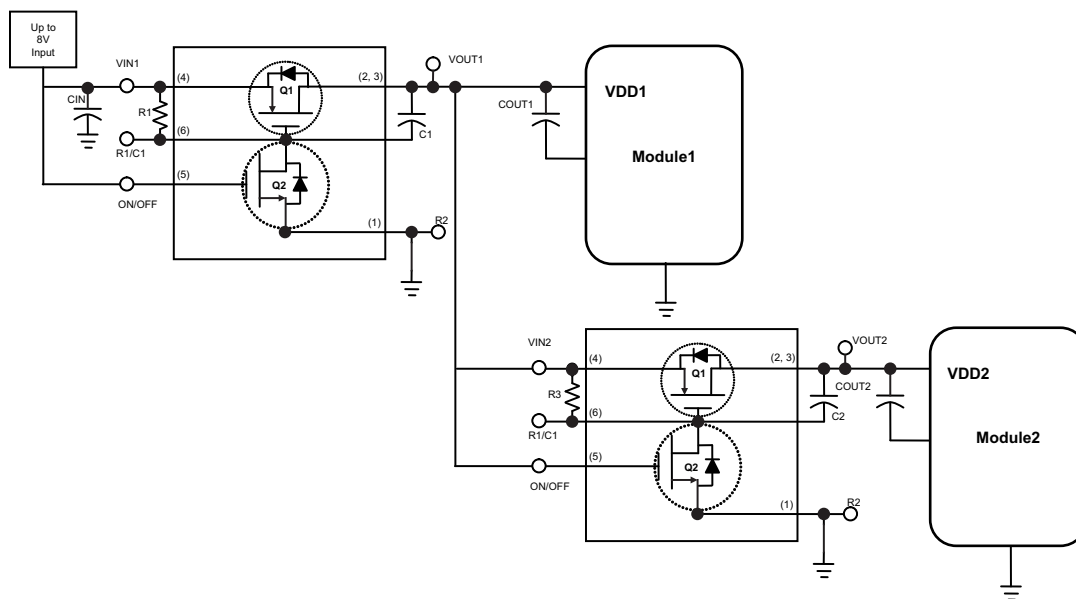


Figure 7. Power Sequencing using TPS27082L, Example 3

When a GPIO signal is not available connecting the ON/OFF pin of TPS27082 connected to Module 2 will power up Module 2 after Module 1, when resistor R4 and capacitor C1 are chosen appropriately. The two TPS27082L in this configuration will also control load inrush current.

PFET Q1 Minimum Safe Operating Area

(Refer to [DISSIPATION RATINGS](#)⁽¹⁾⁽²⁾⁽³⁾ for PC board details)

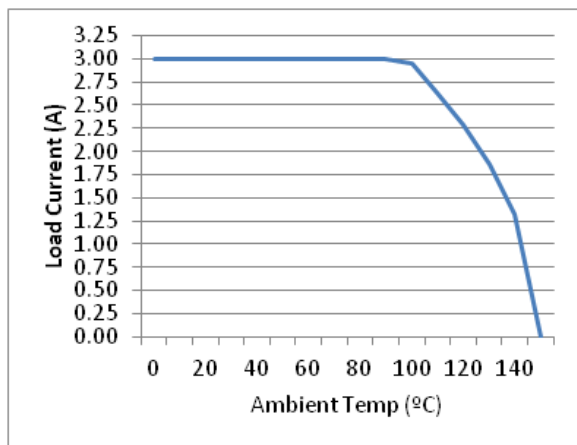


Figure 8. Q1 SOA at VGS_Q1=-4.5V

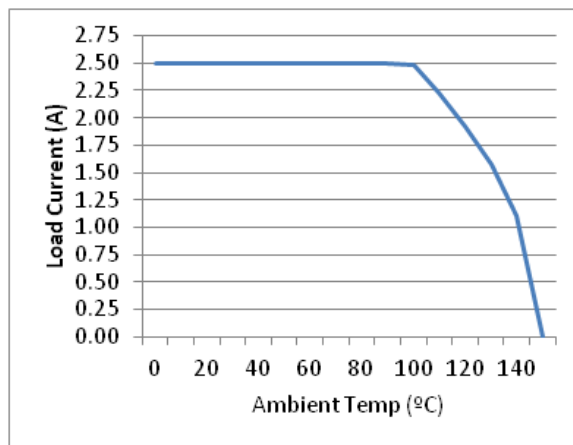


Figure 9. Q1 SOA at VGS_Q1=-3.0V

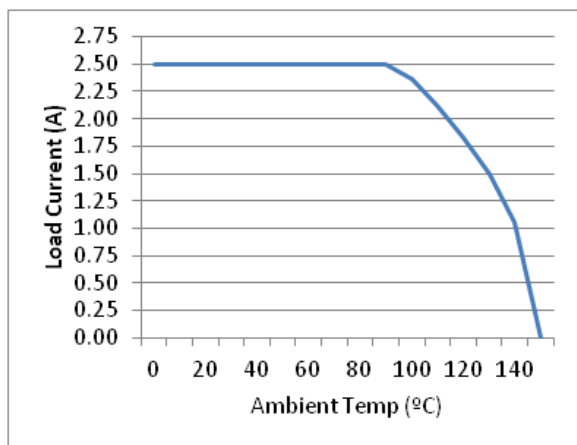


Figure 10. Q1 SOA at VGS_Q1=-2.5V

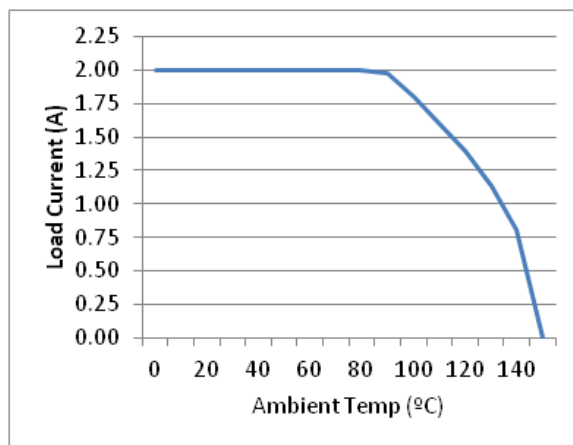


Figure 11. Q1 SOA at VGS_Q1=-1.8V

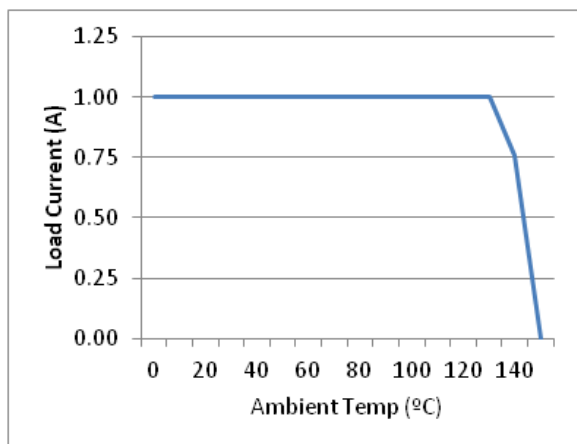


Figure 12. Q1 SOA at VGS_Q1=-1.5V

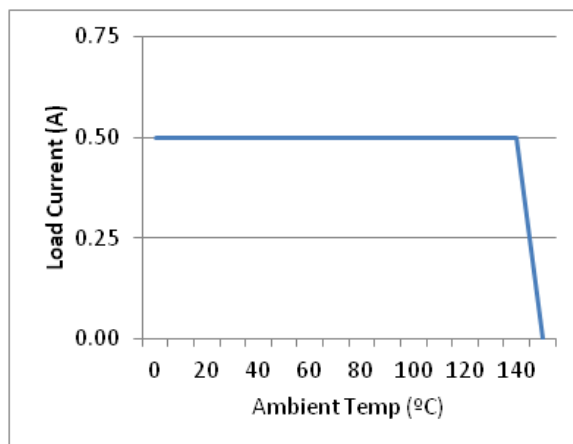


Figure 13. Q1 SOA at VGS_Q1=-1.2V

- (1) Maximum dissipation values for retaining a maximum allowable device junction temperature of 150°C
- (2) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance
- (3) Package thermal data based on a 76x114x1.6mm, 4-layer board with 2-oz Copper on outer layers

PFET Q1 Minimum Safe Operating Area (continued)

(Refer to [DISSIPATION RATINGS](#)⁽¹⁾⁽²⁾⁽³⁾ for PC board details)

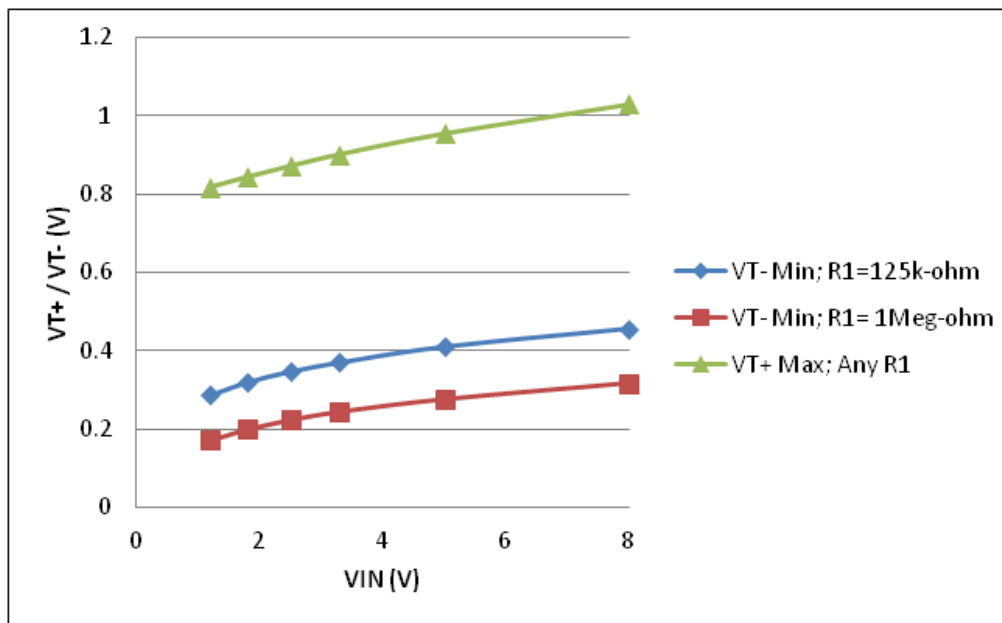


Figure 14. ON/OFF Positive and Negative Going Threshold Voltage

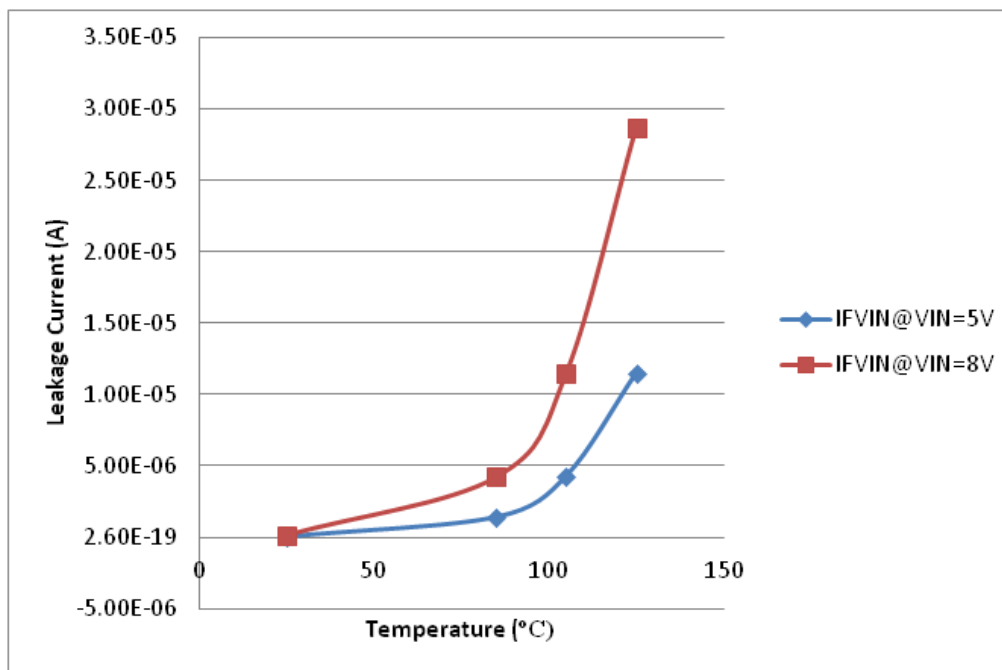


Figure 15. VIN Pin Leakage Current

Typical VIN to VOUT Voltage Drop Characteristic Plots

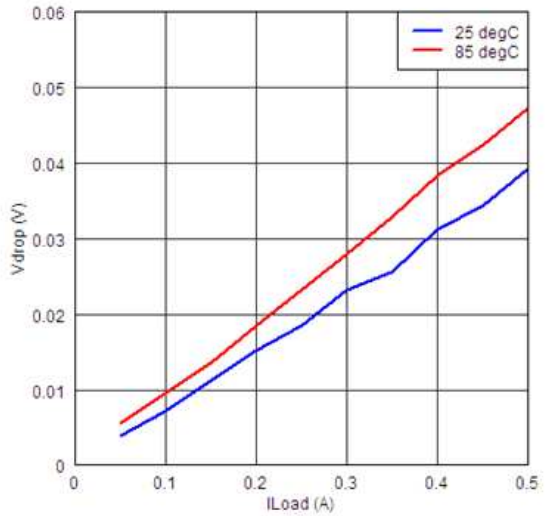


Figure 16. Vdrop vs IL; VGS_Q1 = -1.2V

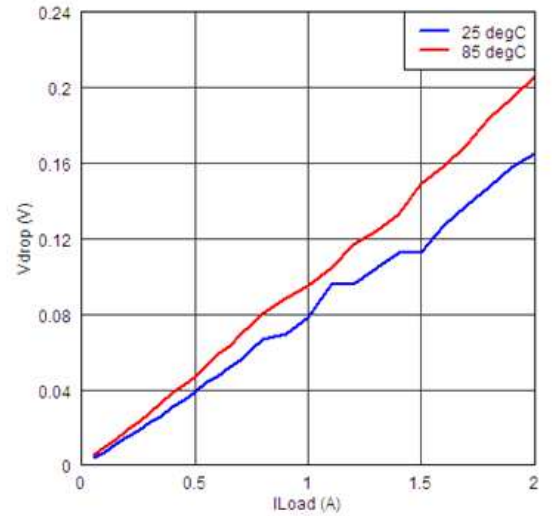


Figure 17. Vdrop vs IL; VGS_Q1 = -1.8V

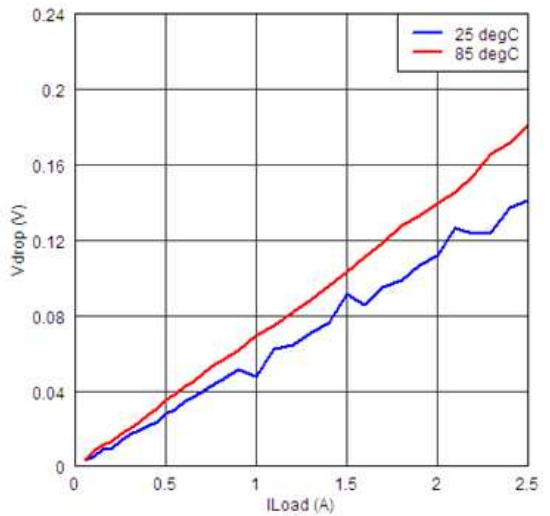


Figure 18. Vdrop vs IL; VGS_Q1 = -2.5V

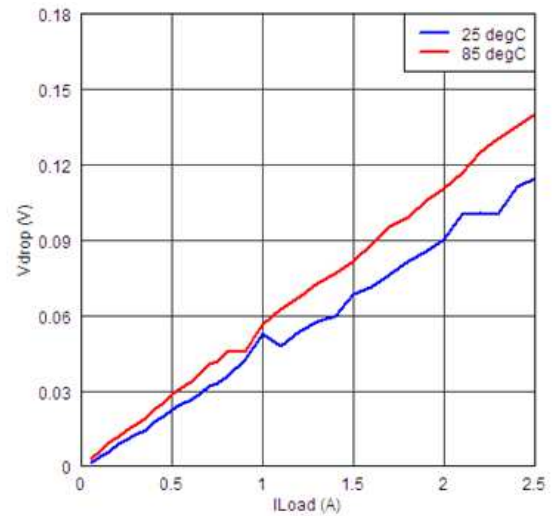


Figure 19. Vdrop vs IL; VGS_Q1 = -3.3V

Typical VIN to VOUT Voltage Drop Characteristic Plots (continued)

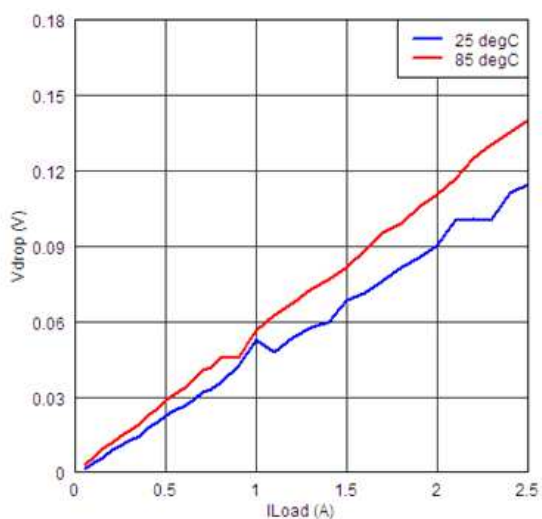


Figure 20. Vdrop vs IL; VGS_Q1 = -4.5V

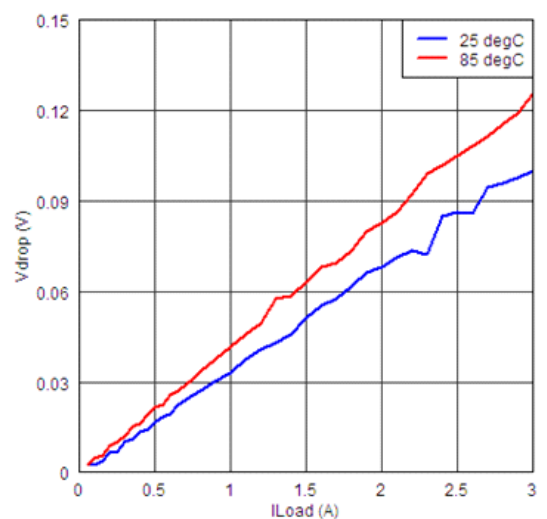


Figure 21. Vdrop vs IL; VGS_Q1 = -5.5V

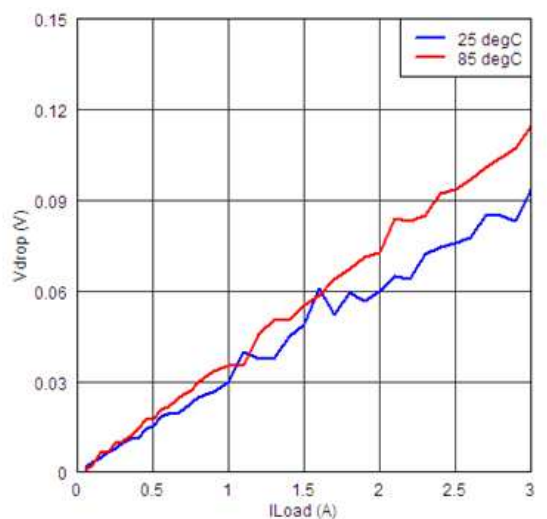


Figure 22. Vdrop vs IL; VGS_Q1 = -7V

REVISION HISTORY

Changes from Original (December 2012) to Revision A	Page
• 更新了文档中的措词。	1

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS27082LDDCR	NRND	Production	SOT-23- THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	BUA
TPS27082LDDCR.B	NRND	Production	SOT-23- THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	BUA

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS27082LDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS27082LDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0



SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



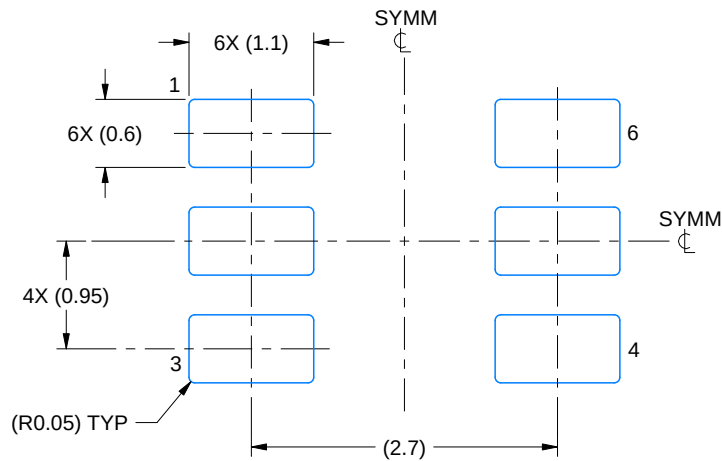
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

EXAMPLE BOARD LAYOUT

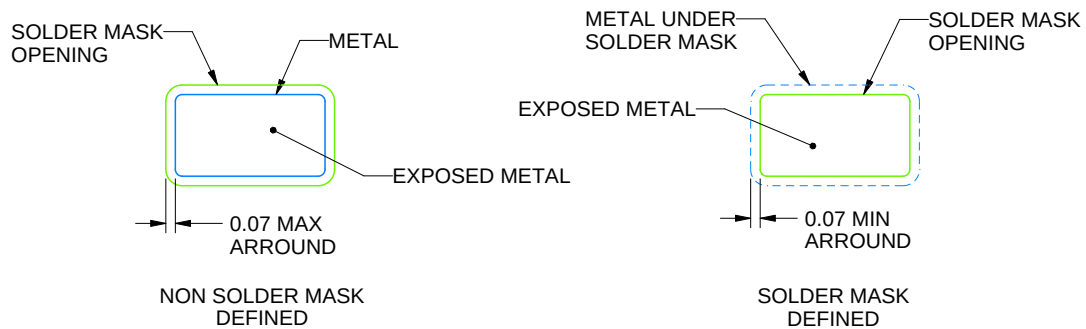
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X

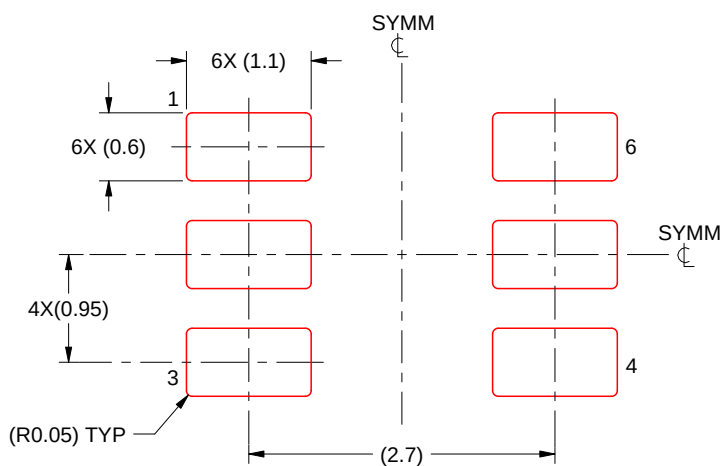


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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