具有电平位移&可调转换率控制的 1.2V-8V，3A 聚合物薄膜场效应晶体管 (PFET) 高侧负载开关

查询样品: TPS27081A

特性

- 低导通电阻，高电流 **PFET**
  - V_{GS} = –4.5V 时，$R_{导通}$ = 32mΩ
  - V_{GS} = –3.0V 时，$R_{导通}$ = 44mΩ
  - V_{GS} = –1.8V 时，$R_{导通}$ = 82mΩ
  - V_{GS} = –1.5V 时，$R_{导通}$ = 93mΩ
  - V_{GS} = –1.2V 时，$R_{导通}$ = 155mΩ
- 通过外部 **R1**，**R2** 和 **C1** 实现的可调打开和关闭转换率控制
- 支持 **1.2V** 到高达 **8V** 的宽范围电源输入
- 用于 **PFET** 控制的集成 **NMOS**
- **NMOS** 打开/关闭支持 **1.0V** 至高达 **8.0V** 的宽范围控制逻辑接口
- 完全静电放电 **(ESD)** 保护（所有引脚）
  - 人体模型 **(HBM) 2kV**，充电器件模型 **(CDM) 500V**
- 待机模式下的超低泄漏电流（典型值 **100nA**）
- 采用微型 **6** 引脚封装
  - **2.9mm x 2.8mm x 0.75mm** 薄型小外形尺寸晶体管 **(SOT)-23 (DDC)** 封装

应用范围

- 高侧负载开关
- 涌入电流控制
- 电源排序和控制
- 待机电源隔离
- 便携式电源开关

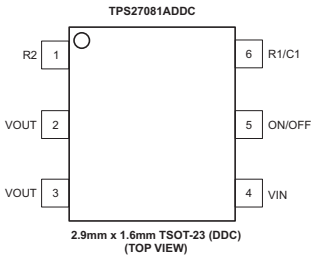


图 1. **TPS27081A** 封装

说明

TPS27081A 是一款高侧负载开关，此开关在微封装内集成了一个功率 PFET 和一个控制 NMOS。

TPS27081A 在所有引脚上特有业界标准 ESD 保护，从而提供与其它板载组件更好的 ESD 兼容性。

TPS27081A 可将开/关逻辑信号的电平转换为 VIN 电平，并且支持低至 1.0V 的 CPU 或 MCU 逻辑以在不需要外部电平位移器的前提下控制更高电压的电源。

通过一个快速开/关逻辑信号来开启大值输出电容器有可能导致过多的涌入电流。 为了控制负载涌入电流，如图 2所示，连接一个电阻器 R2。 可增加一个外部电容器 C1 来进一步限制涌入电流。 要配置 TPS27081A 以获得一个特定的转换率，请参考应用信息一节。

无需对涌入电流进行控制的待机电源开关应用需要一个单一上拉电阻器 R1。 在此类应用中，将 TPS27081A 引脚 R2 连接至系统接地。

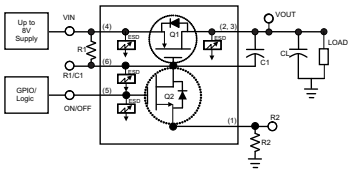


图 2. 简化方框图&应用图

组件表（典型应用）

组件	说明
R1	电平位移器/上拉电阻器
R2	可选(1)
C1	可选(1)

(1) 负载涌入电流（转换率）控制需要此选项

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PART NUMBER	PACKAGE		TOP-SIDE MARKING (2)
–40°C to 85°C	TPS27081ADDCR	6-Pin Thin SOT	Reel of 3000	AU_

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) DDC: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Specified at T_J = –40°C to 105°C unless otherwise noted.

			VALUE		UNIT
			MIN	MAX	
V_{INmax}, V_{OUTmax}	V_{IN}, V_{OUT} pin Maximum Voltage with reference to pin R2		–0.1	8	V
$V_{ON/OFF}$	ON/OFF Pin max Voltage with respect to Pin R2		–0.3	8	V
I_{Q1-ON}	Max Continuous Drain Current of Q1 at T_J = 105°C			3	A
	Max Pulsed Drain Current of Q1 (3) at T_J = 105°C			9.5	
P_D	Max power dissipation at T_A = 25°C, T_J = 150°C	6 Pin - TSOT, θ_{JA} = 105°C/W		1190	mW
All pins	ESD Rating – HBM			2000	V
	ESD Rating – CDM			500	
T_A	Operating free-air ambient temperature range		–40	85(4)	°C
T_{J-max}(5)	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance
(3) Pulse Width <300us, Duty Cycle <2%
(4) TJ-max limits and other related conditions apply. Refer to SOA charts, Figure 17 through Figure 21
(5) Operating at the absolute T_{J-max} of 150°C can affect reliability – for higher reliability it is recommended to ensure T_J <105°C

DISSIPATION RATINGS(1)(2)(3)

BOARD	PACKAGE	θ_{JC}	θ_{JA}(4)	T_A < 25°C	T_A = 70°C	T_A = 85°C	DERATING FACTOR ABOVE T_A = 25ºC
High-K(JEDEC 51-7)	6-Pin Thin SOT (DDC)	43°C/W	105°C/W	1190 mW	760 mW	619 mW	9.55 mW/°C

(1) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance.
(2) Maximum dissipation values for retaining a maximum allowable device junction temperature of 150°C
(3) Package thermal data based on a 76x114x1.6mm, 4-layer board with 2-oz Copper on outer layers
(4) Operating at the absolute TJ-max of 150°C can affect reliability; TJ ≤ 105°C is recommended

ELECTRICAL CHARACTERISTICS

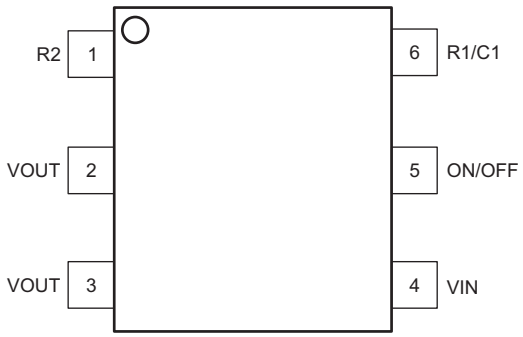
Specified over the recommended junction temperature range TJ = -40°C to 105°C unless otherwise noted. Typical values specified at TA = TJ = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
BV_{IN}	Q1 drain-to-source breakdown voltage	$V_{ON/OFF}$ = 0 V, VGS(Q1) = 0V, ID(Q1) = 250 µA		-8			V
I_{LOAD} (1)	VIN Pin total leakage current	V_{IN}= 8V, $V_{ON/OFF}$ = 0V, R1 = 10k Ω	T_J = 25°C		0.15	0.75	µA
			T_J = 85°C (2)		5	20	
I_{LOAD} (1)	VIN Pin total leakage current	V_{IN}= 5V, $V_{ON/OFF}$ = 0V, R1 = 10k Ω	T_J = 25°C		0.05		µA
			T_J = 85°C (2)		2		
IF_{Q2}	Q2 drain-to-source leakage current	V_{IN}= 8V, $V_{ON/OFF}$ = 0V	T_J = 25°C		0.030	0.050	uA
			T_J = 85°C (2)		0.350	0.600	
IF_{Q2}	Q2 drain-to-source leakage current	V_{IN}= 5V, $V_{ON/OFF}$ = 0V	T_J = 25°C		0.025		µA
			T_J = 85°C (2)		0.250		
ON CHARACTERISTICS (3)							
VIL	ON/OFF pin low-level input voltage	V_{IN} = 5.0V, ID(Q1) < 2µA, R1 = 10kΩ, R2 = RL = 0Ω	T_J = 25°C			0.3	V
		V_{IN} = 5.0V, ID(Q1) < 20µA, R1 = 10kΩ, R2 = RL = 0Ω	T_J = 85°C (2)			0.2	
VIH	ON/OFF pin high-level input voltage	VIN=5.0V, R1=10kΩ		1.0			V
$R_{Q1(ON)}$	Q1 Channel ON resistance (4)	VGS = -4.5 V, ID(Q1) = 3.0 A			32	55	mΩ
		VGS = -3.0 V, ID(Q1) = 2.5 A			44	77	
		VGS = -2.5 V, ID(Q1) = 2.5 A			50	85	
		VGS = -1.8 V, ID(Q1) = 2.0 A			82	147	
		VGS = -1.5 V, ID(Q1) = 1.0 A			93	166	
		VGS = -1.2 V, ID(Q1) = 0.5 A			155	260	
$R_{Q2(ON)}$	Q2 Channel ON resistance	VGS = 4.5 V, ID(Q2) = 0.4 A			1.8	3	Ω
		VGS = 3.0 V, ID(Q2) = 0.3 A			2.3	6.2	
		VGS = 2.5 V, ID(Q2) = 0.2 A			2.6	6.1	
		VGS = 1.8 V, ID(Q2) = 0.1 A			3.8	10	
		VGS = 1.5 V, ID(Q2) = 0.05 A			4.4	8.5	
		VGS = 1.2 V, ID(Q2) = 0.03 A			6.25	13.5	
Q1 DRAIN-SOURCE DIODE PARAMETERS (3)(5)							
IF_{SD}	Source-drain diode peak forward current	VF_{SD} = 0.8 V, $V_{ON/OFF}$ = 0 V			1.0		A
VF_{SD}	Source-drain diode forward voltage	$V_{ON/OFF}$ = 0 V, IF_{SD} = –0.6A,				1.0	V

(1) Pull-up Resistor R1 dependent
(2) Guaranteed by design only
(3) Pulse width <300 µs, Duty Cycle <2.0%
(4) Refer to SOA charts for current rating
(5) Not rated for continuous current operation

DEVICE INFORMATION

TPS27081ADDC



2.9mm x 1.6mm TSOT-23 (DDC)
(TOP VIEW)

TPS27081A PIN DESCRIPTION

PIN		DESCRIPTION
NAME	NUMBER	
R2	1	Source Terminal of NMOS (Q2) - Connect to system GND directly or through a slew rate control resistor
VOUT	2, 3	Drain Terminal of Power PFET (Q1) - Connect a slew control capacitor between pins VOUT and R1/C1
VIN	4	Source Terminal of Power PFET (Q1) - connect a pull-up resistor between the pins VIN/R1 and R1/C1
ON/OFF	5	Active high enable pin – when driven with a high impedance driver connect an external pull down resistor to GND
R1/C1	6	Gate Terminal of Power PFET (Q1)

APPLICATION INFORMATION

The TPS27081A IC is a high side load switch that integrates a Power PFET and a Control NMOS in a tiny package. The TPS27081A internal components are rated for up to 8V supply and support up to 3A of load current. The TPS27081A can be used in a variety applications. Figure 3 below shows a general application of TPS27081A to control the load inrush current.

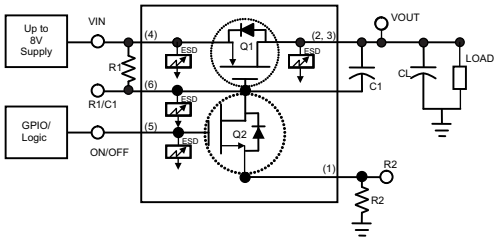


Figure 3. Typical Application Diagram

Configuring Q1 ON Resistance

The V_{GS-Q1} Gate-Source voltage across the PMOS transistor Q1 sets its ON resistance $R_{Q1(ON)}$. Directly connecting the pin R2 to ground maximizes the ON state V_{GS-Q1} and thus minimizes the VIN to VOUT voltage dropout. When a resistor R2 is installed to control the Turn-ON slew rate then V_{GS-Q1} is given by:

$$VGS_{Q1} = -VIN \times \frac{R1}{R1 + R2} V \quad (1)$$

e.g. R1 = 10 x R2, VIN = 5V sets V_{GS-Q1} = –4.5V

Note: It is recommended to keep R1 > 10 x R2. Higher value of resistor R1 minimizes quiescient current when is PMOS is on, however may adversely impact off state leakage current. Refer to the ILoad parameter in the ELECTRICAL CHARACTERISTICS.

Configuring Turn-ON Slew Rate

Switching a large capacitive load CL instantaneously results in a load inrush current given by the following equation:

$$I_{inrush} = C_{load} \times \frac{dv}{dt} = C_{load} \times \frac{VOUT_{final} - VOUT_{initial}}{\text{Vout Slew Rate}} \quad (2)$$

An uncontrolled fast rising ON/OFF logic input may result in a high slew rate at the output resulting in a very high dv/dt thus leading to a higher inrush current. To control the inrush current connect a resistor R2 and a capacitor C1 as shown in the Electrical Characteristics Table. Use the following equation to configure the TPS27081A slew rate to a specific value. Refer to Table 1 for component values to configure TPS27081A to achieve standard slew rates.

$$t_{rise} = \frac{3.9 \times R2 \times C1}{VIN^{2/3}} sec \quad (3)$$

Where t_{rise} is the time delta starting from the ON/OFF signal's rising edge to charge up the load capacitor CL from 10% to 90% of VIN voltage.

Note: The t_{rise} equation is accurate to within +/-20% across full VIN range supported by TPS27081A. Ensure that R1 > 10 x R2.

Table 1. Component Values for VOUT Rise Time

C1[1]	Rise Time (µs)[2][3]							
	R1=10kΩ, R2=1kΩ				R1=5.1kΩ, R2=510Ω			
	VIN = 7V	VIN = 5V	VIN = 3.3V	VIN = 1.2V	VIN = 7V	VIN = 5V	VIN = 3.3V	VIN = 1.2V
220pF	.253	.316	.416	.810	.129	.161	.212	.413
1000pF	1.15	1.44	1.89	3.68	.586	.732	.963	1.88
4700pF	5.4	6.75	8.88	17.3	2.76	3.44	4.53	8.83
0.18uF	207	258	340	663	106	132	173	338
0.27uF	310	388	510	994	158	198	260	507
0.33uF	379	474	623	1220	194	242	318	620
1uF	1150	1440	1890	3680	586	732	963	1880

(1) Typical ceramic capacitor values
(2) CLoad=10uF. Output rise time is independent of CLoad when CLoad >> C1
(3) Rise Time is 250ns for R2=0Ω and C1=CLoad=0F

Configuring Turn-OFF Delay

TPS27081A PMOS turn-off delay from the falling edge of ON/OFF logic signal depends upon the component values of resistor R1 & capacitor C1. Lower values of resistor R1 ensures quicker turn-off.

$t_{off} > 2 \times R1 \times C1$ sec

Low Voltage ON/OFF Interface

The VGS_{Q2} is set by the ON/OFF logic level. To turn ON, the transistor Q2 requires a VGS > 1.0V (Typical). For reliable operation apply ON/OFF logic that has the following VIH and VIL limits:

$VIH_{ON} > 1.0V + I_{Q2} \times R2$ V

$VIL_{OFF} < 0.2$ V

Minimizing I_{Q2} x R2 drop helps achieve a direct interface with a low voltage ON/OFF logic. To minimize I_{Q2} x R2 voltage drop select a high R1/R2 ratio. E.g. When VIN= 1.8V, selecting R1/R2 = 40 will require V_{IH} > 1.0 + 45mV and thus allowing a 1.2V GPIO interface.

In applications where ON/OFF signal is not available connect ON/OFF pin to VIN. The TPS27081A will turn ON/OFF in sync with the input supply connected to VIN.

Note: Connect a pull down resistor between ON/OFF pin to GND when ON/OFF is driven by a high-impedance (tri-state) driver.

On-Chip Power Dissipation

Use the below equation to calculate TPS27081A on-chip power dissipation P_D:

$PD = ID_{Q1}^2 \times R_{Q1(ON)} + ID_{Q2}^2 \times R_{Q2(ON)}$

Where, ID_{Q1} and ID_{Q2} are the DC current flowing through the transistors Q1 and Q2 respectively. Refer to the ELECTRICAL CHARACTERISTICS table and/or Figure 10 through Figure 16 to estimate $R_{Q1(ON)}$ and $R_{Q2(ON)}$ for various values of VGS_{Q1} and VGS_{Q2} respectively.

Note: MOS switches can get extremely hot when operated in saturation region. As a general guideline, to avoid transistors Q1 and Q2 going into saturation region set VGS > VT +VDS. E.g. VGS > 1.5V and VDS < 200mV ensures operation as a switch.

Thermal Reliability

For higher reliability it is recommended to limit TPS27081A IC's die junction temperature to less than 105°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate maximum on-chip power dissipation to achieve the maximum die junction temperature target:

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) \Big/ \theta_{JA}$$

Where:

$T_{J(MAX)}$ is the target maximum junction temperature.

T_A is the operating ambient temperature.

$R_{\theta JA}$ is the package junction to ambient thermal resistance. (4)

Improving Package Thermal Performance

The package θ_{JA} value under standard conditions on a High-K board is listed in the DISSIPATION RATINGS. θ_{JA} value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce θ_{JA} and thus improve device thermal capabilities. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

APPLICATION EXAMPLES

TFT LCD Module Inrush Current Control

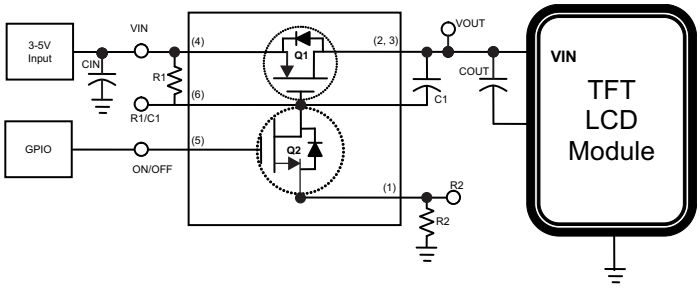


Figure 4. Inrush Current Control Using TPS27081A

LCD panels require inrush current control to prevent permanent system damages during turn-ON and turn-OFF events.

Standby Power Isolation

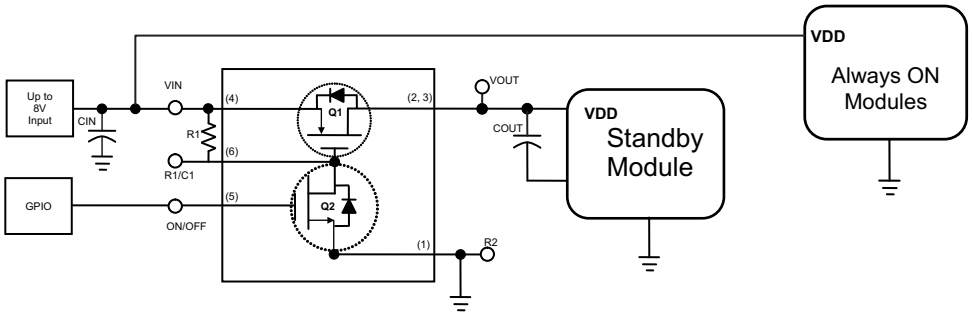


Figure 5. Standby Power Generation Using TPS27081A

Many applications have some always ON modules to support various core functions. However, some modules are selectively powered ON or OFF to save power and multiplexing of various on board resources. Such modules that are selectively turned ON or OFF require standby power generation. In such applications TPS27081A requires only a single pull-up resistor. In this configuration the VOUT voltage rise time is approximately 250ns when VIN = 5V.

Boost Regulator with True Shutdown

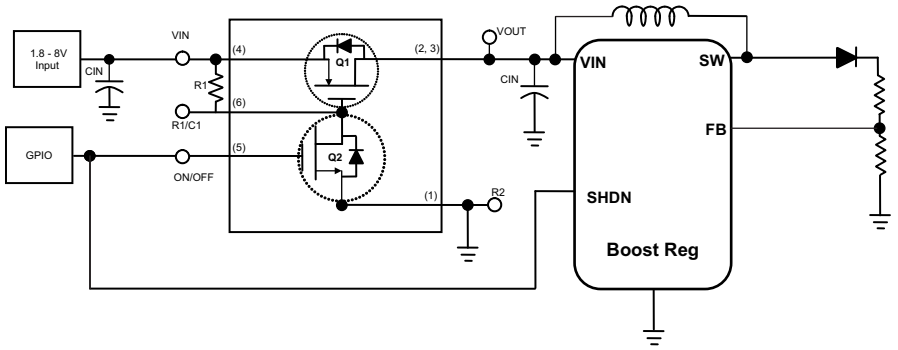


Figure 6. True Shutdown Using TPS27081A

The most common boost regulator topology provides a current leakage path through inductor and diode into the feedback resistor even when the regulator is shut down. Adding a TPS27081A in the input side power path prevents this leakage current and thus providing a true shutdown.

Single Module Multiple Power Supply Sequencing

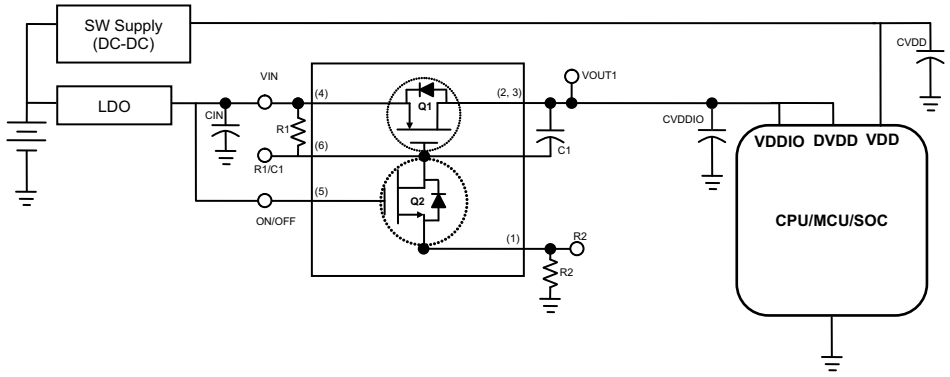


Figure 7. Power Sequencing Using TPS27081A, Example 1

Most modern SOCs and CPUs require multiple voltage inputs for its Analog, Digital cores and IO interfaces. These ICs require that these supplies be applied simultaneously or in a certain sequence. TPS27081A when configured, as shown in Figure 7, with the VOUT1 rise time adjusted appropriately through resistor R2 and capacitor C1, will delay the early arriving LDO output to match up with late arriving DC-DC output and thus achieving power sequencing.

Multiple Modules Interdependent Power Supply Sequencing

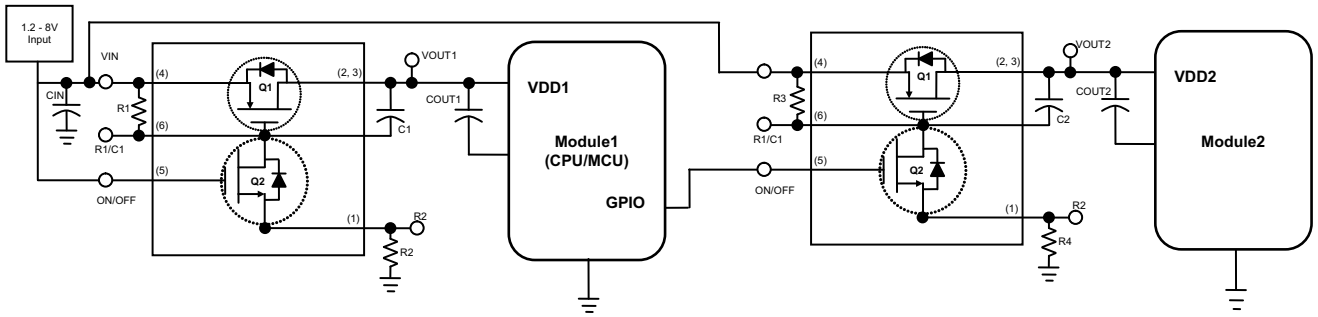


Figure 8. Power Sequencing Using TPS27081A, Example 2

For system integrity reasons a certain power sequencing may be required among various modules. As shown in Figure 8, Module 2 will power up only after Module 1 is powered up and the Module 1 GPIO output is enabled to turn ON Module 2. TPS27081A when used as shown in Figure 8 will not only sequence the Module 2 power, but also it will help prevent inrush current into the power path of Module 1 and 2.

Multiple Modules Interdependent Supply Sequencing without a GPIO Input

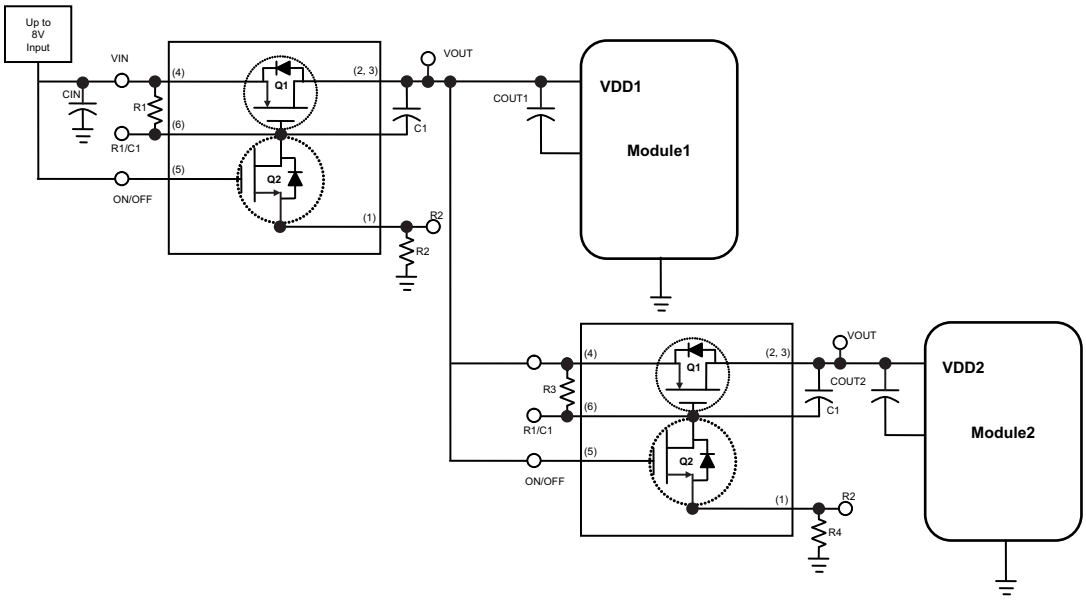
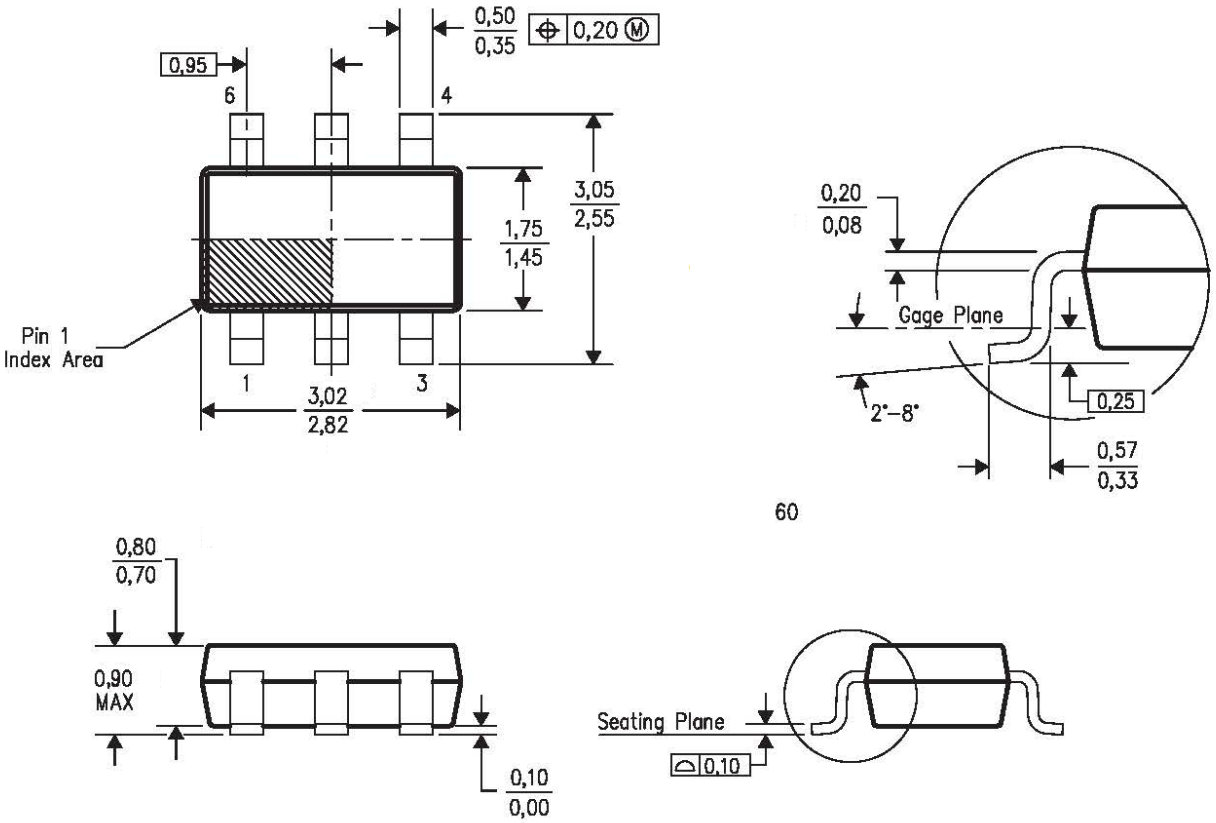


Figure 9. Power Sequencing using TPS27081A, Example 3

When a GPIO signal is not available connecting the ON/OFF pin of TPS27081 connected to Module 2 will power up Module 2 after Module 1, when resistor R4 and capacitor C1 are chosen appropriately. The two TPS27081A in this configuration will also control load inrush current.

TPS27081A THIN SOT$_{(DDC)}$ SPECIFIC PACKAGE DIMENSIONS



NOTES:

- All linear dimensions are in millimeters.
- Body dimensions do not include mold flash or protrusion.
- Falls within JEDEC MO-193 variation AA (6 pin).

TYPICAL CHARACTERISTICS

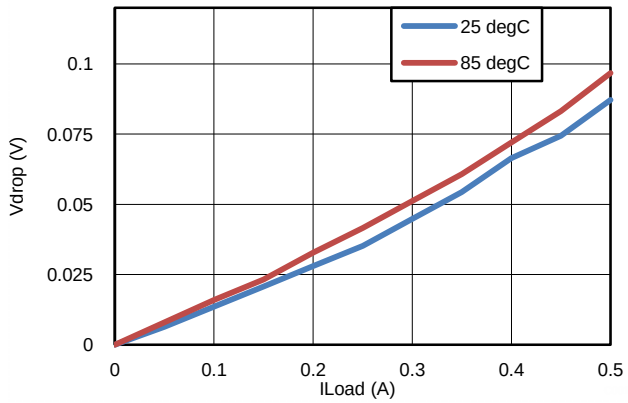


Figure 10. Vdrop vs IL; VGS_{Q1}=-1.2V

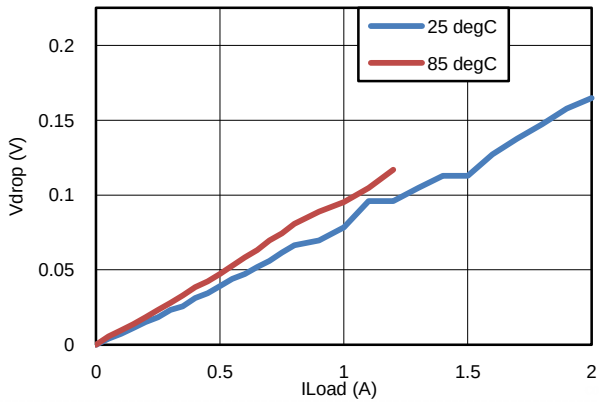


Figure 11. Vdrop vs IL; VGS_{Q1}=-1.8V

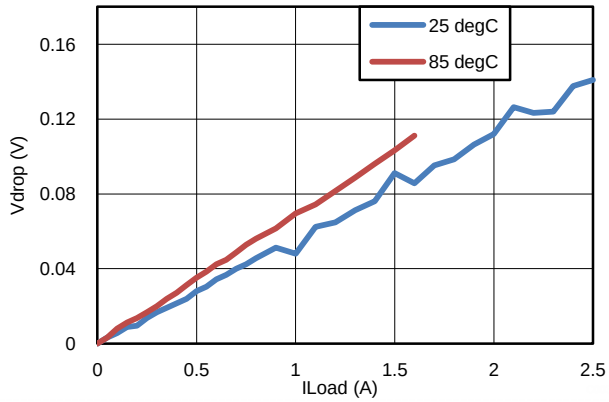


Figure 12. Vdrop vs IL; VGS_{Q1}=-2.5V

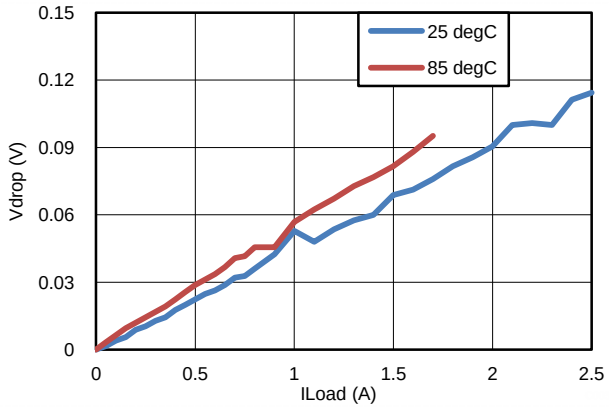


Figure 13. Vdrop vs IL; VGS_{Q1}=-3.3V

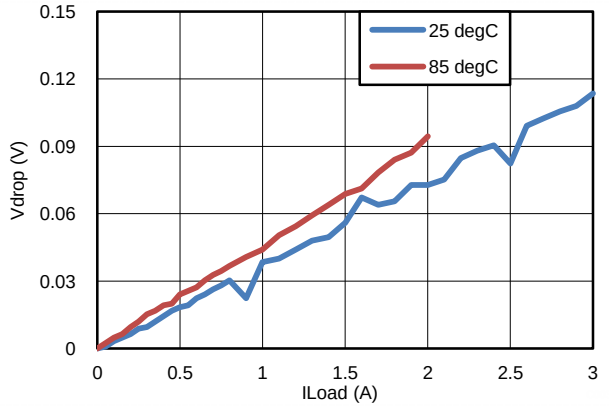


Figure 14. Vdrop vs IL; VGS_{Q1}=-4.5V

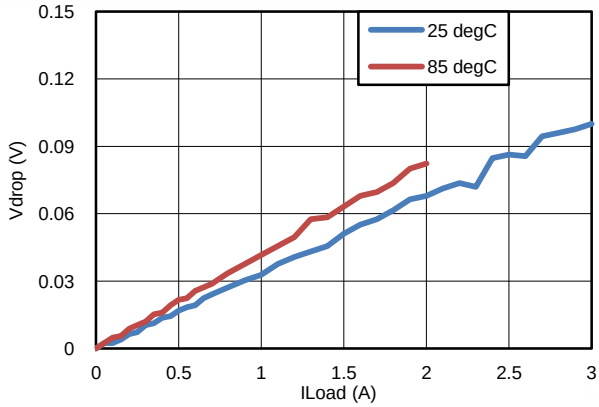


Figure 15. Vdrop vs IL; VGS_{Q1}=-5.5V

TYPICAL CHARACTERISTICS (continued)

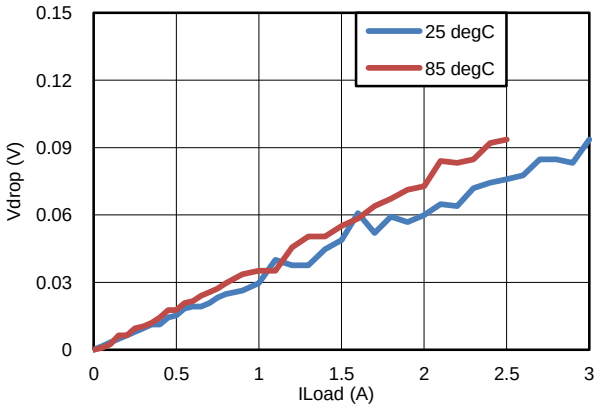


Figure 16. Vdrop vs IL; VGS_{Q1}=-7V

PFET Q1 Minimum Safe Operating Area (SOA)

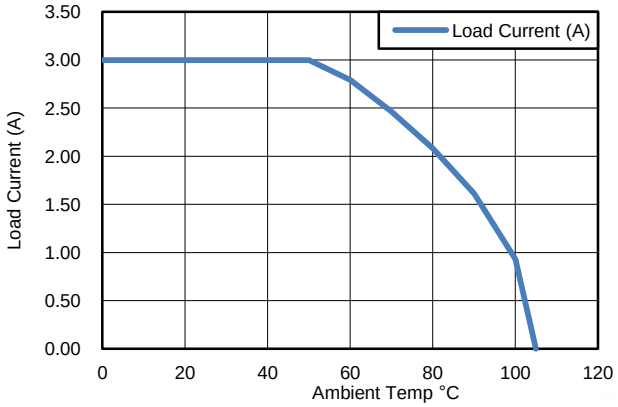


Figure 17. Q1 SOA @ VGS_Q1 = -4.5V

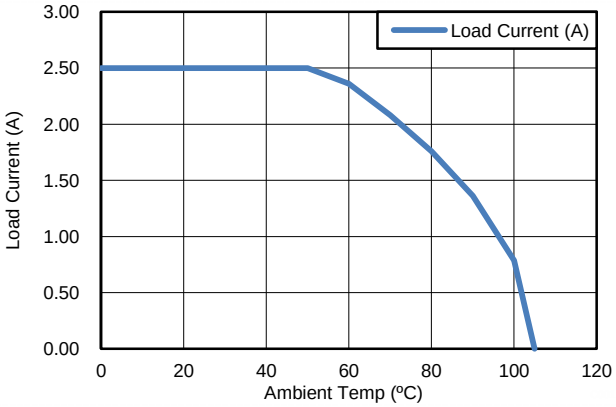


Figure 18. Q1 SOA @ VGS_Q1 = -3.0V

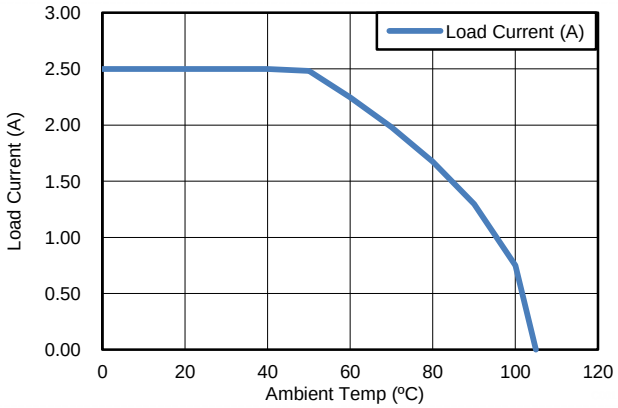


Figure 19. Q1 SOA @ VGS_Q1 = -2.5V

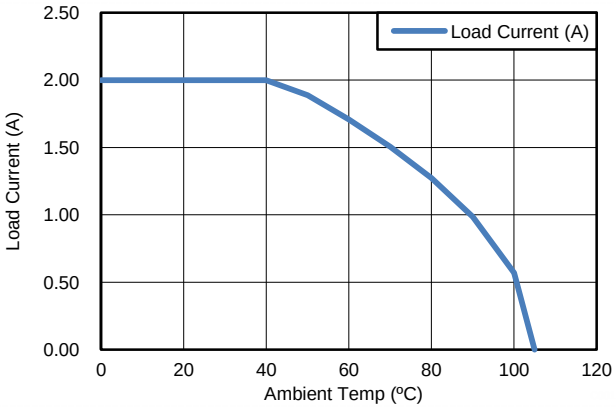


Figure 20. Q1 SOA @ VGS_Q1 = -1.8V

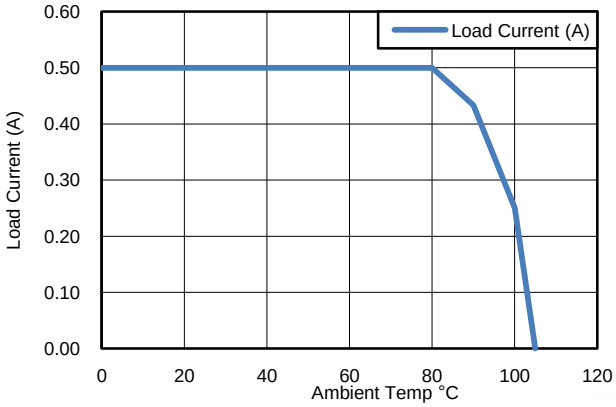


Figure 21. Q1 SOA @ VGS_Q1 = -1.2V

REVISION HISTORY

Changes from Revision B (September 2012) to Revision C **Page**

- 从数据表中删除了 DRV 封装预览。 1

Changes from Revision C (January 2013) to Revision D **Page**

- 更新了文档中的措词。 1

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS27081ADDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	AUA
TPS27081ADDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	AUA
TPS27081ADDCR.B	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	AUA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

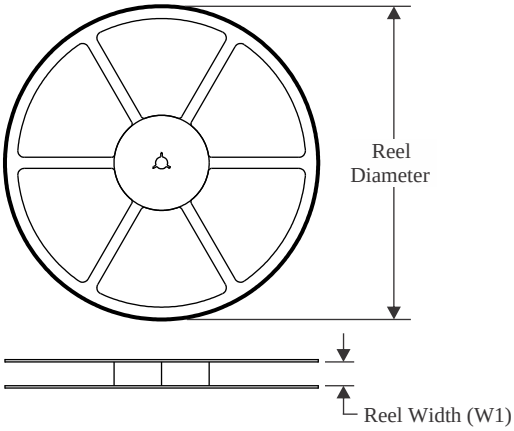
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

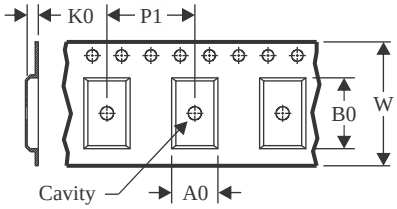
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

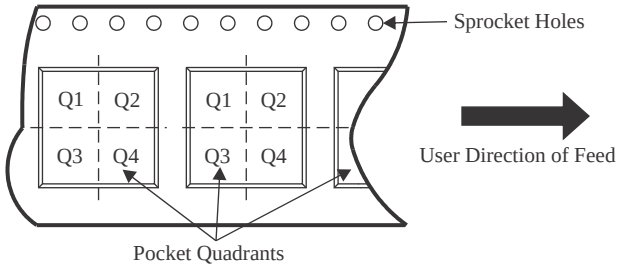


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

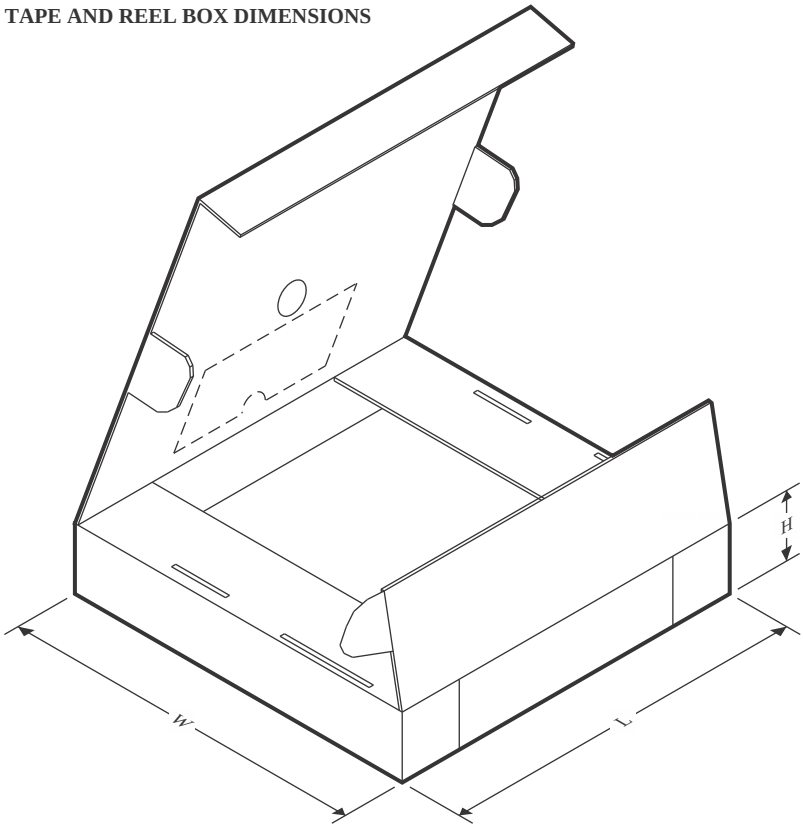
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS27081ADDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

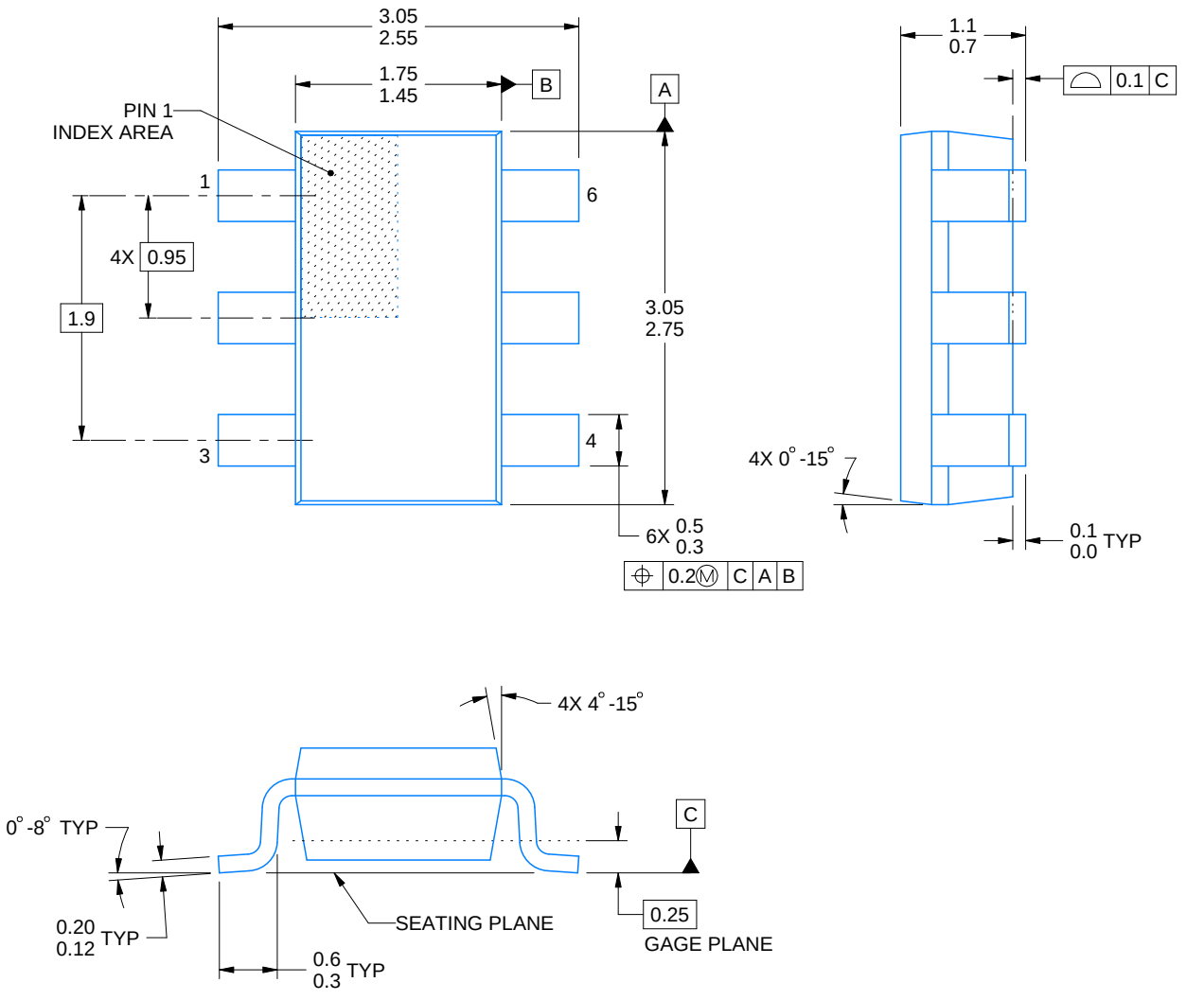
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS27081ADDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

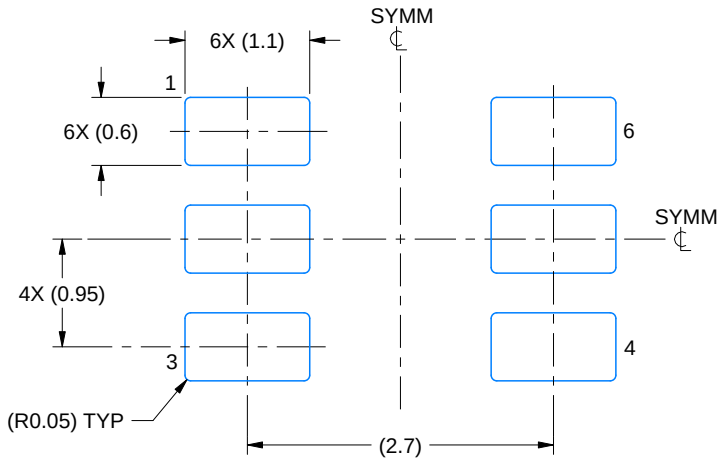
SMALL OUTLINE TRANSISTOR



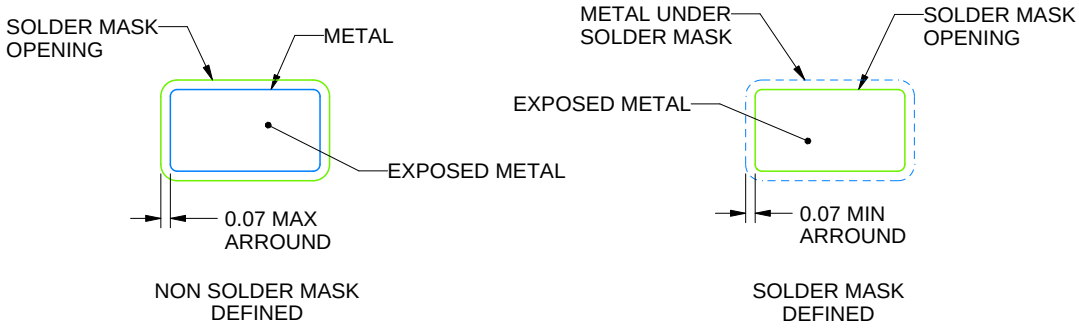
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

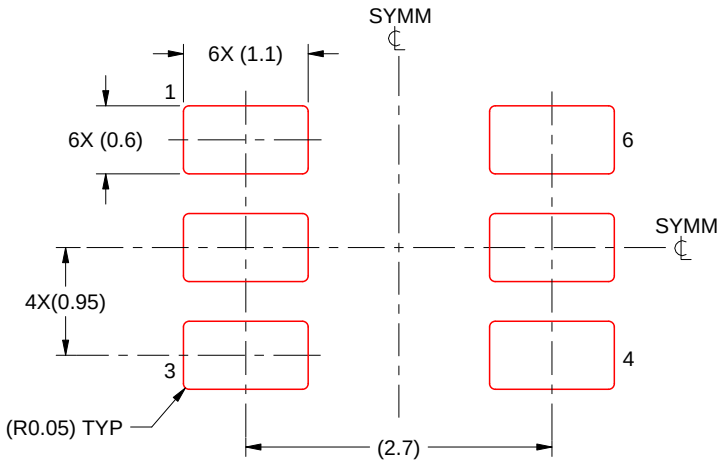


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265