# 具有过压保护和阻断场效应晶体管 (FET) 控制的 5V/12V 电子熔丝 (eFuse)

查询样品: **TPS2592Ax**, **TPS2592Bx**

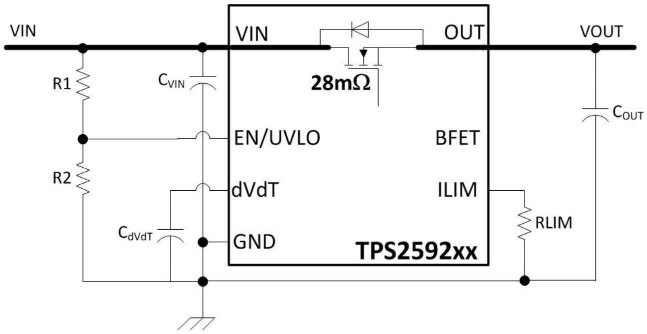
## 特性

- **12V** 保护 **- TPS2592Ax**
- **5V** 保护 **– TPS2592Bx**
- 集成的 **28mΩ** 导通金属氧化物半导体场效应晶体管 **(MOSFET)**
- **20V** 的绝对最大电压
- 可编程电流限值（准确度 **±15%**）
- 阻断 **FET** 驱动器
- 固定过压设置
- 可编程 **OUT**（输出）转换率，欠压闭锁 **(UVLO)**
- 内置热关断
- **UL** 认证正在处理中
- 单点故障测试期间安全 **(UL60950)**
- 小型封装 **- 10L (3mm x 3mm)** 超薄小外形尺寸无引线封装 **(VSON)**

## 应用范围

- 硬盘 **(HDD)** 和固态硬盘 **(SSD)**
- 机顶盒
- 服务器**/**辅助 **(AUX)** 电源
- 风扇控制
- **PCI/PCIe** 卡
- 交换机**/**路由器

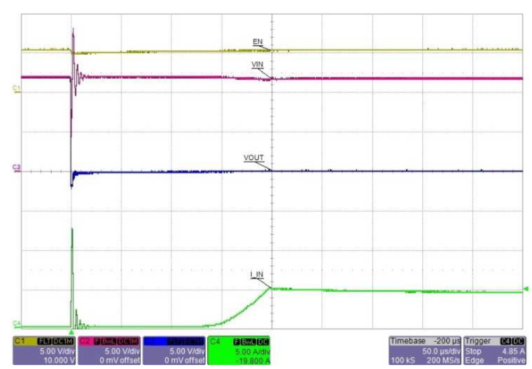
应用电路原理图




## 说明

TPS2592xx 系列 eFuse 是采用微型封装的高度集成电路保护和电源管理解决方案。 借助于极少的外部组件和多重保护模式，它们可在过载、短路、电压浪涌、过多涌入电流和反向电流情况发生时为器件提供稳健耐用的保护。 设定电流限值电平只需一个外部电阻器，此电阻器具有 ±15% 的典型准确度。 过压事件由内部钳位电路限制在一个安全的固定最大值，而无需外部组件。 TPS2592Ax 器件为 12V 系统提供过压保护 (OVP)，而 TPS2592Bx 器件为 5V 系统提供过压保护。 在有特定的电压斜升要求的情况下，提供了一个可由一个单个电容器进行编程的 dV/dT 引脚，以确保适当的输出斜升速率。 诸如 SSD 的很多系统，绝对不允许累积电容能量经 FET 体二极管转储回一个电压下降或短接总线。 BFET 引脚就是用于这样系统的引脚。 一个外部 NFET 可与 TPS2592xx 输出和 BFET 驱动的栅极“背靠背”连接。 当 TPS2592xx 被禁用时，此时，两个方向上的电流均被停止。 TPS2592xL 部件将在一个故障后锁存关闭，而 TPS2592xA 部件将尝试在热关闭复位后重新启动。

瞬态：输出短路




产品信息

| 部件号 | 欠压闭锁 (UVLO) | 过压钳位（典型值） | 故障响应 | 状态 |
|---|---|---|---|---|
| TPS2592AA | 4.3V | 15.0V | 自动重试 | 激活 |
| TPS2592BA | 4.3V | 6.1V | 自动重试 | 预览 |
| TPS2592AL | 4.3V | 15.0V | 被锁存 | 预览 |
| TPS2592BL | 4.3V | 6.1V | 被锁存 | 激活 |


English Data Sheet: SLVSC11

## ORDERING INFORMATION(1)

| PART NUMBER | PART MARKING | PACKAGE |
|---|---|---|
| TPS2592ALDRC | 2592AL | 10-pin DRC |
| TPS2592AADRC | 2592AA | 10-pin DRC |
| TPS2592BLDRC | 2592BL | 10-pin DRC |
| TPS2592BADRC | 2592BA | 10-pin DRC |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | VALUE(2) MIN | VALUE(2) MAX | UNIT |
|---|---|---|---|---|
| Supply voltage range(3) | VIN | –0.3 | 20 | V |
| | VIN (10ms Transient) | | 22 | V |
| Output voltage | OUT | –0.3 | VIN + 0.3 | V |
| ILIM | | –0.3 | 7 | V |
| EN/UVLO | | –0.3 | 7 | V |
| dV/dT | | –0.3 | 7 | V |
| BFET | | –0.3 | 30 | V |
| Electrostatic discharge | Human body model(4) | | ±2000 | V |
| | Charged-device model(5) | | ±500 | V |
| Continuous power dissipation | | See Thermal Characteristics | | |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

## THERMAL CHARACTERISTICS(1)

| THERMAL METRIC | | TPS2592xx DRC (10) PINS | UNIT |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 45.9 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 53 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 21.2 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 21.4 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 5.9 | |

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range | VIN TPS2592Ax | 4.5 | 12 | 13.8 | V |
| | VIN TPS2592Bx | 4.5 | 5 | 5.5 | |
| | BFET | 0 | | VIN+6 | |
| | dV/dT, EN/UVLO | 0 | | 6 | |
| | ILIM | 0 | | 3.3 | |
| Resistance | ILIM | 40.2 | 100 | 162 | kΩ |
| External capacitance | OUT | 0.1 | 1 | 1000 | µF |
| | dV/dT | | 1 | 1000 | nF |
| Operating junction temperature range, $T_J$ | | –40 | 25 | 125 | °C |
| Operating Ambient temperature range, $T_A$ | | –40 | 25 | 85 | °C |

## ELECTRICAL CHARACTERISTICS

–40°C ≤ $T_J$ ≤ 125°C, VIN = 12V for TPS2592Ax, VIN = 5V for TPS2592Bx, $V_{EN/UVLO}$ = 2V, $R_{ILIM}$ = 100kΩ, $C_{dVdT}$ = OPEN. All voltages referenced to GND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VIN (INPUT SUPPLY)** | | | | | | |
| $V_{UVR}$ | UVLO threshold, rising | | 4.15 | 4.3 | 4.45 | V |
| $V_{UVhyst}$ | UVLO hysteresis | | | 5.4% | | |
| $IQ_{ON}$ | Supply current | Enabled: EN/UVLO = 2V, TPS2592AX | 0.2 | 0.42 | 0.65 | mA |
| | | Enabled: EN/UVLO = 2V, TPS2592Bx | 0.4 | 0.62 | 0.80 | mA |
| $IQ_{OFF}$ | | EN/UVLO = 0V | | 0.1 | 0.25 | mA |
| $V_{OVC}$ | Over-voltage clamp | VIN > 16.5V, $I_{OUT}$ = 10mA, TPS2592Ax | 13.8 | 15 | 16.5 | V |
| | | TPS2592Bx, VIN > 6.75V, $I_{OUT}$ = 10 mA, –40℃ ≤ $T_J$ ≤ 85℃ | 5.5 | 6.1 | 6.75 | |
| | | TPS2592Bx, VIN > 6.75V, $I_{OUT}$ = 10 mA, –40℃ ≤ $T_J$ ≤ 125℃ | 5.25 | 6.1 | 6.75 | |
| **EN/UVLO (ENABLE/UVLO INPUT)** | | | | | | |
| $V_{ENR}$ | EN Threshold voltage, rising | | 1.37 | 1.4 | 1.44 | V |
| $V_{ENF}$ | EN Threshold voltage, falling | | 1.32 | 1.35 | 1.39 | V |
| $I_{EN}$ | EN Input leakage current | 0 V ≤ $V_{EN}$ ≤ 5V | –100 | 0 | 100 | nA |
| $T_{OFFdly}$ | Turn Off delay | EN↓ to BFET↓, $C_{BFET}$ = 0 | | 0.4 | | µs |
| **dV/dT (OUTPUT RAMP CONTROL)** | | | | | | |
| $T_{dVdT}$ | Output ramp time | TPS2592Ax, EN/UVLO → H to OUT = 11.7V, $C_{dVdT}$ = 0 | 0.7 | 1 | 1.3 | ms |
| | | TPS2592Bx, EN/UVLO → H to OUT = 4.9V, $C_{dVdT}$ = 0 | 0.28 | 0.4 | 0.52 | |
| | | TPS2592Ax, EN/UVLO → H to OUT = 11.7V, $C_{dVdT}$ = 1 nF | | 12 | | |
| | | TPS2592Bx, EN/UVLO → H to OUT = 4.9V, $C_{dVdT}$ = 1 nF | | 5 | | |
| $I_{dVdT}$ | dV/dT Charging current | $V_{dVdT}$ = 0 V | | 220 | | nA |
| $R_{dVdT\_disch}$ | dV/dT Discharging resistance | EN/UVLO = 0 V, $I_{dVdT}$ = 10 mA sinking | 50 | 73 | 100 | Ω |
| $V_{dVdTmax}$ | dV/dT Max capacitor voltage | | | 5.5 | | V |
| $GAIN_{dVdT}$ | dV/dT to OUT gain | $\Delta V_{dVdT}$ | | 4.85 | | V/V |

## ELECTRICAL CHARACTERISTICS (continued)

–40°C ≤ $T_J$ ≤ 125°C, VIN = 12V for TPS2592Ax, VIN = 5V for TPS2592Bx, $V_{EN/UVLO}$ = 2V, $R_{ILIM}$ = 100kΩ, $C_{dVdT}$ = OPEN. All voltages referenced to GND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ILIM (CURRENT LIMIT PROGRAMMING)** | | | | | | |
| $I_{ILIM}$ | ILIM Bias current | | | 10 | | µA |
| $I_{OL}$ | Overload current limit | $R_{ILIM}$ = 45.3 kΩ, $V_{VIN-OUT}$ = 1 V | 1.79 | 2.10 | 2.42 | A |
| | | $R_{ILIM}$ = 100 kΩ, $V_{VIN-OUT}$ = 1 V | 3.46 | 3.75 | 4.03 | |
| | | $R_{ILIM}$ = 150 kΩ, $V_{VIN-OUT}$ = 1 V | 4.4 | 5.2 | 6 | |
| $I_{OL-R-Short}$ | | $R_{ILIM}$ = 0 Ω, Shorted Resistor Current Limit (Single Point Failure Test: UL60950) | | 0.7 | | A |
| $I_{OL-R-Open}$ | | $R_{ILIM}$ = OPEN, Open Resistor Current Limit (Single Point Failure Test: UL60950) | | 0.55 | | A |
| $I_{SCL}$ | Short-circuit current limit | $R_{ILIM}$ = 45.3 kΩ, $V_{VIN-OUT}$ = 5 V, TPS2592Bx | 1.72 | 2.05 | 2.38 | A |
| | | $R_{ILIM}$ = 45.3 kΩ, $V_{VIN-OUT}$ = 12 V, TPS2592Ax | 1.66 | 1.98 | 2.29 | |
| | | $R_{ILIM}$ = 100 kΩ, $V_{VIN-OUT}$ = 5 V, TPS2592Bx | 3.14 | 3.56 | 3.98 | |
| | | $R_{ILIM}$ = 100 kΩ, $V_{VIN-OUT}$ = 12 V, TPS2592Ax | 2.90 | 3.32 | 3.75 | |
| | | $R_{ILIM}$ = 150 kΩ, $V_{VIN-OUT}$ = 5 V, TPS2592Bx | 4.12 | 4.86 | 5.60 | |
| | | $R_{ILIM}$ = 150 kΩ, $V_{VIN-OUT}$ = 12 V, TPS2592Ax | 3.75 | 4.42 | 5.10 | |
| $RATIO_{FASTRIP}$ | Fast-Trip comparator level w.r.t. overload current limit | $I_{FASTRIP}$ : $I_{OL}$ | | 160% | | |
| $T_{FastOffDly}$ | Fast-Trip comparator delay | $I_{OUT}$ > $I_{FASTRIP}$ | | 3 | | µs |
| $V_{OpenILIM}$ | ILIM Open resistor detect threshold | $V_{ILIM}$ Rising, $R_{ILIM}$ = OPEN | | 3.1 | | V |
| **OUT (PASS FET OUTPUT)** | | | | | | |
| $T_{ON}$ | Turn-on delay | EN/UVLO → H to $I_{VIN}$ = 100mA, 1A resistive load at OUT | | 220 | | µs |
| $R_{DSon}$ | FET ON resistance | $T_J$ = 25°C | 21 | 28 | 33 | mΩ |
| | | $T_J$ = 125°C(1) | | 39 | 46 | |
| $I_{OUT-OFF-LKG}$ | OUT Bias current in off state | $V_{EN/UVLO}$ = 0 V, $V_{OUT}$ = 0 V (Sourcing) | –5 | 0 | 1 | µA |
| $I_{OUT-OFF-SINK}$ | | $V_{EN/UVLO}$ = 0V, $V_{OUT}$ = 300 mV (Sinking) | 10 | 15 | 20 | |
| **BFET (BLOCKING FET GATE DRIVER)** | | | | | | |
| $I_{BFET}$ | BFET Charging current | $V_{BFET}$ = $V_{OUT}$ | | 2 | | µA |
| $V_{BFETmax}$ | BFET Clamp voltage | | | $V_{VIN+6.4}$ | | V |
| $R_{BFETdisch}$ | BFET Discharging resistance | $V_{EN/UVLO}$ = 0 V, $I_{BFET}$ = 100 A | 15 | 26 | 36 | Ω |
| $T_{BFET-ON}$ | BFET Turn-on duration | EN/UVLO → H to $V_{BFET}$ = 12 V, $C_{BFET}$ = 1 nF | | 4.2 | | ms |
| | | EN/UVLO → H to $VB_{FET}$ = 12 V, $C_{BFET}$ = 10 nF | | 42 | | |
| $T_{BFET-OFF}$ | BFET Turn-off duration | EN/UVLO → L to $_{VBFET}$ = 1 V, $C_{BFET}$ = 1 nF | | 0.4 | | µs |
| | | EN/UVLO → L to $V_{BFET}$ = 1 V, $C_{BFET}$ = 10 nF | | 1.4 | | |
| **TSD (THERMAL SHUT DOWN)** | | | | | | |
| $T_{SHDN}$ | TSD Threshold, rising(1) | | | 160 | | °C |
| $T_{SHDNhyst}$ | TSD Hysteresis(1) | | | 10 | | °C |
| | Thermal fault: latched or autoretry | TPS2592xL | | LATCHED | | |
| | | TPS2592xA | | AUTO-RETRY | | |

(1) The limits for these parameters are specified based on characterization data, and are not tested during production.

## TYPICAL CHARACTERISTICS

$T_J$ = 25°C, $V_{VIN}$ = 12 V for TPS2592Ax, $V_{VIN}$ = 5 V for TPS2592Bx, $V_{EN/UVLO}$ = 2 V, $R_{ILIM}$ = 100 kΩ, $C_{VIN}$=0.1 µF, $C_{OUT}$=1µF, $C_{dVdT}$ = OPEN (unless stated otherwise)

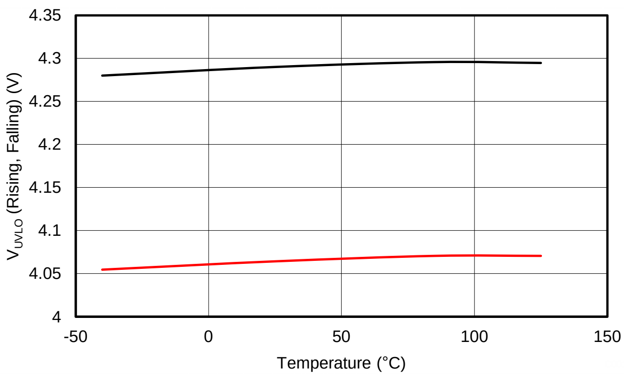



**Figure 1. $V_{UVLO}$ vs TEMPERATURE**

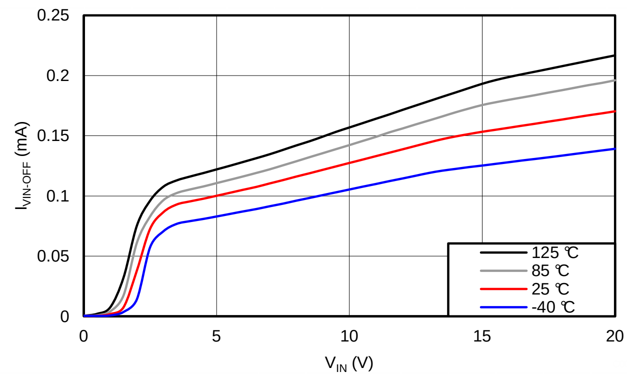



**Figure 2. $I_{VIN-OFF}$ vs $V_{IN}$ ACROSS TEMPERATURE**

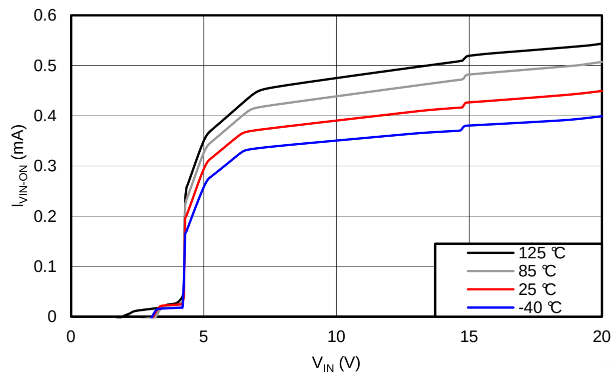



**Figure 3. $I_{VIN-ON}$ vs $V_{IN}$ ACROSS TEMPERATURE (TPS2592Ax)**

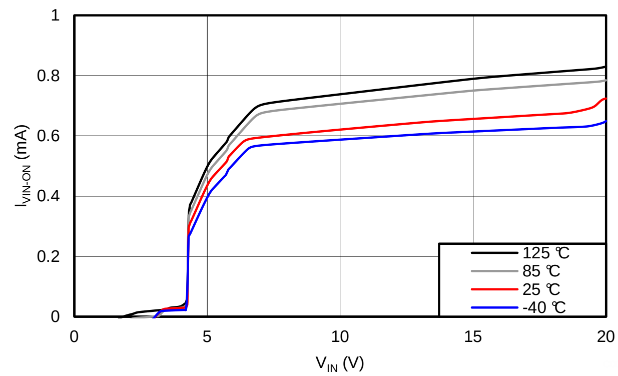



**Figure 4. $I_{VIN-ON}$ vs $V_{IN}$ ACROSS TEMPERATURE (TPS2592Bx)**

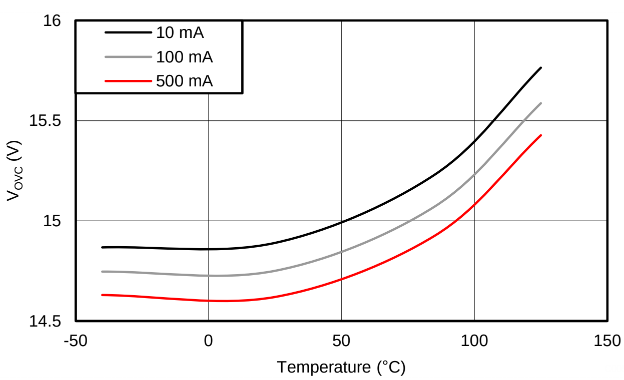



**Figure 5. $V_{OVC}$ vs TEMPERATURE ACROSS $I_{OUT}$ (TPS2592Ax)**

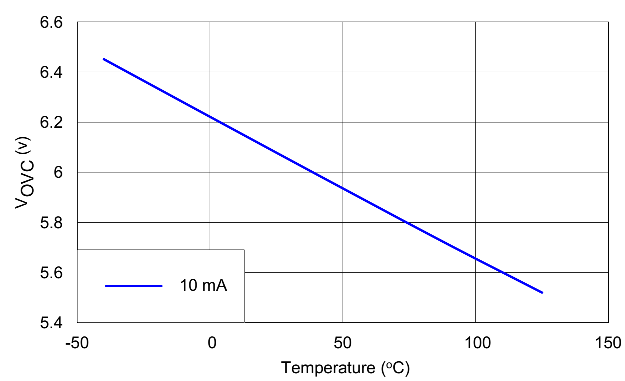



**Figure 6. $V_{OVC}$ vs TEMPERATURE (TPS2592Bx)**

## TYPICAL CHARACTERISTICS (continued)

$T_J$ = 25°C, $V_{VIN}$ = 12 V for TPS2592Ax, $V_{VIN}$ = 5 V for TPS2592Bx, $V_{EN/UVLO}$ = 2 V, $R_{ILIM}$ = 100 kΩ, $C_{VIN}$=0.1 µF, $C_{OUT}$=1µF, $C_{dVdT}$ = OPEN (unless stated otherwise)

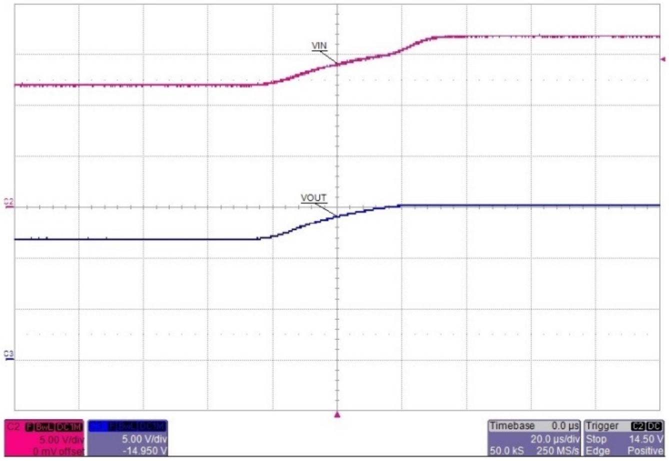



**Figure 7. TRANSIENT: OVER-VOLTAGE CLAMP: TPS2592Ax**

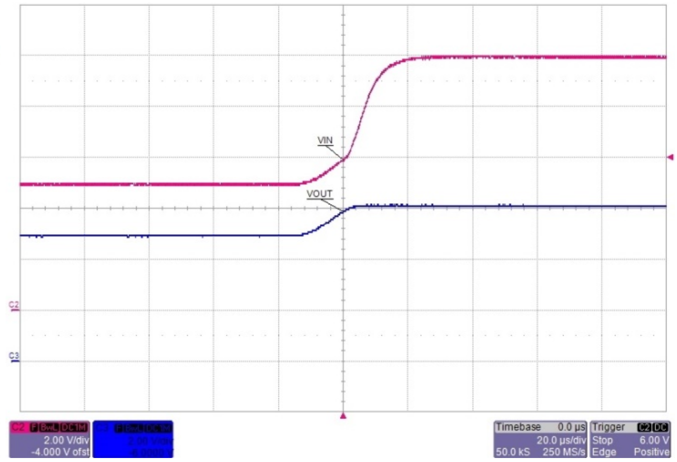



**Figure 8. TRANSIENT: OVER-VOLTAGE CLAMP: TPS2592Bx**

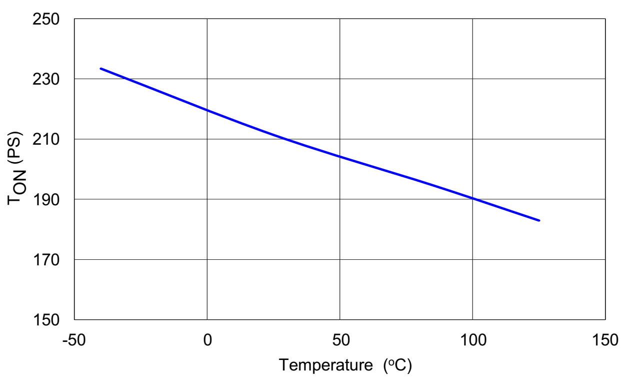



**Figure 9. $T_{ON}$ vs TEMPERATURE**

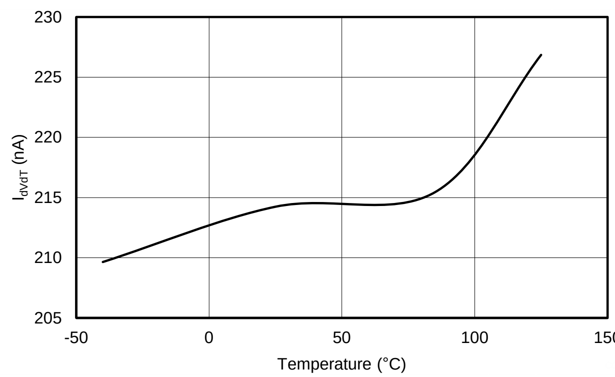



**Figure 10. $I_{dVdT}$ vs TEMPERATURE**

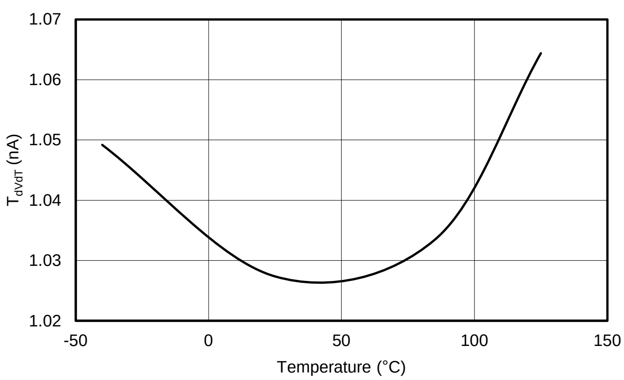



**Figure 11. $T_{dVdT}$ vs TEMPERATURE (TPS2592Ax)**

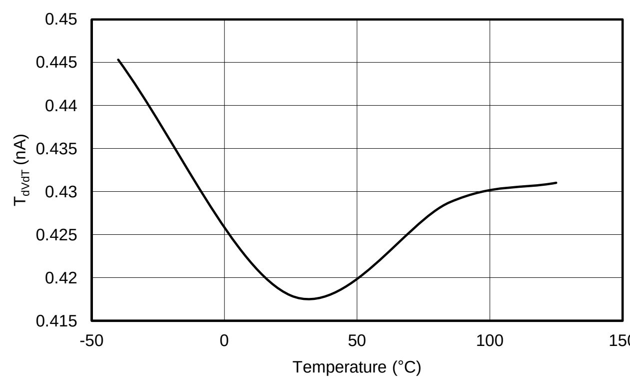



**Figure 12. $T_{dVdT}$ vs TEMPERATURE (TPS2592Bx)**

## TYPICAL CHARACTERISTICS (continued)

$T_J$ = 25°C, $V_{VIN}$ = 12 V for TPS2592Ax, $V_{VIN}$ = 5 V for TPS2592Bx, $V_{EN/UVLO}$ = 2 V, $R_{ILIM}$ = 100 kΩ, $C_{VIN}$=0.1 µF, $C_{OUT}$=1µF, $C_{dVdT}$ = OPEN (unless stated otherwise)

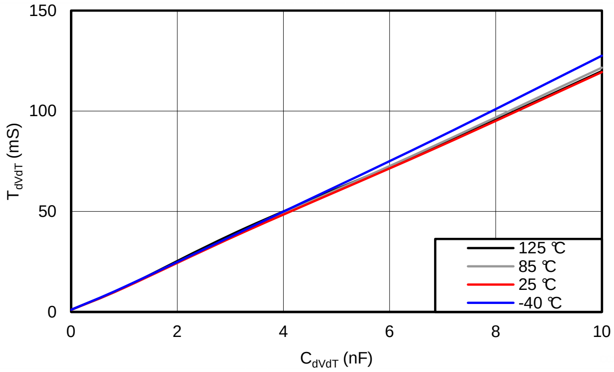



**Figure 13. $T_{dVdT}$ vs $C_{dVdT}$ (TPS2592Ax)**

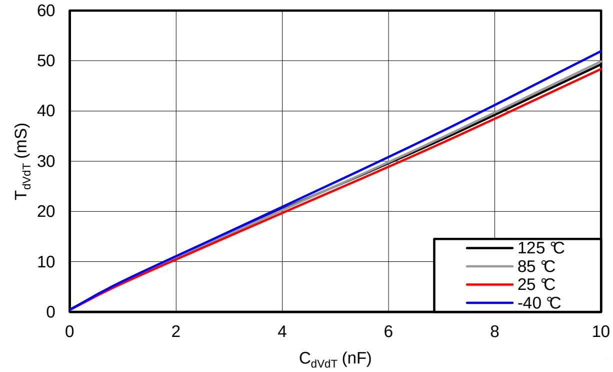



**Figure 14. $T_{dVdT}$ vs $C_{dVdT}$ (TPS2592Bx)**

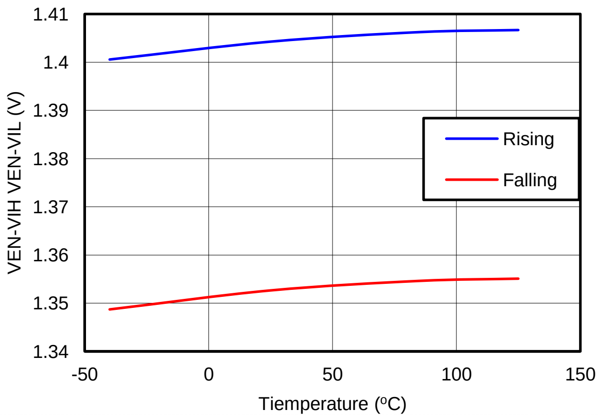



**Figure 15. $V_{EN\_VIH}$, $V_{EN\_VIL}$ vs TEMPERATURE**

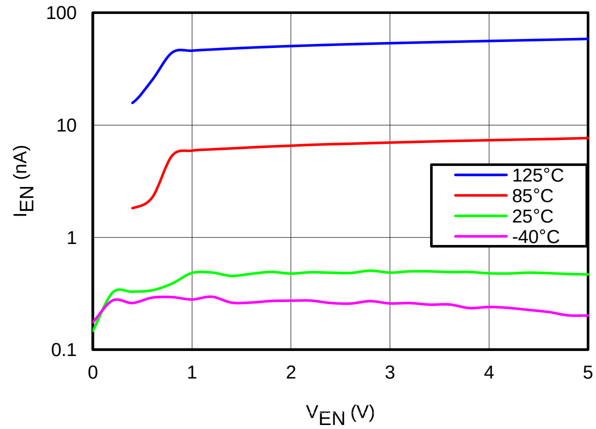



**Figure 16. $I_{EN}$ (Leakage Current) vs $V_{EN}$**

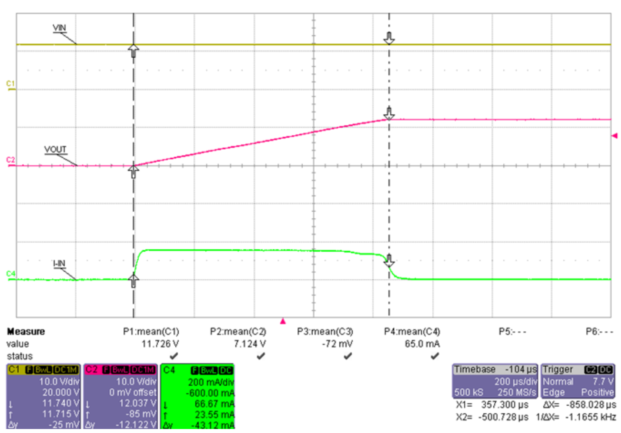



**Figure 17. TRANSIENT: OUTPUT RAMP ($C_{dVdT}$ = OPEN): TPS2592Ax**

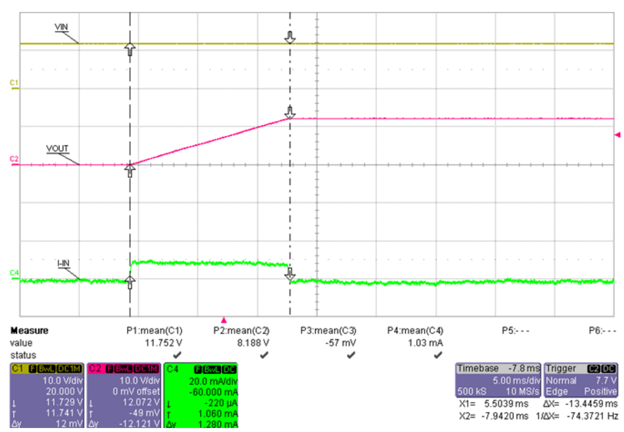



**Figure 18. TRANSIENT: OUTPUT RAMP ($C_{dVdT}$ = 1 nF): TPS2592Ax**

## TYPICAL CHARACTERISTICS (continued)

$T_J$ = 25°C, $V_{VIN}$ = 12 V for TPS2592Ax, $V_{VIN}$ = 5 V for TPS2592Bx, $V_{EN/UVLO}$ = 2 V, $R_{ILIM}$ = 100 kΩ, $C_{VIN}$=0.1 µF, $C_{OUT}$=1µF, $C_{dVdT}$ = OPEN (unless stated otherwise)

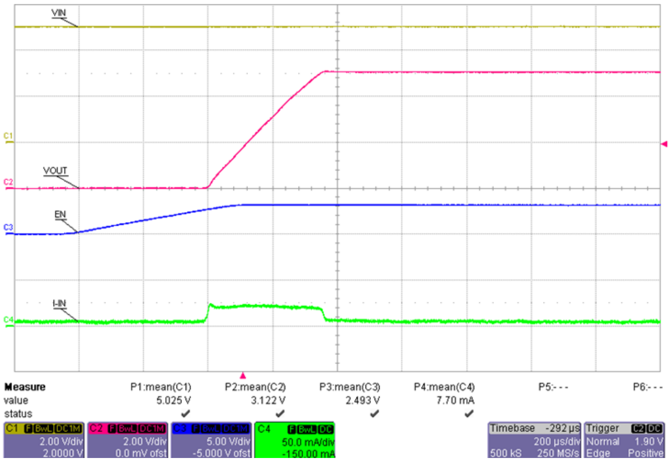



**Figure 19. TRANSIENT: OUTPUT RAMP ($C_{dVdT}$ = OPEN): TPS2592Bx**

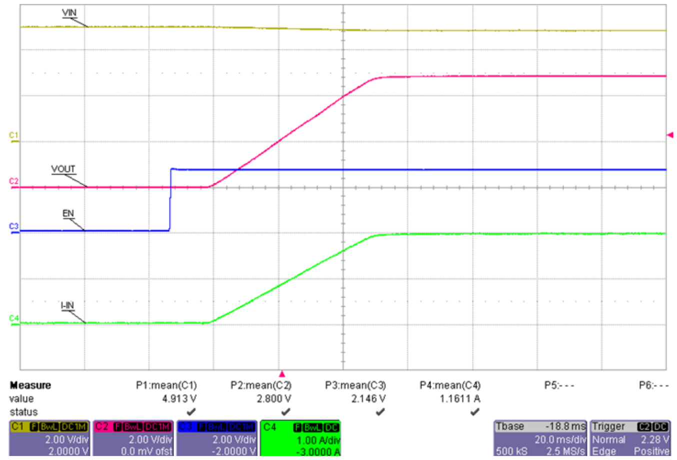



**Figure 20. Transient Output Ramp ($C_{dVdT}$ = 1 nF, $C_{OUT}$=10 µF, $R_{OUT}$= 2.5 Ω) : TPS2592Bx**

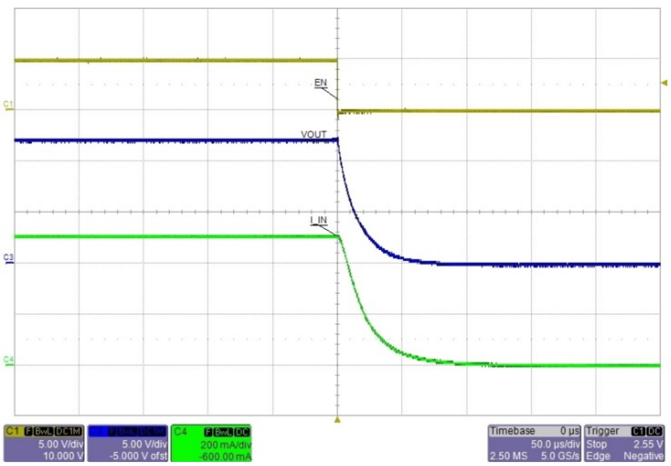



**Figure 21. TRANSIENT: TURN OFF DELAY (EN ↓)**

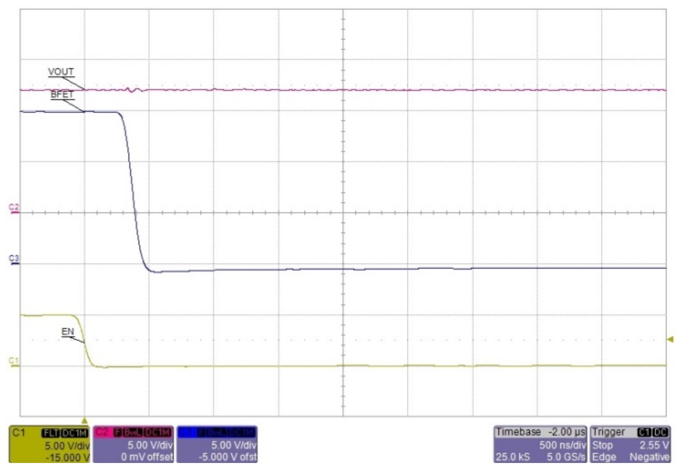



**Figure 22. TURN OFF DELAY TO BFET (EN↓)**

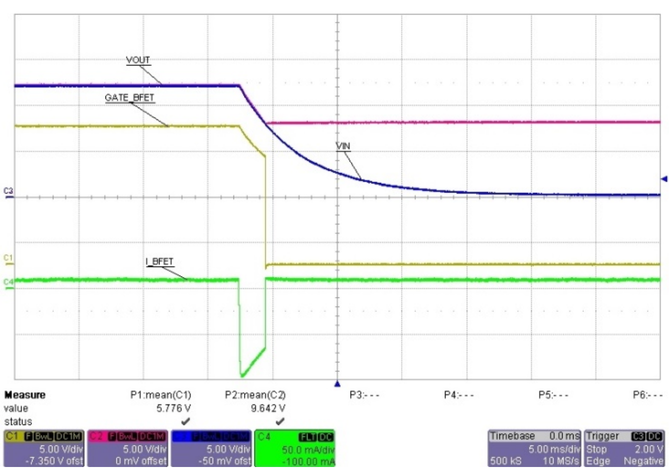



**Figure 23. TURN OFF DELAY TO BFET (VIN↓)**

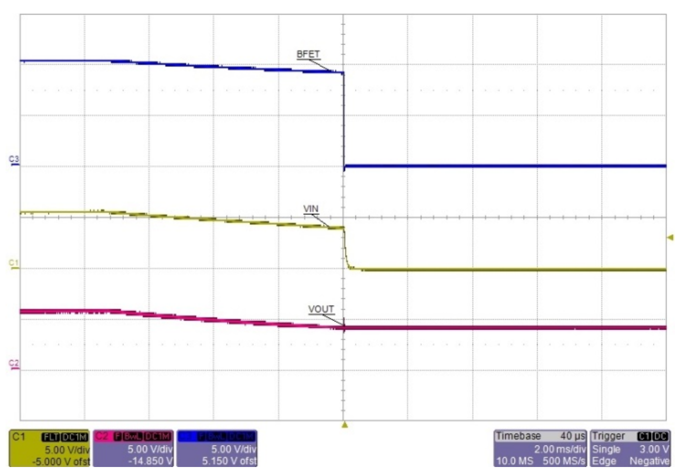



**Figure 24. TRANSIENT: TURN OFF DELAY TO BFET (VIN↓)**

## TYPICAL CHARACTERISTICS (continued)

$T_J$ = 25°C, $V_{VIN}$ = 12 V for TPS2592Ax, $V_{VIN}$ = 5 V for TPS2592Bx, $V_{EN/UVLO}$ = 2 V, $R_{ILIM}$ = 100 kΩ, $C_{VIN}$=0.1 µF, $C_{OUT}$=1µF, $C_{dVdT}$ = OPEN (unless stated otherwise)

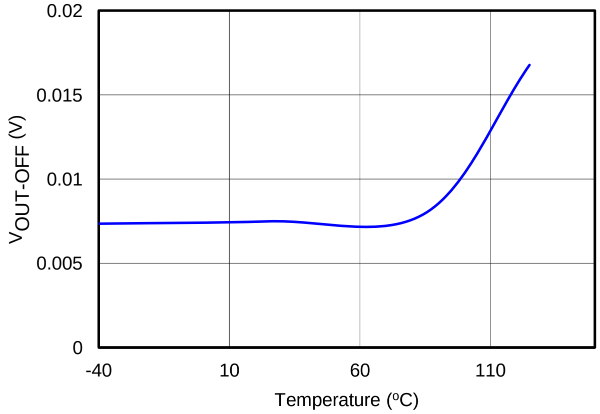



**Figure 25. $V_{OUT-OFF}$ vs TEMPERATURE**

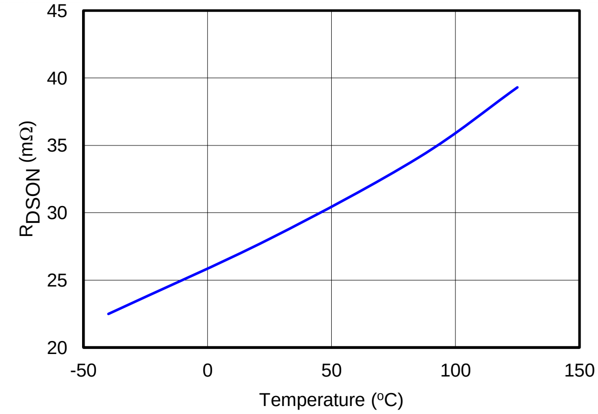



**Figure 26. $R_{DSON}$ vs TEMPERATURE**

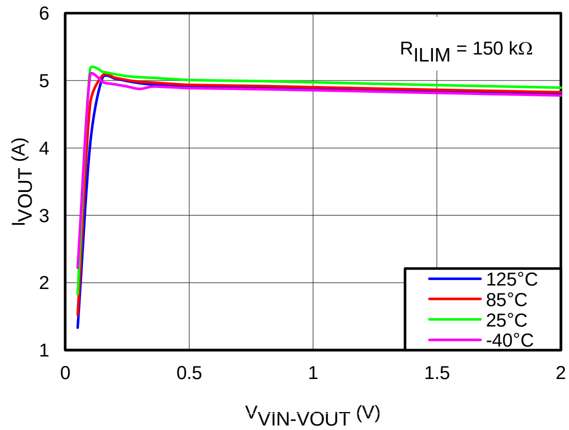



**Figure 27. $I_{OUT}$ vs $V_{VIN-OUT}$ ACROSS TEMPERATURE (150kΩ)**

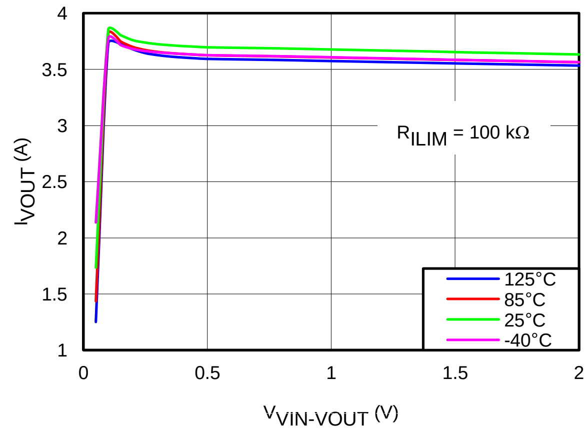



**Figure 28. $I_{OUT}$ vs $V_{VIN-OUT}$ ACROSS TEMPERATURE (100kΩ)**

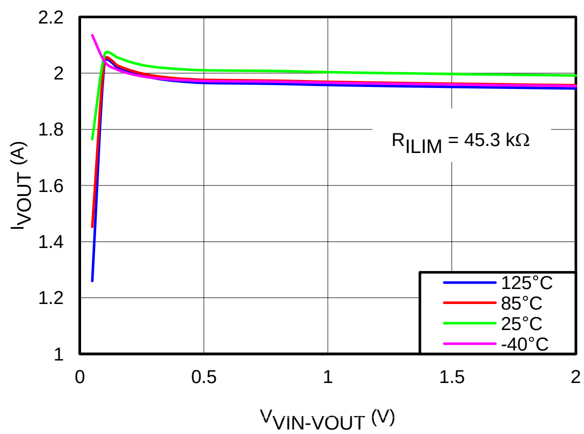



**Figure 29. $I_{OUT}$ vs $V_{VIN-OUT}$ ACROSS TEMPERATURE (45.3kΩ)**

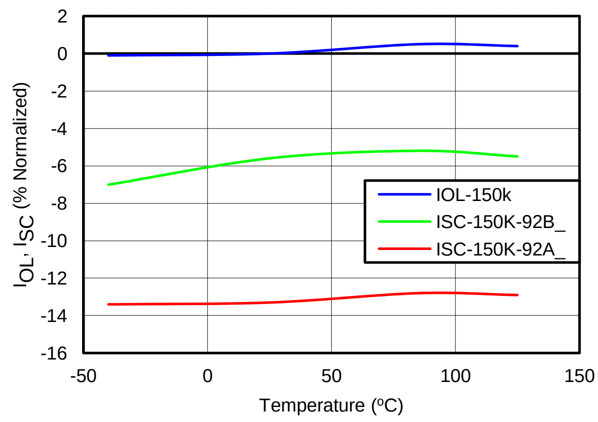



**Figure 30. $I_{OL}$, $I_{SC}$ vs TEMPERATURE (150kΩ)**

## TYPICAL CHARACTERISTICS (continued)

$T_J$ = 25°C, $V_{VIN}$ = 12 V for TPS2592Ax, $V_{VIN}$ = 5 V for TPS2592Bx, $V_{EN/UVLO}$ = 2 V, $R_{ILIM}$ = 100 kΩ, $C_{VIN}$=0.1 µF, $C_{OUT}$=1µF, $C_{dVdT}$ = OPEN (unless stated otherwise)

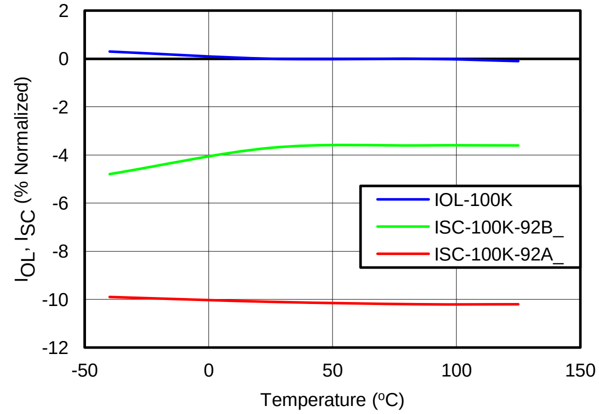



**Figure 31. $I_{OL}$, $I_{SC}$ vs TEMPERATURE (100kΩ)**

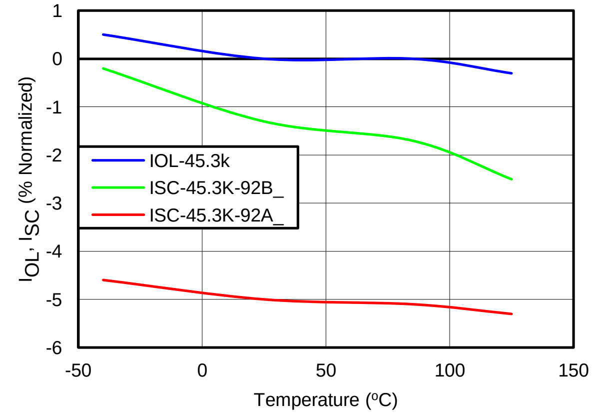



**Figure 32. $I_{OL}$, $I_{SC}$ vs TEMPERATURE (45.3kΩ)**

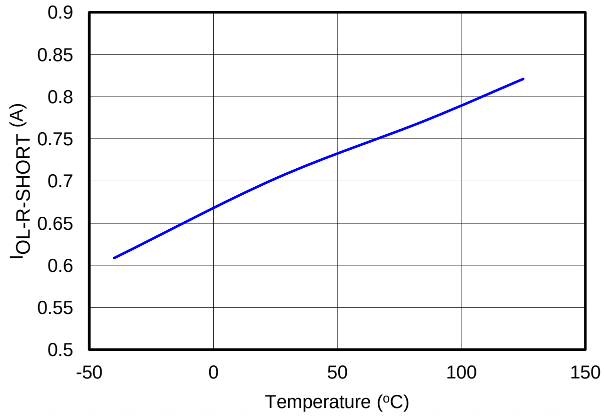



**Figure 33. $I_{OL\text{-}R\text{-}Short}$ vs TEMPERATURE ($R_{ILIM}$ = 0)**

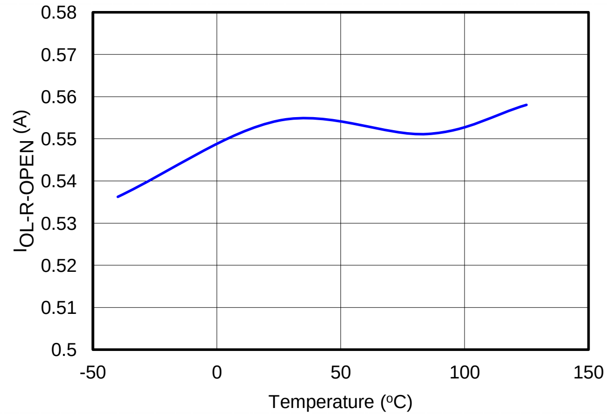



**Figure 34. $I_{OL\text{-}R\text{-}Open}$ vs TEMPERATURE ($R_{ILIM}$ = OPEN)**

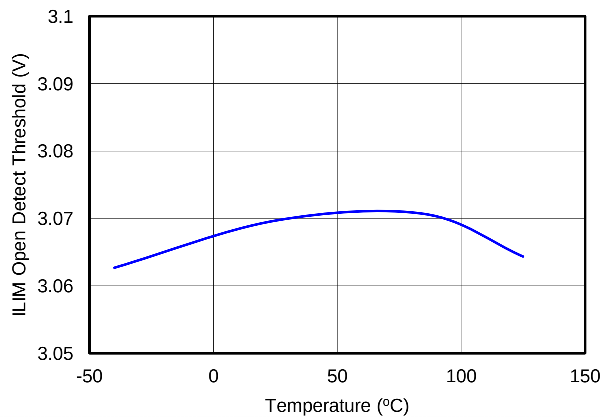



**Figure 35. $V_{OpenILIM}$ vs TEMPERATURE**

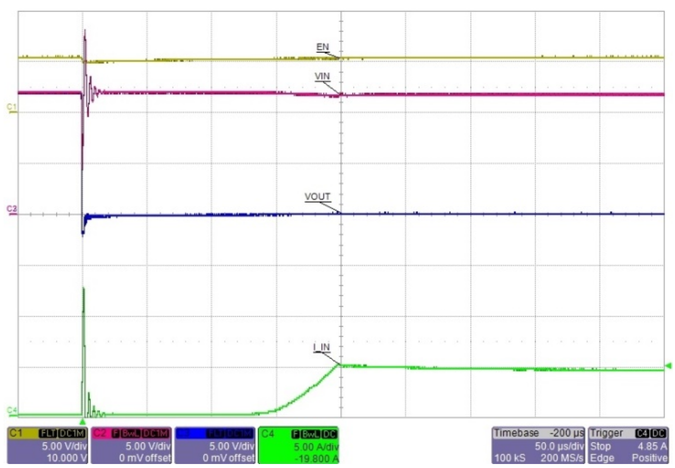



**Figure 36. TRANSIENT: OUTPUT SHORT CIRCUIT**

## TYPICAL CHARACTERISTICS (continued)

$T_J$ = 25°C, $V_{VIN}$ = 12 V for TPS2592Ax, $V_{VIN}$ = 5 V for TPS2592Bx, $V_{EN/UVLO}$ = 2 V, $R_{ILIM}$ = 100 kΩ, $C_{VIN}$=0.1 µF, $C_{OUT}$=1µF, $C_{dVdT}$ = OPEN (unless stated otherwise)

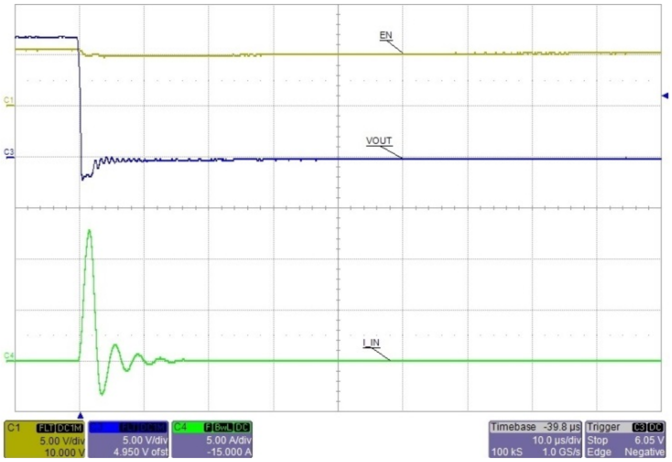



**Figure 37. SHORT CIRCUIT (Zoom): FAST-TRIP COMPARATOR**

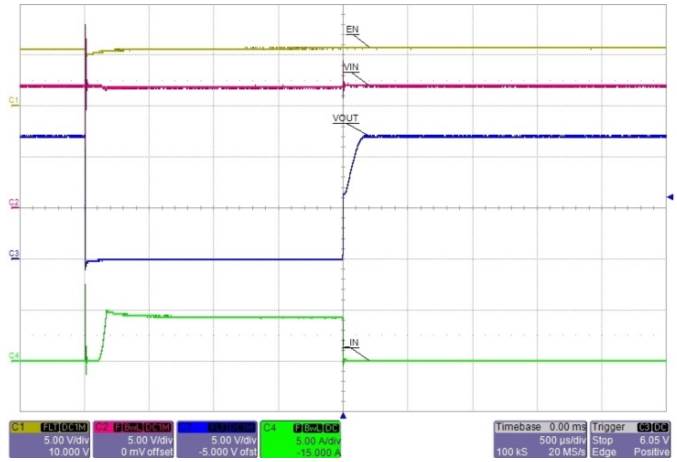



**Figure 38. TRANSIENT: RECOVERY FROM SHORT CIRCUIT**

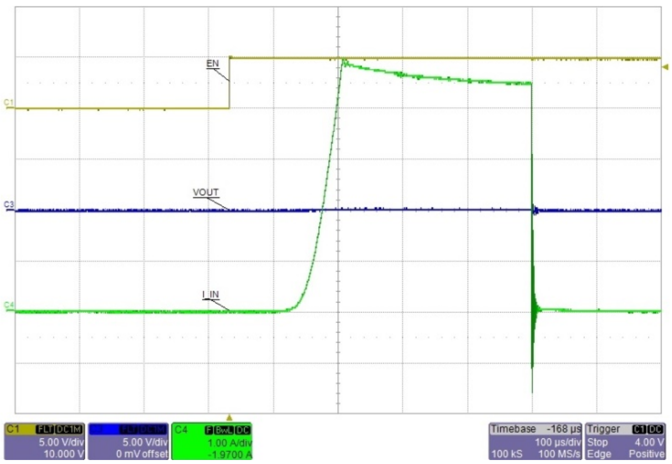



**Figure 39. TRANSIENT: WAKE UP TO SHORT CIRCUIT**

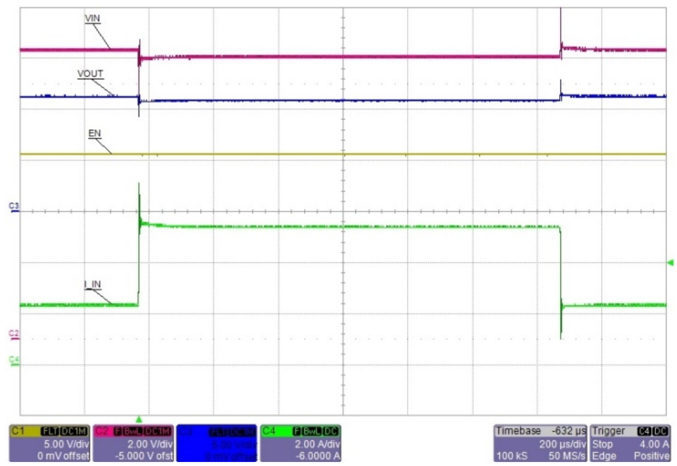



**Figure 40. TRANSIENT: OVERLOAD CURRENT LIMIT: ($I_{LOAD}$ stepped from 50% to 120%, back to 50%)**

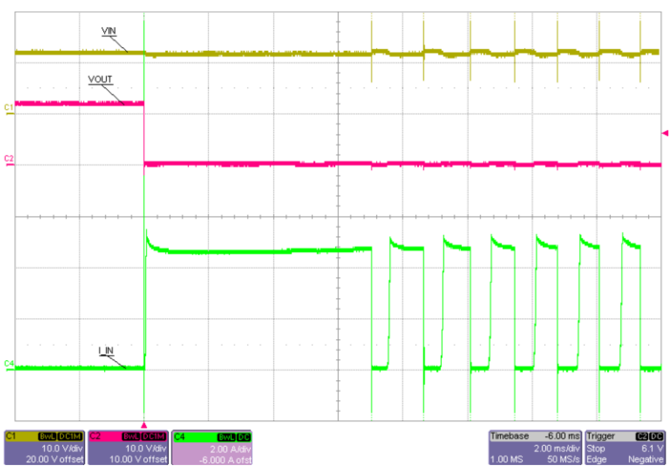



**Figure 41. TRANSIENT: THERMAL FAULT AUTO-RETRY (TPS2592xA)**

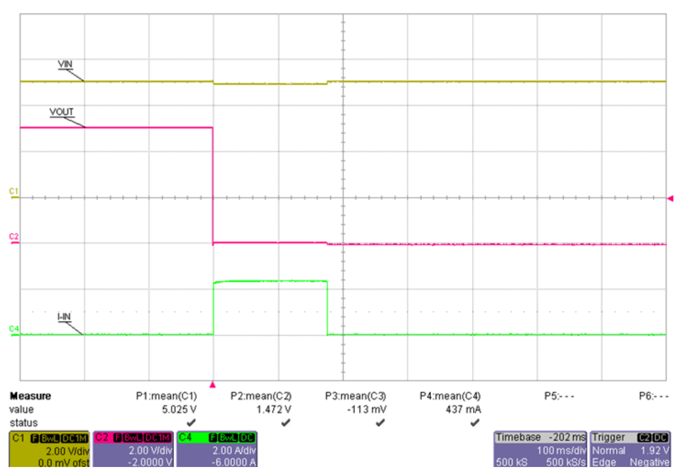
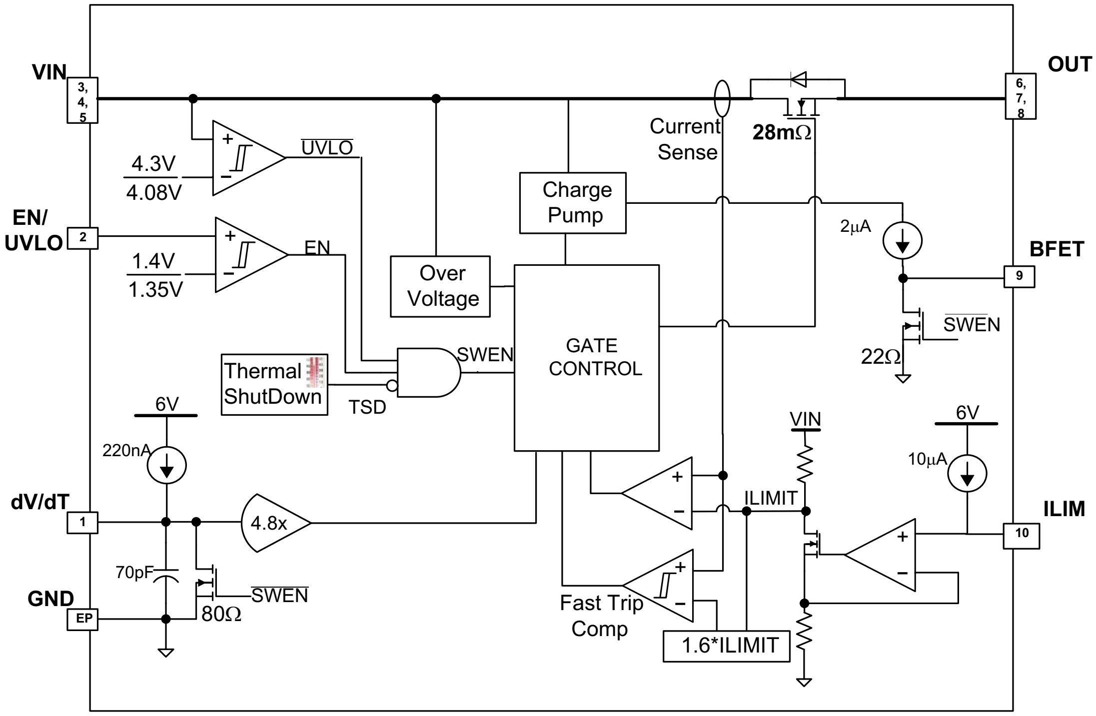
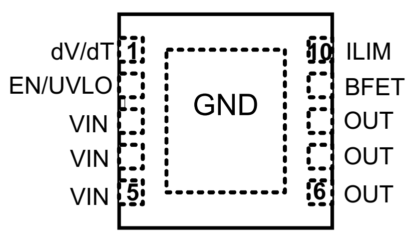



**Figure 42. TRANSIENT: THERMAL FAULT LATCHED (TPS2592xL)**

## FUNCTIONAL BLOCK DIAGRAM




**DRC PACKAGE**
**(TOP VIEW)**




## PIN DESCRIPTIONS

| PIN | | DESCRIPTION |
|---|---|---|
| **NAME** | **NO.** | |
| **SUPPLY PINS** | | |
| VIN | 3-5 | Input Supply Voltage |
| GND | Power Pad | GND |
| **CONTROL PINS** | | |
| dV/dT | 1 | Tie a capacitor from this pin to GND to control the ramp rate of OUT at device turn-on. |
| EN/UVLO | 2 | This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET and pulls BFET to GND. When pulled high, it enables the device and BFET.<br>As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider. |
| BFET | 9 | Connect this pin to the gate of a blocking NFET. See detailed pin description and application note in this datasheet. |
| ILIM | 10 | A resistor from this pin to GND will set the overload and short circuit limit. |
| **LOAD PINS** | | |
| OUT | 6-8 | Output of the device |

## DEVICE OPERATION

The TPS2592xx is a hot-swap controller with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage threshold ($V_{UVLO}$), the device samples the EN/UVLO pin. A high level on this pin will enable the internal MOSFET and also start charging the gate of external blocking FET (if connected) via the BFET pin. As VIN rises, the internal MOSFET of the device and external FET (if connected) will start conducting and allow current to flow from VIN to OUT. When EN/UVLO is held low (i.e., below $V_{ENF}$), the internal MOSFET is turned off and BFET pin is discharged, thereby blocking the flow of current from VIN to OUT. User also has the ability to modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

Having successfully completed its start-up sequence, the device now actively monitors its load current and input voltage, ensuring that the adjustable overload current limit $I_{OL}$ is not exceeded and input voltage spikes are safely clamped to $V_{OVC}$ level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature ($T_J$) exceeds $T_{SHDN}$ , typically 160°C, the thermal shutdown circuitry will shut down the internal MOSFET thereby disconnecting the load from the supply. In the TPS2592xL, the output will remain disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS2592xA device will remain off during a cooling period until device temperature falls below $T_{SHDN}$ – 10°C, after which it will attempt to restart. This ON and OFF cycle will continue until fault is cleared.

## DETAILED PIN DESCRIPTION

**GND:** This is the most negative voltage in the circuit and is used as a reference for all voltage measurements unless otherwise specified.

**VIN:** Input voltage to the TPS2592xx. A ceramic bypass capacitor close to the device from VIN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 4.5V – 13.8V for TPS2592Ax and 4.5V – 5.5V for TPS2592Bx. The device can continuously sustain a voltage of 20V on VIN pin. However, above the recommended maximum bus voltage, the device will be in over-voltage protection (OVP) mode, limiting the output voltage to $V_{OVC}$. The power dissipation in OVP mode is $P_{D\_OVP} = (V_{VIN} - V_{OVC}) * I_{OUT}$, which can potentially heat up the device and cause thermal shutdown.

**dV/dT:** Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum $T_{dVdT}$) on the output. Equation governing slew rate at start-up is shown below:

$$I_{dVdT} = \left(C_{EXT} + C_{INT}\right) \times \frac{\left(\frac{dV_{OUT}}{dT}\right)}{GAIN_{dVdT}} \quad (1)$$

Where:

$I_{dVdT}$ = 220 nA (TYP)
$C_{INT}$ = 70pF (TYP)
$GAIN_{dVdT}$ = 4.85
$\frac{dV_{OUT}}{dT}$ = Desired output slew rate

The total ramp time ($T_{dVdT}$) for 0 to VIN can be calculated using the following equation:

$$T_{dVdT} = 10^6 \times VIN \times \left(C_{EXT} + 70pF\right) \quad (2)$$

For details on how to select an appropriate charging time/rate, refer to the applications section: "INRUSH CURRENT AND POWER DISSIPATION DURING START-UP".

**BFET:** Connect this pin to an external NFET that can be used to disconnect input supply from rest of the system in the event of power failure at VIN. BFET pin is controlled by either UVLO event or EN/UVLO (see table below). BFET can source charging current of 2µA (TYP) and sink (discharge) current from the gate of the external FET via a 26Ω internal discharge resistor to initiate fast turn-off, typically <1 µs.

| EN/UVLO > $V_{ENR}$ | VIN>$V_{UVR}$ | BFET Mode |
|---|---|---|
| H | H | Charge |
| X | L | Discharge |
| L | X | Discharge |

**EN/UVLO:** As an input pin, it controls both the ON/OFF state of the internal MOSFET and that of the external blocking FET. In its high state, the internal MOSFET is enabled and charging begins for the gate of external FET. A low on this pin will turn off the internal MOSFET and pull the gate of the external FET to GND via the built-in discharge resistor. High and Low levels are specified in the parametric table of the datasheet. The EN/UVLO pin is also used to clear a thermal shutdown latch in the TPS2592xL by toggling this pin (H→L).

The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (1us typical) for quick detection of power failure. When used with a resistor divider from supply to EN/UVLO to GND, power-fail detection on EN/UVLO helps in quick turn-off of the BFET driver, thereby stopping the flow of reverse current (see typical application diagram, Figure 47). For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND

**ILIM:** The device continuously monitors the load current and keeps it limited to the value programmed by RILIM. After start-up event and during normal operation, current limit is set to $I_{OL}$ (over-load current limit).

$$I_{OL} = \left(0.7 + 3 \times 10^{-5} \times R_{ILIM}\right) \quad (3)$$

When power dissipation in the internal MOSFET [$P_D$ = ($V_{VIN}$ -$V_{OUT}$) × $I_{OUT}$] exceeds 10W, there is a 2% – 12% thermal foldback in the current limit value so that $I_{OL}$ drops to $I_{SC}$. In each of the two modes, MOSFET gate voltage is regulated to throttle short-circuit and overload current flowing to the load. Eventually, the device shuts down due to over temperature.

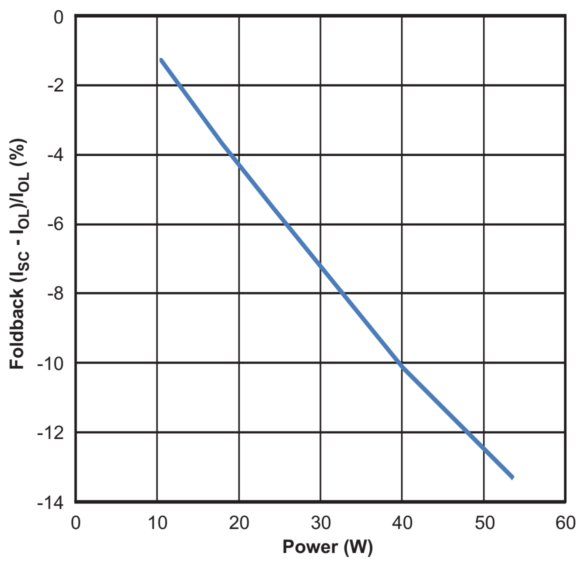



**Figure 43. Thermal Foldback in Current Limit**

During a transient short circuit event, the current through the device increases very rapidly. The current-limit amplifier cannot respond very quickly to this event due to its limited bandwidth. Therefore, the TPS2592 incorporates a fast-trip comparator, which shuts down the pass device very quickly when $I_{OUT}$ > $I_{FASTRIP}$, and terminates the rapid short-circuit peak current. The trip threshold is set to 60% higher than the programmed over-load current limit ($I_{FASTRIP}$ = 1.6 x $I_{OL}$). After the transient short-circuit peak current has been terminated by the fast-trip comparator, the current limit amplifier smoothly regulates the output current to $I_{OL}$ (see figure below).

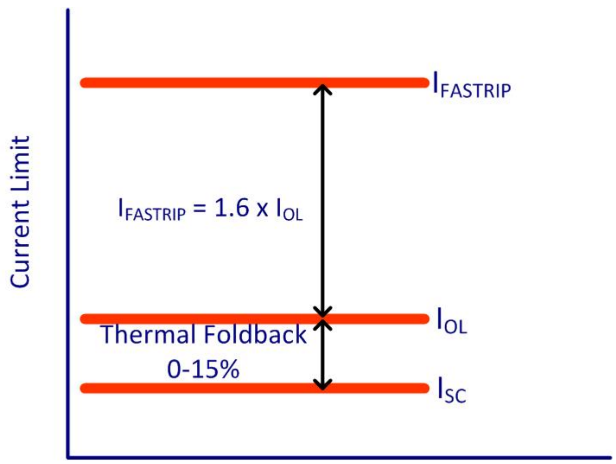



**Figure 44. Fast-Trip Current**

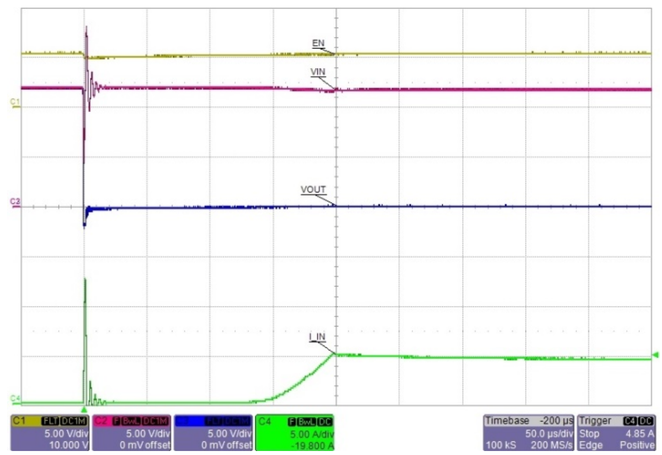



**Figure 45. Fast-Trip and Current Limit Amplifier Response for Short Circuit**

## TYPICAL APPLICATIONS

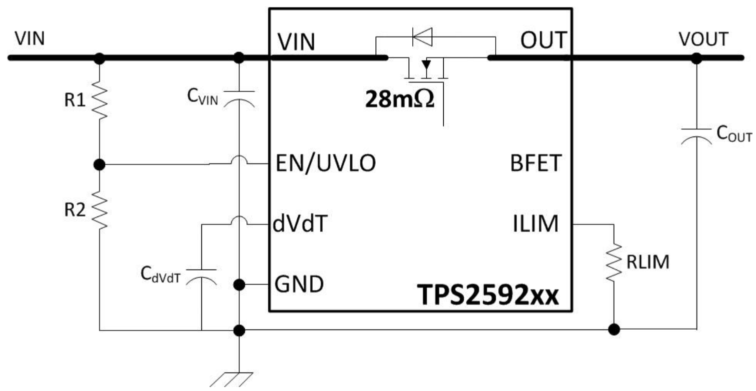



**Figure 46. Simple e-Fuse (Current-Limiter): Application with Output Ramp-Rate Control**

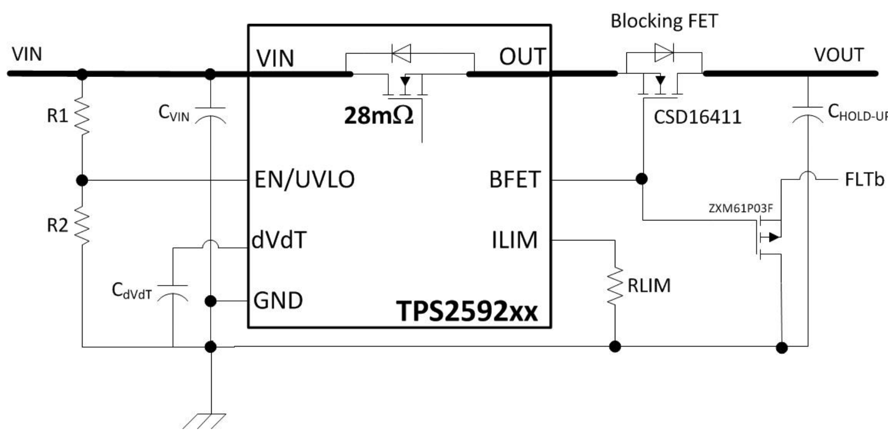



**Figure 47. Reverse Current Protection (e.g., SSD) Application with Blocking FET $C_{HOLD-UP}$ (TPS2592 UVLO is used as power fail comparator)**

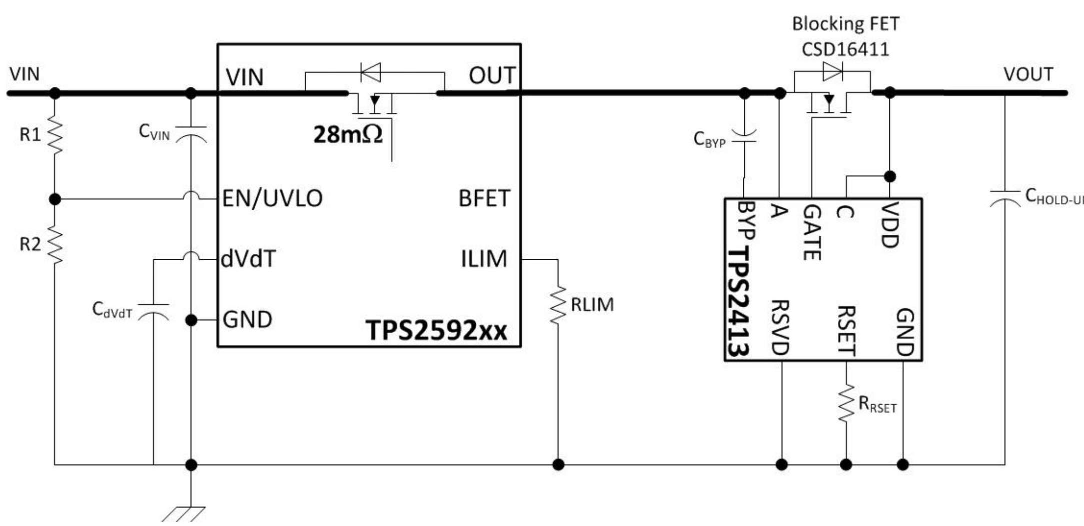



**Figure 48. Reverse Current Protection Application with External Blocking Controller (TPS2413 is used as reverse current comparator)**

# APPLICATION INFORMATION

## INRUSH CURRENT AND POWER DISSIPATION DURING START-UP

A successful design needs to keep the junction temperature of TPS2592 well below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up.

During start-up, as the output capacitor charges, the voltage difference across the internal FET decreases, and the power dissipated decreases as well. Typical ramp-up of output voltage $V_{OUT}$ with inrush current limit is shown in Figure 49 and variation of power dissipation with ramp-up time is plotted in Figure 50. The average power dissipated in the device during start-up is equal to area of triangular plot as highlighted.

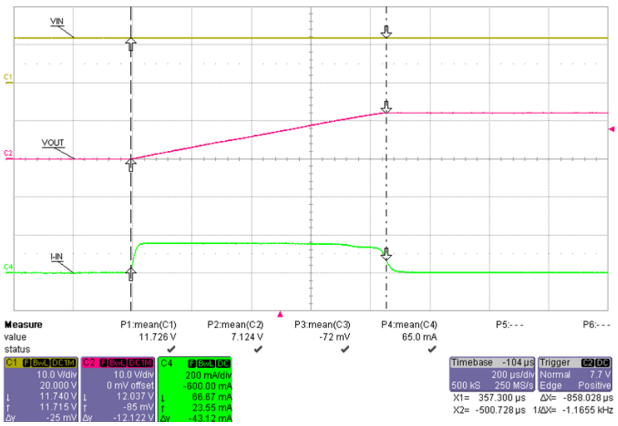



Figure 49. Start-Up Waveform

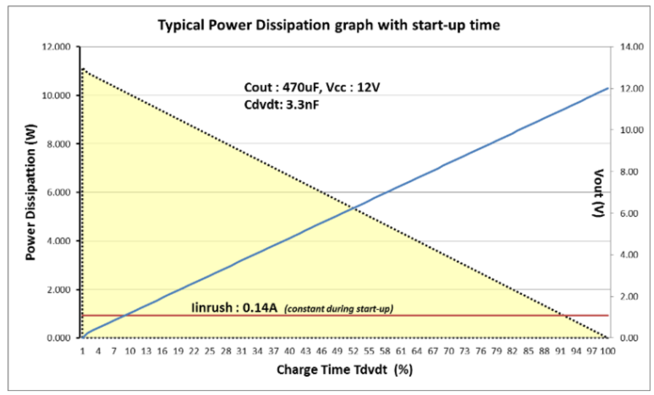



Figure 50. $P_{DISS}$ During Start-Up

For the TPS2592, the inrush current is determined as:

$$I = C \times \frac{dv}{dt} => I_{INRUSH} = C_{OUT} \times \frac{V_{VIN}}{T_{dvdt}} \quad (4)$$

Power dissipation during start-up will be:

$$P_{INRUSH} = 0.5 \times V_{VIN} \times I_{INRUSH} \quad (5)$$

The above calculation assumes that load does not draw any current until the output voltage has reached its final value.

If the load draws current during the turn-on sequence, there will be additional power dissipated during the start-up phase. Considering a resistive load $R_L$, load current ramps up proportionally with increase in output voltage during $T_{dvdt}$ time. Typical ramp-up of output voltage $V_{OUT}$ and Load current is shown in Figure 51 and variation of power dissipation with ramp-up time is plotted in Figure 52. The additional power dissipation during start-up phase is represented and calculated as follows:

$$V_{DS}(t) = V_{VIN} \times \left(1 - \frac{t}{T_{dvdt}}\right) \quad (6)$$

$$I_{LOAD}(t) = \left(\frac{V_{VIN}}{R_L}\right) \times \frac{t}{T_{dvdt}} \quad (7)$$

Average energy loss due in FET during charging time due to resistive load is given by:

$$W_{Tdvdt} = \int_0^{Tdvdt} V_{VIN} \times \left(1 - \frac{t}{T_{dvdt}}\right) \times \left(\frac{V_{VIN}}{R_L} \times \frac{t}{T_{dvdt}}\right) dt \quad (8)$$

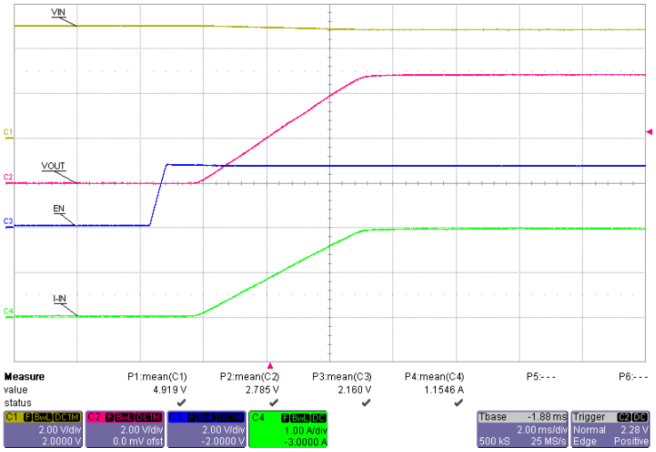



Figure 51. Start-up Waveform with Load (2.5W)

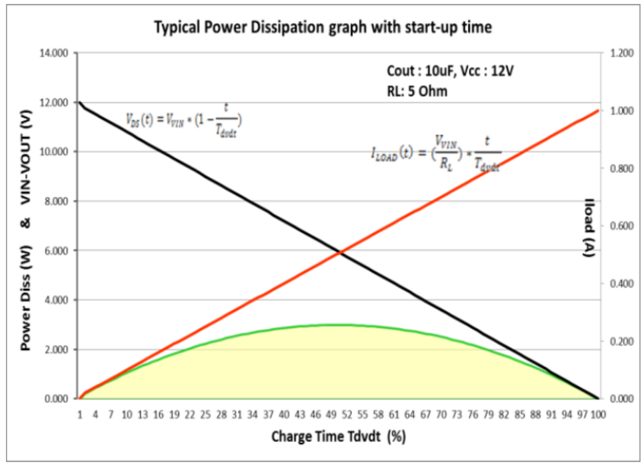



Figure 52. $P_{DISS}$ During Due to Load Current

Linearizing the parabolic equation and representing as triangle, the average power loss is:

$$P_{DISS\_LOAD} = \left(\frac{1}{6}\right) \times \frac{V_{VIN}^2}{R_L} \tag{9}$$

Total power dissipated in the device during startup is:

$$P_{STARTUP} = P_{INRUSH} + P_{DISS\_LOAD} \tag{10}$$

Total current during startup is given by:

$$I_{STARTUP} = I_{INRUSH} + I_{LOAD}(t) \tag{11}$$

If $I_{STARTUP} > I_{LIM}$, the device limits the current to $I_{LIM}$ and the minimum charging time is determined by:

$$T_{dvdt\_min} = C_{OUT} \times \frac{V_{VIN}}{I_{LIM}} \tag{12}$$

Power dissipation for a selected start-up time should not exceed the limits shown in below plots as shaded area. Typical curves for no load and load are shown in Figure 53 and Figure 54.

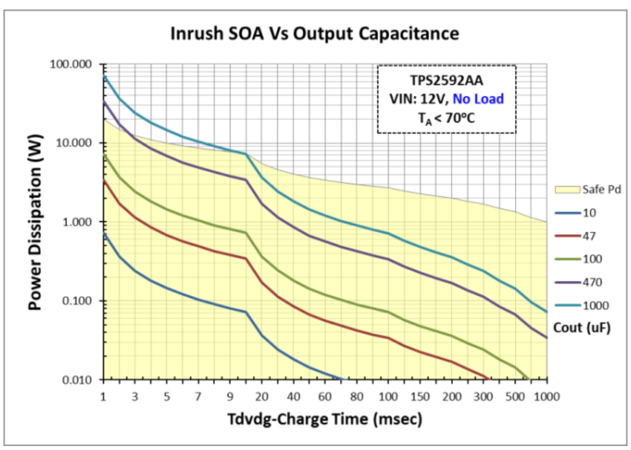



Figure 53. $I_{INRUSH}$ SOA Variation with $C_{OUT}$ and $T_{dvdt}$ (NO Load)

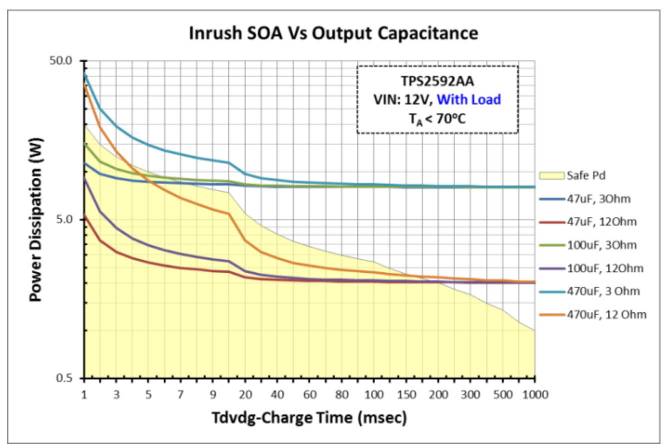



Figure 54. $I_{INRUSH}$ SOA Variation with $C_{OUT}$ and $T_{dvdt}$ (with Load)

**Example:**

$V_{VIN}$ = 12V, $C_{OUT}$ = 470uF, and Load: $R_L$ = 12Ω

As a first choice, let $C_{EXT}$ = $C_{dVdT}$ = 3.3nF:

$$T_{dvdt} = 10^6 \times 12 \times (100pF + 70pF) = 2.04\,ms \quad (13)$$

$$I_{INRUSH} = (470 \times 10^{-6}) \times \left(\frac{12}{2.04 \times 10^{-3}}\right) = 2.764\,A \quad (14)$$

$$P_{INRUSH} = 0.5 \times 12 \times 2.764 = 16.584\,W \quad (15)$$

$$P_{DISS\_LOAD} = \left(\frac{1}{6}\right) \times \left(\frac{(12 \times 12)}{3}\right) = 2.00\,W \quad (16)$$

$$P_{STARTUP} = (16.584 + 2.00) = 18.84\,W \quad (17)$$

The power dissipated is well above the shaded area of power dissipation graph; to have safe operating power area, increase the capacitance

As a second choice, let $C_{EXT}$ = $C_{dVdT}$ = 0.47 nF:

$$T_{dvdt} = 10^6 \times 12 \times (470pF + 70pF) = 6.48\,ms \quad (18)$$

$$I_{INRUSH} = (470 \times 10^{(-6)}) \times \left(\frac{12}{6.48 \times 10^{(-3)}}\right) = 0.87A \quad (19)$$

$$P_{INRUSH} = 0.5 \times 12 \times 0.87 = 5.22\,W \quad (20)$$

$$P_{DISS\_LOAD} = \left(\frac{1}{6}\right) \times \left(\frac{(12 \times 12)}{12}\right) = 2.00\,W \quad (21)$$

$$P_{STARTUP} = (5.22 + 2.00) = 7.22\,W \quad (22)$$

The power dissipated is well below the shaded area of the power dissipation graph. The following table illustrates the acceptability for different $C_{dVdT}$ capacitances.

| Capacitance $C_{dVdT}$ (nF) | 0.10 | 0.47 | 3.30 | 27.0 |
|---|---|---|---|---|
| Charging Time $T_{dvdt}$ (ms) | 2.0 | 6.5 | 40.5 | 325 |
| Power Dissipation (W) | 18.84 | 7.22 | 2.84 | 2.10 |
| Limits | Not OK | OK | OK | Not OK |

## REVISION HISTORY

| Changes from Original (June 2013) to Revision A | Page |
|---|---|
| • Changed 从产品预览改为生产数据 | 1 |

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS2592AADRCR | NRND | Production | VSON (DRC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592AA |
| TPS2592AADRCR.A | NRND | Production | VSON (DRC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592AA |
| TPS2592AADRCT | NRND | Production | VSON (DRC) \| 10 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592AA |
| TPS2592AADRCT.A | NRND | Production | VSON (DRC) \| 10 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592AA |
| TPS2592ALDRCR | NRND | Production | VSON (DRC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592AL |
| TPS2592ALDRCR.A | NRND | Production | VSON (DRC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592AL |
| TPS2592ALDRCT | NRND | Production | VSON (DRC) \| 10 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592AL |
| TPS2592ALDRCT.A | NRND | Production | VSON (DRC) \| 10 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592AL |
| TPS2592BADRCR | NRND | Production | VSON (DRC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592BA |
| TPS2592BADRCR.A | NRND | Production | VSON (DRC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592BA |
| TPS2592BADRCT | NRND | Production | VSON (DRC) \| 10 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592BA |
| TPS2592BADRCT.A | NRND | Production | VSON (DRC) \| 10 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592BA |
| TPS2592BLDRCR | NRND | Production | VSON (DRC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592BL |
| TPS2592BLDRCR.A | NRND | Production | VSON (DRC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592BL |
| TPS2592BLDRCT | NRND | Production | VSON (DRC) \| 10 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592BL |
| TPS2592BLDRCT.A | NRND | Production | VSON (DRC) \| 10 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2592BL |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

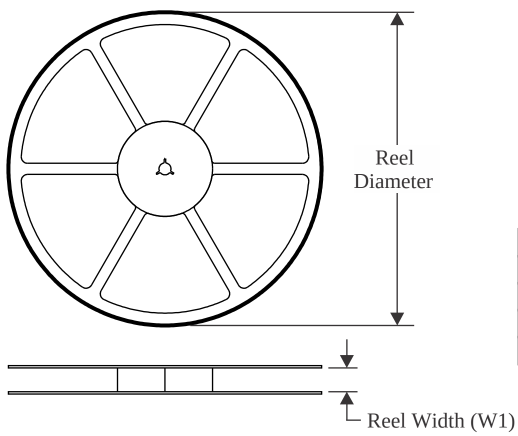
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

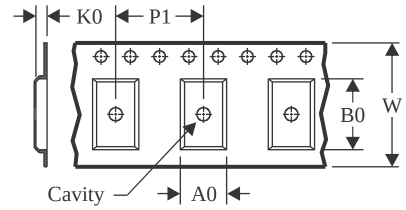
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

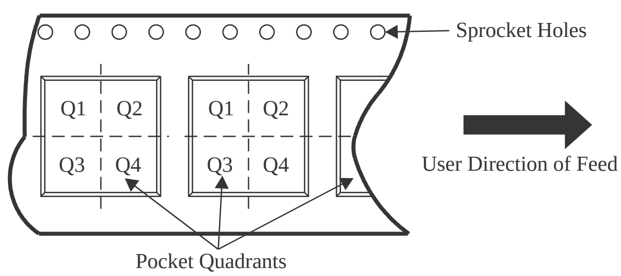



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

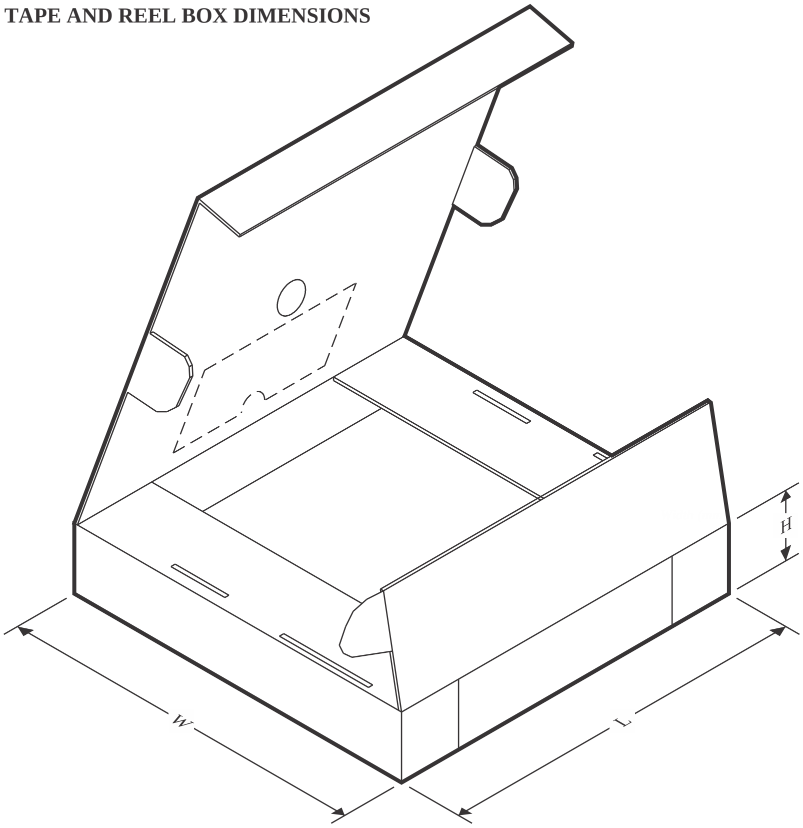
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2592AADRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS2592AADRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS2592ALDRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS2592ALDRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS2592BADRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS2592BADRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS2592BLDRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS2592BLDRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS2592AADRCR | VSON | DRC | 10 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS2592AADRCT | VSON | DRC | 10 | 250 | 210.0 | 185.0 | 35.0 |
| TPS2592ALDRCR | VSON | DRC | 10 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS2592ALDRCT | VSON | DRC | 10 | 250 | 210.0 | 185.0 | 35.0 |
| TPS2592BADRCR | VSON | DRC | 10 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS2592BADRCT | VSON | DRC | 10 | 250 | 210.0 | 185.0 | 35.0 |
| TPS2592BLDRCR | VSON | DRC | 10 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS2592BLDRCT | VSON | DRC | 10 | 250 | 182.0 | 182.0 | 20.0 |

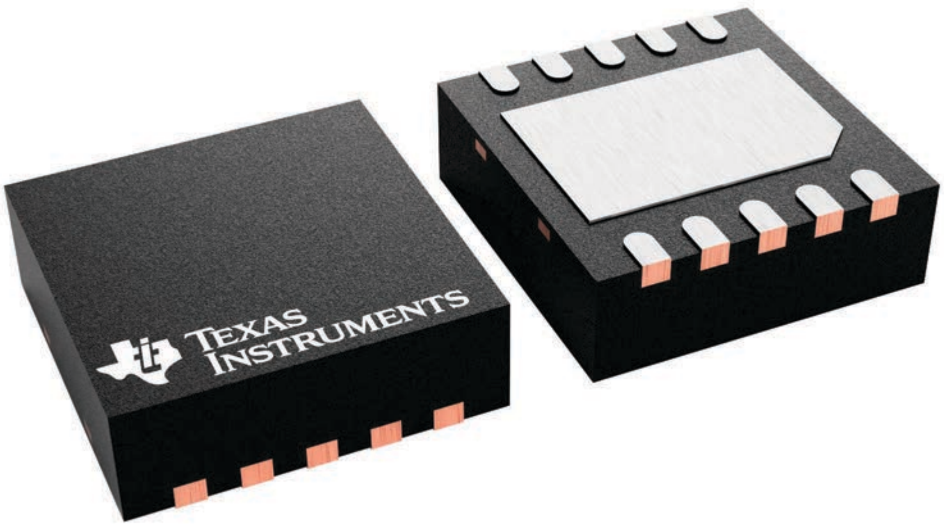
# DRC 10

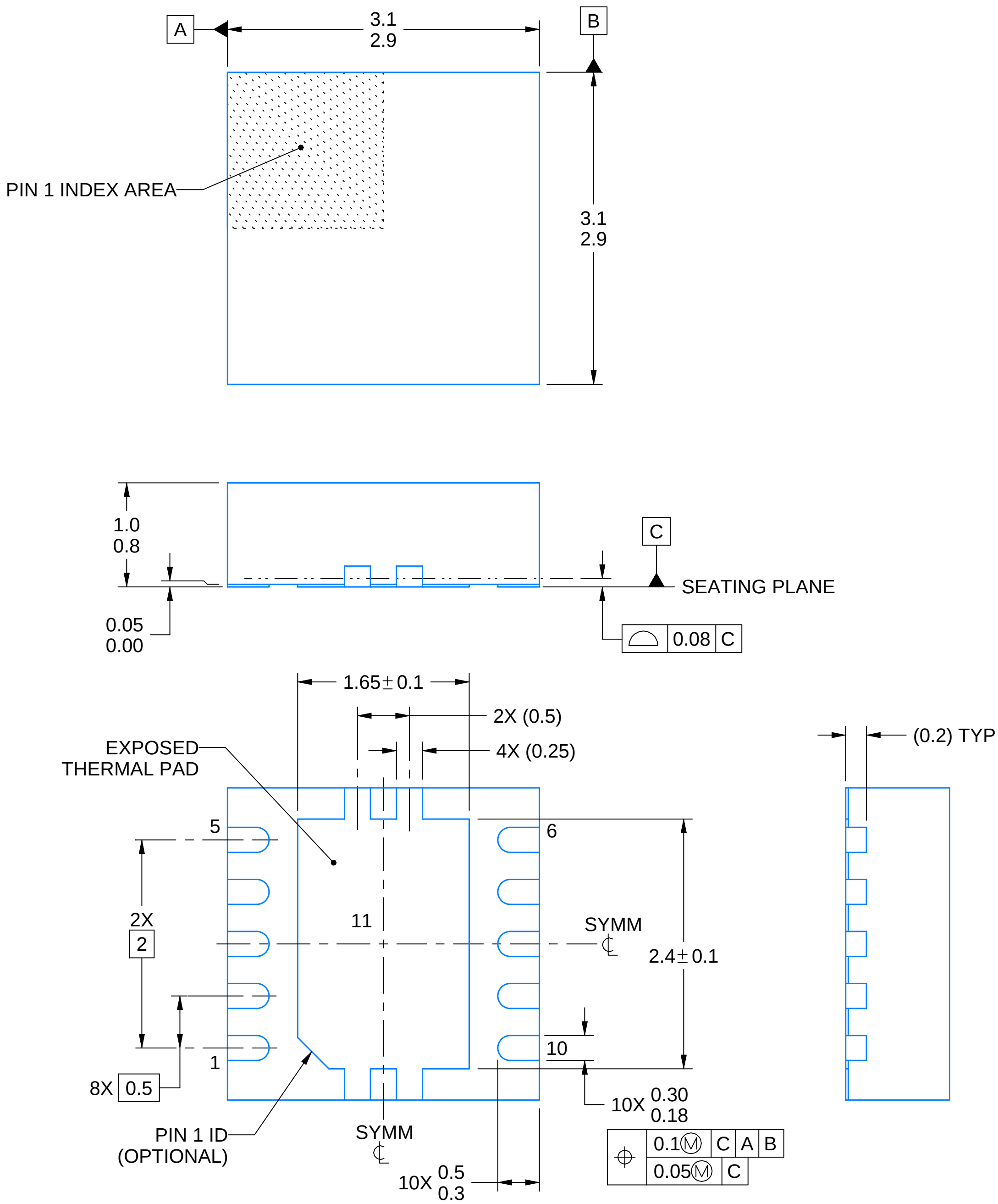
**VSON - 1 mm max height**

**3 x 3, 0.5 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD

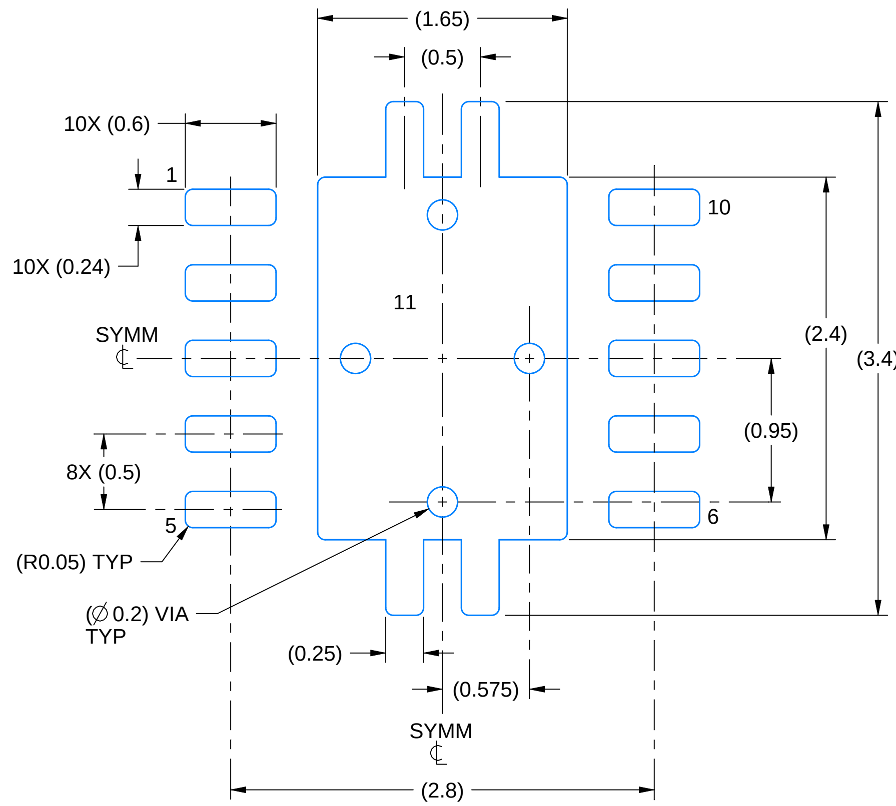
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



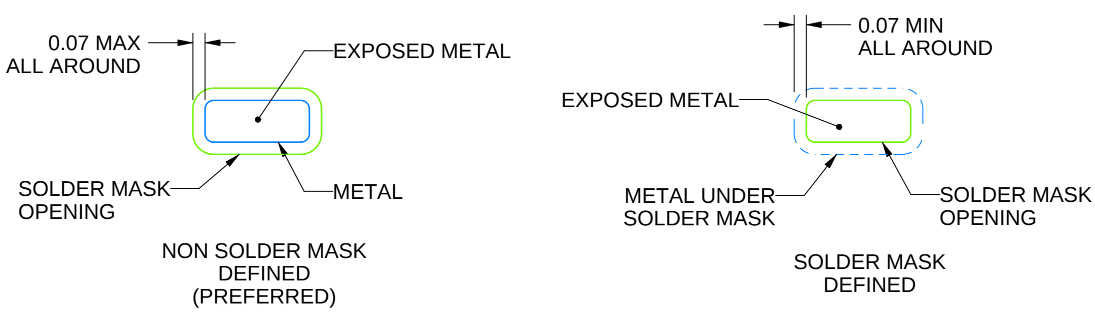



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X




SOLDER MASK DETAILS

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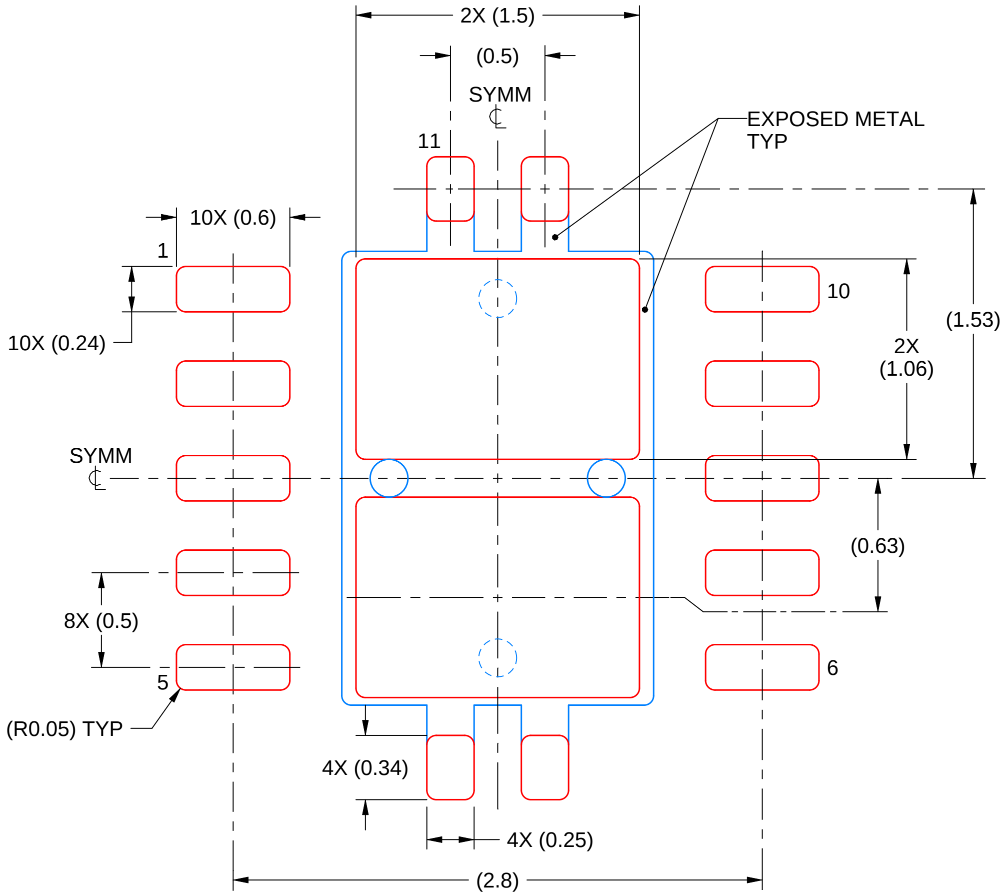
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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