

## TPS255xD 高精度可调式限流配电开关

### 1 特性

- 最大负载电流可达 1.5A
- 1.7A 电流下的电流限制精度为  $\pm 6\%$  (典型值)
- 满足 USB 限流要求
- 与 TPS2550/51 向后兼容
- 可调电流限制值, 75mA-1700mA (典型值)
- 恒流 (TPS2552D 和 TPS2553D)
- TPS2552D (支持低电流) 和 TPS2553D (支持高电流)
- 快速过流响应 -  $2\mu\text{s}$  (典型值)
- 85m $\Omega$  高侧金属氧化物半导体场效应晶体管 (MOSFET) (DBV 封装)
- 反向输入-输出电压保护
- 工作范围: 2.7V 至 6.5V
- 内置软启动
- 15kV ESD 保护, 符合 IEC 61000-4-2 标准 (带外部电容)
- UL 列表 - 文件号 E169910 和 NEMKO IEC60950-1-am1 ed2.0
- 请见 [TI 开关系列产品](#)

### 2 应用

- USB 端口/集线器
- 数字电视
- 机顶盒
- 网络语音 (VOIP) 电话

### 3 说明

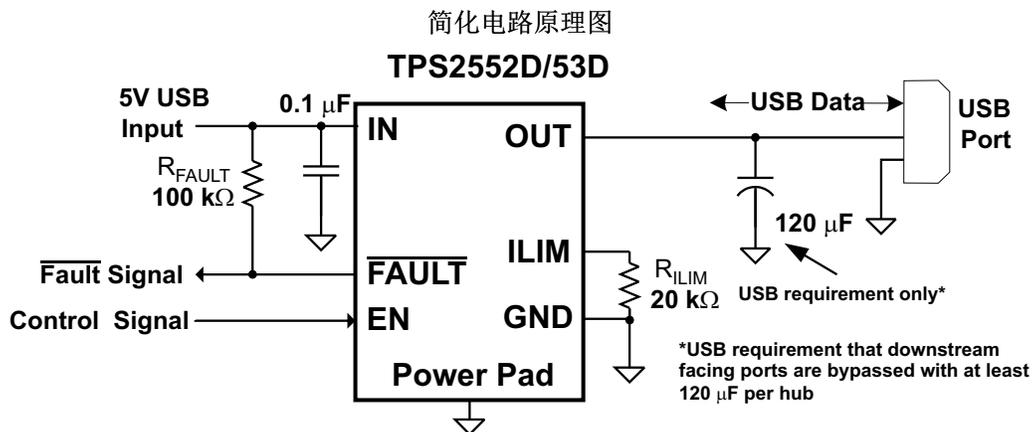
TPS2552D 和 TPS2553D 配电开关专门用于电流限制精度有要求或者会遇到重电容负载和短路的应用, 并提供高达 1.5A 的持续负载电流。这些器件借助一个外部电阻器提供一个 75mA 至 1.7A (典型值) 间的可编程电流限制阈值。在更高电流限制设置上可实现严格至  $\pm 6\%$  的电流限制精度。对电源开关的上升和下降次数进行控制以大大降低接通/切断期间的电流冲击。

当输出负载超过电流限制阈值时, TPS2552D/3D 器件会通过使用恒流模式将输出电流限制到安全水平。当输出电压被驱动至高于输入电压时, 内部反向电压比较器将禁用电源开关以保护此开关输入端的器件。在过流和反向电压情况下, FAULT 输出被置为低电平。

#### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPS2552D	SOT-23 (6)	2.90mm x 1.60mm
TPS2553D	SOT-23 (6)	2.90mm x 1.60mm

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。



## 目录

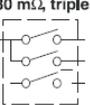
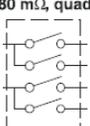
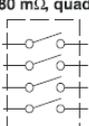
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## 4 修订历史记录

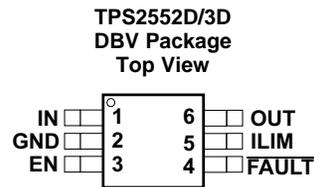
注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	注释
2016 年 9 月	*	最初发布版本

## 5 Device Comparison Table

GENERAL SWITCH CATALOG						
33 mΩ, single	80 mΩ, single	80 mΩ, dual	80 mΩ, dual	80 mΩ, triple	80 mΩ, quad	80 mΩ, quad
						
TPS201xA 0.2 A - 2 A TPS202x 0.2 A - 2 A TPS203x 0.2 A - 2 A	TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A	TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA

## 6 Pin Configuration and Functions



EN = Active Low for the TPS2552D

EN = Active High for the TPS2553D

### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	TPS2552D	TPS2553D		
	DBV	DBV		
$\overline{\text{EN}}$	3	–	I	Enable input, logic low turns on power switch
EN	–	3	I	Enable input, logic high turns on power switch
GND	2	2		Ground connection; connect externally to PowerPAD
IN	1	1	I	Input voltage; connect a 0.1 $\mu\text{F}$ or greater ceramic capacitor from IN to GND as close to the IC as possible.
$\overline{\text{FAULT}}$	4	4	O	Active-low open-drain output, asserted during overcurrent, overtemperature, or reverse-voltage conditions.
OUT	6	6	O	Power-switch output
ILIM	5	5	O	External resistor used to set current-limit threshold; recommended $15 \text{ k}\Omega \leq R_{\text{ILIM}} \leq 232 \text{ k}\Omega$ .
PowerPAD <sup>™</sup>	–	–		Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND pin externally.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)(2)</sup>

	MIN	MAX	UNIT
Voltage range on IN, OUT, EN, ILIM, $\overline{\text{FAULT}}$	-0.3	7	V
Voltage range from IN to OUT	-7	7	V
$I_{\text{O}}$ Continuous output current	Internally Limited		
Continuous total power dissipation	See the <a href="#">Thermal Information</a>		
Continuous $\overline{\text{FAULT}}$ sink current	0	25	mA
ILIM source current	0	1	mA
$T_{\text{J}}$ Maximum junction temperature	-40	150	°C
$T_{\text{stg}}$ Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltages are referenced to GND unless otherwise noted.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{\text{(ESD)}}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500	
	IEC 61000-4-2 contact discharge <sup>(3)</sup>	±8000	
	IEC 61000-4-2 air-gap discharge <sup>(3)</sup>	±15000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- (3) Surges per EN61000-4-2. 1999 applied to output terminals of EVM. These are passing test levels, not failure threshold.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{\text{IN}}$	Input voltage, IN		2.7		6.5	V
$\overline{V_{\text{EN}}}$	Enable voltage	TPS2552D	0		6.5	V
$V_{\text{EN}}$		TPS2553D	0		6.5	
$V_{\text{EN}}$	Enable voltage		0		6.5	V
$V_{\text{IH}}$	High-level input voltage on EN		1.1			V
$V_{\text{IL}}$	Low-level input voltage on EN				0.66	
$I_{\text{OUT}}$	Continuous output current, OUT	$-40\text{ }^{\circ}\text{C} \leq T_{\text{J}} \leq 125\text{ }^{\circ}\text{C}$	0		1.2	A
		$-40\text{ }^{\circ}\text{C} \leq T_{\text{J}} \leq 105\text{ }^{\circ}\text{C}$	0		1.5	
$R_{\text{ILIM}}$	Current-limit threshold resistor range (nominal 1%) from ILIM to GND		15		232	K $\Omega$
$I_{\text{O}}$	Continuous $\overline{\text{FAULT}}$ sink current		0		10	mA
	Input de-coupling capacitance, IN to GND		0.1			$\mu\text{F}$
$T_{\text{J}}$	Operating virtual junction temperature <sup>(1)</sup>	$I_{\text{OUT}} \leq 1.2\text{ A}$	-40		125	°C
		$I_{\text{OUT}} \leq 1.5\text{ A}$	-40		105	

- (1) See "Dissipation Rating Table" and "Power Dissipation and Junction Temperature" sections for details on how to calculate maximum junction temperature for specific applications and packages.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS2552D	TPS2553D	UNIT
		DBV	DBV	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182.6	182.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	122.2	122.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.4	29.4	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	20.8	20.8	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	28.9	28.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over recommended operating conditions,  $V_{EN} = V_{IN}$ ,  $R_{FAULT} = 10\text{ k}\Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP	MAX	UNIT
<b>POWER SWITCH</b>							
$r_{DS(on)}$	Static drain-source on-state resistance	DBV package, $T_J = 25^\circ\text{C}$		85	95		m $\Omega$
		DBV package, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$				135	
		DRV package, $T_J = 25^\circ\text{C}$		100	115		
		DRV package, $-40^\circ\text{C} \leq T_J \leq 105^\circ\text{C}$				140	
		DRV package, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$				150	
$t_r$	Rise time, output	$V_{IN} = 6.5\text{ V}$	$C_L = 1\text{ }\mu\text{F}$ , $R_L = 100\text{ }\Omega$ , (see <a href="#">图 20</a> )	1.1	1.5		ms
		$V_{IN} = 2.5\text{ V}$		0.7	1		
$t_f$	Fall time, output	$V_{IN} = 6.5\text{ V}$		0.2	0.5		
		$V_{IN} = 2.5\text{ V}$		0.2	0.5		
<b>ENABLE INPUT EN OR <math>\overline{\text{EN}}</math></b>							
Enable pin turn on/off threshold				0.66		1.1	V
$I_{EN}$	Input current	$V_{EN} = 0\text{ V}$ or $6.5\text{ V}$ , $V_{EN} = 0\text{ V}$ or $6.5\text{ V}$		-0.5		0.5	$\mu\text{A}$
$t_{on}$	Turnon time	$C_L = 1\text{ }\mu\text{F}$ , $R_L = 100\text{ }\Omega$ , (see <a href="#">图 20</a> )				3	ms
$t_{off}$	Turnoff time					3	ms
<b>CURRENT LIMIT</b>							
$I_{OS}$	Current-limit threshold (Maximum DC output current $I_{OUT}$ delivered to load) and Short-circuit current, OUT connected to GND	$R_{ILIM} = 15\text{ k}\Omega$	$-40^\circ\text{C} \leq T_J \leq 105^\circ\text{C}$	1610	1700	1800	mA
			$T_J = 25^\circ\text{C}$	1215	1295	1375	
		$R_{ILIM} = 20\text{ k}\Omega$	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	1200	1295	1375	
			$T_J = 25^\circ\text{C}$	490	520	550	
		$R_{ILIM} = 49.9\text{ k}\Omega$	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	475	520	565	
			$T_J = 25^\circ\text{C}$	110	130	150	
$R_{ILIM} = 210\text{ k}\Omega$		110	130	150			
$I_{LIM}$	shorted to IN			50	75	100	
$t_{IOS}$	Response time to short circuit	$V_{IN} = 5\text{ V}$ (see <a href="#">图 21</a> )				2	$\mu\text{s}$
<b>REVERSE-VOLTAGE PROTECTION</b>							
Reverse-voltage comparator trip point ( $V_{OUT} - V_{IN}$ )				95	135	190	mV
Time from reverse-voltage condition to MOSFET turn off		$V_{IN} = 5\text{ V}$		3	5	7	ms
<b>SUPPLY CURRENT</b>							
$I_{IN\_off}$	Supply current, low-level output	$V_{IN} = 6.5\text{ V}$ , No load on OUT, $V_{EN} = 0\text{ V}$			0.1	1	$\mu\text{A}$
$I_{IN\_on}$	Supply current, high-level output	$V_{IN} = 6.5\text{ V}$ , No load on OUT		$R_{ILIM} = 20\text{ k}\Omega$	120	150	$\mu\text{A}$
				$R_{ILIM} = 210\text{ k}\Omega$	100	130	$\mu\text{A}$
$I_{REV}$	Reverse leakage current	$V_{OUT} = 6.5\text{ V}$ , $V_{IN} = 0\text{ V}$		$T_J = 25^\circ\text{C}$	0.01	1	$\mu\text{A}$
<b>UNDERVOLTAGE LOCKOUT</b>							
UVLO	Low-level input voltage, IN	$V_{IN}$ rising		2.35	2.45		V
	Hysteresis, IN	$T_J = 25^\circ\text{C}$			25		mV
<b>FAULT FLAG</b>							
$V_{OL}$	Output low voltage, $\overline{\text{FAULT}}$	$I_{FAULT} = 1\text{ mA}$				180	mV
	Off-state leakage	$V_{FAULT} = 6.5\text{ V}$				1	$\mu\text{A}$
$\overline{\text{FAULT}}$	deglitch	$\overline{\text{FAULT}}$ assertion or de-assertion due to overcurrent condition		5	7.5	10	ms
		$\overline{\text{FAULT}}$ assertion or de-assertion due to reverse-voltage condition		2	4	6	ms
<b>THERMAL SHUTDOWN</b>							
	Thermal shutdown threshold			155			$^\circ\text{C}$
	Thermal shutdown threshold in current-limit			135			$^\circ\text{C}$
	Hysteresis				10		$^\circ\text{C}$

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

## 7.6 Typical Characteristics

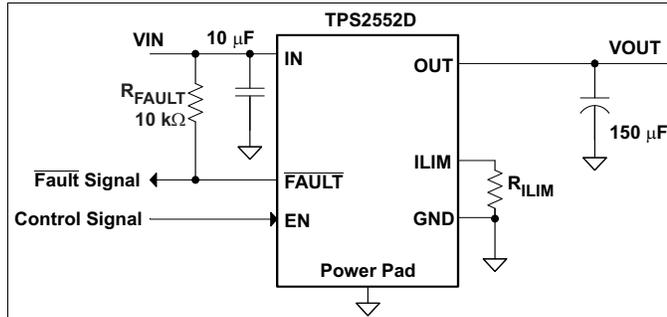


图 1. Typical Characteristics Reference Schematic

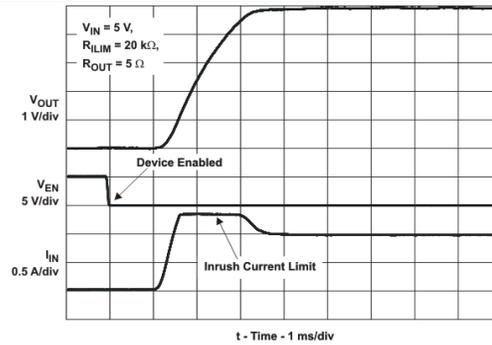


图 2. Turnon Delay and Rise Time

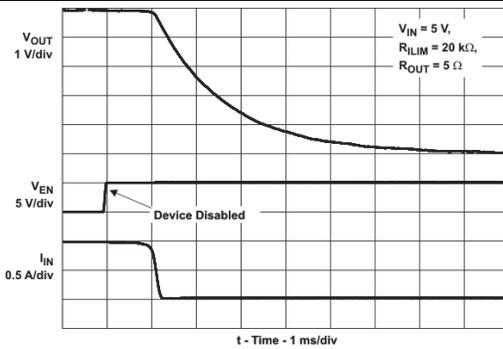


图 3. Turnoff Delay and Fall Time

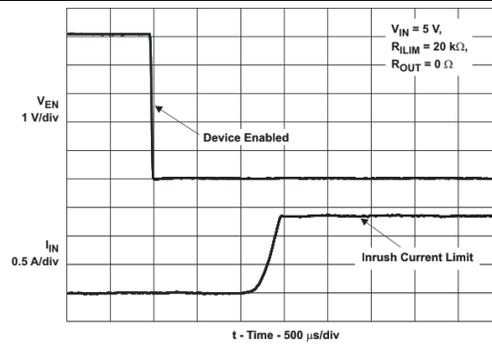


图 4. Device Enabled into Short-Circuit

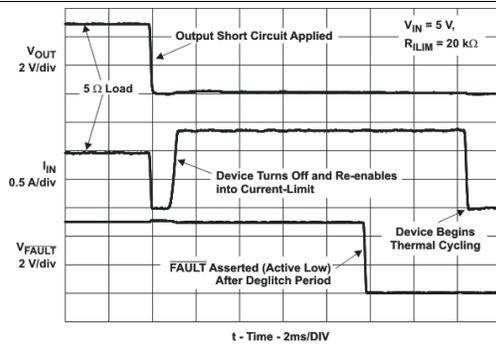


图 5. Full-Load to Short-Circuit Transient Response

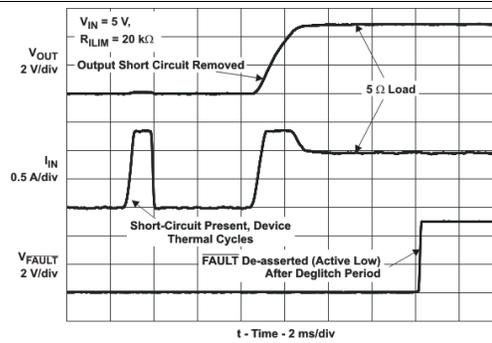


图 6. Short-Circuit to Full-Load Recovery Response

Typical Characteristics (接下页)

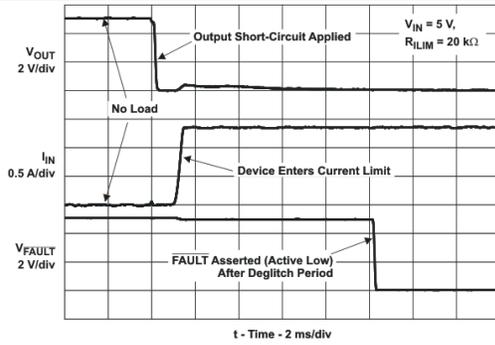


图 7. No-Load to Short-Circuit Transient Response

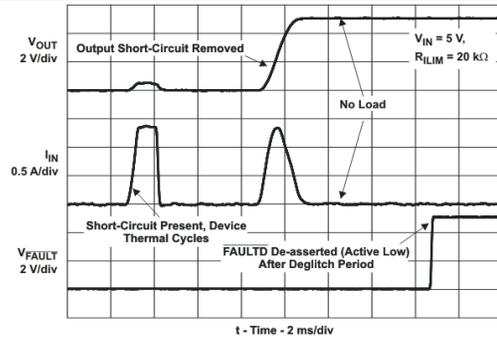


图 8. Short-Circuit to No-Load Recovery Response

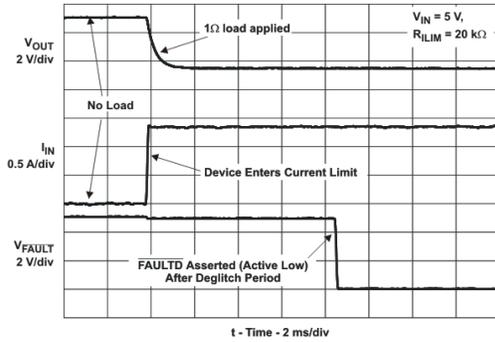


图 9. No Load to 1-Ω Transient Response

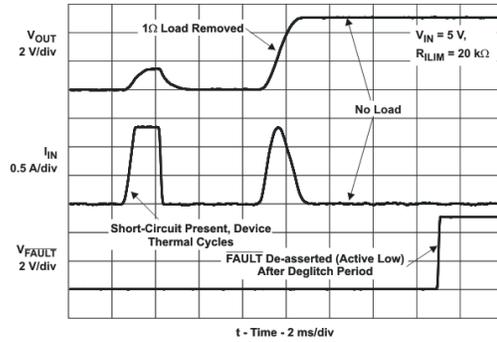


图 10. 1-Ω to No Load Transient Response

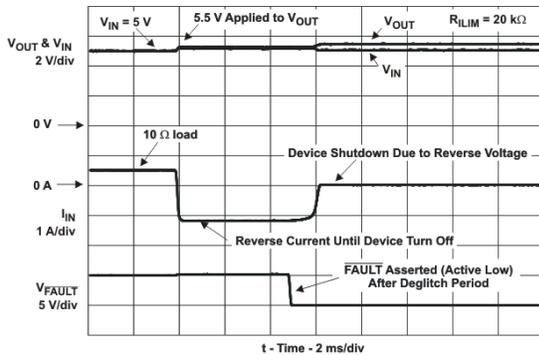


图 11. Reverse-Voltage Protection Response

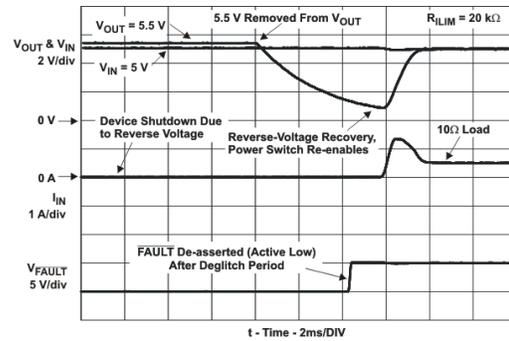


图 12. Reverse-Voltage Protection Recovery

Typical Characteristics (接下页)

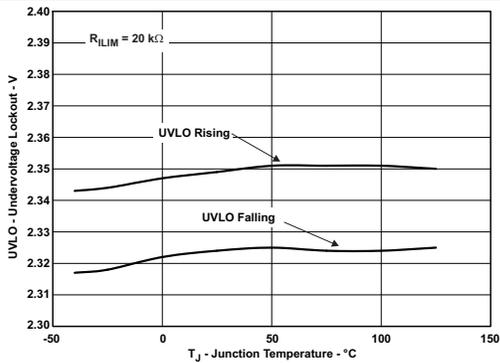


图 13. UVLO – Undervoltage Lockout – V

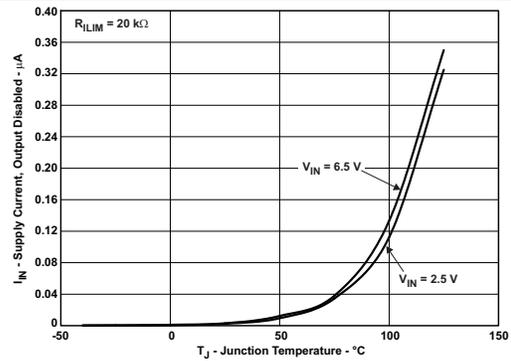


图 14.  $I_{IN}$  – Supply Current, Output Disabled –  $\mu A$

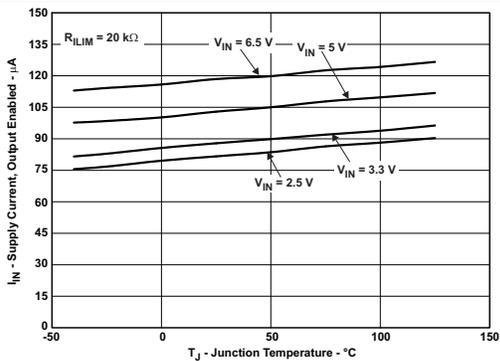


图 15.  $I_{IN}$  – Supply Current, Output Enabled –  $\mu A$

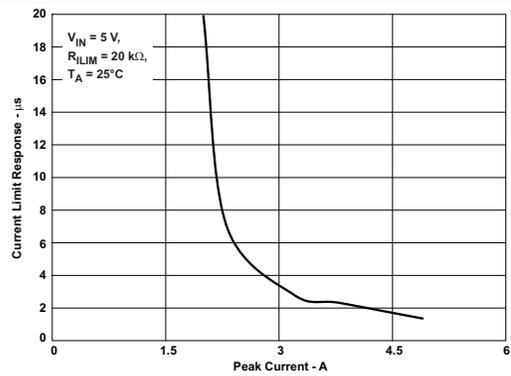


图 16. Current Limit Response –  $\mu s$

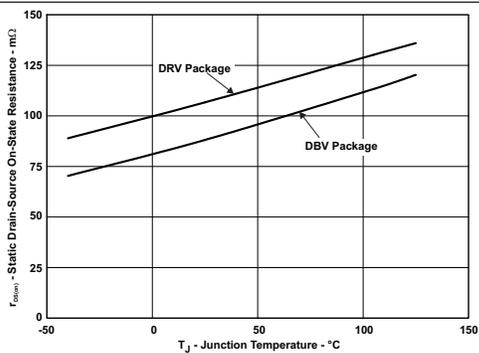


图 17. MOSFET  $r_{DS(on)}$  Vs. Junction Temperature

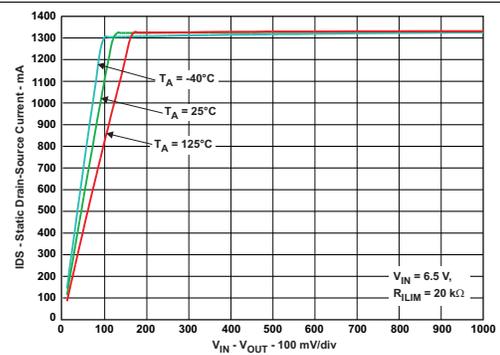


图 18. Switch Current Vs. Drain-Source Voltage Across Switch

Typical Characteristics (接下页)

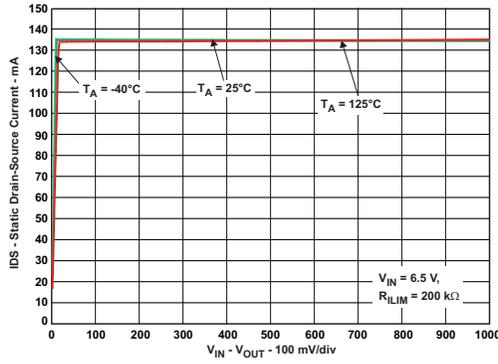


图 19. Switch Current Vs. Drain-Source Voltage Across Switch

8 Parameter Measurement Information

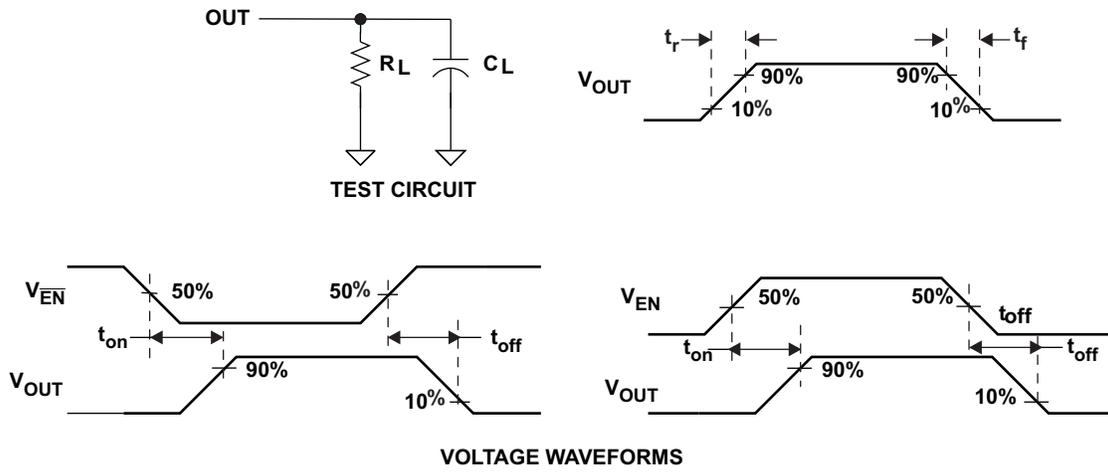


图 20. Test Circuit and Voltage Waveforms

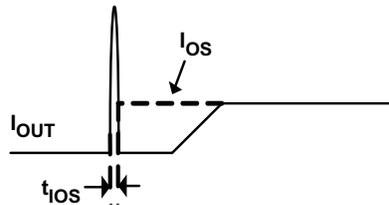


图 21. Response Time to Short Circuit Waveform

Parameter Measurement Information (接下页)

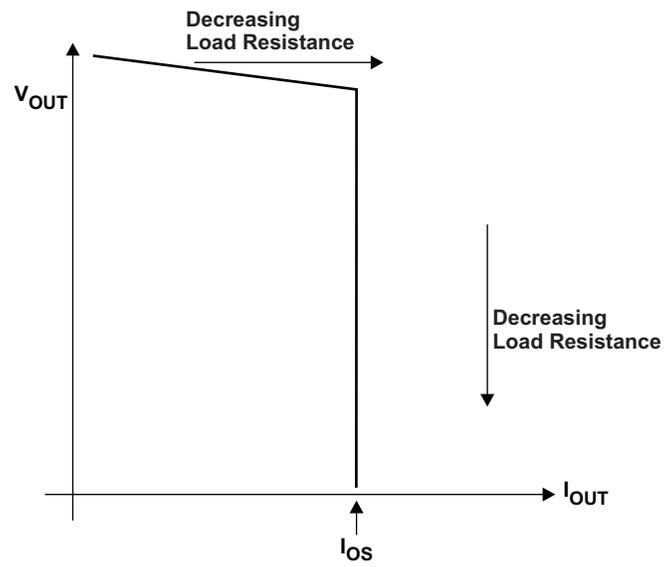


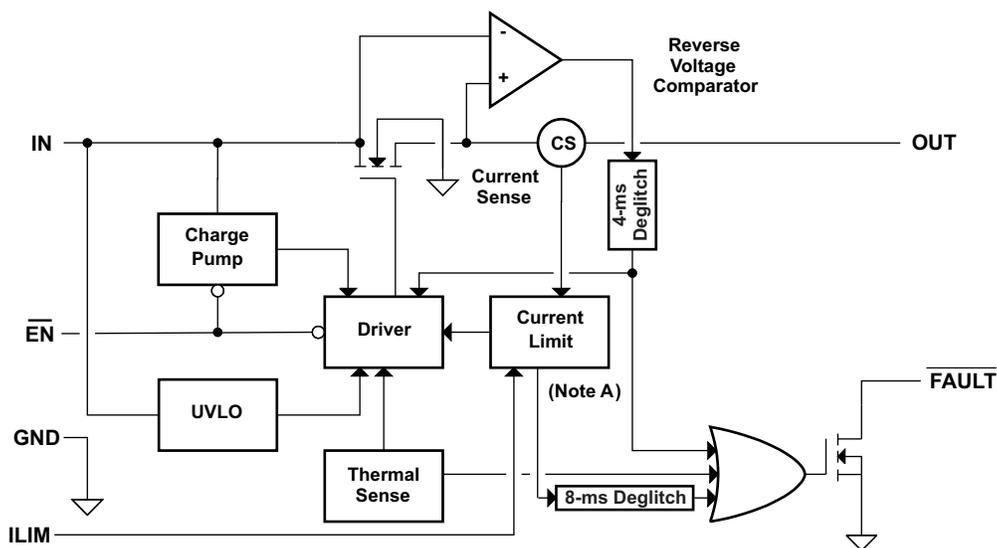
图 22. Output Voltage Vs. Current-Limit Threshold

## 9 Detailed Description

### 9.1 Overview

The TPS2552D and TPS2553D are current-limited, power-distribution switches using N-channel MOSFETs for applications where short circuits or heavy capacitive loads will be encountered and provide up to 1.5 A of continuous load current. These devices allow the user to program the current-limit threshold between 75 mA and 1.7 A (typ) via an external resistor. Additional device shutdown features include overtemperature protection and reverse-voltage protection. The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. There are two device families that handle overcurrent situations differently. The TPS255xD family enters constant-current mode when the load exceeds the current-limit threshold.

### 9.2 Functional Block Diagram



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A. TPS255x parts enter constant current mode during current limit condition

### 9.3 Feature Description

#### 9.3.1 Overcurrent Conditions

The TPS2552D and TPS2553D respond to overcurrent conditions by limiting their output current to the  $I_{OS}$  levels shown in Figure 23. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS2552D and TPS2553D ramps the output current to  $I_{OS}$ . The TPS2552D and TPS2553D devices limit the current to  $I_{OS}$  until the overload condition is removed or the device begins to thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time  $t_{IOS}$  (see Figure 21). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and limits the output current to  $I_{OS}$ . Similar to the previous case, the TPS2552D and TPS2553D devices limit the current to  $I_{OS}$  until the overload condition is removed or the device begins to thermal cycle.

## Feature Description (接下页)

The TPS2552D/53D thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (typ) while in current limit. The device remains off until the junction temperature cools 10°C (typ) and then restarts. The TPS2552D/53D cycle on/off until the overload is removed (see 图 6 and 图 8) .

### 9.3.2 Reverse-Voltage Protection

The reverse-voltage protection feature turns off the N-channel MOSFET whenever the output voltage exceeds the input voltage by 135 mV (typ) for 4-ms (typ). A reverse current of  $(V_{OUT} - V_{IN})/r_{DS(on)}$  are present when this occurs. This prevents damage to devices on the input side of the TPS2552D/53D by preventing significant current from sinking into the input capacitance. The TPS2552D/53D devices allow the N-channel MOSFET to turn on once the output voltage goes below the input voltage for the same 4-ms deglitch time. The reverse-voltage comparator also asserts the FAULT output (active-low) after 4-ms.

### 9.3.3 FAULT Response

The FAULT open-drain output is asserted (active low) during an overcurrent, overtemperature or reverse-voltage condition. The TPS2552D/53D asserts the FAULT signal until the fault condition is removed and the device resumes normal operation. The TPS2552D/53D are designed to eliminate false FAULT reporting by using an internal delay "deglitch" circuit for overcurrent (7.5-ms typ) and reverse-voltage (4-ms typ) conditions without the need for external circuitry. This ensures that FAULT is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving fault conditions. Overtemperature conditions are not deglitched and assert the FAULT signal immediately.

### 9.3.4 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

### 9.3.5 ENABLE

The logic enable controls the power switch, bias for the charge pump, driver, and other circuits to reduce the supply current. The supply current is reduced to less than 1-μA when a logic high is present on EN or when a logic low is present on EN. A logic low input on EN or a logic high input on EN enables the driver, A logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

### 9.3.6 Thermal Sense

The TPS2552D/53D self-protection features use two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The TPS2552D/53D devices operate in constant-current mode during an overcurrent conditions, which increases the voltage drop across power-switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C (min) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 10°C.

The TPS2552D/3D also have a second ambient thermal sensor. The ambient thermal sensor turns off the power-switch when the die temperature exceeds 155°C (min) regardless of whether the power switch is in current limit and will turn on the power switch after the device has cooled approximately 10°C. The TPS2552D/53D families continue to cycle off and on until the fault is removed.

The open-drain fault reporting output FAULT is asserted (active low) immediately during an overtemperature shutdown condition.

## 9.4 Device Functional Modes

There are no other functional modes.

## 9.5 Programming

### 9.5.1 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable via an external resistor. The TPS2552D/53D use an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for  $R_{ILIM}$  is  $15\text{ k}\Omega \leq R_{ILIM} \leq 232\text{ k}\Omega$  to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for  $R_{ILIM}$ . The following equations and [Figure 23](#) can be used to calculate the resulting overcurrent threshold for a given external resistor value ( $R_{ILIM}$ ). [Figure 23](#) includes current-limit tolerance due to variations caused by temperature and process. However, the equations do not account for tolerance due to external resistor variation, so it is important to account for this tolerance when selecting  $R_{ILIM}$ . The traces routing the  $R_{ILIM}$  resistor to the TPS2552D/53D should be as short as possible to reduce parasitic effects on the current-limit accuracy.

$R_{ILIM}$  can be selected to provide a current-limit threshold that occurs 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of  $R_{ILIM}$  and the maximum desired load current on the  $I_{OS(min)}$  curve and choose a value of  $R_{ILIM}$  below this value. Programming the current limit above a minimum threshold is important to ensure start up into full load or heavy capacitive loads. The resulting maximum current-limit threshold is the intersection of the selected value of  $R_{ILIM}$  and the  $I_{OS(max)}$  curve.

To design below a maximum current-limit threshold, find the intersection of  $R_{ILIM}$  and the maximum desired load current on the  $I_{OS(max)}$  curve and choose a value of  $R_{ILIM}$  above this value. Programming the current limit below a maximum threshold is important to avoid current limiting upstream power supplies causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of  $R_{ILIM}$  and the  $I_{OS(min)}$  curve.

Current-Limit Threshold Equations ( $I_{OS}$ ):

$$\begin{aligned} I_{OSmax}(\text{mA}) &= \frac{22980V}{R_{ILIM}^{0.94}\text{k}\Omega} \\ I_{OSnom}(\text{mA}) &= \frac{23950V}{R_{ILIM}^{0.977}\text{k}\Omega} \\ I_{OSmin}(\text{mA}) &= \frac{25230V}{R_{ILIM}^{1.016}\text{k}\Omega} \end{aligned} \quad (1)$$

where  $15\text{ k}\Omega \leq R_{ILIM} \leq 232\text{ k}\Omega$ .

While the maximum recommended value of  $R_{ILIM}$  is  $232\text{ k}\Omega$ , there is one additional configuration that allows for a lower current-limit threshold. The ILIM pin may be connected directly to IN to provide a  $75\text{ mA}$  (typ) current-limit threshold. Additional low-ESR ceramic capacitance may be necessary from IN to GND in this configuration to prevent unwanted noise from coupling into the sensitive ILIM circuitry.

Programming (接下页)

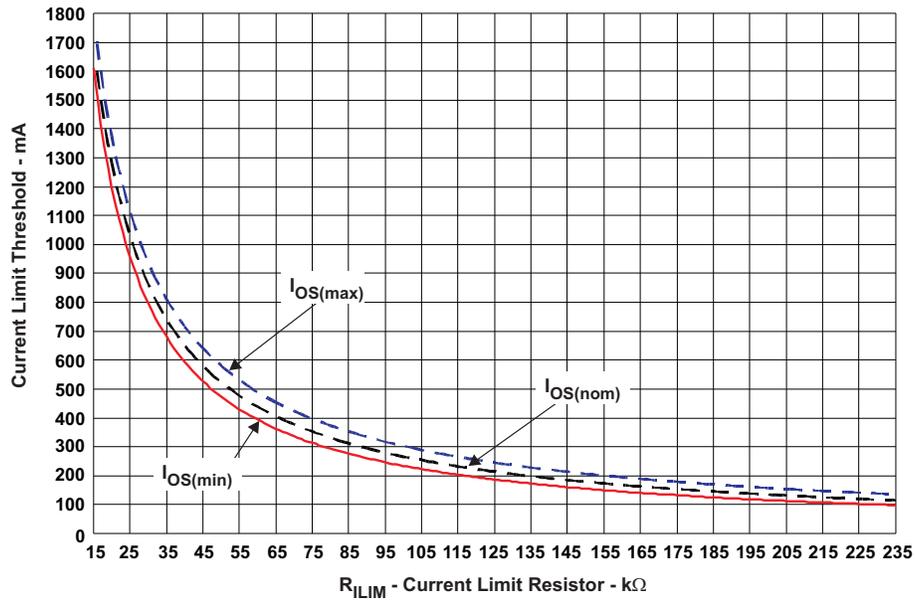


图 23. Current-Limit Threshold vs  $R_{ILIM}$

## 10 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

#### 10.1.1 Constant-Current and Impact on Output Voltage

During normal operation the N-channel MOSFET is fully enhanced, and  $V_{OUT} = V_{IN} - (I_{OUT} \times r_{DS(on)})$ . The voltage drop across the MOSFET is relatively small compared to  $V_{IN}$ , and  $V_{OUT} \approx V_{IN}$ .

The TPS2552D/53D devices limit current to the programmed current-limit threshold set to  $R_{ILIM}$  by operating the N-channel MOSFET in the linear mode. During current-limit operation, the N-channel MOSFET is no longer fully-enhanced and the resistance of the device increases. This allows the device to effectively regulate the current to the current-limit threshold. The effect of increasing the resistance of the MOSFET is that the voltage drop across the device is no longer negligible ( $V_{IN} \neq V_{OUT}$ ), and  $V_{OUT}$  decreases. The amount that  $V_{OUT}$  decreases is proportional to the magnitude of the overload condition. The expected  $V_{OUT}$  can be calculated by  $I_{OS} \times R_{LOAD}$ , where  $I_{OS}$  is the current-limit threshold and  $R_{LOAD}$  is the magnitude of the overload condition. For example, if  $I_{OS}$  is programmed to 1 A and a 1  $\Omega$  overload condition is applied, the resulting  $V_{OUT}$  is 1 V.

The TPS2552D/53D devices assert the  $\overline{FAULT}$  flag after the deglitch period and continue to regulate the current to the current-limit threshold indefinitely. In practical circuits, the power dissipation in the package will increase the die temperature above the overtemperature shutdown threshold (135°C min), and the device will turn off until the die temperature decreases by the hysteresis of the thermal shutdown circuit (10°C typ). The device will turn on and continue to thermal cycle until the overload condition is removed. The TPS2552D/53D devices resume normal operation once the overload condition is removed.

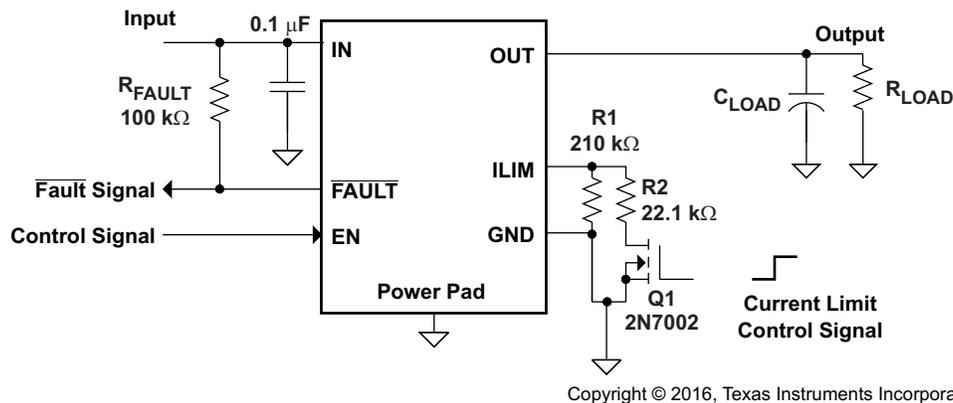
### 10.2 Typical Applications

#### 10.2.1 Two-Level Current-Limit Circuit

Some applications require different current-limit thresholds depending on external system conditions. [图 24](#) shows an implementation for an externally controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see the [Programming the Current-Limit Threshold](#) section). A logic-level input enables/disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFET/resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

### 注

ILIM should never be driven directly with an external signal.

**Typical Applications (接下页)**


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**图 24. Two-Level Current-Limit Circuit**
**10.2.1.1 Design Requirements**

 For this example, use the parameters shown in [表 1](#).

**表 1. Design Requirements**

PARAMETER	VALUE
Input voltage	5 V
Output voltage	5 V
Above a minimum current limit	1000 mA
Below a maximum current limit	500 mA

**10.2.1.2 Detailed Design Procedures**
**10.2.1.2.1 Designing Above a Minimum Current Limit**

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 1 A must be delivered to the load so that the minimum desired current-limit threshold is 1000 mA. Use the  $I_{OS}$  equations and [图 23](#) to select  $R_{ILIM}$ .

$$I_{OSmin}(\text{mA}) = 1000\text{mA}$$

$$I_{OSmin}(\text{mA}) = \frac{25230\text{V}}{R_{ILIM}^{1.016}\text{k}\Omega}$$

$$R_{ILIM}(\text{k}\Omega) = \left( \frac{25230\text{V}}{I_{OSmin}(\text{mA})} \right)^{\frac{1}{1.016}}$$

$$R_{ILIM}(\text{k}\Omega) = 24\text{k}\Omega$$

(2)

Select the closest 1% resistor less than the calculated value:  $R_{ILIM} = 23.7\text{ k}\Omega$ . This sets the minimum current-limit threshold at 1 A. Use the  $I_{OS}$  equations, [图 23](#), and the previously calculated value for  $R_{ILIM}$  to calculate the maximum resulting current-limit threshold.

$$R_{ILIM}(\text{k}\Omega) = 23.7\text{k}\Omega$$

$$I_{OSmax}(\text{mA}) = \frac{22980\text{V}}{R_{ILIM}^{0.94}\text{k}\Omega}$$

$$I_{OSmax}(\text{mA}) = \frac{22980\text{V}}{23.7^{0.94}\text{k}\Omega}$$

$$I_{OSmax}(\text{mA}) = 1172.4\text{mA}$$

(3)

The resulting maximum current-limit threshold is 1172.4 mA with a 23.7 kΩ resistor.

### 10.2.1.2.2 Designing Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that the desired upper current-limit threshold must be below 500 mA to protect an up-stream power supply. Use the  $I_{OS}$  equations and [Figure 23](#) to select  $R_{ILIM}$ .

$$I_{OSmax}(\text{mA}) = 500\text{mA}$$

$$I_{OSmax}(\text{mA}) = \frac{22980\text{V}}{R_{ILIM}^{0.94}\text{k}\Omega}$$

$$R_{ILIM}(\text{k}\Omega) = \left( \frac{22980\text{V}}{I_{OSmax}\text{mA}} \right)^{\frac{1}{0.94}}$$

$$R_{ILIM}(\text{k}\Omega) = 58.7\text{k}\Omega \tag{4}$$

Select the closest 1% resistor greater than the calculated value:  $R_{ILIM} = 59 \text{ k}\Omega$ . This sets the maximum current-limit threshold at 500 mA. Use the  $I_{OS}$  equations, [Figure 23](#), and the previously calculated value for  $R_{ILIM}$  to calculate the minimum resulting current-limit threshold.

$$R_{ILIM}(\text{k}\Omega) = 59\text{k}\Omega$$

$$I_{OSmin}(\text{mA}) = \frac{25230\text{V}}{R_{ILIM}^{1.016}\text{k}\Omega}$$

$$I_{OSmin}(\text{mA}) = \frac{25230\text{V}}{59^{1.016}\text{k}\Omega}$$

$$I_{OSmin}(\text{mA}) = 400.6\text{mA} \tag{5}$$

The resulting minimum current-limit threshold is 400.6 mA with a 59 k $\Omega$  resistor.

### 10.2.1.2.3 Accounting for Resistor Tolerance

The previous sections described the selection of  $R_{ILIM}$  given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on the TPS2552D/53D performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional  $R_{ILIM}$  resistance tolerance directly affects the current-limit threshold accuracy at a system level. The following table shows a process that accounts for worst-case resistor tolerance assuming 1% resistor values. Step one follows the selection process outlined in the application examples above. Step two determines the upper and lower resistance bounds of the selected resistor. Step three uses the upper and lower resistor bounds in the  $I_{OS}$  equations to calculate the threshold limits. It is important to use tighter tolerance resistors, e.g. 0.5% or 0.1%, when precision current limiting is desired.

表 2. Common  $R_{ILIM}$  Resistor Selections

DESIRED NOMINAL CURRENT LIMIT (mA)	IDEAL RESISTOR (kΩ)	CLOSEST 1% RESISTOR (kΩ)	RESISTOR TOLERANCE		ACTUAL LIMITS		
			1% LOW (kΩ)	1% HIGHT (kΩ)	IOS MIN (mA)	IOS NOM (mA)	IOS MAX (mA)
75		SHORT ILIM to IN			50.0	75.0	100.0
120	226.1	226	223.7	228.3	101.3	120.0	142.1
200	134.0	133	131.7	134.3	173.7	201.5	233.9
300	88.5	88.7	87.8	89.6	262.1	299.4	342.3
400	65.9	66.5	65.8	67.2	351.2	396.7	448.7
500	52.5	52.3	51.8	52.8	448.3	501.6	562.4
600	43.5	43.2	42.8	43.6	544.3	604.6	673.1
700	37.2	37.4	37.0	37.8	630.2	696.0	770.8
800	32.4	32.4	32.1	32.7	729.1	800.8	882.1
900	28.7	28.7	28.4	29.0	824.7	901.5	988.7
1000	25.8	26.1	25.8	26.4	908.3	989.1	1081.0
1100	23.4	23.2	23.0	23.4	1023.7	1109.7	1207.5
1200	21.4	21.5	21.3	21.7	1106.0	1195.4	1297.1
1300	19.7	19.6	19.4	19.8	1215.1	1308.5	1414.9
1400	18.3	18.2	18.0	18.4	1310.1	1406.7	1517.0
1500	17.0	16.9	16.7	17.1	1412.5	1512.4	1626.4
1600	16.0	15.8	15.6	16.0	1512.5	1615.2	1732.7
1700	15.0	15.0	14.9	15.2	1594.5	1699.3	1819.4

10.2.1.2.4 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1μF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise de-coupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power-supply.

Placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

10.2.1.3 Application Curves

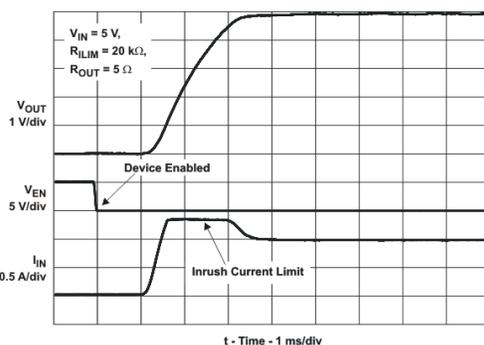


图 25. Turn on Delay and Rise Time

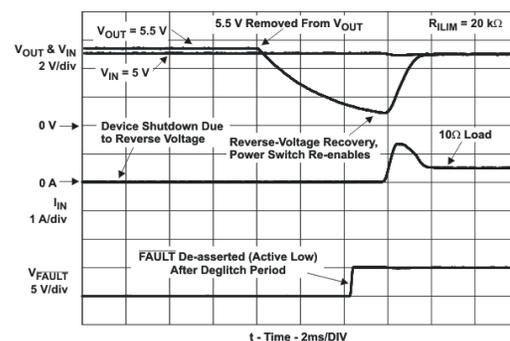


图 26. Reverse-Voltage Protection Recovery

### 10.2.2 Auto-Retry Functionality

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This *auto-retry* functionality can be implemented with an external resistor and capacitor. During a fault condition, **FAULT** pulls low disabling the part. The part is disabled when **EN** is pulled low, and **FAULT** goes high impedance allowing  $C_{RETRY}$  to begin charging. The part re-enables when the voltage on **EN** reaches the turnon threshold, and the auto-retry time is determined by the resistor/capacitor time constant. The device continues to cycle in this manner until the fault condition is removed.

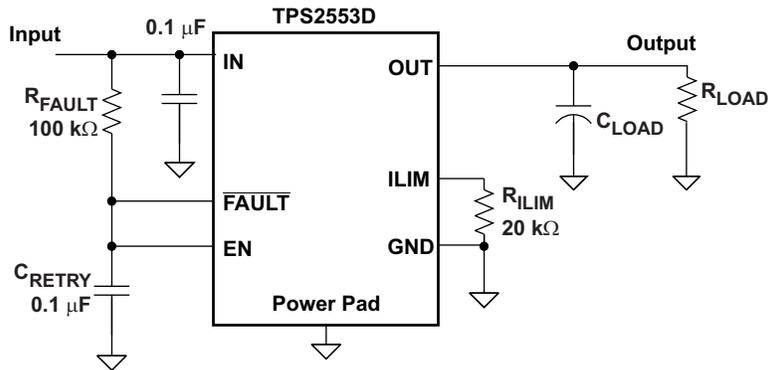


图 27. Auto-Retry Functionality

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. 图 28 shows how an external logic signal can drive **EN** through  $R_{FAULT}$  and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

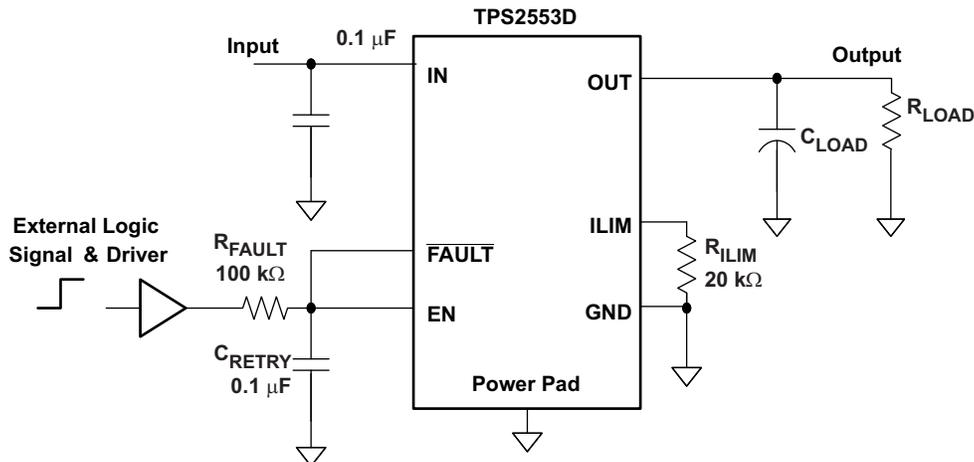


图 28. Auto-Retry Functionality With External EN Signal

#### 10.2.2.1 Design Requirements

For this example, use the parameters shown in 表 3.

表 3. Design Requirements

PARAMETER	VALUE
Input voltage	5 V
Output voltage	5 V
Current	1200 mA

### 10.2.2.2 Detailed Design Procedure

Refer to [Programming the Current-Limit Threshold](#) section for the current limit setting. For auto-retry functionality, once  $\overline{\text{FAULT}}$  asserted, EN pull low, TPS2553D is disabled,  $\overline{\text{FAULT}}$  des-asserted,  $C_{\text{RETRY}}$  is slowly charged to EN logic high via  $R_{\text{FAULT}}$ , then enable, after deglitch time,  $\overline{\text{FAULT}}$  asserted again. In the event of an over-load, TPS2553D cycles and has output average current. ON-time with output current is decided by  $\overline{\text{FAULT}}$  deglitch time. OFF-time without output current is decided by  $R_{\text{FAULT}} \times C_{\text{RETRY}}$  constant time to EN logic high and  $t_{\text{on}}$  time. Therefore, set the  $R_{\text{FAULT}} \times C_{\text{RETRY}}$  to get the desired output average current during overload.

### 10.2.3 Typical Application as USB Power Switch

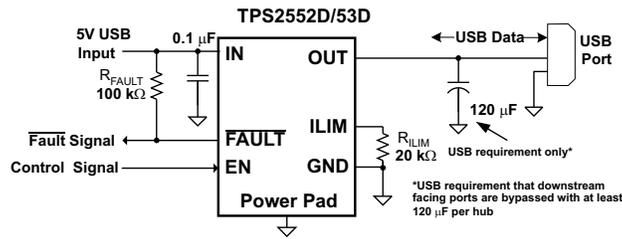


图 29. Typical Application as USB Power Switch

#### 10.2.3.1 Design Requirements

For this example, use the parameters shown in 表 4.

表 4. Design Requirements

PARAMETER	VALUE
Input voltage	5 V
Output voltage	5 V
Current	1200 mA

##### 10.2.3.1.1 USB Power-Distribution Requirements

USB can be implemented in several ways regardless of the type of USB device being developed. Several power-distribution features must be implemented.

- SPHs must:
  - Current limit downstream ports
  - Report overcurrent conditions
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2552D/53D meets each of these requirements. The integrated current limiting and overcurrent reporting is required by self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs and the input ports for bus-powered functions.

### 10.2.3.2 Detailed Design Procedure

#### 10.2.3.2.1 Universal Serial Bus (USB) Power-Distribution Requirements

One application for this device is for current limiting in universal serial bus (USB) applications. The original USB interface was a 12-Mb/s or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). As the demand for more bandwidth increased, the USB 2.0 standard was introduced increasing the maximum data rate to 480-Mb/s. The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply. The USB specification classifies two different classes of devices depending on its maximum current draw. A device classified as low-power can draw up to 100 mA as defined by the standard. A device classified as high-power can draw up to 500 mA. It is important that the minimum current-limit threshold of the current-limiting power-switch exceed the maximum current-limit draw of the intended application. The latest USB standard should always be referenced when considering the current-limit threshold.

The USB specification defines two types of devices as hubs and functions. A USB hub is a device that contains multiple ports for different USB devices to connect and can be self-powered (SPH) or bus-powered (BPH). A function is a USB device that is able to transmit or receive data or control information over the bus. A USB function can be embedded in a USB hub. A USB function can be one of three types included in the list below.

- Low-power, bus-powered function
- High-power, bus-powered function
- Self-powered function

SPHs and BPHs distribute data and power to downstream functions. The TPS2552D/53D have higher current capabilities than required for a single USB port allowing it to power multiple downstream ports.

## 11 Power Supply Recommendations

### 11.1 Self-Powered and Bus-Powered Hubs

A SPH has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V to 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

A BPH obtains all power from an upstream port and often contains an embedded function. It must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This is accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

### 11.2 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 μF at power up, the device must implement inrush current limiting.

### 11.3 Power Dissipation and Junction Temperature

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the  $r_{DS(on)}$  of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read  $r_{DS(on)}$  from the typical characteristics graph. Using this value, the power dissipation can be calculated using [公式 6](#).

$$P_D = r_{DS(on)} \times I_{OUT}^2$$

where

- $P_D$  = Total power dissipation (W)
- $r_{DS(on)}$  = Power switch on-resistance (Ω)
- $I_{OUT}$  = Maximum current-limit threshold (A)
- This step calculates the total power dissipation of the N-channel MOSFET. (6)

Finally, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A$$

where

- $T_A$  = Ambient temperature (°C)
- $\theta_{JA}$  = Thermal resistance (°C/W)
- $P_D$  = Total power dissipation (W) (7)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined"  $r_{DS(on)}$  from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance  $\theta_{JA}$ , and thermal resistance is highly dependent on the individual package and board layout. The [Thermal Information Table](#) provides example thermal resistances for specific packages and board layouts.

## 12 Layout

### 12.1 Layout Guidelines

- TI recommends placing the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace.
- TI recommends placing a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin is recommended when large transient currents are expected on the output.
- The traces routing the RILIM resistor to the device should be as short as possible to reduce parasitic effects on the current limit accuracy.
- The PowerPAD should be directly connected to PCB ground plane using wide and short copper trace.

### 12.2 Layout Example

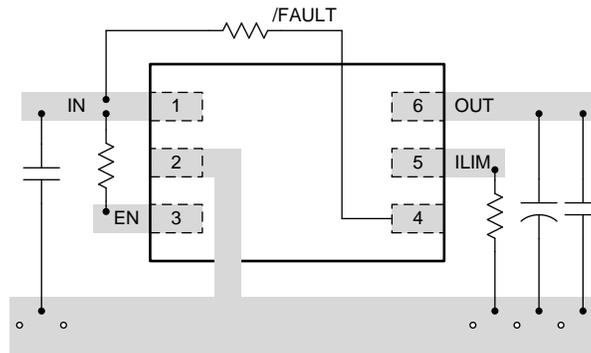


图 30. Layout Recommendation

## 13 器件和文档支持

### 13.1 器件支持

有关 TI 开关产品组合的信息，[请访问此处](#)。

### 13.2 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，以及样片或购买的快速访问。

表 5. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS2552D	<a href="#">请单击此处</a>				
TPS2553D	<a href="#">请单击此处</a>				

### 13.3 接收文档更新通知

如需接收文档更新通知，请访问 [www.ti.com.cn](http://www.ti.com.cn) 网站上的器件产品文件夹。点击右上角的**提醒我 (Alert me)** 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

### 13.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.5 商标

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### 13.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS2552DDBVR</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15IL
TPS2552DDBVR.B	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15IL
<a href="#">TPS2552DDBVT</a>	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15IL
TPS2552DDBVT.B	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15IL
<a href="#">TPS2553DDBVR</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15JL
TPS2553DDBVR.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15JL
TPS2553DDBVR.B	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15JL
TPS2553DDBVRG4	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15JL
TPS2553DDBVRG4.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15JL
TPS2553DDBVRG4.B	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15JL
<a href="#">TPS2553DDBVT</a>	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15JL
TPS2553DDBVT.A	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15JL
TPS2553DDBVT.B	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15JL

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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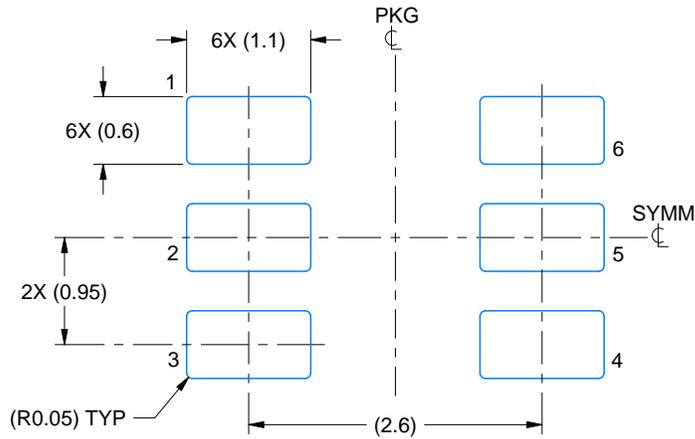


# EXAMPLE BOARD LAYOUT

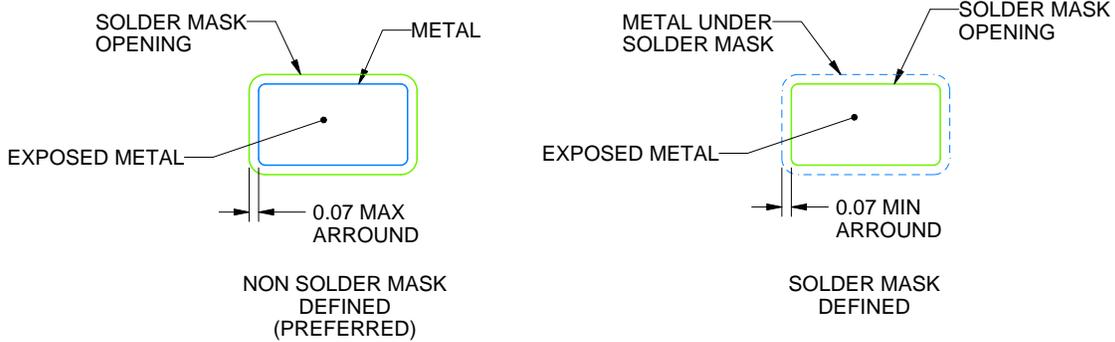
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

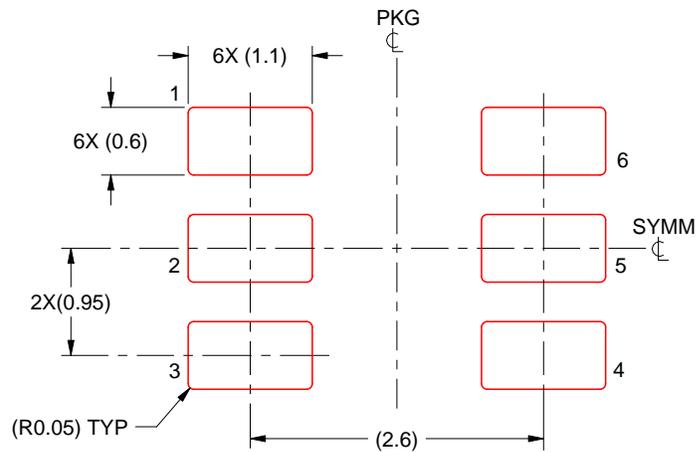
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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