

TPS254900-Q1 具有 V_{BATT} 短路保护的汽车用 USB 主机充电器

1 特性

- 具有符合 AEC-Q100 标准的下列结果：
 - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H2
 - 器件组件充电模式 (CDM) ESD 分类等级 C5
- 4.5V 至 6.5V 的输入工作电压范围
- 集成 $45m\Omega$ (典型值) 高侧金属氧化物半导体场效应晶体管 (MOSFET)
- 最大连续开关电流达 3A
- 连接器上的电缆补偿精度 $V_{BUS} \pm 5\%$
- 支持 USB BC 1.2 充电下行端口 (CDP) 和标准下行端口 (SDP) 模式
- OUT、DP_IN 和 DM_IN 引脚上具备电池短路保护
- DP_IN 和 DM_IN 上的保护等级符合 IEC 61000-4-2 标准
 - $\pm 8kV$ 接触放电和 $\pm 15kV$ 空气放电
- 20 引脚 4mm x 3mm 四方扁平无引线 (QFN) 封装

2 应用范围

- 汽车 USB 充电端口 (主机和集线器)
- 汽车类 USB 保护

3 说明

TPS254900-Q1 器件是一款具有电池短路保护功能的 USB 充电端口控制器和电源开关。该功能为 OUT、DM_IN 和 DP_IN 引脚提供保护。这三个引脚可耐受高达 18V 的电压。当发生电池短路时，内部 MOSFET 迅速关断。迅速关断功能对于保护上行 DC-DC 转换器、处理器或集线器数据线路来说非常重要。

TPS254900-Q1 $45m\Omega$ 电源开关具有两个可选的可调节电流限值，可通过在相邻端口承载高负载时切换至较低电流限值来支持端口电源管理。对于具有多个端口且上行电源容量有限的系统而言，这一功能非常重要。

TPS254900-Q1 具有一个能够控制上行电源的电流感测输出，即使在充电电流过大时也能在 USB 端口保持 5V 的电压。该功能对于 USB 电缆较长的系统而言至关重要，因为在对便携式设备进行快速充电的过程中会产生大幅压降。

凭借电流监视器，系统能够通过监视 IMON 电压来实时监视负载电流。电流监视器非常有用，可用于端口电源动态管理。

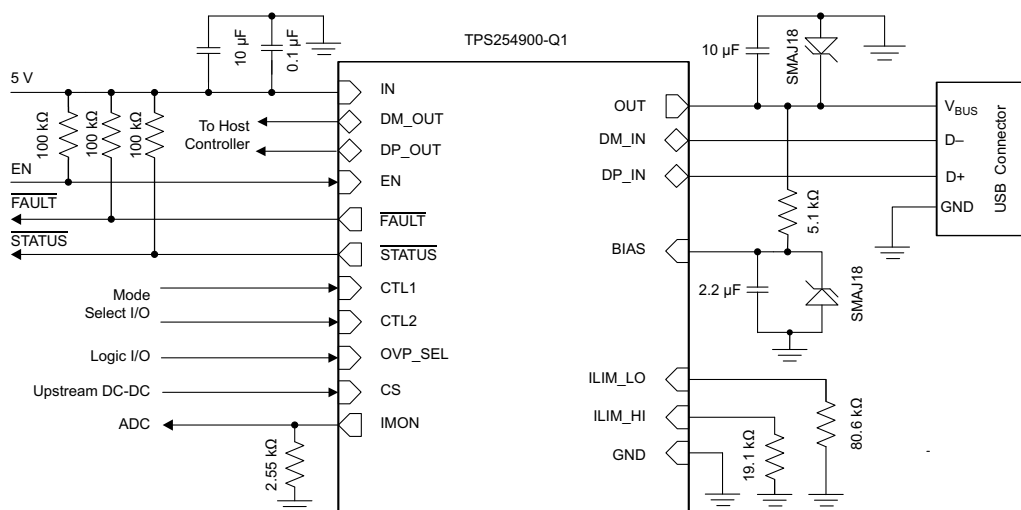
TPS254900-Q1 器件还为 DP_IN 和 DM_IN 引脚提供了符合 IEC 61000-4-2 标准的 4 级 ESD 保护功能。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸 (标称值) |
|--------------|-----------|-----------------|
| TPS254900-Q1 | WQFN (20) | 4.00mm x 3.00mm |

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

原理图



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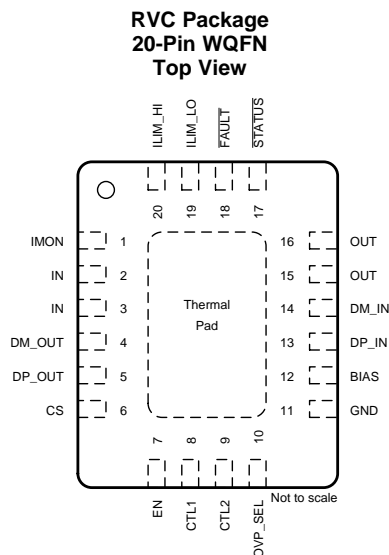
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4 修订历史记录

| Changes from Original (September 2016) to Revision A | Page |
|--|------|
| <ul style="list-style-type: none"> 已将数据表状态由“产品预览”改为“量产数据” | 1 |

5 Pin Configuration and Functions



Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-------------|-------|---------------------|---|
| NAME | NO. | | |
| BIAS | 12 | PWR | Used for IEC protection. Typically, connect a 2.2-μF capacitor and a transient-voltage suppressor (TVS) to ground and 5.1 kΩ to OUT. |
| CS | 6 | O | Linear cable compensation current. Connect to divider resistor of front-end dc-dc converter. |
| CTL1 | 8 | I | Logic-level control input for controlling the charging mode and the signal switches; see the Device Truth Table (TT) . |
| CTL2 | 9 | I | Logic-level control input for controlling the charging mode and the signal switches; see the Device Truth Table (TT) . |
| DM_IN | 14 | I/O | D– data line to downstream connector |
| DM_OUT | 4 | I/O | D– data line to upstream USB host controller |
| DP_IN | 13 | I/O | D+ data line to downstream connector |
| DP_OUT | 5 | I/O | D+ data line to upstream USB host controller |
| EN | 7 | I | Logic-level control input for turning the power and signal switches on or off. When EN is low, the device is disabled, and the signal and power switches are OFF. |
| FAULT | 18 | O | Active-low, open-drain output, asserted during overtemperature, overcurrent, and overvoltage conditions. |
| GND | 11 | — | Ground connection; should be connected externally to the thermal pad. |
| ILIM_HI | 20 | I | External resistor used to set the high current-limit threshold. |
| ILIM_LO | 19 | I | External resistor used to set the low current-limit threshold and the load-detection current threshold. |
| IMON | 1 | O | This pin sources a scaled-down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage; used as an analog current monitor. |
| IN | 2,3 | PWR | Input supply voltage; connect a 0.1-μF or greater ceramic capacitor from IN to GND as close to the IC as possible. |
| OUT | 15,16 | PWR | Power-switch output |
| OVP_SEL | 10 | I | Logic-level control input for choosing the OUT overvoltage threshold. When OVP_SEL is low, V _(OV_OUT_LOW) is active. When OVP_SEL is high, V _(OV_OUT_HIGH) is active. |
| STATUS | 17 | O | Active-low open-drain output, asserted in load-detect conditions |
| Thermal pad | — | — | Thermal pad on the bottom of the package |

(1) I = Input, O = Output, I/O = Input and output, PWR = Power

6 Specifications

6.1 Absolute Maximum Ratings

Voltages are with respect to GND unless otherwise noted⁽¹⁾

| | | MIN | MAX | UNIT | |
|--------------------|---|--|--------------------|--------------------|----|
| Voltage range | CS, CTL1, CTL2, EN, $\overline{\text{FAULT}}$, ILIM_HI, ILIM_LO, IN, IMON, OVP_SEL, $\overline{\text{STATUS}}$ | −0.3 | 7 | V | |
| | DM_OUT, DP_OUT | −0.3 | 5.7 | | |
| | BIAS, DM_IN, DP_IN, OUT | −0.3 | 18 | | |
| Continuous current | DM_IN to DM_OUT or DP_IN to DP_OUT | −100 | 100 | mA | |
| | OUT | Internally limited | | | |
| I _{SRC} | Continuous output source current | ILIM_HI, ILIM_LO, IMON | | A | |
| I _{SNK} | Continuous output sink current | $\overline{\text{FAULT}}$, $\overline{\text{STATUS}}$ | | 25 | mA |
| | | CS | | Internally limited | A |
| T _J | Operating junction temperature | −40 | Internally limited | °C | |
| T _{stg} | Storage temperature | −65 | 150 | °C | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|---|-----------------------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2 000 ⁽²⁾ |
| | | Charged-device model (CDM), per AEC Q100-011 | ±750 ⁽³⁾ |
| | | IEC 61000-4-2 contact discharge, DP_IN and DM_IN ⁽⁴⁾ | ±8 000 |
| | | IEC 61000-4-2 air discharge, DP_IN and DM_IN ⁽⁴⁾ | ±15 000 |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The passing level per AEC-Q100 Classification H2.
(3) The passing level per AEC-Q100 Classification C5
(4) Surges per IEC 61000-4-2, level 4, 1999 applied from DP_IN and DM_IN to output ground of the TPS254900Q1EVM-817 (SLUUBIO) evaluation module.

6.3 Recommended Operating Conditions

Voltages are with respect to GND unless otherwise noted.

| | | | MIN | NOM | MAX | UNIT |
|------------------------|--------------------------------|-------------------------------------|------|-----|------|------|
| V _(IN) | Supply voltage | IN | 4.5 | | 6.5 | V |
| | Input voltage | CTL1, CTL2, EN, OVP_SEL | 0 | | 6.5 | V |
| | | DM_IN, DM_OUT, DP_IN, DP_OUT | 0 | | 3.6 | V |
| I _(OUT) | Output continuous current | OUT (–40°C ≤ T _A ≤ 85°C) | | | 3 | A |
| | | DM_IN to DM_OUT or DP_IN to DP_OUT | –30 | | 30 | mA |
| | Continuous output sink current | $\overline{\text{FAULT}}$, STATUS | | | 10 | mA |
| R _(ILIM_xx) | Current-limit-set resistors | | 14.3 | | 1000 | kΩ |
| T _J | Operating junction temperature | | –40 | | 125 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS254900-Q1 | UNIT |
|-------------------------------|--|--------------|------|
| | | RVC (WQFN) | |
| | | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 37.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 39.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 11.9 | °C/W |
| ψ_{JT} | Junction-to-top characterization parameter | 0.5 | °C/W |
| ψ_{JB} | Junction-to-board characterization parameter | 11.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Unless otherwise noted, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ and $4.5\text{ V} \leq V_{(IN)} \leq 6.5\text{ V}$, $V_{(EN)} = V_{(CTL1)} = V_{(CTL2)} = V_{(IN)}$, $R_{(FAULT)} = R_{(STATUS)} = 10\text{ k}\Omega$, $R_{(IMON)} = 2.55\text{ k}\Omega$, $R_{(ILIM_HI)} = 19.1\text{ k}\Omega$, $R_{(ILIM_LO)} = 80.6\text{ k}\Omega$. Positive currents are into pins. Typical values are at 25°C . All voltages are with respect to GND.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|---|--|------|------|------|------|
| OUT – POWER SWITCH | | | | | | |
| r _{DS(on)} | On-resistance ⁽¹⁾ | T _J = 25°C | | 45 | 55 | mΩ |
| | | −40°C ≤ T _J ≤ 85°C | | 45 | 69 | |
| | | −40°C ≤ T _J ≤ 125°C | | 45 | 77 | |
| I _{lkg} | Reverse leakage current | V _{OUT} = 6.5 V, V _{IN} = V _{EN} = 0 V, −40°C ≤ T _J ≤ 85°C, measure I _{I(IN)} | | 0.01 | 2 | μA |
| OUT – DISCHARGE | | | | | | |
| R _(DCHG) | Discharge resistance (mode change) | | 400 | 500 | 630 | Ω |
| CTL1, CTL2, EN, OVP_SEL INPUTS | | | | | | |
| | Input pin rising logic threshold voltage | | 1 | 1.35 | 2 | V |
| | Input pin falling logic threshold voltage | | 0.85 | 1.15 | 1.65 | V |
| | Hysteresis ⁽²⁾ | | | 200 | | mV |
| | Input current | Pin voltage = 0 V or 6.5 V | −1 | | 1 | μA |
| CURRENT LIMIT | | | | | | |
| I _{OS} | OUT short-circuit current limit | R _(ILIM_LO) = 210 kΩ | 190 | 240 | 290 | mA |
| | | R _(ILIM_LO) = 80.6 kΩ | 555 | 620 | 680 | |
| | | R _(ILIM_LO) = 21.5 kΩ | 2145 | 2300 | 2460 | |
| | | R _(ILIM_LO) = 19.1 kΩ | 2420 | 2590 | 2760 | |
| | | R _(ILIM_HI) = 18.2 kΩ | 2545 | 2720 | 2895 | |
| | | R _(ILIM_HI) = 14.3 kΩ | 3240 | 3455 | 3670 | |
| | | R _(ILIM_HI) shorted to GND | 5000 | 6500 | 8000 | |
| SUPPLY CURRENT | | | | | | |
| I _(IN_OFF) | Disabled IN supply current | V _(EN) = 0 V, V _(OUT) = 0 V, −40°C ≤ T _J ≤ 85°C, no 5.1-kΩ resistor (open) between BIAS and OUT | | 0.1 | 5 | μA |
| I _(IN_ON) | Enabled IN supply current | SDP mode (CTL1, CTL2 = 0, 1) | | 170 | 250 | μA |
| | | CDP mode (CTL1, CTL2 = 1, 1) | | 200 | 280 | |
| | | Client mode (CTL1, CTL2 = 0, 0) | | 120 | 210 | |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.

(2) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

Electrical Characteristics (continued)

Unless otherwise noted, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ and $4.5\text{ V} \leq V_{(\text{IN})} \leq 6.5\text{ V}$, $V_{(\text{EN})} = V_{(\text{CTL1})} = V_{(\text{CTL2})} = V_{(\text{IN})}$, $R_{(\text{FAULT})} = R_{(\text{STATUS})} = 10\text{ k}\Omega$, $R_{(\text{IMON})} = 2.55\text{ k}\Omega$, $R_{(\text{ILIM_HI})} = 19.1\text{ k}\Omega$, $R_{(\text{ILIM_LO})} = 80.6\text{ k}\Omega$. Positive currents are into pins. Typical values are at 25°C . All voltages are with respect to GND.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|------|------|------|------|
| UNDERVOLTAGE LOCKOUT, IN | | | | | | |
| V _(UVLO) | UVLO threshold voltage | IN rising | 3.9 | 4.15 | 4.3 | V |
| | Hysteresis ⁽³⁾ | T _J = 25°C | | 100 | | mV |
| FAULT | | | | | | |
| | Output low voltage | I _(FAULT) = 1 mA | | | 100 | mV |
| | Off-state leakage | V _(FAULT) = 6.5 V | | | 2 | μA |
| STATUS | | | | | | |
| | Output low voltage | I _(STATUS) = 1 mA | | | 100 | mV |
| | Off-state leakage | V _(STATUS) = 6.5 V | | | 2 | μA |
| THERMAL SHUTDOWN | | | | | | |
| T _(OTSD2) | Thermal shutdown threshold | | 155 | | | °C |
| T _(OTSD1) | Thermal shutdown threshold in current-limit | | 135 | | | °C |
| | Hysteresis ⁽³⁾ | | | 20 | | °C |
| LOAD DETECT (V _{CTL1} = V _{CTL2} = V _{IN}) | | | | | | |
| I _(LD) | I _{OUT} load detection threshold | R _(ILIM_LO) = 80.6 kΩ, rising load current | 585 | 650 | 715 | mA |
| | Hysteresis ⁽³⁾ | | | 50 | | mA |
| DM_IN AND DP_IN OVERVOLTAGE PROTECTION | | | | | | |
| V _(OV_Data) | Protection trip threshold | DP_IN and DM_IN rising | 3.7 | 3.9 | 4.15 | V |
| | Hysteresis ⁽³⁾ | | | 100 | | mV |
| R _(DCHG_Data) | Discharge resistor after OVP(2) | DP_IN = DM_IN = 18 V, IN = 5 V or 0 V | | 200 | | kΩ |
| | | DP_IN = DM_IN = 5 V, IN = 5 V | | 370 | | |
| | | DP_IN = DM_IN = 5 V, IN = 0 | | 390 | | |
| OUT OVERVOLTAGE PROTECTION | | | | | | |
| V _(OV_OUT_LOW) | Protection trip threshold | OUT rising | 5.65 | 6 | 6.35 | V |
| | Hysteresis ⁽³⁾ | | | 90 | | mV |
| V _(OV_OUT_HIGH) | Protection trip threshold | OUT rising | 6.6 | 6.95 | 7.3 | V |
| | Hysteresis ⁽³⁾ | | | 130 | | mV |
| R _(DCHG_OUT) | Discharge resistor | OUT = 18 V, IN = 5 V | | 55 | 85 | kΩ |
| | | OUT = 18 V, IN = 0 | | 80 | 120 | |
| CABLE COMPENSATION | | | | | | |
| I _(CS) | Sink current | Load = 3 A, 2.5 V ≤ V _(CS) ≤ 6.5 V | 234 | 246 | 258 | μA |
| | | Load = 2.4 A, 2.5 V ≤ V _(CS) ≤ 6.5 V | 187 | 197 | 207 | |
| | | Load = 2.1 A, 2.5 V ≤ V _(CS) ≤ 6.5 V | 163 | 172 | 181 | |
| | | Load = 1 A, 2.5 V ≤ V _(CS) ≤ 6.5 V | 77 | 82 | 87 | |
| CURRENT MONITOR OUTPUT (IMON) | | | | | | |
| I _(IMON) | Source current | Load = 3 A, 0 ≤ V _(IMON) ≤ 2.5 V | 287 | 312 | 337 | μA |
| | | Load = 2.4 A, 0 ≤ V _(IMON) ≤ 2.5 V | 230 | 250 | 270 | |
| | | Load = 2.1 A, 0 ≤ V _(IMON) ≤ 2.5 V | 201 | 218 | 235 | |
| | | Load = 1 A, 0 ≤ V _(IMON) ≤ 2.5 V | 94 | 104 | 114 | |
| | | Load = 0.5 A, 0 ≤ V _(IMON) ≤ 2.5 V | 44 | 52 | 60 | |

(3) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

Electrical Characteristics (continued)

Unless otherwise noted, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ and $4.5\text{ V} \leq V_{(IN)} \leq 6.5\text{ V}$, $V_{(EN)} = V_{(CTL1)} = V_{(CTL2)} = V_{(IN)}$, $R_{(FAULT)} = R_{(STATUS)} = 10\text{ k}\Omega$, $R_{(IMON)} = 2.55\text{ k}\Omega$, $R_{(ILIM_HI)} = 19.1\text{ k}\Omega$, $R_{(ILIM_LO)} = 80.6\text{ k}\Omega$. Positive currents are into pins. Typical values are at 25°C . All voltages are with respect to GND.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--|------|------|---------------|
| HIGH-BANDWIDTH ANALOG SWITCH | | | | | |
| $R_{(HS_ON)}$ DP and DM switch on-resistance | $V_{(DP_OUT)} = V_{(DM_OUT)} = 0\text{ V}$, $I_{(DP_IN)} = I_{(DM_IN)} = 30\text{ mA}$ | | 3.2 | 6.5 | Ω |
| | $V_{(DP_OUT)} = V_{(DM_OUT)} = 2.4\text{ V}$, $I_{(DP_IN)} = I_{(DM_IN)} = -15\text{ mA}$ | | 3.8 | 7.6 | |
| $ \Delta R_{(HS_ON)} $ Switch resistance mismatch between DP and DM channels | $V_{(DP_OUT)} = V_{(DM_OUT)} = 0\text{ V}$, $I_{(DP_IN)} = I_{(DM_IN)} = 30\text{ mA}$ | | 0.05 | 0.15 | Ω |
| | $V_{(DP_OUT)} = V_{(DM_OUT)} = 2.4\text{ V}$, $I_{(DP_IN)} = I_{(DM_IN)} = -15\text{ mA}$ | | 0.05 | 0.15 | |
| $C_{(IO_OFF)}$ DP and DM switch off-state capacitance ⁽⁴⁾ | $V_{EN} = 0\text{ V}$, $V_{(DP_IN)} = V_{(DM_IN)} = 0.3\text{ V}$, $V_{AC} = 0.03\text{ V}_{PP}$, $f = 1\text{ MHz}$ | | 8.8 | | pF |
| $C_{(IO_ON)}$ DP and DM switch on-state capacitance ⁽⁴⁾ | $V_{(DP_IN)} = V_{(DM_IN)} = 0.3\text{ V}$, $V_{AC} = 0.03\text{ V}_{PP}$, $f = 1\text{ MHz}$ | | 10.9 | | pF |
| | Off-state isolation ⁽³⁾ | $V_{(EN)} = 0\text{ V}$, $f = 250\text{ MHz}$ | 8 | | dB |
| | On-state cross-channel isolation ⁽⁴⁾ | $f = 250\text{ MHz}$ | 30 | | dB |
| $I_{(IKG_OFF)}$ Off-state leakage current | $V_{EN} = 0\text{ V}$, $V_{(DP_IN)} = V_{(DM_IN)} = 3.6\text{ V}$, $V_{(DP_OUT)} = V_{(DM_OUT)} = 0\text{ V}$, measure $I_{(DP_OUT)}$ and $I_{(DM_OUT)}$ | | 0.1 | 1.5 | μA |
| BW Bandwidth (-3 dB) ⁽⁴⁾ | $R_{(L)} = 50\text{ }\Omega$ | | 940 | | MHz |
| CHARGING DOWNSTREAM PORT DETECT | | | | | |
| $V_{(DM_SRC)}$ DM_IN CDP output voltage | $V_{(DP_IN)} = 0.6\text{ V}$, $-250\text{ }\mu\text{A} < I_{(DM_IN)} < 0\text{ }\mu\text{A}$ | 0.5 | 0.6 | 0.7 | V |
| $V_{(DAT_REF)}$ DP_IN rising lower window threshold for $V_{(DM_SRC)}$ activation | | 0.36 | | 0.4 | V |
| | Hysteresis ⁽⁴⁾ | | 50 | | mV |
| $V_{(LGC_SRC)}$ DP_IN rising upper window threshold for $V_{(DM_SRC)}$ de-activation | | 0.8 | | 0.88 | V |
| $V_{(LGC_SRC_HYS)}$ Hysteresis ⁽⁴⁾ | | | 100 | | mV |
| $I_{(DP_SINK)}$ DP_IN sink current | $V_{(DP_IN)} = 0.6\text{ V}$ | 40 | 75 | 100 | μA |

(4) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

6.6 Switching Characteristics

Unless otherwise noted $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ and $4.5\text{ V} \leq V_{(\text{IN})} \leq 6.5\text{ V}$, $V_{(\text{EN})} = V_{(\text{IN})}$, $V_{(\text{CTL1})} = V_{(\text{CTL2})} = V_{(\text{IN})}$, $R_{(\text{FAULT})} = R_{(\text{STATUS})} = 10\text{ k}\Omega$, $R_{(\text{IMON})} = 2.55\text{ k}\Omega$, $R_{(\text{ILIM_HI})} = 19.1\text{ k}\Omega$, $R_{(\text{ILIM_LO})} = 80.6\text{ k}\Omega$. Positive currents are into pins. Typical values are at 25°C . All voltages are with respect to GND.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|------|------|------|---------------|
| t_r OUT voltage rise time | $V_{(\text{IN})} = 5\text{ V}$, $C_{(\text{L})} = 1\text{ }\mu\text{F}$, $R_{(\text{L})} = 100\text{ }\Omega$ | 1.05 | 1.75 | 3.1 | ms |
| t_f OUT voltage fall time | | 0.27 | 0.47 | 0.82 | ms |
| t_{on} OUT voltage turnon time | $V_{(\text{IN})} = 5\text{ V}$, $C_{(\text{L})} = 1\text{ }\mu\text{F}$, $R_{(\text{L})} = 100\text{ }\Omega$ | | 7.5 | 11 | ms |
| t_{off} OUT voltage turnoff time | | | 2.7 | 5 | ms |
| $t_{(\text{DCHG_S})}$ Discharge hold time (mode change) | Time $V_{(\text{OUT})} < 0.7\text{ V}$ | 1.1 | 2 | 2.9 | s |
| $t_{(\text{IOS})}$ OUT short-circuit response time ⁽¹⁾ | $V_{(\text{IN})} = 5\text{ V}$, $R_{(\text{SHORT})} = 50\text{ m}\Omega$ | | 2 | | μs |
| $t_{(\text{OC_OUT_FAULT})}$ OUT $\overline{\text{FAULT}}$ deglitch time | Bidirectional deglitch applicable to current-limit condition only (no deglitch assertion for OTSD) | 5.5 | 8.5 | 11.5 | ms |
| t_{pd} Analog switch propagation delay ⁽¹⁾ | $V_{(\text{IN})} = 5\text{ V}$ | | 0.14 | | ns |
| $t_{(\text{SK})}$ Analog switch skew between opposite transitions of the same port ($t_{\text{PHL}} - t_{\text{PLH}}$) ⁽¹⁾ | $V_{(\text{IN})} = 5\text{ V}$ | | 0.02 | | ns |
| $t_{(\text{LD_SET})}$ Load-detect set time | $V_{(\text{IN})} = 5\text{ V}$ | 120 | 210 | 280 | ms |
| $t_{(\text{LD_RESET})}$ Load-detect reset time | $V_{(\text{IN})} = 5\text{ V}$ | 1.8 | 3 | 4.2 | s |
| $t_{(\text{OV_Data})}$ DP_IN and DM_IN overvoltage protection response time | | | 5 | | μs |
| $t_{(\text{OV_OUT})}$ OUT overvoltage protection response time | | | 0.3 | | μs |
| $t_{(\text{OV_D_FAULT})}$ DP_IN and DM_IN $\overline{\text{FAULT}}$ -asserted deglitch time | | 11 | 16 | 23 | ms |
| OUT $\overline{\text{FAULT}}$ -asserted deglitch time | | 11 | 16 | 23 | ms |

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

6.7 Typical Characteristics

$T_A = 25^{\circ}\text{C}$, $V_{(\text{IN})} = 5\text{ V}$, $V_{(\text{EN})} = 5\text{ V}$, $V_{(\text{CTL1})} = V_{(\text{CTL2})} = 5\text{ V}$, $\overline{\text{FAULT}}$ and $\overline{\text{STATUS}}$ connect to $V_{(\text{IN})}$ via a 10-k Ω pullup resistor (unless stated otherwise)

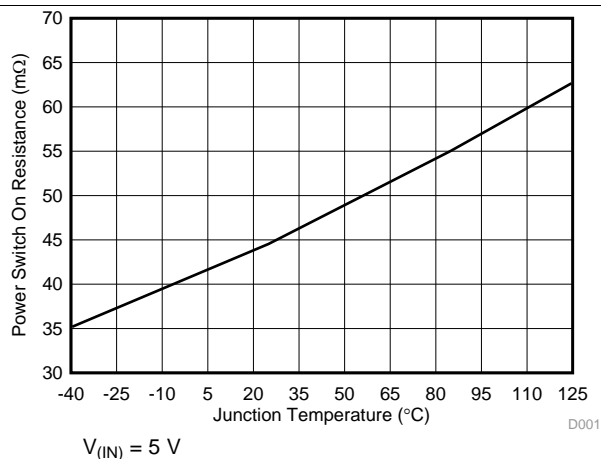


Figure 1. Power Switch On-Resistance vs Temperature

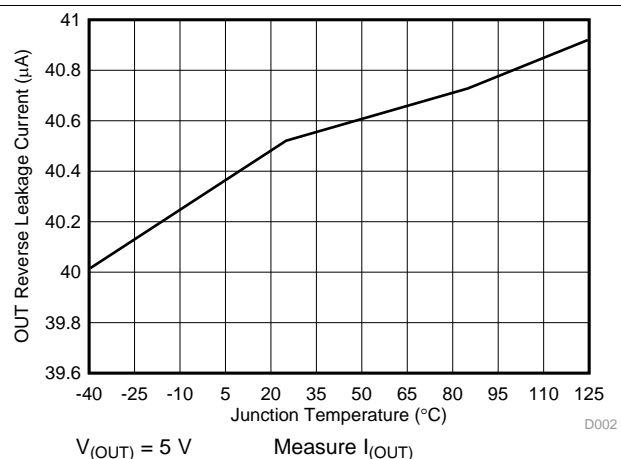


Figure 2. Reverse Leakage Current vs Temperature

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{(IN)} = 5\text{ V}$, $V_{(EN)} = 5\text{ V}$, $V_{(CTL1)} = V_{(CTL2)} = 5\text{ V}$, $\overline{\text{FAULT}}$ and $\overline{\text{STATUS}}$ connect to $V_{(IN)}$ via a 10-k Ω pullup resistor (unless stated otherwise)

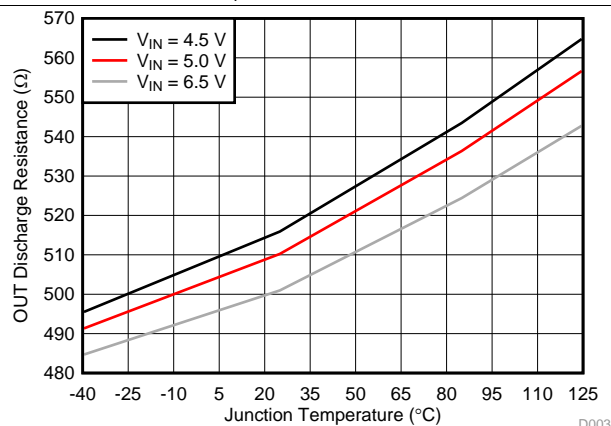


Figure 3. OUT Discharge Resistance (Mode Change) vs Temperature

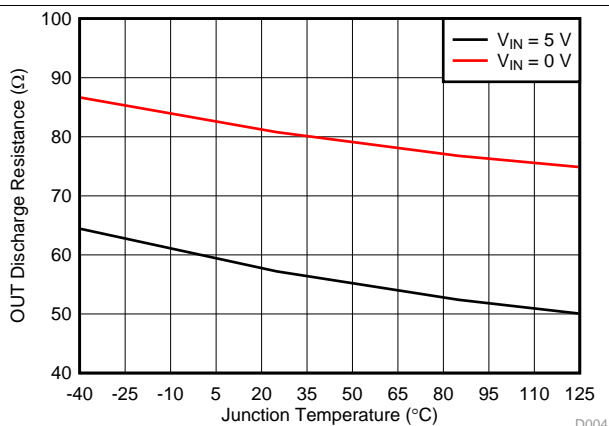


Figure 4. OUT Discharge Resistance (OVP) vs Temperature

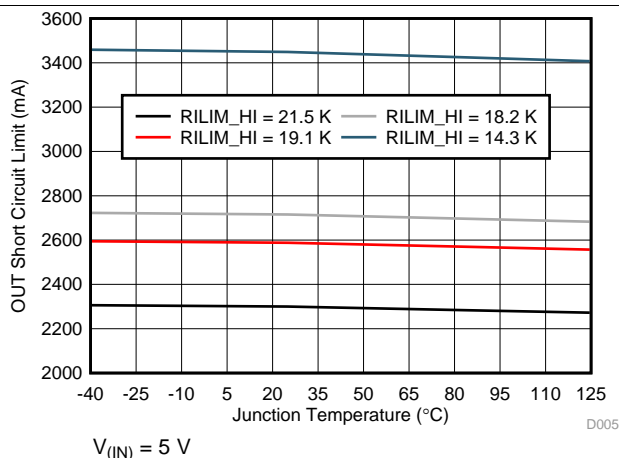


Figure 5. OUT Short-Circuit Current Limit vs Temperature I

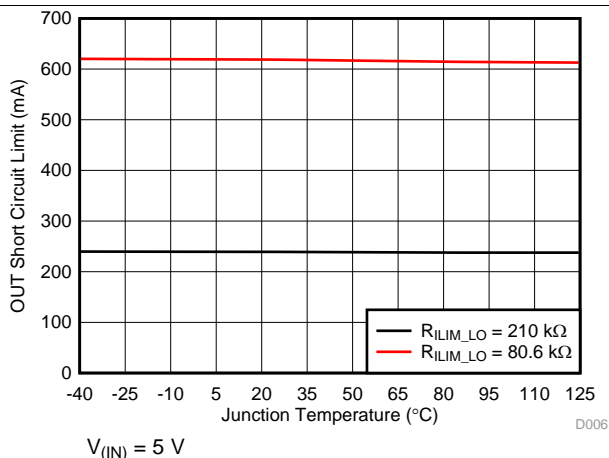


Figure 6. OUT Short-Circuit Current Limit vs Temperature II

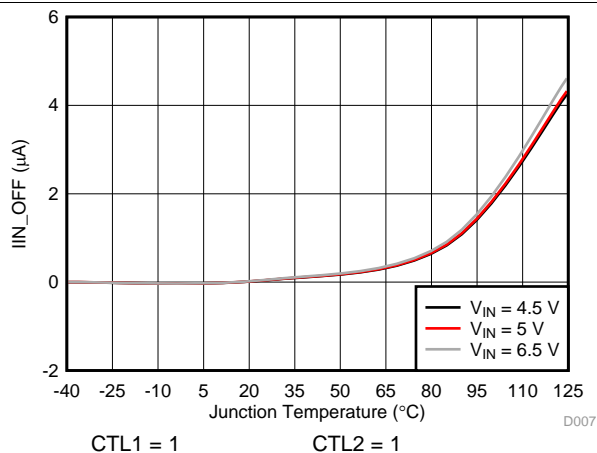


Figure 7. Disabled IN Supply Current vs Temperature

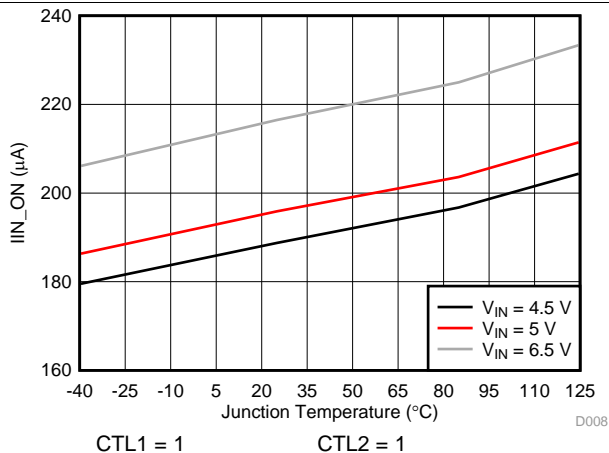


Figure 8. Enabled IN Supply Current – CDP (11) vs Temperature

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{(IN)} = 5\text{ V}$, $V_{(EN)} = 5\text{ V}$, $V_{(CTL1)} = V_{(CTL2)} = 5\text{ V}$, $\overline{\text{FAULT}}$ and $\overline{\text{STATUS}}$ connect to $V_{(IN)}$ via a 10-k Ω pullup resistor (unless stated otherwise)

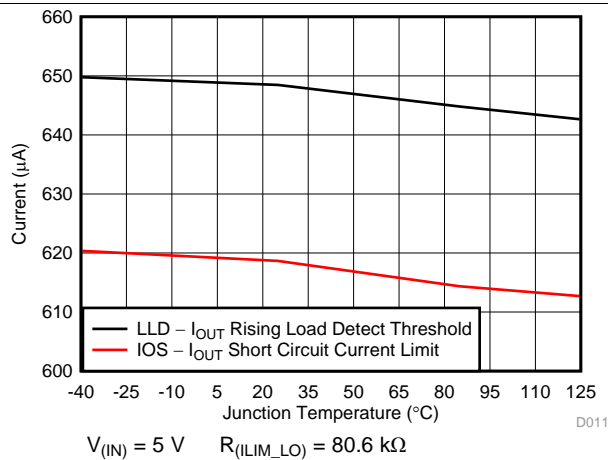


Figure 9. $I_{O(OUT)}$ Rising Load-Detect Threshold and OUT Short-Circuit Limit vs Temperature

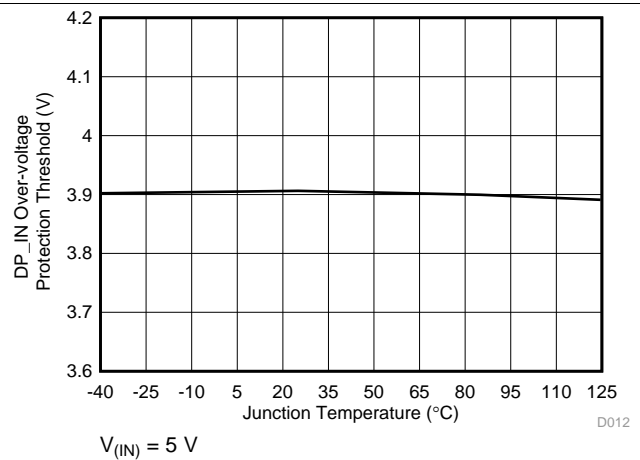


Figure 10. DP_IN Overvoltage Protection Threshold vs Temperature

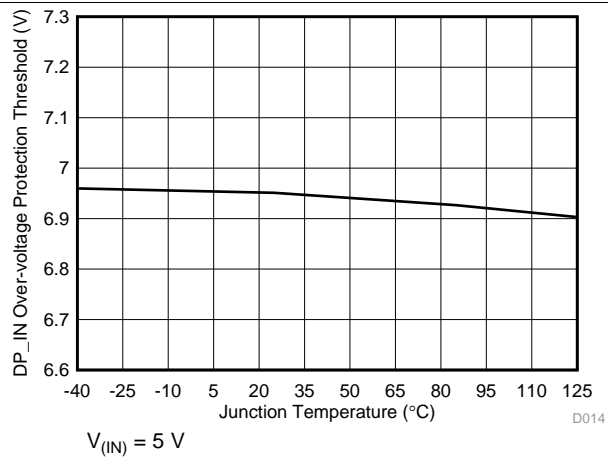


Figure 11. OUT Overvoltage Protection Threshold vs Temperature

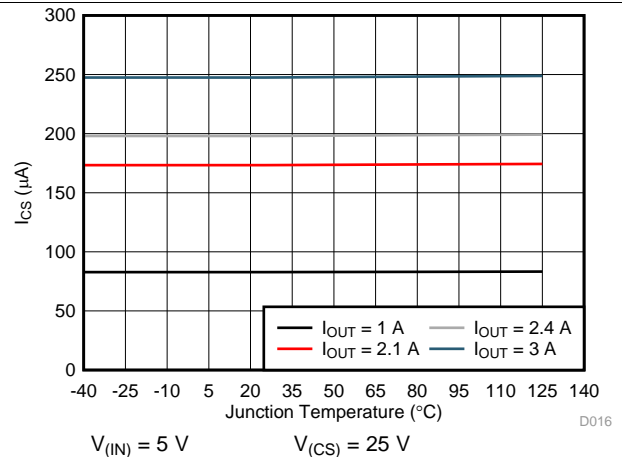


Figure 12. I_{CS} vs Temperature

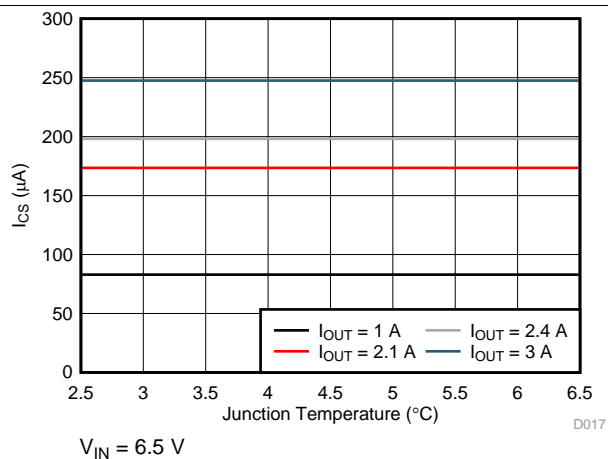


Figure 13. I_{CS} vs V_{CS} Voltage

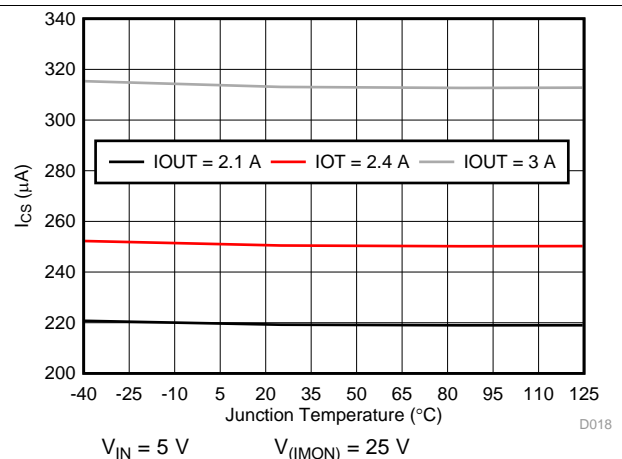


Figure 14. I_{IMON} vs Temperature

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{(IN)} = 5\text{ V}$, $V_{(EN)} = 5\text{ V}$, $V_{(CTL1)} = V_{(CTL2)} = 5\text{ V}$, $\overline{\text{FAULT}}$ and $\overline{\text{STATUS}}$ connect to $V_{(IN)}$ via a 10-k Ω pullup resistor (unless stated otherwise)

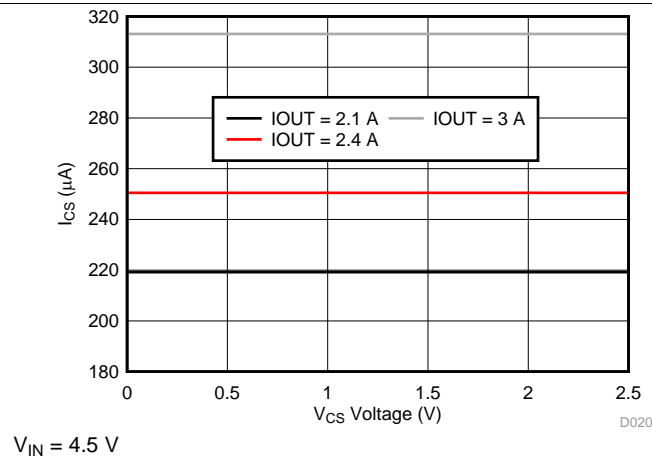
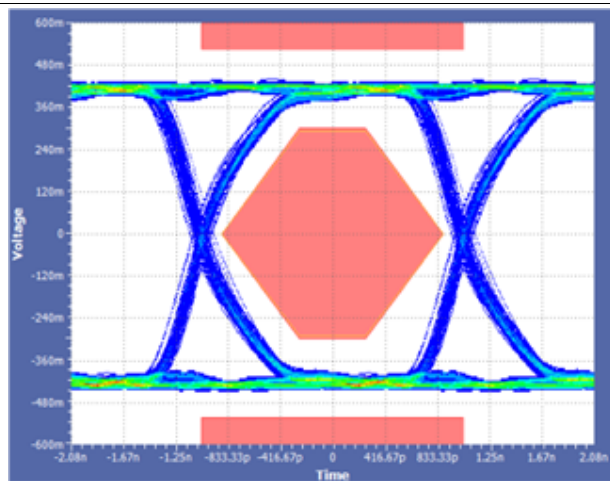
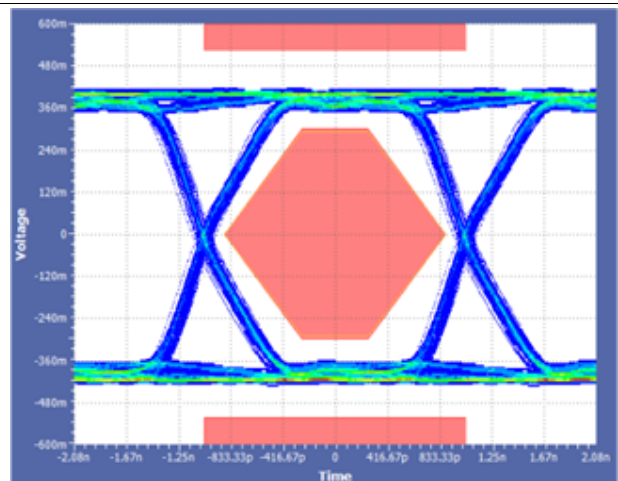


Figure 15. $I_{(IMON)}$ vs $V_{(CS)}$ Voltage



Measured on EVM with 10-cm cable

Figure 16. Bypassing the TPS254900-Q1 Data Switch



Measured on EVM with 10-cm cable

Figure 17. Through the TPS254900-Q1 Data Switch

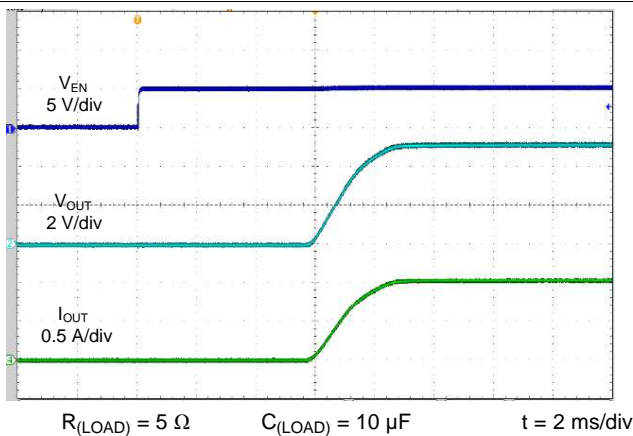


Figure 18. Turnon Response

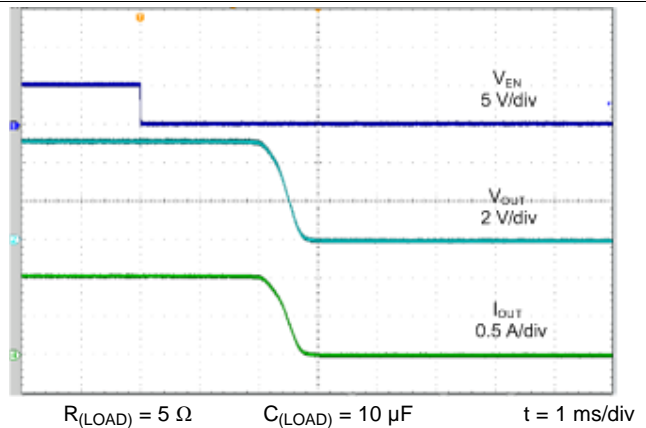


Figure 19. Turnoff Response

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{(IN)} = 5\text{ V}$, $V_{(EN)} = 5\text{ V}$, $V_{(CTL1)} = V_{(CTL2)} = 5\text{ V}$, $\overline{\text{FAULT}}$ and $\overline{\text{STATUS}}$ connect to $V_{(IN)}$ via a 10-k Ω pullup resistor (unless stated otherwise)

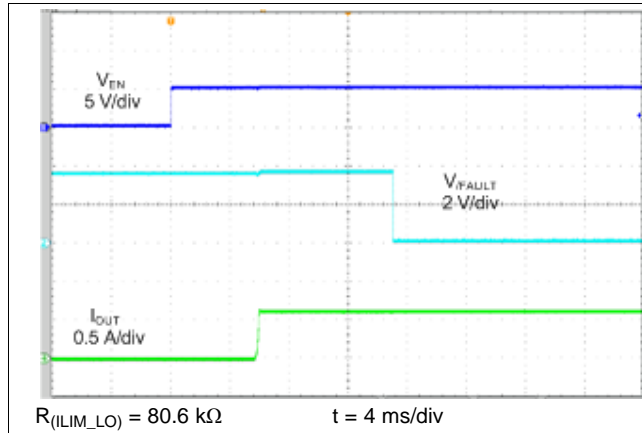


Figure 20. Enable Into Short (SDP)

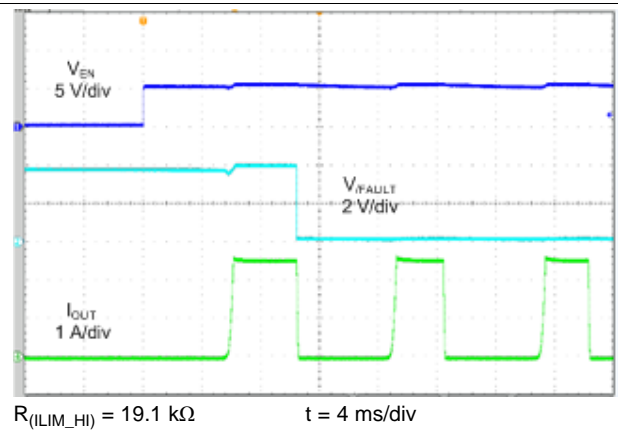


Figure 21. Enable Into Short (CDP) – Thermal Cycling

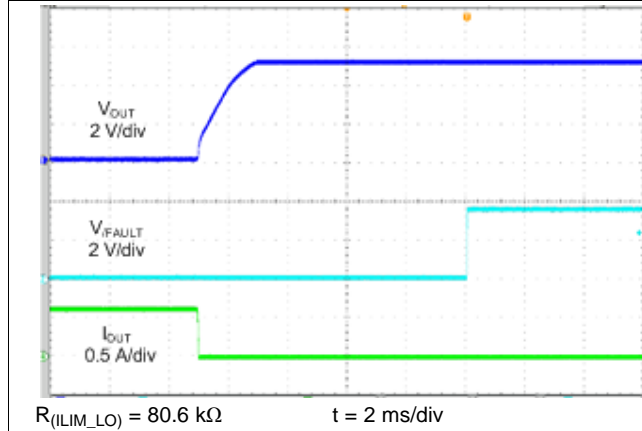


Figure 22. Short Circuit to No Load (SDP)

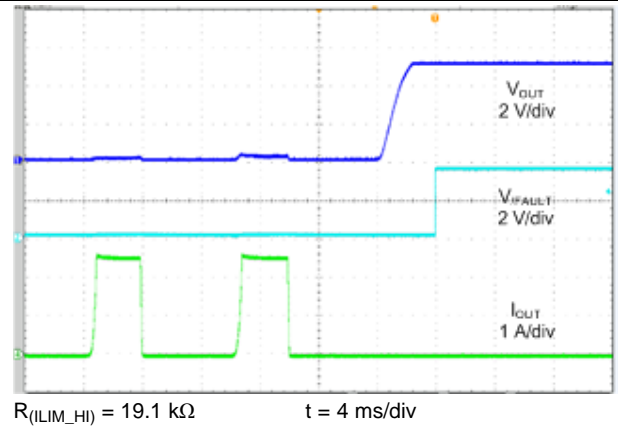


Figure 23. Short Circuit to No Load (CDP)

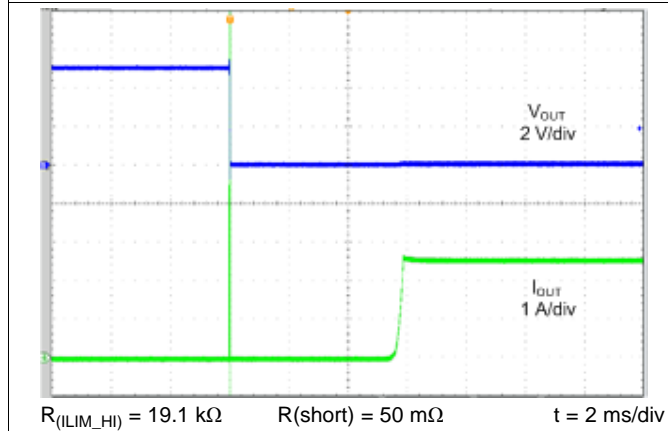


Figure 24. Hot Short

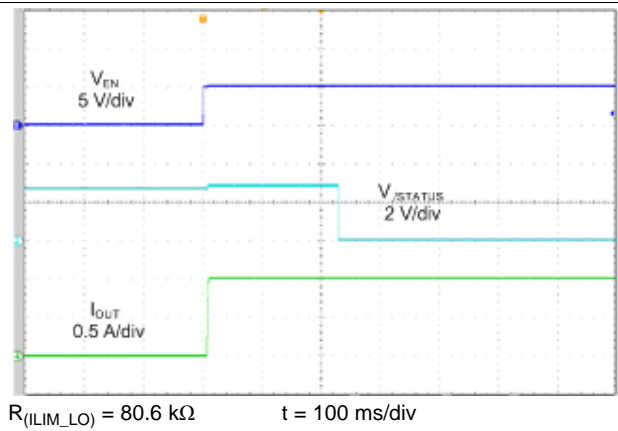


Figure 25. Load-Detection Set Time

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{(IN)} = 5\text{ V}$, $V_{(EN)} = 5\text{ V}$, $V_{(CTL1)} = V_{(CTL2)} = 5\text{ V}$, $\overline{\text{FAULT}}$ and $\overline{\text{STATUS}}$ connect to $V_{(IN)}$ via a 10-k Ω pullup resistor (unless stated otherwise)

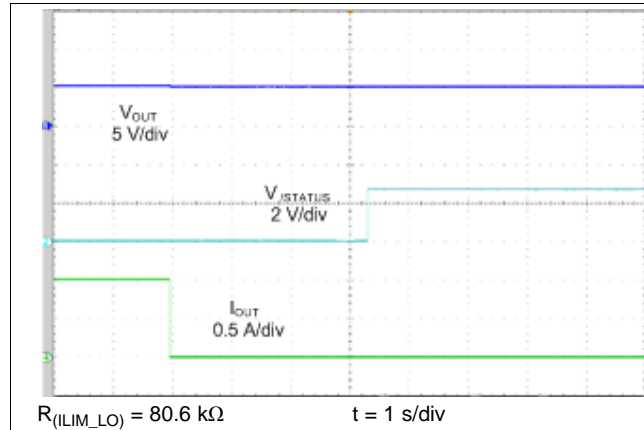


Figure 26. Load-Detection Reset Time

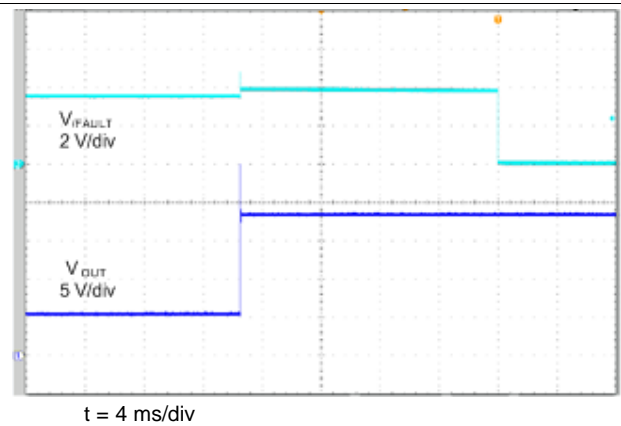


Figure 27. OUT Short to Battery

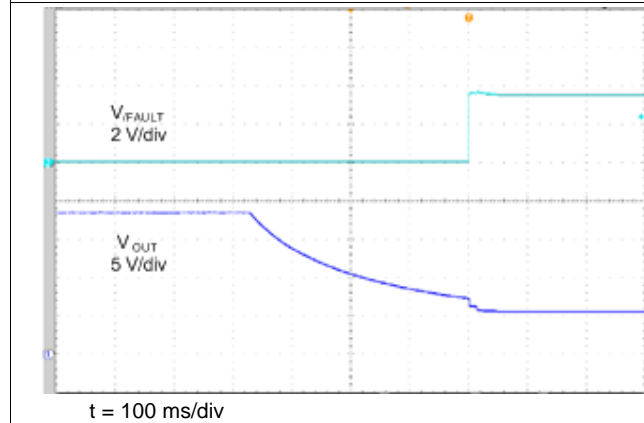


Figure 28. OUT Short-to-Battery Recovery

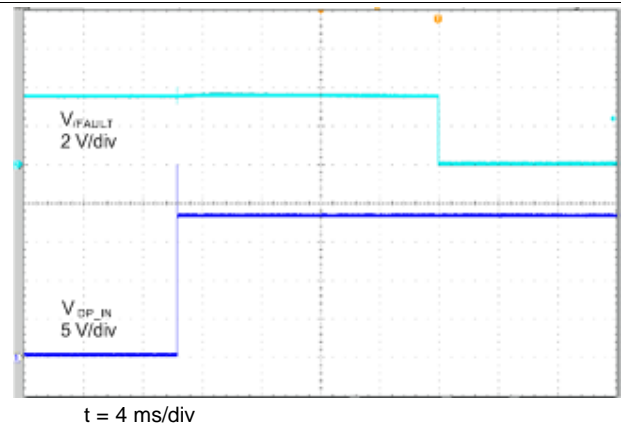


Figure 29. DP_IN Short to Battery

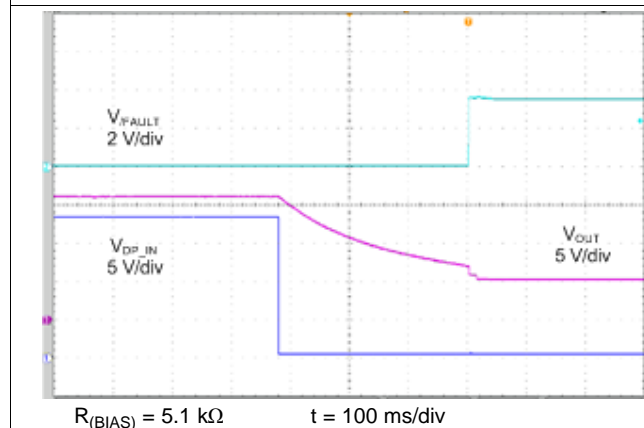


Figure 30. DP_IN Short-to-Battery Recovery

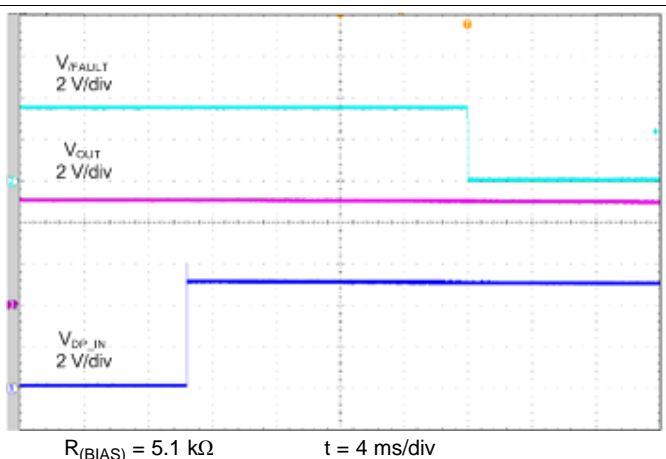


Figure 31. DP_IN Short to V_{BUS}

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{(IN)} = 5\text{ V}$, $V_{(EN)} = 5\text{ V}$, $V_{(CTL1)} = V_{(CTL2)} = 5\text{ V}$, $\overline{\text{FAULT}}$ and $\overline{\text{STATUS}}$ connect to $V_{(IN)}$ via a 10-k Ω pullup resistor (unless stated otherwise)

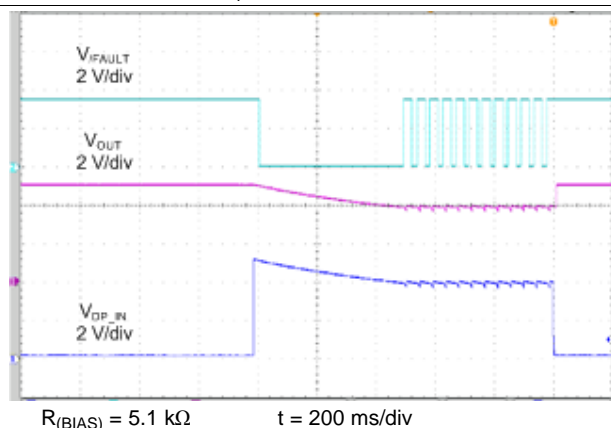


Figure 32. DP_IN Short-to- V_{BUS} and Recovery

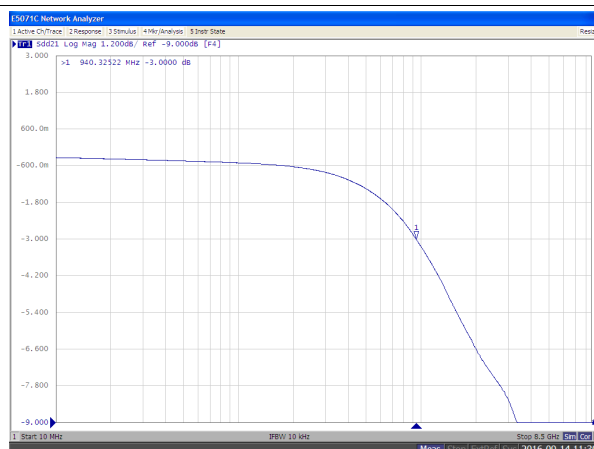


Figure 33. Data Transmission Characteristics vs Frequency

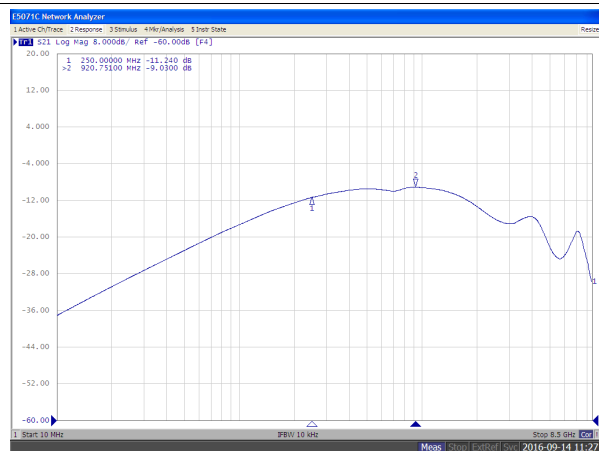


Figure 34. Off-State Data-Switch Isolation vs Frequency

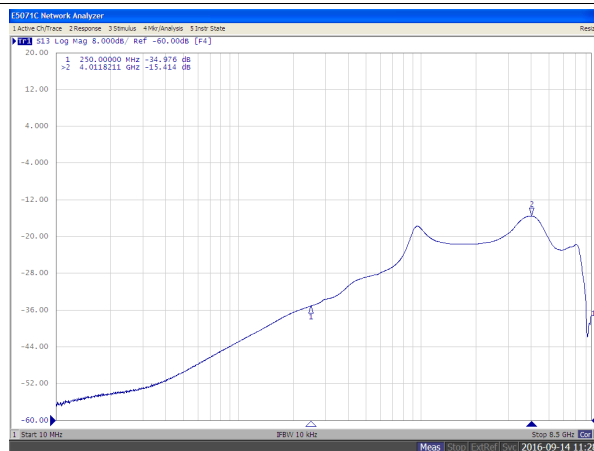
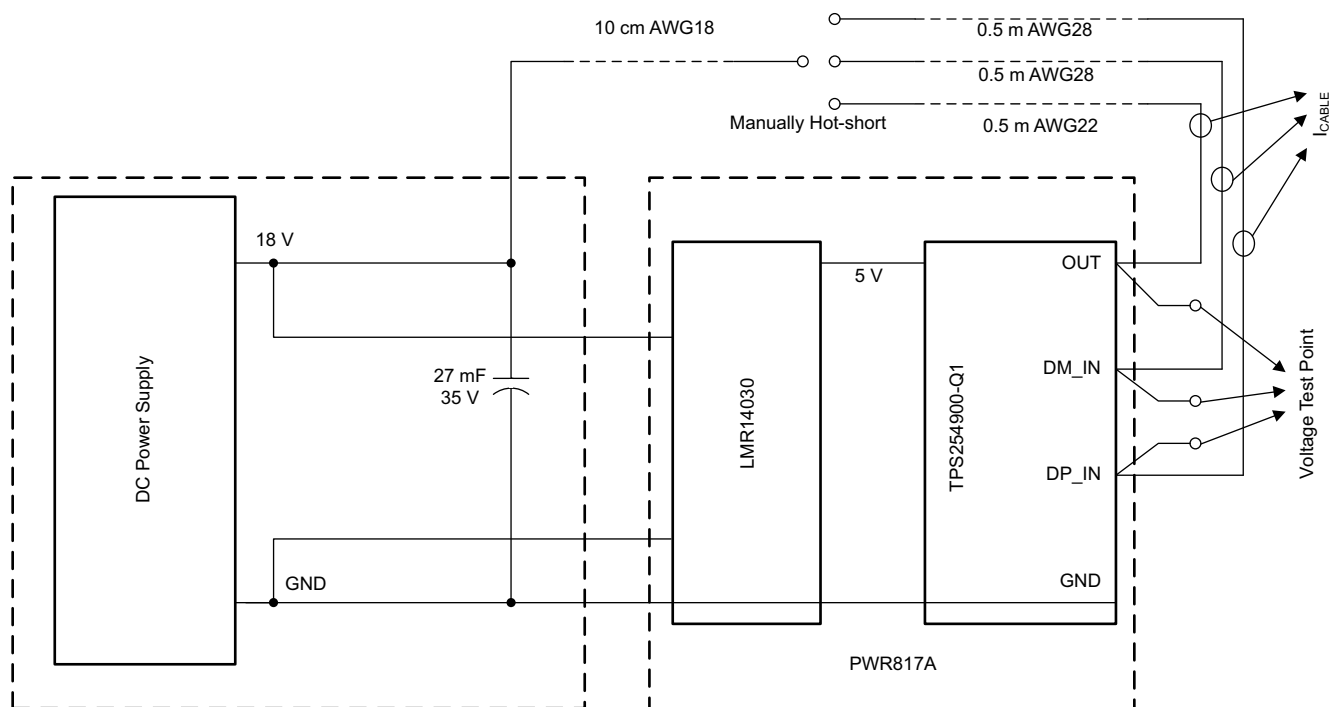


Figure 35. On-State Cross-Channel Isolation vs Frequency

7 Parameter Measurement Information



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Figure 36. Short-to-Battery System Test Setup

8 Detailed Description

8.1 Overview

The TPS254900-Q1 device is a USB charging controller and power switch which integrates D+ and D– short-to-battery protection, cable compensation, current monitor (IMON), and IEC ESD protection suitable for automotive USB charging and USB port protection applications.

The integrated power distribution switch uses N-channel MOSFETs suitable for applications where short circuits or heavy capacitive loads will be encountered. The device allows the user to adjust the current-limit thresholds using external resistors. The device enters constant-current mode when the load exceeds the current-limit threshold.

The TPS254900-Q1 device provides V_{BUS} , D+, and D– short-to-battery protection. This protects the upstream voltage regulator, automotive processor, and hub when these pins are exposed to fault conditions.

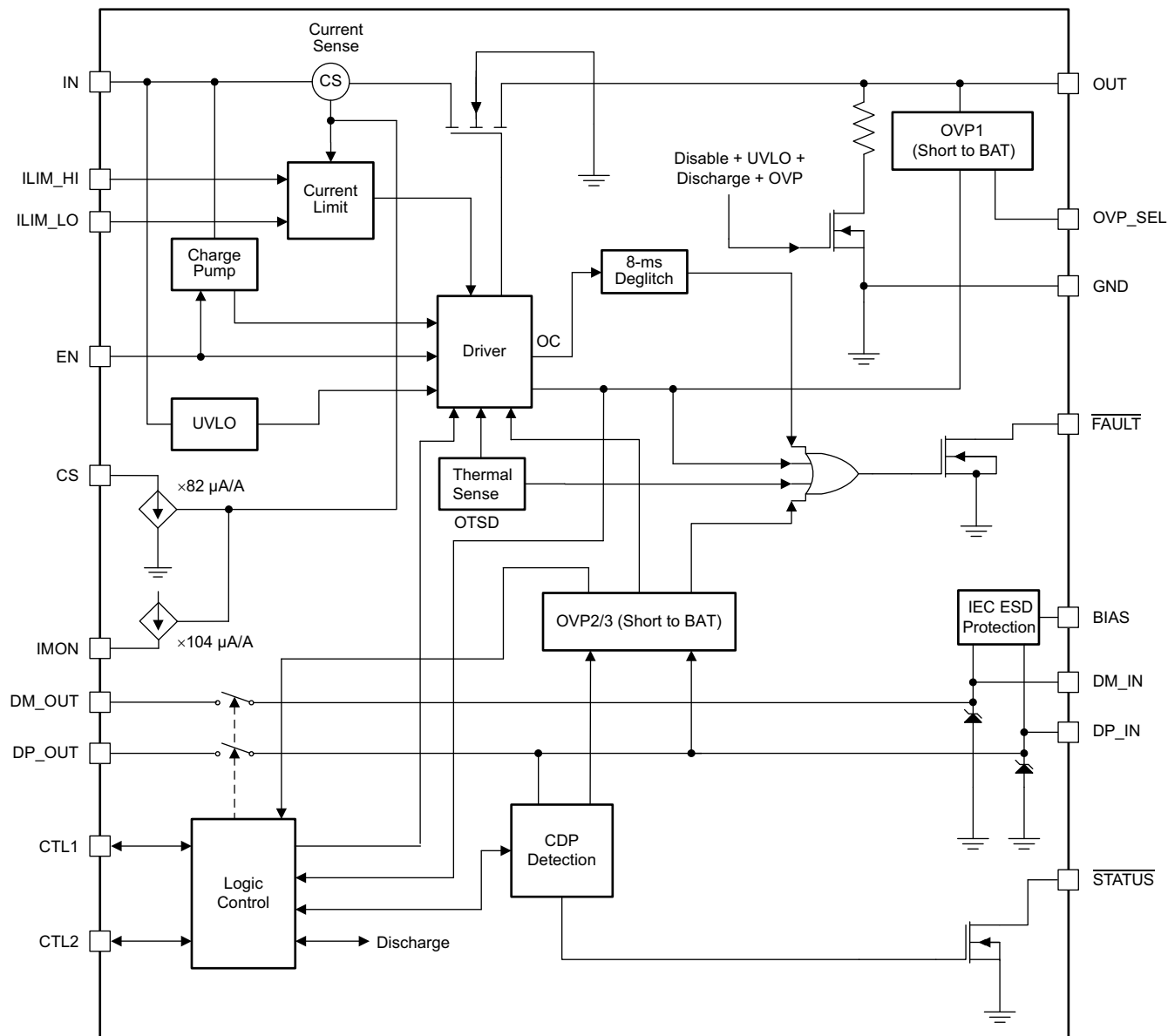
The device also integrates CDP mode, defined in the BC1.2 specification, to enable up to 1.5-A fast charging of most portable devices during data communication.

The TPS254900-Q1 device integrates a cable compensation (CS) feature to compensate for long-cable voltage drop. This keeps the remote USB port output voltage constant to enhance the user experience under high-current charging conditions.

The TPS254900-Q1 device provides a current-monitor function (IMON) by connecting a resistor from the IMON pin to GND to provide a positive voltage linearly with load current. This can be used for system power or dynamic power management.

Additionally, the device provides ESD protection up to ± 8 kV (contact discharge) and ± 15 kV (air discharge) per IEC 61000-4-2 on DP_IN and DM_IN.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 $\overline{\text{FAULT}}$ Response

The device features an active-low, open-drain fault output. $\overline{\text{FAULT}}$ goes low when there is a fault condition. Fault detection includes overtemperature, overcurrent, or overvoltage on V_{BUS} , DP_IN and DM_IN . Connect a 10-k Ω pull-up resistor from $\overline{\text{FAULT}}$ to IN.

Table 1 summarizes the conditions that generate a fault and actions taken by the device.

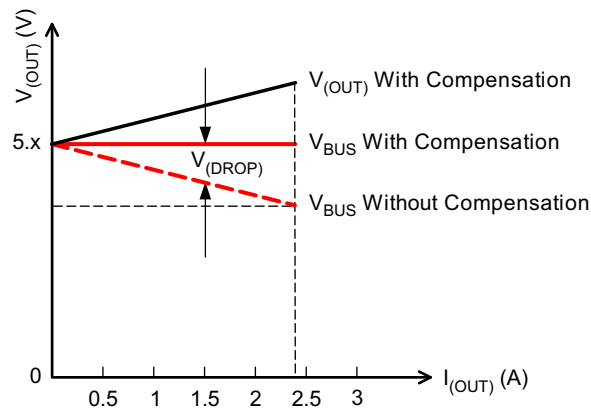
Feature Description (continued)

Table 1. Fault Conditions

| EVENT | CONDITION | ACTION |
|-------------------------------|--|---|
| Overvoltage on the data lines | $V_{(DP_IN)}$ or $V_{(DM_IN)} > 3.9\text{ V}$ | The device immediately shuts off the USB data switches and the internal power switch. The fault indicator asserts with a 16-ms deglitch, and deasserts without deglitch. |
| Overvoltage on $V_{(OUT)}$ | $V_{(OUT)} > 6\text{ V}$ or 6.95 V | The device immediately shuts off the internal power switch and the USB data switches. The fault indicator asserts with a 16-ms deglitch and deasserts without deglitch. |
| Overcurrent on $V_{(OUT)}$ | $I_{(OUT)} > I_{(OS)}$ | The device regulates switch current at $I_{(OS)}$ until thermal cycling occurs. The fault indicator asserts and deasserts with an 8-ms deglitch (the device does not assert FAULT on overcurrent in SDP1 mode). |
| Overtemperature | $T_J > OTSD2$ in non-current-limited or $T_J > OTSD1$ in current-limited mode. | The device immediately shuts off the internal power switch and the USB data switches. The fault indicator asserts immediately when the junction temperature exceeds OTSD2 or OTSD1 while in a current-limiting condition. The device has a thermal hysteresis of 20°C . |

8.3.2 Cable Compensation

When a load draws current through a long or thin wire, there is an IR drop that reduces the voltage delivered to the load. In the vehicle from the voltage regulator 5-V output to the V_{PD_IN} (input voltage of portable device), the total resistance of power switch $r_{DS(on)}$ and cable resistance causes an IR drop at the PD input. So the charging current of most portable devices is less than their expected maximum charging current.


Figure 37. Voltage Drop

TPS254900-Q1 device detects the load current and applies a proportional sink current that can be used to adjust the output voltage of the upstream regulator to compensate for the IR drop in the charging path. The gain $G_{(CS)}$ of the sink current proportional to load current is $82\text{ }\mu\text{A/A}$.

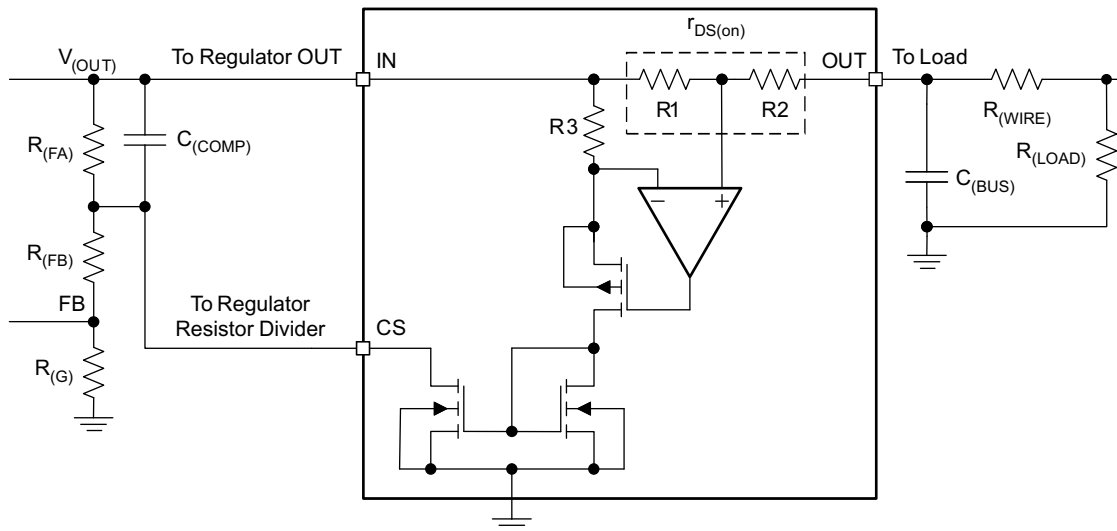


Figure 38. Cable Compensation Equivalent Circuit

8.3.2.1 Design Procedure

To start the procedure, the total resistance, including the power switch $r_{DS(on)}$ and wire resistance $R_{(WIRE)}$, must be known.

1. Choose $R_{(G)}$ following the voltage-regulator feedback resistor-divider design guideline.

2. Calculate $R_{(FA)}$ according to Equation 1.

$$R_{FA} = (r_{DS(on)} + R_{(WIRE)}) / G_{(CS)} \quad (1)$$

3. Calculate $R_{(FB)}$ according to Equation 2.

$$R_{(FB)} = \frac{V_{(OUT)}}{V_{(FB)} / R_{(G)}} - R_{(G)} - R_{(FA)} \quad (2)$$

4. $C_{(COMP)}$ in parallel with $R_{(FA)}$ is required to stabilize $V_{(OUT)}$ when $C_{(BUS)}$ is large. Start with $C_{(COMP)} \geq 3 \times G_{(CS)} \times C_{(OUT)}$, then adjust $C_{(COMP)}$ to optimize the load transient of the voltage regulator output. $V_{(OUT)}$ stability should always be verified in the end application circuit.

8.3.3 D+ and D– Protection

D+ and D– protection consists of ESD and OVP (overvoltage protection). The DP_IN and DM_IN pins provide ESD protection up to ± 15 kV (air discharge) and ± 8 kV (contact discharge) per IEC 61000-4-2 (see the [ESD Ratings](#) section for test conditions).

The ESD stress seen at DP_IN and DM_IN is impacted by many external factors, like the parasitic resistance and inductance between ESD test points and the DP_IN and DM_IN pins. For air discharge, the temperature and humidity of the environment can cause some difference, so the IEC performance should always be verified in the end-application circuit.

The IEC ESD performance of the TPS254900-Q1 device depends on the capacitance connected from BIAS to GND. A 2.2- μ F capacitor placed close to the BIAS pin is recommended. Connect the BIAS pin to OUT using a 5.1-k Ω resistor as a discharge path for the ESD stress.

OVP protection is provided for short-to- V_{BUS} or short-to-battery conditions in the vehicle harness, preventing damage to the upstream USB transceiver or hub. When the voltage on DP_IN or DM_IN exceeds 3.9 V (typical), the TPS254900-Q1 device quickly responds to block the high-voltage reverse connection to DP_OUT and DM_OUT. Overcurrent short-to-GND protection for D+ and D– is provided by the upstream USB transceiver.

8.3.4 V_{BUS} OVP Protection

The TPS254900-Q1 OUT pin can withstand up to 18 V. The internal MOSFET turns off quickly when a short-to-battery condition occurs.

The TPS254900-Q1 device has two OVP thresholds; one is 6 V (typical) and the other is 6.95 V (typical). Set the OVP threshold using the external OVP_SEL pin.

8.3.5 Output and D+ or D– Discharge

To allow a charging port to renegotiate current with a portable device, the TPS254900-Q1 device uses the OUT discharge function. During mode change, the TPS254900-Q1 device turns off the power switch while discharging OUT with a 500-Ω resistance, then turning back on the power switches to reassert the OUT voltage.

When an OVP condition occurs on DP_IN or DM_IN, the TPS254900-Q1 device enables an internal 200-kΩ discharge resistance from DP_IN to ground and from DM_IN to ground. The analog switches are also turned off. The TPS254900-Q1 device automatically disables the discharge paths and turns on the analog switches once the OVP condition is removed.

When an OVP condition occurs on OUT, the TPS254900-Q1 device turns on an internal discharge path (see Table 2 for the discharge resistance). The TPS254900-Q1 device automatically turns off the discharge path and turns on the power switch once the OVP condition is removed.

Table 2. OUT Discharge Resistance

| VIN ⁽¹⁾ | EN ⁽¹⁾ | OVP ⁽¹⁾ | OUT Discharge Resistance ⁽²⁾ |
|--------------------|-------------------|--------------------|---|
| 0 | 0 | 0 | — |
| 0 | 0 | 1 | 80 kΩ |
| 0 | 1 | 0 | — |
| 0 | 1 | 1 | 80 kΩ |
| 1 | 0 | 0 | 500 Ω |
| 1 | 0 | 1 | 500 Ω or 55 kΩ |
| 1 | 1 | 0 | — |
| 1 | 1 | 1 | 55 kΩ |

(1) 0 = inactive, 1 = active

(2) — = no discharge resistance

8.3.6 Port Power Management (PPM)

PPM is the intelligent and dynamic allocation of power. PPM is for systems that have multiple charging ports but cannot power them all simultaneously.

8.3.6.1 Benefits of PPM

The benefits of PPM include the following:

- Delivers better user experience
- Prevents overloading of system power supply
- Allows for dynamic power limits based on system state
- Allows every port potentially to be a high-power charging port
- Allows for smaller power-supply capacity because loading is controlled

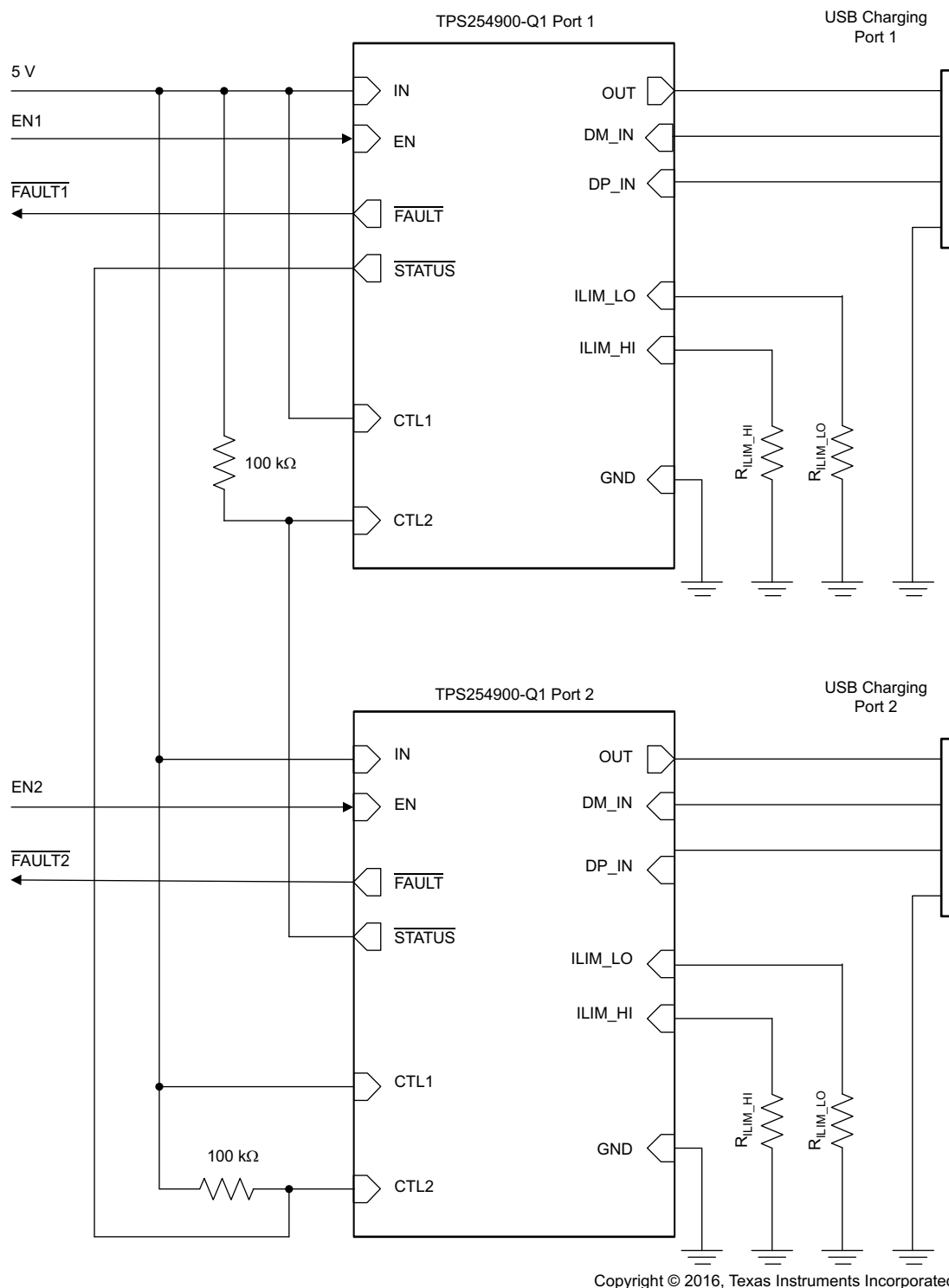
8.3.6.2 PPM Details

All ports are allowed to broadcast high-current charging. The current limit is based on ILIM_HI. The system monitors the STATUS pin to see when high-current loads are present. Once the allowed number of ports asserts STATUS, the remaining ports are toggled to a non-charging port. The current limit of the non-charging port is based on the ILIM_LO setting. The non-charging ports are automatically toggled back to charging ports when a charging port deasserts STATUS.

STATUS asserts in a charging port when the load current is above ILIM_LO + 30 mA for 210 ms (typical). STATUS deasserts in a charging port when the load current is below ILIM_LO – 20 mA for 3 seconds (typical).

8.3.6.3 Implementing PPM in a System With Two Charging Ports (CDP and SDP1)

Figure 39 shows the implementation of the two charging ports with data communication, each with a TPS254900-Q1 device and configured in CDP mode. In this example, the 5-V power supply for the two charging ports is rated at less than 3.5 A. Both TPS254900-Q1 devices have $R_{(ILIM)}$ chosen to correspond to the low (1-A) and high (2.4-A) current-limit setting for the port. In this implementation, the system can support only one of the two ports at 2.4-A charging current, whereas the other port is set to the SDP1 mode and I_{OS} corresponds to 1 A.



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Figure 39. PPM Between CDP and SDP1

8.3.7 Overcurrent Protection

When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur. In the first condition, the output is shorted before the device is enabled or before the application of $V_{(IN)}$. The TPS254900-Q1 device senses the short and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents flow for 1 to 2 μs (typical) before the current-limit circuit reacts. The device operates in constant-current mode after the current-limit circuit has responded. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting. The device remains off until the junction temperature cools approximately 20°C and then restarts. The device continues to cycle on and off until the overcurrent condition is removed.

8.3.8 Undervoltage Lockout

The undervoltage-lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted oscillations on the output due to input voltage drop from large current surges.

8.3.9 Thermal Sensing

Two independent thermal-sensing circuits protect the TPS254900-Q1 device if the temperature exceeds recommended operating conditions. These circuits monitor the operating temperature of the power-distribution switch and disable operation. The power dissipation in the package is proportional to the voltage drop across the power switch, so the junction temperature rises during an overcurrent condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C and the device is in current limit. The second thermal sensor turns off the power switch when the die temperature exceeds 155°C regardless of whether the power switch is in current limit. Hysteresis is built into both thermal sensors, and the switch turns on after the device has cooled by approximately 20°C. The switch continues to cycle off and then on until the fault is removed. The open-drain false-reporting output, $\overline{\text{FAULT}}$, is asserted (low) during an overtemperature shutdown condition.

8.3.10 Current-Limit Setting

The TPS254900-Q1 has two independent current-limit settings that are each adjusted externally with a resistor. The ILIM_HI setting is adjusted with $R_{(\text{ILIM_HI})}$ connected between ILIM_HI and GND. The ILIM_LO setting is adjusted with $R_{(\text{ILIM_LO})}$ connected between ILIM_LO and GND. Consult the device truth table (Table 3) to see when each current limit is used. Both settings have the same relation between the current limit and the adjusting resistor.

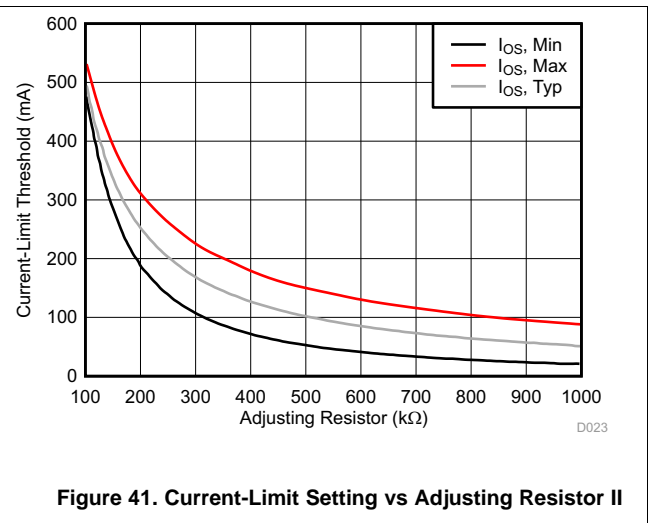
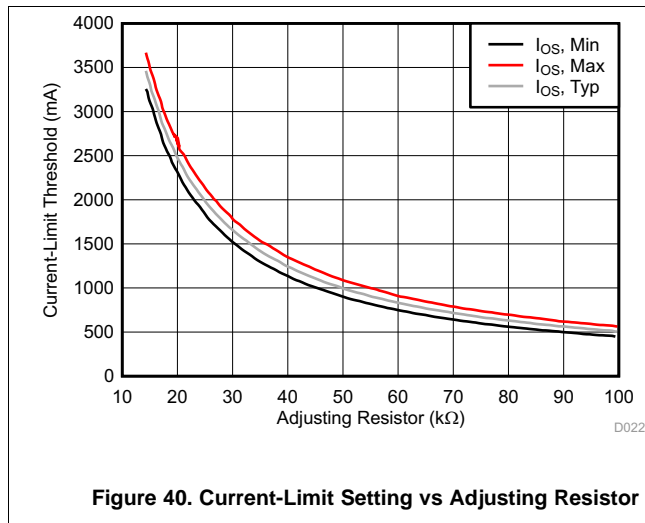
The following equation calculates the value of resistor for adjusting the typical current limit:

$$I_{\text{OS(nom)}} \text{ (mA)} = \frac{48687 \text{ V}}{R_{(\text{ILIM_xx})}^{0.9945} \text{ k}\Omega} \quad (3)$$

Many applications require that the current limit meet specific tolerance limits. When designing to these tolerance limits, both the tolerance of the TPS254900-Q1 current limit and the tolerance of the external adjusting resistor must be taken into account. The following equations approximate the TPS254900-Q1 minimum and maximum current limits to within a few milliamperes and are appropriate for design purposes. The equations do not constitute part of TI's published device specifications for purposes of TI's product warranty. These equations assume an ideal—no variation—external adjusting resistor. To take resistor tolerance into account, first determine the minimum and maximum resistor values based on its tolerance specifications and use these values in the equations. Because of the inverse relation between the current limit and the adjusting resistor, use the maximum resistor value in the $I_{\text{OS(min)}}$ equation and the minimum resistor value in the $I_{\text{OS(max)}}$ equation.

$$I_{\text{OS(min)}} \text{ (mA)} = \frac{46464 \text{ V}}{R_{(\text{ILIM_xx})}^{0.9974} \text{ k}\Omega} - 32 \quad (4)$$

$$I_{\text{OS(max)}} \text{ (mA)} = \frac{51820 \text{ V}}{R_{(\text{ILIM_xx})}^{0.9987} \text{ k}\Omega} + 38 \quad (5)$$



The routing of the traces to the $R_{(ILIM_xx)}$ resistors should have a sufficiently low resistance so as not to affect the current-limit accuracy. The ground connection for the $R_{(ILIM_xx)}$ resistors is also very important. The resistors must reference back to the TPS254900-Q1 GND pin. Follow normal board layout practices to ensure that current flow from other parts of the board does not impact the ground potential between the resistors and the TPS254900-Q1 GND pin.

8.4 Device Functional Modes

8.4.1 Device Truth Table (TT)

The device truth table (Table 3) lists all valid combinations for both control pins (CTL1 and CTL2), and the corresponding charging mode. The TPS254900-Q1 device monitors the CTL inputs and transitions to the charging mode to which it is commanded.

Table 3. Truth Table

| CTL1 | CTL2 | CURRENT LIMIT SELECTED | MODE | STATUS for Load Detect | \overline{CS} FOR CABLE COMPENSATION | IMON FOR CURRENT MONITOR | FAULT REPORT | NOTES |
|------|------|------------------------|----------------------------|------------------------|--|--------------------------|-------------------|---|
| 0 | 0 | N/A | Client mode ⁽¹⁾ | OFF | OFF | OFF | OFF | Power switch is disabled, only analog switch is on. |
| 0 | 1 | ILIM_LO | SDP | OFF | ON | ON | ON | Standard SDP |
| 1 | 0 | ILIM_LO | SDP1 ⁽²⁾ | OFF | ON | ON | ON ⁽³⁾ | No OUT discharge between CDP and SDP1 for PPM |
| 1 | 1 | ILIM_HI | CDP ⁽²⁾ | ON | ON | ON | ON | |

(1) No 5.1-kΩ resistor from BIAS to OUT (open between the pins), or OUT still has 5-V voltage from an external downstream port; client mode is still active.

(2) No OUT discharge when changing from 10 to 11 or from 11 to 10.

(3) A fault only trips OTSD, OUT, DP_IN, DM_IN, and OVP.

8.4.2 USB BC1.2 Specification Overview

The BC1.2 specification includes three different port types:

- Standard downstream port (SDP)
- Charging downstream port (CDP)
- Dedicated charging port (DCP)

BC1.2 defines a charging port as a downstream-facing USB port that provides power for charging portable equipment. Under this definition, CDP and DCP are defined as charging ports.

Table 4 lists the difference between these port types.

Table 4. Operating Modes Table

| PORT TYPE | SUPPORTS USB2.0 COMMUNICATION | MAXIMUM ALLOWABLE CURRENT DRAWN BY PORTABLE EQUIPMENT (A) |
|---------------|-------------------------------|---|
| SDP (USB 2.0) | YES | 0.5 |
| SDP (USB 3.0) | YES | 0.9 |
| CDP | YES | 1.5 |
| DCP | NO | 1.5 |

8.4.3 Standard Downstream Port (SDP) Mode — USB 2.0 and USB 3.0

An SDP is a traditional USB port that follows the USB 2.0 or USB 3.0 protocol. An SDP supplies a minimum of 500 mA per port for USB 2.0 and 900 mA per port for USB 3.0. USB 2.0 and USB 3.0 communication is supported, and the host controller must be active to allow charging.

8.4.4 Charging Downstream Port (CDP) Mode

A CDP is a USB port that follows the USB BC1.2 specification and supplies a minimum of 1.5 A per port. A CDP provides power and meets the USB 2.0 requirements for device enumeration. USB 2.0 communication is supported, and the host controller must be active to allow charging. The difference between CDP and SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

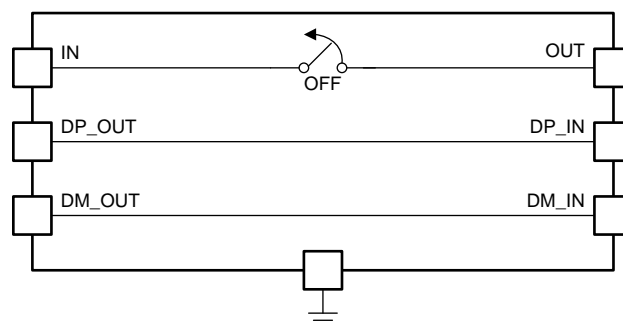
The CDP handshaking process occurs in two steps. During the first step, the portable equipment outputs a nominal 0.6-V output on the D+ line and reads the voltage input on the D– line. The portable device detects the connection to an SDP if the voltage is less than the nominal data-detect voltage of 0.3 V. The portable device detects the connection to a CDP if the D– voltage is greater than the nominal data-detect voltage of 0.3 V and optionally less than 0.8 V.

The second step is necessary for portable equipment to determine whether the equipment is connected to a CDP or a DCP. The portable device outputs a nominal 0.6-V output on the D– line and reads the voltage input on the D+ line. The portable device concludes the equipment is connected to a CDP if the data line being read remains less than the nominal data detects voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data-detect voltage of 0.3 V.

The TPS254900-Q1 integrates CDP detection protocol, used at a downstream port as the CDP controller to support CDP portable-device fast charge up to 1.5 A.

8.4.5 Client Mode

The TPS254900-Q1 device integrates client mode as shown in Figure 42. The internal power switch is OFF to block current flow from OUT to IN, and the signal switches are ON. This mode can be used for software upgrades from the USB port.



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Figure 42. Client-Mode Equivalent Circuit

Passing the IEC 61000-4-2 test for DP_IN and DM_IN requires connecting a discharge resistor to OUT during USB 2.0 high-speed enumeration. In client mode, because the power switch is OFF, OUT must be 5 V so that the device can work normally (usually powered by an external downstream USB port). If the OUT voltage is low, the communication may not work properly.

8.4.6 High-Bandwidth Data-Line Switch

The D+ and D– data lines pass through the device to enable monitoring and handshaking while supporting the charging operation. A wide-bandwidth signal switch allows data to pass through the device without corrupting signal integrity. The data-line switches are turned on in any of the CDP, SDP or client operating modes. The EN input must be at logic high for the data-line switches to be enabled.

NOTE

- While in CDP mode, the data switches are ON, even during CDP handshaking.
 - The data switches are only for the USB-2.0 differential pair. In the case of a USB-3.0 host, the super-speed differential pairs must be routed directly to the USB connector without passing through the TPS254900-Q1 device.
 - Data switches are OFF during OUT (V_{BUS}) discharge.
-

9 Application and Implementation

NOTE

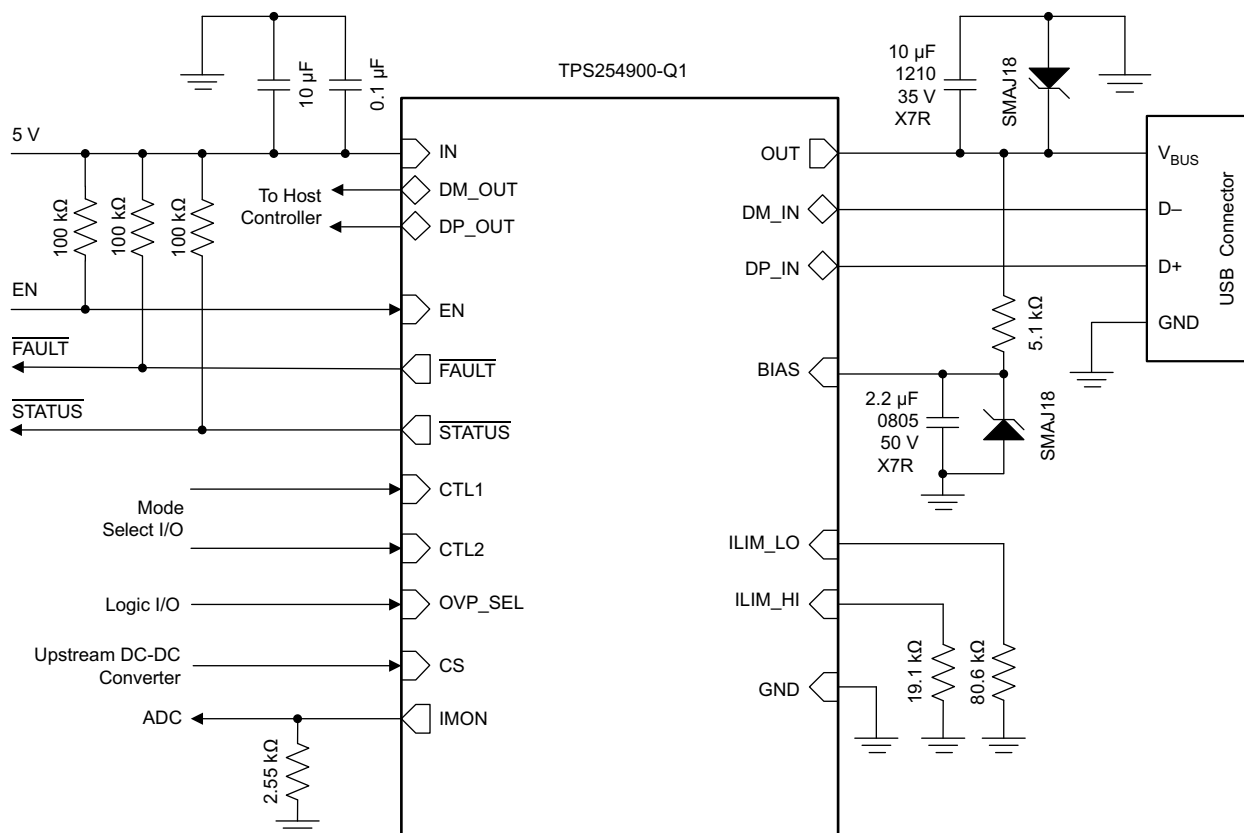
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS254900-Q1 device is a USB charging-port controller and power switch with cable compensation and short-to-battery protection for V_{BUS} , D+, and D-. The device is typically used for automotive USB port protection and as a USB charging controller. The following design procedure can be used to select components for the TPS254900-Q1. This section presents a simplified discussion of how to choose external components for V_{BUS} , D+, and D- short-to-battery protection. For cable-compensation design information, see the data sheet ([SLUSCE3](#)) for the TPS2549-Q1 device, which has features and design considerations very similar to those of the TPS254900-Q1 device.

9.2 Typical Application

For an automotive USB charging port, the V_{BUS} , D+, and D- pins are exposed and require a protection device. The protection required includes V_{BUS} overcurrent, D+ and D- ESD protection, and short-to-battery protection. This charging-port device protects the upstream dc-dc converter (bus line) and automotive SOC or hub chips (D+ and D- data lines). An application schematic of this circuit with short-to-battery protection is shown in [Figure 43](#).



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Figure 43. Typical Application Schematic: USB Port Charging With Cable Compensation

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

| DESIGN PARAMETER | EXAMPLE VALUE |
|------------------------------|---------------|
| Battery voltage, $V_{(BAT)}$ | 18 V |
| Short-circuit cable | 0.5 m |

9.2.2 Detailed Design Procedure

To begin the design process, the designer must know the following:

- The battery voltage
- The short-circuit cable length
- The maximum continuous output current for the charging port. The minimum current-limit setting of TPS254900-Q1 device must be higher than this current.
- The maximum output current of the upstream dc-dc converter. The maximum current-limit setting of TPS254900-Q1 device must be lower than this current.
- For cable compensation, the total resistance including power switch $r_{DS(on)}$, cable resistance, and connector contact resistance must be specified.

9.2.2.1 Input Capacitance

Consider the following application situations when choosing the input capacitors.

For all applications, TI recommends a 0.1- μ F or greater ceramic bypass capacitor between IN and GND, placed as close as possible to the device for local noise decoupling.

During output short or hot plug-in of a capacitive load, high current flows through the TPS254900-Q1 device back to the upstream dc-dc converter until the TPS254900-Q1 device responds (after $t_{(IOS)}$). During this response time, the TPS254900-Q1 input capacitance and the dc-dc converter output capacitance source current to keep V_{IN} above the UVLO of the TPS254900-Q1 device and any shared circuits. Size the input capacitance for the expected transient conditions and keep the path between the TPS254900-Q1 device and the dc-dc converter short to help minimize voltage drops.

Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power-bus inductance and input capacitance when the IN pin is in the high-impedance state (before turnon). Theoretically, the peak voltage is 2 times the applied voltage. The second cause is due to the abrupt reduction of output short-circuit current when the TPS254900-Q1 device turns off and energy stored in the input inductance drives the input voltage high. Applications with large input inductance (for example, a connection between the evaluation board and the bench power supply through long cables) may require large input capacitance to prevent the voltage overshoot from exceeding the absolute-maximum voltage of the device.

During the short-to-battery (EN = HIGH) condition, the input voltage follows the output voltage until OVP protection is triggered ($t_{(OV_OUT)}$). After the TPS254900-Q1 device responds and turns off the power switch, the stored energy in the input inductance can cause ringing.

Based on the three situations described, 10- μ F and 0.1- μ F low-ESR ceramic capacitors, placed close to the input, are recommended.

9.2.2.2 Output Capacitance

Consider the following application situations when choosing the output capacitors.

After an output short occurs, the TPS254900-Q1 device abruptly reduces the OUT current, and the energy stored in the output power-bus inductance causes voltage undershoot and potentially reverse voltage as it discharges.

Applications with large output inductance (such as from a cable) benefit from the use of a high-value output capacitor to control the voltage undershoot.

For USB port applications, because the V_{BUS} pin is exposed to IEC61000-4-2 level-4 ESD, use a low-ESR capacitance to protect OUT.

The TPS254900-Q1 device is capable of handling up to 18-V battery voltage. When V_{BUS} is shorted to the battery, the LCR tank circuit formed can induce ringing. The peak voltage seen on the OUT pin depends on the short-circuit cable length. The parasitic inductance and resistance varies with length, causing the damping factor and peak voltage to differ. Longer cables with larger resistance reduce the peak current and peak voltage. Consider high-voltage derating for the ceramic capacitor, because the peak voltage can be higher than twice the battery voltage.

Based on the three situations described, a 10- μ F, 35-V, X7R, 1210 low-ESR ceramic capacitor placed close to OUT is recommended. If the battery voltage is 16 V and a 16-V transient voltage suppressor (TVS) is used, then the capacitor voltage can be reduced to 25 V. Considering temperature variation, placing an additional 35-V aluminum electrolytic capacitor can lower the peak voltage and make the system more robust.

9.2.2.3 BIAS Capacitance

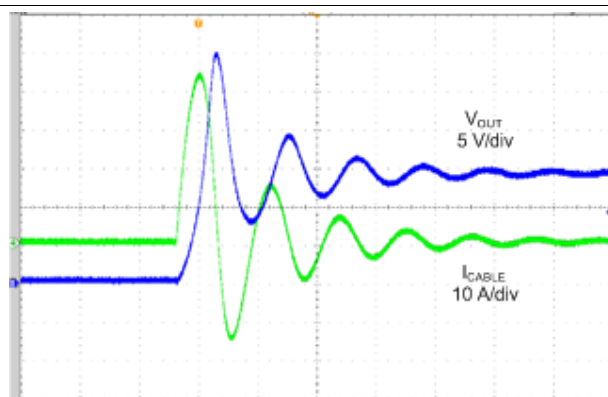
The capacitance on the BIAS pin helps the IEC ESD performance on the DM_IN and DP_IN pins.

When a short to battery on DP_IN, DM_IN and/or OUT occurs, high voltage can be seen on the BIAS pin. Place a 2.2- μ F, 50-V, X7R, 0805, low-ESR ceramic capacitor close to the BIAS pin. The whole current path from BIAS to GND should be as short as possible. Additionally, use a 5.1-k Ω discharge resistor from BIAS to OUT.

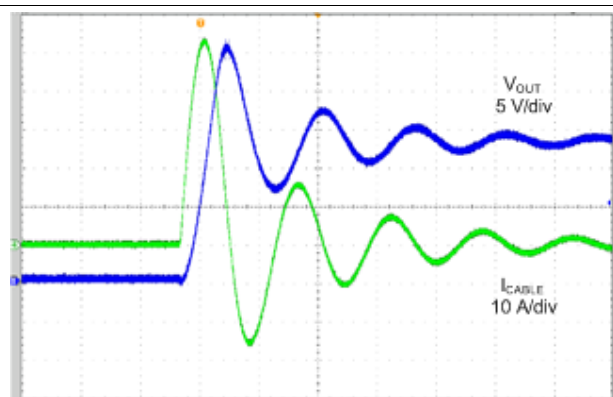
9.2.2.4 Output and BIAS TVS

The TPS254900-Q1 device can withstand high transient voltages due to LCR tank ringing, but in order to make OUT, DP_IN, and DM_IN robust, place one TVS close to the OUT pin, and another TVS close to the BIAS pin. When choosing the TVS, the reverse standoff voltage V_R depends on the battery voltage (16 V or 18 V). Considering the peak pulse power capability, a 400-W device is recommended such as an SMAJ16 for a 16-V battery or an SMAJ18 for an 18-V battery.

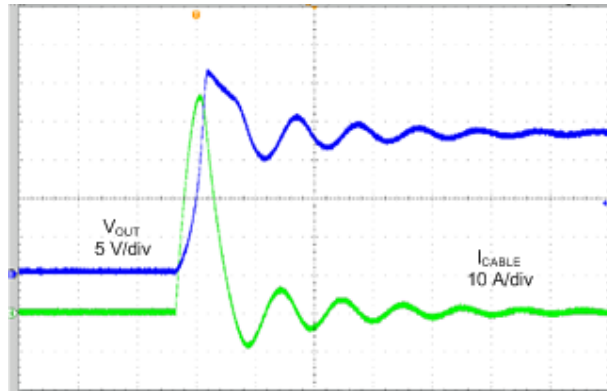
9.2.3 Application Curves



$V_{BAT} = 14\text{ V}$ $t = 10\text{ }\mu\text{s/div}$
Figure 44. Disabled, 25-V, 1206, X7R C_{OUT} Capacitor Without SMAJ18

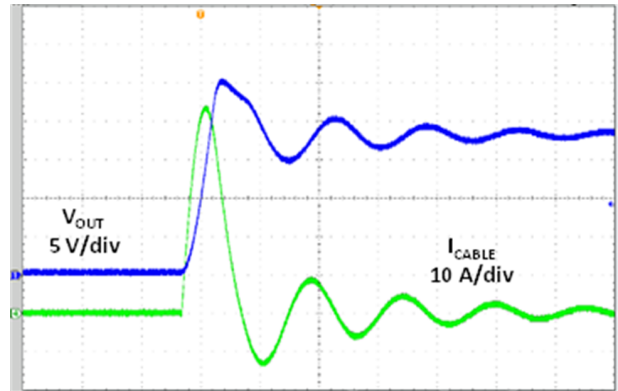


$V_{BAT} = 18\text{ V}$ $t = 10\text{ }\mu\text{s/div}$
Figure 45. Disabled, 35-V, 1210, X7R C_{OUT} Capacitor Without SMAJ18



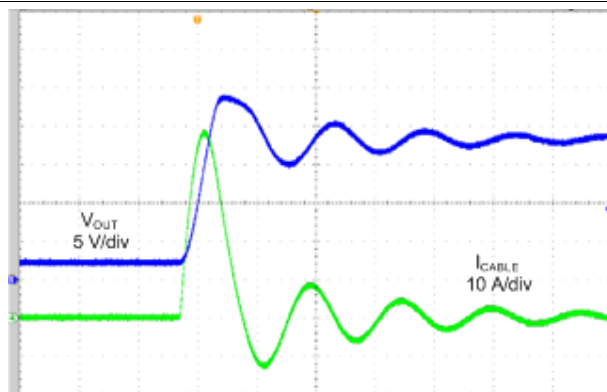
$t = 10 \mu\text{s/div}$

Figure 46. Disabled, 25-V, 1206, X7R C_{OUT} Capacitor With SMAJ18, OUT Shorted to Battery



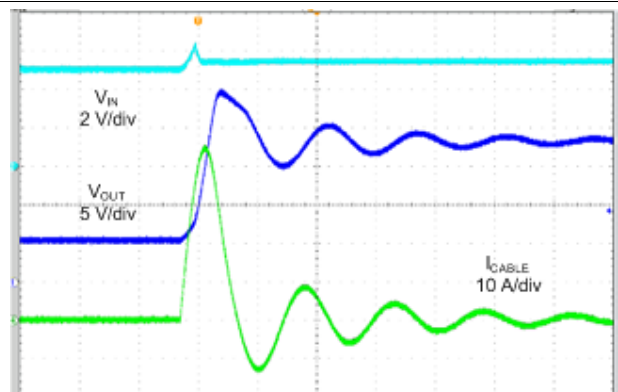
$t = 10 \mu\text{s/div}$

Figure 47. Disabled, 35-V, 1210, X7R C_{OUT} Capacitor With SMAJ18, OUT Shorted to Battery



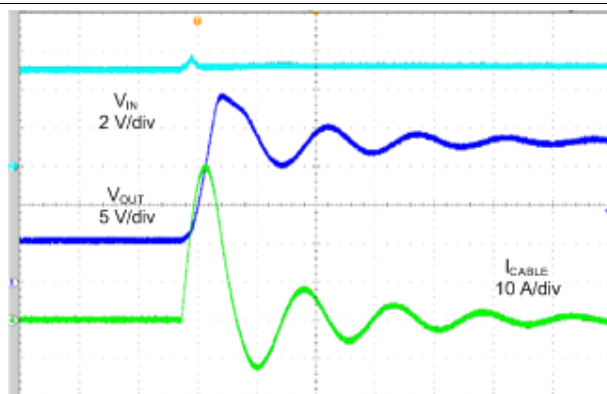
$t = 10 \mu\text{s/div}$

Figure 48. DC-DC Input Is Floating, OUT Shorted to Battery



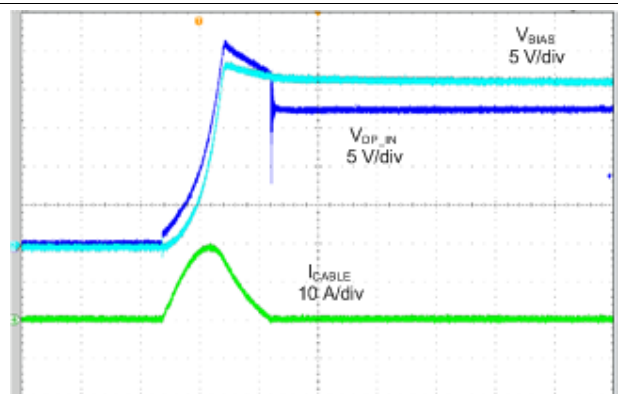
$t = 10 \mu\text{s/div}$

Figure 49. Enabled With OVP_SEL = High, OUT Shorted to Battery



$t = 10 \mu\text{s/div}$

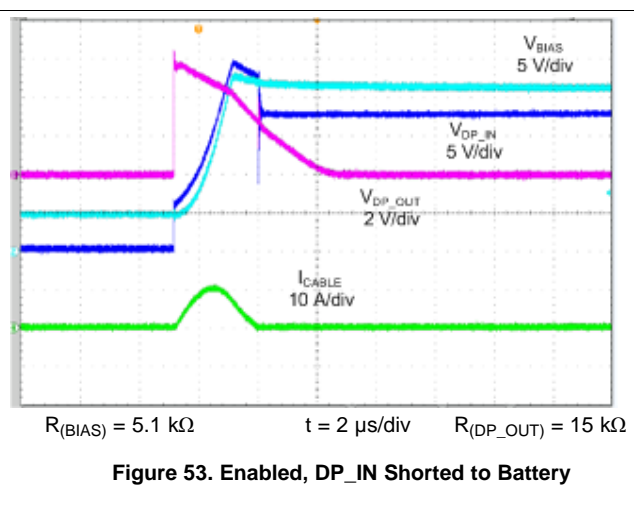
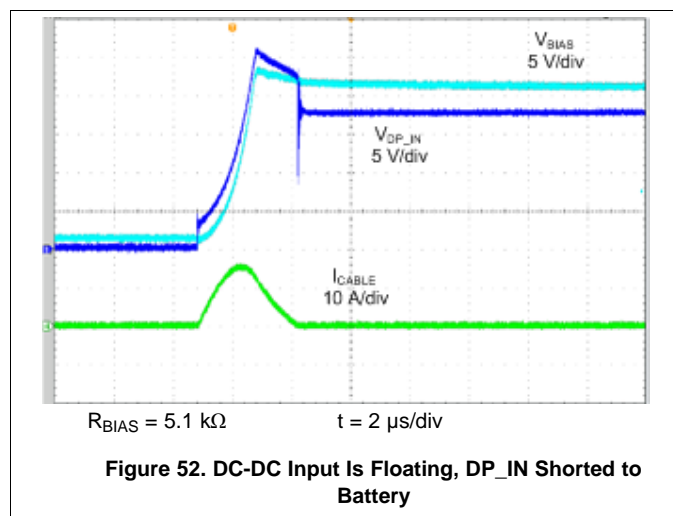
Figure 50. Enabled With OVP_SEL = Low, OUT Shorted to Battery



$R_{BIAS} = 5.1 \text{ k}\Omega$

$t = 2 \mu\text{s/div}$

Figure 51. Disabled, DP_IN Shorted to Battery



10 Power Supply Recommendations

The TPS254900-Q1 device is designed for a supply voltage range of $4.5 \text{ V} \leq V_{IN} \leq 6.5 \text{ V}$, with its power switch used for protecting the upstream power supply when a fault such as overcurrent or short to ground occurs on the USB port. Therefore, the power supply should be rated higher than the current-limit setting to avoid voltage drops during overcurrent or short-circuit conditions.

11 Layout

11.1 Layout Guidelines

Layout best practices for the TPS254900-Q1 are listed as follows.

- Considerations for input and output power traces
 - Make the power traces as short as possible.
 - Make the power traces as wide as possible.
- Considerations for input-capacitor traces
 - For all applications, 10- μF and 0.1- μF low-ESR ceramic capacitors are recommended, placed close to the IN pin.
- The resistors attached to the ILIM_HI and ILIM_LO pins of the device have several requirements.
 - It is recommended to use 1% low-temperature-coefficient resistors.
 - The trace routing between these two pins and GND should be as short as possible to reduce parasitic effects on current limit. These traces should not have any coupling to switching signals on the board.
- Locate all TPS254900-Q1 pullup resistors for open-drain outputs close to their connection pin. Pullup resistors should be 100 k Ω .
 - If a particular open-drain output is not used or needed in the system, tie it to GND.
- ESD considerations
 - The TPS254900-Q1 device has built-in ESD protection for DP_IN and DM_IN. Keep trace lengths minimal from the USB connector to the DP_IN and DM_IN pins on the TPS254900-Q1 device, and use minimal vias along the traces.
 - The capacitor on BIAS helps to improve the IEC ESD performance. A 2.2- μF capacitor should be placed close to BIAS, and the current path from BIAS to GND across this capacitor should be as short as possible. Do not use vias along the connection traces.
 - A 10- μF output capacitor should be placed close to the OUT pin and TVS.
 - See the *ESD Protection Layout Guide* (SLVA680) for additional information.
- TVS Considerations
 - For OUT, a TVS like SMAJ18 should be placed near the OUT pin.
 - For BIAS, a TVS like SMAJ18 should be placed close to the BIAS pin, but behind the 2.2- μF capacitor.

Layout Guidelines (continued)

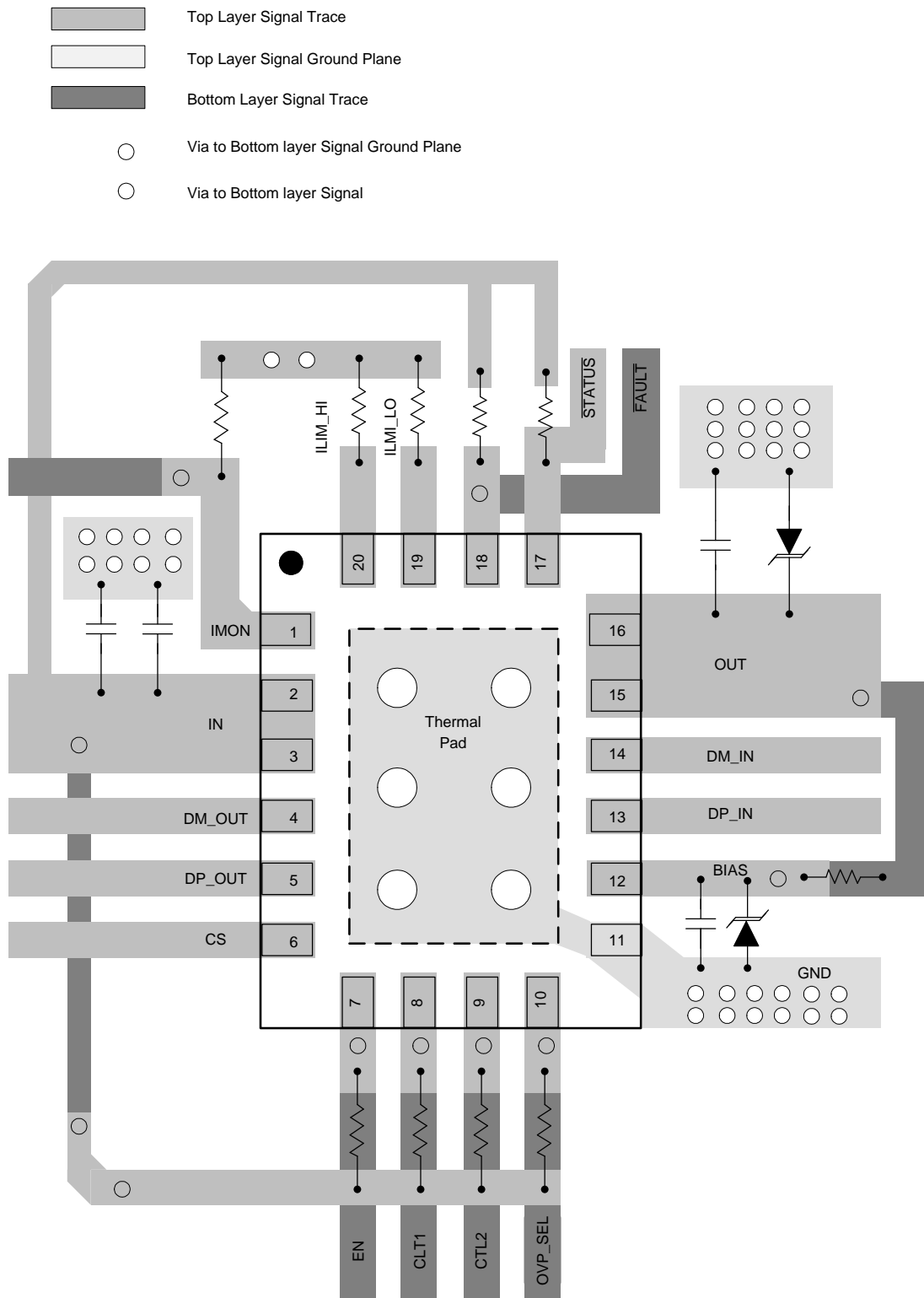
- The whole path from OUT to GND or BIAS to GND across the TVS should be as short as possible.
- DP_IN, DM_IN, DP_OUT, and DM_OUT routing considerations
 - Route these traces as microstrips with nominal differential impedance of 90 Ω .
 - Minimize the use of vias on the high-speed data lines.
 - Keep the reference GND plane devoid from cuts or splits above the differential pairs to prevent impedance discontinuities.
 - For more USB 2.0 high-speed D+ and D– differential routing information, see the *High Speed USB Platform Design Guideline* from Intel.
- Thermal Considerations
 - When properly mounted, the thermal-pad package provides significantly greater cooling ability than an ordinary package. To operate at rated power, the thermal pad must be soldered to the board GND plane directly under the device. The thermal pad is at GND potential and can be connected using multiple vias to inner-layer GND. Other planes, such as the bottom side of the circuit board, can be used to increase heat sinking in higher-current applications. See the *PowerPad™ Thermally Enhanced Package* application report (SLMA002) and *PowerPAD™ Made Easy* application brief (SLMA004) for more information on using this thermal pad package.

TPS254900-Q1

ZHCSFK7A – SEPTEMBER 2016 – REVISED OCTOBER 2016

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11.2 Layout Example



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Figure 54. TPS254900-Q1 Layout Diagram

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.2 文档支持

12.2.1 相关文档

《高速 USB 平台设计指南》，Intel

12.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

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12.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件提供的最新数据。本数据随时可能发生变更并且不对本文档进行修订，恕不另行通知。要获得这份数据表的浏览器版本，请查阅左侧的导航窗格。

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS254900IRVCRQ1 | Active | Production | WQFN (RVC) 20 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 254900Q |
| TPS254900IRVCRQ1.A | Active | Production | WQFN (RVC) 20 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 254900Q |
| TPS254900IRVCTQ1 | Active | Production | WQFN (RVC) 20 | 250 SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 254900Q |
| TPS254900IRVCTQ1.A | Active | Production | WQFN (RVC) 20 | 250 SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 254900Q |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS254900IRVCRQ1 | WQFN | RVC | 20 | 3000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |
| TPS254900IRVCTQ1 | WQFN | RVC | 20 | 250 | 180.0 | 12.4 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

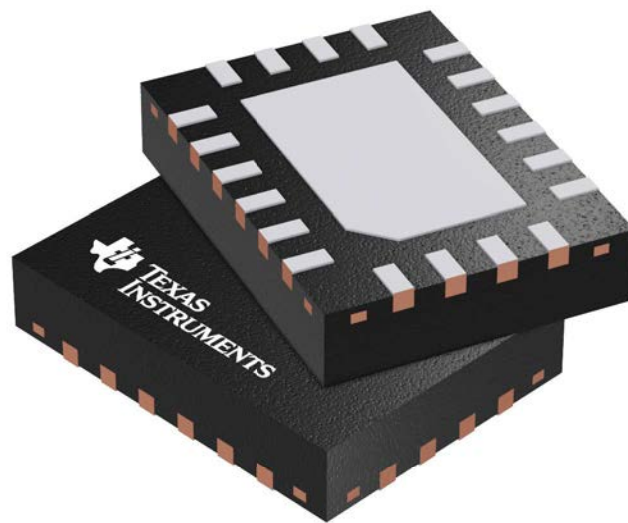
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS254900IRVCRQ1 | WQFN | RVC | 20 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS254900IRVCTQ1 | WQFN | RVC | 20 | 250 | 210.0 | 185.0 | 35.0 |

GENERIC PACKAGE VIEW

RVC 20

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4209819/B

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