

TPS22966-Q1 双通道、超低电阻负载开关

1 特性

- 符合汽车类应用 要求
- 具有符合 AEC-Q100 标准的下列特性：
 - 器件温度等级 2: -40°C 至 105°C 的环境工作温度范围
 - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H1C
 - 器件组件充电模式 (CDM) ESD 分类等级 C6
- 集成双通道负载开关
- 输入电压范围: 0V 至 5.5V
- 超低导通电阻 (R_{ON})
 - $V_{\text{IN}} = 5\text{V}$ ($V_{\text{BIAS}} = 5\text{V}$) 时, $R_{\text{ON}} = 16\text{m}\Omega$
 - $V_{\text{IN}} = 3.3\text{V}$ ($V_{\text{BIAS}} = 5\text{V}$) 时, $R_{\text{ON}} = 16\text{m}\Omega$
 - $V_{\text{IN}} = 1.8\text{V}$ ($V_{\text{BIAS}} = 5\text{V}$) 时, $R_{\text{ON}} = 16\text{m}\Omega$
- 每通道最大 4A 持续开关电流
- 低静态电流
 - $80\mu\text{A}$ (两个通道)
 - $80\mu\text{A}$ (单通道)
- 低控制输入阈值支持使用 1.2V 、 1.8V 、 2.5V 和 3.3V 逻辑器件
- 可配置的上升时间
- 快速输出放电 (QOD)
- 带有散热焊盘的 SON 14 引脚封装

2 应用

- 信息娱乐
- ADAS (高级驾驶辅助系统)

3 说明

TPS22966-Q1 器件是一款上升时间可调节的小型、超低 R_{ON} 双通道负载开关。此器件包含两个可在 0V 至 5.5V 输入电压范围内工作的 N 沟道 MOSFET，并且每通道支持最大 4A 的连续电流。每个开关由一个导通/关断输入 (ON1 和 ON2) 单独控制，此输入可与低电压控制信号直接连接。TPS22966-Q1 包含一个 230Ω 片上电阻，用于在开关关闭时快速输出放电。

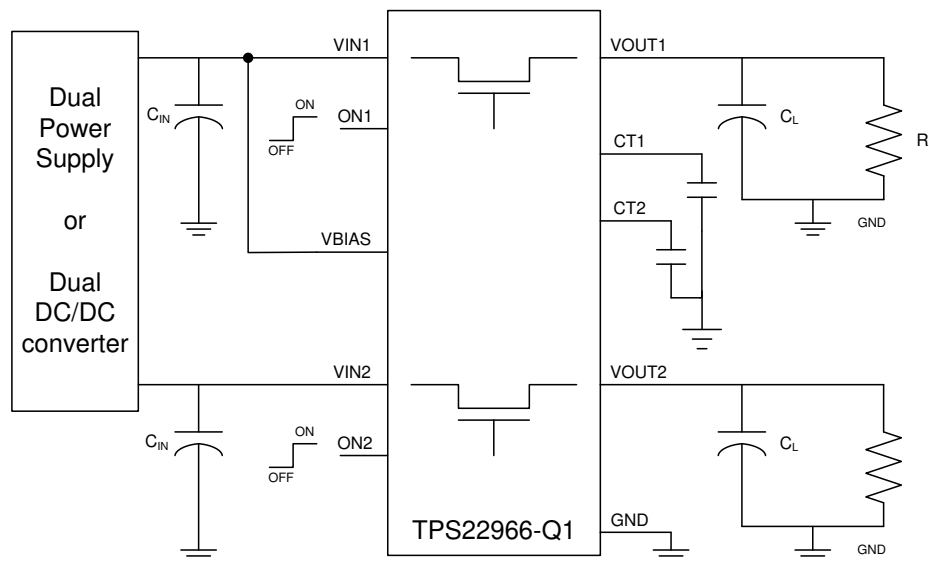
TPS22966-Q1 采用节省空间的 $2\text{mm} \times 3\text{mm}$ 14-SON 小型封装 (DPU)，带有集成散热焊盘，可实现较高的功率耗散。器件在自然通风环境下的额定运行温度范围为 -40°C 至 105°C 。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPS22966-Q1	WSO (14)	$3.00\text{mm} \times 2.00\text{mm}$

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用原理图



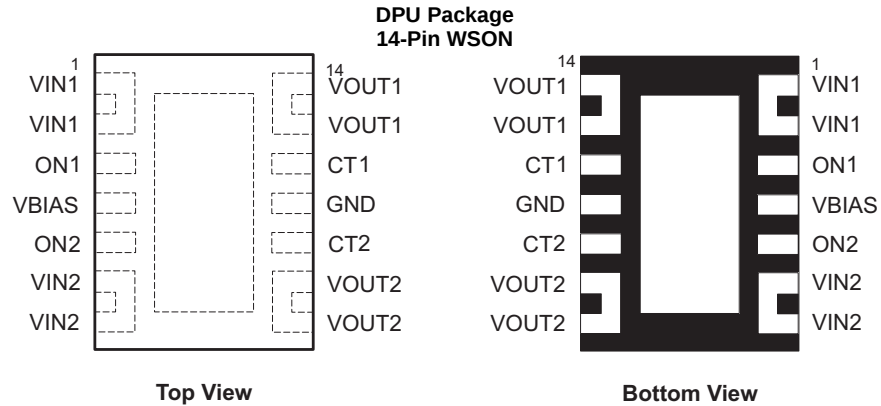
目录

1	特性	1	8.2	Functional Block Diagram	14
2	应用	1	8.3	Feature Description	15
3	说明	1	8.4	Device Functional Modes	15
4	修订历史记录	2	9	Application and Implementation	16
5	Pin Configuration and Functions	3	9.1	Application Information	16
6	Specifications	4	9.2	Typical Application	18
6.1	Absolute Maximum Ratings	4	10	Power Supply Recommendations	20
6.2	ESD Ratings	4	11	Layout	20
6.3	Recommended Operating Conditions	4	11.1	Layout Guidelines	20
6.4	Thermal Information	5	11.2	Layout Example	21
6.5	Electrical Characteristics: $V_{BIAS} = 5\text{ V}$	5	12	器件和文档支持	22
6.6	Electrical Characteristics: $V_{BIAS} = 2.5\text{ V}$	6	12.1	商标	22
6.7	Switching Characteristics	7	12.2	静电放电警告	22
6.8	Typical Characteristics	8	12.3	Glossary	22
7	Parameter Measurement Information	13	12.4	接收文档更新通知	22
8	Detailed Description	14	12.5	支持资源	22
8.1	Overview	14	13	机械、封装和可订购信息	22

4 修订历史记录

Changes from Revision A (March 2015) to Revision B		Page
•	Changed Input voltage range from 0.8 V to 0 V in the <i>Recommended Operating Conditions</i> table	4
Changes from Original (December 2013) to Revision A		Page
•	已添加 添加了引脚配置和功能 部分、ESD 额定值 表、特性 说明 部分、器件功能模式、应用和 实施 部分、电源建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN1	I	Switch 1 input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See Application Information section for more information.
2	VIN1	I	Switch 1 input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See Application Information for more information.
3	ON1	I	Active high switch 1 control input. Do not leave floating.
4	VBIAS	I	Bias voltage. Power supply to the device. See Application Information for more information.
5	ON2	I	Active high switch 2 control input. Do not leave floating.
6	VIN2	I	Switch 2 input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See Application Information for more information.
7	VIN2	I	Switch 2 input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See Application Information for more information.
8	VOUT2	O	Switch 2 output.
9	VOUT2	O	Switch 2 output.
10	CT2	O	Switch 2 slew rate control. Can be left floating. Capacitor used on this pin should be rated for a minimum of 25 V for desired rise time performance.
11	GND	–	Ground
12	CT1	O	Switch 1 slew rate control. Can be left floating. Capacitor used on this pin should be rated for a minimum of 25 V for desired rise time performance.
13	VOUT1	O	Switch 1 output.
14	VOUT1	O	Switch 1 output.
15	Thermal Pad	O	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See Layout Guidelines for layout guidelines.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{IN1,2}	Input voltage	−0.3	6	V
V _{OUT1,2}	Output voltage	−0.3	6	V
V _{ON1,2}	ON-pin voltage	−0.3	6	V
V _{BIAS}	VBIAS voltage	−0.3	6	V
I _{MAX}	Maximum continuous switch current per channel		4	A
I _{PLS}	Maximum pulsed switch current per channel, pulse <300 μs, 2% duty cycle		6	A
T _J	Maximum junction temperature		150	°C
T _{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
T _{STG}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V _{IN1,2}	Input voltage range		0	V _{BIAS}	V
V _{BIAS}	Bias voltage range		2.5	5.5	V
V _{ON1,2}	ON voltage range		0	5.5	V
V _{OUT1,2}	Output voltage range			V _{IN}	V
V _{IH}	High-level input voltage, ON	V _{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
V _{IL}	Low-level input voltage, ON	V _{BIAS} = 2.5 V to 5.5 V	0	0.5	V
C _{IN1,2}	Input capacitor		1 ⁽¹⁾		μF
T _A	Operating free-air temperature ⁽²⁾		−40	105	°C

- (1) Refer to [Application Information](#).
- (2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T_{A(max)}] is dependent on the maximum operating junction temperature [T_{J(max)}], the maximum power dissipation of the device in the application [P_{D(max)}], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: T_{A(max)} = T_{J(max)} − (θ_{JA} × P_{D(max)})

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22966-Q1	UNIT
		DPU (WSON)	
		14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	52.3	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance	45.9	
θ_{JB}	Junction-to-board thermal resistance	11.5	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	11.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6.9	

(1) 有关传统和新热指标的更多信息，请参见应用报告《半导体和 IC 封装热指标》（文献编号：SPRA953）。

6.5 Electrical Characteristics: $V_{BIAS} = 5\text{ V}$

Unless otherwise noted, the specifications apply over the operating ambient temperature, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ (full) and $V_{BIAS} = 5\text{ V}$. Typical values are for $T_A = 25^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS							
$I_{IN}(V_{BIAS-ON})$	V_{BIAS} quiescent current (both channels)	$I_{OUT1} = I_{OUT2} = 0\text{ mA}$, $V_{IN1,2} = V_{ON1,2} = V_{BIAS} = 5\text{ V}$	-40°C to 105°C		80	120	μA
$I_{IN}(V_{BIAS-ON})$	V_{BIAS} quiescent current (single channel)	$I_{OUT1} = I_{OUT2} = 0\text{ mA}$, $V_{ON2} = 0\text{ V}$ $V_{IN1,2} = V_{ON1} = V_{BIAS} = 5\text{ V}$	-40°C to 105°C		80	120	μA
$I_{IN}(V_{BIAS-OFF})$	V_{BIAS} shutdown current	$V_{ON1,2} = 0\text{ V}$, $V_{OUT1,2} = 0\text{ V}$	-40°C to 105°C			2	μA
$I_{IN}(V_{IN-OFF})$	$V_{IN1,2}$ off-state supply current (per channel)	$V_{ON1,2} = 0\text{ V}$, $V_{OUT1,2} = 0\text{ V}$	-40°C to 105°C		0.5	8	μA
					0.1	3	
					0.07	2	
					0.04	1	
I_{ON}	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$	-40°C to 105°C			1	μA
RESISTANCE CHARACTERISTICS							
R_{ON}	ON-state resistance (per channel)	$I_{OUT} = -200\text{ mA}$, $V_{BIAS} = 5\text{ V}$	$V_{IN} = 5\text{ V}$	25°C	16	19	m Ω
				-40°C to 85°C		21	
				-40°C to 105°C		23	
			$V_{IN} = 3.3\text{ V}$	25°C	16	19	
				-40°C to 85°C		21	
				-40°C to 105°C		23	
			$V_{IN} = 1.8\text{ V}$	25°C	16	19	
				-40°C to 85°C		21	
				-40°C to 105°C		23	
			$V_{IN} = 1.5\text{ V}$	25°C	16	19	
				-40°C to 85°C		21	
				-40°C to 105°C		23	
			$V_{IN} = 1.2\text{ V}$	25°C	16	19	
				-40°C to 85°C		21	
				-40°C to 105°C		23	
			$V_{IN} = 0.8\text{ V}$	25°C	16	19	
				-40°C to 85°C		21	
				-40°C to 105°C		23	
R_{PD}	Output pulldown resistance	$V_{IN} = 5.0\text{ V}$, $V_{ON} = 0\text{ V}$, $I_{OUT} = 15\text{ mA}$	-40°C to 105°C		230	330	Ω

6.6 Electrical Characteristics: $V_{BIAS} = 2.5\text{ V}$

Unless otherwise noted, the specifications apply over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ (full) and $V_{BIAS} = 2.5\text{ V}$. Typical values are for $T_A = 25^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T _A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
I _{IN(VBIAS-ON)}	V _{BIAS} quiescent current (both channels)	I _{OUT1} = I _{OUT2} = 0 mA, V _{IN1,2} = V _{ON1,2} = V _{BIAS} = 2.5 V		−40°C to 105°C		32	40	μA
I _{IN(VBIAS-ON)}	V _{BIAS} quiescent current (single channel)	I _{OUT1} = I _{OUT2} = 0 mA, V _{ON2} = 0 V V _{IN1,2} = V _{ON1} = V _{BIAS} = 2.5 V		−40°C to 105°C		32	40	μA
I _{IN(VBIAS-OFF)}	V _{BIAS} shutdown current	V _{ON1,2} = 0 V, V _{OUT1,2} = 0 V		−40°C to 105°C			2	μA
I _{IN(VIN-OFF)}	V _{IN1,2} off-state supply current (per channel)	V _{ON1,2} = 0 V, V _{OUT1,2} = 0 V	V _{IN1,2} = 2.5 V	−40°C to 105°C		0.13	3	μA
			V _{IN1,2} = 1.8 V			0.07	2	
			V _{IN1,2} = 1.2 V			0.05	2	
			V _{IN1,2} = 0.8 V			0.04	1	
I _{ON}	ON pin input leakage current	V _{ON} = 5.5 V		−40°C to 105°C			1	μA
RESISTANCE CHARACTERISTICS								
R _{ON}	ON-state resistance	I _{OUT} = −200 mA, V _{BIAS} = 2.5 V	V _{IN} = 2.5 V	25°C		21	24	mΩ
				−40°C to 85°C			27	
				−40°C to 105°C			29	
			V _{IN} = 1.8 V	25°C		19	22	
				−40°C to 85°C			25	
				−40°C to 105°C			27	
			V _{IN} = 1.5 V	25°C		18	21	
				−40°C to 85°C			24	
				−40°C to 105°C			26	
			V _{IN} = 1.2 V	25°C		18	21	
				−40°C to 85°C			24	
				−40°C to 105°C			26	
			V _{IN} = 0.8 V	25°C		17	20	
				−40°C to 85°C			23	
				−40°C to 105°C			25	
R _{PD}	Output pulldown resistance	V _{IN} = 2.5 V, V _{ON} = 0 V, I _{OUT} = 1 mA		Full		280	330	Ω

6.7 Switching Characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{IN} = V _{ON} = V _{BIAS} = 5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turnon time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		1559		μs
t _{OFF}	Turnoff time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		6		
t _R	V _{OUT} rise time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		1991		
t _F	V _{OUT} fall time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		2		
t _D	ON delay time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		665		
V _{IN} = 0.8 V, V _{ON} = V _{BIAS} = 5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turnon time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		732		μs
t _{OFF}	Turnoff time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		161		
t _R	V _{OUT} rise time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		371		
t _F	V _{OUT} fall time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		14		
t _D	ON delay time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		544		
V _{IN} = 2.5 V, V _{ON} = 5 V, V _{BIAS} = 2.5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turnon time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		2410		μs
t _{OFF}	Turnoff time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		7		
t _R	V _{OUT} rise time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		2412		
t _F	V _{OUT} fall time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		2		
t _D	ON delay time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		1181		
V _{IN} = 0.8 V, V _{ON} = 5 V, V _{BIAS} = 2.5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turnon time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		1575		μs
t _{OFF}	Turnoff time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		124		
t _R	V _{OUT} rise time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		927		
t _F	V _{OUT} fall time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		14		
t _D	ON delay time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		1089		

6.8 Typical Characteristics

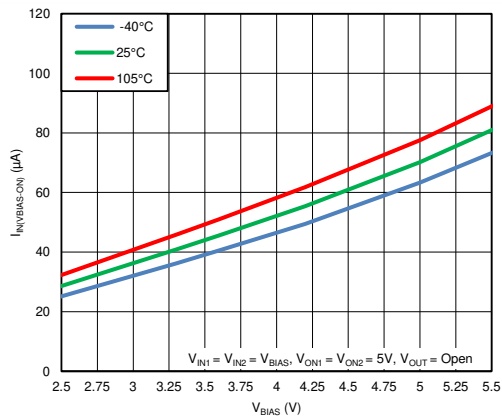


图 1. Quiescent Current vs. V_{BIAS} (Both Channels)

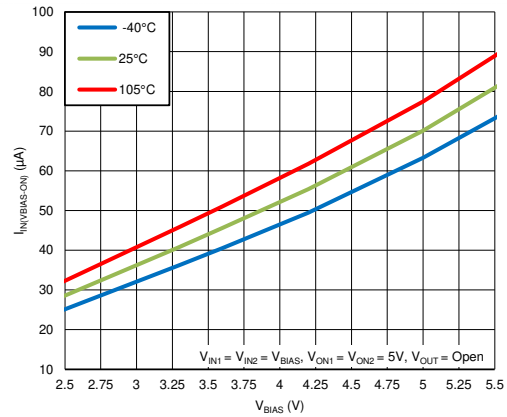


图 2. Quiescent Current vs. V_{BIAS} (Single Channel)

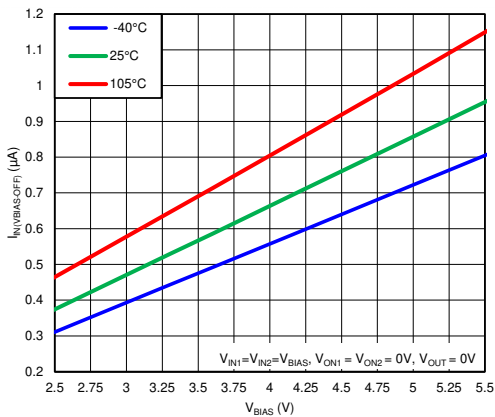


图 3. Shutdown Current vs. V_{BIAS} (Both Channels)

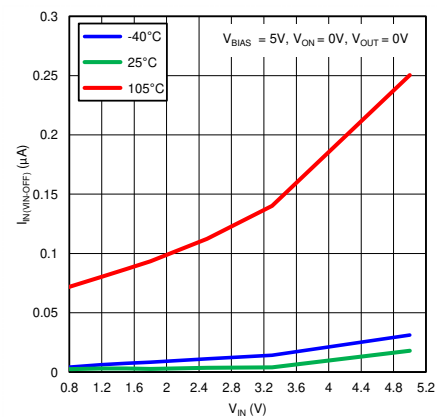


图 4. Off-State V_{IN} Current vs. V_{IN} (Single Channel)

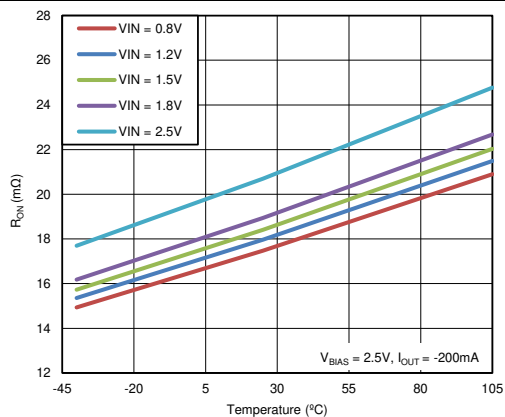


图 5. R_{ON} vs. Temperature ($V_{BIAS} = 2.5$ V, Single Channel)

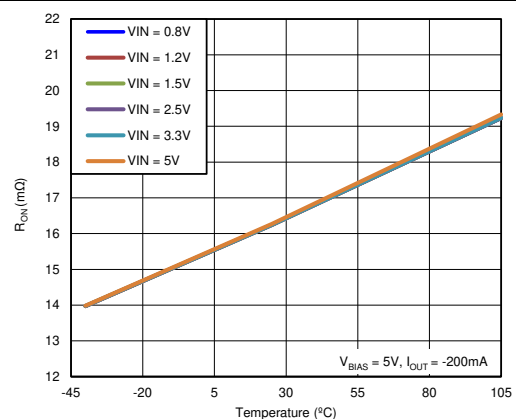


图 6. R_{ON} vs. Temperature ($V_{BIAS} = 5$ V, Single Channel)

Typical Characteristics (接下页)

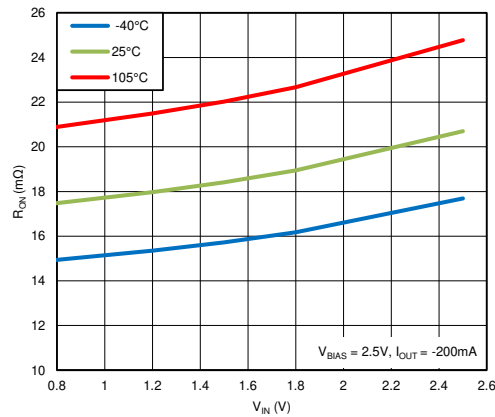


图 7. R_{ON} vs. V_{IN} ($V_{BIAS} = 2.5$ V, Single Channel)

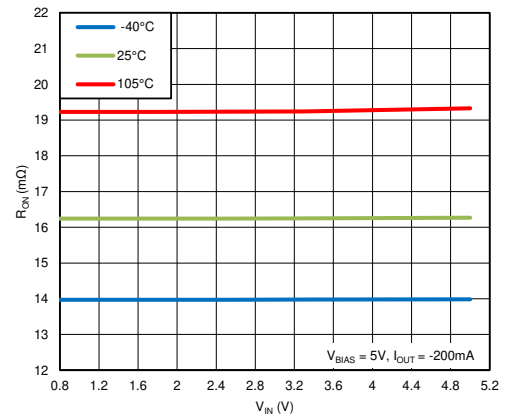


图 8. R_{ON} vs. V_{IN} ($V_{BIAS} = 5$ V, Single Channel)

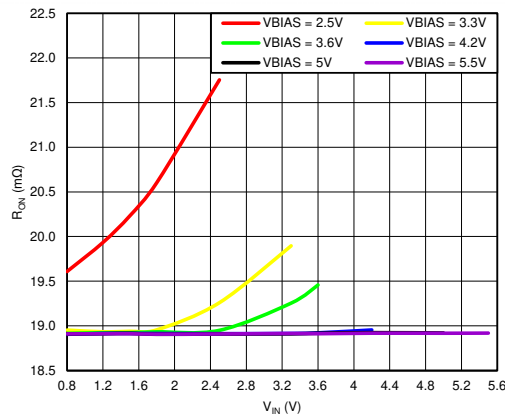


图 9. R_{ON} vs. V_{IN} ($T_A = 25^\circ\text{C}$, Single Channel)

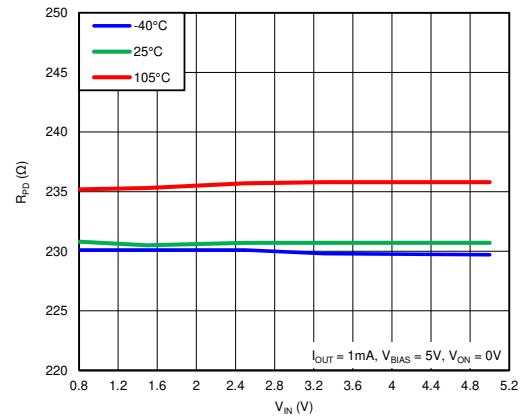


图 10. R_{PD} vs. V_{IN} ($V_{BIAS} = 5$ V, Single Channel)

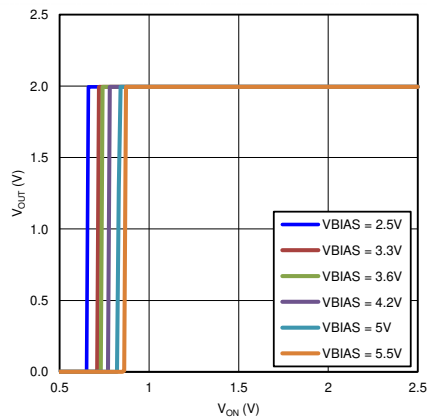


图 11. V_{OUT} vs. V_{ON} ($T_A = 25^\circ\text{C}$, Single Channel)

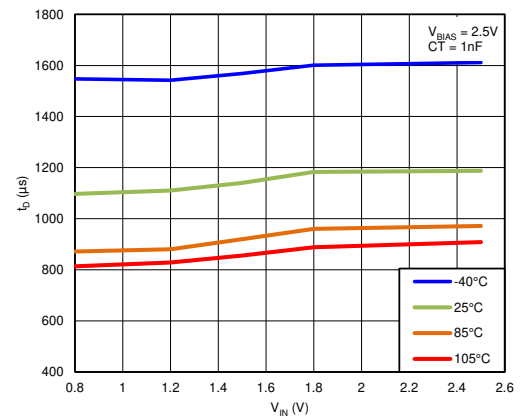


图 12. t_D vs. V_{IN} ($V_{BIAS} = 2.5$ V, $C_T = 1$ nF)

Typical Characteristics (接下页)

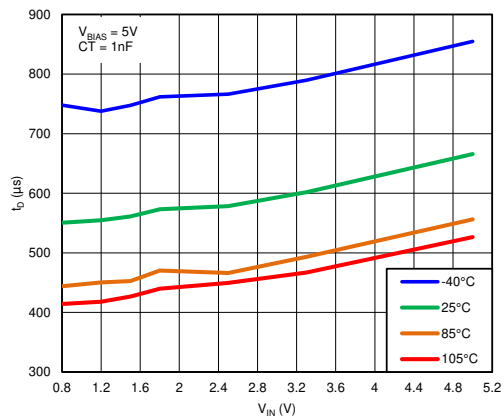


图 13. t_D vs. V_{IN} ($V_{BIAS} = 5\text{ V}$, $C_T = 1\text{ nF}$)

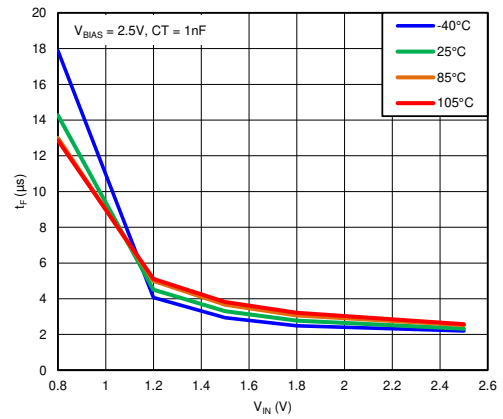


图 14. t_F vs. V_{IN} ($V_{BIAS} = 2.5\text{ V}$, $C_T = 1\text{ nF}$)

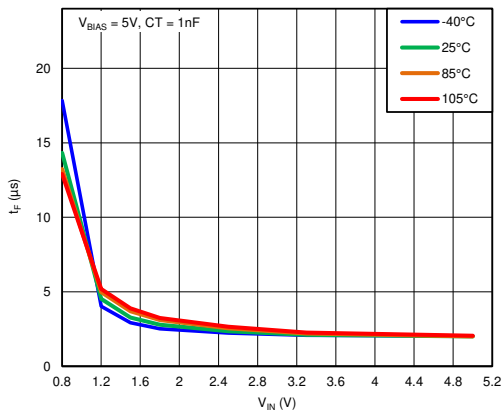


图 15. t_F vs. V_{IN} ($V_{BIAS} = 5\text{ V}$, $C_T = 1\text{ nF}$)

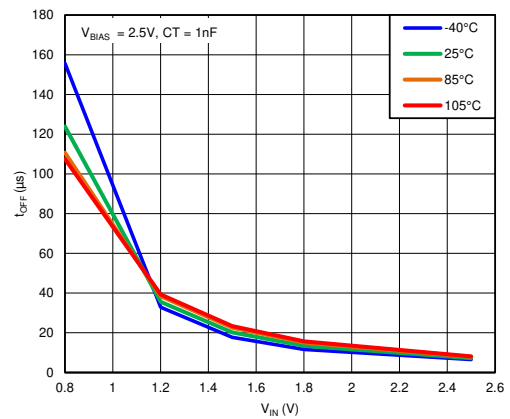


图 16. t_{OFF} vs. V_{IN} ($V_{BIAS} = 2.5\text{ V}$, $C_T = 1\text{ nF}$)

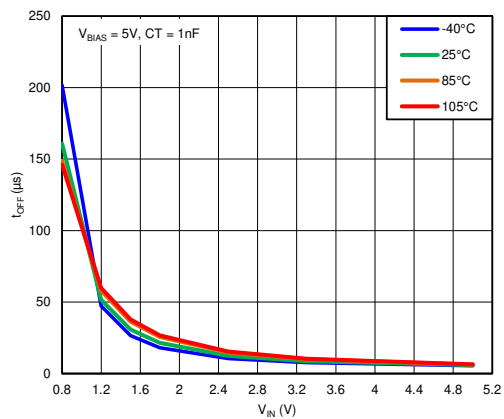


图 17. t_{OFF} vs. V_{IN} ($V_{BIAS} = 5\text{ V}$, $C_T = 1\text{ nF}$)

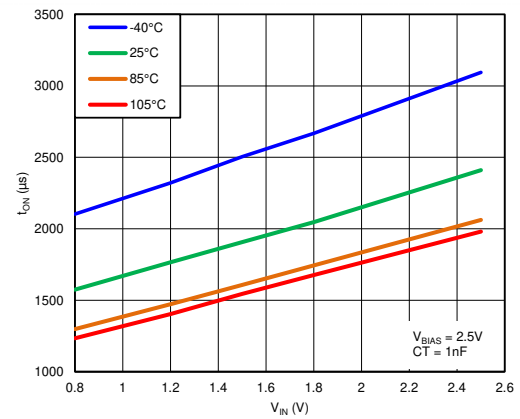


图 18. t_{ON} vs. V_{IN} ($V_{BIAS} = 2.5\text{ V}$, $C_T = 1\text{ nF}$)

Typical Characteristics (接下页)

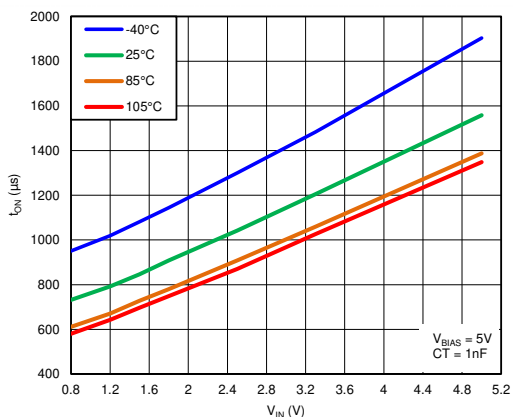


图 19. t_{ON} vs. V_{IN} ($V_{BIAS} = 5\text{ V}$, $CT = 1\text{ nF}$)

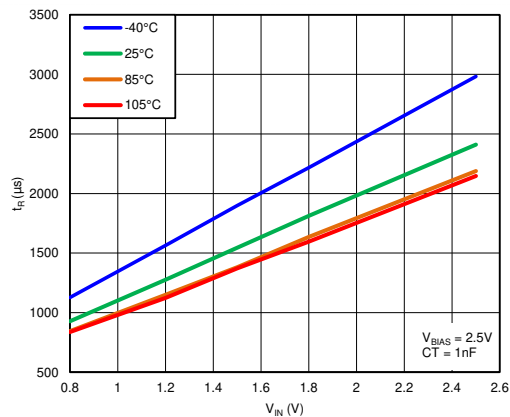


图 20. t_R vs. V_{IN} ($V_{BIAS} = 2.5\text{ V}$, $CT = 1\text{ nF}$)

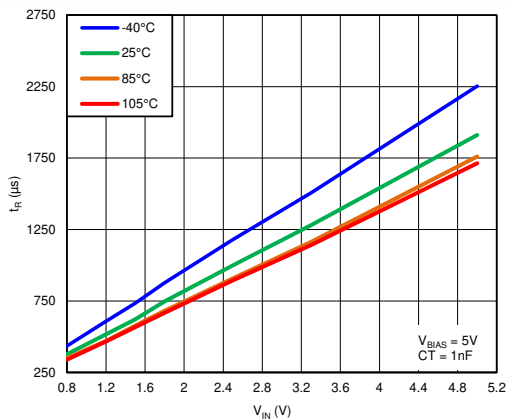


图 21. t_R vs. V_{IN} ($V_{BIAS} = 5\text{ V}$, $CT = 1\text{ nF}$)

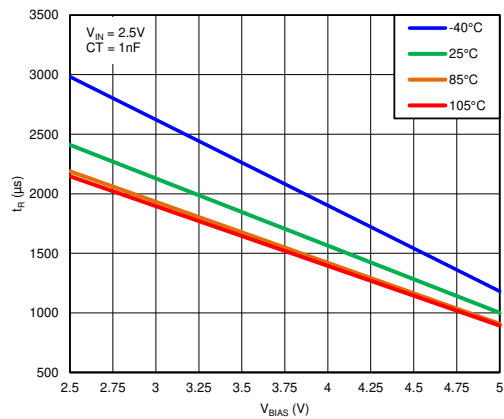


图 22. t_R vs. V_{BIAS} ($V_{IN} = 2.5\text{ V}$, $CT = 1\text{ nF}$)

6.8.1 Typical AC Scope Captures at $T_A = 25^\circ\text{C}$, $CT = 1\text{ nF}$

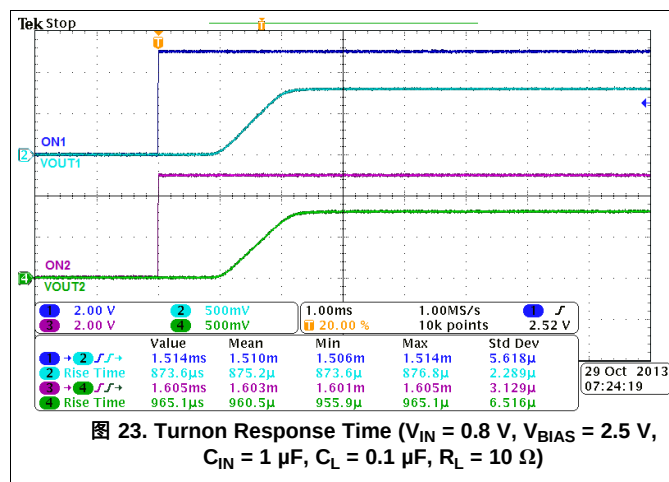


图 23. Turnon Response Time ($V_{IN} = 0.8\text{ V}$, $V_{BIAS} = 2.5\text{ V}$, $C_{IN} = 1\text{ μF}$, $C_L = 0.1\text{ μF}$, $R_L = 10\text{ Ω}$)

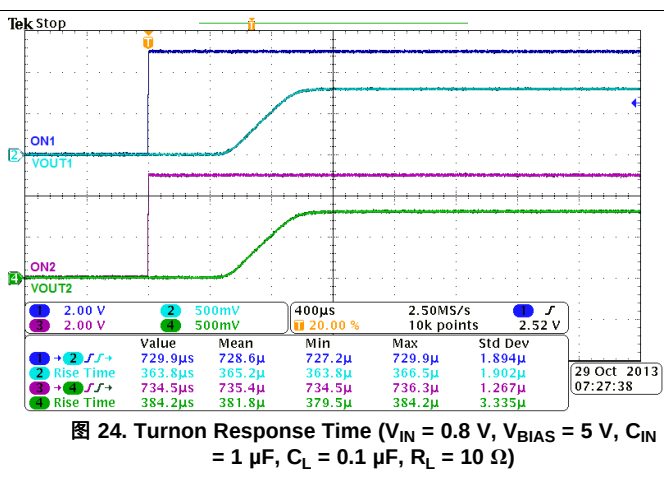


图 24. Turnon Response Time ($V_{IN} = 0.8\text{ V}$, $V_{BIAS} = 5\text{ V}$, $C_{IN} = 1\text{ μF}$, $C_L = 0.1\text{ μF}$, $R_L = 10\text{ Ω}$)

Typical AC Scope Captures at $T_A = 25^\circ\text{C}$, $C_T = 1\text{ nF}$ (接下页)

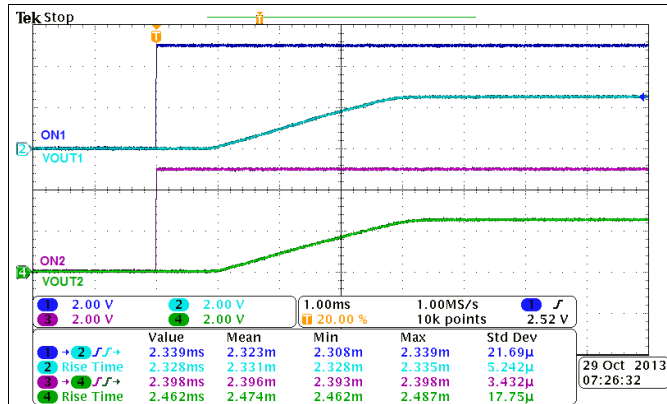


图 25. Turnon Response Time ($V_{IN} = 2.5\text{ V}$, $V_{BIAS} = 2.5\text{ V}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

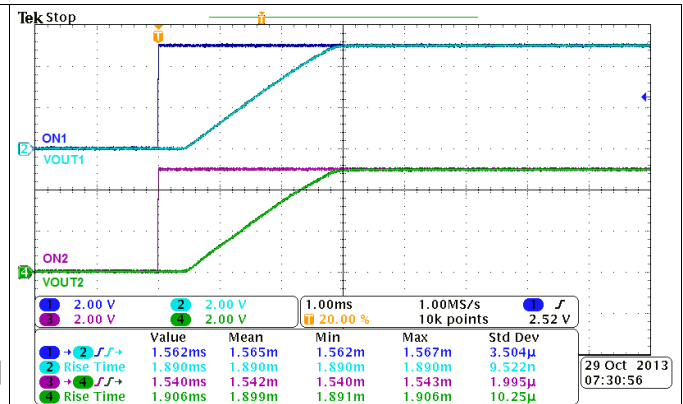


图 26. Turnon Response Time ($V_{IN} = 5\text{ V}$, $V_{BIAS} = 5\text{ V}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

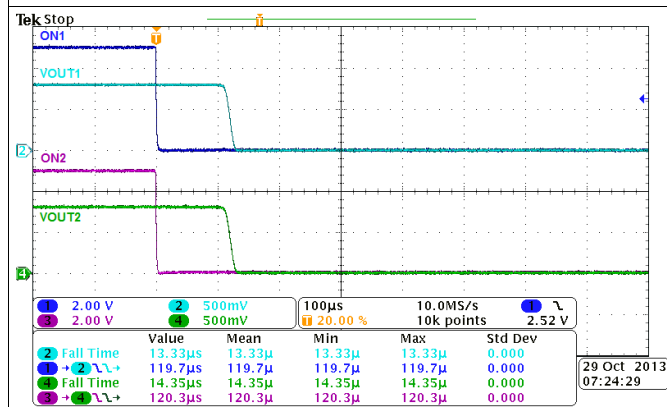


图 27. Turnoff Response Time ($V_{IN} = 0.8\text{ V}$, $V_{BIAS} = 2.5\text{ V}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

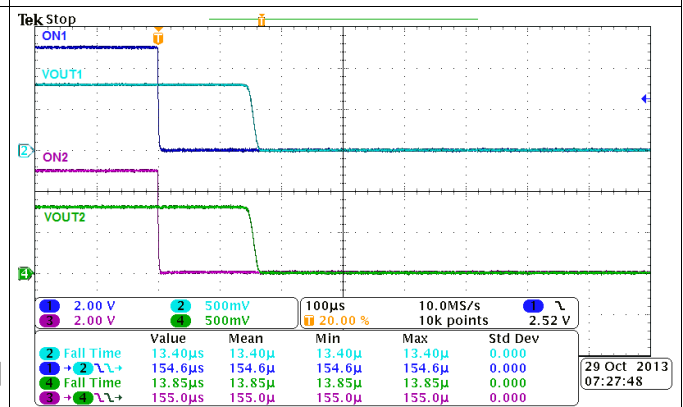


图 28. Turnoff Response Time ($V_{IN} = 0.8\text{ V}$, $V_{BIAS} = 5\text{ V}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

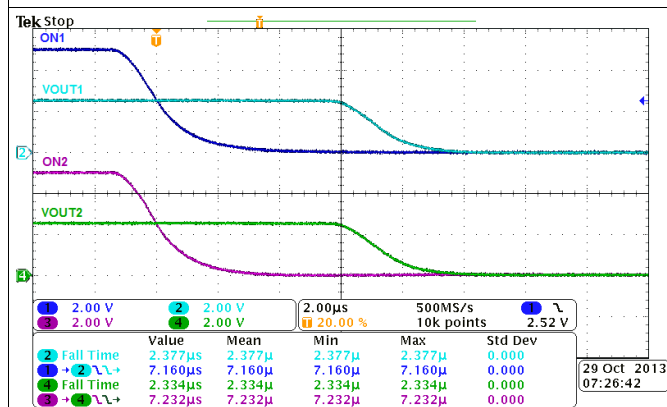


图 29. Turnoff Response Time ($V_{IN} = 2.5\text{ V}$, $V_{BIAS} = 2.5\text{ V}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

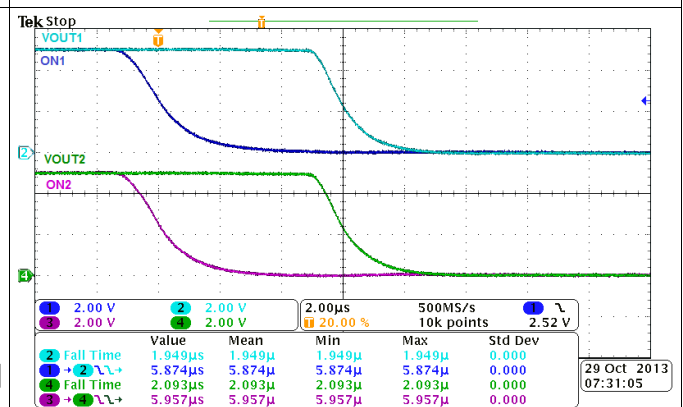
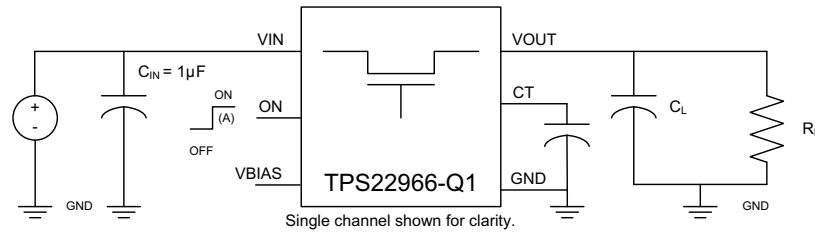
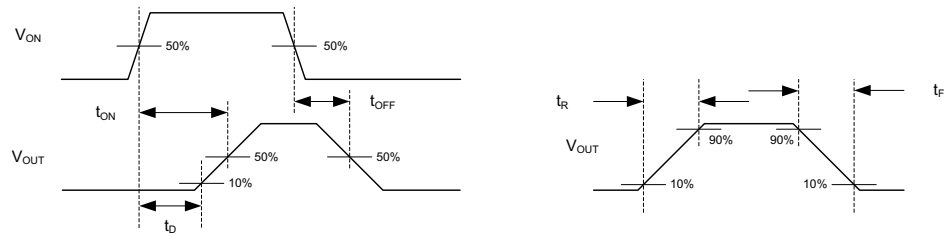


图 30. Turnoff Response Time ($V_{IN} = 5\text{ V}$, $V_{BIAS} = 5\text{ V}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

7 Parameter Measurement Information



TEST CIRCUIT



TIMING WAVEFORMS

(A) Control signal rise and fall times are 100 ns.

图 31. Test Circuit and Timing Waveforms

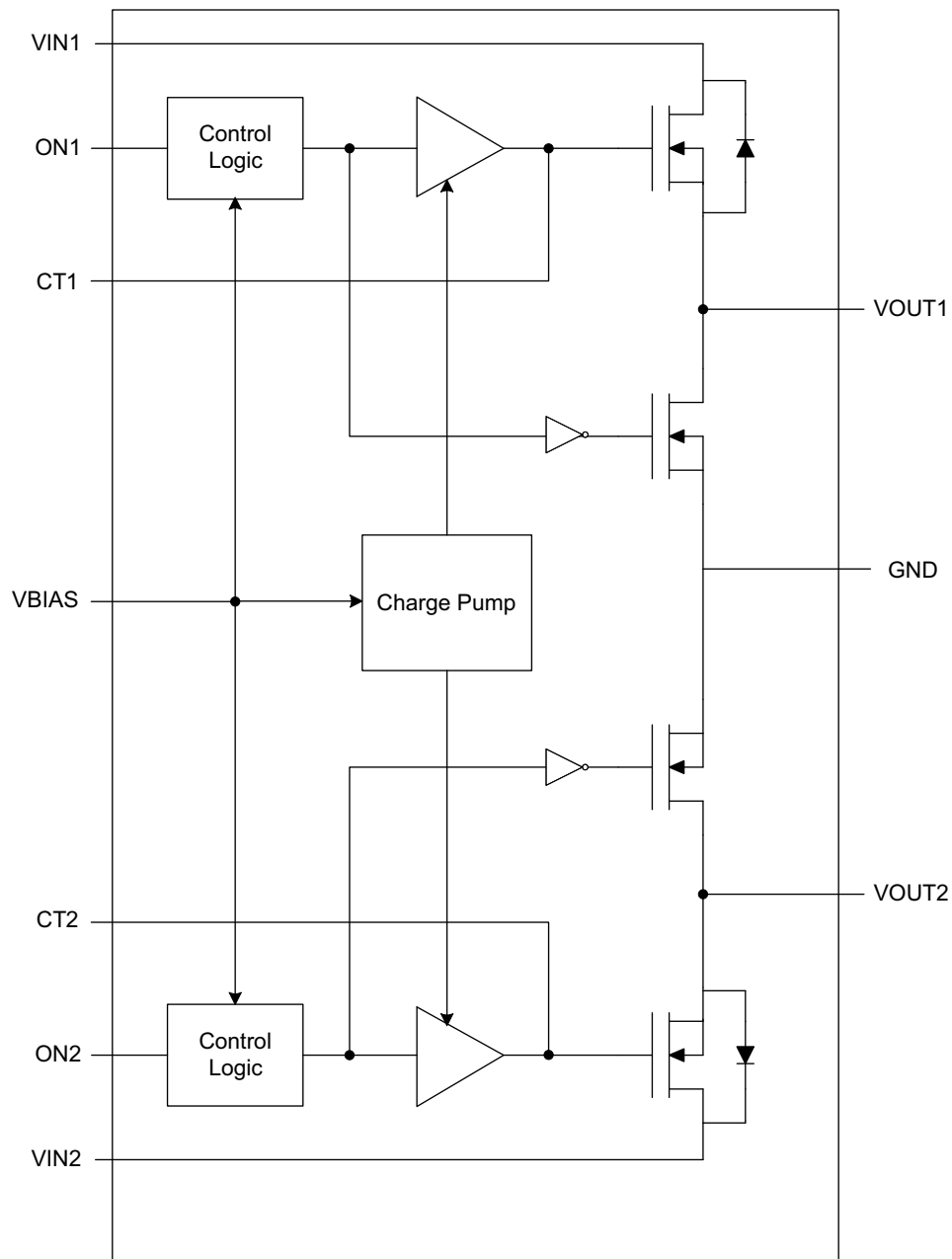
8 Detailed Description

8.1 Overview

The device is a dual-channel, 4-A automotive load switch in a 14-pin SON package. To reduce the voltage drop in high current rails, the device implements a low-resistance N-channel MOSFET.

The device has a programmable slew rate for applications that require specific rise-time. The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Quick Output Discharge

Each channel of the TPS22966-Q1 includes a Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 230-Ω and prevents the output from floating while the switch is disabled.

8.3.2 ON/OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

8.3.3 Adjustable Rise Time

A capacitor to GND on the CTx pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25 V should be used on the CTx pin. An approximate formula for the relationship between CTx and slew rate is (the equation below accounts for 10% to 90% measurement on VOUT and does **NOT** apply for CTx = 0 pF. Use 表 1 to determine rise times for when CTx = 0 pF):

$$SR = 0.32 \times CT + 13.7$$

where

- SR = slew rate (in μs/V)
- CT = the capacitance value on the CTx pin (in pF)
- The units for the constant 13.7 is in μs/V. (1)

Rise time can be calculated by multiplying the input voltage by the slew rate. 表 1 shows rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition, and the ON pin is asserted high.

表 1. Rise Time Values

CTx (pF)	RISE TIME (μs) 10% - 90%, CL = 0.1μF, CIN = 1μF, RL = 10Ω TYPICAL VALUES at 25°C, VBIAS = 5V, 25V X7R 10% CERAMIC CAP						
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V
0	124	88	63	60	53	49	42
220	481	323	193	166	143	133	109
470	855	603	348	299	251	228	175
1000	1724	1185	670	570	469	411	342
2200	3328	2240	1308	1088	893	808	650
4700	7459	4950	2820	2429	1920	1748	1411
10000	16059	10835	6040	5055	4230	3770	3033

8.4 Device Functional Modes

表 2. Functional Table

ONx	VINx to VOUTx	VOUTx to GND
L	Off	On
H	On	Off

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between VIN and GND. A 1- μ F ceramic capacitor, CIN, placed close to the pins, is usually sufficient. Higher values of CIN can be used to further reduce the voltage drop in high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.1.2 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a CIN greater than CL is highly recommended. A CL greater than CIN can cause VOUT to exceed VIN when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A CIN to CL ratio of 10 to 1 is recommended for minimizing VIN dip caused by inrush currents during start-up, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more VIN dip upon turnon due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see [Adjustable Rise Time](#)).

9.1.3 VIN and VBIAS Voltage Range

For optimal RON performance, make sure VIN $\leq$ VBIAS. The device will still be functional if VIN > VBIAS but it will exhibit RON greater than what is listed in [Electrical Characteristics](#). See [图 32](#) for an example of a typical device. Notice the increasing RON as VIN exceeds VBIAS voltage.

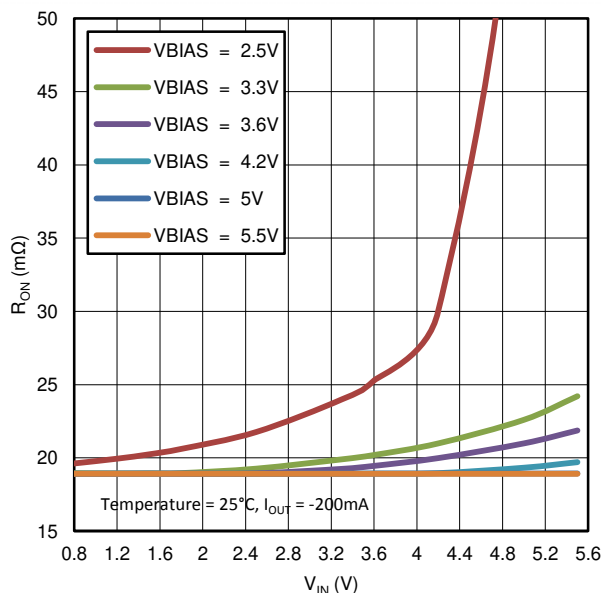


图 32. RON vs. VIN (Single Channel)

Application Information (接下页)

9.1.4 Safe Operating Area (SOA)

The SOA curves in 图 33 show the continuous current carrying capability of the device versus ambient temperature (T_A) to ensure reliable operation over 100,000 hours of device lifetime. Each curve represents a specific percent of time that the switch is on.

The 100% curve represents use for a full 24 hours in a day. The 75% curve indicates 18 hours of use in a day while the 12.5% curve shows 3 hours of use per day.

Examples on how to use this plot:

- The application has an ambient temperature of 60°C and the switch will be on 100% of the time. The maximum continuous current that can be applied is approximately 2.1 A.
- The application requires the switch to be on 12.5% of the time and the current while on will be 3 A. The maximum ambient temperature is approximately 100°C.
- The application requires 2 A and will be operated at 70°C. The switch can be on for a maximum of 75% of the time.
- It is expected that most applications will not have specific use cases as defined in the examples above. Different use cases can be combined to generate a more complete view of a specific application. This example shows use under various conditions simplified to an average use case. The application requires operation at 4 A for 25% of the time, 1 A for 25% of the time and is off the remaining 50% of the time. Ambient temperature will vary from 25°C to 50°C. Will there be any limitations? The average current can be calculated as $(4\text{ A} \times 25\% + 1\text{ A} \times 25\% + 0\text{ A} \times 50\%)$. The average current calculates to be 1.25 A. Assuming worst case temperature of 50°C, the resulting application is within the safe operating area.

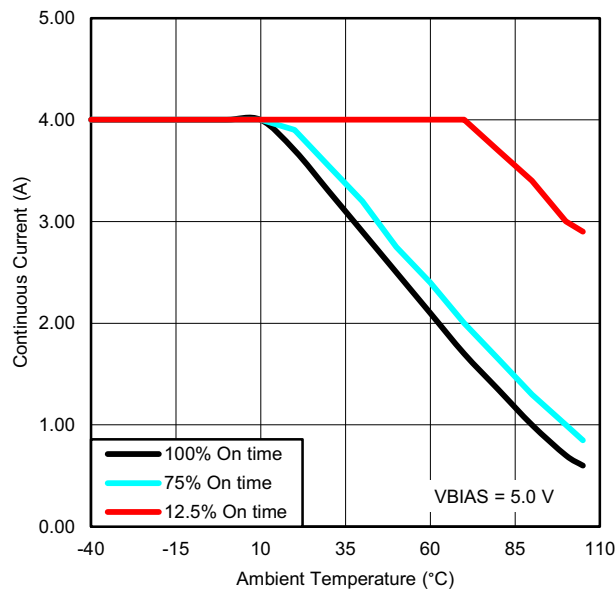


图 33. Safe Operating Area

9.2 Typical Application

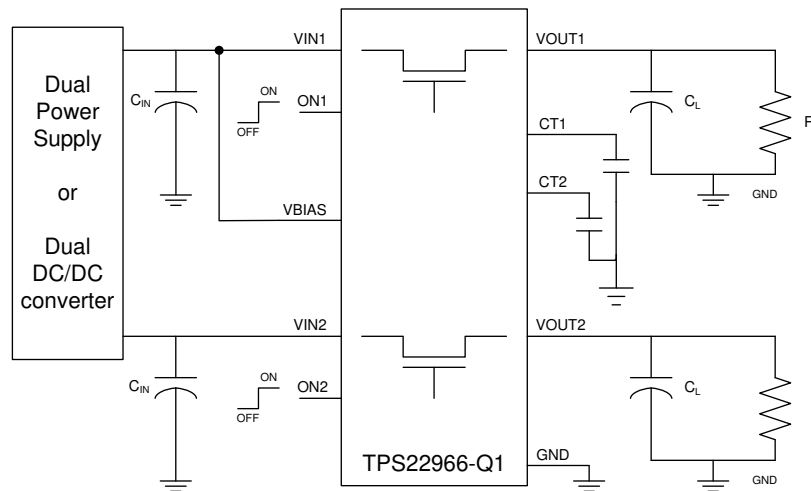


图 34. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 3 as the input parameters.

表 3. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage	3.3 V
Bias voltage	5 V
Load capacitance (CL)	22 μF
Maximum acceptable inrush current	400 mA

9.2.2 Detailed Design Procedure

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using 公式 2:

$$\text{Inrush Current} = C \times dV/dt$$

where

- C = output capacitance
 - dV = output voltage
 - dt = rise time
- (2)

The TPS22966-Q1 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turnon. The appropriate rise time can be calculated using 表 3 and the inrush current equation.

$$400 \text{ mA} = 22 \text{ μF} \times 3.3 \text{ V}/dt \quad (3)$$

$$dt = 181.5 \text{ μs} \quad (4)$$

To ensure an inrush current of less than 400 mA, choose a CT value that will yield a rise time of more than 181.5 μs. See the oscilloscope captures in for an example of how the CT capacitor can be used to reduce inrush current.

9.2.3 Application Curves

$V_{BIAS} = 5\text{ V}$; $V_{IN} = 3.3\text{ V}$; $C_L = 22\text{ }\mu\text{F}$

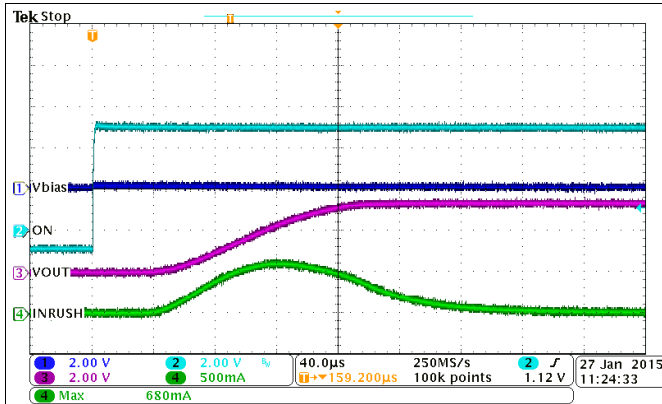


图 35. Inrush Current With $CT = 0\text{ pF}$

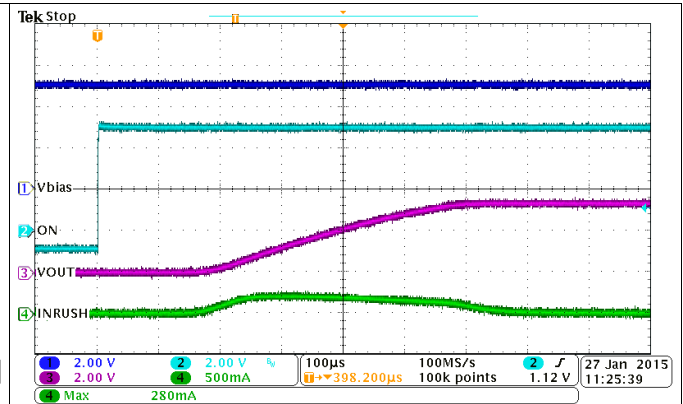


图 36. Inrush Current With $CT = 220\text{ pF}$

10 Power Supply Recommendations

The device is designed to operate from a VBIAS range of 2.5 V to 5.5 V and a VIN voltage range of 0 V to 5.5 V. The power supply should be well regulated and placed as close to the device terminals as possible. It must be able to withstand all transient and load current steps. In most situations, using an input capacitance of 1 uF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

The requirements for larger input capacitance can be mitigated by adding additional capacitance to the CT pin. This will cause the load switch to turn on more slowly. Not only will this reduce transient inrush current, but it will also give the power supply more time to respond to the load current step.

11 Layout

11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. To calculate the maximum allowable power dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}}$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (150°C for the TPS22966-Q1)
- T_A = ambient temperature
- θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout. (5)

 37 shows an example of a layout. Notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

11.2 Layout Example

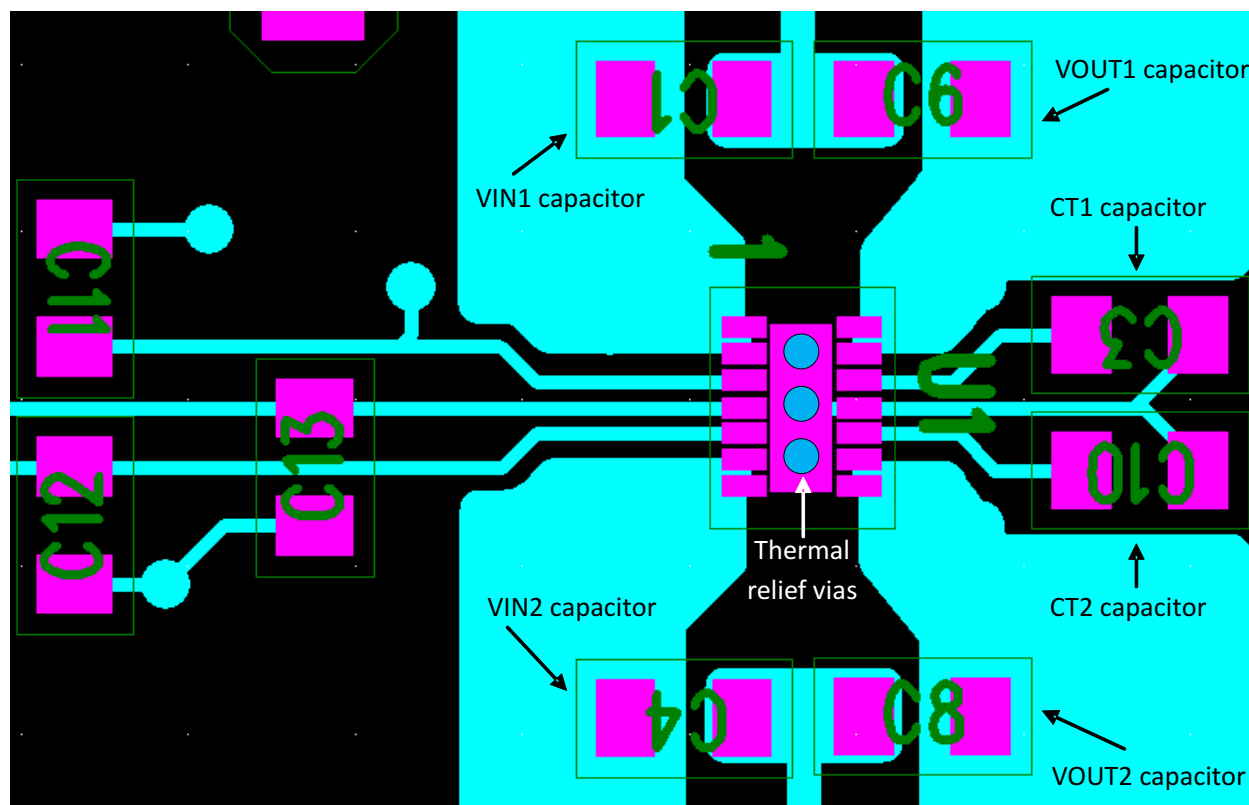


图 37. Layout Example

12 器件和文档支持

12.1 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.2 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12.4 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.5 支持资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22966TDPURQ1	Active	Production	WSO (DPU) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	966TQ1
TPS22966TDPURQ1.A	Active	Production	WSO (DPU) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	966TQ1
TPS22966TDPUTQ1	Active	Production	WSO (DPU) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	966TQ1
TPS22966TDPUTQ1.A	Active	Production	WSO (DPU) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	966TQ1

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS22966-Q1 :

- Catalog : [TPS22966](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22966TDPURQ1	WSO	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22966TDPURQ1	WSO	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

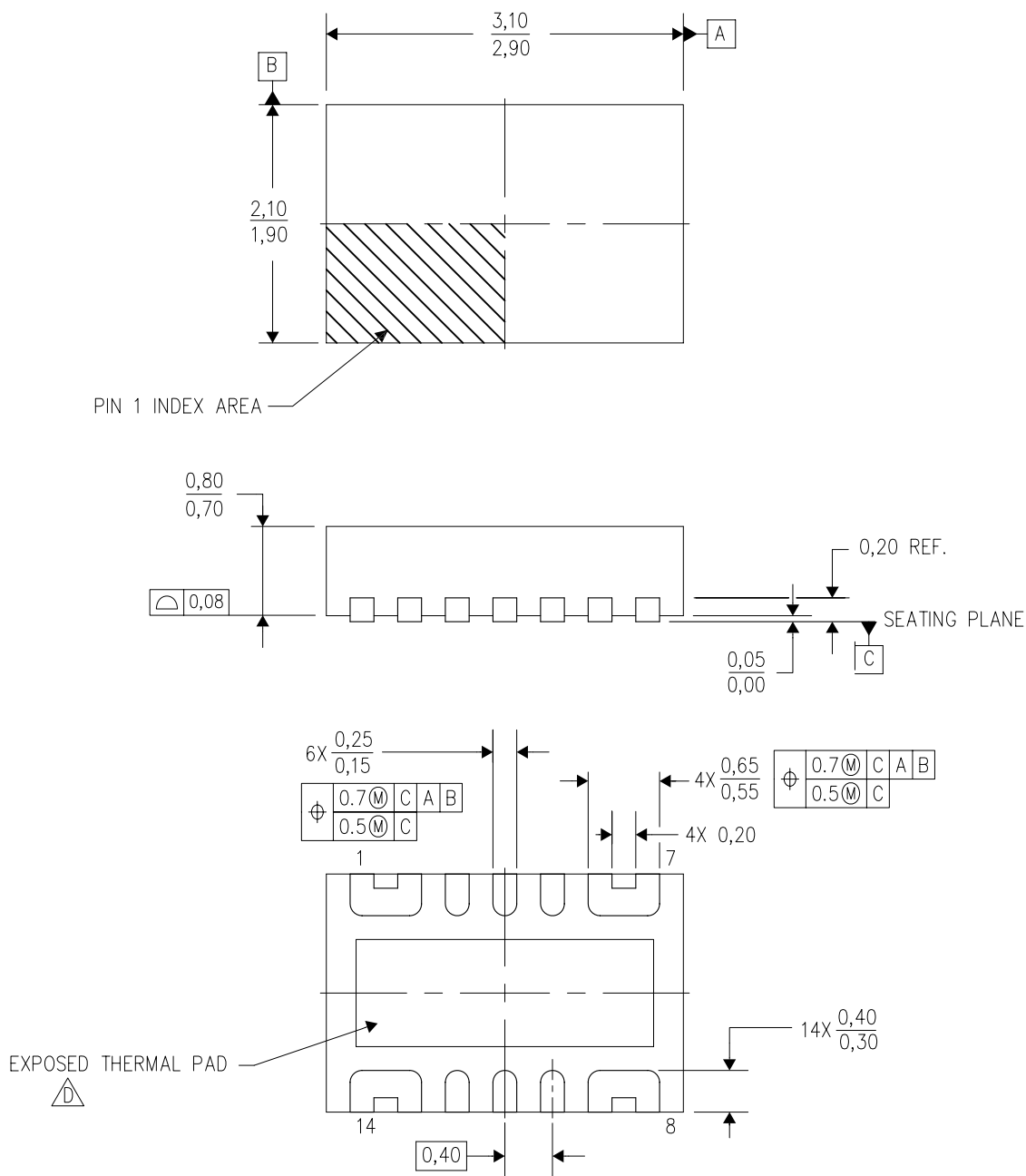


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22966TDPURQ1	WSN	DPU	14	3000	210.0	185.0	35.0
TPS22966TDPUTQ1	WSN	DPU	14	250	210.0	185.0	35.0

DPU (R-PWSON-N14)

PLASTIC SMALL OUTLINE NO-LEAD



4211321/B 11/10

- NOTES:
- | | |
|-----------|---|
| A. | All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. |
| B. | This drawing is subject to change without notice. |
| C. | Small Outline No-Lead (SON) package configuration. |
| D. | The package thermal pad must be soldered to the board for thermal and mechanical performance. |
| | See the Product Data Sheet for details regarding the exposed thermal pad dimensions. |
| E. | This package is Pb-free. |

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司