TPS22860 超低泄漏电流负载开关

1 特性

- 集成单通道负载开关
- 偏置电压范围 (V_{BIAS})：1.65V 至 5.5V
- 输入电压范围：0V 至 V_{BIAS}
- 导通电阻 (R_{ON})
  - VIN = 5V (V_{BIAS} = 5V) 时，R_{ON} = 0.73Ω
  - VIN = 3.3V (V_{BIAS} = 5V) 时，R_{ON} = 0.68Ω
  - VIN = 1.8V (V_{BIAS} = 5V) 时，R_{ON} = 0.63Ω
- 200mA 最大持续开关电流
- 超低泄漏电流
  - V_{IN} 泄漏电流 = 2nA
  - V_{BIAS} 泄漏电流（5.5V 时）= 10nA
- 6 引脚小外形尺寸晶体管 (SOT)-23 封装或 SC70 封装
- 静电放电 (ESD) 性能经测试符合 JESD 22 规范
  - 2kV 人体放电模式 (HBM) 和 1kV 组件充电模式 (CDM)

2 应用

- 可穿戴产品
- 物联网
- 无线传感器网络

3 说明

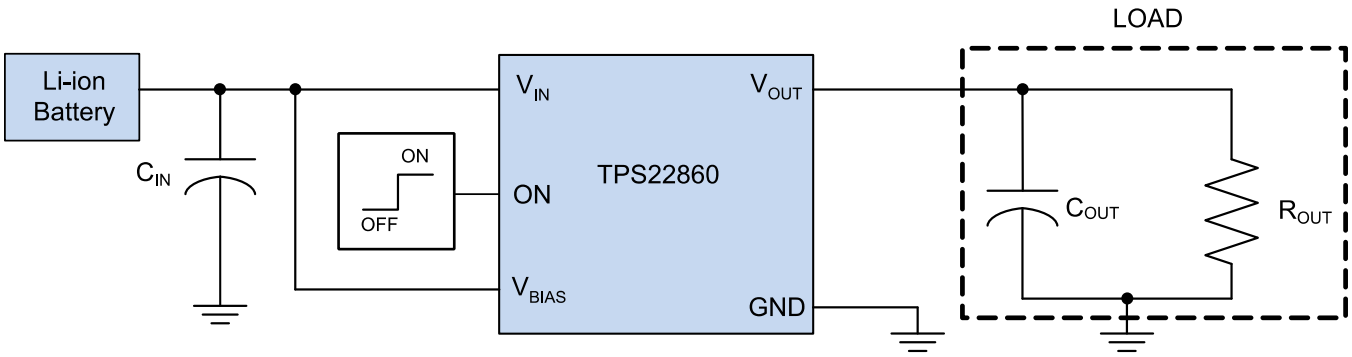
TPS22968 是一款小型、超低泄漏电流、单通道负载开关。 该器件需要一个 V_{BIAS} 电压，工作输入电压范围为 0V 至 V_{BIAS}。 它可支持最大 200mA 的持续电流。 此开关可由一个打开/关闭输入 (ON) 控制，此输入可与低压控制信号直接对接。 TPS22860 采用两种节省空间的 6 引脚 SOT-23 和 SC70 小型封装。 器件在自然通风环境下的额定运行温度范围为 -40°C 至 85°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS22860	SOT-23	2.80 x 2.90mm
	SC-70	2.10 x 2.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 常见应用电路原理图

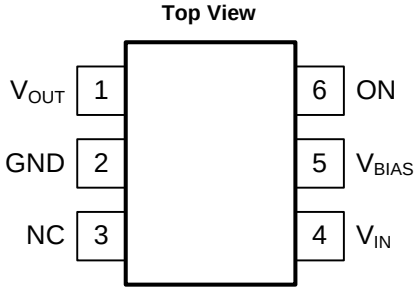


目录

5 修订历史记录

日期	修订版本	注释
2015 年 4 月	*	首次发布。

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{OUT}	1	O	Switch output.
GND	2	—	Ground
NC	3	—	No connect
V_{IN}	4	I	Switch input. Connect a ceramic capacitor from V_{IN} to GND.
V_{BIAS}	5	I	Bias voltage. Power supply to the device.
ON	6	I	Active high switch control input. Do not leave floating.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT(2)
V_{BIAS}	BIAS voltage range	–0.5	6.5	V
V_{IN}	Input voltage range	–0.5	V_{BIAS} + 0.5	V
V_{OUT}	Output voltage range	–0.5	V_{BIAS} + 0.5	V
V_{ON}	Input voltage range	–0.5	6.5	V
I_{MAX}	Maximum Continuous Switch Current		200	mA
I_{PLS}	Maximum Pulsed Switch Current, pulse <300us, 2% duty cycle		400	mA
T_A	Operating free-air temperature range(3)	–40	85	°C
T_J	Maximum junction temperature		125	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Inapplications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (M JA \times P_{D(max)})$

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range		0		V_{BIAS}	V
V_{BIAS}	Supply voltage range		1.65		5.5	V
V_{ON}	Control input voltage range		0		5.5	V
V_{OUT}	Output voltage range		0		V_{BIAS}	V
$V_{IH, ON}$	High-level input voltage, ON	V_{BIAS} = 5 V	2.4		5.5	V
$V_{IL, ON}$	Low-level input voltage, ON	V_{BIAS} = 5 V	0		0.8	V
C_{IN}	Input Capacitor		1			µF

7.4 Thermal Information

THERMAL METRIC(1)(2)		TPS22860		UNIT
		DBV	DCK	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	235.2	249.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	164.8	107.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	82,.5	95.8	
ψ_{JT}	Junction-to-top characterization parameter	52.9	6.2	
ψ_{JB}	Junction-to-board characterization parameter	82.0	93.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

7.5 Electrical Characteristics

over operating free-air temperature range(1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{ON} = V_{BIAS} = 3.3 V				10	100	nA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	V_{ON} = 0 V				10	100	
$I_{SD, VIN}$	V_{IN} shutdown current	V_{ON} = 0 V, V_{OUT} = 1 V	V_{IN} = 3.0 V			2	50	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V					100	
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –100 mA, V_{BIAS} = 3.3 V	V_{IN} = 3.3 V	T_A = 25°C		0.92	1.15	Ω
				Full T_A			1.31	
			V_{IN} = 2 V	T_A = 25°C		1.2	1.5	
				Full T_A			1.7	
			V_{IN} = 1.8 V	T_A = 25°C		0.95	1.2	
				Full T_A			1.35	

(1) Over the operating ambient temp –40°C ≤ TA ≤ 85°C (full) and VBIAS = 3.3V. Typical values are for TA = 25°C. (unless otherwise noted)

7.6 Switching Characteristics

over operating free-air temperature range(1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time	V_{OUT} = V_{BIAS}, R_L = 50 Ω C_L = 35 pF	T_A = 25°C	V_{BIAS} = 3.3 V	2	4.5	13	ns
			Full T_A	V_{BIAS} = 3 V to 3.6 V	1		15	
t_{OFF}	Turn-off time	V_{OUT} = V_{BIAS}, R_L = 50 Ω C_L = 35 pF	T_A = 25°C	V_{BIAS} = 3.3 V	3	9	15	ns
			Full T_A	V_{BIAS} = 3 V to 3.6 V	2		20	
$t_{ON/OFF}$	ON/OFF delay time				See Figure 9			

(1) V_{IN} = V_{ON} = V_{BIAS} = 5V, TA = 25ºC

7.7 Typical Characteristics

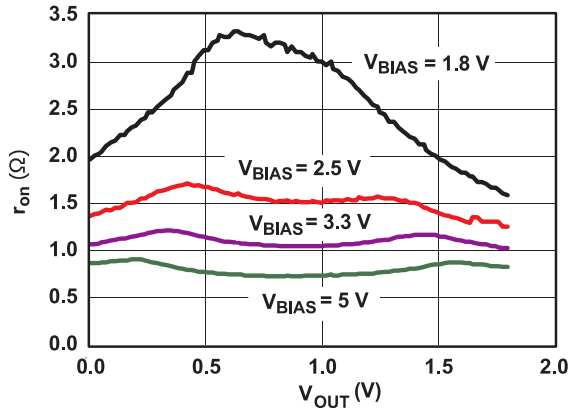


Figure 1. r_{on} vs V_{OUT}

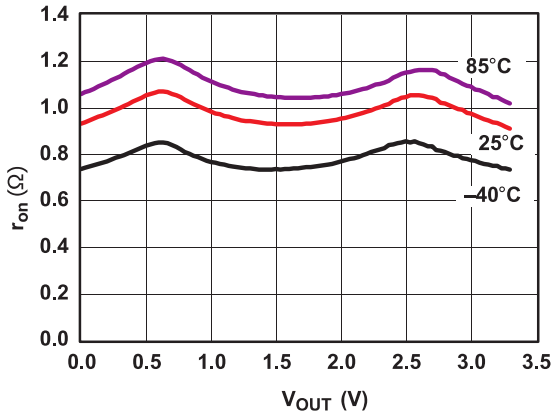


Figure 2. r_{on} vs V_{OUT} (V_{BIAS} = 3.3 V)

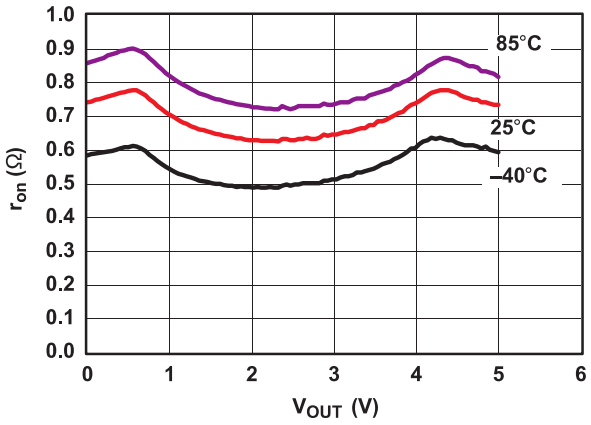


Figure 3. r_{on} vs V_{OUT} (V_{BIAS} = 5 V)

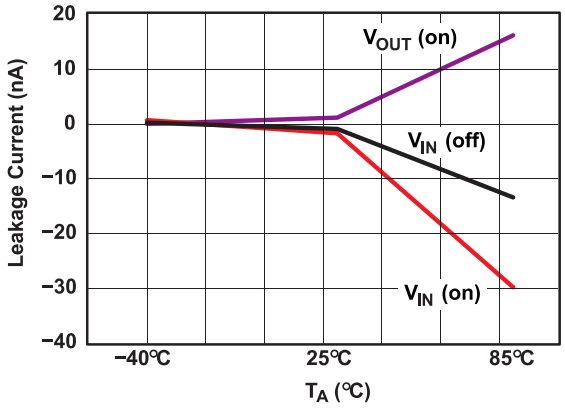


Figure 4. Leakage Current vs Temperature (V_{BIAS} = 5.5 V)

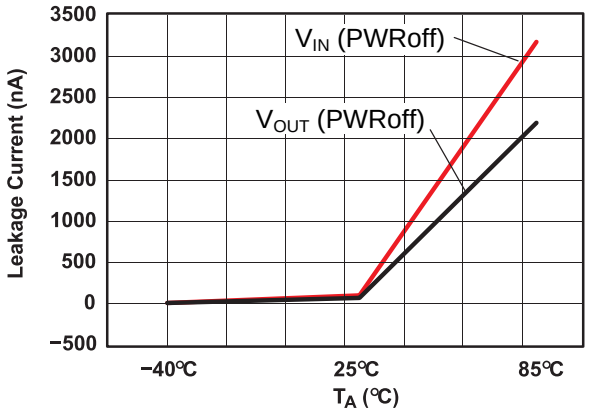


Figure 5. Leakage Current vs Temperature (V_{BIAS} = 5 V)

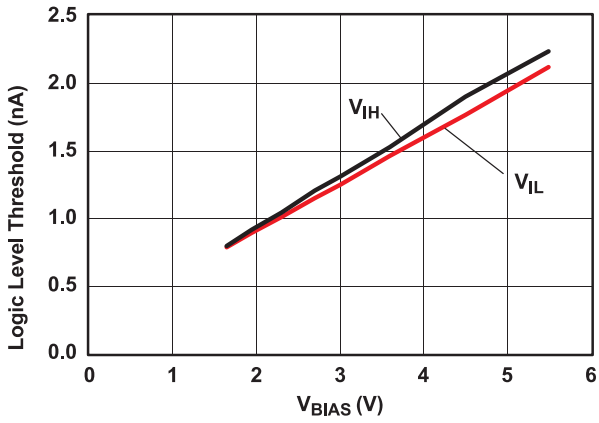


Figure 6. Logic-Level Threshold vs V_{BIAS}

Typical Characteristics (continued)

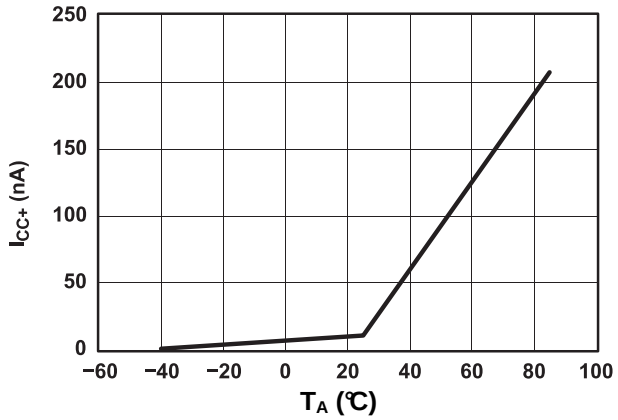


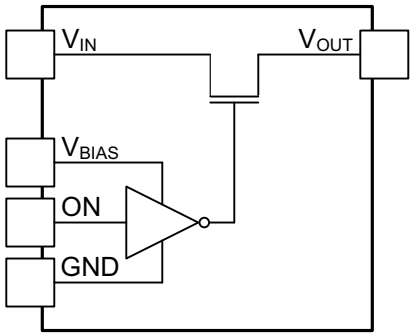
Figure 7. Power-Supply Current vs Temperature (V_{BIAS} = 5 V)

8 Detailed Description

8.1 Overview

The TPS22860 is a small, ultra-low leakage current, single channel bi-driectional load switch. The device requires a V_{BIAS} voltage and can operate over an input voltage range of 0 V to V_{BIAS}. It can support a maximum continuous current of 200 mA. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. The TPS22860 is available in two small, space-saving 6-pin SOT-23 and SC70 packages. The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ON/OFF Control

The ON input controls the load switch with positive logic.

8.3.2 Pass Transistor

The TPS22860 supports up to 200-mA current flow in either direction. R_{ON} is dependent on V_{BIAS} as shown in Figure 1, Figure 2, and Figure 3.

8.4 Device Functional Modes

Table 1. Functional Table

ON	V_{IN} to V_{OUT}
L	Off
H	On

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section will highlight some of the design considerations when implementing this device in a common application.

9.2 Typical Application

The TPS22860 IC is a high side load switch. The TPS22860 internal components are rated for 1.65-V to 5.5-V supply and support up to 200 mA of load current. The TPS22860 can be used in a variety of applications. Figure 8 below shows a general application of TPS22860 to control the load inrush current.

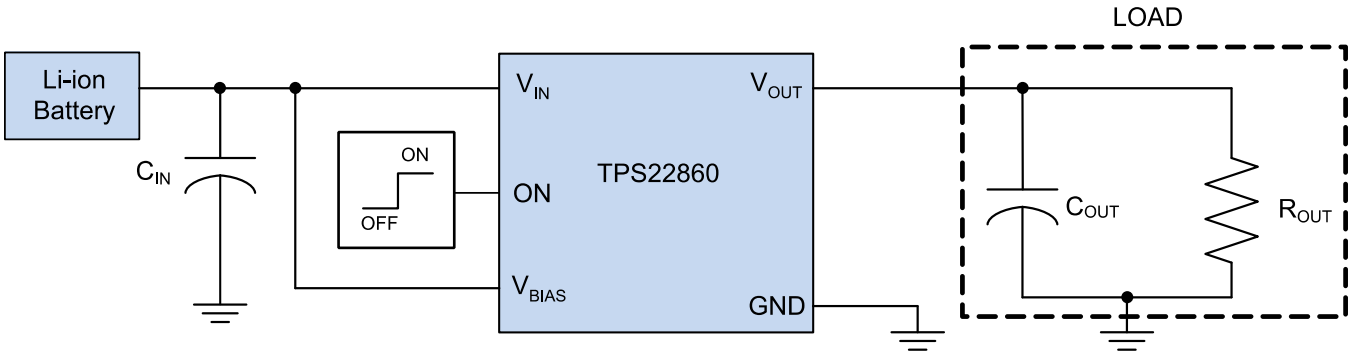


Figure 8. Standard Load Switching Application

9.2.1 Design Requirements

Table 2. Component Table

COMPONENT	DESCRIPTION
C_{IN}	Input capacitance (1)
LOAD	Load resistance and capacitance will affect the output rise time

(1) Required for load inrush current (slew rate) control

9.2.2 Detailed Design Procedure

9.2.2.1 Inrush Current

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor must be placed between V_{IN} and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current applications. When switching heavy loads, TI recommends to have an input capacitor about 10× higher than the output capacitor to avoid excessive voltage drop. Do not float the ON pin.

9.2.2.2 ON/OFF Interface

The load switch is controlled by the voltage at the ON pin. To turn ON, the input voltage must be larger than V_{IH} and to turn off the voltage must be below V_{IL}.

In applications where an ON/OFF signal is not available, connect ON pin to V_{IN}. The TPS22860 will turn ON/OFF in sync with the input supply connected to V_{IN}.

NOTE

Connect a pull down resistor from the ON pin to GND when the ON/OFF signal is driven by a high-impedance (tri-state) driver.

9.2.3 Application Curves

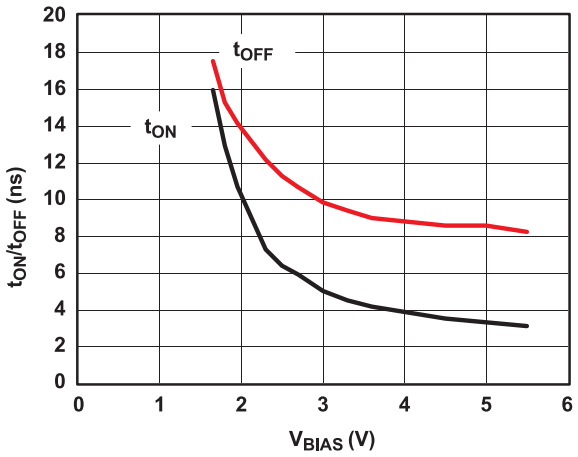


Figure 9. t_{ON} and t_{OFF} vs V_{BIAS}

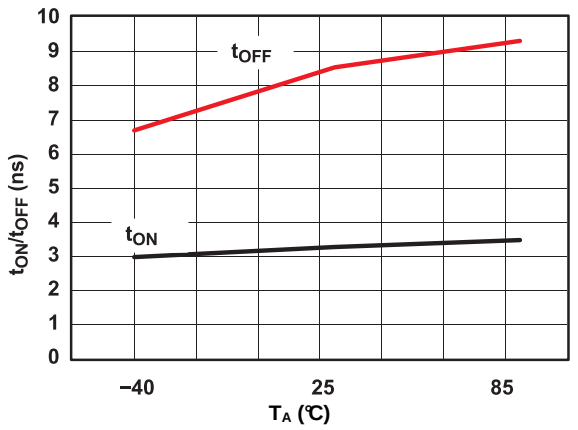


Figure 10. t_{ON} and t_{OFF} vs Temperature (V_{BIAS} = 5 V)

10 Power Supply Recommendations

The device is designed to operate from a VIN range of 1.65 V to 5.5 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1 µF may be sufficient.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- V_{IN} and V_{OUT} traces should be as short and wide as possible to accommodate for high current.
- The V_{IN} pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- The VOUT pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the V_{IN} bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.

11.2 Thermal Reliability

For higher reliability it is recommended to limit TPS22860 IC's die junction temperature to less than 105°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate maximum on-chip power dissipation to achieve the maximum die junction temperature target:

$$PD_{(MAX)} = \frac{\left(T_{J(MAX)} - T_A\right)}{\theta_{JA}} \quad (1)$$

Where:

$T_{J(MAX)}$ is the target maximum junction temperature.

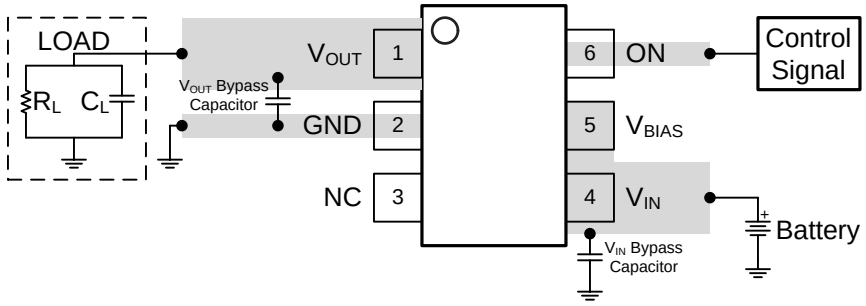
T_A is the operating ambient temperature.

$R_{\theta JA}$ is the package junction to ambient thermal resistance.

11.3 Improving Package Thermal Performance

The package $R_{\theta JA}$ value under standard conditions on a High-K board is listed in the *Thermal Information* table. $R_{\theta JA}$ value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce $R_{\theta JA}$ and thus improve device thermal capabilities. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

11.4 Layout Example



⏚ Indicates connection to ground plane

Figure 11. Basic PCB Layout

12 器件和文档支持

12.1 商标

All trademarks are the property of their respective owners.

12.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22860DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZFNR
TPS22860DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZFNR
TPS22860DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZFNR
TPS22860DBVRG4.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZFNR

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

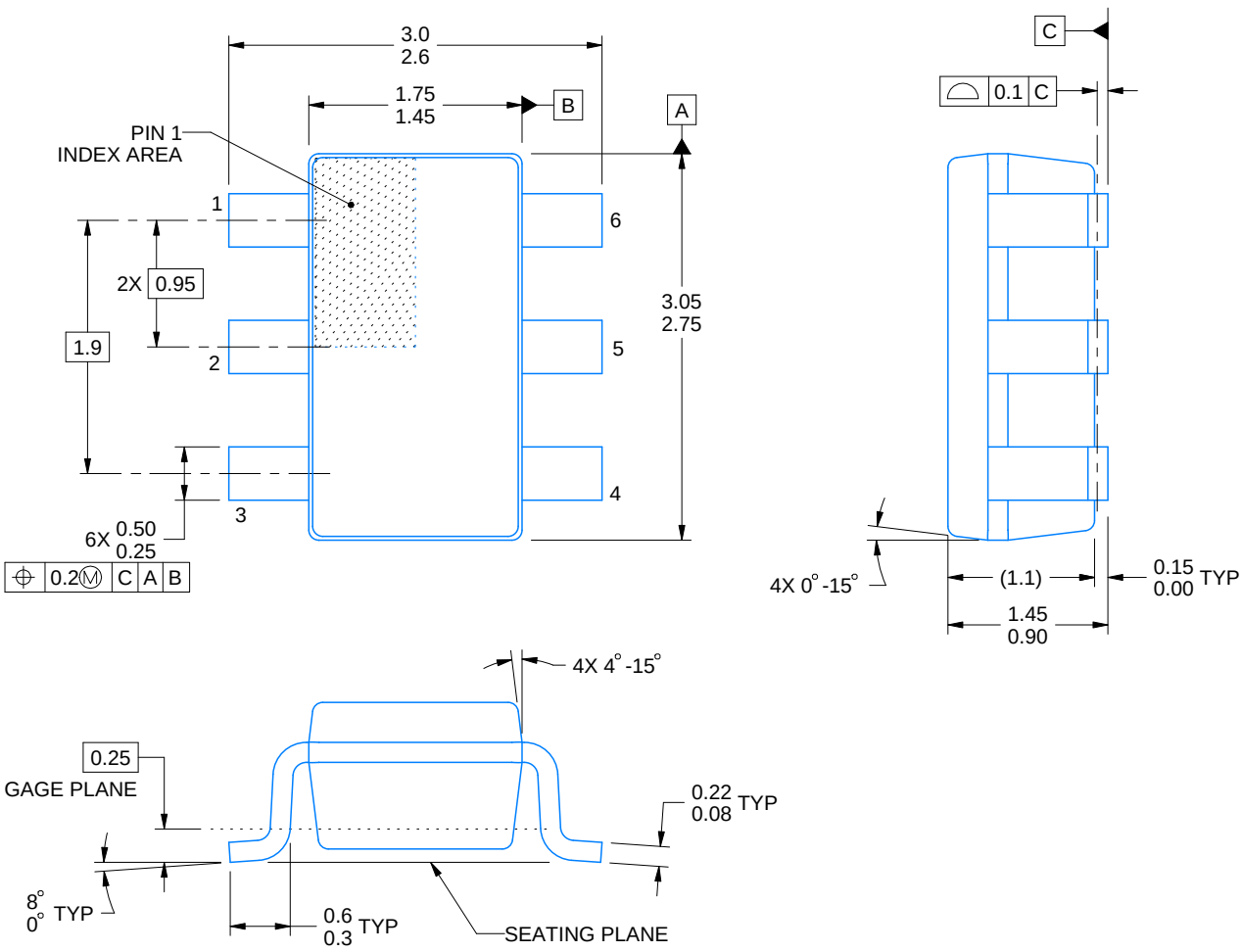
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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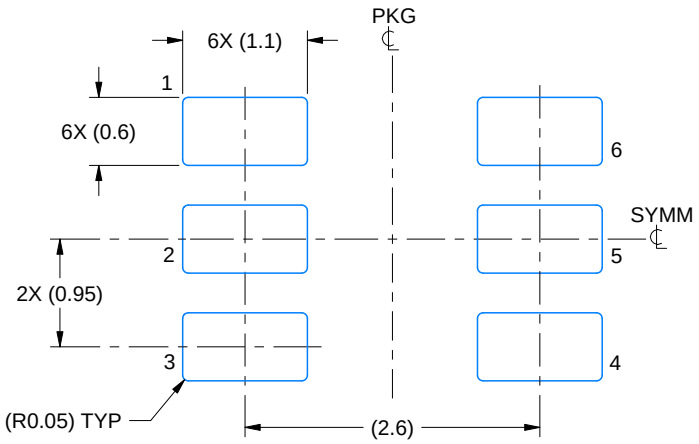
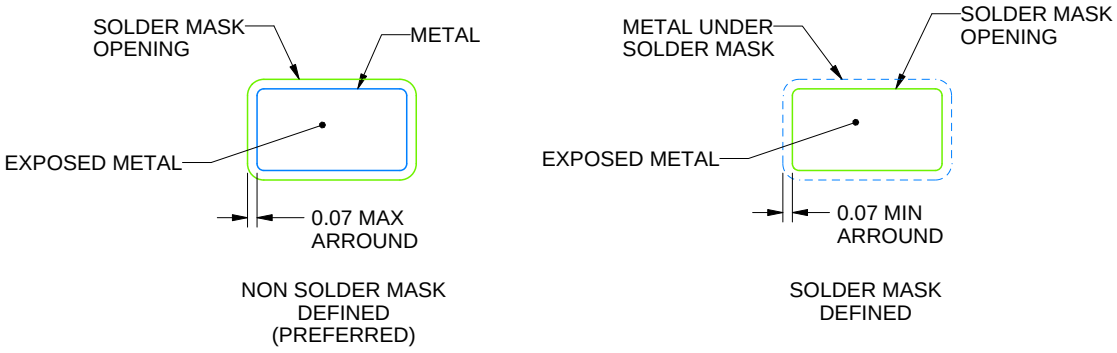
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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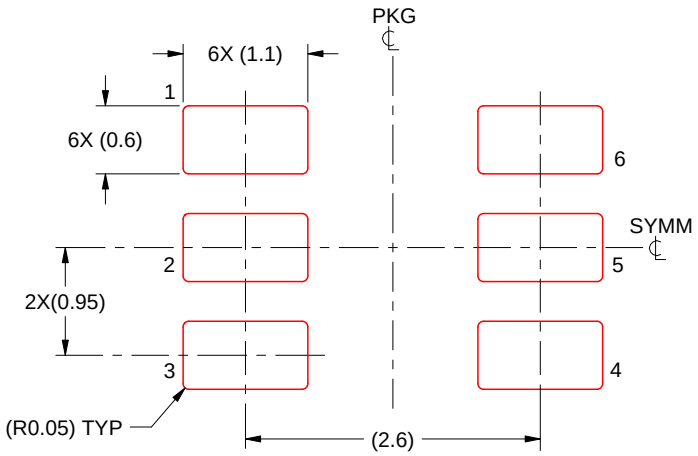
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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