

具有热保护功能的 TPS22810-Q1 2.7V-18V、79mΩ 导通电阻负载开关

1 特性

- 符合汽车类标准
- 具有符合 AEC-Q100 标准的下列特性：
 - 器件温度等级 2：环境工作温度范围为 -40°C 至 $+105^{\circ}\text{C}$
 - 器件 HBM ESD 分类等级 2
 - 器件 CDM ESD 分类等级 C5
- 集成单通道负载开关
- 最大连续电流为 2A
- 输入电压：2.7V 至 18V
- 绝对最大输入电压：20V
- 导通电阻 (R_{ON})
 - $R_{\text{ON}} = 79\text{m}\Omega$ ($V_{\text{IN}} = 12\text{V}$ 时的典型值)
- 静态电流
 - $62\mu\text{A}$ ($V_{\text{IN}} = 12\text{V}$ 时的典型值)
- 关断电流
 - 500nA ($V_{\text{IN}} = 12\text{V}$ 时的典型值)
- 热关断
- 欠压闭锁 (UVLO)
- 可调节快速输出放电 (QOD)
- 可通过 CT 引脚配置的上升时间
- 小外形尺寸晶体管 (SOT) 23-6 封装
 - $2.9\text{mm} \times 2.8\text{mm}$, 0.95mm 间距, 1.45mm 高 (DBV)

2 应用

- 汽车音响主机
- 环视 ECU

3 说明

TPS22810-Q1 是一款单通道负载开关，具有可配置的上升时间和集成式快速输出放电 (QOD) 功能。该器件具有热关断功能，可保护器件免受高结温的损坏，因此可从根本上确保器件的安全运行区。该器件具有一个 N 沟道 MOSFET，可在 2.7V 至 18V 的输入电压范围内运行。该器件可支持 2A 的最大电流。开关可由一个打开和关闭输入控制，此输入可直接连接至低压控制信号。

该器件的可配置上升时间可大幅降低大容量负载电容所产生的浪涌电流，从而降低或消除电源压降。欠压闭锁用于在输入电压降至阈值以下时关闭器件，以确保下游电路不会因为供电电压低于预期值而损坏。可配置的快速输出放电 (QOD) 引脚控制器件的下降时间，以便针对掉电进行灵活设计。

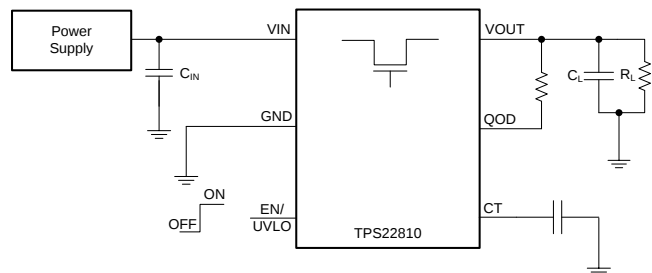
TPS22810-Q1 器件可提供方便目测检查焊点的带引线的 SOT-23 封装 (DBV)。该器件在自然通风环境下的额定运行温度范围为 -40°C 至 $+105^{\circ}\text{C}$ 。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPS22810-Q1	SOT-23 (6)	2.90mm x 2.80mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



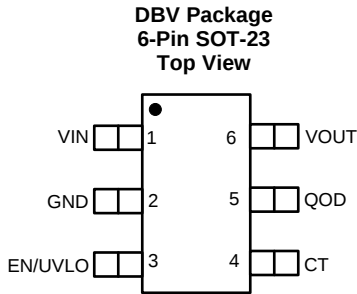
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4 修订历史记录

日期	修订版本	说明
4 月2018	*	最初发布版本。

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CT	4	O	Switch slew rate control. Can be left floating
EN/UVLO	3	I	Active high switch control input and UVLO adjustment. Do not leave floating
GND	2	—	Device ground
QOD	5	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways: - Placing an external resistor between VOUT and QOD - Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) - Disabling QOD by leaving pin floating See the Quick Output Discharge (QOD) for more information
VIN	1	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND
VOUT	6	O	Switch output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{IN}	Maximum Input Voltage Range	VIN	–0.3	20	V
V _{OUT}	Maximum Output Voltage Range	VOUT	–0.3	min (20V, V _{IN} + 0.3)	
V _{EN/UVLO}	Maximum Enable Pin Voltage Range	EN/UVLO	–0.3	20	V
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±3000	V
		Charged device model (CDM), per AEC Q100-011	±750	
		Corner pins (VIN, VOUT, EN/UVLO, and CT)	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{IN}	Input Voltage Range	IN	2.7	18	V
V _{OUT}	Output Voltage Range	OUT		V _{IN}	V
V _{EN/UVLO}	Enable Pin Voltage Range	EN/UVLO	0	18	V
IMAX	Maximum continuous switch current, TA = 65°C	IN to OUT		2	A
IMAX	Maximum continuous switch current, TA = 85°C	IN to OUT		1.5	A
IMAX	Maximum continuous switch current, TA = 105°C	IN to OUT		1	A
T _A	Operating free-air temperature		–40	105	°C
C _{IN}	Input Capacitor ⁽¹⁾		1		μF

- (1) See the Detailed Description section.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22810-Q1	UNIT
		DBV (SOT23)	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	182	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	127.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	16.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	26.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	36.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the following ambient operating temperature $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$. Typical values are for $T_A = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT	
I _{Q, VIN}	Quiescent current	I _{OUT} = 0 A	V _{IN} = 18 V	T _A = −40°C to +85°C		62	80	μA	
				T _A = −40°C to +105°C			85		
			V _{IN} = 12 V	T _A = −40°C to +85°C		62	80		
				T _A = −40°C to +105°C			85		
			V _{IN} = 5 V	T _A = −40°C to +85°C		59	80		
				T _A = −40°C to +105°C			85		
			V _{IN} = 3.3 V	T _A = −40°C to +85°C		53	80		
				T _A = −40°C to +105°C			85		
			V _{IN} = 2.7 V	T _A = −40°C to +85°C		49	70		
				T _A = −40°C to +105°C			85		
I _{SD, VIN}	Shutdown current	V _{EN} = 0 V, V _{OUT} = 0 V	V _{IN} = 18 V	T _A = −40°C to +85°C		0.5	2.3	μA	
				T _A = −40°C to +105°C			3.8		
			V _{IN} = 12 V	T _A = −40°C to +85°C		0.5	2.3		
				T _A = −40°C to +105°C			3.8		
			V _{IN} = 5 V	T _A = −40°C to +85°C		0.5	2.3		
				T _A = −40°C to +105°C			3.8		
			V _{IN} = 3.3 V	T _A = −40°C to +85°C		0.5	2.3		
				T _A = −40°C to +105°C			3.8		
			V _{IN} = 2.7 V	T _A = −40°C to +85°C		0.5	2.3		
				T _A = −40°C to +105°C			3.8		
I _{EN/UVLO}	EN/UVLO pin input leakage current	V _{IN} = 18 V, I _{OUT} = 0 A		T _A = −40°C to +105°C			0.1	μA	
V _{UVR}	VIN UVLO threshold, rising			T _A = −40°C to +105°C		2	2.54	2.62	V
V _{UVRhyst}	VIN UVLO hysteresis			T _A = −40°C to +105°C			5		%
V _{ENR}	EN threshold, rising			T _A = −40°C to +105°C		1.13	1.23	1.3	V
V _{ENF}	EN threshold, falling			T _A = −40°C to +105°C		1.08	1.13	1.18	V
V _{SHUTF}	EN threshold voltage for low I _Q shutdown			T _A = −40°C to +105°C		0.5	0.75	0.9	V
R _{ON}	On-resistance	V _{IN} = 18 V, I _{OUT} = −200 mA	T _A = 25°C			79	86	mΩ	
			T _A = −40°C to +85°C				105		
			T _A = −40°C to +105°C				115		
		V _{IN} = 12 V, I _{OUT} = −200 mA	T _A = 25°C			79	86		
			T _A = −40°C to +85°C				105		
			T _A = −40°C to +105°C				115		
		V _{IN} = 9 V, I _{OUT} = −200 mA	T _A = 25°C			79	86		
			T _A = −40°C to +85°C				105		
			T _A = −40°C to +105°C				115		
		V _{IN} = 5 V, I _{OUT} = −200 mA	T _A = 25°C			79	86		
			T _A = −40°C to +85°C				105		
			T _A = −40°C to +105°C				115		
		V _{IN} = 3.3 V, I _{OUT} = −200 mA	T _A = 25°C			83	92		
			T _A = −40°C to +85°C				115		
			T _A = −40°C to +105°C				125		
		V _{IN} = 2.7 V, I _{OUT} = −200 mA	T _A = 25°C			86	95		
			T _A = −40°C to +85°C				120		
			T _A = −40°C to +105°C				130		

Electrical Characteristics (continued)

Unless otherwise noted, the specification in the following table applies over the following ambient operating temperature $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$. Typical values are for $T_A = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R _{PD}	Output pull down resistance	V _{IN} = V _{OUT} = 18 V, V _{EN/UVLO} = 0 V	T _A = −40°C to +105°C		290	350	Ω
		V _{IN} = V _{OUT} = 12 V, V _{EN/UVLO} = 0 V	T _A = −40°C to +105°C		265	350	
		V _{IN} = V _{OUT} = 5 V, V _{EN/UVLO} = 0 V	T _A = −40°C to +105°C		250	400	
T _{SD}	Thermal shutdown threshold	V _{IN} = 18 V	T _A = −40°C to +105°C		160		°C
T _{SD,HYS}	Thermal shutdown hysteresis	V _{IN} = 18 V	T _A = −40°C to +105°C		30		°C

6.6 Switching Characteristics

Refer to the timing test circuit in [Figure 16](#) (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where V_{IN} is already in steady state condition before the EN/UVLO pin is asserted high.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN} = 18 V, V _{EN/UVLO} = 5 V, T _A = 25 °C (unless otherwise noted)						
t _{ON}	Turnon time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		520		μs
t _{OFF}	Turnoff time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		3.3		
t _R	V _{OUT} rise time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		700		
t _F	V _{OUT} fall time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		2		
t _D	Delay time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		180		
V _{IN} = 12 V, V _{EN/UVLO} = 5 V, T _A = 25 °C (unless otherwise noted)						
t _{ON}	Turnon time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		380		μs
t _{OFF}	Turnoff time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		3.3		
t _R	V _{OUT} rise time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		460		
t _F	V _{OUT} fall time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		2		
t _D	Delay time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		150		
V _{IN} = 3.3 V, V _{EN/UVLO} = 5 V, T _A = 25 °C (unless otherwise noted)						
t _{ON}	Turnon time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		185		μs
t _{OFF}	Turnoff time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		3.3		
t _R	V _{OUT} rise time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		120		
t _F	V _{OUT} fall time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		2		
t _D	Delay time	R _L = 10 Ω, C _{IN} = 1 μF, C _L = 0.1 μF, C _T = 2200 pF		130		

6.7 Typical DC Characteristics

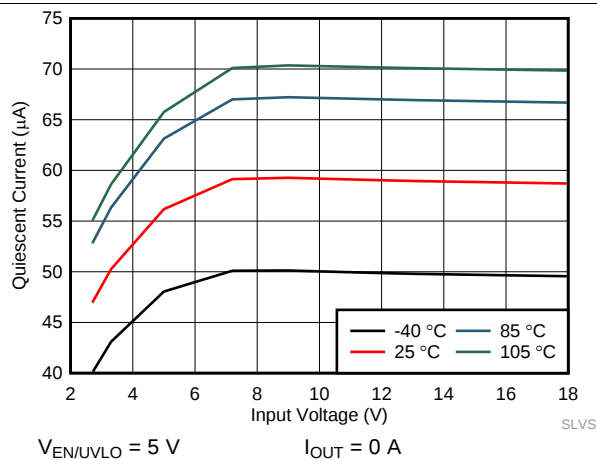


图 1. Quiescent Current vs Input Voltage

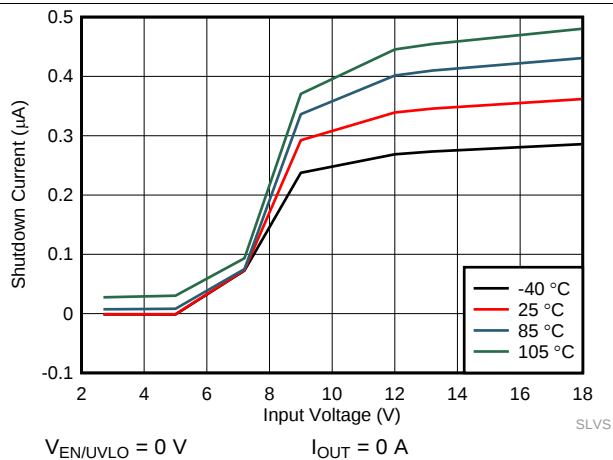


图 2. Shutdown Current vs Input Voltage

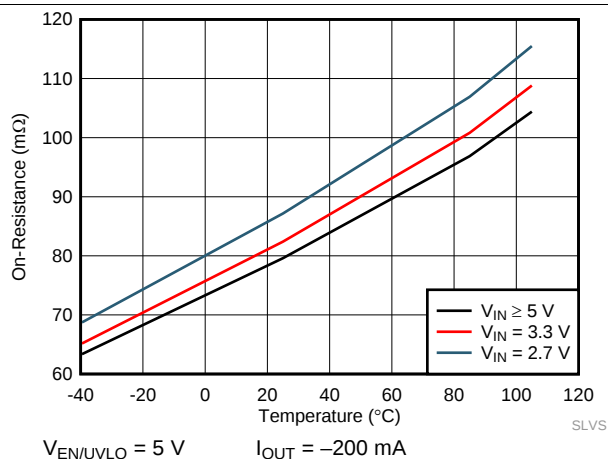


图 3. On-Resistance vs Temperature

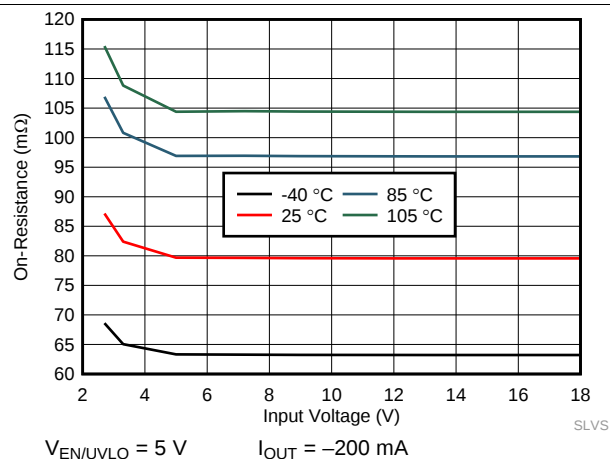


图 4. On-Resistance vs Input Voltage

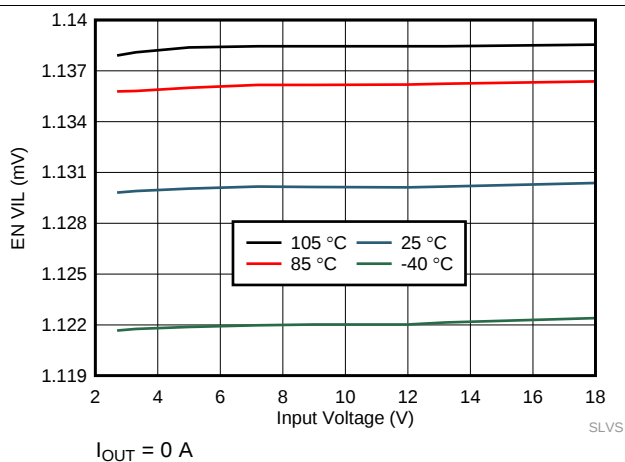


图 5. EN VIL vs Input Voltage

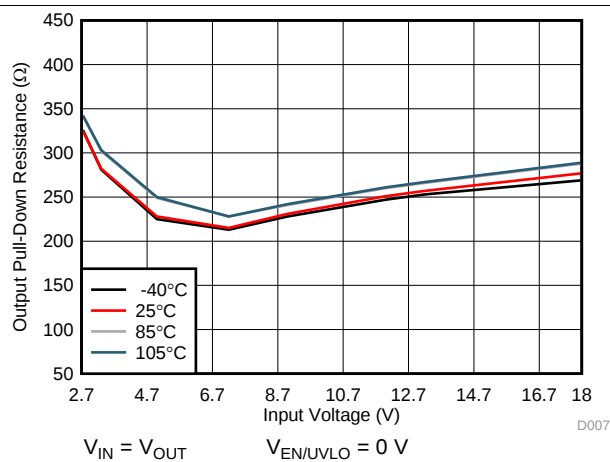


图 6. Output Pull-Down Resistance vs Input Voltage

6.8 Typical AC Characteristics

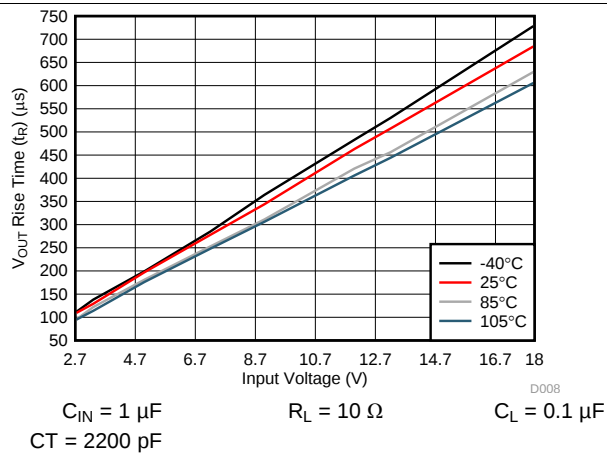


图 7. V_{OUT} Rise Time (t_R) vs Input Voltage

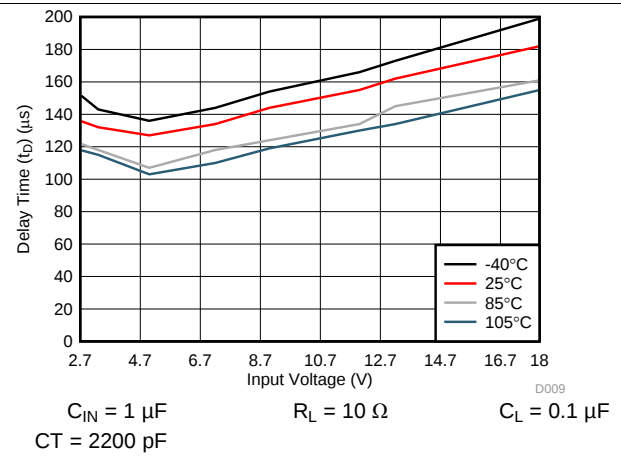


图 8. Delay Time (t_D) vs Input Voltage

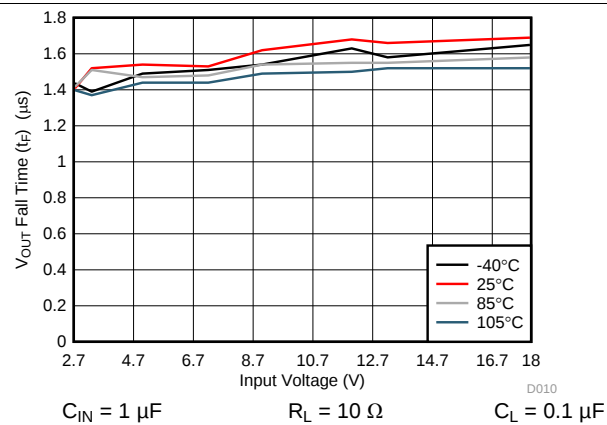


图 9. V_{OUT} Fall Time (t_F) vs Input Voltage

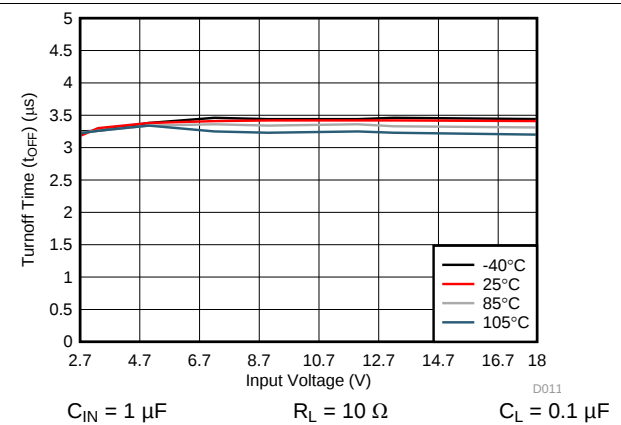


图 10. Turnoff Time (t_{OFF}) vs Input Voltage

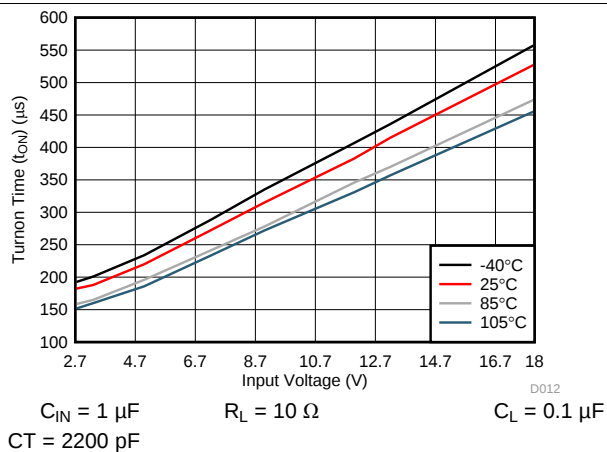


图 11. Turnon Time (t_{ON}) vs Input Voltage

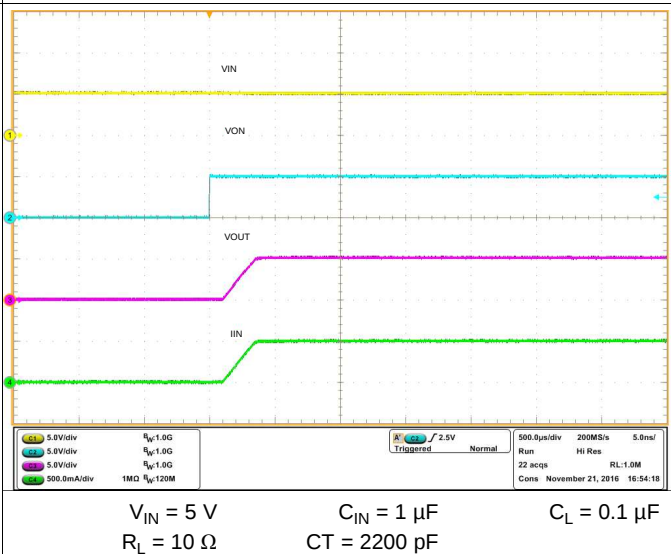
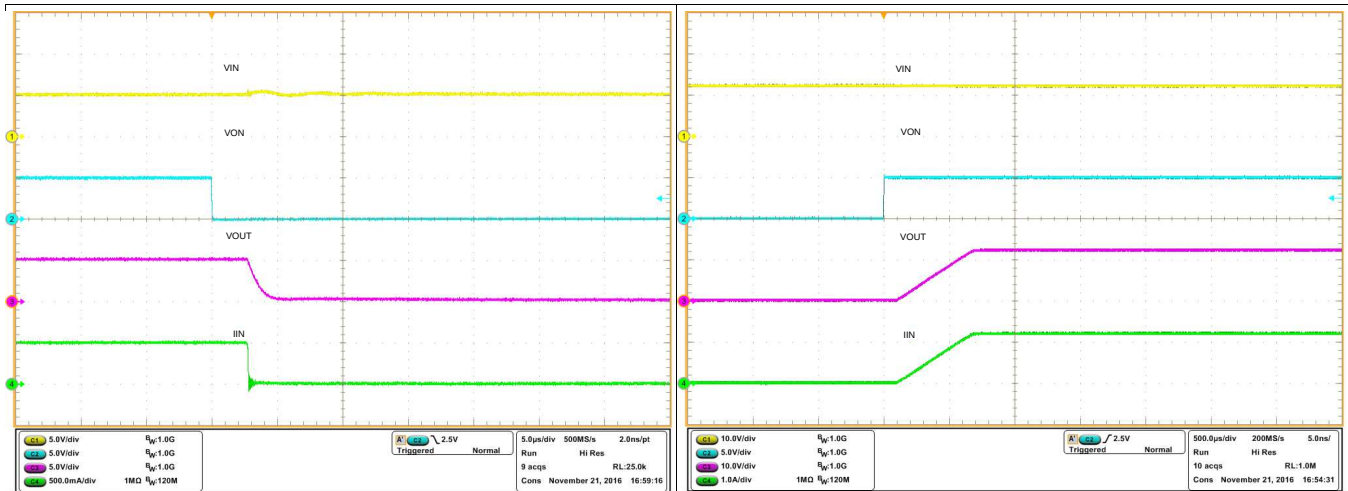


图 12. Rise Time t_R at $V_{IN} = 5 V$

Typical AC Characteristics (接下页)

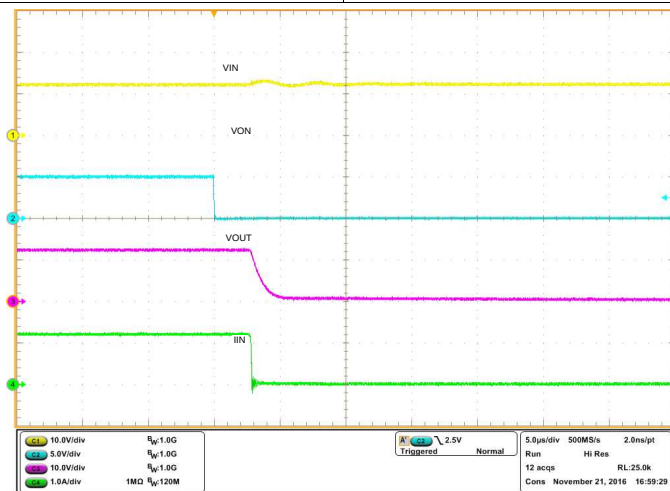


$V_{IN} = 5V$
 $R_L = 10\Omega$
 $C_{IN} = 1\mu F$
 $QOD = \text{Open}$
 $C_L = 0.1\mu F$

图 13. Fall Time t_F at $V_{IN} = 5V$

$V_{IN} = 12V$
 $R_L = 10\Omega$
 $C_{IN} = 1\mu F$
 $CT = 2200pF$
 $C_L = 0.1\mu F$

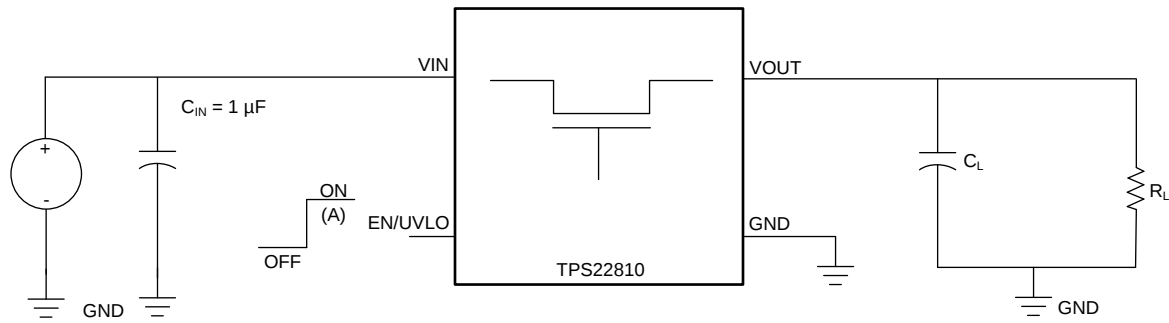
图 14. Rise Time t_R at $V_{IN} = 12V$



$V_{IN} = 12V$
 $R_L = 10\Omega$
 $C_{IN} = 1\mu F$
 $QOD = \text{Open}$
 $C_L = 0.1\mu F$

图 15. Fall Time t_F at $V_{IN} = 12V$

7 Parameter Measurement Information



A. Rise and fall times of the control signal are 100 ns

图 16. Test Circuit

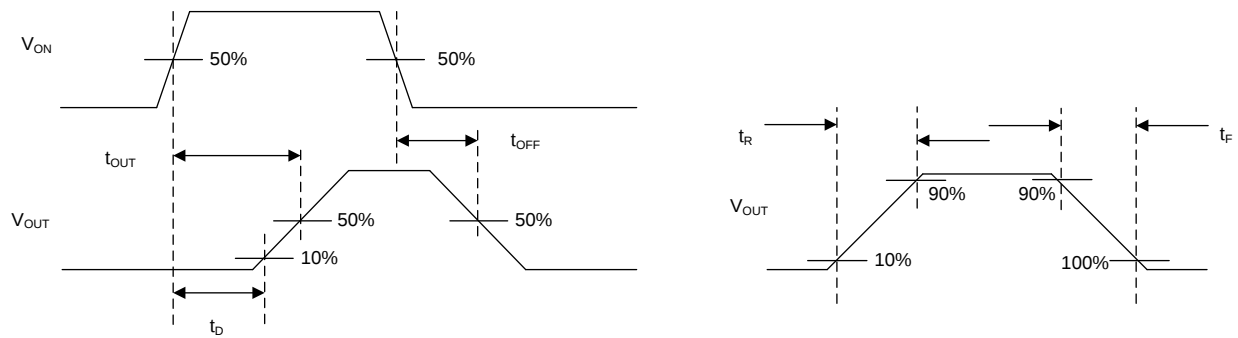


图 17. Timing Waveforms

8 Detailed Description

8.1 Overview

The TPS22810-Q1 is a 6-pin, 2.7-18-V load switch with thermal protection. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET which reduces the drop out voltage across the device.

The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage-lockout threshold (V_{UVR}), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. When VIN rises, the internal MOSFET of the device starts conducting and allow current to flow from VIN to VOUT. When EN/UVLO is held low (below V_{ENF}), internal MOSFET is turned off.

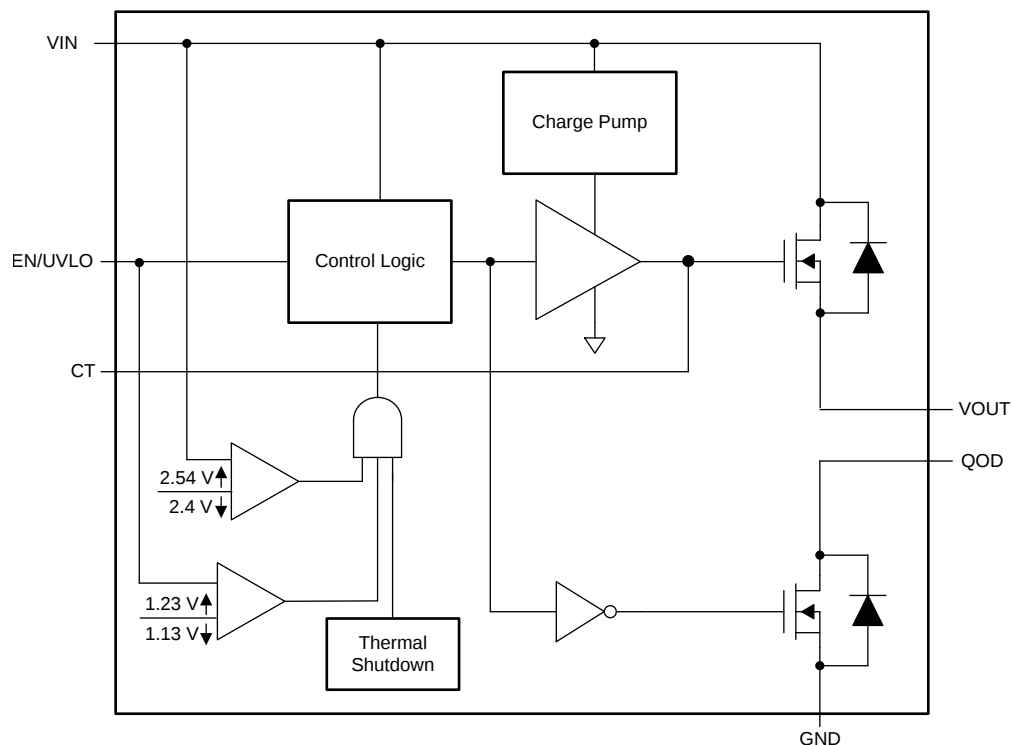
A voltage $V_{EN/UVLO} < V_{ENF}$ on this pin turns off the internal FET, thus disconnecting VIN from VOUT, while voltage below V_{SHUTF} takes the device into shutdown mode, with I_Q less than 1 μA to ensure minimal power loss.

The device has a configurable slew rate which helps reduce or eliminate power supply droop because of large inrush currents. The device also features a QOD (Quick Output Discharge) pin with an internal pull-down resistance (R_{PD}) which can be used to discharge VOUT once the switch is disabled.

During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

The device has a thermal protection feature to protect itself against thermal damage due to overtemperature and overcurrent conditions. Safe Operating Area (SOA) requirements are thus inherently met without any special design consideration by the board designer.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The EN/UVLO pin controls the state of the switch. EN/UVLO is active high and has a low threshold that can interface with low-voltage signals. The EN/UVLO pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

8.3.2 Quick Output Discharge (QOD)

The TPS22810-Q1 includes a QOD feature. The QOD pin can be configured in one of three ways:

- QOD pin shorted to VOUT pin. Using this method, the discharge rate after the switch becomes disabled is controlled with the value of the internal pull-down resistance (R_{PD}). The value of this resistance is listed in the [Electrical Characteristics](#) table.
- QOD pin connected to VOUT pin using an external resistor R_{EXT} . After the switch becomes disabled, the discharge rate is controlled by the value of the total resistance of the QOD. To adjust the total QOD resistance, [公式 1](#) can be used.

$$R_{QOD} = R_{PD} + R_{EXT}$$

where

- R_{QOD} is the total output discharge resistance
- R_{PD} is the internal pulldown resistance
- R_{EXT} is the external resistance placed between the VOUT and QOD pin. (1)
- QOD pin is unused and left floating. Using this method, there is no quick output discharge functionality, and the output remains floating after the switch is disabled.

Note that during thermal shutdown, the QOD functionality is not available. The device does not discharge the load because R_{PD} does not become engaged.

The fall times of the device depend on many factors including the total resistance of the QOD, V_{IN} , and the output capacitance. When QOD is connected to VOUT, the fall time changes over V_{IN} because the internal R_{PD} varies over V_{IN} . To calculate the approximate fall time of V_{OUT} for a given R_{QOD} , use [公式 2](#) and [表 1](#).

$$V_{CAP} = V_{IN} \times e^{-t/\tau}$$

where

- V_{CAP} is the voltage across the capacitor (V)
- t is the time since power supply removal (s)
- τ is the time constant equal to $R_{QOD} \times C_L$ (2)

The fall time's dependency on V_{IN} becomes minimal because the QOD value increases with additional external resistance. See [表 1](#) for QOD fall times.

表 1. QOD Fall Times

V_{IN} (V)	FALL TIME (μ s) 90% - 10%, $C_{IN} = 1 \mu$ F, $I_{OUT} = 0$ A, $V_{IN} = 0$ V, ON = 0 V ⁽¹⁾					
	$T_A = 25^\circ\text{C}$			$T_A = 85^\circ\text{C}$		
	$C_L = 1 \mu$ F	$C_L = 10 \mu$ F	$C_L = 100 \mu$ F	$C_L = 1 \mu$ F	$C_L = 10 \mu$ F	$C_L = 100 \mu$ F
18	470	4700	47000	470	4700	47000
12	450	4500	45000	450	4500	45000
9	440	4400	44000	440	4400	44000
5	500	5000	50000	480	4800	48000
3.3	600	6000	60000	570	5700	57000

(1) TYPICAL VALUES WITH QOD SHORTED TO VOUT

8.3.2.1 QOD when System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor, C_{IN} , discharges at V_{IN} . Past the set UVLO level, the pull-down resistance R_{PD} becomes disabled and the output no longer becomes discharged. If there is still remaining charge on the output capacitor, this results in longer fall times. Care must be taken such that C_{IN} is large enough to meet the device UVLO settings.

8.3.2.2 Internal QOD Considerations

Special considerations must be taken when using the internal R_{PD} by shorting the QOD pin to the VOUT pin. The internal R_{PD} is a pull-down resistance designed to quickly discharge a load after the switch has been disabled. Care must be used to ensure that excessive current does not flow through R_{PD} during discharge so that the maximum T_J of 125°C is not exceeded. When using only the internal R_{PD} to discharge a load, the total capacitive load must not exceed 200 μ F. Otherwise, an external resistor, R_{EXT} must be used to ensure the amount of current flowing through R_{PD} is properly limited and the maximum T_J is not exceeded. To ensure the device is not damaged, the remaining charge from C_L must decay naturally through the internal QOD resistance and must not be driven.

8.3.3 EN/UVLO

EN/UVLO controls the ON and OFF state of the internal MOSFET, as an input pin. In its high state, the internal MOSFET is enabled. A low on this pin turns off the internal MOSFET. High and Low levels are specified in the parametric table of the datasheet.

A voltage $V_{EN/UVLO} < V_{ENF}$ on this pin turns off the internal FET, thus disconnecting V_{IN} from VOUT, while voltage below V_{SHUTF} takes the device into shutdown mode, with I_Q less than 1 μ A to ensure minimal power loss.

The EN/UVLO pin can be directly driven by a 1.8 V, 3.3 V or 5 V general purpose output pin.

The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (2.5 μ s typical) for quick detection of power failure. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

The undervoltage lock out (UVLO) threshold can be programmed by using an external resistor divider from supply V_{IN} terminal to EN/UVLO terminal to GND shown in [Figure 18](#). When an undervoltage or input power fail event is detected, the internal FET is quickly turned off. If the programmable UVLO function is not needed, the EN/UVLO terminal must be connected to the V_{IN} terminal. EN/UVLO terminal must not be left floating.

The device also implements internal UVLO circuitry on the V_{IN} terminal. The device disables when the V_{IN} terminal voltage falls below internal UVLO Threshold (V_{UVF}). The internal UVLO threshold has a hysteresis ($V_{UVRhyst}$). See [Figure 19](#) and [Figure 20](#).

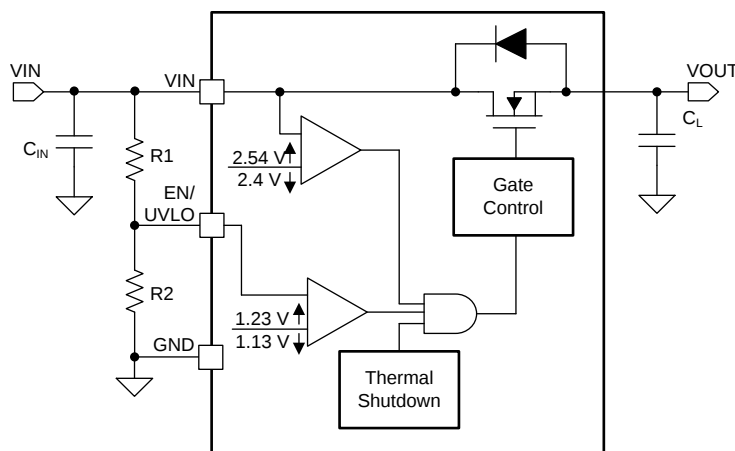


图 18. Configuring UVLO with External Resistor Network

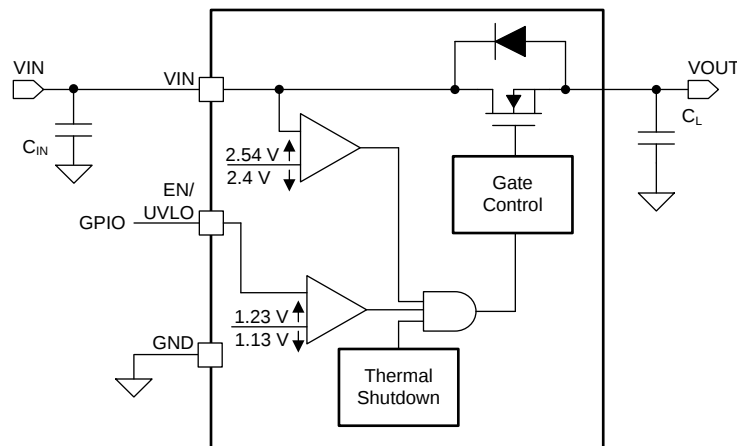


图 19. Using 1.8 V/3.3 V GPIO Signal Directly from Processor

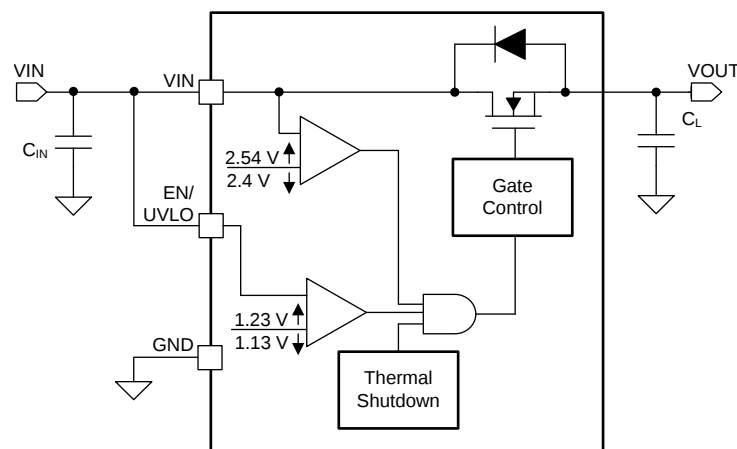


图 20. Default UVLO Threshold V_{UVR} Using No Additional External Components

8.3.4 Adjustable Rise Time (CT)

A capacitor to GND on the CT pin sets the slew rate. The voltage on the CT pin can be as high as 2.5 V. An approximate formula for the relationship between CT and slew rate is shown in 公式 3. This equation accounts for 10% to 90% measurement on VOUT and does NOT apply for $CT < 1 \text{ nF}$.

Use 表 2 to determine rise times for when $CT \geq 1 \text{ nF}$.

$$SR = 46.62 / CT$$

where

- SR is the slew rate (in $\text{V}/\mu\text{s}$)
- CT is the the capacitance value on the CT pin (in pF)

Rise time can be calculated by dividing the input voltage by the slew rate. 表 2 describes rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where VIN is already in steady state condition before the EN/UVLO pin is asserted high.

表 2. Rise Time Table

CT (pF)	RISE TIME (μ s) 10% - 90%, $C_L = 0.1 \mu$ F, $C_{IN} = 1 \mu$ F, $R_L = 10 \Omega$				
	VIN = 18 V	VIN = 12 V	VIN = 9 V	VIN = 5 V	VIN = 3.3 V
0	115	91	78	60	98
470	136	94	80	63	98
1000	310	209	158	91	102
2200	688	464	345	198	135
4700	1430	957	704	397	265
10000	3115	2085	1540	864	550
27000	8230	5460	4010	2245	1430

8.3.5 Thermal Shutdown

The switch disables when the junction temperature (T_J) rises above the thermal shutdown threshold, T_{SD} . The switch re-enables once the temperature drops below the $T_{SD} - T_{SD,HYS}$ value.

8.4 Device Functional Modes

The features of the TPS22810-Q1 depend on the operating mode. 表 3 summarizes the Device Functional Modes.

表 3. Function Table

EN/UVLO	Device State
L	Disabled
H	Enabled

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com (See the Device Support section for more information).

9.1.1 ON and OFF Control

The EN/UVLO pin controls the state of the switch. Asserting EN/UVLO high enables the switch. EN/UVLO is active high and has a low threshold that can interface with low-voltage signals. The EN/UVLO pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

9.1.2 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor must be placed between VIN and GND. A 1- μ F ceramic capacitor, C_{IN} , placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.1.3 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause VOUT to exceed VIN when the system supply is removed. This can result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing VIN dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) can cause slightly more VIN dip upon turnon due to inrush currents.

This can be mitigated by increasing the capacitance on the CT pin for a longer rise time.

9.2 Typical Application

This typical application demonstrates how the TPS22810-Q1 can be used to power downstream modules.

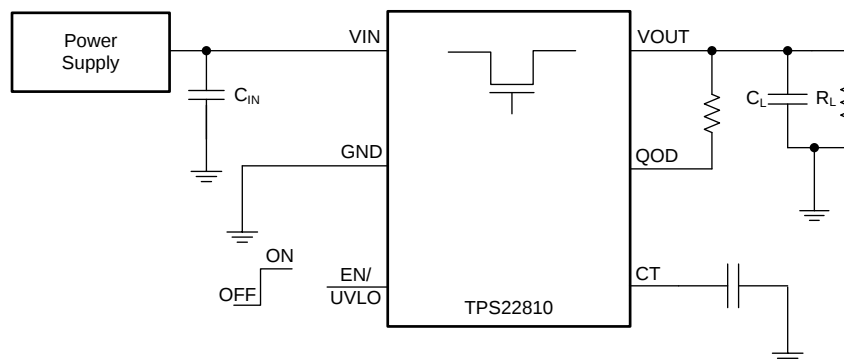


图 21. Typical Application Schematic

Typical Application (接下页)

9.2.1 Design Requirements

For this design example, use the values listed in 表 4:

表 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V _{IN}	12 V
Load current	2 A
C _L	22 μF
Desired fall time	20 ms
Maximum acceptable inrush current	400 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Shutdown Sequencing During Unexpected Power Loss

Using the adjustable Quick Output Discharge function of the TPS22810-Q1, adding a load switch to each power rail can be used to manage the power down sequencing in the event of an unexpected power loss (for example, battery removal). To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down. Next, consult 表 1 to determine appropriate C_L and R_{QOD} values for each power rail's load switch so that the load switches' fall times correspond to the order in which they need to be powered down. In the above example, we must have this power rail's fall time to be 4 ms. Using 公式 2, we can determine the appropriate R_{QOD} to achieve our desired fall time.

Since fall times are measured from 90% of V_{OUT} to 10% of V_{OUT}, using 公式 2, we get 公式 4 and 公式 5.

$$1.2\text{V} = 10.8\text{V} \times e^{-(20\text{ms})/(R_{\text{QOD}} \times (22\mu\text{F}))} \quad (4)$$

$$R_{\text{QOD}} = 413.7 \, \Omega \quad (5)$$

Consulting 图 6, R_{PD} at V_{IN} = 12 V is approximately 250 Ω. Using 公式 1, the required external QOD resistance can be calculated shown in 公式 6 and 公式 7.

$$413.7 \, \Omega = 250 \, \Omega + R_{\text{EXT}} \quad (6)$$

$$R_{\text{EXT}} = 163.7 \, \Omega \quad (7)$$

图 22 through 图 25 are scope shots demonstrating an example of the QOD functionality when power is removed from the device (both ON and VIN are disconnected simultaneously). In the scope shots, the V_{IN} = 12 V and correspond to when R_{QOD} = 1000 Ω, R_{QOD} = 500 Ω, and QOD = V_{OUT} with two values of C_L = 10 μF and 22 μF.

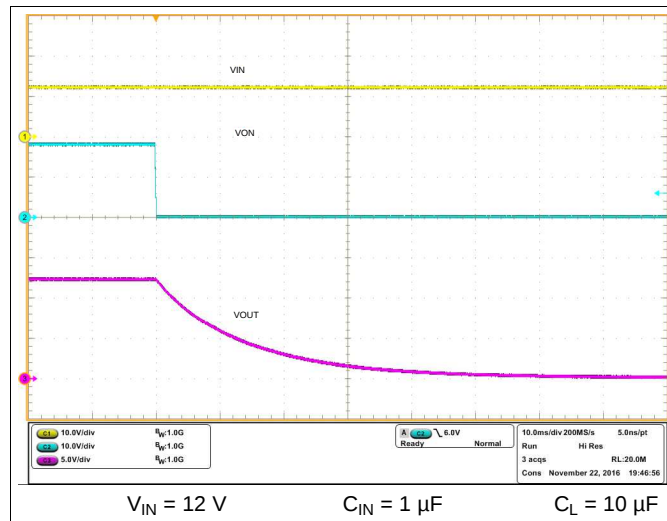


图 22. Fall Time t_F at $V_{IN} = 12\text{ V}$, $R_{QOD} = 1000\ \Omega$

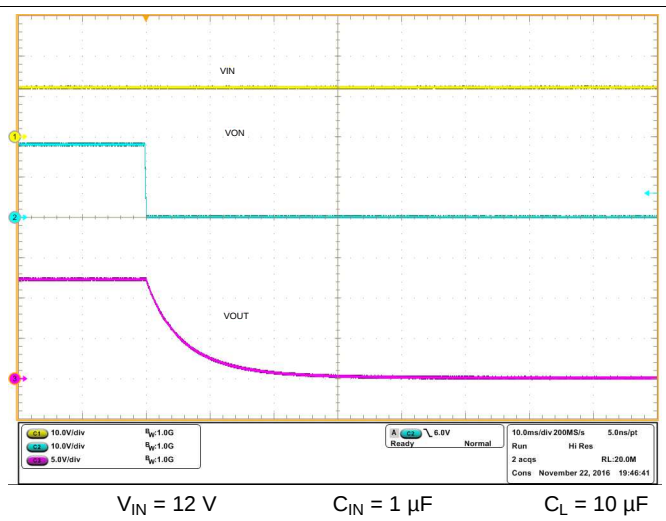


图 23. Fall Time t_F at $V_{IN} = 12\text{ V}$, $R_{QOD} = 500\ \Omega$

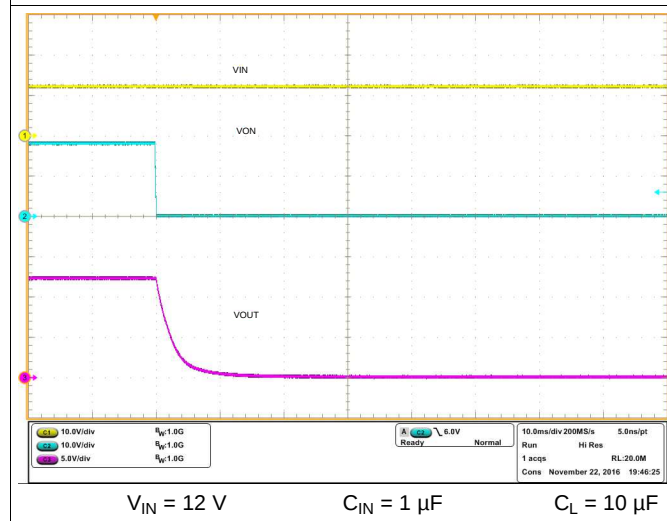


图 24. t_F at $V_{IN} = 12\text{ V}$, $Q_{OD} = V_{OUT}$

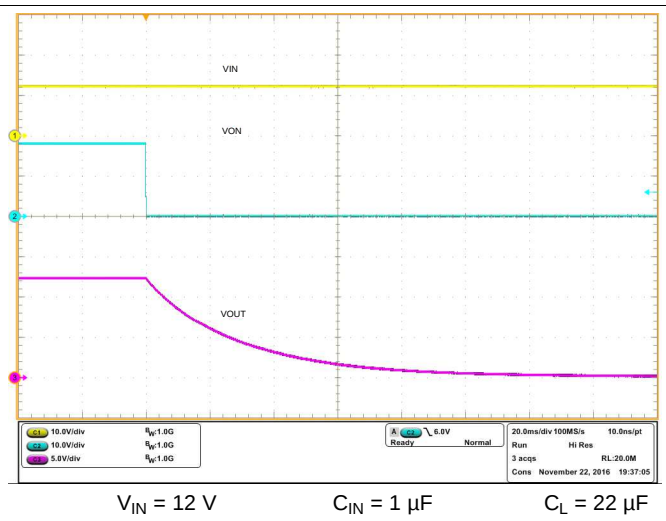
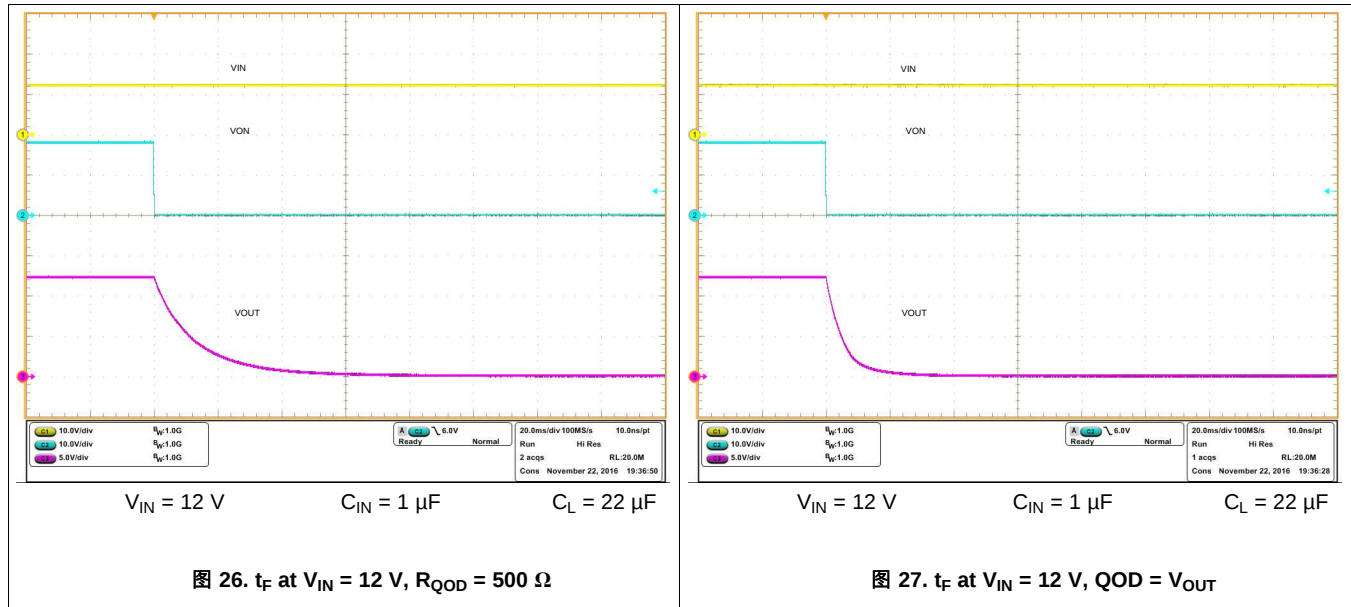


图 25. t_F at $V_{IN} = 12\text{ V}$, $R_{QOD} = 1000\ \Omega$



9.2.2.2 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN conditions of the device. Refer to the R_{ON} specification of the device in the [Electrical Characteristics](#) table of this datasheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use [公式 8](#) to calculate the VIN to VOUT voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON}$$

where

- ΔV is the voltage drop from VIN to VOUT
- I_{LOAD} is the load current
- R_{ON} is the On-resistance of the device for a specific V_{IN}

(8)

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

9.2.2.3 Inrush Current

To determine how much inrush current is caused by the C_L capacitor, use [公式 9](#).

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt}$$

where

- I_{INRUSH} is the amount of inrush caused by C_L
- C_L is the capacitance on VOUT
- dt is the Output Voltage rise time during the ramp up of VOUT when the device is enabled
- dV_{OUT} is the change in V_{OUT} during the ramp up of VOUT when the device is enabled

(9)

The appropriate rise time can be calculated using the design requirements and the inrush current equation. When we calculate the rise time (measured from 10% to 90% of V_{OUT}), we account for this in our dV_{OUT} parameter (80% of $V_{OUT} = 9.6\text{ V}$) shown in [公式 10](#) and [公式 11](#).

$$400\text{ mA} = 22\ \mu\text{F} \times 9.6\text{ V}/dt \quad (10)$$

$$dt = 528\ \mu\text{s} \quad (11)$$

To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 528 μs . Consulting [表 2](#) at $V_{IN} = 12\text{ V}$, $CT = 4700\text{ pF}$ provides a typical rise time of 957 μs . Using this rise time and voltage into [公式 9](#), yields [公式 12](#) and [公式 13](#).

$$I_{Inrush} = 22\ \mu\text{F} \times 9.6\text{ V}/957\ \mu\text{s} \quad (12)$$

$$I_{Inrush} = 220\text{ mA} \quad (13)$$

An appropriate C_L value must be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

9.2.3 Application Curves

See the oscilloscope captures below for an example of how the CT capacitor can be used to reduce inrush current for $V_{IN} = 12$ V. See the [Adjustable Rise Time \(CT\)](#) section for rise times for corresponding CT values.

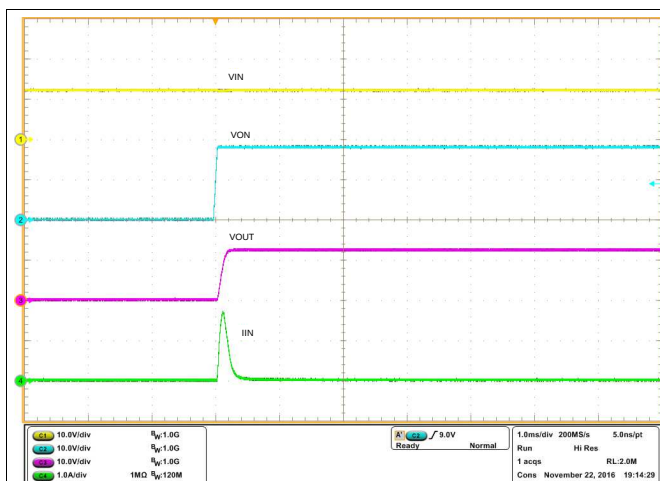


图 28. TPS22810-Q1 Inrush Current With $C_L = 22 \mu F$, $CT = 0$ pF

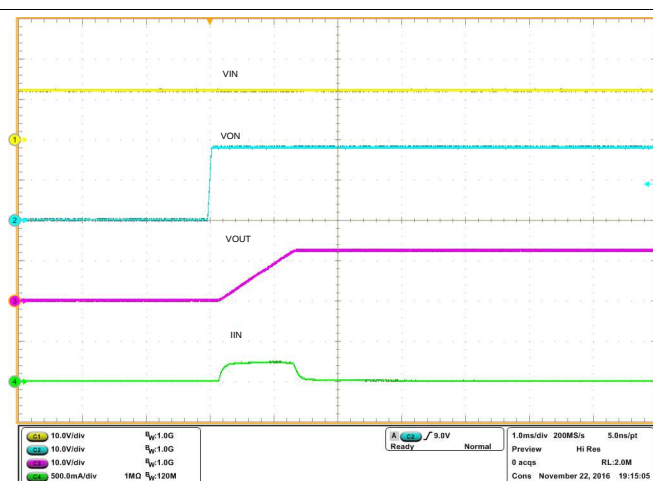


图 29. TPS22810-Q1 Inrush Current with $C_L = 22 \mu F$, $CT = 4700$ pF

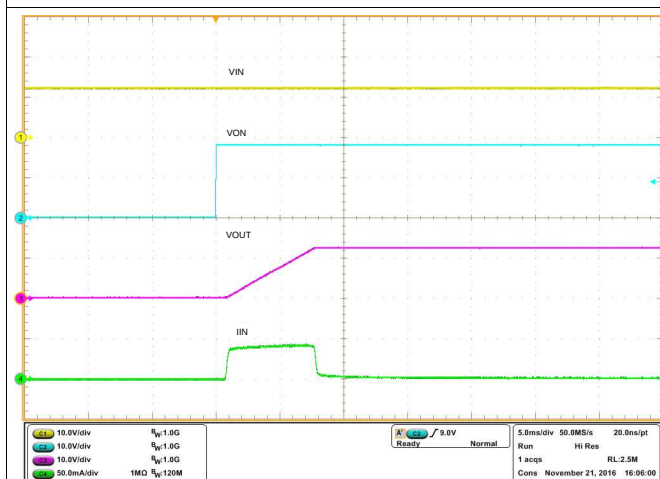


图 30. TPS22810-Q1 Inrush Current With $C_L = 22 \mu F$, $CT = 27000$ pF

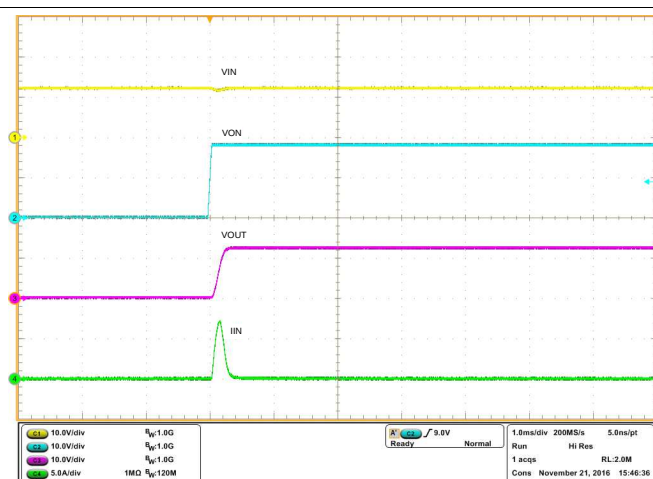
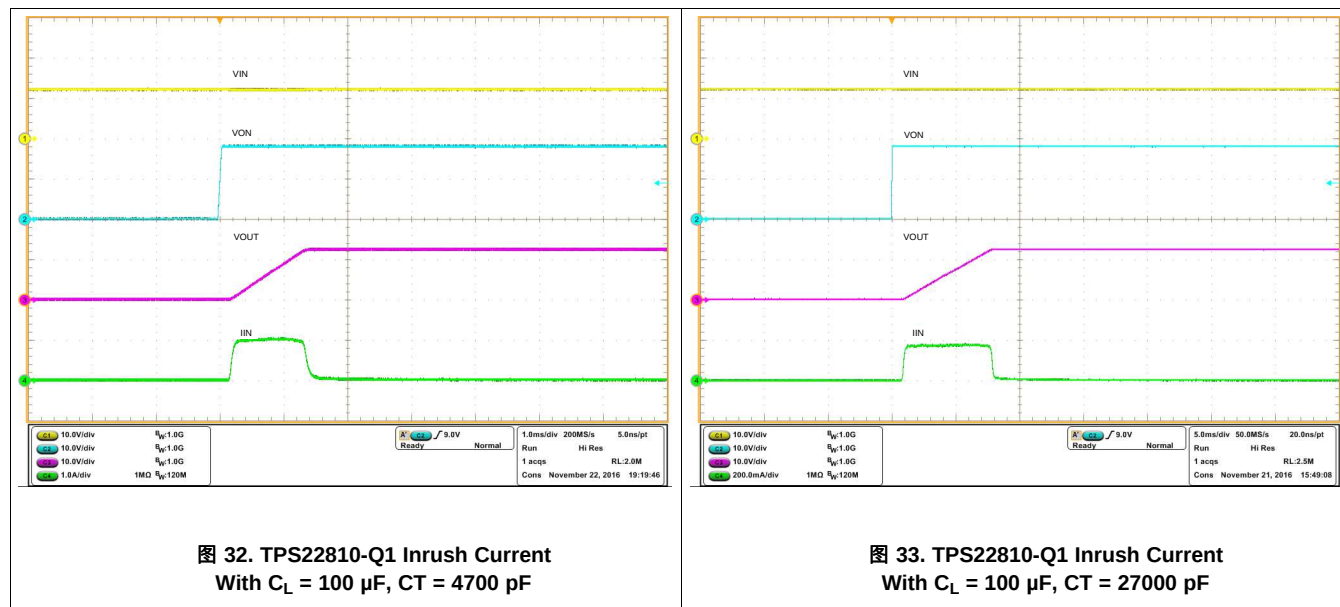


图 31. TPS22810-Q1 Inrush Current With $C_L = 100 \mu F$, $CT = 0$ pF



10 Power Supply Recommendations

The device is designed to operate from a VIN range of 2.7 V to 18 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1- μF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1- μF may be sufficient.

The TPS22810-Q1 operates regardless of power sequencing order. The order in which voltages are applied to VIN and EN/UVLO does not damage the device as long as the voltages do not exceed the absolute maximum operating conditions.

11 Layout

11.1 Layout Guidelines

1. VIN and VOUT traces must be as short and wide as possible to accommodate for high current.
2. The VIN pin must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-μF ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.

11.2 Layout Example

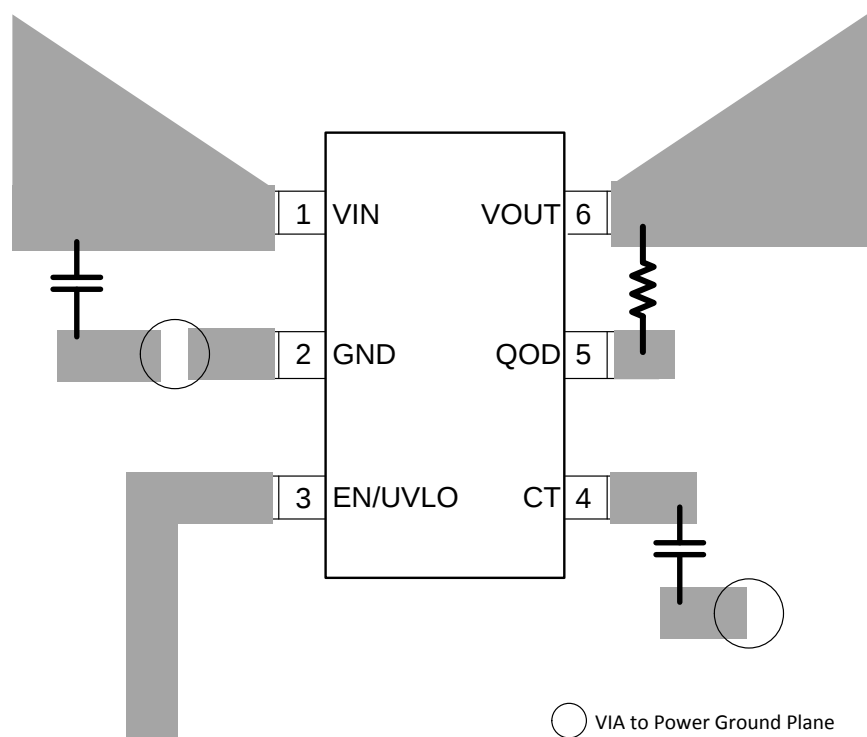


图 34. Recommended Board Layout

11.3 Thermal Considerations

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use 公式 14.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where

- $P_{D(MAX)}$ is the maximum allowable power dissipation
- $T_{J(MAX)}$ is the maximum allowable junction temperature (150°C for the TPS22810-Q1)
- T_A is the ambient temperature of the device
- θ_{JA} is the junction to air thermal impedance. Refer to the [Thermal Information](#) table. This parameter highly depends on the board layout.

(14)

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

关于 TPS22810 PSpice 瞬态模型，请参见 [《TPS22810 PSpice 瞬态模型》](#)

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- [TPS22810 负载开关评估模块](#)
- [选择一个负载开关以代替分立式解决方案](#)
- [负载开关的计时](#)

12.3 接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 ti.com.cn 上您的器件对应的产品文件夹。单击右上角的通知我按钮。点击后，您将每周定期收到已更改的产品信息（如果有的话）。有关更改的详细信息，请查看任意已修订文档的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22810TDBVRQ1	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1EFF
TPS22810TDBVRQ1.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1EFF

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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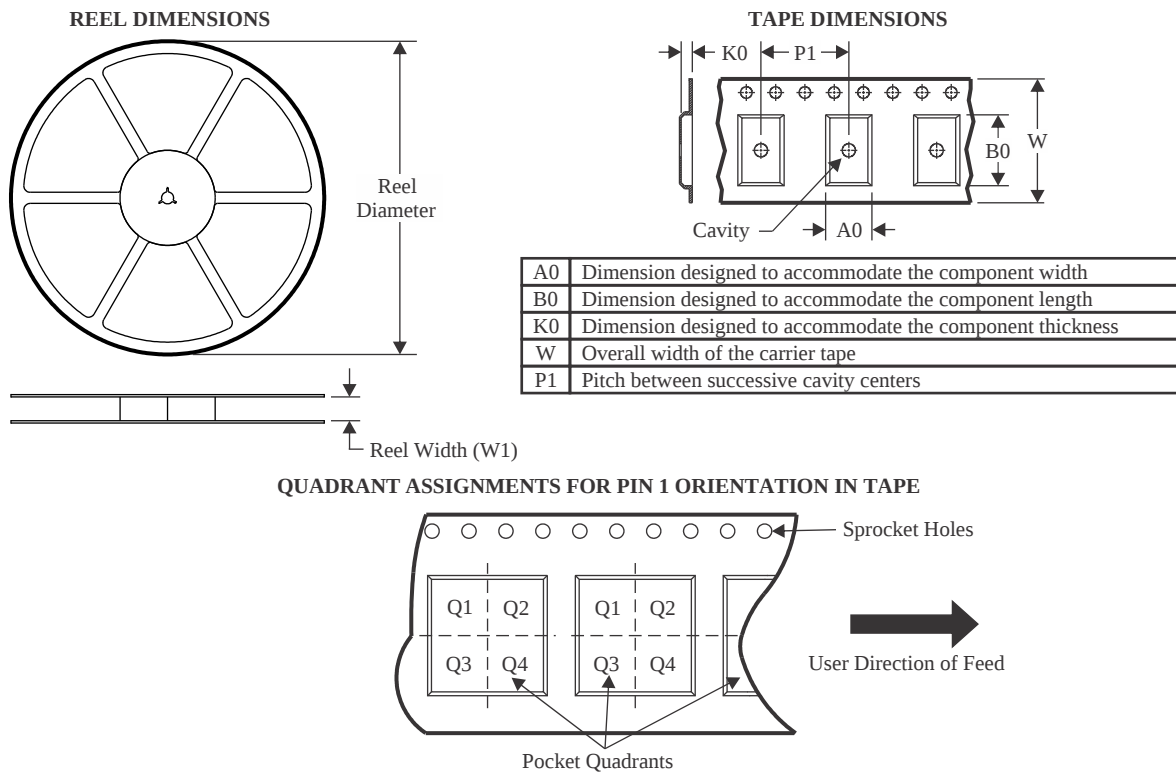
OTHER QUALIFIED VERSIONS OF TPS22810-Q1 :

- Catalog : [TPS22810](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

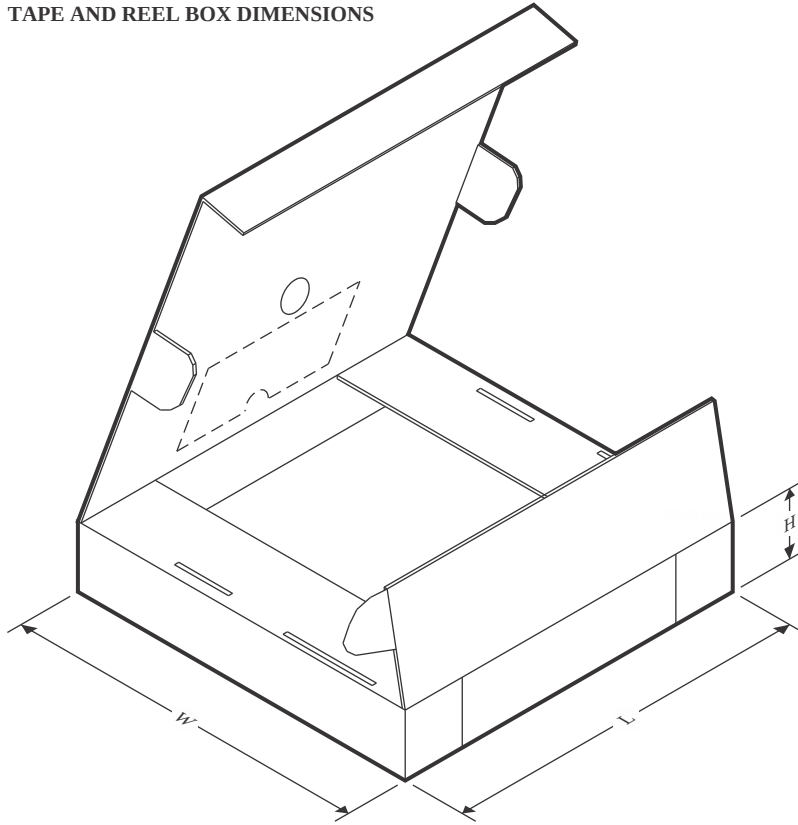
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22810TDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

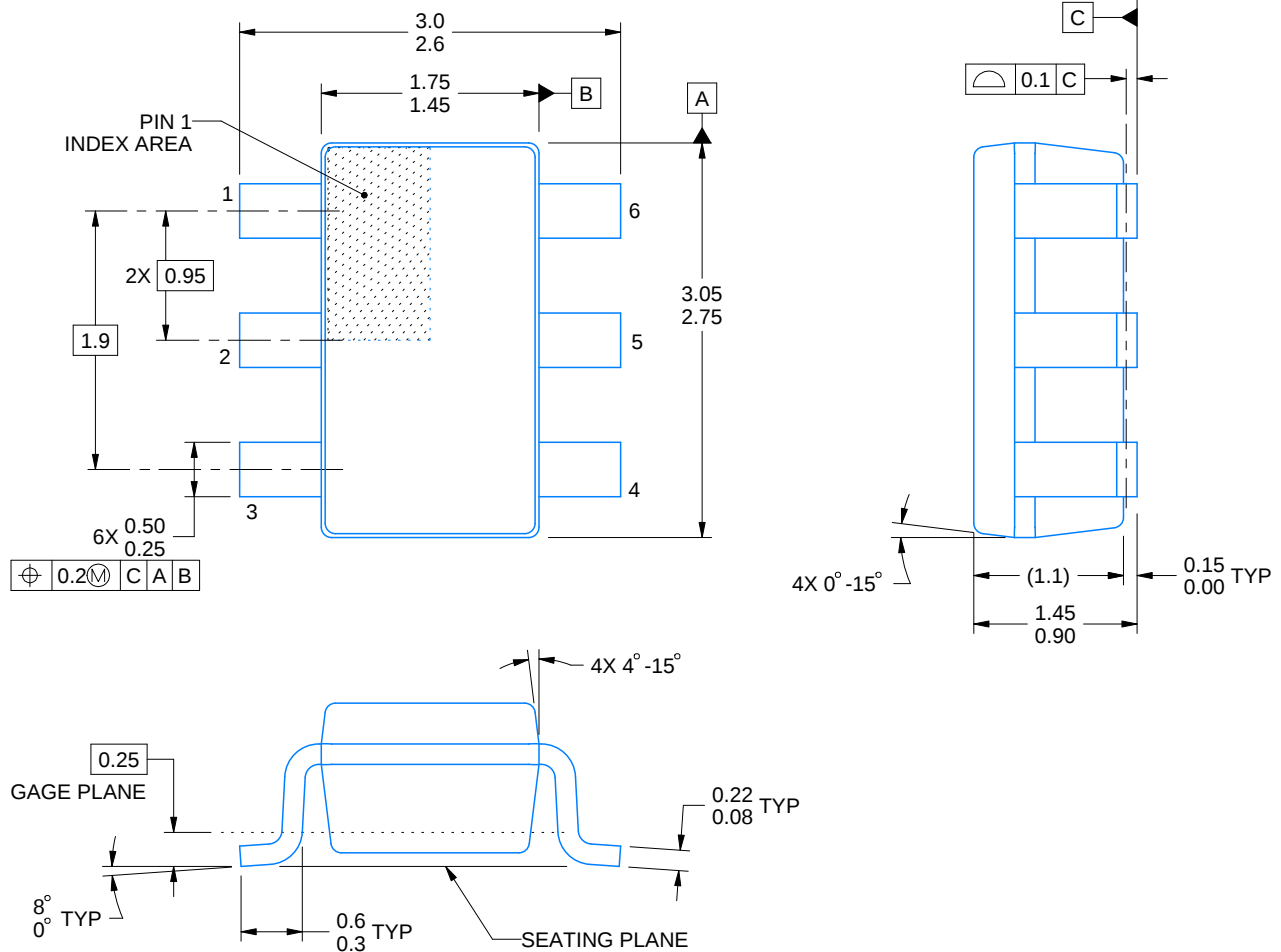


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22810TDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0

DBV0006A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



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NOTES:

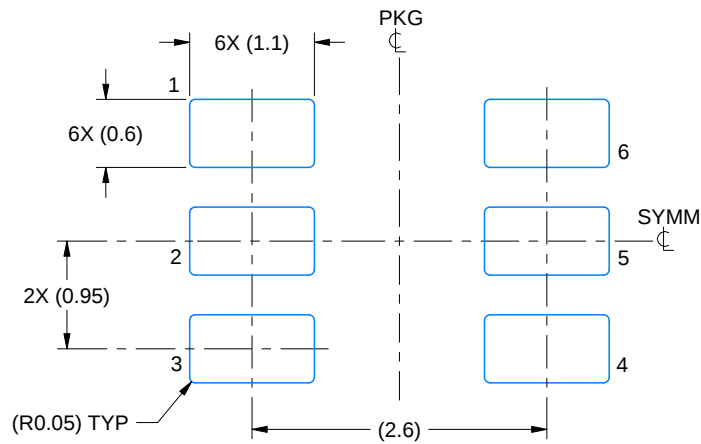
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

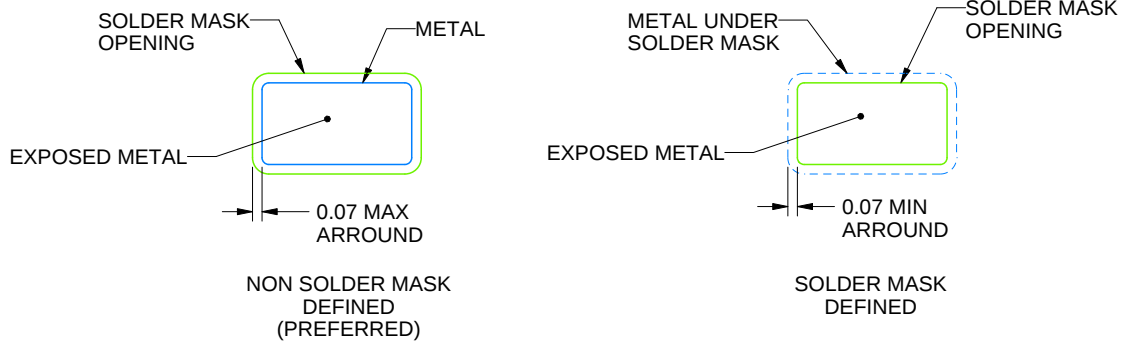
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

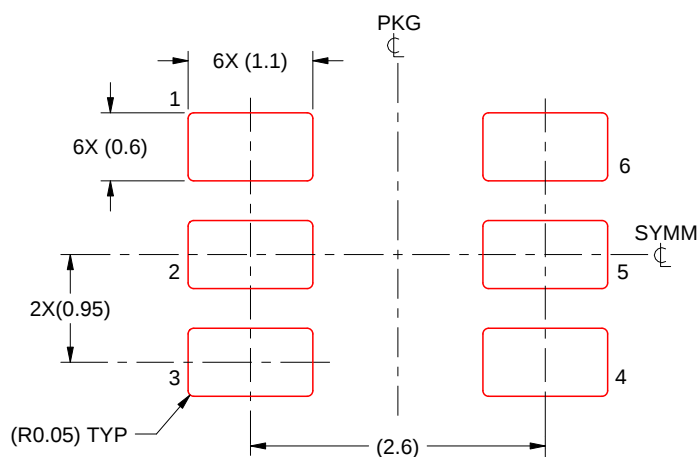
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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