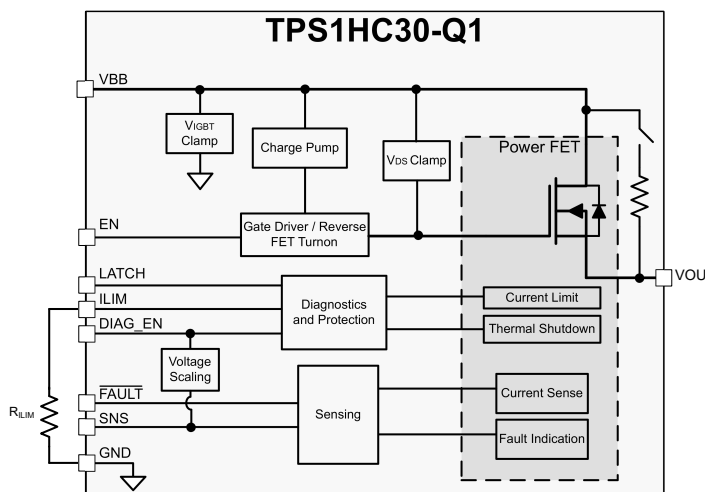


## TPS1HC30-Q1 30mΩ、5A 单通道汽车智能高侧开关

## 1 特性

- 具有全面诊断功能的单通道智能汽车高侧电源开关
  - 开漏状态输出
  - 电流检测模拟输出
- 宽工作电压范围：3V 至 28V
- 低待机电流：85°C 下为 2.5μA
- 工作结温范围：-40°C 至 150°C
- 支持 1.8V、3.3V 和 5V 逻辑电压
- 通过故障检测电压调节功能实现 ADC 保护
- 可编程电流限制和精度 ±15% (3.5A 时)
- 高精度电流检测，1A 时精度为 ±6%
- 保护
  - 过载和短路保护
  - 感性负载负电压钳位
  - 欠压锁定 (UVLO) 保护
  - 具备自恢复功能的热关断和热振荡
  - 接地失效保护和失电保护
  - 反向电池保护
- 诊断
  - 开启和关闭状态输出的开路负载和电池短路检测
  - 过载和接地短路检测
  - 热关断和热振荡检测
- 资格认证
  - 符合面向汽车应用的 AEC-Q100 标准：
    - 温度等级 1：-40°C 至 +125°C，T<sub>A</sub>
  - 通过 ISO7637-2 和 ISO16750-2 电瞬变抗扰度认证
- 14 引脚热增强型 PWP 封装



功能方框图

## 2 应用

- 汽车显示模块
- ADAS 模块
- 座椅舒适模块
- HVAC 控制模块
- 车身控制模块

## 3 说明

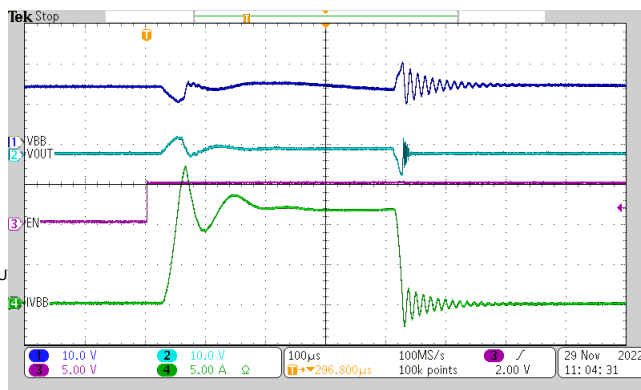
TPS1HC30-Q1 器件是一款具有全方位保护的高侧电源开关，它集成有 NMOS 功率 FET 和电荷泵，专用于对各类负载进行智能控制。该器件凭借着精确的电流检测和可编程电流限制特性在市场上脱颖而出。

由于输入引脚具有 1.5V 低逻辑高电平阈值  $V_{IH}$ ，可以使用低至 1.8V 的 MCU。高精度电流检测功能可实现更好的实时监测效果和更准确的诊断，无需进一步校准。外部高精度电流限制功能允许根据应用设置电流限制值。该器件通过在启动或短路条件下有效地钳制浪涌电流，极大地提高了系统的可靠性。TPS1HC30-Q1 器件可用作各种阻性、感性和容性负载（包括低瓦数灯泡、LED、继电器、电磁阀和加热器）的高侧电源开关。

## 封装信息

| 器件型号        | 封装 <sup>(1)</sup> | 封装尺寸 (标称值)      |
|-------------|-------------------|-----------------|
| TPS1HC30-Q1 | PWP (HTSSOP、14)   | 4.40mm × 5.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



电流限制应用



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision * (July 2022) to Revision A (December 2022) | Page     |
|---|----------|
| • 将器件状态从 <i>预告信息</i> 更改为 <i>量产数据</i> .....                        | <b>1</b> |

## 5 Pin Configuration and Functions

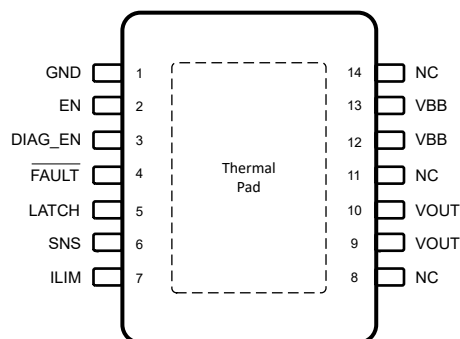


图 5-1. PWP Package, 14-Pin HTSSOP (Top View)

表 5-1. Pin Functions

| PIN         |         | TYPE  | DESCRIPTION  |
|-------------|---------|-------|--|
| NO.         | NAME    |       |  |
| 1           | GND     | Power | Ground of device. Connect to resistor-diode ground network to have reverse battery protection.     |
| 2           | EN      | I     | Input control for channel activation, internal pulldown  |
| 3           | DIAG_EN | I     | Enable-disable pin for diagnostics, internal pulldown  |
| 4           | FAULT   | O     | Open-drain global fault output. Referred to FAULT, FLT, or fault pin.                              |
| 5           | LATCH   | I     | Thermal shutdown behavior, latch-off or auto-retry, internal pulldown                              |
| 6           | SNS     | O     | Output corresponding sense value based on sense ratio  |
| 7           | ILIM    | O     | Adjustable current limit. Short to ground or leave floating if external current limit is not used. |
| 8, 11, 14   | NC      | N/A   | No internal connection   |
| 9, 10       | VOUT    | Power | Output of high-side switch, connected to load  |
| 12, 13      | VBB     | Power | Power supply   |
| Thermal Pad | Pad     | —     | Thermal Pad, internally shorted to ground  |

### Recommended Connection for Unused Pins

The TPS1HC30-Q1 is designed to provide an enhanced set of diagnostic and protection features. However, if the system design only allows for a limited number of I/O connections, some pins can be considered as optional.

表 5-2. Connections For Optional Pins

| PIN NAME | CONNECTION IF NOT USED                      | IMPACT IF NOT USED  |
|----------|---|---|
| SNS      | Ground through 1-k $\Omega$ resistor        | Analog sense is not available.  |
| LATCH    | Float or ground through $R_{PROT}$ resistor | With LATCH unused, the device auto-retries after a fault. If latched behavior is desired, but the system describes limited I/O, it is possible to use one microcontroller output to control the latch function of several high side channels. |
| ILIM     | Float                                       | If the ILIM pin is left floating, the device is set to the default internal current-limit threshold. This impact is considered a fault state for the device.  |
| DIA_EN   | Float or ground through $R_{PROT}$ resistor | With DIA_EN unused, the analog sense, open-load, and short-to-battery diagnostics are not available.  |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|  |  | MIN   | MAX  | UNIT |
|--|--|-------|------|------|
| Maximum continuous supply voltage, $V_{BB}$  |  |       | 28   | V    |
| Load dump voltage, $V_{LD}$                  | ISO16750-2:2010(E)   |       | 35   | V    |
| Reverse Polarity Voltage                     | Maximum duration of 3 minutes and with the application circuit | - 18  |      | V    |
| Enable pin current, $I_{EN}$                 | Enable pin current, $I_{EN}$                                   | - 1   | 20   | mA   |
| Enable pin voltage, $V_{EN}$                 |  | - 1   | 7    | V    |
| Diagnostic Enable pin current, $I_{DIA\_EN}$ |  | - 1   | 20   | mA   |
| Diagnostic Enable pin voltage, $V_{DIA\_EN}$ |  | - 1   | 7    | V    |
| Sense pin current, $I_{SNS}$                 |  | - 100 | 10   | mA   |
| Sense pin voltage, $V_{SNS}$                 |  | - 1   | 5.5  | V    |
| Latch pin current, $I_{LATCH}$               |  | -1    | 10   | mA   |
| Latch pin voltage, $V_{LATCH}$               |  | - 1   | 7    | V    |
| FLT pin current, $I_{FLT}$                   |  | -30   | 10   | mA   |
| FLT pin voltage, $V_{FLT}$                   |  | - 0.3 | 7    | V    |
| Reverse ground current, $I_{GND}$            | $V_{BB} < 0$ V   |       | - 50 | mA   |
| Storage temperature, $T_{stg}$               |  | - 65  | 150  | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

|             |  |  |                             | VALUE | UNIT |
|-------------|--|--|-----------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge <sup>(1)</sup> | Human-body model (HBM), per AEC Q100-002 Classification Level 2 <sup>(2)</sup> | All pins except VS and VOUT | ±2000 | V    |
|             |  |  | VS and VOUT                 | ±4000 |      |
|             |  | Charged-device model (CDM), per AEC Q100-011 Classification Level C5           | All pins                    | ±750  |      |

- (1) All ESD strikes are with reference from the pin mentioned to GND  
 (2) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.

### 6.3 建议运行条件

在自然通风条件下的工作温度范围内测得 (除非另有说明) <sup>(1)</sup>

|                |                       | 最小值 | 最大值 | 单位 |
|----------------|-----------------------|-----|-----|----|
| $V_{VBB\_NOM}$ | 标称电源电压 <sup>(1)</sup> | 3.5 | 18  | V  |
| $V_{VBB\_EXT}$ | 扩展电源电压 <sup>(2)</sup> | 2.6 | 28  | V  |
| $V_{VBB\_SC}$  | 短路电源电压能力              |     | 28  | V  |
| $V_{EN}$       | 使能电压                  | -1  | 5.5 | V  |
| $V_{DIA\_EN}$  | 诊断使能电压                | -1  | 5.5 | V  |
| $V_{LATCH}$    | 门锁电压                  | -1  | 5.5 | V  |
| $V_{SNS}$      | 检测电压                  | -1  | 7   | V  |
| $T_A$          | 自然通风工作温度              | -40 | 125 | °C |

- (1) 所有工作电压条件均以器件 GND 为基准进行测量。

- (2) 器件将在更广的工作电压范围工作，但某些时序参数值可能不适用。有关使用的电压，请参阅相应章节。此外，有关更多说明，请参见节 9.3。

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1) (2)</sup> |  | TPS1HC30-Q1  | UNIT |
|-----------------------------------|--|--------------|------|
|                                   |  | PWP (HTSSOP) |      |
|                                   |  | 14 PINS      |      |
| $R_{\theta JA}$                   | Junction-to-ambient thermal resistance       | 44.2         | °C/W |
| $R_{\theta JC(top)}$              | Junction-to-case (top) thermal resistance    | 33.8         | °C/W |
| $R_{\theta JB}$                   | Junction-to-board thermal resistance         | 19.2         | °C/W |
| $\psi_{JT}$                       | Junction-to-top characterization parameter   | 1.4          | °C/W |
| $\psi_{JB}$                       | Junction-to-board characterization parameter | 19.2         | °C/W |
| $R_{\theta JC(bot)}$              | Junction-to-case (bottom) thermal resistance | 5.0          | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [SPRA953](#) application report.  
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

## 6.5 Electrical Characteristics

$V_{BB} = 6\text{ V to }28\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted); Typical application is  $13.5\text{ V}$ ,  $10\ \Omega$ , RILIM=Open (unless otherwise specified)

| PARAMETER                     |  | TEST CONDITIONS  |                                  | MIN | TYP  | MAX | UNIT |   |
|-------------------------------|--|--|----------------------------------|-----|------|-----|------|---|
| INPUT VOLTAGE AND CURRENT     |  |  |                                  |     |      |     |      |   |
| V <sub>Clamp</sub>            | V <sub>DS</sub> clamp voltage                                    |  | T <sub>J</sub> =25°C             | 35  |      | 43  | V    |   |
|                               |  |  | T <sub>J</sub> = - 40°C to 150°C | 33  |      | 45  | V    |   |
| V <sub>UVLOR</sub>            | V <sub>BB</sub> undervoltage lockout rising                      | Measured with respect to the GND pin of the device   |                                  | 3.0 | 3.5  | 4.0 | V    |   |
| V <sub>UVLOF</sub>            | V <sub>BB</sub> undervoltage lockout falling                     |  |                                  | 2.4 | 2.6  | 3.0 | V    |   |
| I <sub>SB</sub>               | Standby current (total device leakage including MOSFET channel)  | V <sub>BB</sub> ≤ 18 V, V <sub>EN</sub> = V <sub>DIA_EN</sub> = 0 V, V <sub>OUT</sub> = 0 V                                | T <sub>J</sub> = 25°C            |     |      | 0.3 | μA   |   |
|                               |  |  | T <sub>J</sub> = 85°C            |     |      | 2.5 | μA   |   |
|                               |  |  | T <sub>J</sub> = 125°C           |     |      | 9   | μA   |   |
| I <sub>OUT(standby)</sub>     | Output leakage current   | V <sub>BB</sub> ≤ 18 V, V <sub>EN</sub> = V <sub>DIA_EN</sub> = 0 V, V <sub>OUT</sub> = 0 V                                | T <sub>J</sub> = 25°C            |     | 0.01 | 0.3 | μA   |   |
|                               |  |  | T <sub>J</sub> = 85°C            |     |      | 2.5 | μA   |   |
| I <sub>DIA</sub>              | Current consumption in diagnostic mode                           | V <sub>BB</sub> ≤ 18 V, I <sub>SNS</sub> = 0 mA<br>V <sub>EN</sub> = 0 V, V <sub>DIA_EN</sub> = 5 V, V <sub>OUT</sub> = 0V |                                  |     | 1.3  | 3   | mA   |   |
| I <sub>Q</sub>                | Quiescent current channel enabled                                | V <sub>BB</sub> ≤ 28 V<br>V <sub>EN</sub> = V <sub>DIA_EN</sub> = 5 V, I <sub>OUTx</sub> = 0 A                             |                                  |     | 1.6  | 3   | mA   |   |
| I <sub>L</sub> NOM            | Continuous load current  | Channel enabled, T <sub>AMB</sub> = 85°C   |                                  |     | 4.5  |     | A    |   |
| t <sub>STBY</sub>             | Standby mode delay time  | V <sub>ENx</sub> = V <sub>DIA_EN</sub> = 0 V to standby  |                                  |     | 20   |     | ms   |   |
| RON CHARACTERISTICS           |  |  |                                  |     |      |     |      |   |
| R <sub>ON</sub>               | On-resistance (Includes MOSFET channel and metallization on die) | 6 V ≤ V <sub>BB</sub> ≤ 28 V,<br>I <sub>OUT</sub> = 1 A  | T <sub>J</sub> = 25°C            |     | 30   |     | m Ω  |   |
|                               |  |  | T <sub>J</sub> = 150°C           |     |      | 57  | m Ω  |   |
|                               |  | 3 V ≤ V <sub>BB</sub> ≤ 6 V,<br>I <sub>OUT</sub> =1 A  | T <sub>J</sub> = 25°C            |     |      | 57  | m Ω  |   |
|                               |  |  | T <sub>J</sub> = 150°C           |     |      | 75  | m Ω  |   |
| R <sub>ON(REV)</sub>          | On-resistance during reverse polarity                            | -18 V ≤ V <sub>BB</sub> ≤ -6 V   | T <sub>J</sub> = 25°C            |     | 30   |     | m Ω  |   |
|                               |  |  | T <sub>J</sub> = 150°C           |     |      | 57  | m Ω  |   |
| V <sub>F</sub>                | Source-to-drain body diode voltage                               | V <sub>EN</sub> = 0 V I <sub>OUT</sub> = - 1 A   |                                  |     | 0.3  | 0.7 | 1    | V |
| CURRENT SENSE CHARACTERISTICS |  |  |                                  |     |      |     |      |   |

## 6.5 Electrical Characteristics (continued)

$V_{BB} = 6\text{ V to } 28\text{ V}$ ,  $T_A = -40^\circ\text{C to } 125^\circ\text{C}$  (unless otherwise noted); Typical application is  $13.5\text{ V}$ ,  $10\ \Omega$ ,  $R_{ILIM} = \text{Open}$  (unless otherwise specified)

| PARAMETER                     |  | TEST CONDITIONS  |   | MIN                   | TYP  | MAX  | UNIT |
|-------------------------------|--|--|---|-----------------------|------|------|------|
| K <sub>SNS</sub>              | Current sense ratio<br>I <sub>OUT</sub> / I <sub>SNS</sub>                     | I <sub>OUT</sub> = 1.5 A   |   | 1560                  |      |      |      |
| I <sub>SNSI</sub>             | Current sense current and accuracy   | V <sub>BB</sub> > V <sub>BB_ISNS</sub> , V <sub>EN</sub> = V <sub>DIA_EN</sub> = 5 V | I <sub>OUT</sub> = 6 A                    | 3.8                   |      |      | mA   |
|                               |  |  |   | - 3                   | 3    | %    |      |
|                               |  |  | I <sub>OUT</sub> = 3 A                    | 1.92                  |      |      | mA   |
|                               |  |  |   | - 4                   | 4    | %    |      |
|                               |  |  | I <sub>OUT</sub> = 1.5 A                  | 0.96                  |      |      | mA   |
|                               |  |  |   | - 4                   | 4    | %    |      |
|                               |  |  | I <sub>OUT</sub> = 750 mA                 | 0.48                  |      |      | mA   |
|                               |  |  |   | - 6                   | 6    | %    |      |
|                               |  |  | I <sub>OUT</sub> = 300 mA                 | 0.192                 |      |      | mA   |
|                               |  |  |   | - 10                  | 10   | %    |      |
|                               |  |  | I <sub>OUT</sub> = 150 mA                 | 0.096                 |      |      | mA   |
|                               |  |  |   | - 15                  | 15   | %    |      |
|                               |  |  | I <sub>OUT</sub> = 75 mA                  | 0.0481                |      |      | mA   |
|                               |  |  |   | - 25                  | 25   | %    |      |
|                               |  |  | I <sub>OUT</sub> = 30 mA                  | 0.0192                |      |      | mA   |
|                               |  |  |   | - 40                  | 40   | %    |      |
|                               |  |  | I <sub>OUT</sub> = 15 mA                  | 0.0096                |      |      | mA   |
|                               |  |  |   | - 60                  | 60   | %    |      |
|                               |  |  | I <sub>OUT</sub> = 7.5 mA                 | 0.0048                |      |      | mA   |
|                               |  |  |   | -80                   | 80   | %    |      |
| SNS CHARACTERISTICS           |  |  |   |                       |      |      |      |
| V <sub>SNSFH</sub>            | V <sub>SNS</sub> fault high-level  | V <sub>DIA_EN</sub> = 5 V  |   | 4.2                   | 5    | 5.77 | V    |
|                               |  | V <sub>DIA_EN</sub> = 3.3 V  |   | 3.3                   | 3.5  | 3.75 | V    |
|                               |  | V <sub>DIA_EN</sub> = V <sub>IH</sub>  |   | 2.8                   | 3.15 | 3.5  | V    |
| I <sub>SNSFH</sub>            | I <sub>SNS</sub> fault high-level  | V <sub>DIA_EN</sub> > V <sub>IH,DIA_EN</sub>   |   | 6.6                   |      |      | mA   |
| V <sub>BB_ISNS</sub>          | V <sub>BB</sub> headroom needed for full current sense and fault functionality | V <sub>DIAG_EN</sub> = 3.3 V   |   | 5.3                   |      |      | V    |
| V <sub>BB_ISNS</sub>          | V <sub>BB</sub> headroom needed for full current sense and fault functionality | V <sub>DIAG_EN</sub> = 5 V   |   | 6.5                   |      |      | V    |
| CURRENT LIMIT CHARACTERISTICS |  |  |   |                       |      |      |      |
| I <sub>CL_LINPK</sub>         | Linear Mode peak   | T <sub>J</sub> = - 40°C to 150°C dI/dt < 0.01 A/ms                                   | R <sub>ILIM</sub> = 7.15 kΩ to 71.5 kΩ    | 1.4 × I <sub>CL</sub> |      |      | A    |
| I <sub>CL_ENPS</sub>          | Peak current enabling into permanent short                                     | T <sub>J</sub> = - 40°C to 150°C   | R <sub>ILIM</sub> = 7.15 kΩ to 71.5 kΩ    | 2 × I <sub>CL</sub>   |      |      | A    |
| I <sub>OVCR</sub>             | OVCR Peak current threshold when short is applied while switch enabled         | T <sub>J</sub> = - 40°C to 150°C   | R <sub>ILIM</sub> ≥ 35 kΩ                 | 15                    |      |      | A    |
|                               |  |  | 15 kΩ ≤ R <sub>ILIM</sub> < 35 kΩ         | 23                    |      |      | A    |
|                               |  |  | R <sub>ILIM</sub> < 15kΩ                  | 33                    |      |      | A    |
| I <sub>CL</sub>               | I <sub>CL</sub> Current Limit Threshold <sup>(1)</sup>                         | T <sub>J</sub> = - 40°C to 150°C, V <sub>DS</sub> = 3 V                              | R <sub>ILIM</sub> = GND                   | 9.1                   | 13   | 16.9 | A    |
|                               |  |  | R <sub>ILIM</sub> = open, or out of range | 5                     |      |      | A    |

## 6.5 Electrical Characteristics (continued)

$V_{BB} = 6\text{ V to }28\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted); Typical application is  $13.5\text{ V}$ ,  $10\ \Omega$ ,  $R_{ILIM} = \text{Open}$  (unless otherwise specified)

| PARAMETER                  |  | TEST CONDITIONS   |                              | MIN  | TYP  | MAX   | UNIT    |
|----------------------------|--|---|------------------------------|------|------|-------|---------|
| K <sub>CL</sub>            | Current Limit Ratio <sup>(1)</sup>                 | T <sub>J</sub> = - 40°C to 150°C,<br>V <sub>DS</sub> = 3 V  | R <sub>ILIM</sub> = 7.15 k Ω | 65.6 | 87.5 | 109.4 | A * k Ω |
|                            |  |   | R <sub>ILIM</sub> = 25 k Ω   | 76.5 | 90   | 103.5 | A * k Ω |
|                            |  |   | R <sub>ILIM</sub> = 71.5 k Ω | 69   | 95   | 115   | A * k Ω |
| FAULT CHARACTERISTICS      |  |   |                              |      |      |       |         |
| R <sub>VOL</sub>           | Open-load (OL) detection internal pull-up resistor | V <sub>EN</sub> = 0 V, V <sub>DIA_EN</sub> = 5 V  | 150                          |      |      | k Ω   |         |
| t <sub>OL</sub>            | Open-load (OL) detection deglitch time             | V <sub>EN</sub> = 0 V, V <sub>DIA_EN</sub> = 5 V, When V <sub>BB</sub> - V <sub>OUT</sub> < V <sub>OL</sub> , duration longer than t <sub>OL</sub> . Openload detected. | 400                          | 1000 | μs   |       |         |
| V <sub>OL</sub>            | Open-load (OL) detection voltage                   | V <sub>EN</sub> = 0 V, V <sub>DIA_EN</sub> = 5 V  | 1.5                          |      |      | V     |         |
| V <sub>FLT</sub>           | FLT low output voltage                             | I <sub>FLT</sub> = 2.5 mA   | 0.5                          |      |      | V     |         |
| t <sub>OL1</sub>           | OL and STB indication-time from EN falling         | V <sub>EN</sub> = 5 V to 0 V, V <sub>DIA_EN</sub> = 5 V<br>I <sub>OUT</sub> = 0 mA, V <sub>OUT</sub> = V <sub>BB</sub> - V <sub>OL</sub>                                | 500                          | 1000 | μs   |       |         |
| t <sub>OL2</sub>           | OL and STB indication-time from DIA_EN rising      | V <sub>EN</sub> = 0 V, V <sub>DIA_EN</sub> = 0 V to 5 V<br>I <sub>OUT</sub> = 0 mA, V <sub>OUT</sub> = V <sub>BB</sub> - V <sub>OL</sub>                                | 1000                         |      |      | μs    |         |
| T <sub>ABS</sub>           | Thermal shutdown                                   |   | 165                          |      |      | °C    |         |
| T <sub>REL</sub>           | Relative thermal shutdown                          |   | 85                           |      |      | °C    |         |
| T <sub>HYS</sub>           | Thermal shutdown hysteresis                        |   | 25                           |      |      | °C    |         |
| t <sub>FAULT_FLT</sub>     | Fault indication-time                              | V <sub>DIA_EN</sub> = 5 V<br>Time between fault and FLT asserting   | 60                           |      |      | μs    |         |
| t <sub>FAULT_SNS</sub>     | Fault indication-time                              | V <sub>DIA_EN</sub> = 5 V<br>Time between fault and I <sub>SNS</sub> settling at V <sub>SNSFH</sub>   | 60                           |      |      | μs    |         |
| t <sub>RETRY</sub>         | Retry time   | Time from fault shutdown until switch re-enable (thermal shutdown).   | 1                            | 2    | 3    | ms    |         |
| EN PIN CHARACTERISTICS     |  |   |                              |      |      |       |         |
| V <sub>IL, EN</sub>        | Input voltage low-level                            | No GND Network  | 0.8                          |      |      | V     |         |
| V <sub>IH, EN</sub>        | Input voltage high-level                           | No GND Network  | 1.5                          |      |      | V     |         |
| V <sub>IHYS, EN</sub>      | Input voltage hysteresis                           |   | 280                          |      |      | mV    |         |
| R <sub>EN</sub>            | Internal pulldown resistor                         |   | 200                          | 350  | 500  | k Ω   |         |
| I <sub>IL, EN</sub>        | Input current low-level                            | V <sub>EN</sub> = 0.8 V   | 2.2                          |      |      | μA    |         |
| I <sub>IH, EN</sub>        | Input current high-level                           | V <sub>EN</sub> = 5 V   | 14                           |      |      | μA    |         |
| DIA_EN PIN CHARACTERISTICS |  |   |                              |      |      |       |         |
| V <sub>IL, DIA_EN</sub>    | Input voltage low-level                            | No GND Network  | 0.8                          |      |      | V     |         |
| V <sub>IH, DIA_EN</sub>    | Input voltage high-level                           | No GND Network  | 1.5                          |      |      | V     |         |
| V <sub>IHYS, DIA_EN</sub>  | Input voltage hysteresis                           |   | 280                          |      |      | mV    |         |
| R <sub>DIA_EN</sub>        | Internal pulldown resistor                         |   | 100                          | 250  | 500  | k Ω   |         |
| I <sub>IL, DIA_EN</sub>    | Input current low-level                            | V <sub>DIA_EN</sub> = 0.8 V   | 2.2                          |      |      | μA    |         |
| I <sub>IH, DIA_EN</sub>    | Input current high-level                           | V <sub>DIA_EN</sub> = 5 V   | 14                           |      |      | μA    |         |
| LATCH PIN Characteristics  |  |   |                              |      |      |       |         |
| V <sub>IL, LATCH</sub>     | Input voltage low-level                            | No GND Network  | 0.8                          |      |      | V     |         |
| V <sub>IH, LATCH</sub>     | Input voltage high-level                           | No GND Network  | 1.5                          |      |      | V     |         |
| V <sub>IHYS, LATCH</sub>   | Input voltage hysteresis                           |   | 280                          |      |      | mV    |         |
| R <sub>LATCH</sub>         | Internal pulldown resistor                         |   | 0.7                          | 1    | 1.3  | M Ω   |         |

## 6.5 Electrical Characteristics (continued)

$V_{BB} = 6\text{ V to }28\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted); Typical application is  $13.5\text{ V}$ ,  $10\ \Omega$ , RILIM=Open (unless otherwise specified)

| PARAMETER       |                          | TEST CONDITIONS            | MIN | TYP | MAX | UNIT          |
|-----------------|--------------------------|----------------------------|-----|-----|-----|---------------|
| $I_{IL, LATCH}$ | Input current low-level  | $V_{LATCH} = 0.8\text{ V}$ |     | 2.2 |     | $\mu\text{A}$ |
| $I_{IH, LATCH}$ | Input current high-level | $V_{LATCH} = 5\text{ V}$   |     | 14  |     | $\mu\text{A}$ |

(1) Current limit regulation value will vary with increase of VDS voltage. For more information, see [节 8.3.2](#)

## 6.6 SNS Timing Characteristics

$V_{BB} = 6\text{ V to }18\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                         |   | TEST CONDITIONS   | MIN | TYP | MAX | UNIT          |
|-----------------------------------|---|---|-----|-----|-----|---------------|
| <b>SNS TIMING - CURRENT SENSE</b> |   |   |     |     |     |               |
| $t_{SNSION1}$                     | Settling time from rising edge of DIA_EN<br>50% of $V_{DIA\_EN}$ to 90% of settled ISNS                         | $V_{ENx} = 5\text{ V}$ , $V_{DIA\_EN} = 0\text{ V to }5\text{ V}$<br>$R_{SNS} = 1\text{ k}\Omega$ , $I_L = 1\text{ A}$                                |     |     | 30  | $\mu\text{s}$ |
|                                   |   | $V_{EN} = 5\text{ V}$ , $V_{DIA\_EN} = 0\text{ V to }5\text{ V}$<br>$R_{SNS} = 1\text{ k}\Omega$ , $I_L = 30\text{ mA}$                               |     |     | 30  | $\mu\text{s}$ |
| $t_{SNSION2}$                     | Settling time from rising edge of EN and<br>DIA_EN<br>50% of $V_{DIA\_EN}$ $V_{EN}$ to 90% of settled ISNS      | $V_{EN} = V_{DIA\_EN} = 0\text{ V to }5\text{ V}$<br>$V_{BB} = 13.5\text{ V}$ , $R_{SNS} = 1\text{ k}\Omega$ , $R_{LOAD} = 10\ \Omega$                |     |     | 150 | $\mu\text{s}$ |
| $t_{SNSION3}$                     | Settling time from rising edge of EN with<br>DIA_EN HI;<br>50% of $V_{DIA\_EN}$ $V_{EN}$ to 90% of settled ISNS | $V_{EN} = 0\text{ V to }5\text{ V}$ , $V_{DIA\_EN} = 5\text{ V}$ , $V_{BB} = 13.5\text{ V}$<br>$R_{SNS} = 1\text{ k}\Omega$ , $R_{LOAD} = 10\ \Omega$ |     |     | 150 | $\mu\text{s}$ |
| $t_{SNSIOFF}$                     | Settling time from falling edge of DIA_EN   | $V_{EN} = 5\text{ V}$ , $V_{DIA\_EN} = 5\text{ V to }0\text{ V}$ , $V_{BB} = 13.5\text{ V}$<br>$R_{SNS} = 1\text{ k}\Omega$ , $R_L = 10\ \Omega$      |     |     | 20  | $\mu\text{s}$ |
| $t_{SETTLEH}$                     | Settling time from rising edge of load step   | $V_{EN} = 5\text{ V}$ , $V_{DIA\_EN} = 5\text{ V}$<br>$R_{SNS} = 1\text{ k}\Omega$ , $I_{OUT} = 0.5\text{ A to }3\text{ A}$                           |     |     | 20  | $\mu\text{s}$ |
| $t_{SETTLEL}$                     | Settling time from falling edge of load step  | $V_{EN} = 5\text{ V}$ , $V_{DIA\_EN} = 5\text{ V}$<br>$R_{SNS} = 1\text{ k}\Omega$ , $I_{OUT} = 3\text{ A to }0.5\text{ A}$                           |     |     | 20  | $\mu\text{s}$ |

## 6.7 Switching Characteristics

$V_{BB} = 13.5\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$  (unless otherwise noted)

| PARAMETER |   | TEST CONDITIONS  | MIN | TYP | MAX | UNIT                   |
|-----------|---|--|-----|-----|-----|------------------------|
| $t_{DR}$  | Channel Turn-on delay time (from Standby) | $V_{BB} = 13.5\text{ V}$ , $R_L = 10\ \Omega$ 50% of EN to 10% of VOUT     | 10  | 40  | 55  | $\mu\text{s}$          |
| $t_{DR}$  | Channel Turn-on delay time (from Active)  | $V_{BB} = 13.5\text{ V}$ , $R_L = 10\ \Omega$ 50% of EN to 10% of VOUT     | 10  | 35  | 45  | $\mu\text{s}$          |
| $t_{DF}$  | Channel Turn-off delay time               | $V_{BB} = 13.5\text{ V}$ , $R_L = 10\ \Omega$ 50% of EN to 90% of VOUT     | 10  | 30  | 45  | $\mu\text{s}$          |
| $SR_R$    | VOUT rising slew rate                     | $V_{BB} = 13.5\text{ V}$ , 20% to 80% of $V_{OUT}$ ,<br>$R_L = 10\ \Omega$ | 0.1 | 0.3 | 0.6 | $\text{V}/\mu\text{s}$ |
| $SR_F$    | VOUT falling slew rate                    | $V_{BB} = 13.5\text{ V}$ , 80% to 20% of $V_{OUT}$ ,<br>$R_L = 10\ \Omega$ | 0.1 | 0.3 | 0.6 | $\text{V}/\mu\text{s}$ |
| $f_{max}$ | Maximum PWM frequency                     |  |     | 0.4 | 2   | $\text{kHz}$           |
| $t_{ON}$  | Channel Turn-on time                      | $V_{BB} = 13.5\text{ V}$ , $R_L = 10\ \Omega$ 50% of EN to 80% of VOUT     | 30  | 70  | 145 | $\mu\text{s}$          |
| $t_{OFF}$ | Channel Turn-off time                     | $V_{BB} = 13.5\text{ V}$ , $R_L = 10\ \Omega$ 50% of EN to 20% of VOUT     | 30  | 70  | 145 | $\mu\text{s}$          |



## 6.7 Switching Characteristics (continued)

$V_{BB} = 13.5\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  (unless otherwise noted)

| PARAMETER          |   | TEST CONDITIONS  | MIN  | TYP | MAX | UNIT          |
|--------------------|---|--|------|-----|-----|---------------|
| $t_{ON} - t_{OFF}$ | Turn-on and off matching                | 1-ms enable pulse $V_{BB} = 13.5\text{ V}$ , $R_L = 10\ \Omega$                              | - 40 |     | 40  | $\mu\text{s}$ |
|                    |   | 200- $\mu\text{s}$ enable pulse, $V_{BB} = 13.5\text{ V}$ , $R_L = 10\ \Omega$               | - 40 |     | 40  | $\mu\text{s}$ |
| $\Delta_{PWM}$     | PWM accuracy - average load current     | 200- $\mu\text{s}$ enable pulse (1-ms period), $V_{BB} = 13.5\text{ V}$ , $R_L = 10\ \Omega$ | - 25 |     | 25  | %             |
|                    |   | $\leq 500\text{ Hz}$ , 50% Duty cycle $V_{BB} = 13.5\text{ V}$ , $R_L = 10\ \Omega$          | - 12 |     | 12  | %             |
| $E_{ON}$           | Switching energy losses during turn-on  | $V_{BB} = 13.5\text{ V}$ , $R_L = 10\ \Omega$  |      | 0.5 |     | mJ            |
| $E_{OFF}$          | Switching energy losses during turn-off | $V_{BB} = 13.5\text{ V}$ , $R_L = 10\ \Omega$  |      | 0.5 |     | mJ            |

## 6.8 Typical Characteristics

All the following data are based on the mean value of the three lots samples,  $V_{VBB} = 13.5\text{ V}$  if not specified.

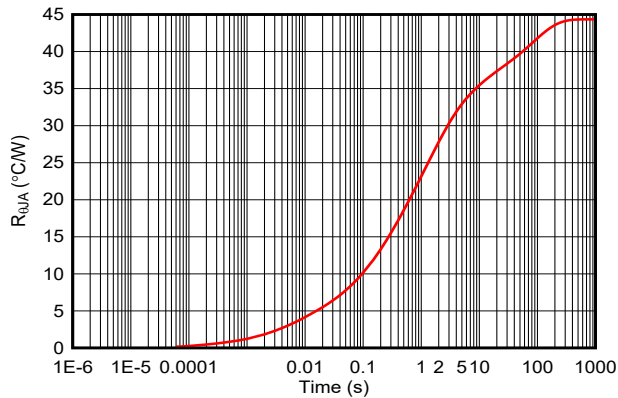


图 6-1. Transient Thermal Impedance

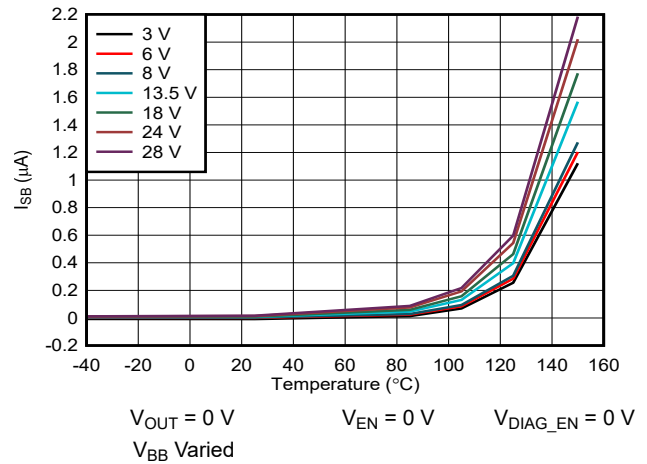


图 6-2. Standby Current  $I_{SB}$  vs Temperature

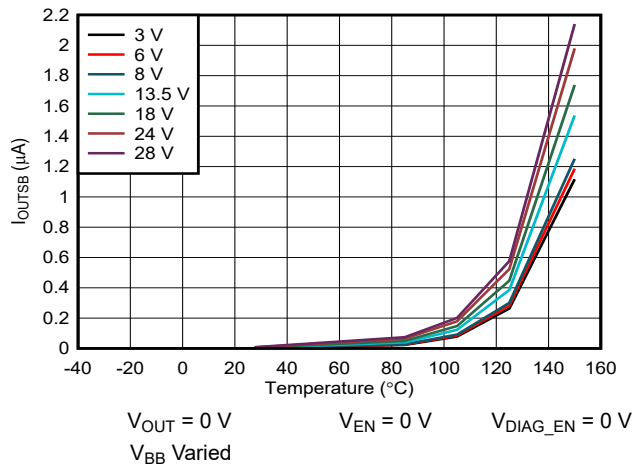


图 6-3. Output Leakage Current  $I_{OUT,STBY}$  vs Temperature

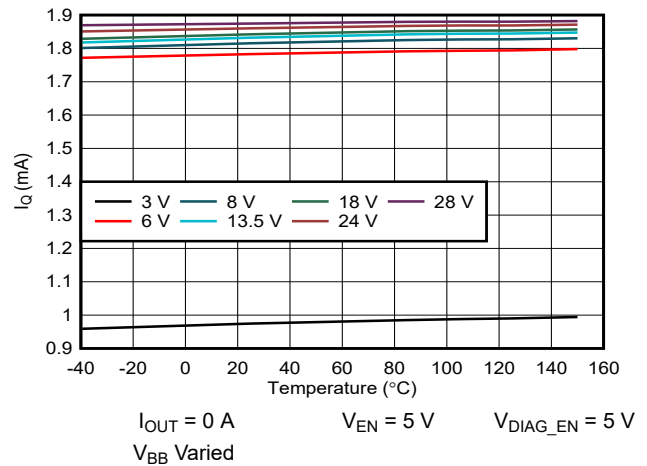


图 6-4. Quiescent Current  $I_Q$  vs Temperature

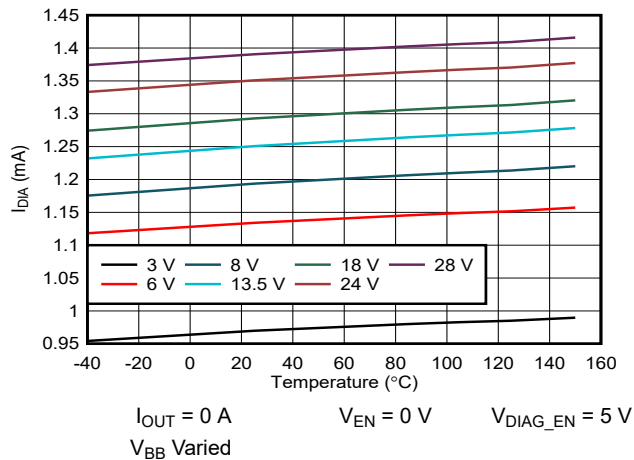


图 6-5. Diagnostic Current  $I_{DIA}$  vs Temperature

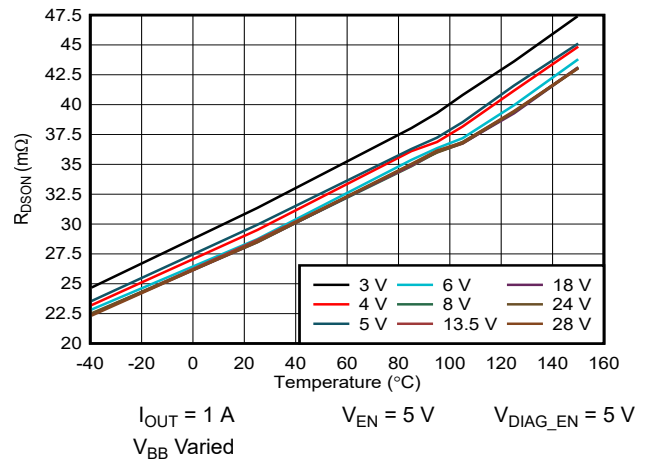


图 6-6.  $R_{DS(on)}$  vs Temperature

## 6.8 Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples,  $V_{VBB} = 13.5$  V if not specified.

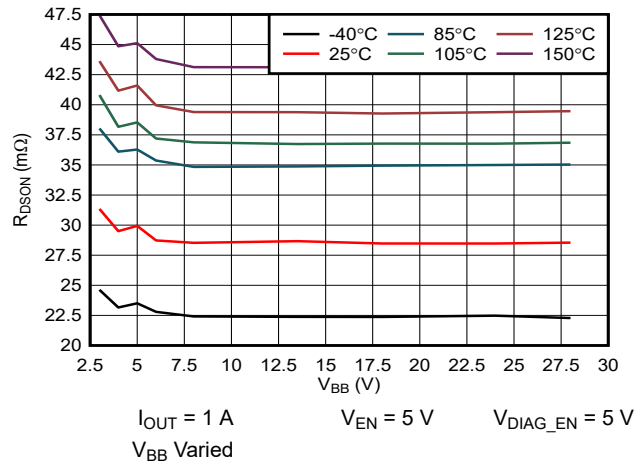


图 6-7.  $R_{DSON}$  vs  $V_{BB}$

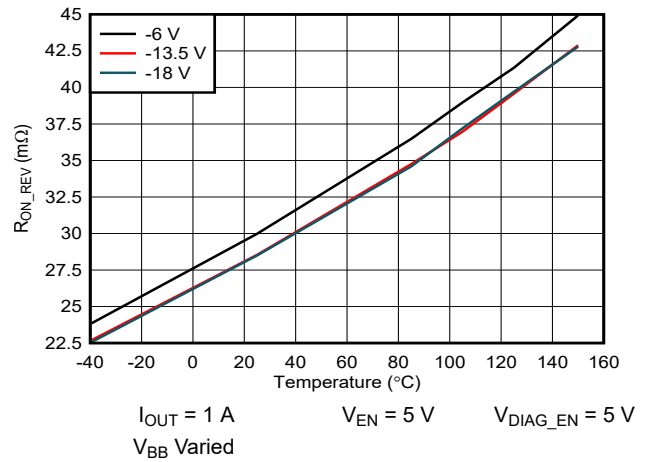


图 6-8.  $R_{ONREV}$  vs Temperature

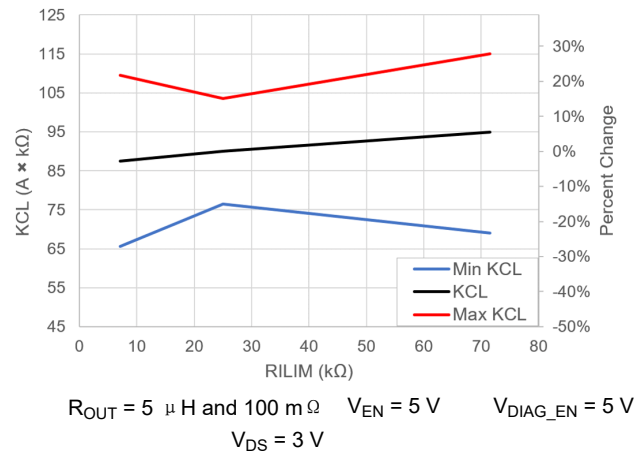


图 6-9. KCL vs RILIM

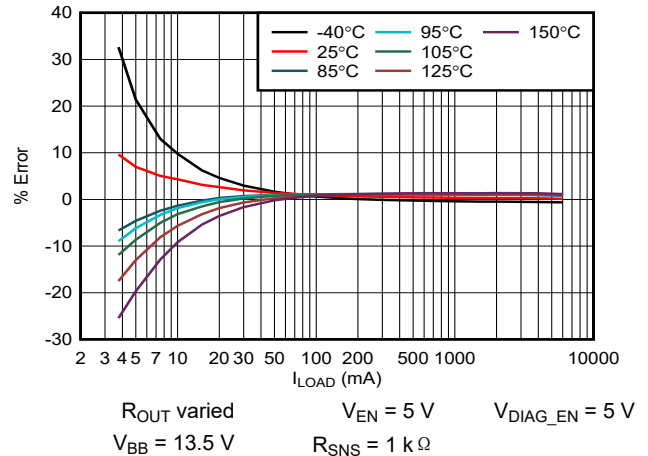


图 6-10. KSNS Error vs Load Current

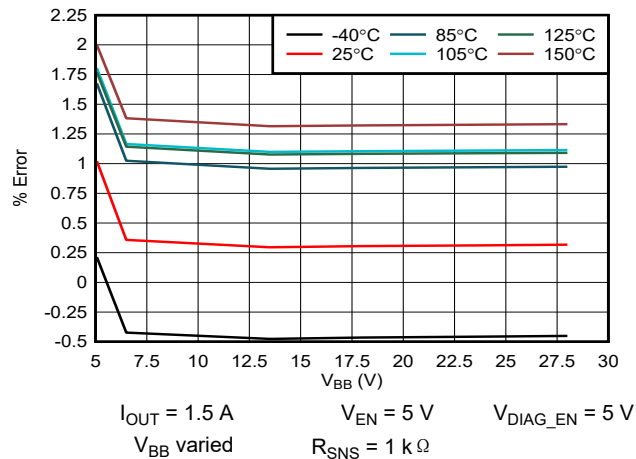


图 6-11. KSNS Error vs  $V_{BB}$

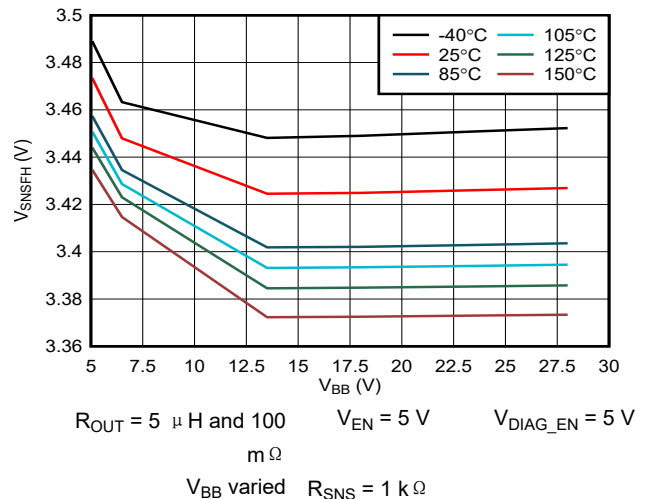


图 6-12.  $V_{SNSFH}$  (3.3 V) vs  $V_{BB}$

## 6.8 Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples,  $V_{VBB} = 13.5 \text{ V}$  if not specified.

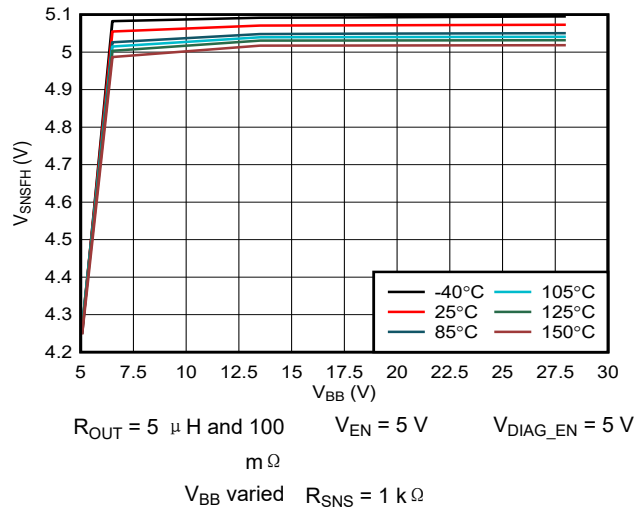


图 6-13. VSNFSH (5 V) vs VBB

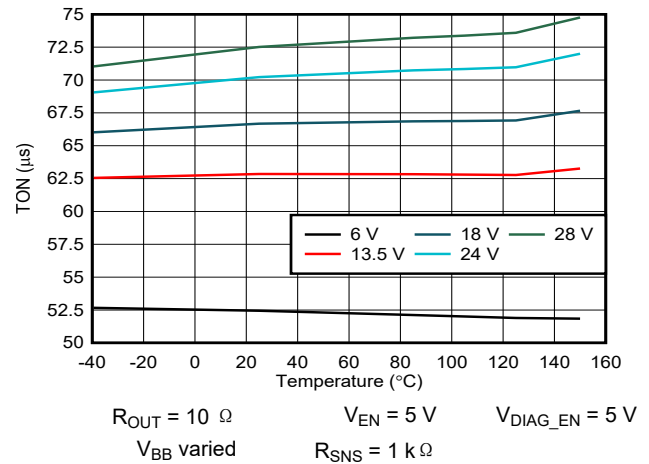


图 6-14. Turn-On Time  $T_{ON}$  vs Temperature

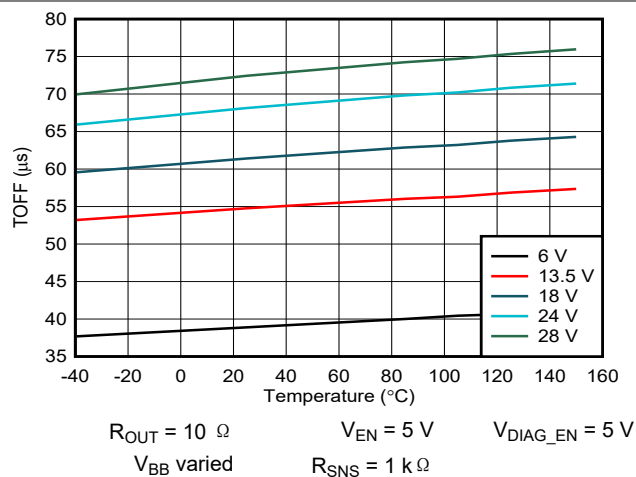


图 6-15. Turn-Off Time  $T_{OFF}$  vs Temperature

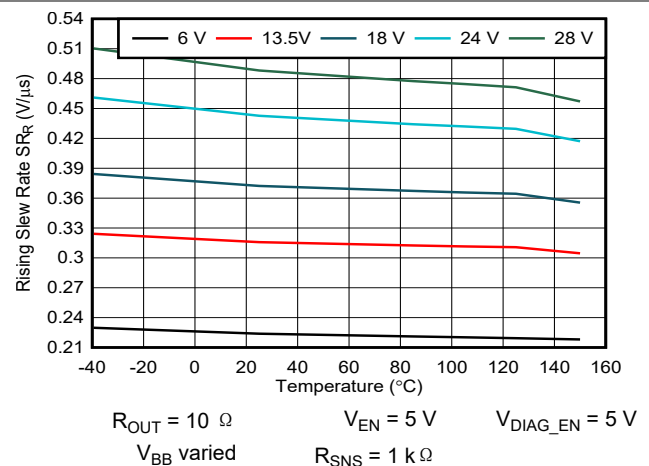


图 6-16. Rising Slew Rate SRR vs Temperature

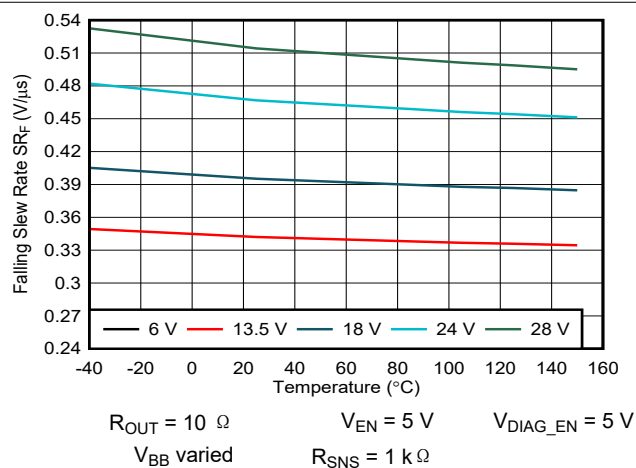


图 6-17. Falling Slew Rate SRF vs Temperature

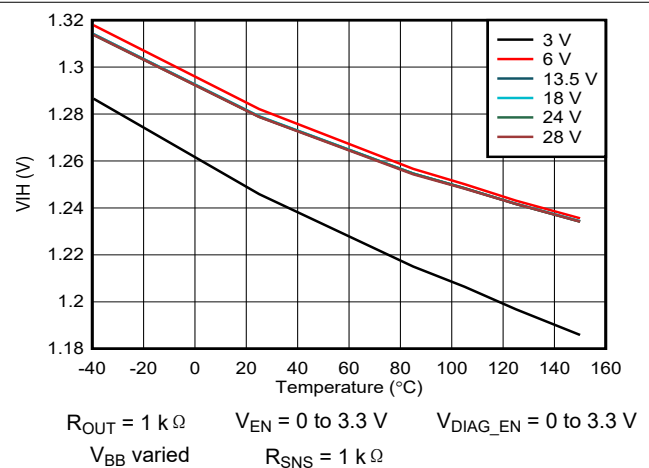


图 6-18.  $V_{IH}$  vs Temperature

## 6.8 Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples,  $V_{VBB} = 13.5\text{ V}$  if not specified.

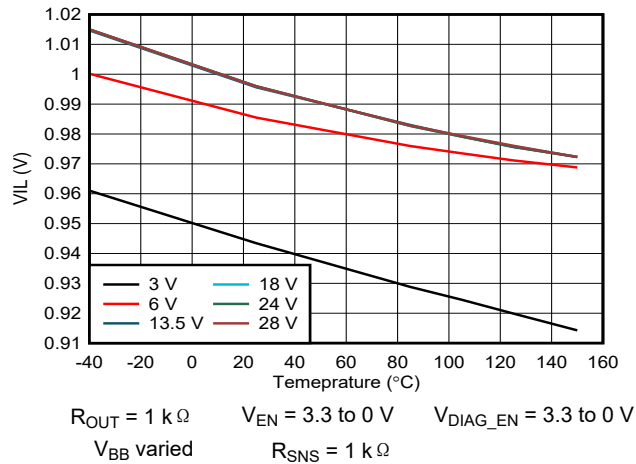


图 6-19.  $V_{IL}$  vs Temperature

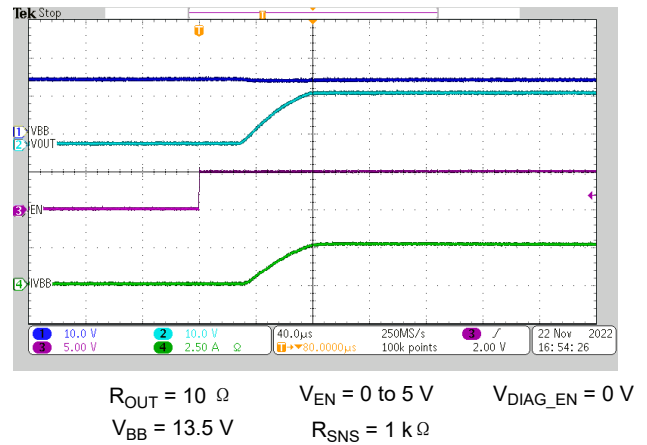


图 6-20. Turn-On Time ( $t_{ON}$ )

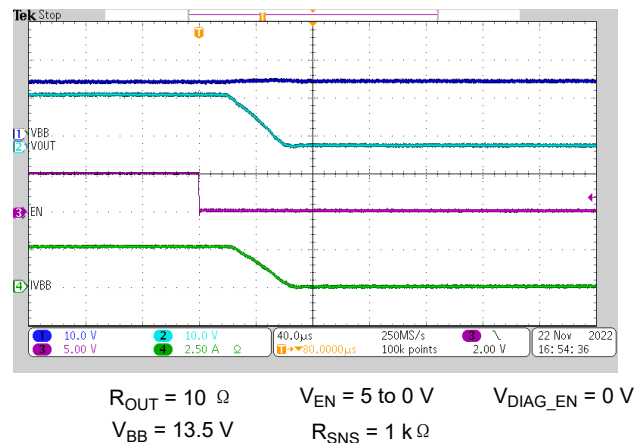


图 6-21. Turn-Off Time ( $t_{OFF}$ )

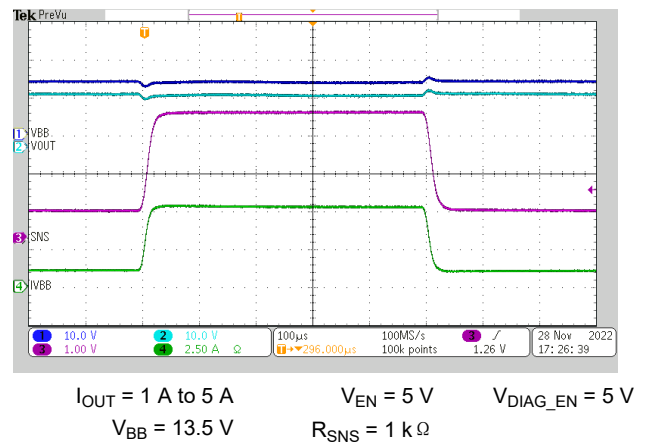


图 6-22. ISNS Settling Time ( $t_{SNSION}$ ) on Load Step

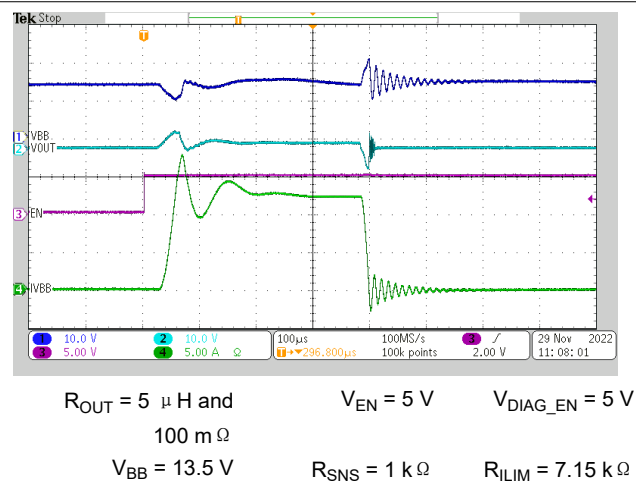


图 6-23. Short Circuit With ILIM Shorted to Ground

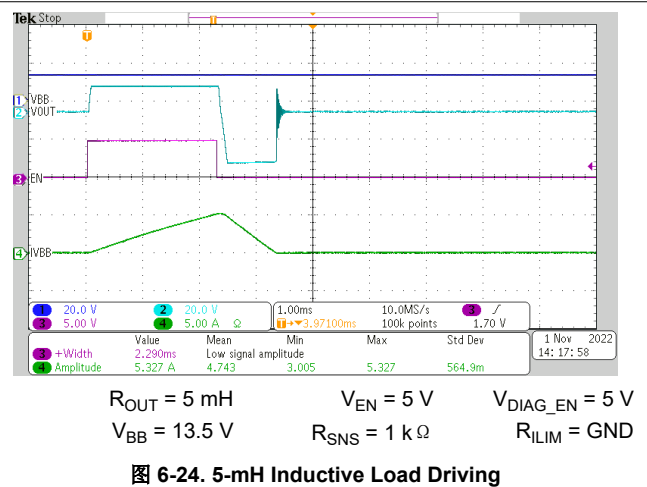
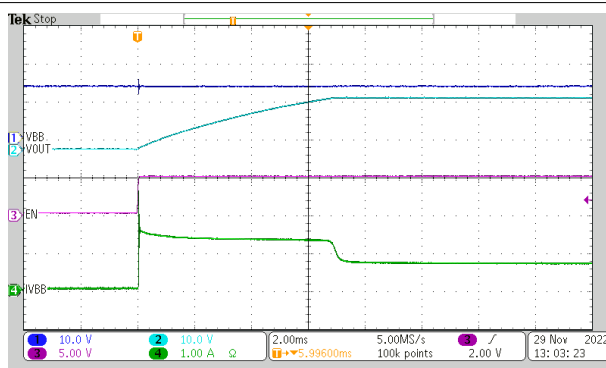


图 6-24. 5-mH Inductive Load Driving

## 6.8 Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples,  $V_{VBB} = 13.5\text{ V}$  if not specified.



$R_{OUT} = 470\ \mu\text{F}$  and  $20\ \Omega$

$V_{BB} = 13.5\text{ V}$

$V_{EN} = 5\text{ V}$

$R_{SNS} = 1\text{ k}\Omega$

$V_{DIAG\_EN} = 5\text{ V}$

$R_{ILIM} = 71.5\text{ k}\Omega$

图 6-25. 470-  $\mu\text{F}$  Capacitive Load Driving

## 7 Parameter Measurement Information

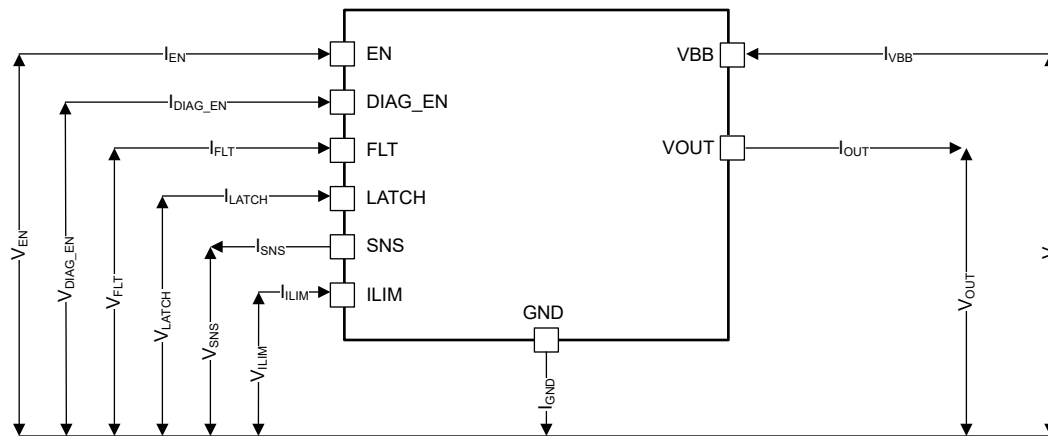


图 7-1. Parameter Definitions

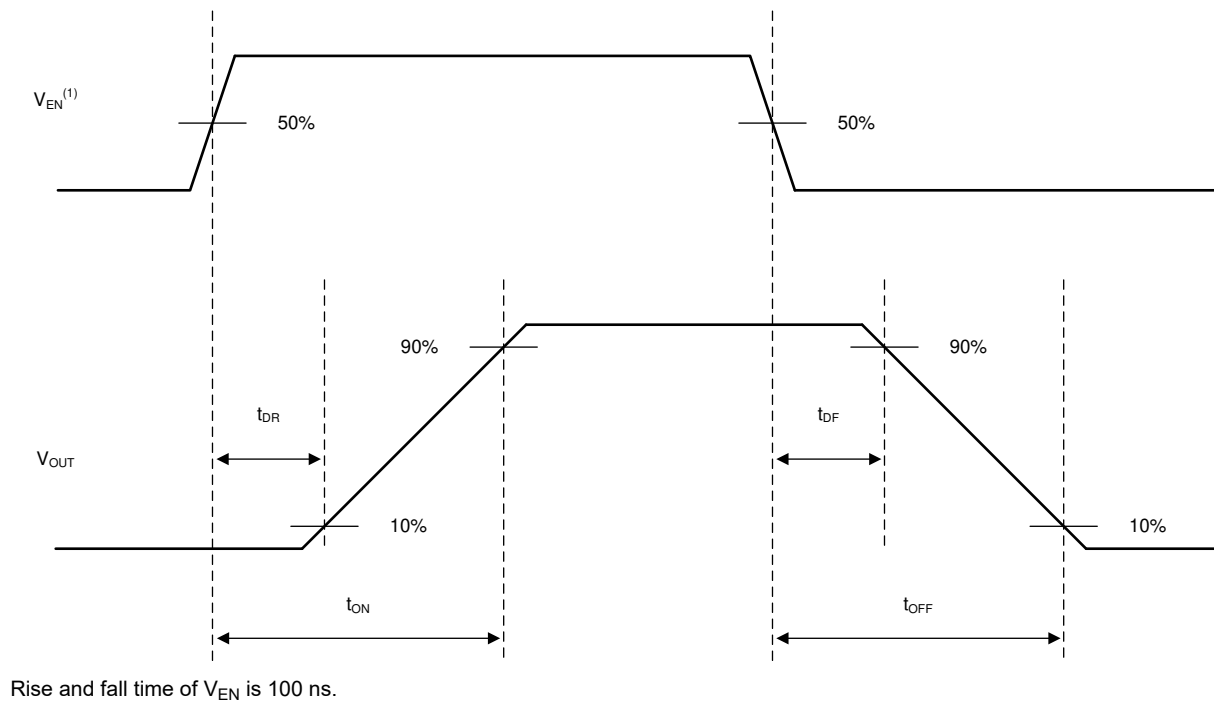
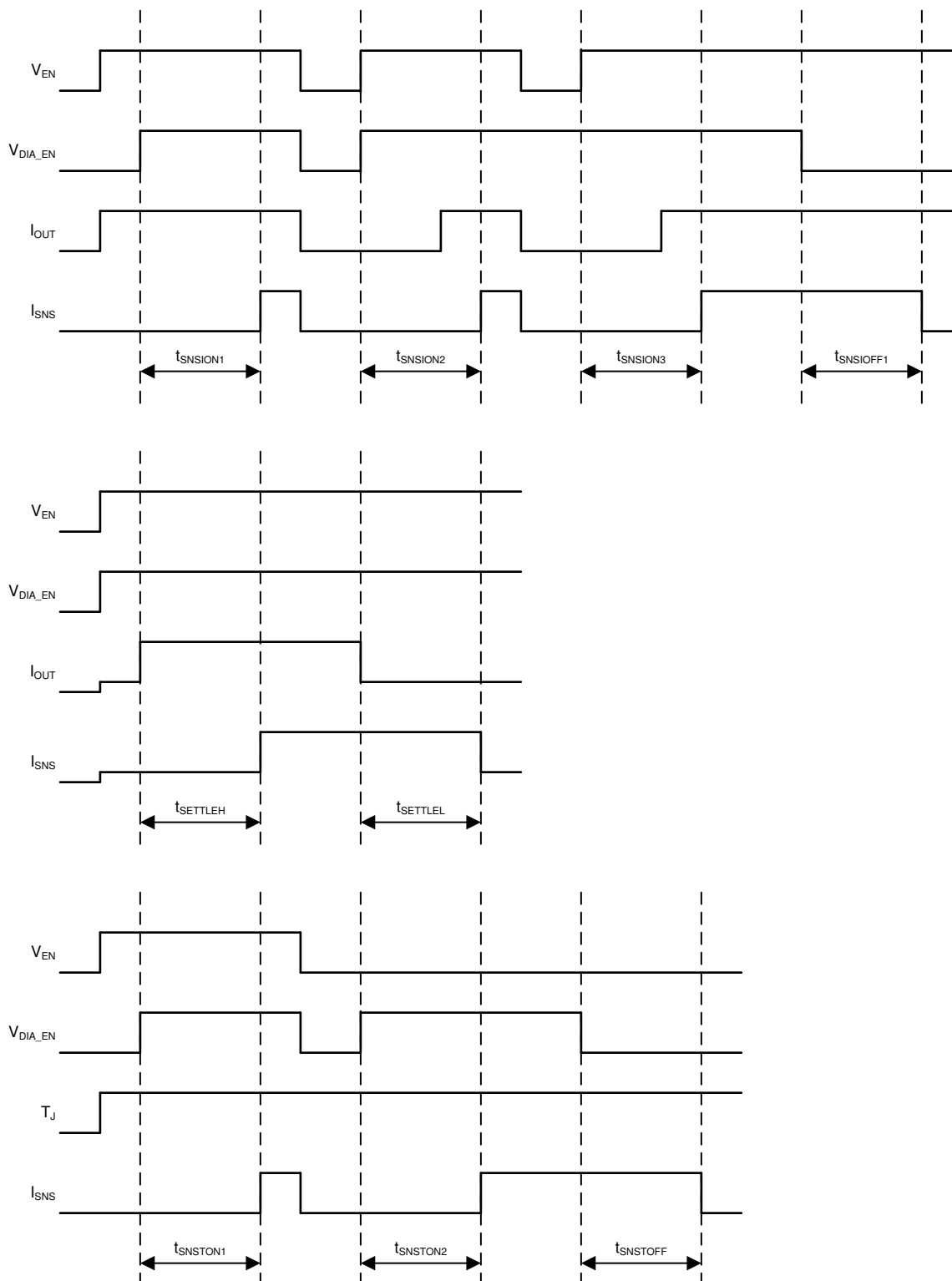


图 7-2. Switching Characteristics Definitions



Rise and fall times of control signals are 100 ns. Control signals include: EN, DIA\_EN.

**图 7-3. SNS Timing Characteristics Definitions**



## 8 Detailed Description

### 8.1 Overview

The TPS1HC30-Q1 is a single-channel, fully-protected, high side power switch with an integrated NMOS power FET and charge pump. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. Low logic high threshold,  $V_{IH}$ , of 1.5 V on the input pins allow use of MCUs down to 1.8 V. A programmable current-limit function greatly improves the reliability of the whole system. The device diagnostic reporting has two pins to support both digital status and analog current-sense output, both of which can be set to the high-impedance state when diagnostics are disabled, for multiplexing the MCU analog or digital interface among devices.

The digital status report is implemented with an open-drain structure on the fault pin. When a fault condition occurs, the pin is pulled down to GND. An external pullup is required to match the microcontroller supply level. High-accuracy current sensing allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source  $1 / K_{SNS}$  of the load current, which is reflected as voltage on the SNS pin.  $K_{SNS}$  is a constant value across the temperature and supply voltage. The current-sensing function operates normally within a wide linear region from 0 V to 4 V. The SNS pin can also report a fault by forcing a voltage of  $V_{SNSFH}$  that scales with the diagnostic enable voltage so that the maximum voltage seen by the system ADC is within an acceptable value. This action removes the need for an external Zener diode or resistor divider on the SNS pin.

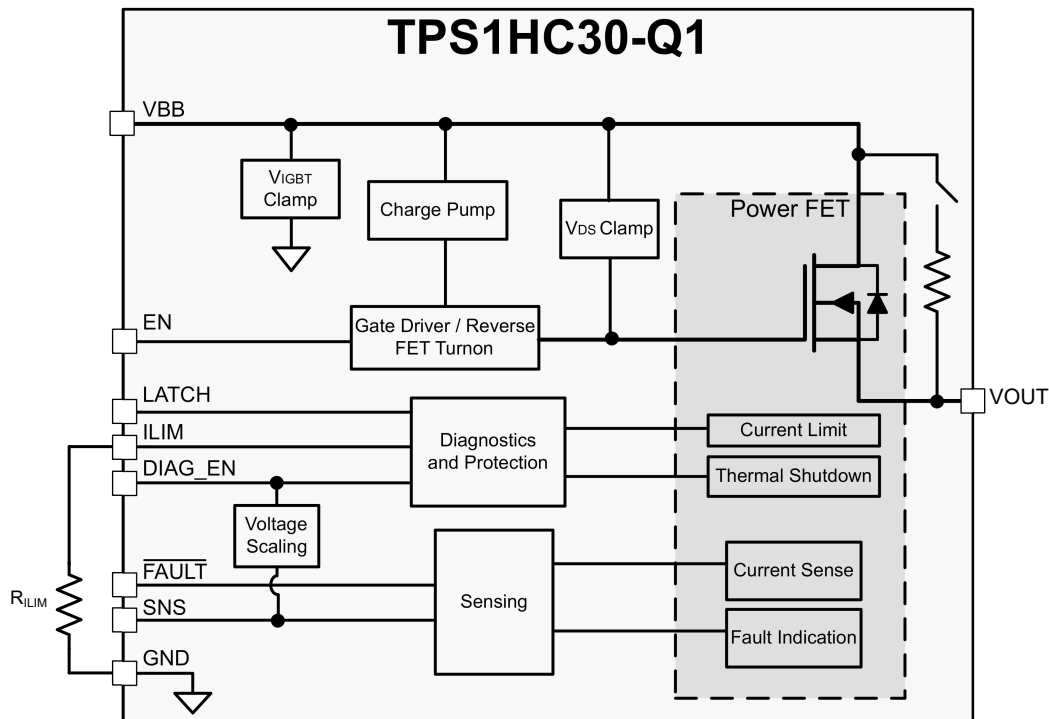
The external high-accuracy current limit allows setting the current limit value by application. The current limit highly improves the reliability of the system by clamping the inrush current effectively under start-up or short-circuit conditions. Also, the current limit can save system costs by reducing PCB trace, connector size, and the preceding power-stage capacity. An internal current limit is also implemented in this device. The lower value of the external or internal current-limit value is applied.

An active drain and source voltage clamp is built in to address switching off the energy of inductive loads, such as relays, solenoids, pumps, motors, and so forth. During the inductive switching-off cycle, both the energy of the power supply ( $E_{BAT}$ ) and the load ( $E_{LOAD}$ ) are dissipated on the high side power switch itself. With the benefits of process technology and excellent IC layout, the TPS1HC30-Q1 device can achieve excellent power dissipation capacity, which can help save the external free-wheeling circuitry in most cases. For more details, see [Inductive-Load Switching-Off Clamp](#).

Short-circuit reliability is critical for smart high side power-switch devices. The standard of AEC-Q100-012 is to determine the reliability of the devices when operating in a continuous short-circuit condition. Different grade levels are specified according to the pass cycles. This device is qualified with the highest level, Grade A, 1 million times short-to-GND certification.

The TPS1HC30-Q1 device can be used as a high side power switch for a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, and heaters.

## 8.2 Functional Block Diagram

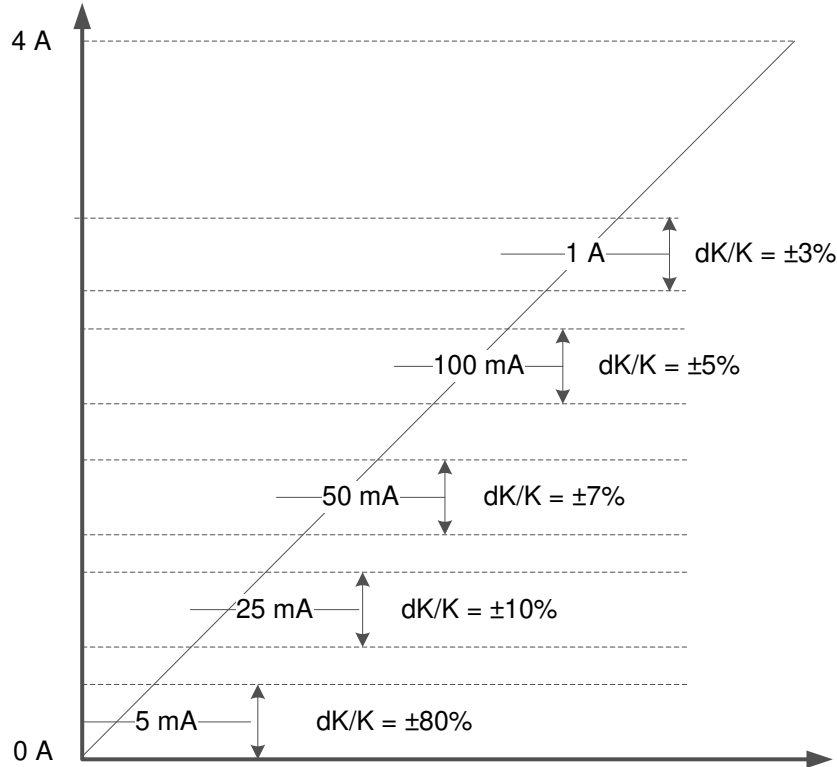


### 8.3 Feature Description

### 8.3.1 Accurate Current Sense

The high-accuracy current-sense function is internally implemented, which allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source  $1 / K_{SNS}$  of the load current, flowing out to the external resistor between the SNS pin and GND, and reflected as voltage on the SNS pin.

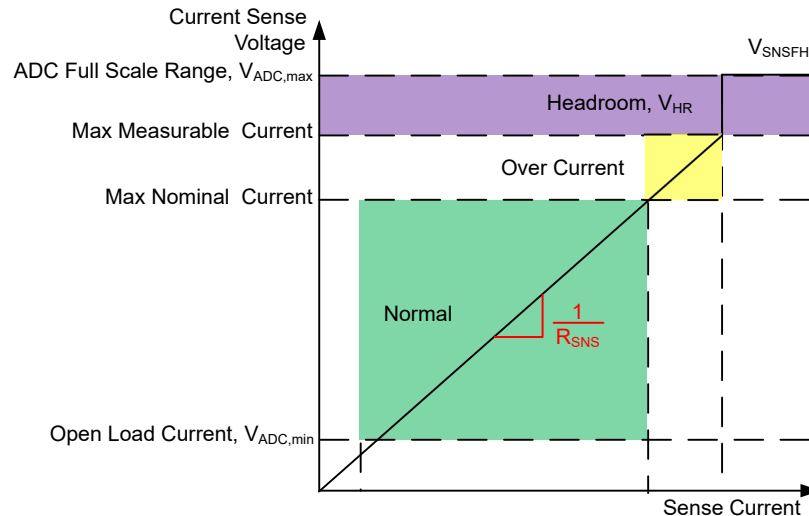
$K_{SNS}$  is the ratio of the output current and the sense current. The accuracy values of  $K_{SNS}$  quoted in the electrical characteristics do take into consideration temperature and supply voltage. Each device was internally calibrated while in production, so post-calibration by users is not required in most cases.



**图 8-1. Current-Sense Accuracy**

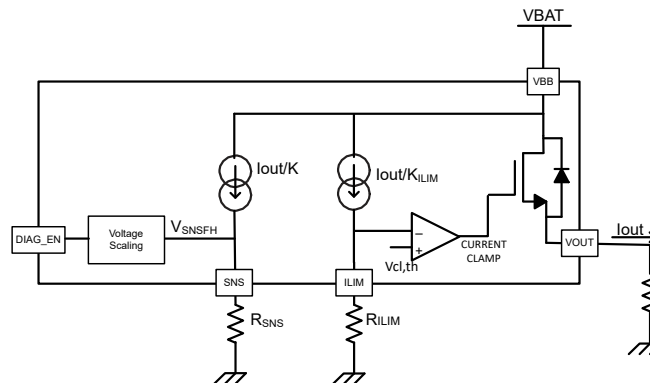
The maximum voltage out on the SNS pin is clamped to  $V_{SNSFH}$ , which is the fault voltage level. To make sure that this voltage is not higher than the system can tolerate, TI has correlated the voltage coming in on the DIAG\_EN pin with the maximum voltage out on the SNS pin. If DIAG\_EN is between  $V_{IH}$  and 3.3 V, the maximum output on the SNS pin is approximately 3.3 V. However, if the voltage at DIAG\_EN is above 3.3 V, then the fault SNS voltage,  $V_{SNSFH}$ , tracks that voltage up to 5 V. Tracking is done because the GPIO voltage output that is powering the diagnostics through DIAG\_EN is close to the maximum acceptable ADC voltage within the same microcontroller. Therefore, the sense resistor value,  $R_{SNS}$ , can be chosen to maximize the range of currents needed to be measured by the system. The  $R_{SNS}$  value must be chosen based on application need. The maximum usable  $R_{SNS}$  value is bounded by the ADC minimum acceptable voltage,  $V_{ADC,min}$ , for the smallest load current needed to be measured by the system,  $I_{LOAD,min}$ . The minimum acceptable  $R_{SNS}$  value has to ensure the  $V_{SNS}$  voltage is below the  $V_{SNSFH}$  value so that the system can determine faults. This difference between the maximum readable current through the SNS pin,  $I_{LOAD,max} \times R_{SNS}$ , and the  $V_{SNSFH}$  is called the headroom voltage,  $V_{HR}$ . The headroom voltage is determined by the system but is important so that there is a difference between the maximum readable current and a fault condition. Therefore, the minimum  $R_{SNS}$  value has to be the  $V_{SNSFH}$  minus the  $V_{HR}$  times the sense current ratio,  $K_{SNS}$  divided by the maximum load current the system must measure,  $I_{LOAD,max}$ . Use the following equation to see the boundary equation.

$$(V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,max} \leq R_{SNS} \leq V_{ADC,min} \times K_{SNS} / I_{LOAD,min} \quad (1)$$



**图 8-2. Voltage Indication on the Current-Sense Pin**

The maximum current the system wants to read,  $I_{LOAD,max}$ , must be below the current-limit threshold because after the current-limit threshold is tripped the  $V_{SNS}$  value goes to  $V_{SNSFH}$ . Additionally, currents being measured must be below 6 A to ensure that the current sense output is not saturated.



### 图 8-3. Current-Sense and Current-Limit Block Diagram

Because this scheme adapts based on the voltage coming in from the MCU, there is no need to have a Zener diode on the SNS pin to protect from high voltages.

### 8.3.2 Programmable Current Limit

A high-accuracy current limit allows higher reliability, which protects the power supply during short circuit or power up. Also, a current limit can save system costs by reducing PCB traces, connector size, and the capacity of the preceding power stage.

Current limit offers protection from over-stressing to the load and integrated power FET. Current limit holds the current at the set value, and pulls up the SNS pin to  $V_{SNSFH}$  and asserts the  $\overline{FLT}$  pin as diagnostic reports. The three current-limit thresholds are:

- **External programmable current limit** – An external resistor,  $R_{ILIM}$ , is used to set the channel current limit. When the current through the device exceeds  $I_{CL}$  (current limit threshold), a closed loop steps in immediately.  $V_{GS}$  voltage regulates accordingly, leading to the  $V_{DS}$  voltage regulation. When the closed loop is set up, the current is clamped at the set value. The external programmable current limit provides the capability to set the current-limit value by application.

Additionally, this value can be dynamically changed by changing the resistance on the ILIM pin. This information can be seen in the [Applications](#) section.

- Internal current limit:  $I_{LIM}$  pin shorted to ground – If the external current limit is out of range on the lower end or the  $I_{LIM}$  pin is shorted to ground, the internal current limit is fixed and typically 12 A. To use the internal current limit for large-current applications, tie the  $I_{LIM}$  pin directly to the device GND.
- Internal current limit:  $I_{LIM}$  pin open – If the external resistor is out of range on the higher end or the  $I_{LIM}$  pin is open, the current limit reverts to 6 A or half the current limit range. This level is still above the nominal operation for the device to operate in DC STEADY state, but is low enough that if a pin fault occurs and the  $R_{ILIM}$  opens up, the current does not default to the highest rating and put additional stress on the power supply.

Both the internal current limit ( $I_{lim,nom}$ ) and external programmable current limit are always active when  $V_{BB}$  is powered and EN is high. The lower value one (of  $I_{LIM}$  and the external programmable current limit) is applied as the actual current limit. The typical deglitch time for the current limit to assert is 2.5  $\mu$ s.

Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the  $I_{LIM}$  pin must be connected with device GND. Use Equation 2 to calculate  $R_{ILIM}$ .

$$R_{ILIM} = K_{CL} / I_{LIM} \quad (2)$$

For better protection from a "hot short" condition (when  $V_{BB}$  is high, channel is on, and a short to GND happens suddenly), an overcurrent protection, OVCR, circuit is triggered that makes sure to limit the maximum current the device allows to go through. With this OVCR, the device is protected during "hot short" events.

For more information about the current limiting feature, see the [Short-Circuit and Overload Protection](#) section.

### Current Limit Accuracy Across $V_{DS}$

The TPS1HC30-Q1 has very tight accuracy of the current limit regulation level across the full range of currents and temperature. This accuracy is defined at several defined  $R_{ILIM}$  values, 7.15  $k\Omega$ , 25  $k\Omega$ , and 71.5  $k\Omega$  specified in the Electrical Characteristics at  $V_{DS} = 3$  V. However, as  $V_{DS}$  ( $V_{BB} - V_{OUT}$ ) increases, the current regulation value also slightly increases. Taking a typical device, at the 3 different current limits ranges specified, sweeping the  $V_{DS}$  voltage, and plotting the regulation value gives the graphs below.

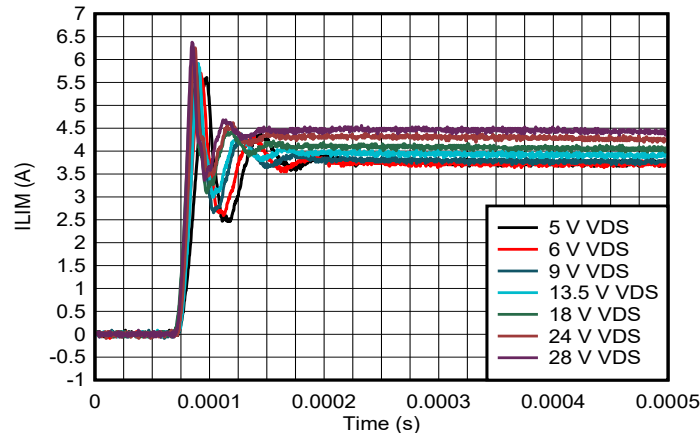


图 8-4. Current Limit Regulation With Varying VDS,  $R_{ILIM} = 25 k\Omega$

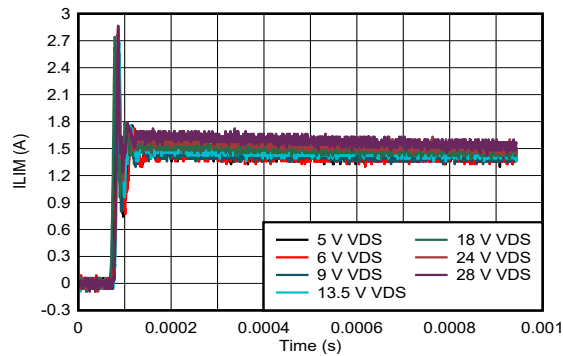


图 8-5. Current Limit Regulation With Varying VDS, RILIM = 71.5 kΩ

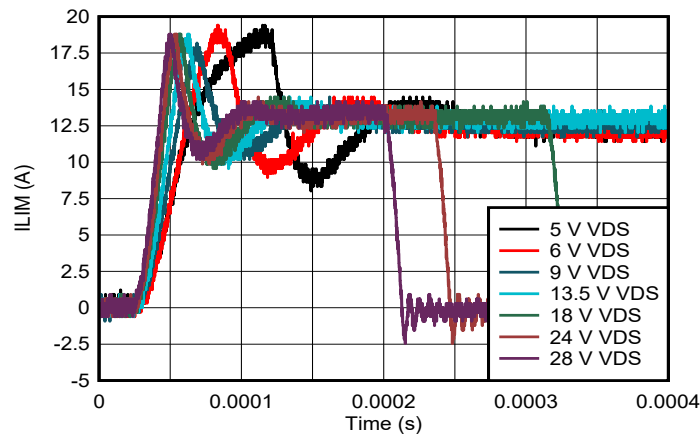


图 8-6. Current Limit Regulation With Varying VDS, RILIM = 7.15 kΩ

Using a point during the regulation time of each of the different RILIM settings, the graph can be normalized to the specification in the electrical characteristics of  $V_{DS} = 3\text{ V}$  which results in graph below.

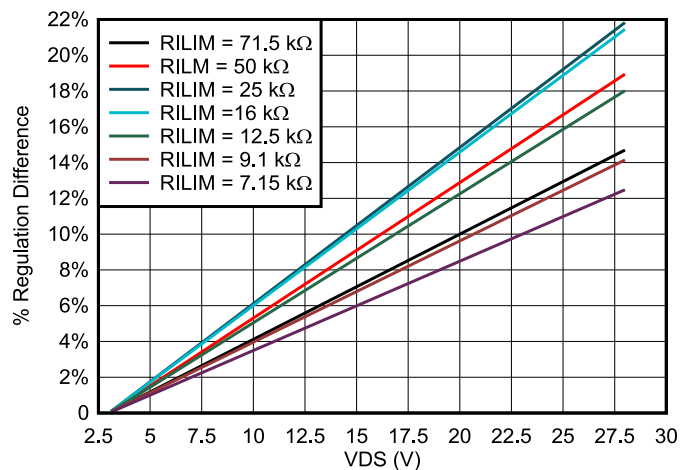


图 8-7. Current Limit Regulation Percentage Change With Varying  $V_{DS}$

Using this figure, the current limit regulation value can be estimated for any current limit value desired based on the  $V_{DS}$  value seen in the application. These graphs were taken on a typical device and should be used as reference when accounting for current limit tolerances. As an example see table below for regulation values based on setting the current limit close to the maximum load current. Note that RILIM tolerances are not factored into analysis below.

| Max Load Current for Application | RILIM           | KCL                        | Minimum Current Limit (at $V_{DS} = 3\text{ V}$ ) | Short Circuit Regulation value at $V_{BB} = V_{DS} = 18\text{ V}$ |
|----------------------------------|-----------------|----------------------------|---|---|
| 1.5 A                            | 47.5 k $\Omega$ | 92.4 A $\times$ k $\Omega$ | 1.53 A (1.94 A - 21%)                             | 2.5 A, +11%   |
| 3 A                              | 25 k $\Omega$   | 90 A $\times$ k $\Omega$   | 3.06 A (3.6 A - 15%)                              | 4.6A, +13%  |
| 6A                               | 11.3 k $\Omega$ | 88.2A $\times$ k $\Omega$  | 6.03 A (7.8 A - 23%)                              | 10.6 A, +11%  |

### 8.3.2.1 Capacitive Charging

The following figure shows the typical setup for a capacitive load application and the internal blocks that function when the device is used. Note that all capacitive loads have an associated "load" in parallel with the capacitor that is described as a resistive load but in reality it can be inductive or resistive.

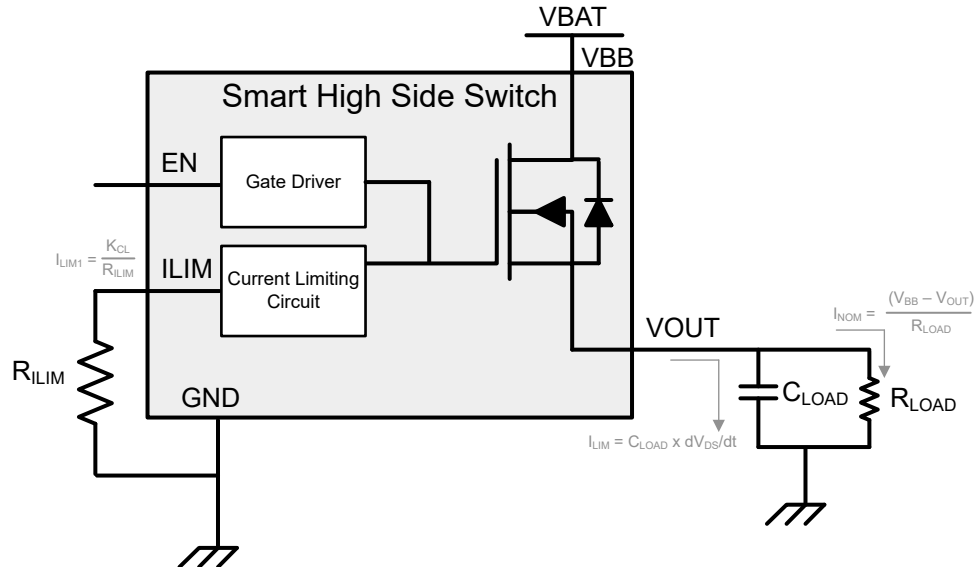


图 8-8. Capacitive Charging Circuit

The first thing to check is that the nominal DC current,  $I_{NOM}$ , is acceptable for the TPS1HC30-Q1 device. This check can easily be done by taking the  $R_{\theta JA}$  from the [Thermal Information](#) section and multiplying the  $R_{ON}$  of the TPS1HC30-Q1 and the  $I_{NOM}$  with it, add the ambient temperature and if that value is below the thermal shutdown value the device can operate with that load current. For an example of this calculation see the [Applications](#) section.

The second key care about for this application is to make sure that the capacitive load can be charged up completely without the device hitting thermal shutdown. The reason is because if the device hits thermal shutdown during the charging, the resistive nature of the load in parallel with the capacitor starts to discharge the capacitor over the duration the TPS1HC30-Q1 is off. Note that there are some application with high enough load impedance that the TPS1HC30-Q1 hitting thermal shutdown and trying again is acceptable; however, for the majority of applications, the system must be designed so that the TPS1HC30-Q1 does not hit thermal shutdown while charging the capacitor.

With the current clamping feature of the TPS1HC30-Q1, capacitors can be charged up at a lower inrush current than other high current limit switches. This lower inrush current means that the capacitor takes a little longer to charge all the way up. The time that it takes to charge up follows the equation below.

$$I_{LIM} = C \times d(V_{BB} - V_{DS}) / dt \quad (3)$$

However, because the  $V_{DS}$  for a typical 3.3-A application is much less than the  $V_{BB}$  voltage ( $V_{DS} \approx 3.3\text{ A} \times 0.03\ \Omega = 100\text{ mV}$ ,  $V_{BB} \approx 13.5\text{ V}$ ), the equation can be rewritten and approximated as

$$dt = C \times dV_{BB} / I_{LIM} \quad (4)$$

The following figure pictures charge timing.

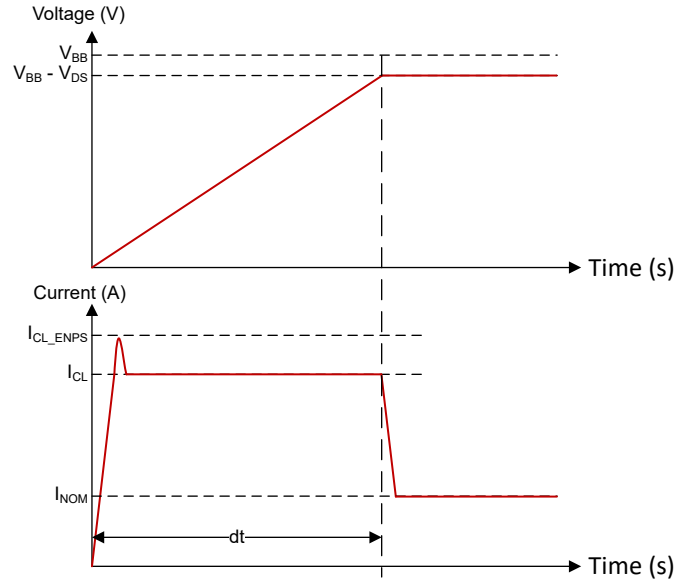


图 8-9. Capacitive Charging Timing

Using this  $dt$  calculated based on the current limit, and finding the transient thermal impedance value at half the  $dt$  value, the junction temperature rise can be approximated by the [方程式 5](#).

$$\Delta T_J \cong \frac{2}{3} \times V_{BB} \times I_{LIM} \times R_{\theta JA}(dt/2) \quad (5)$$

For more information about capacitive charging with high-side switches, see the [How to Drive Resistive, Inductive, Capacitive, and Lighting Loads application note](#). This application note has information about the thermal modeling available along with quick ways to estimate if a high-side switch can charge a capacitor to a given voltage.

### 8.3.3 Inductive-Load Switching-Off Clamp

When an inductive load is switching off, the output voltage is pulled down to negative, due to the inductance characteristics. The power FET can break down if the voltage is not clamped during the current-decay period. To protect the power FET in this situation, internally clamp the drain-to-source voltage, namely  $V_{DS,clamp}$ , the clamp diode between the drain and gate.

$$V_{DS,clamp} = V_{BAT} - V_{OUT} \quad (6)$$

During the current-decay period ( $T_{DECAY}$ ), the power FET is turned on for inductance-energy dissipation. Both the energy of the power supply ( $E_{BAT}$ ) and the load ( $E_{LOAD}$ ) are dissipated on the high side power switch itself, which is called  $E_{HSD}$ . If resistance is in series with inductance, some of the load energy is dissipated in the resistance.

$$E_{HSD} = E_{BAT} + E_{LOAD} = E_{BAT} + E_L - E_R \quad (7)$$

From the high side power switch view,  $E_{HSD}$  equals the integration value during the current-decay period.

$$E_{HSD} = \int_0^{T_{DECAY}} V_{DS,clamp} \times I_{OUT}(t) dt \quad (8)$$

$$T_{DECAY} = \frac{L}{R} \times \ln \left( \frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|} \right) \quad (9)$$



$$E_{HSD} = L \times \frac{V_{BAT} + |V_{OUT}|}{R^2} \times \left[ R \times I_{OUT(MAX)} - |V_{OUT}| \ln \left( \frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|} \right) \right] \quad (10)$$

When R approximately equals 0,  $E_{HSD}$  can be given simply as:

$$E_{HSD} = \frac{1}{2} \times L \times I_{OUT(MAX)}^2 \times \frac{V_{BAT} + |V_{OUT}|}{R^2} \quad (11)$$

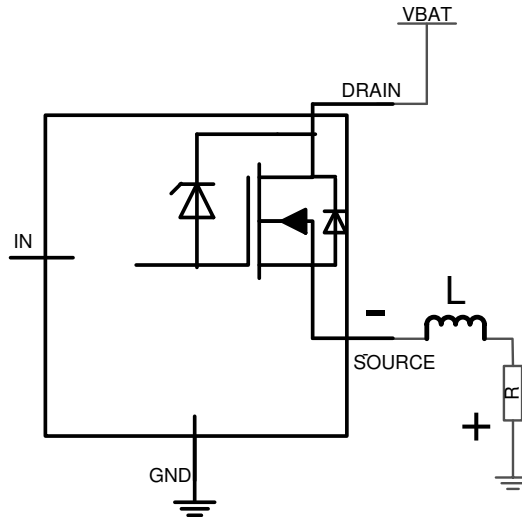


图 8-10. Driving Inductive Load

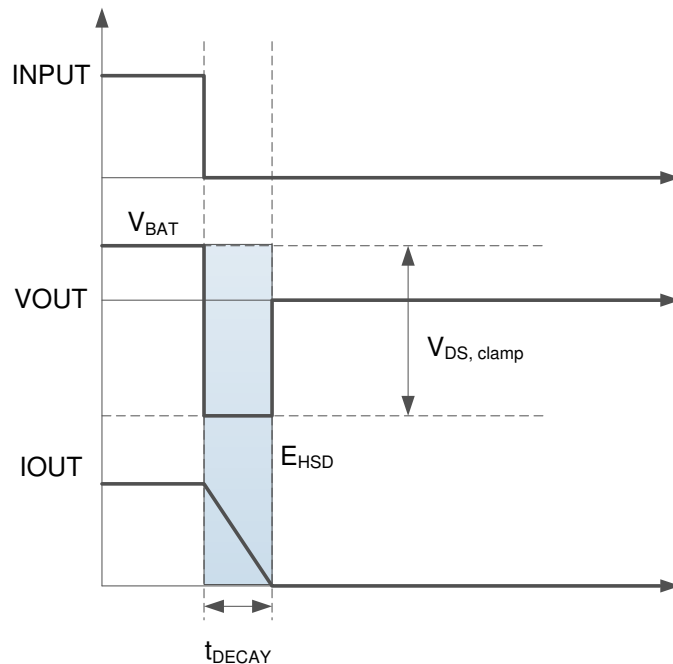


图 8-11. Inductive-Load Switching-Off Diagram

As discussed previously, when switching off, battery energy and load energy are dissipated on the high side power switch, which leads to the large thermal variation. For each high side power switch, the upper limit of the maximum safe power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition. TI provides the upper limit of single-pulse energy that devices can tolerate under the test

condition:  $V_{VS} = 13.5\text{ V}$ , inductance from 0.1 mH to 400 mH,  $R = 0\ \Omega$ , FR4 2s2p board, 2-  $\times$  70-  $\mu\text{m}$  copper, 2-  $\times$  35-  $\mu\text{m}$  copper, thermal pad copper area 600  $\text{mm}^2$ .

### 8.3.4 Full Protections and Diagnostics

表 8-1 is when DIAG\_EN is enabled. When DIAG\_EN is low, current sense and FLT are disabled. The output is in high-impedance mode. For details, refer to the following table.

表 8-1. Diagnostic Enable Logic Table

| DIAG_EN | IN Condition | Protections and Diagnostics   |
|---------|--------------|---|
| HIGH    | ON           | See <a href="#">Fault Table</a>   |
|         | OFF          |   |
| LOW     | ON           | Diagnostics disabled, protection normal<br>SNS and FLT are high impedance |
|         | OFF          |   |

表 8-2. Fault Table

| Conditions  | EN | VOUT  | Latch | FLT  | SNS   | Behavior  | Recovery  |
|---|----|---|-------|------|---|---|---|
| Normal  | L  | L   | x     | Hi-Z | 0   | Normal  |   |
|   | H  | $I_{\text{LOAD}} \times R_{\text{ON}}$                  | x     | Hi-Z | $I_{\text{Load}} / K_{\text{SNS}}$          | Normal  |   |
| Overcurrent   | H  | $V_{\text{BB}} - I_{\text{LIM}} \times R_{\text{LOAD}}$ | x     | L    | $V_{\text{SNSFH}}$                          | Holds the current at the current limit until thermal shutdown or when the overcurrent event is removed      |   |
| STG, Relative Thermal Shutdown, Absolute Thermal Shutdown | H  | H/L   | L     | L    | $V_{\text{SNSFH}}$                          | Shuts down when devices hits relative or absolute thermal shutdown  | Auto retries when $T_{\text{HYS}}$ is met and it has been longer than $t_{\text{RETRY}}$ amount of time |
|   | H  | H/L   | H     | L    | $V_{\text{SNSFH}}$                          | Shuts down when devices hits relative or absolute thermal shutdown  | Stays off until latch or enable is toggled  |
| Open load, STB  | H  | H   | x     | Hi-Z | $I_{\text{Load}} / K_{\text{SNS}} = \sim 0$ | Normal behavior, user can judge through the SNS pin output if it is an open load or not                     |   |
|   | L  | H   | x     | L    | $V_{\text{SNSFH}}$                          | Internal pullup resistor is active. If $V_{\text{BB}} - V_{\text{OUT}} < V_{\text{OL}}$ then fault active.  | Clears when fault goes away   |
| Reverse Polarity  | x  | x   | x     | x    | x   | Channel turns on to lower power dissipation. Current into ground pin is limited by external ground network. |   |

表 8-3. Deglitch Time for Each Fault Condition

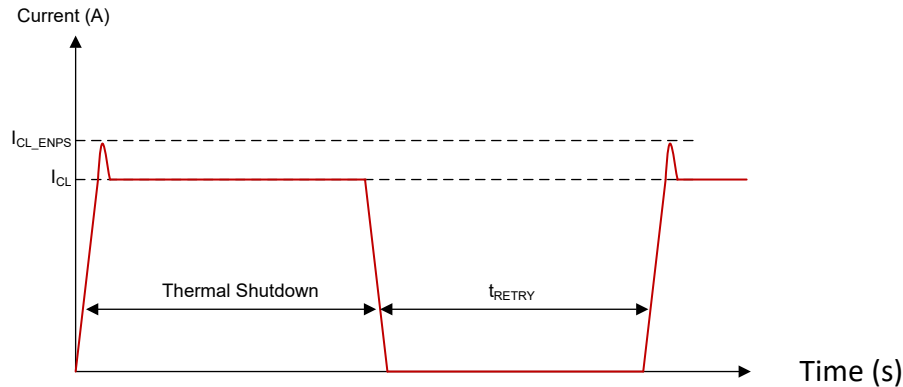
| Fault Condition  | Deglitch Time     |
|------------------|-------------------|
| ILIM             | 2.5 $\mu\text{s}$ |
| $T_{\text{REL}}$ | 2.5 $\mu\text{s}$ |
| $T_{\text{ABS}}$ | 20 $\mu\text{s}$  |
| Open Load        | 500 $\mu\text{s}$ |

#### 8.3.4.1 Short-Circuit and Overload Protection

TPS1HC30-Q1 provides output short-circuit protection to ensure that the device prevents current flow in the event of a low impedance path to GND, removing the risk of damage or significant supply droop. The device is

assured to protect against short-circuit events regardless of the state of the ILIM pins and with up to 28-V supply at 125°C.

The following figure shows the behavior of the TPS1HC30-Q1 when the device is enabled into a short circuit.

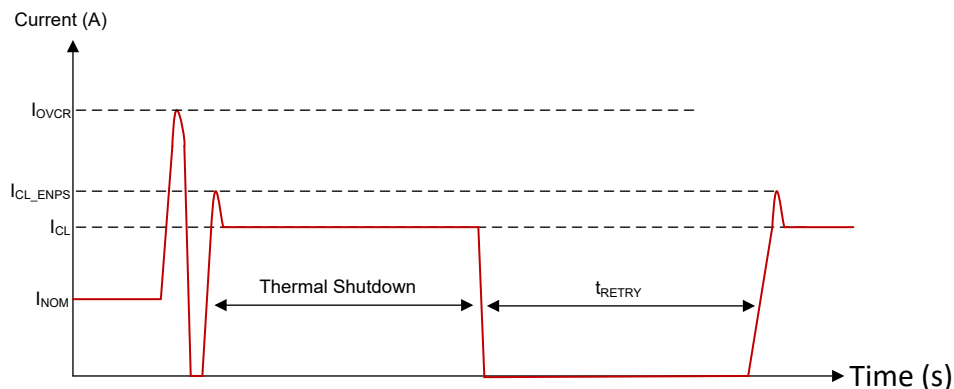


**图 8-12. Enable into Short-Circuit Behavior (LATCH=0)**

Due to the low impedance path, the output current rapidly increases until it hits the current limit threshold. Due to the response time of the current limiting circuit, the measured maximum current can temporarily exceed the  $I_{CL}$  value defined as  $I_{CL\_ENPS}$ , however, it settles to the current limit regulation value.

In this state, high power is dissipated in the FET, so eventually the internal thermal protection temperature for the FET is reached and the device safely shuts down. Then, if LATCH pin is low, the part waits  $t_{RETRY}$  amount of time and turns back on.

图 8-13 shows the behavior of the TPS1HC30-Q1 when a short circuit occurs when the device is in the on-state and already outputting current. When the internal pass FET is fully enabled, the current clamping settling time is slower so to ensure overshoot is limited the device implements a fast-trip level at a level  $I_{OVCR}$ . When this fast-trip threshold is hit, the device immediately shuts off for a short period of time before quickly re-enabling and clamping the current to  $I_{CL}$  level after a brief transient overshoot to the higher peak current ( $I_{CL\_ENPS}$ ) level. The device then keeps the current clamped at the regulation current limit until the thermal shutdown temperature is hit and the device safely shuts off.



**图 8-13. On-State Short-Circuit Behavior**

Overload Behavior shows the behavior of the TPS1HC30-Q1 when there is a small change in impedance that sends the load current above the  $I_{CL}$  threshold. The current rises to  $I_{CL\_LINPK}$  above the regulation level. Then the current limit regulation loop kicks in and the current drops to the  $I_{CL}$  value.

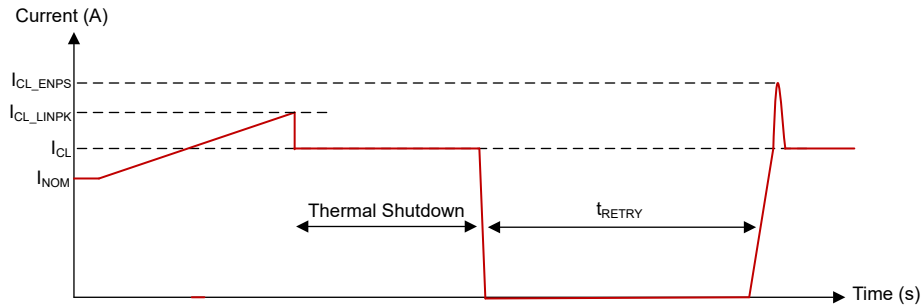


图 8-14. Overload Behavior

In all of these cases, the internal thermal shutdown is safe to hit repetitively. There is no device risk or lifetime reliability concerns from repeatedly hitting this thermal shutdown level.

#### 8.3.4.2 Open-Load and Short-to-Battery Detection

When the main channel is enabled, faults are diagnosed by reading the voltage on the SNS or FLT pin and judged by the user. A benefit of high-accuracy current sense is that this device can achieve a very low open-load detection threshold, which correspondingly expands the normal operation region. TI suggests 15 mA as the upper limit for the open-load detection threshold and 30 mA as the lower limit for the normal operation current. In 图 8-15, the recommended open-load detection region is shown as the dark-shaded region and the light-shaded region is for normal operation. As a guideline, do not overlap these two regions.

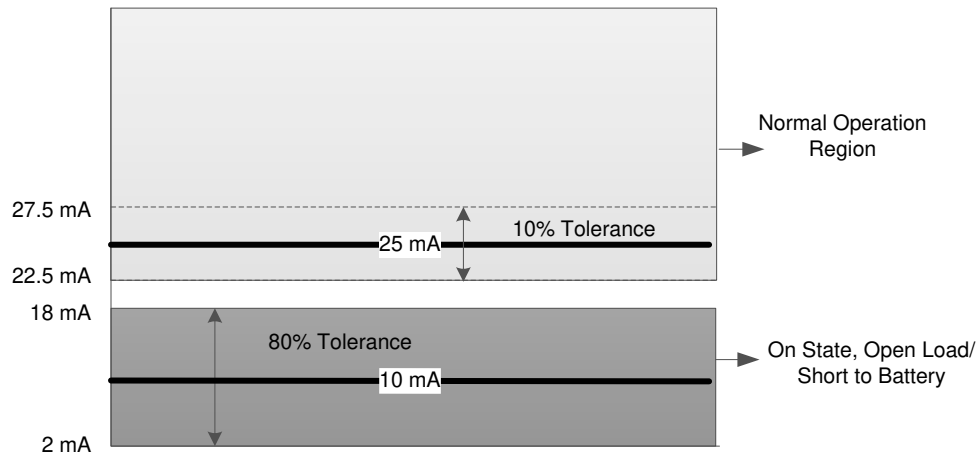


图 8-15. On-State Open-Load Detection and Normal-Operation Diagram

In the off state, if a load is connected, the output voltage is pulled to 0 V. In the case of an open load, the output voltage is close to the supply voltage,  $V_{BB} - V_{OUT} < V_{OL,off}$ . The FLT pin goes low to indicate the fault to the MCU, and the SNS pin is pulled up to  $V_{SNSFH}$ . There is always a leakage current  $I_{OL,off}$  present on the output, due to the internal logic control path or external humidity, corrosion, and so forth. Thus, TI implemented an internal pullup resistor to offset the leakage current. This pullup current must be less than the output load current to avoid false detection in the normal operation mode. To reduce the standby current, TI implemented a switch in series with the pullup resistor controlled by the DIAG\_EN pin. The pullup resistor value is  $R_{PU} = 150\text{ k}\Omega$ .

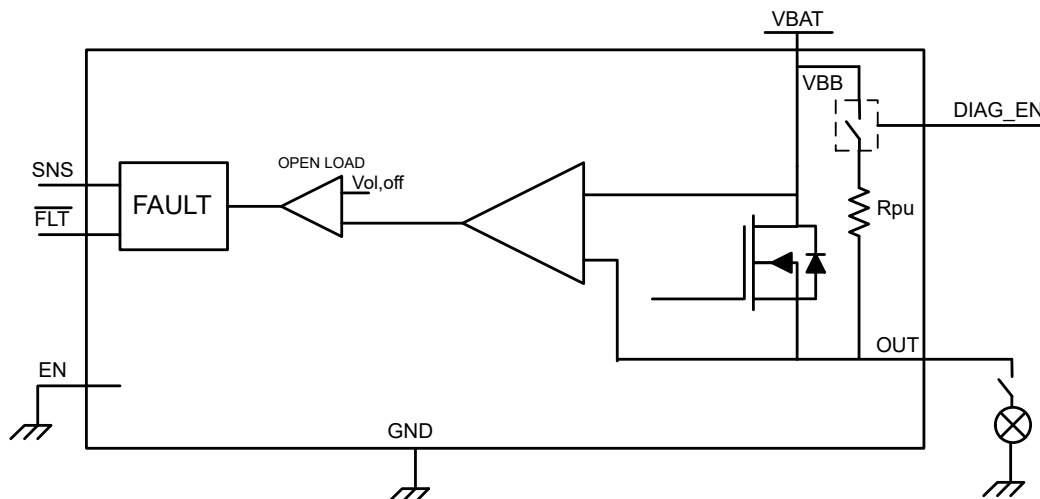


图 8-16. Open-Load Detection Circuit

#### 8.3.4.3 Short-to-Battery Detection

Short-to-battery detection has the same detection mechanism and behavior as open-load detection, both in the on-state and off-state. There is no way to differentiate between open load and short-to-battery in this device, but the system detects the fault and protects accordingly. See 表 8-2 for more details.

#### 8.3.4.4 Reverse-Polarity and Battery Protection

Reverse-polarity, commonly referred to as reverse battery, occurs when the ground of the device goes to the battery potential,  $V_{GND} = V_{BAT}$ , and the supply pin goes to ground,  $V_{BB} = 0$  V. In this case, if the EN pin has a path to the "ground" plane, then the FET turns on to lower the power dissipation through the main channel and prevent current flow through the body diode. Note that the resistor, diode ground network (if there is not a central blocking diode on the supply) must be present for the device to protect itself during a reverse battery event.

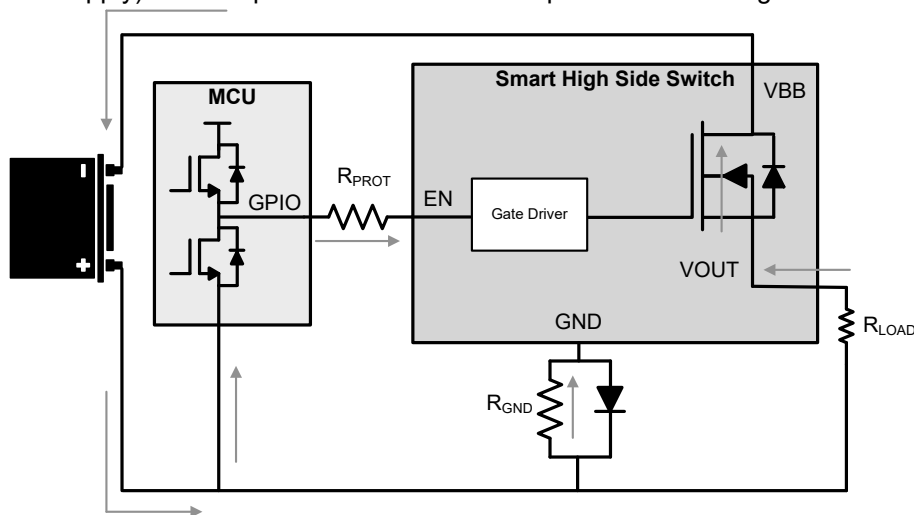


图 8-17. Reverse Battery Circuit

For more external protection circuitry information, see [Reverse Current Protection](#). See the fault truth table for more details.

#### 8.3.4.5 Latch-Off Mode

The TPS1HC30-Q1 comes with a latch functionality that decides after the channel is shut down due to a fault, whether or not to automatically try and turn back on, or stay off until other action is taken. This functionality is done by holding the LATCH pin high for latch-off functionality or holding LATCH low for auto-retry functionality.

The order the events occur is:

1. The device shuts down due to fault (thermal shutdown)
2. Wait  $t_{\text{RETRY}}$
3. If LATCH = 0
  - a. Turn back on the channel
4. If LATCH = 1
  - a. Keep off until LATCH = 0 || EN = 0
    - i. Then if LATCH = 0 and EN = 1
      1. Turn on channel into auto-retry mode
    - ii. If LATCH = 1 and EN = 1
      1. Turn on channel into latch mode where if another fault occurs then output is latched off again

For more information, see [Thermal Protection Behavior](#).

#### 8.3.4.6 Thermal Protection Behavior

The thermal protection behavior can be split up into three categories of events that can happen. [图 8-18](#) shows each of these categories.

1. **Relative thermal shutdown:** The device is enabled into an overcurrent event. The DIAG\_EN pin is high so that diagnostics can be monitored on SNS and FLT (however, DIAG\_EN being high is not necessary for all protection features to function). The output current rises up to the  $I_{\text{ILIM}}$  level and the FLT goes low while the SNS goes to  $V_{\text{SNSFH}}$ . With this large amount of current going through, the junction temperature of the FET increases rapidly with respect to the controller temperature. When the power FET temperature rises  $T_{\text{REL}}$  amount above the controller junction temperature  $\Delta T = T_{\text{FET}} - T_{\text{CON}} > T_{\text{REL}}$ , the device shuts down. The faults are continually shown on SNS and FLT and the part waits for the  $t_{\text{RETRY}}$  timer to expire. When  $t_{\text{RETRY}}$  timer expires, because the LATCH pin is low and EN is still high, the device comes back on into this  $I_{\text{ILIM}}$  condition.
2. **Absolute thermal shutdown:** The device is still enabled in an overcurrent event with DIAG\_EN high and LATCH still low. However, in this case the junction temperature rises up and hits an absolute reference temperature,  $T_{\text{ABS}}$ , and then shuts down. The device does not recover until both  $T_{\text{J}} < T_{\text{ABS}} - T_{\text{hys}}$  and the  $t_{\text{RETRY}}$  timer has expired.
3. **Latch-off mode:** The device is enabled into an overcurrent event. The DIAG\_EN pin is high so that diagnostics can be monitored on SNS and FLT. The output current rises up to the  $I_{\text{ILIM}}$  level and the FLT goes low while the SNS goes to  $V_{\text{SNSFH}}$ . If the part shuts down due to a thermal fault, either relative thermal shutdown or absolute thermal shutdown, the device does not enable the channel until either the LATCH pin OR the EN pin is toggled.

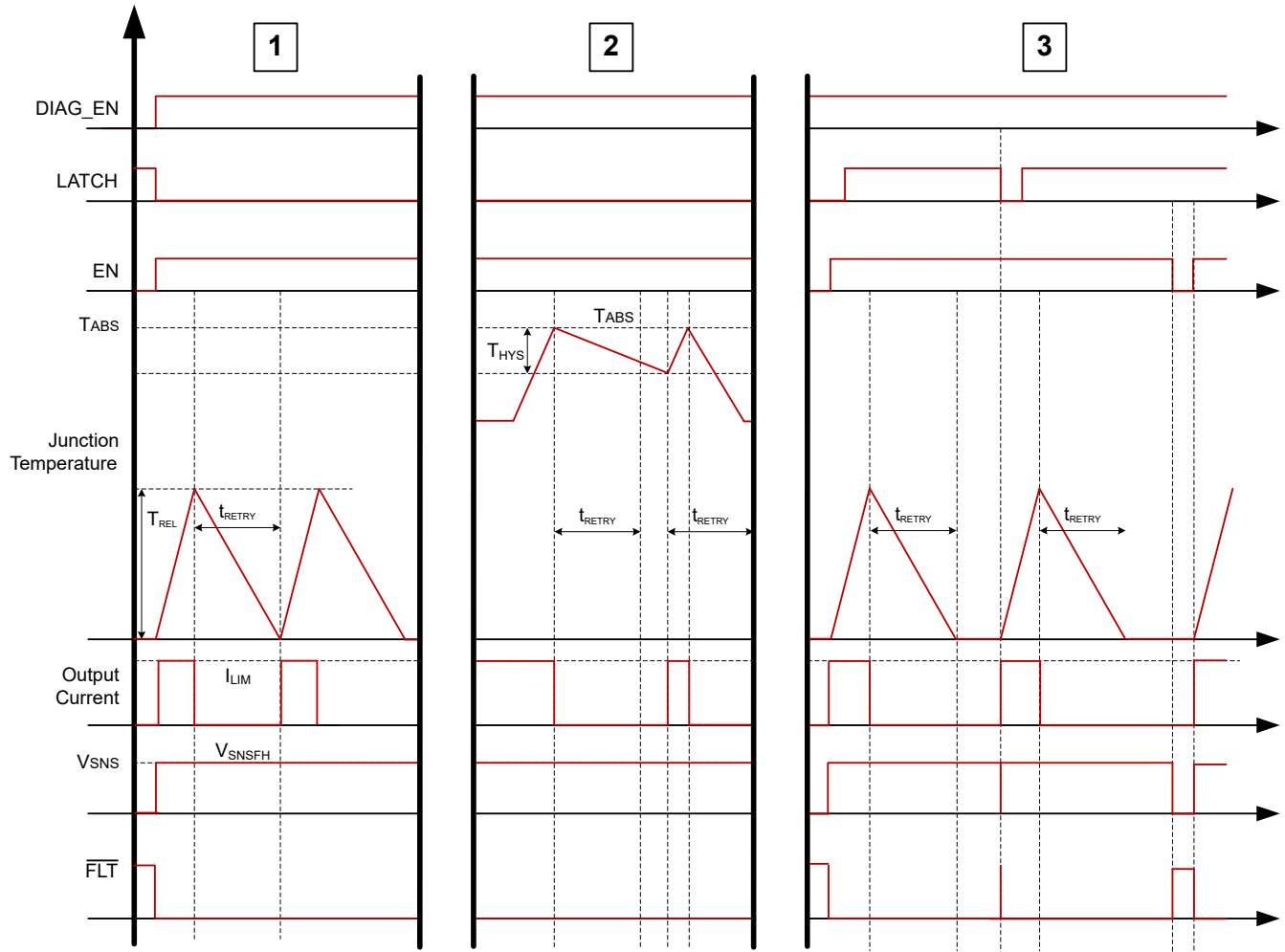


图 8-18. Thermal Behavior

#### 8.3.4.7 UVLO Protection

The device monitors the supply voltage  $V_{BB}$  to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to  $V_{UVLOF}$ , the output stage is shut down automatically. When the supply rises up to  $V_{UVLOR}$ , the device turns on. If an overcurrent event trips the UVLO threshold, the device shuts off and comes back on into a current limit safely.

### 8.3.4.8 Loss of GND Protection

When loss of GND occurs, output is turned off regardless of whether the input signal is high or low.

**Case 1 (Loss of Device GND):** Loss of GND protection is active when the thermal pad (Tab),  $I_{C\_GND}$ , and current limit ground are one trace connected to the system ground, as shown in the following figure.

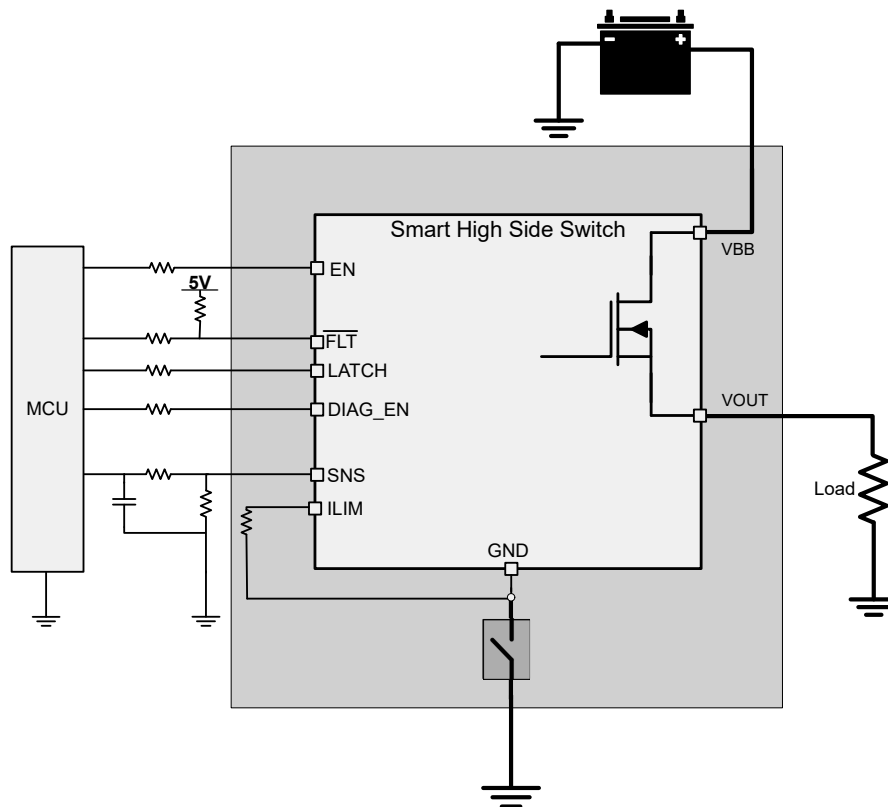


图 8-19. Loss of Device GND



**Case 2 (Loss of Module GND):** When the whole ECU module GND is lost, protections are also active. At this condition, the load GND remains connected.

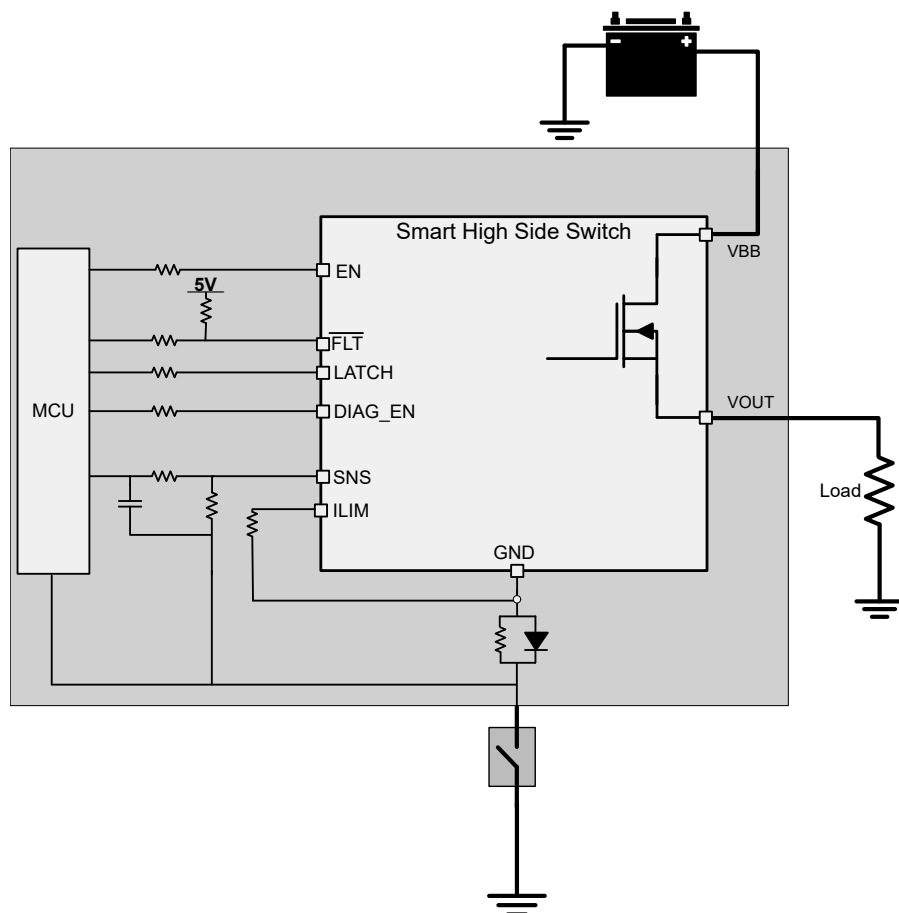


图 8-20. Loss of Module GND

### 8.3.4.9 Loss of Power Supply Protection

When loss of supply occurs, output is turned off regardless of whether the input is high or low. For a resistive or capacitive load, loss of supply protection is easy to achieve due to no more power. The worst case is a charged inductive load. In this case, the current is driven from all of the IOs to maintain the inductance output loop. TI recommends either the MCU serial resistor plus the GND network (diode and resistor in parallel) or external free-wheeling circuitry.

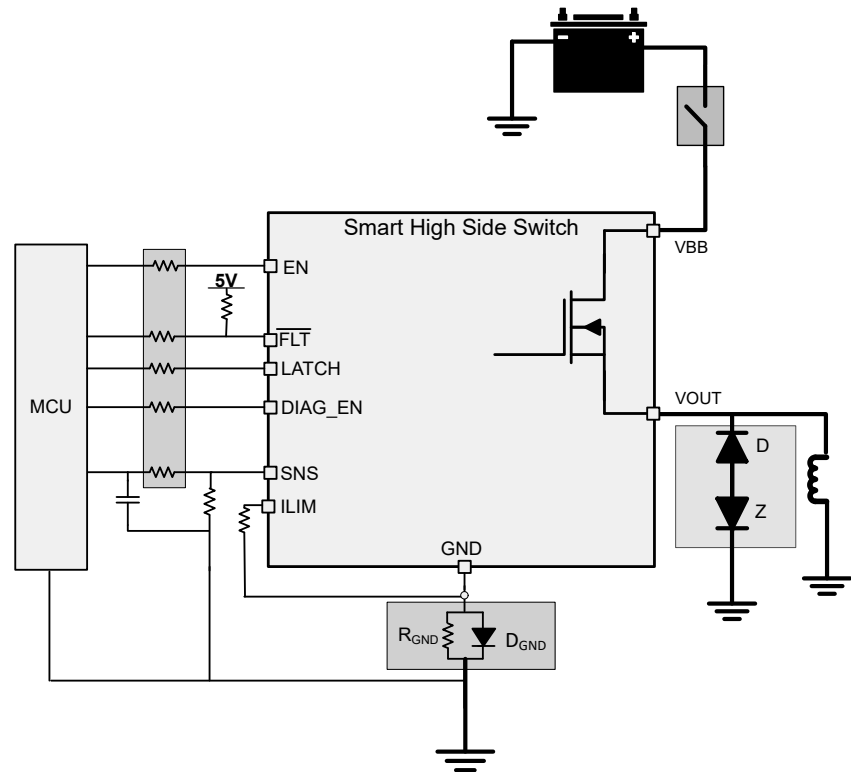


图 8-21. Loss of Battery

#### 8.3.4.10 Reverse Current Protection

**Method 1:** Blocking diode connected with  $V_{BB}$ . Both the device and load are protected when in reverse polarity. The blocking diode does not allow any of the current to flow during reverse battery condition.

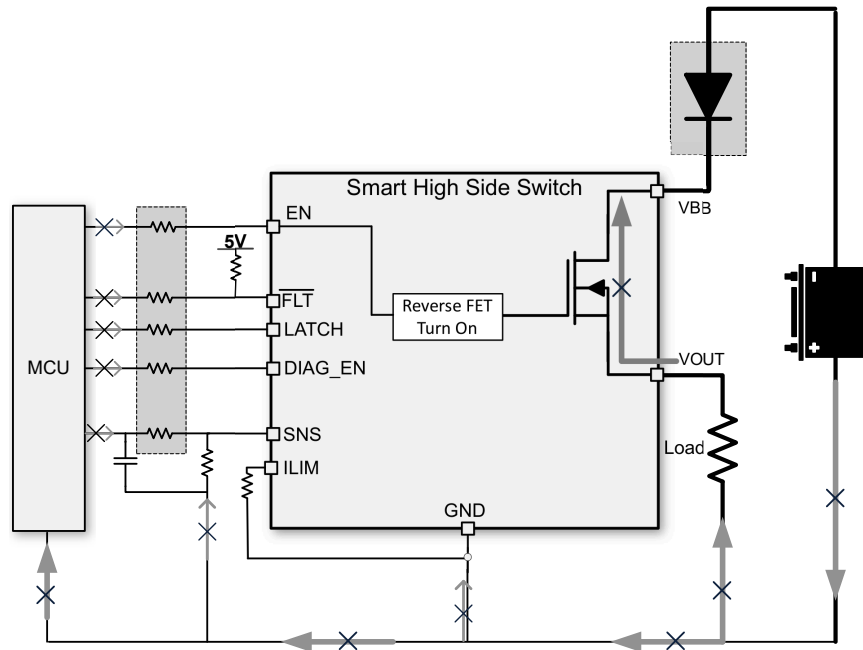


图 8-22. Reverse Protection with Blocking Diode

**Method 2 (GND Network Protection):** Only the high side device is protected under this connection. The load reverse current is limited by the impedance of the load itself. Note when reverse polarity happens, the continuous reverse current through the power FET must not make the heat build up be greater than the absolute maximum junction temperature. This can be calculated using the  $R_{ON(REV)}$  value and the  $R_{\theta JA}$  specification. No matter what types of connection are between the device GND and the board GND, if a GND voltage shift happens, ensure the following proper connections for the normal operation:

- Connect the current limit programmable resistor to the device GND.

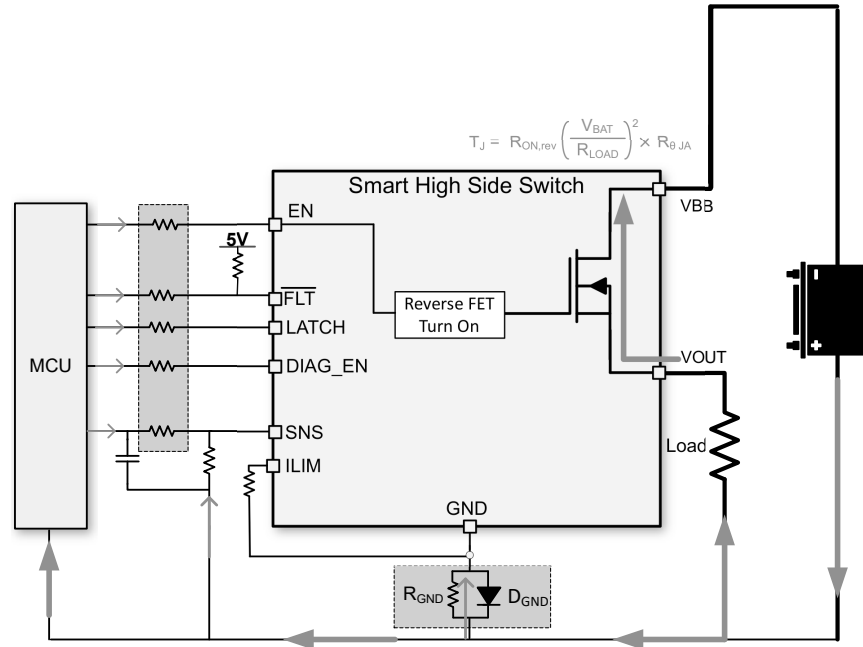


图 8-23. Reverse Protection with GND Network

- Recommendation - Resistor and Diode in Parallel:** A peak negative spike can occur when the inductive load is switching off, which can damage the HSD or the diode. So, TI recommends a resistor in parallel with the diode when driving an inductive load. The recommended selections are a 1-k $\Omega$  resistor in parallel with an  $I_F > 100\text{-mA}$  diode. If multiple high side switches are used, the resistor and diode can be shared among devices.

If multiple high side power switches are used, the resistor can be shared among devices.

- Ground Resistor:** The higher resistor value contributes to a better current limit effect when the reverse battery or negative ISO pulses.

$$R_{GND} \geq \frac{(-V_{CC})}{(-I_{GND})} \quad (12)$$

where

- $V_{CC}$  is the maximum reverse battery voltage (typically -16 V).
- $I_{GND}$  is the maximum reverse current the ground pin can withstand, which is available in the [Absolute Maximum Ratings](#).
- Ground Diode:** A diode is needed to block the reverse voltage, which also brings a ground shift based on the forward voltage of the diode. The ground diode must be  $\leq 400\text{ mV}$  to have full current limit capability. If the forward voltage becomes higher, the current limit can also increase from what the  $R_{ILIM}$  resistor is set to. Additionally, the diode must be approximately 200-V reverse voltage for the ISO 7637 pulse 1 testing so that it does not get biased.

### 8.3.4.11 Protection for MCU I/Os

In many conditions, such as the negative ISO pulse, or the loss of battery with an inductive load, a negative potential on the device GND pin can damage the MCU I/O pins (more likely, the internal circuitry connected to the pins). Therefore, the serial resistors between MCU and HSS are required.

Also, for proper protection against loss of GND, TI recommends 5-k $\Omega$  resistance for the R<sub>PROT</sub> resistors.

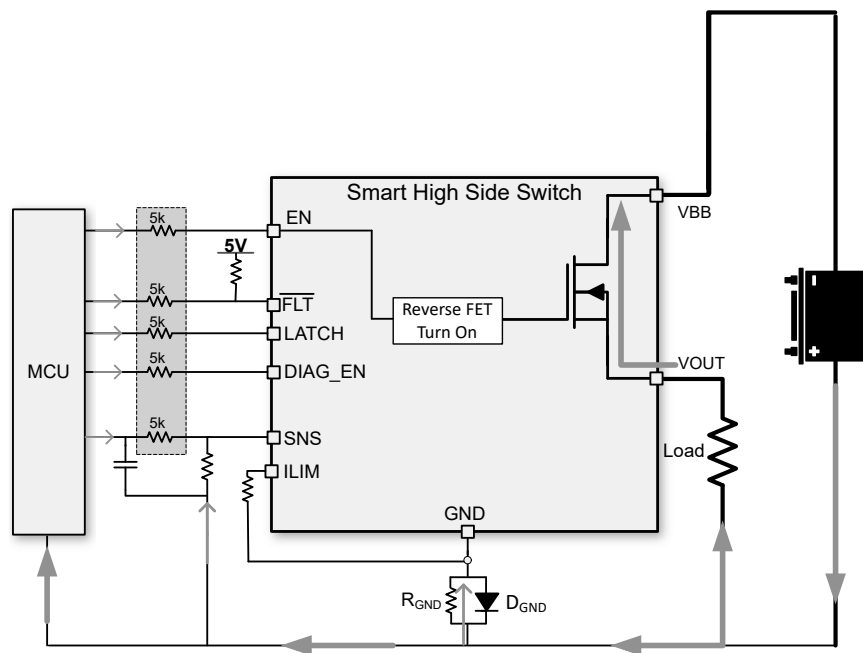


图 8-24. MCU I/O Protections

### 8.3.5 Diagnostic Enable Function

The diagnostic enable pin, DIAG\_EN, offers multiplexing of the microcontroller diagnostic input for current sense or digital status, by sharing the same sense resistor and ADC line or I/O port among multiple devices.

In addition, during the output-off period, the diagnostic disable function lowers the current consumption for the standby condition. The three working modes in the device are normal mode ( $I_Q$ ), standby mode ( $I_{STBY}$ ), and standby mode with diagnostic ( $I_{DIA}$ ). If off-state power saving is required in the system, the standby current is < 500 nA with DIAG\_EN low. If the off-state diagnostic is required in the system, the typical standby current is around 1 mA with DIAG\_EN high.

## 8.4 Device Functional Modes

### 8.4.1 Working Mode

The three working modes in the device are normal mode, standby mode, and standby mode with diagnostic. If an off-state power saving is required in the system, the standby current is less than 500 nA with EN and DIAG\_EN low. If an off-state diagnostic is required in the system, the typical standby current is around 1.2 mA with DIAG\_EN high. Note that entering standby mode requires IN low and  $t > t_{STBY}$ .  $t_{STBY}$  is the standby mode deglitch time, which is used to avoid false triggering or interfere with PWM switching. The following figure shows a work mode state-machine state diagram.

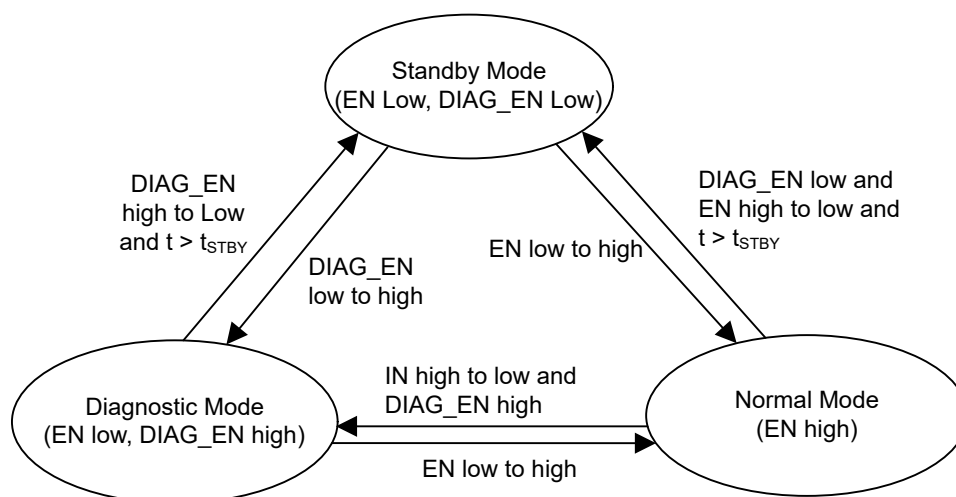


图 8-25. Work Mode State Machine

## 9 Application and Implementation

### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The following discussion notes how to implement the device to distinguish the different fault modes and implement a transient-pulse immunity test.

In some applications, open load, short-to-battery, and short to GND must be distinguished from each other. This action requires two steps.

### 9.2 Typical Application

图 9-1 shows an example of how to design the external circuitry parameters.

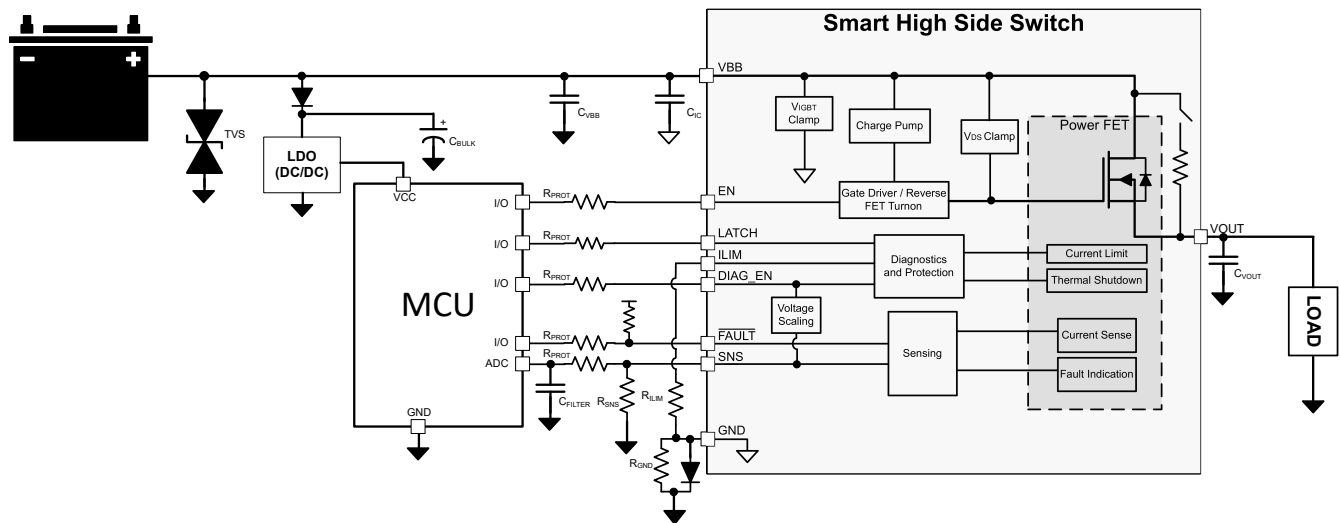


图 9-1. Typical Application Circuitry

### 9.2.1 Design Requirements

| Component | Description               | Purpose   |
|-----------|---------------------------|---|
| TVS       | SMBJ36CA (optional)       | Filter voltage transients coming from battery (ISO7637-2)   |
| CVBB      | 220 nF (optional)         | Better EMI performance  |
| CIC       | 100 nF                    | Minimal amount of capacitance on input for EMI mitigation   |
| CBULK     | 2 – 10 $\mu$ F (optional) | There to hold the rail for the LDO; however, helps to filter voltage transients on supply rail. Not a requirement but can be useful for ISO7637-2 transients. |
| RPROT     | 5 k                       | Protection resistor for microcontroller and device I/O pins   |
| RILIM     | 7 k – 70 k                | Set current limit threshold   |
| RSNS      | 1 k                       | Translate the sense current into sense voltage.   |
| CFILTER   | 100 nF                    | Coupled with RPROT on the SNS line creates a low pass filter to filter out noise going into the ADC of the MCU  |
| CVOUT     | 22 nF                     | Improves EMI performance, filtering of voltage transients   |
| RGND      | 1 k $\Omega$              | Stabilize GND potential during turn-off of inductive load   |
| DGND      | BAS21 Diode               | Keeps GND close to system ground during normal operation  |

### 9.2.2 Detailed Design Procedure

To keep maximum voltage on the SNS pin at an acceptable range for the system, use the following equation to calculate the  $R_{SNS}$ . To achieve better current sense accuracy. A 1% accuracy or better resistor is preferred.

$$(V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,max} \leq R_{SNS} \leq V_{ADC,min} \times K_{SNS} / I_{LOAD,min} \quad (13)$$

表 9-1. Typical Application

| Parameter      | Value |
|----------------|-------|
| $V_{DIAG\_EN}$ | 5 V   |
| $I_{LOAD,max}$ | 6 A   |
| $I_{LOAD,min}$ | 20 mA |
| $V_{ADC,min}$  | 5 mV  |
| $V_{HR}$       | 1 V   |

For this application, an  $R_{SNS}$  value of approximately 1 k $\Omega$  can be chosen to satisfy the equation requirements.

$$(5 \text{ V} - 1 \text{ V}) \times 1814 / 6 \text{ A} \leq \approx 1 \text{ k}\Omega \leq 5 \text{ mV} \times 11814 / 20 \text{ mA} \quad (14)$$

In other applications, more emphasis can be put on the lower end measurable values which increases  $R_{SNS}$ . Likewise, if the higher currents are of more interest the  $R_{SNS}$  can be decreased. Note that the maximum current that can be measured without saturation is 12 A.

Having the maximum SNS voltage scale with the DIAG\_EN voltage removes the need for a Zener diode on the SNS pin going to the ADC.

To set the programmable current limit value at 7 A, use the following equation to calculate the  $R_{LIM}$ .

$$R_{LIM} = K_{CL} / I_{LIM} = 90 / 7 = 12.8 \text{ k}\Omega \quad (15)$$

TI recommends  $R_{PROT} = 5 \text{ k}\Omega$  to ensure the current going into the digital pins (EN, DIAG\_EN, LATCH) is limited.

TI recommends a 1-k $\Omega$  resistor and 200-V, 0.2-A diode (BAS21 for example) for the GND network.



Smart High Side Switch

EN

Gate Driver

Current Limiting Circuit

ILIM

GND

VBAT

VOUT

$I_{LIM} = \frac{K_{CL}}{R_{ILIM}}$

$I_{LIM2} = \frac{K_{CL} (R_{ILIM1} + R_{ILIM2})}{R_{ILIM1} R_{ILIM2}}$

$I_{LIM1} = \frac{K_{CL}}{R_{ILIM}}$

$I_{NOM} = \frac{(V_{BB} - V_{OUT})}{R_{LOAD}}$

$I_{LIM} = C_{LOAD} \times \frac{dV_{DS}}{dt}$

$R_{ILIM2}$

$R_{ILIM1}$

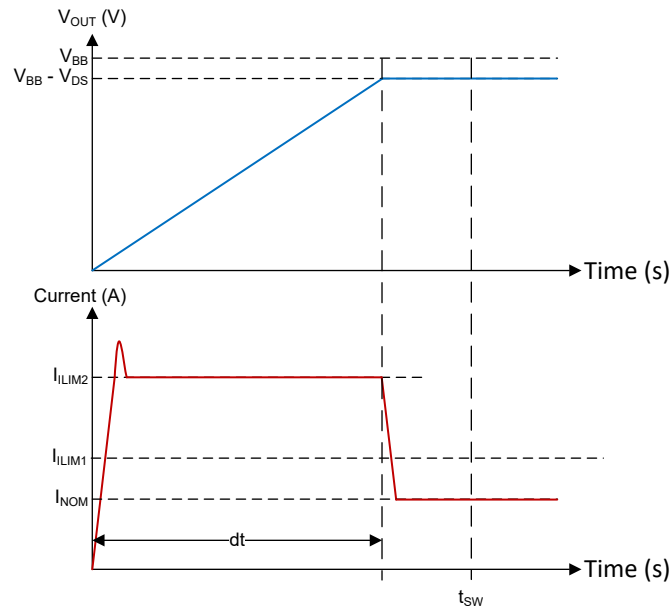
SW

$C_{LOAD}$

$R_{LOAD}$

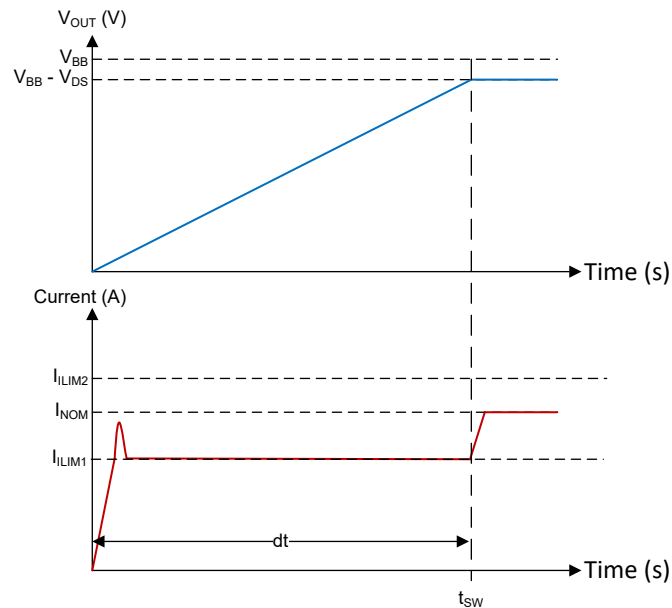
In a capacitive charging case, the initial current to charge the capacitor is the inrush current. Depending on the system requirements, dynamically changing the current limit can help either charge up a capacitor faster or charge up a larger capacitor. To allow a higher inrush level of current through in the beginning, the switch can be closed making the current limit be according to the equation below.

When the inrush event is over and the output voltage is charged up, the switch opens and the current limit is just the  $R_{ILIM1}$  equivalent level. This timing can be seen in 图 9-3.



**图 9-3. Capacitive Charging Changing Current Limit**

Alternatively, if the switch is open, the current limit starts out at a lower value and then the switch can be closed when the capacitance gets charged up. This lower current limit level allows higher value capacitance to be charged up. The timing diagram can be seen in 图 9-4.



**图 9-4. Large Capacitive Charging Changing Current Limit**

#### 9.2.2.2 EMC Transient Disturbances Test

Due to the severe electrical conditions in the automotive environment, immunity capacity against electrical transient disturbances is required, especially for a high side power switch, which is connected directly to the battery. Detailed test requirements are in accordance with the ISO 7637-2:2011 and ISO 16750-2:2010 standards. The TPS1HC30-Q1 device is tested and certificated by a third-party organization.

**表 9-2. ISO 7637-2:2011(E) in 12-V System<sup>(1) (2) (3) (4)</sup>**

| Test Item | Test Pulse Severity Level and vs Accordingly |       | Pulse Duration ( $t_d$ ) | Minimum Number of Pulses or Test Time | Burst-Cycle Pulse-Repetition Time |        | Input Resistance ( $\Omega$ ) | Function Performance Status Classification |
|-----------|--|-------|--------------------------|---------------------------------------|-----------------------------------|--------|-------------------------------|--|
|           | Level  | Vs/V  |                          |                                       | MIN                               | MAX    |                               |  |
| 1         | III  | - 112 | 2 ms                     | 500 pulses                            | 0.5 s                             | —      | 10                            | Status II                                  |
| 2a        | III  | 55    | 50 $\mu$ s               | 500 pulses                            | 0.2 s                             | 5 s    | 2                             | Status II                                  |
| 2b        | IV   | 10    | 0.2 to 2 s               | 10 pulses                             | 0.5 s                             | 5 s    | 0 to 0.05                     | Status II                                  |
| 3a        | IV   | - 220 | 0.1 $\mu$ s              | 1 h                                   | 90 ms                             | 100 ms | 50                            | Status II                                  |
| 3b        | IV   | 150   | 0.1 $\mu$ s              | 1 h                                   | 90 ms                             | 100 ms | 50                            | Status II                                  |

- (1) Tested both under input low condition and high condition.  
(2) The pulse 2-A voltage is 54-V maximum from VBB with respect to ground. A voltage suppressing mechanism must be used to pass Level III. This test was run with an 2-  $\mu$  F capacitor from VBB to ground.  
(3) GND pin network is a 1-k  $\Omega$  resistor in parallel with a diode BAS21-7-F.  
(4) Status II: The function does not perform as designed during the test, but returns automatically to normal operation after the test.

**表 9-3. ISO 16750-2:2010(E) Load Dump Test B in 12-V System<sup>(1) (2) (3) (4) (5)</sup>**

| Test Item | Test Pulse Severity Level and vs Accordingly |      | Pulse Duration ( $t_d$ ) | Minimum Number of Pulses or Test Time | Burst-Cycle Pulse-Repetition Time | Input Resistance ( $\Omega$ ) | Function Performance Status Classification |
|-----------|--|------|--------------------------|---------------------------------------|-----------------------------------|-------------------------------|--|
|           | Level  | Vs/V |                          |                                       |                                   |                               |  |
| Test B    |  | 35   | 40 to 400 ms             | 5 pulses                              | 60 s                              | 0.5 to 4                      | Status II                                  |

- (1) Tested both under input low condition and high condition (DIAG\_EN, EN, and VBB are all classified as inputs).  
(2) Considering the worst test condition, the device is tested without any filter capacitors on VBB and VOUT.  
(3) The GND pin network is a 1-k  $\Omega$  resistor in parallel with a diode BAS21-7-F.  
(4) Status II: The function does not perform as designed during the test, but returns automatically to normal operation after the test.  
(5) Select a 36-V external suppressor.

### 9.3 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 12-V automotive system. The supply voltage must be within the range specified in the [Recommended Operating Conditions](#).

**表 9-4. Voltage Operating Ranges**

| VBB Voltage Range | Note  |
|-------------------|---|
| 3 V to 6 V        | Extended lower 12-V automotive battery operation such as cold crank and start-stop. Device is fully functional and protected but some parametrics such as $R_{ON}$ , current sense accuracy, current limit accuracy and timing parameters can deviate from specifications. Check the individual specifications in the Electrical Characteristics to confirm the voltage range it is applicable for. |
| 6 V to 18 V       | Nominal 12-V automotive battery voltage range. All parametric specifications apply and the device is fully functional and protected.  |
| 18 V to 24 V      | Extended upper 12-V automotive battery operation such as double battery. Device is fully functional and protected but some parametrics such as $R_{ON}$ , current sense accuracy, current limit accuracy, and timing parameters can deviate from specifications. Check the individual specifications in the Electrical Characteristics to confirm the voltage range it is applicable for.           |
| 35 V              | Load dump voltage. Device is operational and lets the pulse pass through without being damaged but does not protect against short circuits.   |

## 9.4 Layout

### 9.4.1 Layout Guidelines

To prevent thermal shutdown,  $T_J$  must be less than  $150^{\circ}\text{C}$ . If the output current is very high, the power dissipation can be large. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the board opposite the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- Plate shut or plug and cap all thermal vias on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage must be at least 85%.

### 9.4.2 Layout Example

#### 9.4.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

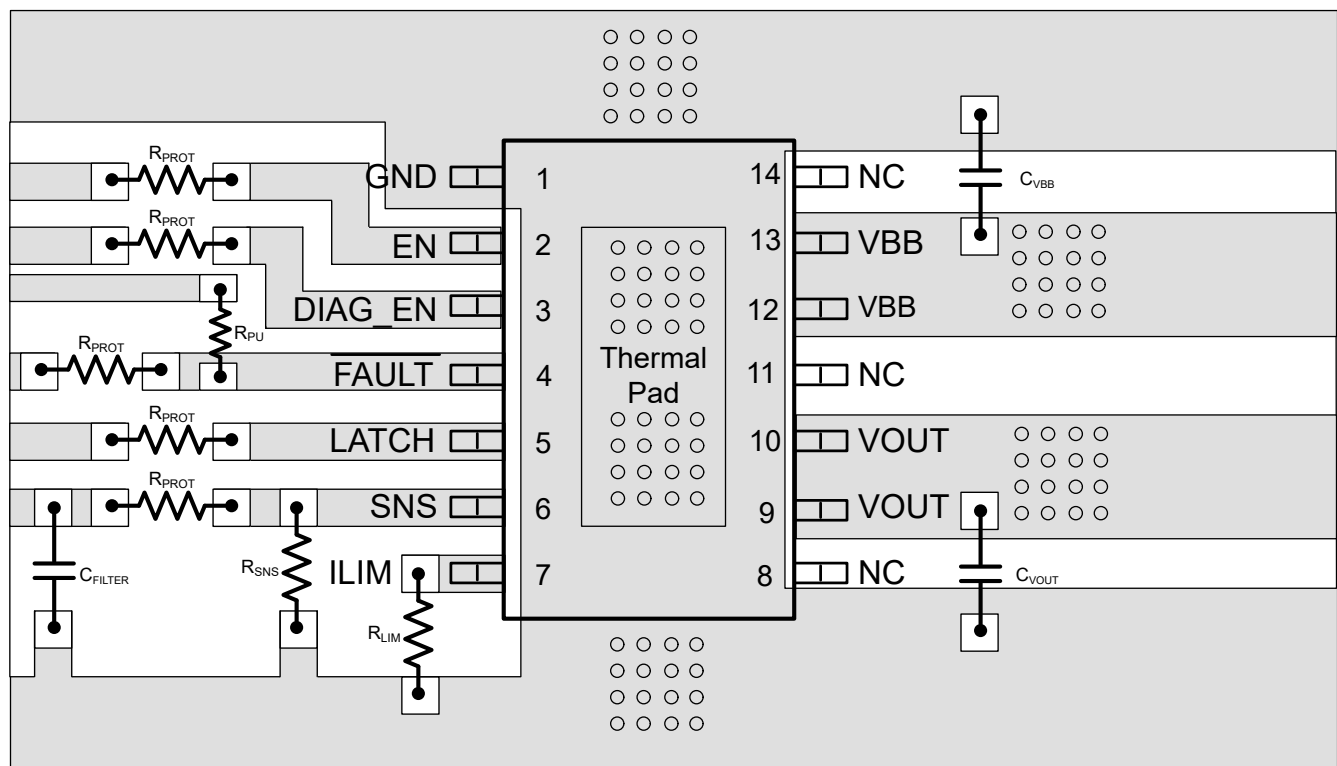


图 9-5. Layout Without a GND Network

#### 9.4.2.2 With a GND Network

With a GND network, tie the thermal pad with one trace through the GND network to the board GND copper.

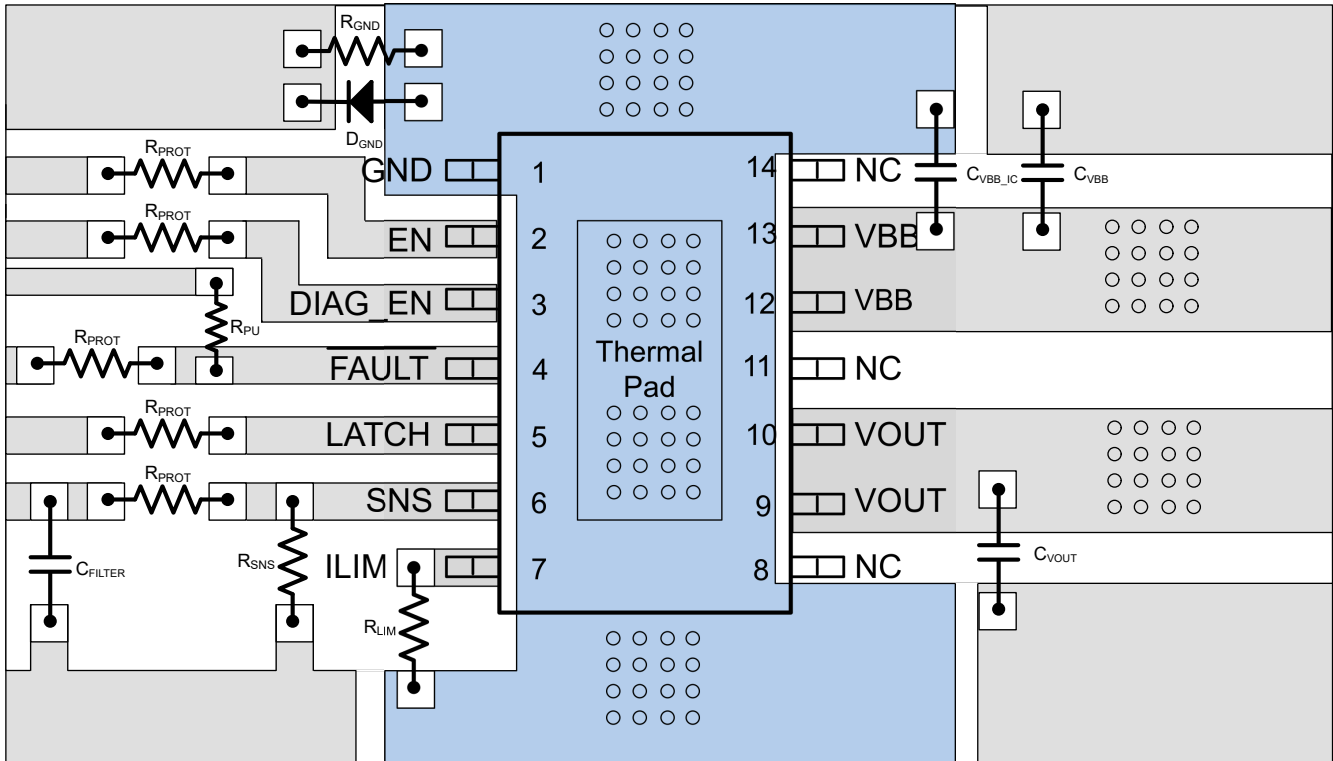


图 9-6. Layout With a GND Network

#### 9.4.3 Thermal Considerations

This device possesses thermal shutdown ( $T_{ABS}$ ) circuitry as a protection from overheating. For continuous normal operation, the junction temperature must not exceed the thermal-shutdown trip point. If the junction temperature exceeds the thermal-shutdown trip point, the output turns off. When the junction temperature falls below the thermal-shutdown trip point, the output turns on again.

Use the following equation to calculate the power dissipated by the device.

$$P_T = I_{OUT}^2 \times R_{DS(on)} + V_{BB} \times I_{NOM} \quad P_T = I_{OUT}^2 \times R_{DS(on)} + V_S \times I_{nom} \quad (17)$$

where

- $P_T$  = Total power dissipation of the device

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + R_{\theta JA} \times P_T \quad T_J = T_A + R_{\theta JA} \times P_T \quad (18)$$

For more information, please see the [How to Drive Resistive, Inductive, Capacitive, and Lighting Loads application note](#).

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, [How to Drive Resistive, Inductive, Capacitive, and Lighting Loads application note](#)

### 10.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 10.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 10.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS1HC30BQPWPRQ1      | Active        | Production           | HTSSOP (PWP)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | 1HC30Q              |
| TPS1HC30BQPWPRQ1.A    | Active        | Production           | HTSSOP (PWP)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | 1HC30Q              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS1HC30BQPWPRQ1 | HTSSOP       | PWP             | 14   | 3000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS1HC30BQPWPRQ1 | HTSSOP       | PWP             | 14   | 3000 | 353.0       | 353.0      | 32.0        |

## GENERIC PACKAGE VIEW

**PWP 14**

**PowerPAD TSSOP - 1.2 mm max height**

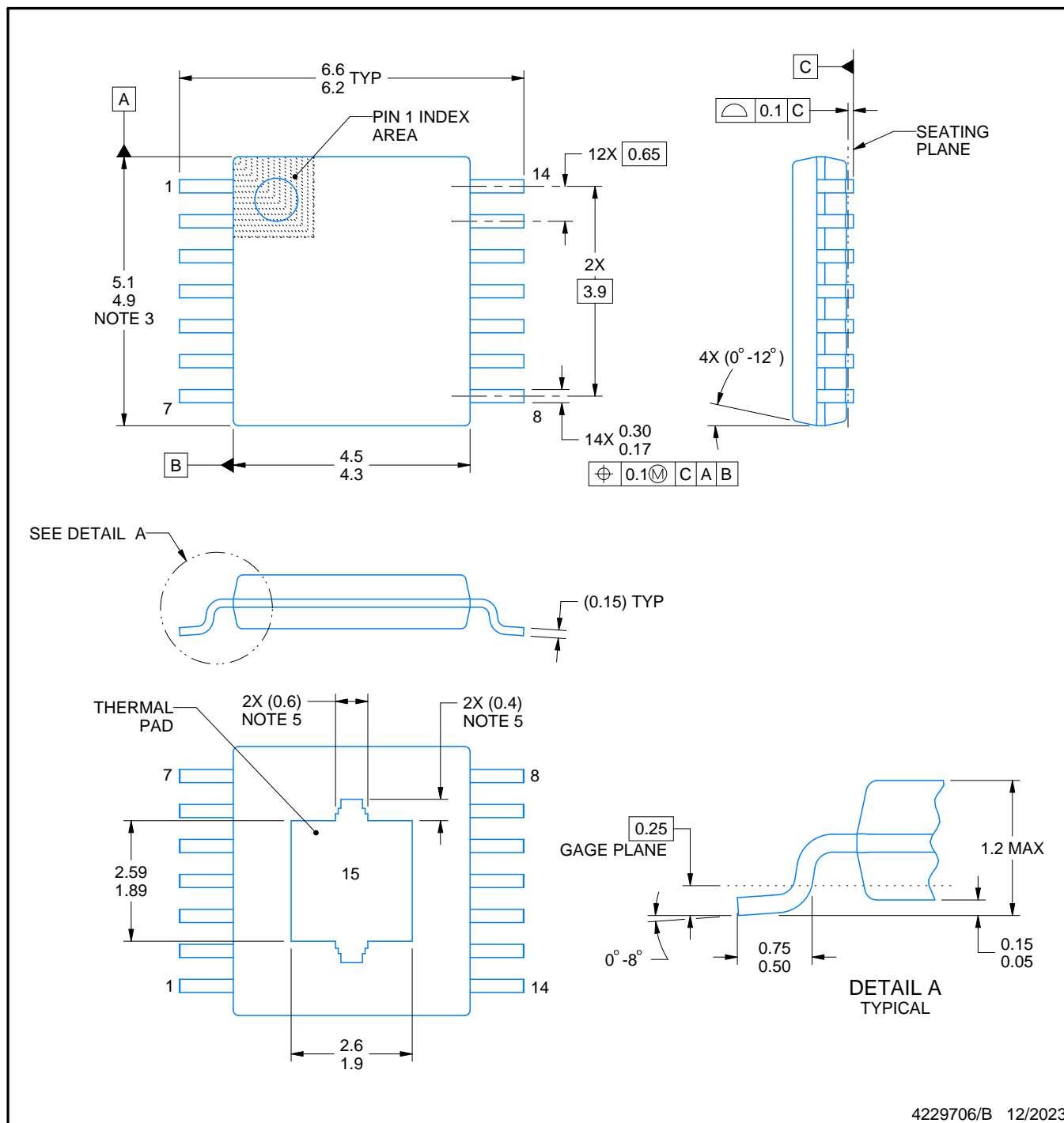
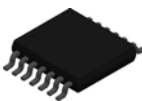
4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224995/A



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## NOTES:

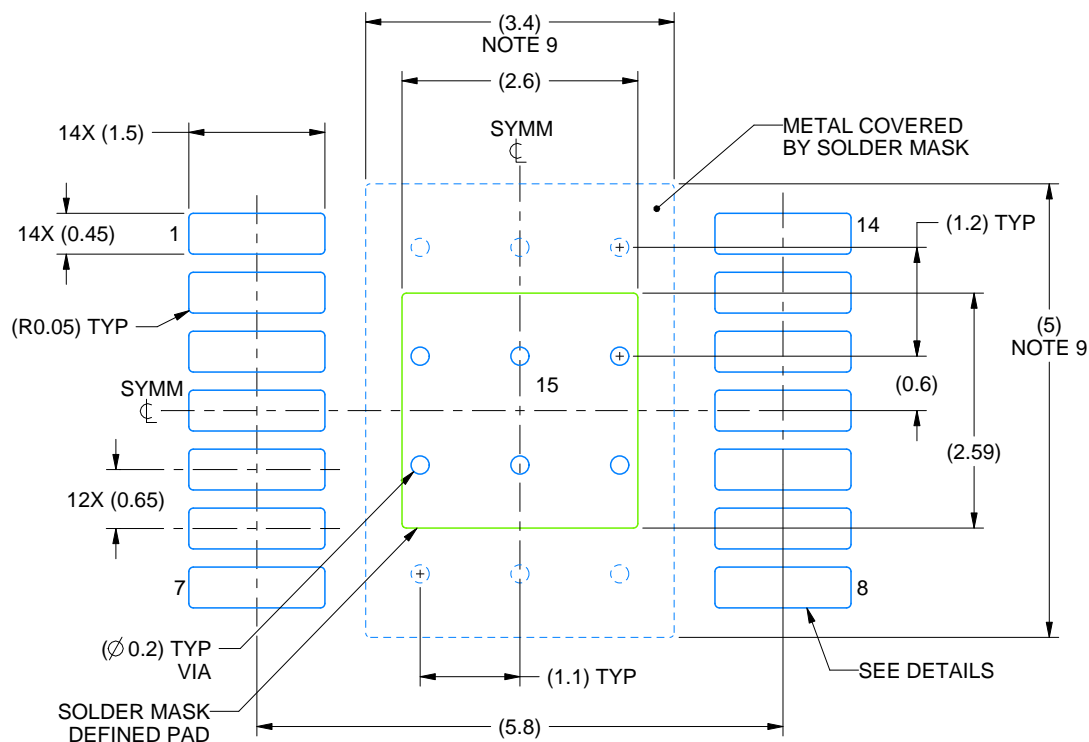
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

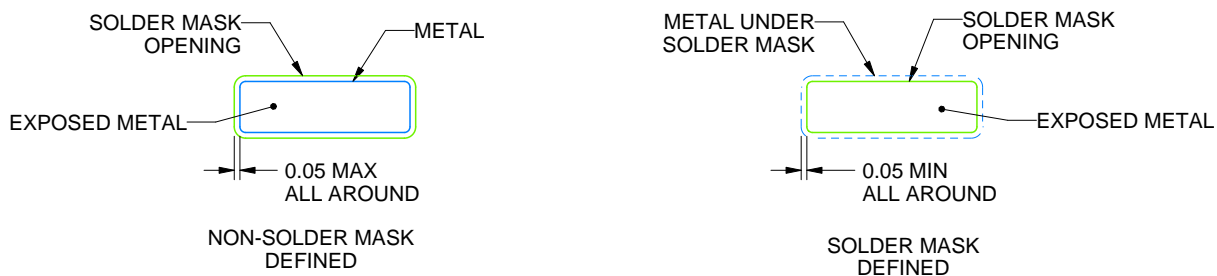
**PWP0014K**

## PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 12X



## SOLDER MASK DETAILS

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NOTES: (continued)

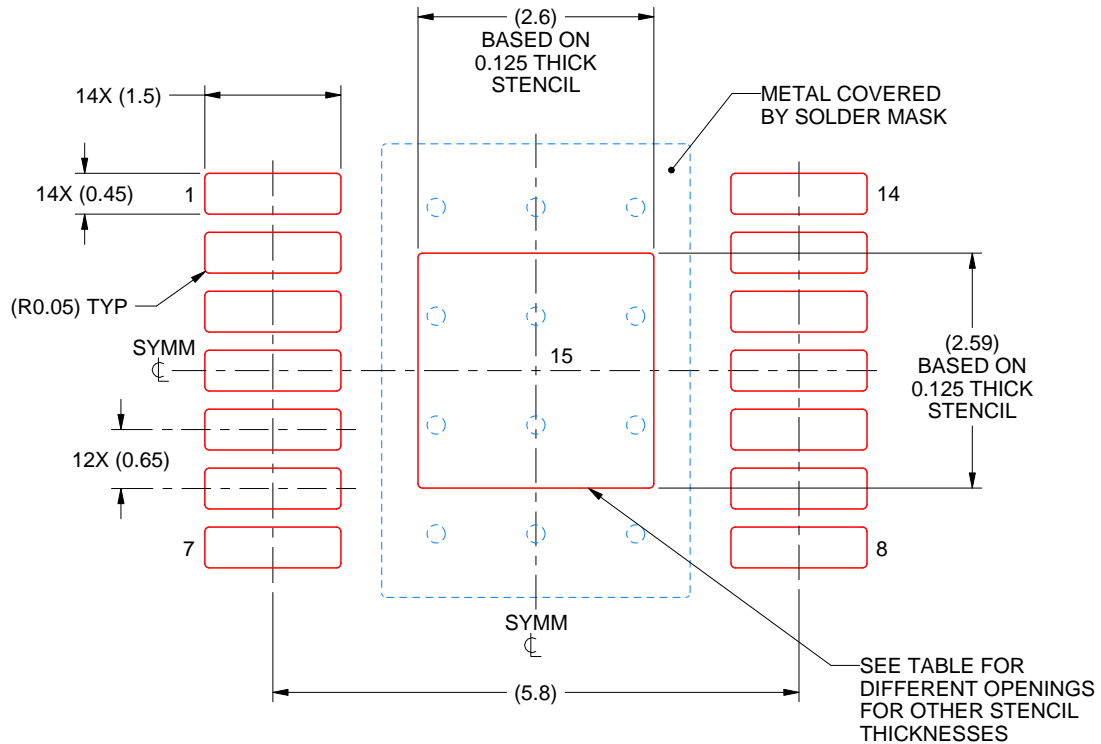
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 12X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 2.91 X 2.90            |
| 0.125             | 2.60 X 2.59 (SHOWN)    |
| 0.15              | 2.37 X 2.36            |
| 0.175             | 2.20 X 2.19            |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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