TPS1HC120-Q1, 120mΩ, 1.5A, Single-Channel Automotive Smart High-Side Switch

1 Features

- Single-channel smart automotive high-side switch with full diagnostics
  - Open-drain status output
  - Current sense analog output (1)
  - ON and OFF state open-load detection (1)
- Wide operating voltage: 3V to 28V
- Low standby current, < 0.5µA at 85°C
- Operating junction temperature, –40°C to 150°C
- Selectable current limit from 0.2A to 2.1A
- Protection
  - Overload and short-circuit protection
  - Inductive load negative voltage clamp
  - Undervoltage Lockout (UVLO) protection
  - Thermal shutdown and swing with self recovery
  - Loss-of-GND, loss-of-battery, and reverse battery protection
  - Auto-retry on soft-short, latch on hard-short(1)
- Diagnostic
  - Fault report for fast interrupt
  - On- and Off-state output open-load and short-to-battery detection(1)
  - Overcurrent and short-to-ground detection
  - Thermal shutdown and swing detection
- Qualifications
  - AEC-Q100 qualified for automotive:
    - Temperature: –40°C to 125°C, T_A
  - Electrical transient disturbance immunity certification of ISO7637-2 and ISO16750-2
- 8-pin small form factor SOT package

(1) Please see the device comparison table for features available to a specific variant.

2 Applications

- ADAS modules
- Automotive display module
- Body control module

3 Description

The TPS1HC120-Q1 is a fully protected high-side switch, with integrated NMOS power FET and charge pump, designed to meet the requirements of 12V automotive systems. The low R_{ON} (120mΩ typical) minimizes the device power dissipation when driving a wide range of output load current up to 1.5A.

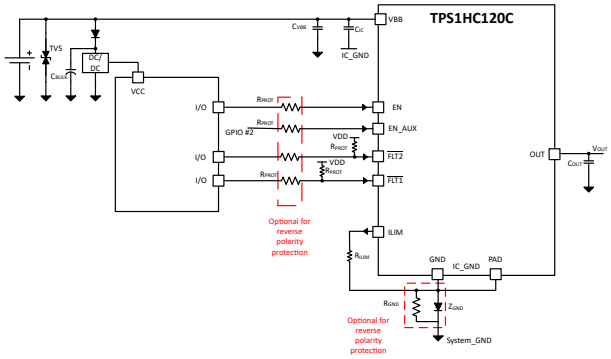
The device integrates protection features such as thermal shutdown, output clamp, and current limit. These features improve system robustness during fault events such as short circuit. The device implements a selectable high-accuracy current limit that improves the reliability of the system by reducing inrush current when driving large capacitive loads. For the A/B variants, the device also provides an accurate current sense that allows for improved load diagnostics such as overload and open-load detection. Low logic high threshold, V_{IH}, of 1.5V on the input pins allow use of MCUs down to 1.8V.

The TPS1HC120-Q1 can be used to drive a wide variety of resistive, inductive, and capacitive loads, including ADAS cameras, LEDs, relays, solenoids, and heaters. The device is available in a 8-pin, ultra-small form-factor 2.1mm × 1.6mm SOT package with 0.5mm pin pitch, minimizing the PCB footprint.

Package Information

PART NUMBER	PACKAGE	PACKAGE SIZE(1)
TPS1HC120-Q1	DYC (SOT, 8)	2.10mm × 1.60mm

(1) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic

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4 Device Comparison Table

PART NUMBER	ON-STATE OPEN LOAD REPORTING	OFF-STATE OPEN LOAD/SHORT-TO-BATTERY	CURRENT SENSE	BEHAVIOR AFTER THERMAL FAULT	EN ORING
TPS1HC120A-Q1(1)	×	✓	✓	Auto-retry	×
TPS1HC120B-Q1(1)	×	✓	✓	Latch	×
TPS1HC120C-Q1	✓	×	×	Hard-short auto-latch	✓

(1) Device in preview. Please contact TI for more information.

5 Pin Configuration and Functions

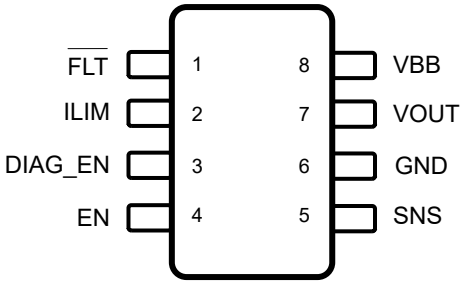


Figure 5-1. DYC Package, 8-Pin SOT (Top View), A, B Versions

Table 5-1. Pin Functions for A, B Versions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{\text{FLT}}$	O	Open drain fault output. Referred to as FLT, or fault pin. Recommended 4.7-10kΩ pullup resistor.
2	ILIM	I	Adjustable current limit. Connect a resistor to device GND, SHORT the pin to device GND, or leave the pin OPEN to set the current limit value.
3	DIAG_EN	I	Enable-disable pin for diagnostics, internal pulldown.
4	EN	I	Input control for channel activation, internal pulldown.
5	SNS	O	Analog current output.
6	GND	Power	Ground of device. Connect to resistor- diode ground network to have reverse battery protection.
7	VOUT	Power	Output of the high side switch.
8	VBB	Power	Power supply.

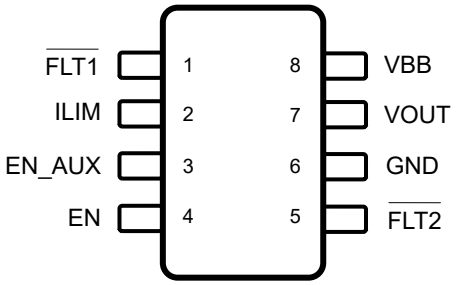


Figure 5-2. DYC Package, 8-Pin SOT (Top View), C Version

Table 5-2. Pin Functions for C Versions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{\text{FLT1}}$	O	Report current limit, short-circuit and thermal shutdown faults. Referred to as FLT1, or fault pin. Recommended 4.7-10kΩ pullup resistor.
2	ILIM	I	Adjustable current limit. Connect a resistor to device GND, SHORT the pin to device GND, or leave the pin OPEN to set the current limit value.
3	EN_AUX	I	Auxiliary input signal for channel activation, internal pulldown. Internally OR'ed with EN signal. Either EN or EN_AUX can be used to enable the output.
4	EN	I	Input control for channel activation, internal pulldown. Internally OR'ed with EN_AUX signal. Either EN or EN_AUX can be used to enable the output.
5	$\overline{\text{FLT2}}$	O	Report ON-state open-load fault. Referred to as FLT2, or fault pin. Recommended 4.7-10kΩ pullup resistor.
6	GND	Power	Ground of device. Connect to resistor- diode ground network to have reverse battery protection.
7	VOUT	Power	Output of the high side switch.
8	VBB	Power	Power supply.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VBB	Maximum continuous supply voltage			28	V
V_{LD}	Load dump voltage, ISO16750-2:2010(E)			35	V
V_{REV}	Reverse Polarity Voltage, maximum duration of 3 minutes and with the application circuit		–18		V
I_{EN}	Enable pin current		–1	20	mA
V_{EN}	Enable pin voltage		–1	7	V
I_{EN_AUX}	Enable Aux pin current		–1	20	mA
V_{EN_AUX}	Enable Aux pin voltage		–1	7	V
I_{FLT1}	FLT1 pin current		-30	10	mA
V_{FLT1}	FLT1 pin voltage		–0.3	7	V
I_{FLT2}	FLT2 pin current		–30	10	mA
V_{FLT2}	FLT2 pin voltage		–1	7	V
I_{ILIM}	ILIM pin current		-30	10	mA
V_{ILIM}	ILIM pin voltage		–0.3	7	V
I_{GND}	Reverse ground current, V_{BB} < 0 V			–50	mA
E_{AS}	Maximum Energy Dissipation, single Pulse	L_{OUT} = 5 mH, $T_{J,start}$ = 125°C, VBB = 28V, I_{OUT} = 1.7A		20	mJ
E_{AR}	Maximum Energy Dissipation, repetitive Pulse	L_{OUT} = 5 mH, $T_{J,start}$ = 125°C, VBB = 28V, I_{OUT} = 1.7A, 1M cycles		7.2	mJ
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per AEC Q100-002(2)	VBB and VOUT	±4000	V
			All other pins	±2000	
		Charged-device model (CDM), per AEC Q100-011	All pins	±750	

(1) All ESD strikes are with reference from the pin mentioned to GND
(2) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{VBB_NOM}	Nominal supply voltage (1)	4	18	V
V_{VBB_EXT}	Extended supply voltage(2)	3	28	V
V_{VBB_SC}	Short circuit supply voltage capability		28	V
V_{DIN}	All digital input pin voltage	–1	5.5	V
T_A	Operating free-air temperature	–40	125	°C

(1) All operating voltage conditions are measured with respect to device GND
(2) Device will function within extended operating range, however some parametric values might not apply.

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS1HC120-Q1 DYC (SOT) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the SPRA953 application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

6.5 Electrical Characteristics

V_{BB} = 6 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted); Typical application is 13.5V, 10Ω, R_{ILIM}=Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT							
$V_{DS,clamp}$	VDS clamp voltage	VBB = 13.5V	T_J = 25°C	35		42	V
			T_J = -40°C to 150°C	33		43	V
		VBB = 6V	T_J = 25°C	30		35	V
			T_J = -40°C to 150°C	25		35	V
V_{UVLOR}	V_{BB} undervoltage lockout rising	Measured with respect to the GND pin of the device		3.4	3.6	3.8	V
V_{UVLOF}	V_{BB} undervoltage lockout falling			2.4	2.6	2.9	V
I_{NOM}	Continuous load current	V_{EN} = 5V, T_A = 85°C			1.5		A
$I_{VBB,SLEEP}$	Standby or sleep current (total device leakage including MOSFET channels)	V_{BB} ≤ 18V, V_{EN} = V_{DIAG_EN} = 0 V for Version A/B, V_{EN} = 0V for Version C, V_{OUT} = 0 V	T_J = 25°C			0.1	µA
			T_J = 85°C			0.5	µA
			T_J = 150°C			12	µA
$I_{LEAK,SLEEP}$	Output leakage current in sleep mode (measured from VOUT pin when VOUT is shorted to GND)	V_{BB} ≤ 18 V, V_{EN} = V_{DIAG_EN} = 0 V for Version A/B, V_{EN} = 0V for Version C, V_{OUT} = 0 V	T_J = 25°C		0.01	0.1	µA
			T_J = 85°C			0.4	µA
			T_J = 150°C			12	µA
I_Q	Quiescent current in normal mode, channel enabled (Version C)	V_{BB} ≤ 18V, V_{EN} = 5V, I_{OUT} = 0 A			2.3	3	mA
t_{STBY}	Standby mode delay time	V_{EN} = V_{DIAG_EN} = 0 V for Version A/B, V_{EN} = 0V for Version C, to standby			20		ms
RON CHARACTERISTICS							
R_{ON}	On-resistance (Includes MOSFET channel and metallization on die)	6 V ≤ V_{BB} ≤ 28 V, I_{OUT} = 1 A	T_J = 25°C		120		mΩ
			T_J = 150°C			240	mΩ
		3V ≤ V_{BB} ≤ 6V, I_{OUT} = 1A	T_J = 25°C		140		mΩ
			T_J = 150°C			290	mΩ

6.5 Electrical Characteristics (continued)

V_{BB} = 6 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted); Typical application is 13.5V, 10Ω, R_{ILIM}=Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_{ON(REV)}$	On-resistance during reverse polarity	-18 V ≤ V_{BB} ≤ -6 V	T_J = 25°C		125		mΩ
			T_J = 150°C			255	mΩ
CURRENT LIMIT CHARACTERISTICS							
$I_{CL\_FLT1\_RISING}$	Current limit fault assertion threshold, Current rising	I_{CL} = 1.8 A, T_J = -40°C to 150°C			0.9 × I_{CL}		
		I_{CL} = 500 mA, T_J = -40°C to 150°C			0.84 × I_{CL}		
$I_{CL\_FLT1\_FALLING}$	Current limit fault de-assertion threshold, Current falling	I_{CL} = 1.8 A, T_J = -40°C to 150°C			0.82 × I_{CL}		
		I_{CL} = 500 mA, T_J = -40°C to 150°C			0.76 × I_{CL}		
I_{CL_LINPK}	Linear Mode peak	T_J = -40°C to 150°C dI/dt ≤ 0.01 A/ms		I_{CL}		1.15 × I_{CL}	
I_{CL_ENPS}	Peak current enabling into permanent short	T_J = -40°C to 150°C	5 µH + 100 mΩ			3 × I_{CL}	A
I_{OVCR}	OVCR Peak current threshold when short is applied while switch enabled	T_J = -40°C to 150°C	5 µH + 100 mΩ			6.5	A
I_{CL}	I_{CL} Current Limit Regulation Level	T_J = -40°C to 150°C, V_{DS} ≤ 3V	R_{ILIM} = 6.75 kΩ		2		A
			R_{ILIM} = 7.5 kΩ		1.73		A
			R_{ILIM} = 8.4 kΩ		1.61		A
			R_{ILIM} = 9.6 kΩ		1.41		A
			R_{ILIM} = 11.3 kΩ		1.2		A
			R_{ILIM} = 13.5 kΩ		1.02		A
			R_{ILIM} = 16.9 kΩ		0.8		A
			R_{ILIM} = 22.9 kΩ	0.519	0.59	0.661	A
			R_{ILIM} = 27 kΩ	0.445	0.5	0.555	A
			R_{ILIM} = 33.75 kΩ	0.352	0.4	0.448	A
			R_{ILIM} = 67.5 kΩ		0.2		A
			R_{ILIM} = Open, short, or out of range (> 67.5kΩ or < 6.75kΩ)	1.7	2.1	2.7	A
FAULT CHARACTERISTICS							
t_{INRUSH}	Inrush period for retrying (Version C)	V_{EN} = 0V to 5V			20		ms
$I_{OL,ON(ENTER)}$	ON state open-load entering threshold (Version C)	V_{EN} = 5 V		15	30	50	mA
$I_{OL,ON(EXIT)}$	ON state open-load exiting threshold (Version C)	V_{EN} = 5 V		45	65	80	mA
$I_{OL,ON(HYST)}$	ON state open-load exiting hysteresis (Version C)	V_{EN} = 5 V		20	33	45	mA
$t_{OL,ENTER}$	ON state open-load deglitch time, enter (Version C)	V_{EN} = 5 V, I_{LOAD} < $I_{OL,ON(ENTER)}$			10		ms
$t_{OL,EXIT}$	ON state open-load deglitch time, exit (Version C)	V_{EN} = 5 V, I_{LOAD} > $I_{OL,ON(EXIT)}$			60		µs
T_{ABS}	Thermal shutdown			150	165	185	°C

6.5 Electrical Characteristics (continued)

V_{BB} = 6 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted); Typical application is 13.5V, 10Ω, R_{ILIM}=Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{REL}	Relative thermal shutdown			64		°C
T_{HYS}	Thermal shutdown hysteresis			26		°C
V_{FLT}	$\overline{FLT}$, $\overline{FLT1}$ low output voltage	$I_{\overline{FLT}}$ = 2.5 mA			0.5	V
V_{FLT}	$\overline{FLT2}$ low output voltage	$I_{\overline{FLT2}}$ = 2.5 mA			0.5	V
t_{FLT_DELAY}	Fault indication-time	V_{DIA_EN} = 5 V (for version A/B), EN = 5V Time between current limit fault and $\overline{FLT}$ or $\overline{FLT1}$ asserting			40	µs
t_{RETRY}	Retry time	Time from thermal shutdown until switch re-enable.	1	2	3	ms
EN PIN CHARACTERISTICS						
$V_{IL, EN}$	Input voltage low-level threshold				0.8	V
$V_{IH, EN}$	Input voltage high-level	No GND Network	1.5			V
$V_{IHYS, EN}$	Input voltage hysteresis			280		mV
R_{EN}	Internal pulldown resistor		200	350	500	kΩ
$I_{IL, EN}$	Input current low-level	V_{EN} = 0.8 V		2.5		µA
$I_{IH, EN}$	Input current high-level	V_{EN} = 5 V		16		µA
DIAG_EN/EN_AUX PIN CHARACTERISTICS						
V_{IL, EN_AUX}	Input voltage low-level	No GND Network			0.8	V
V_{IH, EN_AUX}	Input voltage high-level	No GND Network	1.5			V
V_{IHYS, EN_AUX}	Input voltage hysteresis			280		mV
R_{EN_AUX}	Internal pulldown resistor		200	350	500	kΩ
I_{IL, EN_AUX}	Input current low-level	V_{EN_AUX} = 0.8 V		2.5		µA
I_{IH, EN_AUX}	Input current high-level	V_{EN_AUX} = 5 V		16		µA

6.6 Switching Characteristics

V_{BB} = 13.5 V, T_J = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR_SLEEP}	Channel Turnon delay time (from Sleep)	V_{BB} = 13.5 V, R_L = 30 Ω 50% of EN to 10% of VOUT	28	40	44	µs
t_{DR_STBY}	Channel Turnon delay time (from Standby)	V_{BB} = 13.5 V, R_L = 30Ω 50% of EN to 10% of VOUT	5	20	40	µs
t_{DF}	Channel Turnoff delay time	V_{BB} = 13.5 V, R_L = 30 Ω 50% of EN to 90% of VOUT	20	40	60	µs
SR_R	VOUT rising slew rate	V_{BB} = 13.5 V, 20% to 80% of V_{OUT}, R_L = 30 Ω	0.13	0.3	0.5	V/µs
SR_F	VOUT falling slew rate	V_{BB} = 13.5 V, 80% to 20% of V_{OUT}, R_L = 30 Ω		0.2		V/µs
t_{ON}	Channel Turnon time	V_{BB} = 13.5 V, R_L = 30 Ω 50% of EN to 80% of VOUT	35	50	65	µs
t_{OFF}	ChannelTurnoff time	V_{BB} = 13.5 V, R_L = 30Ω 50% of EN to 20% of VOUT	50	75	110	µs

6.6 Switching Characteristics (continued)

V_{BB} = 13.5 V, T_J = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON} - t_{OFF}	Turnon and off matching	1ms enable pulse V_{BB} = 13.5 V, R_L = 30 Ω	–70		30	µs
		200-µs enable pulse, V_{BB} = 13.5 V, R_L = 30 Ω,	–30		30	µs
Δ_{PWM}	PWM accuracy - average load current	200-µs enable pulse (1ms period), V_{BB} = 13.5 V, R_L = 30 Ω	–15		25	%
Δ_{PWM}	PWM accuracy - average load current	≤500Hz, 50% Duty cycle V_{BB} = 13.5 V, R_L = 30 Ω	–10		10	%
E_{ON}	Switching energy losses during turnon	V_{BB} = 13.5 V, R_L = 30 Ω,		0.05		mJ
E_{OFF}	Switching energy losses during turnoff	V_{BB} = 13.5 V, R_L = 30 Ω,		0.05		mJ

6.7 Typical Characteristics

All the following data are based on the mean value of the three lots samples, VBB = 13.5 V if not specified.

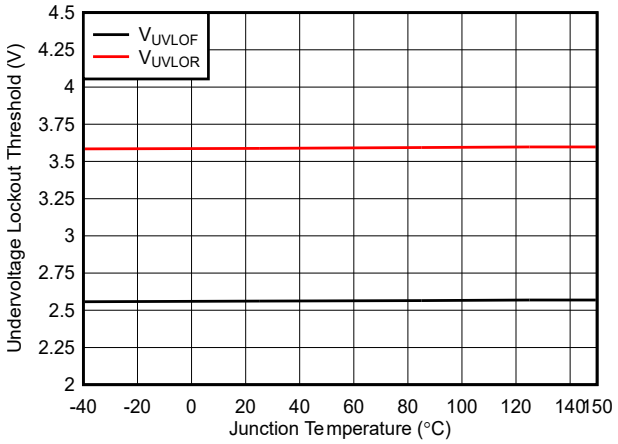


Figure 6-1. V_{UVLOR} and V_{UVLOF}

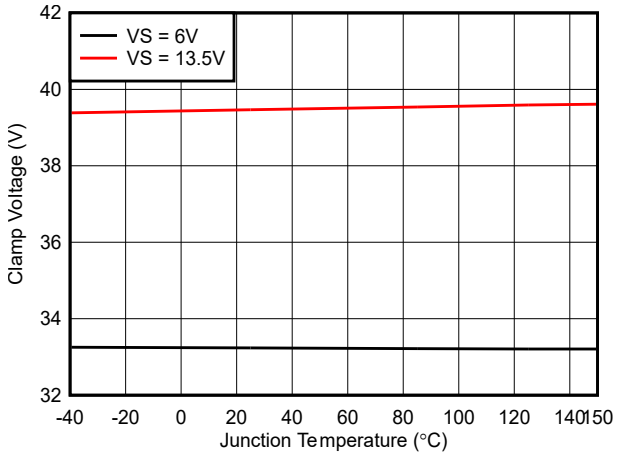


Figure 6-2. $V_{DS,clamp}$

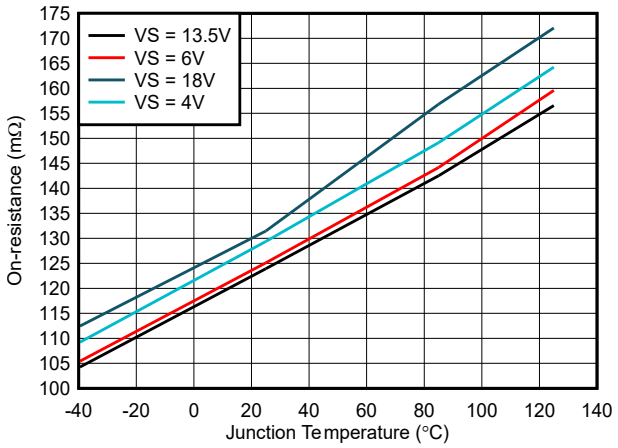


Figure 6-3. R_{ON} vs Temperature

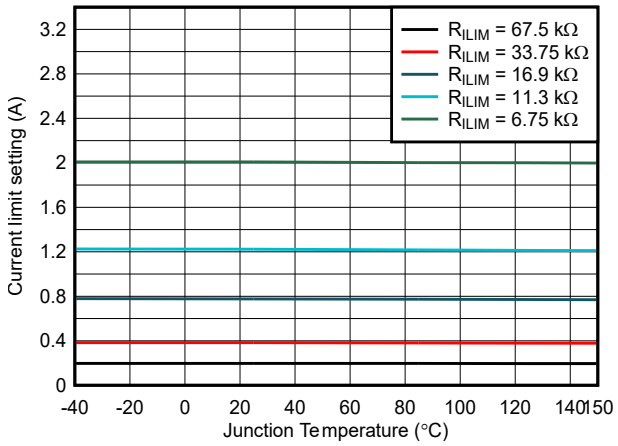


Figure 6-4. I_{CL}

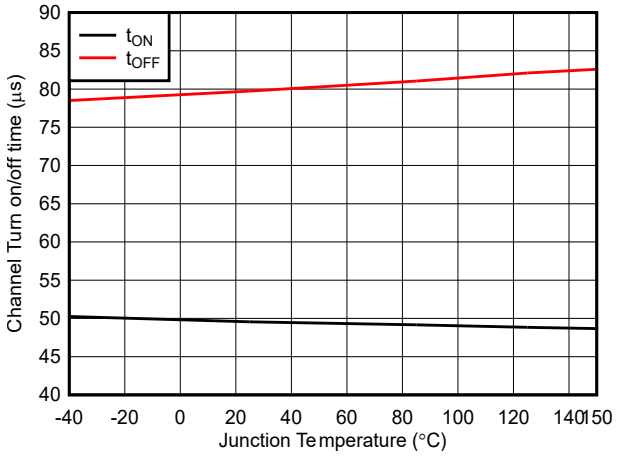


Figure 6-5. t_{ON} and t_{OFF}

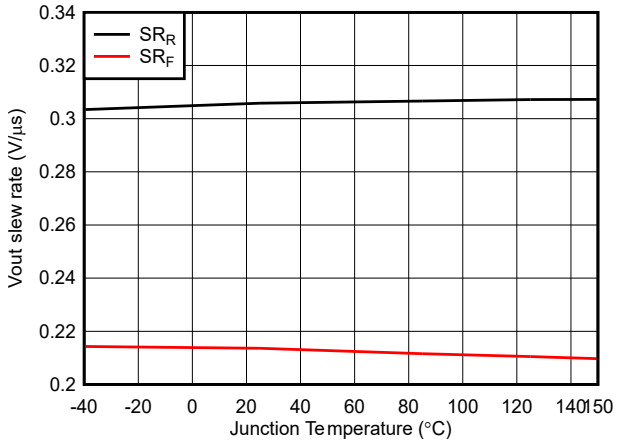


Figure 6-6. SR_R and SR_F

6.7 Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples, VBB = 13.5 V if not specified.

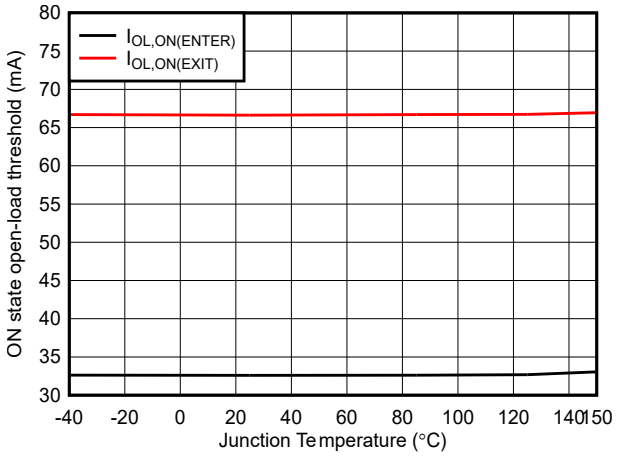


Figure 6-7. ON State Open-Load Entry/Exit Threshold

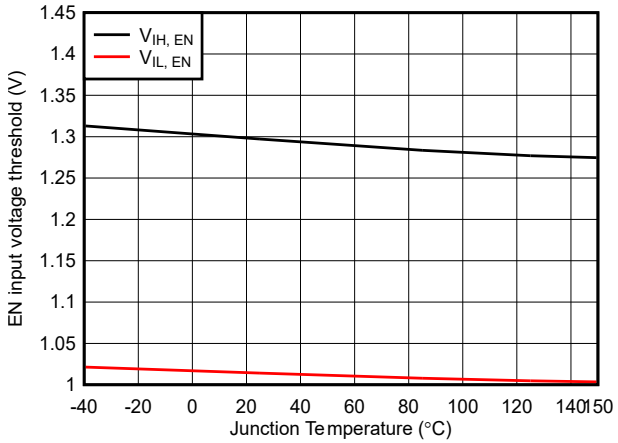


Figure 6-8. EN Input Voltage High/Low Level Thresholds

7 Detailed Description

7.1 Overview

The TPS1HC120-Q1 is a single-channel, fully-protected, high-side power switch with an integrated NMOS power FET and charge pump. Full diagnostics and high-accuracy current-sense (for A/B variants) features enable intelligent control of the load. Low logic high threshold, V_{IH}, of 1.5V on the input pins allow use of MCUs down to 1.8V. A programmable current-limit function greatly improves the reliability of the whole system. The device diagnostic reporting has two open-drain pins (FLT1, FLT2) to indicate both current limit, short-circuit and thermal shutdown faults or ON state open-load fault. When a fault condition occurs, the corresponding FLT pin is pulled down to GND. An external pullup is required to match the microcontroller supply level.

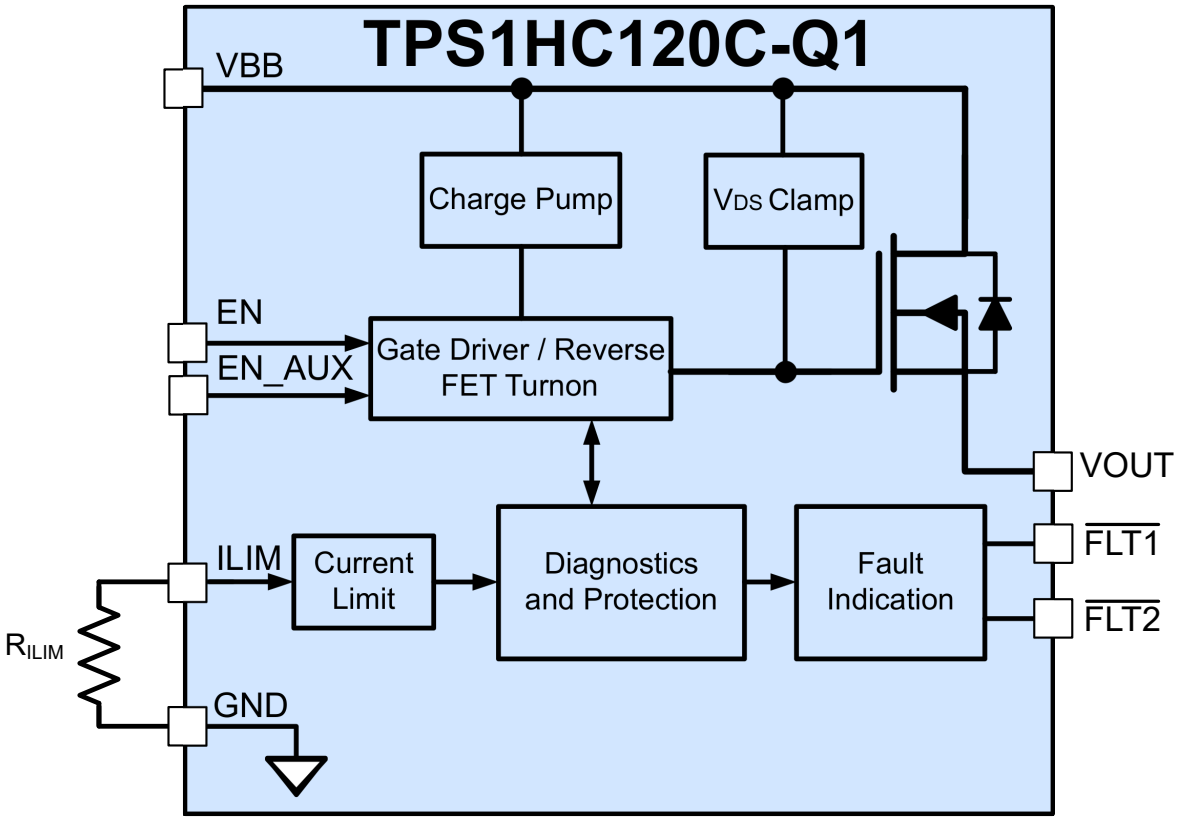
The high-accuracy current limit allows setting the current limit value by application. The current limit highly improves the reliability of the system by clamping the inrush current effectively under start-up or short-circuit conditions. Also, the current limit can save system costs by reducing PCB trace, connector size, and the preceding power-stage capacity. The current limit pin can also be kept open or shorted to ground to set a default current limit.

A drain to source voltage clamp is built in to dissipate the energy of inductive loads, such as relays, solenoids, pumps, motors, and so forth. During the inductive switching-off cycle, both the energy of the power supply and the load are dissipated on the high-side power switch itself. With the benefits of process technology and excellent IC layout, the TPS1HC120-Q1 device can achieve excellent power dissipation capacity, which can help save the external free-wheeling circuitry in most cases. For more details, see *Inductive-Load Switching-Off Clamp*.

Short-circuit reliability is critical for smart high-side power-switch devices. The standard of AEC-Q100-012 is to determine the reliability of the devices when operating in a continuous short-circuit condition. Different grade levels are specified according to the pass cycles. This device is qualified with the highest level, Grade A, 1 million times short-to-GND certification.

The TPS1HC120-Q1 device can be used as a high-side power switch for a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, and heaters.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 ORing of EN and EN_AUX

The EN and EN_AUX pins are internally OR'ed. So, the output channel will be enabled when either the EN or the EN_AUX pin voltage is above the logic high threshold.

Table 7-1. ORing of EN and EN_AUX

EN	EN_AUX	OUTPUT STATUS
$<V_{IL}$	$<V_{IL}$	Disabled
$<V_{IL}$	$>V_{IH}$	Enabled
$>V_{IH}$	$<V_{IL}$	Enabled
$>V_{IH}$	$>V_{IH}$	Enabled

Having two independent Enable pins can be useful in ADAS systems, where either the deserializer or the processor might need to wake-up the the high-side switch depending on the operating condition.

7.3.2 Inductive-Load Switching-Off Clamp

When an inductive load is switching off, the output voltage is pulled down to a negative value, due to the inductance characteristics. The power FET may break down if the voltage is not clamped during the current-decay period. To protect the power FET in this situation, the drain-to-source voltage is internally clamped to $V_{DS,clamp}$.

$$V_{DS,clamp} = V_{BAT} - V_{OUT} \quad (1)$$

During the current-decay period (T_{DECAY}), the power FET is turned on for inductance-energy dissipation. Both the energy of the power supply (E_{BAT}) and the load (E_{LOAD}) are dissipated on the high-side power switch itself, which is called E_{HSD}. If resistance is in series with inductance, some of the load energy is dissipated in the resistance.

$$E_{HSD} = E_{BAT} + E_{LOAD} = E_{BAT} + E_L - E_R \quad (2)$$

From the high-side power switch's view, E_{HSD} equals the integration value during the current-decay period.

$$E_{HSD} = \int_0^{T_{DECAY}} V_{DS,clamp} \times I_{OUT}(t)\,dt \quad (3)$$

$$T_{DECAY} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right) \quad (4)$$

$$E_{HSD} = L \times \frac{V_{BAT} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(MAX)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \quad (5)$$

When R approximately equals 0, E_{HSD} can be given simply as:

$$E_{HSD} = \frac{1}{2} \times L \times I^2_{OUT(MAX)} \frac{V_{BAT} + |V_{OUT}|}{R^2} \quad (6)$$

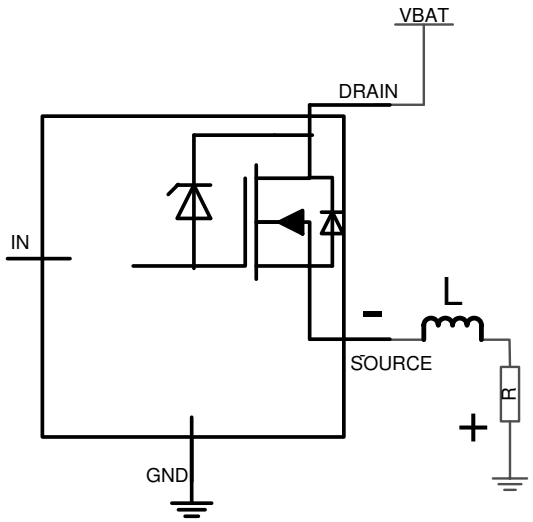


Figure 7-1. Driving Inductive Load

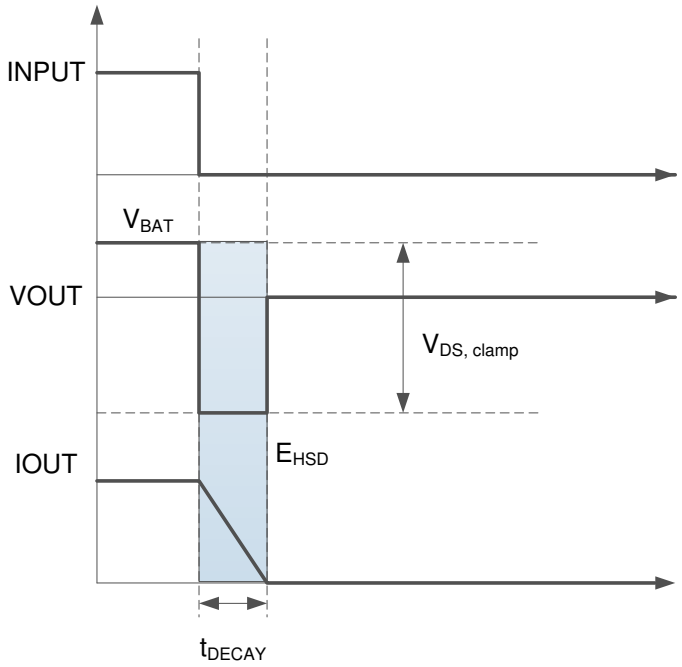


Figure 7-2. Inductive-Load Switching-Off Diagram

As discussed previously, when switching off, battery energy and load energy are dissipated on the high-side power switch, which leads to the large thermal variation. For each high-side power switch, the upper limit of the maximum safe power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

The plot below provides the upper limit of single-pulse energy that the device can tolerate under the test condition: VBB = 13.5V, inductance from 1.5mH to 100mH, R = 0Ω, FR4 2s2p board, 2- × 70µm copper, 2- × 35µm copper.

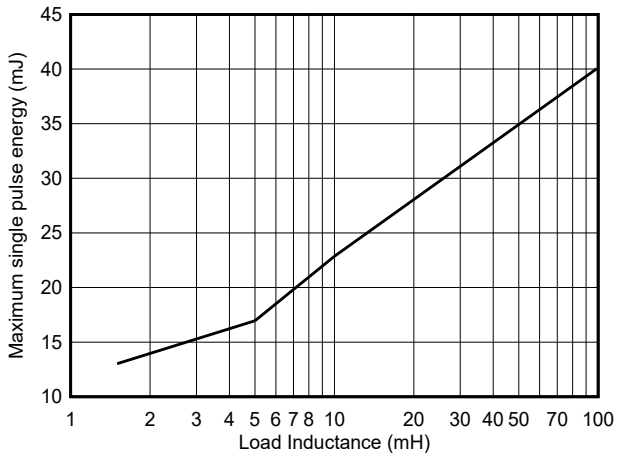


Figure 7-3. Maximum Single Pulse Energy vs Inductance Range

7.3.3 Full Protections and Diagnostics

Table 7-2. Fault Table

CONDITIONS	EN	VOUT	$\overline{FLT1}$	$\overline{FLT2}$	BEHAVIOR	RECOVERY
Normal	L	L	Hi-Z	Hi-Z	Normal	
	H	V_{BB} - I_{LOAD} × R_{ON}	Hi-Z	Hi-Z	Normal	
Overcurrent	H	I_{LIM} × R_{LOAD}	L	Hi-Z	Holds the current at the current limit until thermal shutdown or when the overcurrent event is removed	
Hard-short	H	L	L	Hi-Z	Shut off immediately and retry afterwards. Will latch-off after the first thermal shutdown event.	EN pins need to be toggled
Relative Thermal Shutdown, Absolute Thermal Shutdown	H	L	L	Hi-Z	Shuts down when devices hits relative or absolute thermal shutdown	Auto retries when T_{HYS} is met and it has been longer than t_{RETRY}
On-state Open load	H	H	Hi-Z	L	Indicate fault when load current is below $I_{OL,ON(ENTER)}$	When load current is above $I_{OL,ON(EXIT)}$
Reverse Polarity	x	x	x	x	Channel turns on to lower power dissipation. Current into ground pin is limited by external ground network.	

Table 7-3. Deglitch Time for Each Fault Condition

FAULT CONDITION	DETECTION DEGLITCH TIME
Current limit	5.6µs
Relative thermal shutdown	2.4µs
Absolute thermal shutdown	20µs

7.3.3.1 Programmable Current Limit

A high-accuracy current limit protects the power supply during short circuit or power up and allows higher reliability. Also, a current limit can save system costs by reducing PCB traces, connector size, and the capacity of the preceding power stage.

Current limit offers protection from over-stressing to the load and integrated power FET. Current limit holds the current at the set value, and asserts the $\overline{FLT1}$ pin as diagnostic reports. The pin is asserted when the current rises to the $I_{CL\_FLT1\_RISING}$ level.

The current-limit threshold can be set by either connecting a resistor from the ILIM pin to ground, or by floating the ILIM pin or by shorting the ILIM pin to ground.

- **External programmable current limit**: An external resistor, R_{ILIM}, is used to set the current limit. This value can be dynamically changed by changing the resistance. This information can be seen in the *Applications* section.
- **Internal current limit**: If the ILIM pin is shorted to ground or kept open, or the R_{ILIM} resistor is out of range (< 6.75kΩ or > 67.5kΩ), the internal current limit is fixed and typically 2.1A.

Current limit is active when V_{BB} is powered and EN or EN_AUX is high. Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the ILIM pin must be connected with device GND. Calculate R_{LIM} with Equation 2.

$$R_{LIM}\ (k\Omega) \approx 13.5 / I_{LIM}\ (A) \quad (7)$$

For more information about the current limiting feature, see the *Short-Circuit and Overload Protection* section.

7.3.3.2 Short-Circuit and Overload Protection

The TPS1HC120-Q1 provides output short-circuit protection to ensure that the device will prevent current flow in the event of a low impedance path to GND, removing the risk of damage or significant supply droop. The device is guaranteed to protect against short-circuit events up to 28V supply.

Figure 7-4 shows the behavior of the TPS1HC120-Q1 when the device is enabled into a short-circuit.

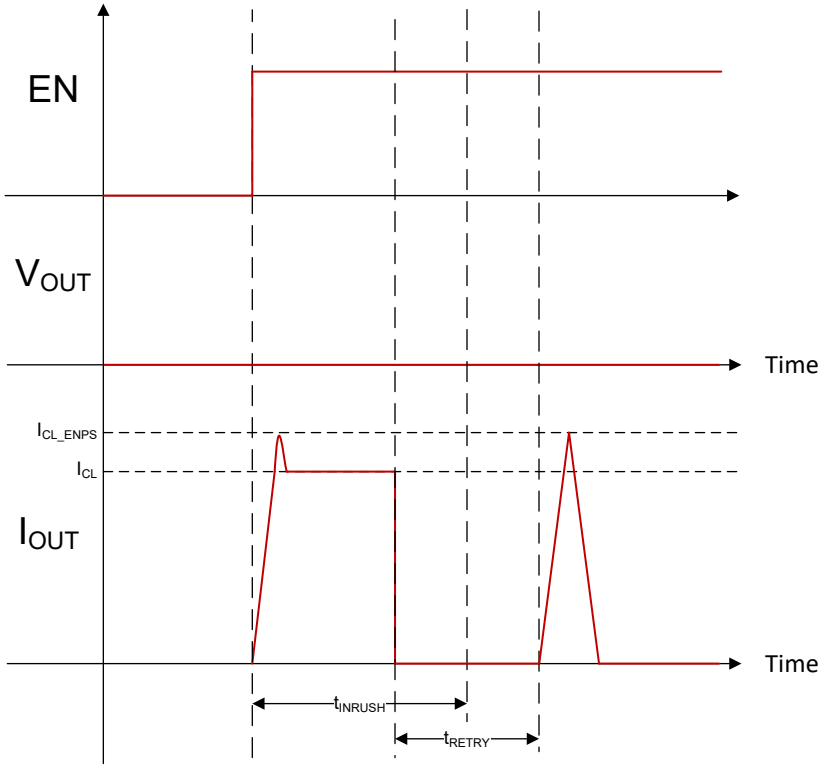


Figure 7-4. Enable Into Permanent Short

Once the device is enabled, due to the low impedance path, the output current will rapidly increase until it hits the current limit threshold (I_{CL}). Due to the response time of the current limiting circuit, the measured maximum current may temporarily exceed the I_{CL} value defined as I_{CL_ENPS}, however, it will settle to the current limit regulation value. In this state, high power is dissipated in the FET, so eventually the internal thermal protection temperature for the FET is reached and the device safely shuts down. After thermal shutdown,

- The device will retry after t_{RETRY} duration if the inrush period (t_{INRUSH}) has not expired. The inrush period starts from the EN rising edge.
- After the inrush period expires, output voltage (V_{OUT}) is sensed every time thermal shutdown is hit.
  - If V_{OUT} is less than 3V, as is the case for strong output short to ground, the device will be latched off until EN inputs toggle.
  - If V_{OUT} is higher than 3V, for example, for an overload scenario, the device will retry.

Figure 7-5 shows the behavior of the TPS1HC120-Q1 when a short-circuit occurs while the device is in the on-state and already delivering current. When the internal pass FET is fully enabled, the current limiting response time is slower. So to ensure that the current overshoot is limited, the device implements a fast trip at a level I_{OVCR}. When this fast trip threshold is hit, the device immediately shuts off for a short period of time before quickly re-enabling and clamping the current to I_{CL} level after a brief transient overshoot to the higher peak current (I_{CL_ENPS}) level. The device will then keep the current clamped at the regulation current limit until the thermal shutdown temperature is hit and the device will safely shut-off. Once thermal shutdown is hit, the device will latch off till the enable inputs toggle if the output voltage is less than 3V, and will retry if the output voltage is more than 3V.

Once the device re-enables due to enable input toggling, if the output short still exists, the scenario is identical to the enable into permanent short scenario.

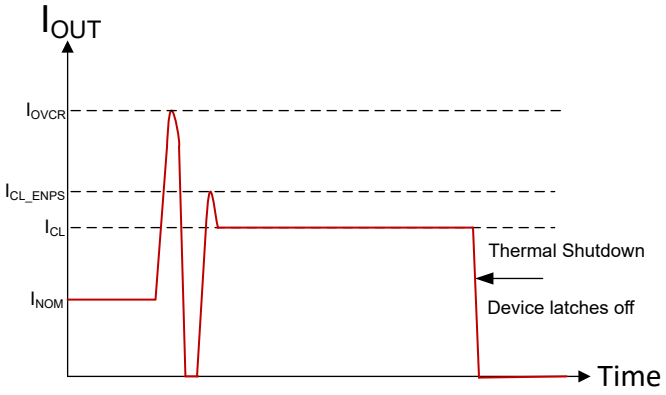


Figure 7-5. On-State Short-Circuit Behavior

Figure 7-6 shows the behavior of the TPS1HC120-Q1 when there is a small change in impedance that sends the load current above the I_{CL} threshold. The current rises to I_{CL_LINPK} above the regulation level. Then the current limit regulation loop kicks in and the current drops to the I_{CL} value.

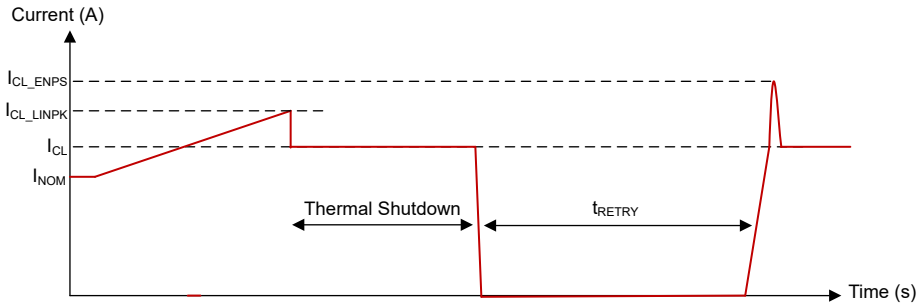


Figure 7-6. Overload Behavior

In all of these cases, the internal thermal shutdown is safe to hit repetitively. There is no device risk or lifetime reliability concerns from repeatedly hitting this thermal shutdown level.

7.3.3.2.1 Capacitive Charging

Figure 7-7 shows the typical set up for a capacitive load application and the internal blocks that function when the device is used. Note that all capacitive loads will have an associated "load" in parallel with the capacitor that is described as a resistive load but in reality it can be inductive or resistive.

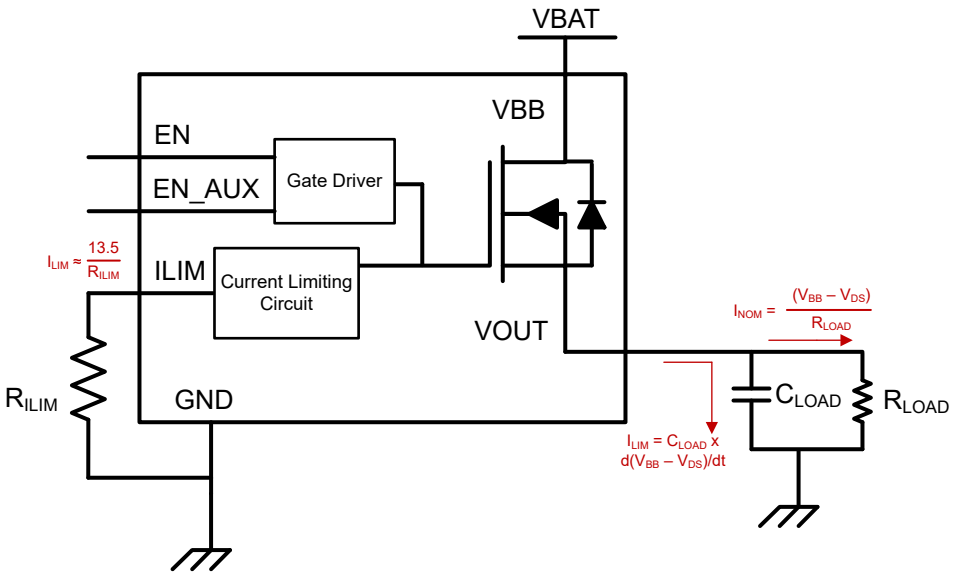


Figure 7-7. Capacitive Charging Circuit

The first thing to check is that the nominal DC current, I_{NOM}, is acceptable for the TPS1HC120-Q1 device. This can easily be done by calculating the junction temperature of the device. If that value is below the thermal shutdown value, the device can operate with that I_{NOM}. For an example of this calculation see the *Applications* section.

The second key care about for this application is to make sure that the capacitive load can be charged up completely without the device hitting thermal shutdown. The reason is because if the device hits thermal shutdown during the charging, the resistive nature of the load in parallel with the capacitor will start to discharge the capacitor over the duration the TPS1HC120-Q1 is off. Note that there are some application with high enough load impedance that the TPS1HC120-Q1 hitting thermal shutdown and trying again is acceptable; however, for the majority of applications, the system should be designed so that the TPS1HC120-Q1 does not hit thermal shutdown while charging the capacitor.

With the current limiting feature of the TPS1HC120-Q1, capacitors can be charged up at a lower inrush current than other high current limit switches. This lower inrush current means that the capacitor will take a little longer to charge all the way up. The time that it takes to charge up will follow the equation below.

$$I_{LIM} = C \times d(V_{BB} - V_{DS})/dt \quad (8)$$

However, since the V_{DS} for a typical 1A applications is much less than the V_{BB} voltage ($V_{DS} \approx 1A \times 0.12\Omega = 120mV$, $V_{BB} \approx 13.5V$), the equation can be rewritten and approximated as

$$dt = C \times dV_{BB} / I_{LIM} \quad (9)$$

This charge timing is pictured in Figure 7-8.

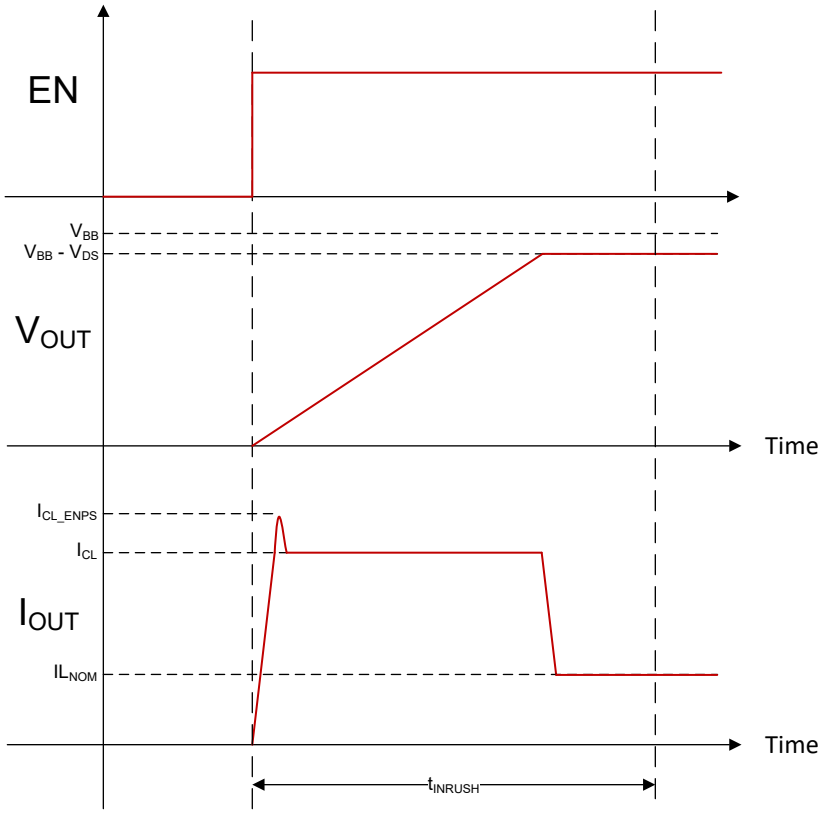


Figure 7-8. Capacitive Charging Timing

For more information about capacitive charging with high side switches, see the *How to Drive Capacitive Loads Application Note*. This application note has information about the thermal modeling available along with quick ways to estimate if a high side switch will be able to charge a capacitor to a given voltage.

7.3.3.3 On-state Open-Load Detection

When the output FET is enabled, if the current through the FET drops below $I_{OL,ON(ENTER)}$, open-load is detected and $\overline{FLT2}$ pin is pulled low. When the current goes above the $I_{OL,ON(EXIT)}$ threshold, $\overline{FLT2}$ pin is released.

7.3.3.4 Reverse-Polarity and Reverse Battery Protection

Reverse-polarity, commonly referred to as reverse battery, occurs when the ground of the device goes to the battery potential, $V_{GND} = V_{BAT}$, and the supply pin goes to ground, V_{BB} = 0V. In this case, if the EN pin has a path to the "ground" plane, then the FET will turn on (with on-resistance $R_{ON(REV)}$)to lower the power dissipation through the main channel and prevent current flow through the body diode. It is important to note that the resistor/diode ground network (if there is not a central blocking diode on the supply) must be present for the device to protect itself during a reverse battery event.

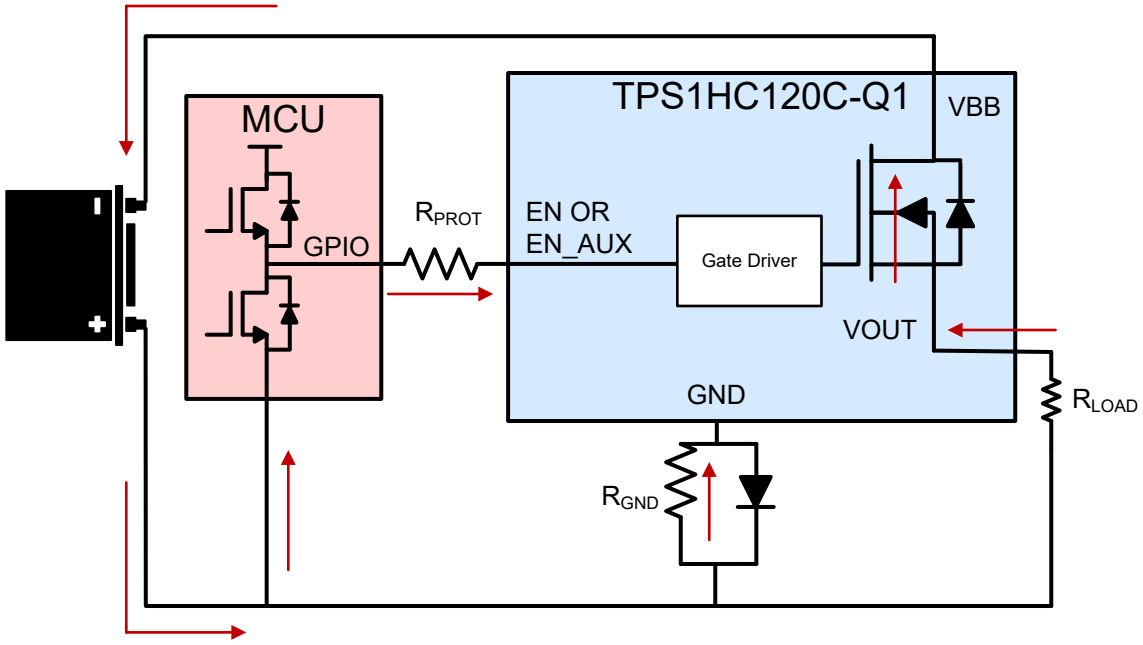


Figure 7-9. Reverse Battery Circuit

For more external protection circuitry information, see *Reverse Current Protection*. See the fault truth table for more details.

7.3.3.5 Thermal Protection Behavior

The thermal protection behavior can be either relative thermal shutdown or absolute thermal shutdown, as explained below -

1. **Relative thermal shutdown**: The device is enabled into an over current event. The output current rises up to the I_{ILIM} level and the FLT1 goes low. With this large amount of current going through, the junction temperature of the FET increases rapidly with respect to the controller temperature. When the power FET temperature rises T_{REL} amount above the controller junction temperature ($\Delta T = T_{FET} - T_{CON} > T_{REL}$), the device shuts down. Once thermal shutdown is hit,
   a. The device will latch off till the enable inputs toggle if the output voltage is less than 3V.
   b. Will retry if the output voltage is more than 3V.
2. **Absolute thermal shutdown**: The device is still enabled in an over current event. However, in this case the junction temperature rises up and hits an absolute reference temperature, T_{ABS}, and then shuts down. Once thermal shutdown is hit,
   a. The device will latch off till the enable inputs toggle if the output voltage is less than 3V.
   b. Will retry once both $T_J < T_{ABS} - T_{hys}$ and the t_{RETRY} timer has expired, if the output voltage is more than 3V.

7.3.3.6 UVLO Protection

The device monitors the supply voltage VBB to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to V_{UVLOF}, the output stage is shut down automatically. When the supply rises up to V_{UVLOR}, the device turns on.

If an overcurrent event trips the UVLO threshold, the device will shut off and come back on into a current limit safely.

7.3.3.7 Loss of GND Protection

When loss of GND occurs, output is turned off regardless of whether the input signal is high or low.

Case 1 (loss of Device GND): Loss of GND protection is active when the I_{C_GND}, and current limit ground are one trace connected to the system ground, as shown in Figure 7-10.

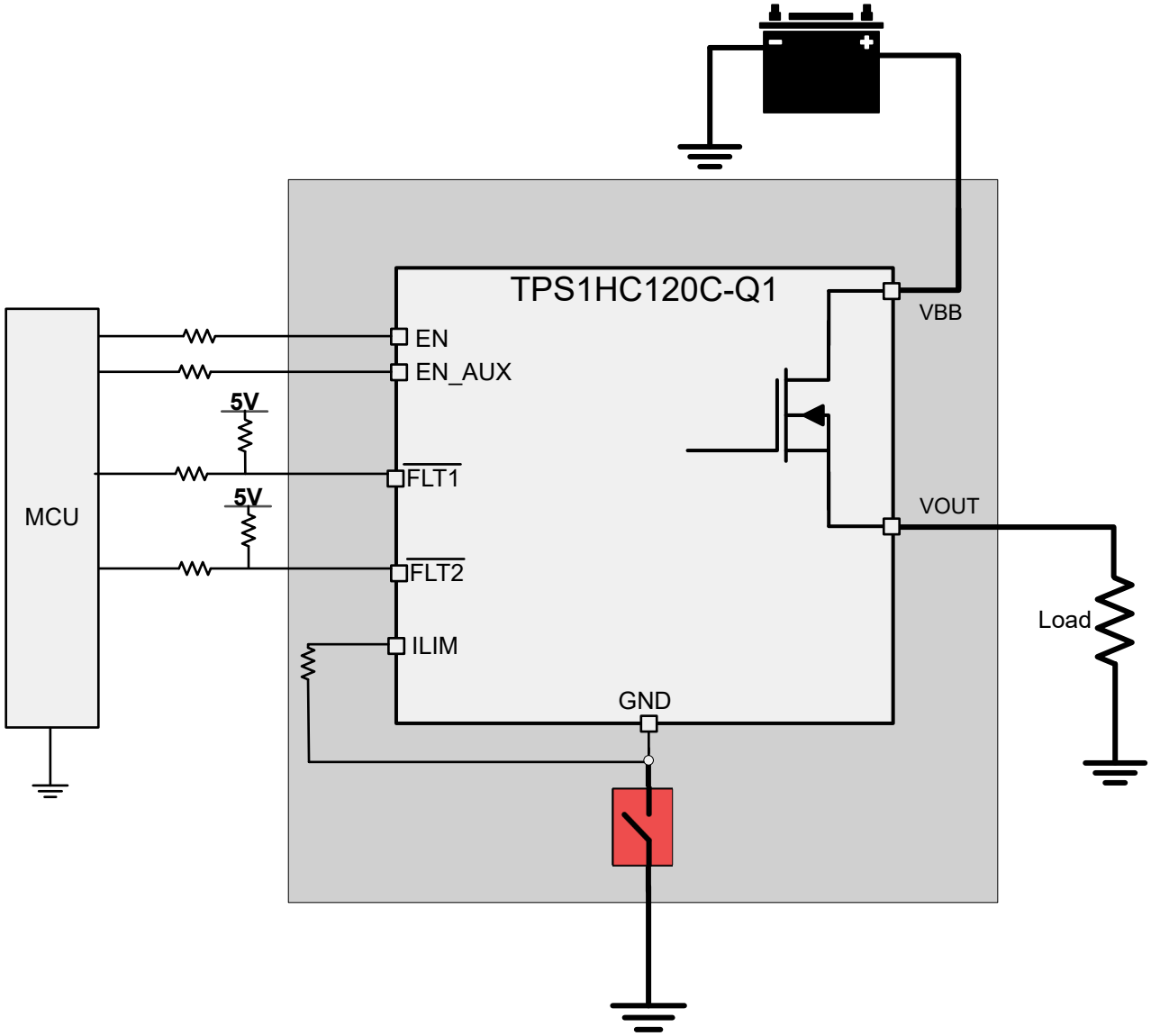


Figure 7-10. Loss of Device GND

Case 2 (loss of Module GND): When the whole ECU module GND is lost, protections are also active. At this condition, the load GND remains connected.

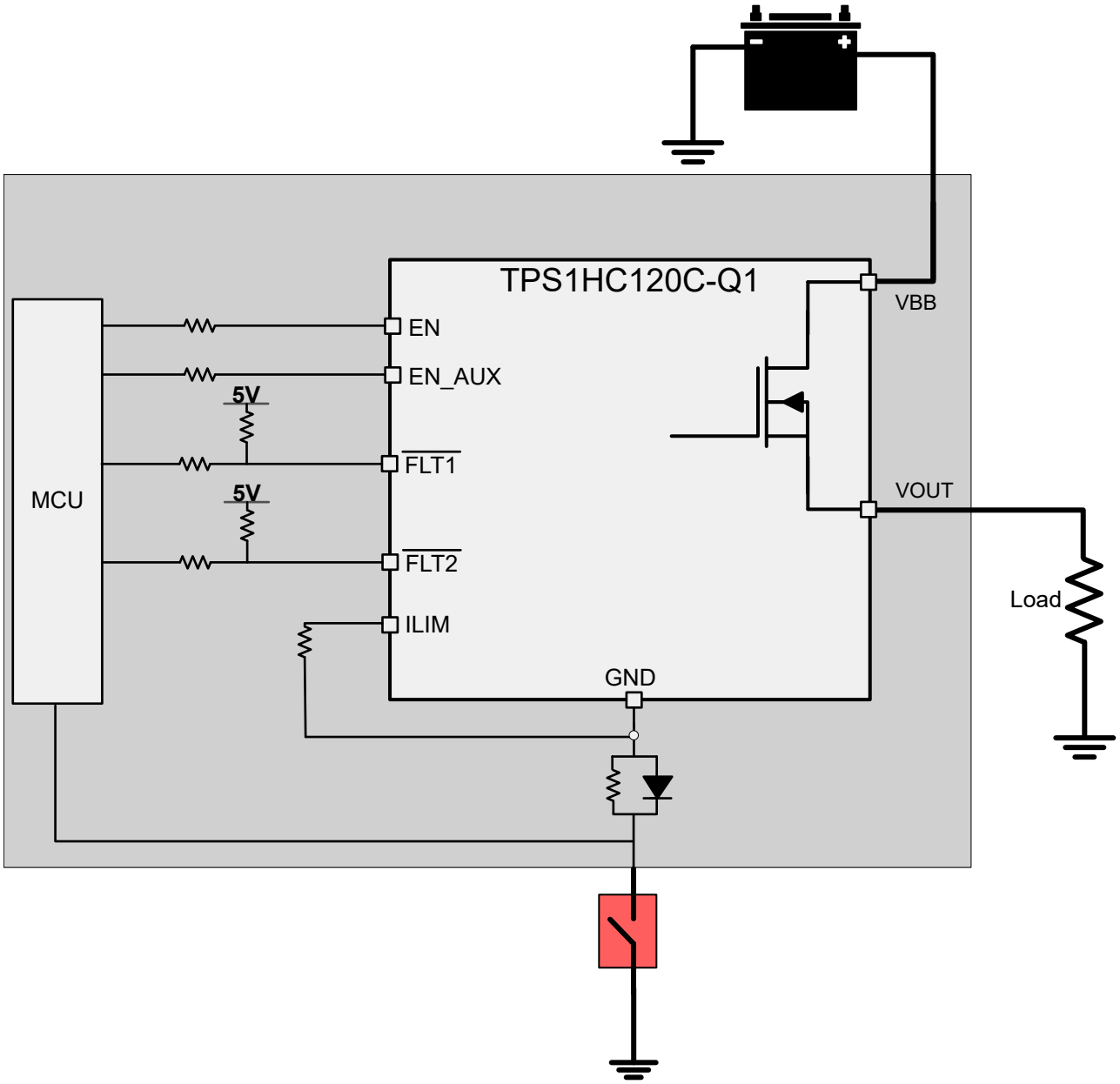


Figure 7-11. Loss of Module GND

7.3.3.8 Loss of Power Supply Protection

When loss of supply occurs, output is turned off regardless of whether the input is high or low. For a resistive or capacitive load, loss of supply protection is easy to achieve due to no more power. The worst case is a charged inductive load. In this case, the current is driven from all of the IOs to maintain the inductance output loop. TI recommends either the MCU serial resistor plus the GND network (diode and resistor in parallel) or external free-wheeling circuitry.

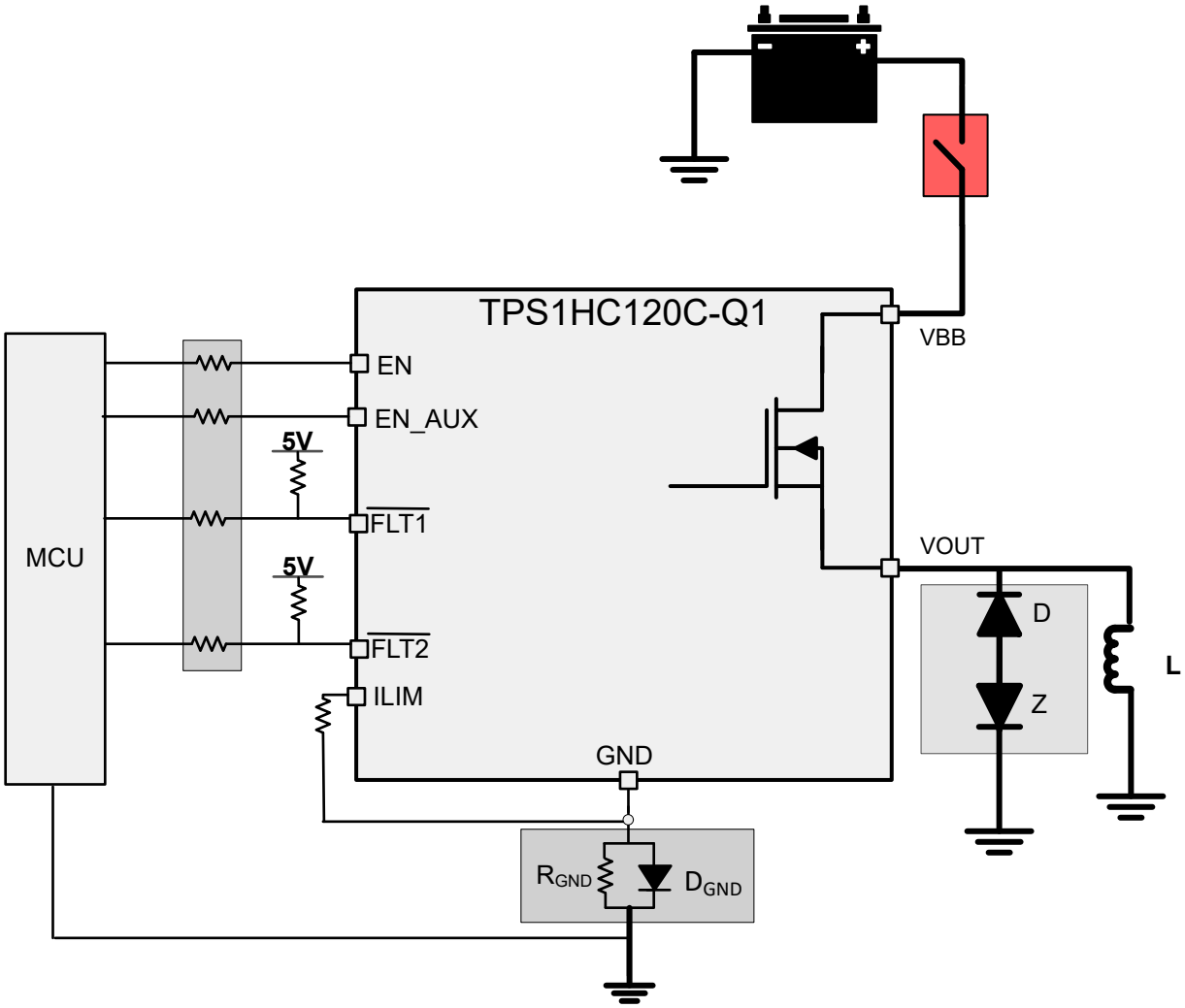


Figure 7-12. Loss of Battery

7.3.3.9 Reverse Current Protection

Method 1: Block diode connected with V_{BB}. Both the device and load are protected when in reverse polarity. The blocking diode does not allow any of the current to flow during reverse battery condition.

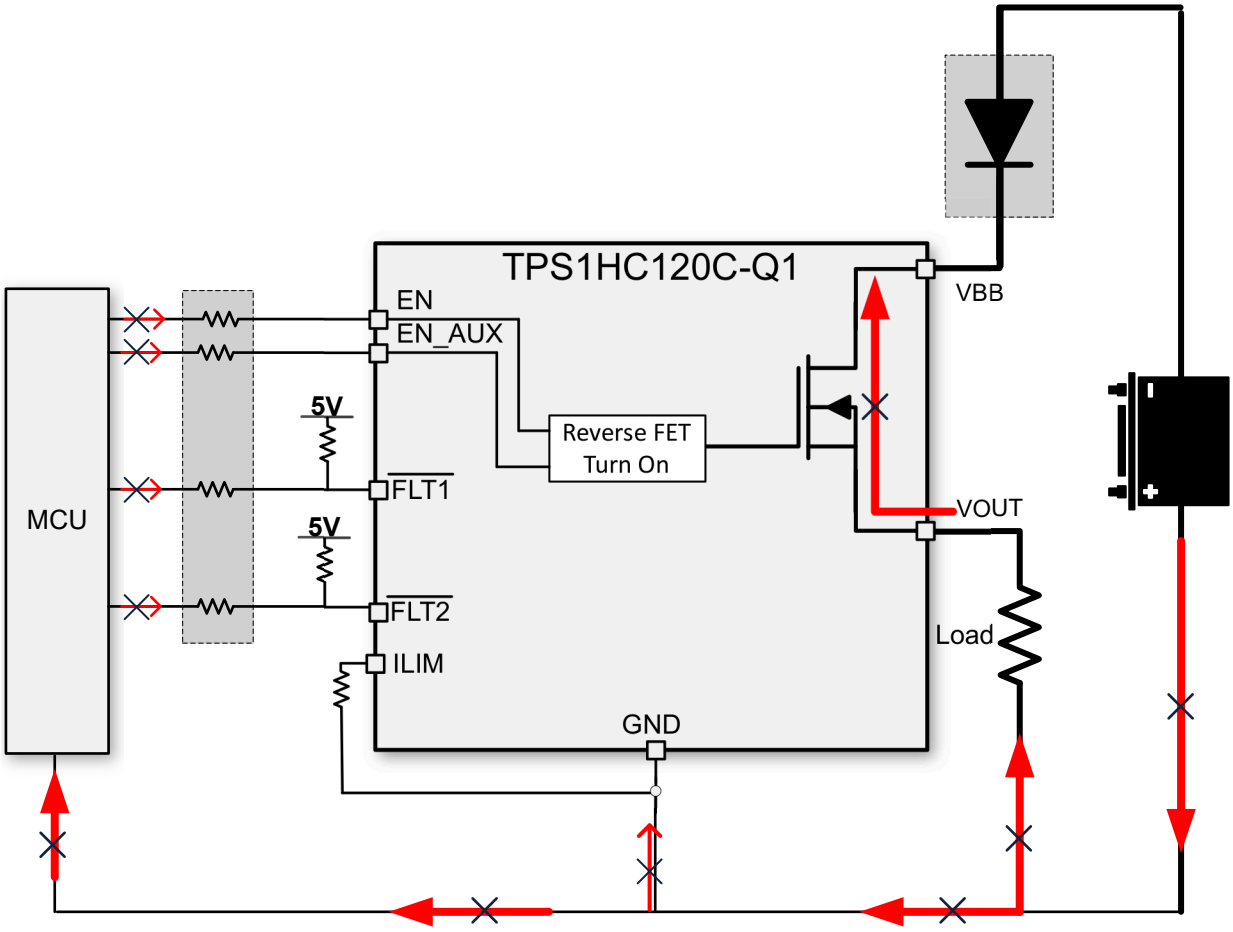


Figure 7-13. Reverse Protection With Block Diode

Method 2 (GND network protection): Only the high-side device is protected under this connection. The load reverse current is limited by the impedance of the load itself. Note when reverse polarity happens, the continuous reverse current through the power FET should not make the heat build up be greater than the absolute maximum junction temperature. This can be calculated using the $R_{ON(REV)}$ value and the $R_{\theta JA}$ specification. No matter what types of connection are between the device GND and the board GND, if a GND voltage shift happens, ensure the following proper connections for the normal operation:

- Connect the current limit programmable resistor to the device GND.

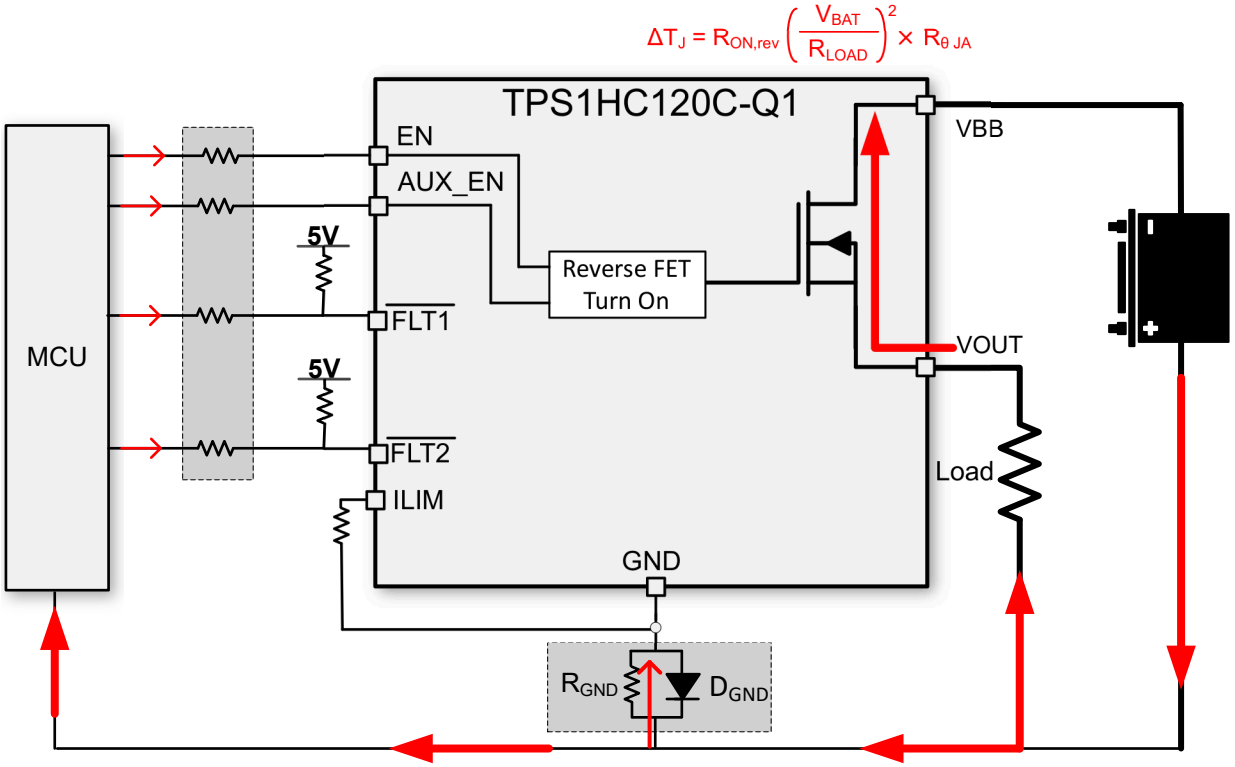


Figure 7-14. Reverse Protection With GND Network

- **Recommendation - Resistor and Diode in Parallel:** A peak negative spike may occur when the inductive load is switching off, which may damage the HSD or the diode. So, TI recommends a resistor in parallel with the diode when driving an inductive load. The recommended selection are a 1kΩ resistor in parallel with an I_F > 100mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices.
  - **Ground Resistor:** The higher resistor value contributes to a better current limit effect when the reverse battery or negative ISO pulses.

$$R_{GND} \geq \frac{(-V_{CC})}{(-I_{GND})} \tag{10}$$

where

- $-V_{CC}$ is the maximum reverse battery voltage (typically –16V).
- $-I_{GND}$ is the maximum reverse current the ground pin can withstand, which is available in the *Absolute Maximum Ratings*.

  - **Ground Diode:** A diode is needed to block the reverse voltage, which also brings a ground shift (≈ 600mV). Additionally, the diode should be ≈ 200V reverse voltage for the ISO 7637 pulse 1 testing so that it does not get biased.

7.3.3.10 Protection for MCU I/Os

In many conditions, such as the negative ISO pulse, or the loss of battery with an inductive load, a negative potential on the device GND pin may damage the MCU I/O pins (more likely, the internal circuitry connected to the pins). Therefore, the serial resistors between MCU and HSS are required.

Also, for proper protection against loss of GND, TI recommends 10kΩ resistance for the R_{PROT} resistors.

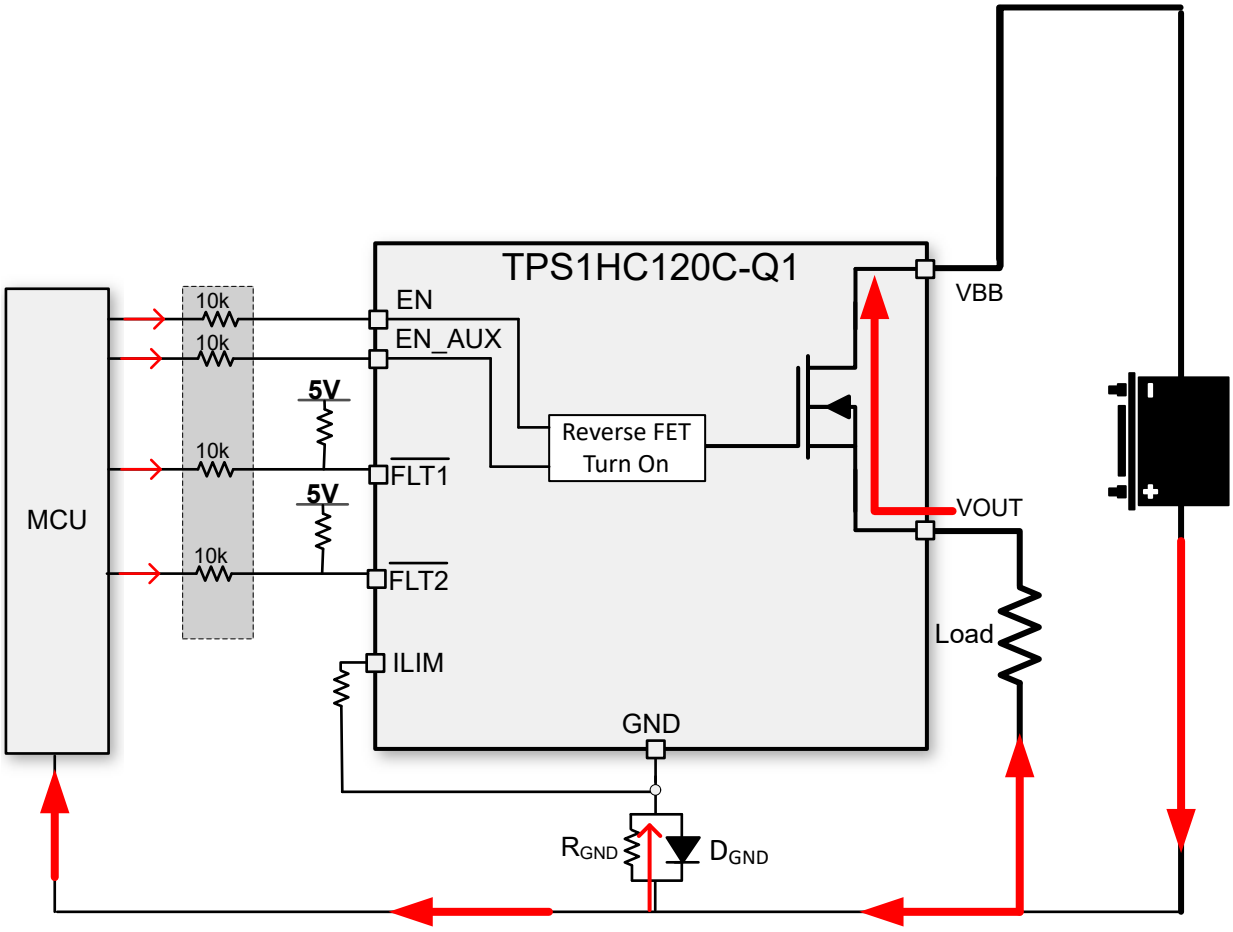


Figure 7-15. MCU I/O Protections

7.4 Device Functional Modes

7.4.1 Working Mode

The three working modes in the device are normal mode, standby mode and sleep mode.

The device can enter standby mode from normal mode when EN is made logic-low. In standby or sleep mode, off-state power saving is supported by the ultra-low standby current $I_{VBB,SLEEP}$ (less than 500nA at 85 °C). Note that to enter sleep mode requires EN low and t > t_{STBY}. t_{STBY} is the standby-mode deglitch time, which is used to avoid false triggering or interfering with PWM switching. Figure 7-16 shows the working-mode state-machine state diagram.

The time taken to turn on the output is longer when the device is in sleep mode (t_{DR_SLEEP}) compared to when the device is in standby mode (t_{DR_STBY}).

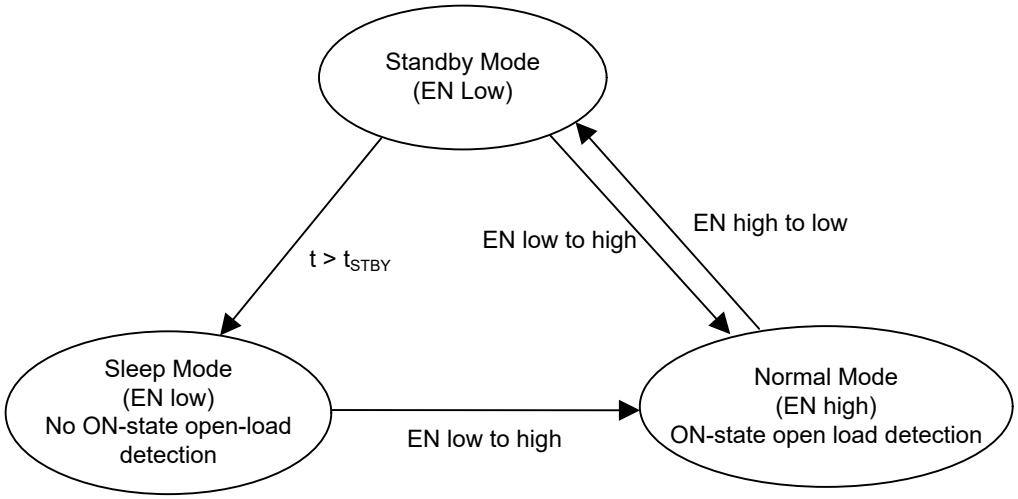


Figure 7-16. Work-Mode State Machine

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS1HC120-Q1 is capable of driving a wide variety of resistive, inductive, and capacitive loads, including ADAS cameras, LEDs, relays, solenoids, heaters, and sub-modules. Full diagnostics enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

8.2 Typical Application

Figure 8-1 shows an example of how to design the external circuit.

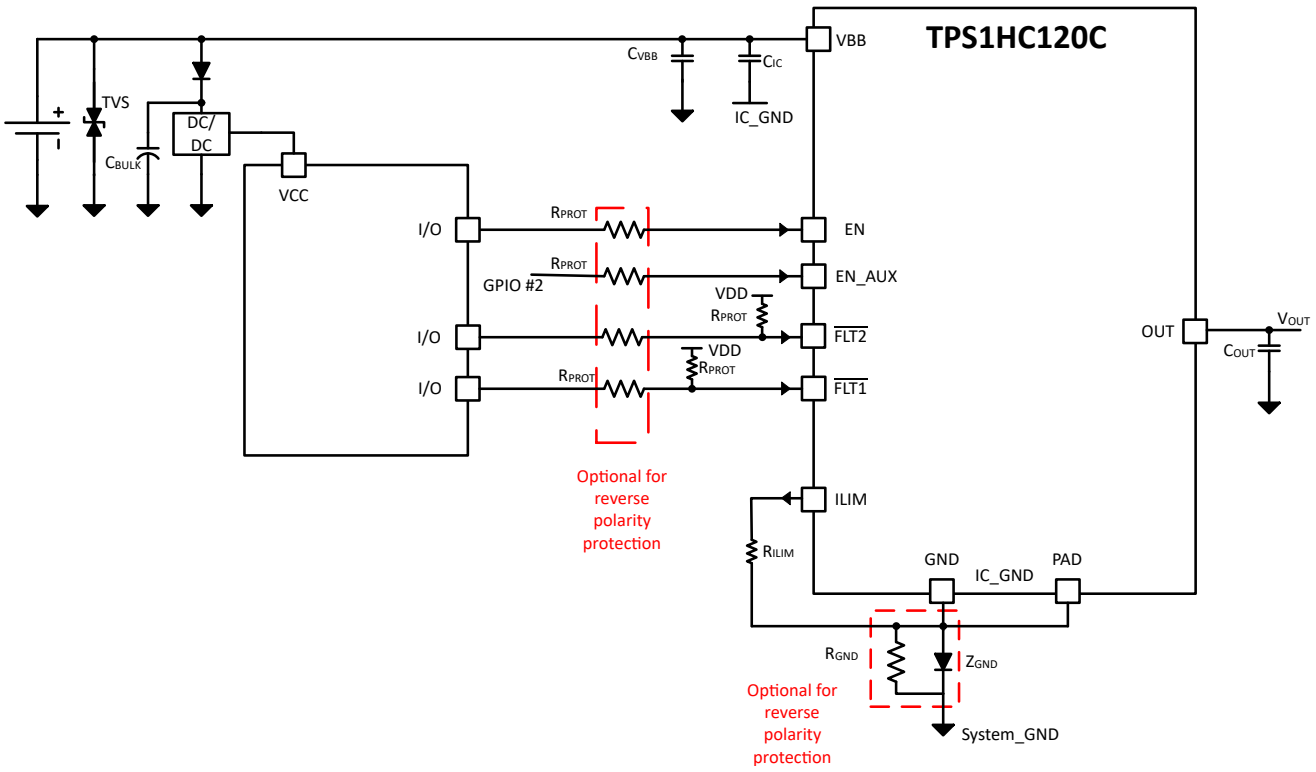


Figure 8-1. Typical Application Circuitry

Table 8-1. Recommended Component Values

COMPONENT	DESCRIPTION	PURPOSE
TVS	SMBJ39CA (optional)	Filter voltage transients coming from battery (ISO7637-2)
C_{VBB}	220nF (optional)	Better EMI performance
C_{IC}	100nF	Minimal amount of capacitance on input for EMI mitigation
C_{BULK}	10µF (optional)	Help filter voltage transients on the supply rail
R_{PROT}	10kΩ	Protection resistor for microcontroller and device I/O pins

Table 8-1. Recommended Component Values (continued)

COMPONENT	DESCRIPTION	PURPOSE
R_{ILIM}	Follow the recommendation in Specifications	Set current limit threshold
C_{VOUT}	22nF	Improves EMI performance, filtering of voltage transients
R_{PU}	4.7kΩ	Pull up resistor for open-drain pins ($\overline{FLT1}$ and $\overline{FLT2}$)
R_{GND}	1kΩ	Stabilize GND potential during turn-off of inductive load
D_{GND}	BAS21 Diode	Keeps GND close to system ground during normal operation

8.2.1 Detailed Design Procedure

8.2.1.1 Dynamically Changing Current Limit

The current limit threshold is able to be changed dynamically by altering the resistance going from the current limit pin to the ground of the device on the fly.

8.2.1.2 AEC Q100-012 Test Grade A Certification

Short-circuit reliability is critical for smart high-side power switch devices. The AEC-Q100-012 standard is used to determine the reliability of the devices when operating in a continuous short-circuit condition. Different grade levels are specified according to the pass cycles. The TPS1HC120-Q1 is qualified with the highest level, Grade A (1 million times short-to-GND).

Three test modes are defined in the AEC Q100-012 standard. See Table 8-2 for cold repetitive short-circuit test – long pulse, cold repetitive short-circuit test – short pulse, and hot repetitive short-circuit test. Hot repetitive short-circuit with continuous output short does not apply to this device, because the output latches off.

Table 8-2. Tests

TEST ITEMS	TEST CONDITION	TEST CYCLES
Cold repetitive short-circuit test – short pulse	–40°C, 10ms pulse, cool down	1M
	85°C, 10ms pulse, cool down	1M
Cold repetitive short-circuit test – long pulse	–40°C, 300ms pulse, cool down	1M
Hot repetitive short-circuit test	85°C, weak overload	1M
Cold repetitive short-circuit test	-40°C, terminal short	1M

Different grade levels are specified according to the pass cycles, as shown below -

Table 8-3. Grade Levels

GRADE	NUMBER OF CYCLES	LOTS,SAMPLES PER LOT	NUMBER OF FAILS
A	>1000000	3, 10	0
B	>300000 to 1000000	3, 10	0
C	>100000 to 300000	3, 10	0
D	>30000 to 100000	3, 10	0
E	>10000 to 30000	3, 10	0
F	>3000 to 10000	3, 10	0
G	>1000 to 3000	3, 10	0
H	300 to 1000	3, 10	0
O	<300	3, 10	0

8.2.1.3 EMC Transient Disturbances Test

Due to the severe electrical conditions in the automotive environment, immunity capacity against electrical transient disturbances is required, especially for a high-side power switch, which is connected directly to the battery. Detailed test requirements are in accordance with the ISO 7637-2:2011 and ISO 16750-2:2010 standards. The TPS1HC120-Q1 test summary is shown below -

Table 8-4. ISO 7637-2:2011(E) in 12V System (1) (2) (3) (4)

Test Item	Test Pulse Severity Level and vs Accordingly		Pulse Duration (t_d)	Minimum Number of Pulses or Test Time	Burst-Cycle Pulse-Repetition Time		Input Resistance (Ω)	Function Performance Status Classification
	Level	VBB/V			MIN	MAX		
1	III	–112	2ms	500 pulses	0.5s	-	10	Status II
2a	III	55	50µs	500 pulses	0.2s	5s	2	Status II
2b	IV	10	0.2s to 2s	10 pulses	0.5s	5s	0 to 0.05	Status II
3a	IV	–220	0.1µs	1h	90ms	100ms	50	Status II
3b	IV	150	0.1µs	1h	90ms	100ms	50	Status II

(1) Tested both under input low condition and high condition.
(2) Considering the worst test condition, it is tested without any filter capacitors on VBB and V_{OUT}.
(3) GND pin network is a 1kΩ resistor in parallel with a diode BAS21-7-F.
(4) Status II: The function does not perform as designed during the test, but returns automatically to normal operation after the test.

Table 8-5. ISO 16750-2:2010(E) Load Dump Test B in 12V System (1) (2) (3) (4) (5)

TEST ITEM	TEST PULSE SEVERITY LEVEL AND VS ACCORDINGLY		PULSE DURATION (t_d)	MINIMUM NUMBER OF PULSES OR TEST TIME	BURST CYCLE/PULSE REPETITION TIME	INPUT RESISTANCE (Ω)	FUNCTION PERFORMANCE STATUS CLASSIFICATION
	LEVEL	VBB/V					
Test B	N/A	35	40ms to 400ms	5 pulses	60s	0.5 to 4	Status II

(1) Tested both under input low condition and high condition.
(2) Considering the worst test condition, the device is tested without any filter capacitors on VBB and V_{OUT}.
(3) The GND pin network is a 1kΩ resistor in parallel with a diode BAS21-7-F.
(4) Status II: The function does not perform as designed during the test, but returns automatically to normal operation after the test.
(5) Select a 39V external suppressor.

8.2.2 Power Dissipation Calculation

For continuous normal operation, the junction temperature should not exceed the thermal-shutdown trip point. Calculate the power dissipated by the device according to Equation 13.

$$P_T = (I_{OUT}{}^2 \times R_{ON}) + (V_{BB} \times I_Q) \quad (11)$$

where P_T is the total power dissipation of the device.

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + R_{\theta JA} \times P_T \quad (12)$$

The R_{ON} has to be extrapolated to correspond to the junction temperature of the device, so multiple iterations of the above calculation might be needed to arrive at the junction temperature estimate of the device.

For more information, please see the *How to Drive Resistive, Inductive, Capacitive, and Lighting Loads Application Note*.

8.2.3 Application Curves

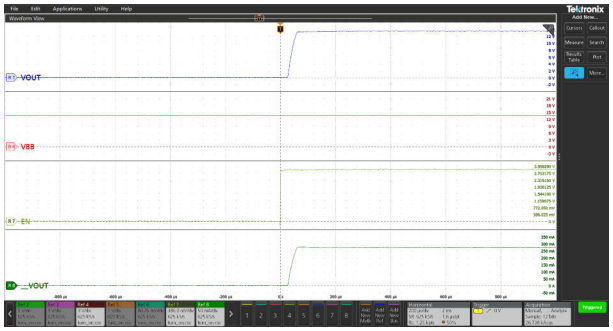


Figure 8-2. Output Turn-On At 13.5V, 50Ω Resistive Load On Output

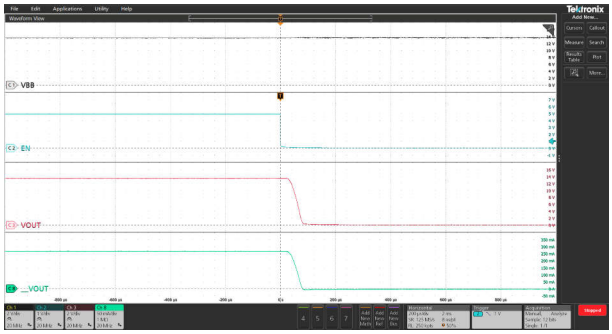


Figure 8-3. Output Turn-Off At 13.5V, 50Ω Resistive Load On Output

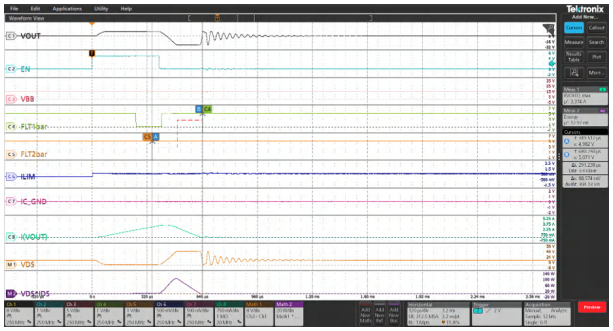


Figure 8-4. Turning-Off 5mH Inductive Load At 13.5V

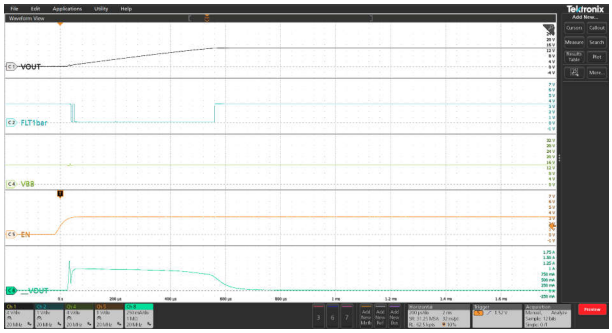


Figure 8-5. Charging 40µF Capacitor With 1A Current Limit At 125°C

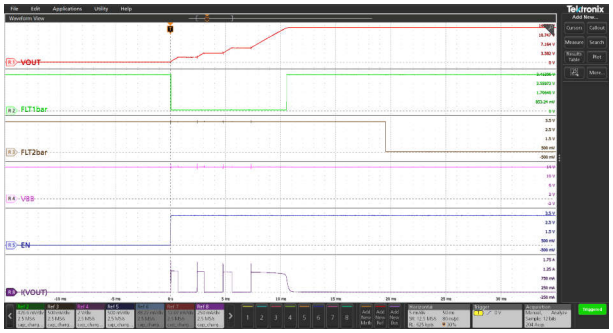


Figure 8-6. Charging 220µF Capacitor With 1A Current ILmit At 125°C

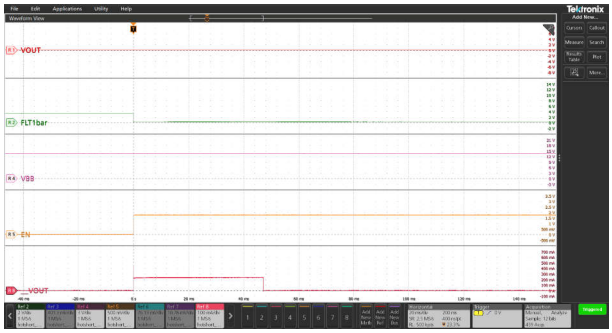


Figure 8-7. Output Hot-Short With 200mA Current Limit

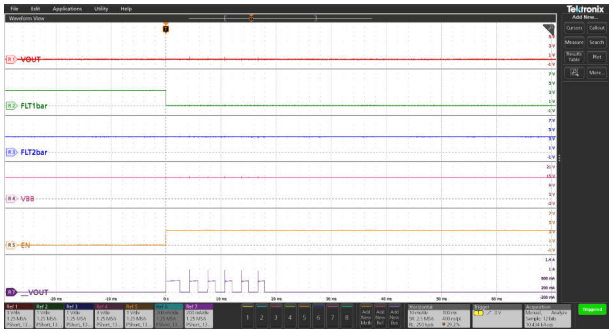


Figure 8-8. Output Short-To-Ground With 400mA Current Limit

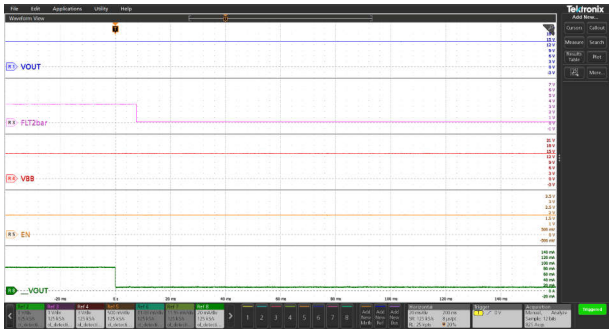


Figure 8-9. On-State Open-Load Detection

8.3 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 12V automotive system. The supply voltage should be within the range specified in the *Recommended Operating Conditions*.

Table 8-6. Voltage Operating Ranges

VBB VOLTAGE RANGE	NOTE
3V to 6V	Extended lower 12V automotive battery operation such as cold crank and start-stop. Device is fully functional and protected but some parametrics such as R_{ON}, current limit accuracy and timing parameters can deviate from specifications. Check the individual specifications in Electrical Characteristics to confirm the voltage range it is applicable for.
6V to 18V	Nominal 12V automotive battery voltage range. All parametric specifications apply and the device is fully functional and protected.
18V to 24V	Extended upper 12V automotive battery operation such as double battery. Device is fully functional and protected but some parametrics such as R_{ON}, current limit accuracy, and timing parameters can deviate from specifications. Check the individual specifications in Electrical Characteristics to confirm the voltage range it is applicable for.
35V	Load dump voltage. Device is operational and lets the pulse pass through without being damaged but does not protect against short circuits.

8.4 Layout

8.4.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. If the output current is very high, the power dissipation may be large. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

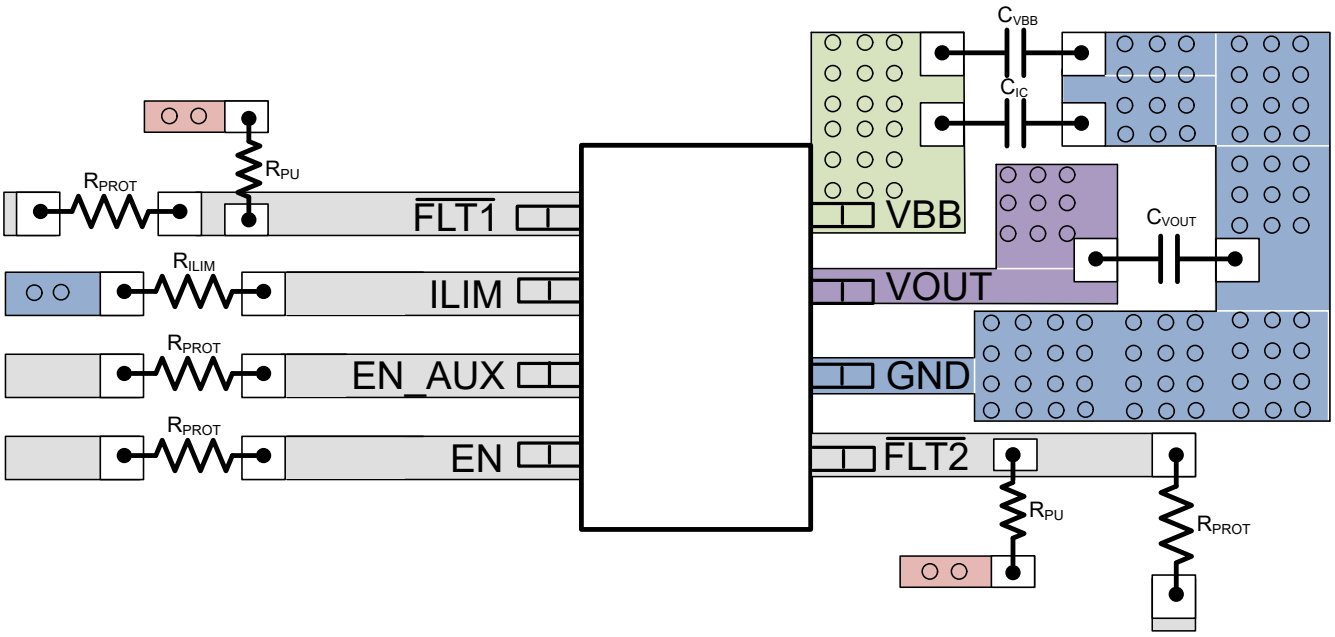
To achieve good thermal performance, connect the VBB pad to a large copper pour. On the top PCB layer, the pour can extend beyond the package dimensions. In addition to this, having a VBB plane on one or more internal PCB layers and/or on the bottom layer is recommended. Vias must connect these planes to the top VBB pour. Connecting the VOUT pad to a large copper pour on the board can also help to achieve better thermal performance.

If used in the design, the C_{IC} capacitor, must be placed as close as possible to the VBB and GND pins of the device. If a ground network is used for reverse battery protection, the C_{IC} capacitor must be connected from the VBB net to the IC_GND net. The C_{VBB} capacitor must be placed close to the VBB pin and connected to system ground to allow for best performance.

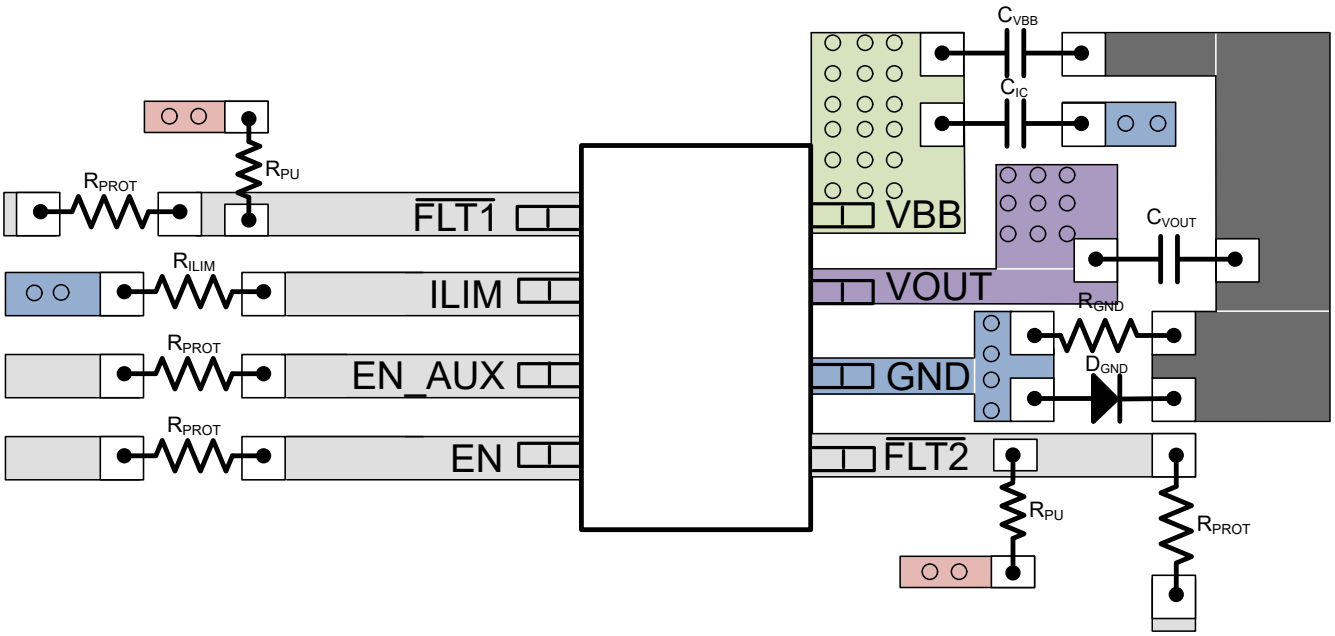
The R_{ILIM} resistor must be placed close to the ILIM and GND pins of the device. If a ground network is used for reverse battery protection, the R_{ILIM} must be connected from the ILIM pin to the IC_GND net for best current limit performance.

8.4.2 Layout Examples

8.4.2.1 Without a GND Network



8.4.2.2 With a GND Network



9 Device and Documentation Support

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS1HC120CQDYCRQ1	Active	Production	SOT-5X3 (DYC) | 8	4000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	H120Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

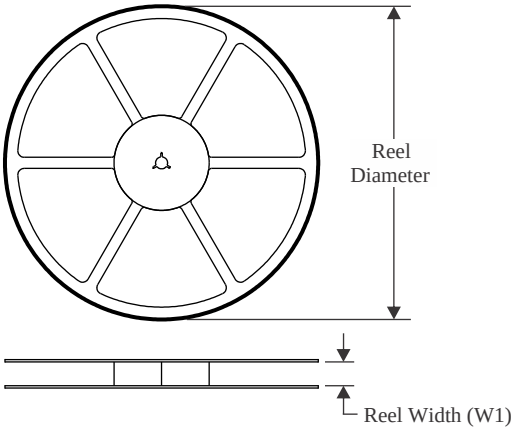
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

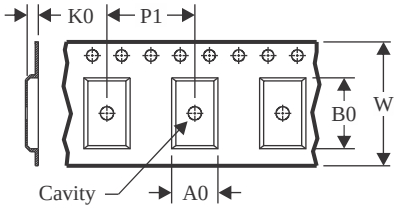
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

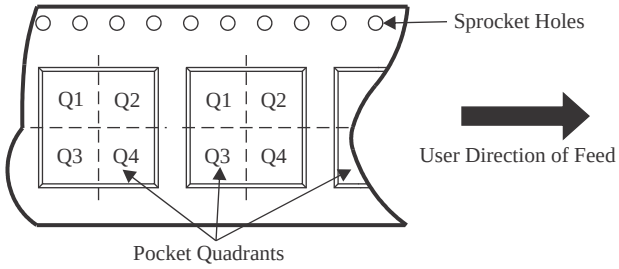


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

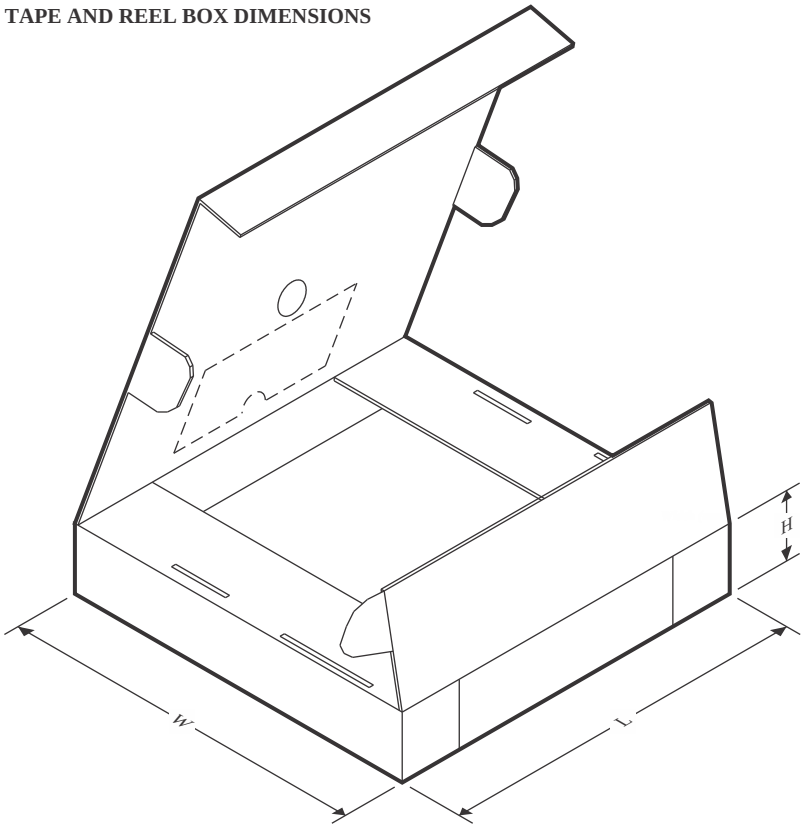
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1HC120CQDYCRQ1	SOT-5X3	DYC	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

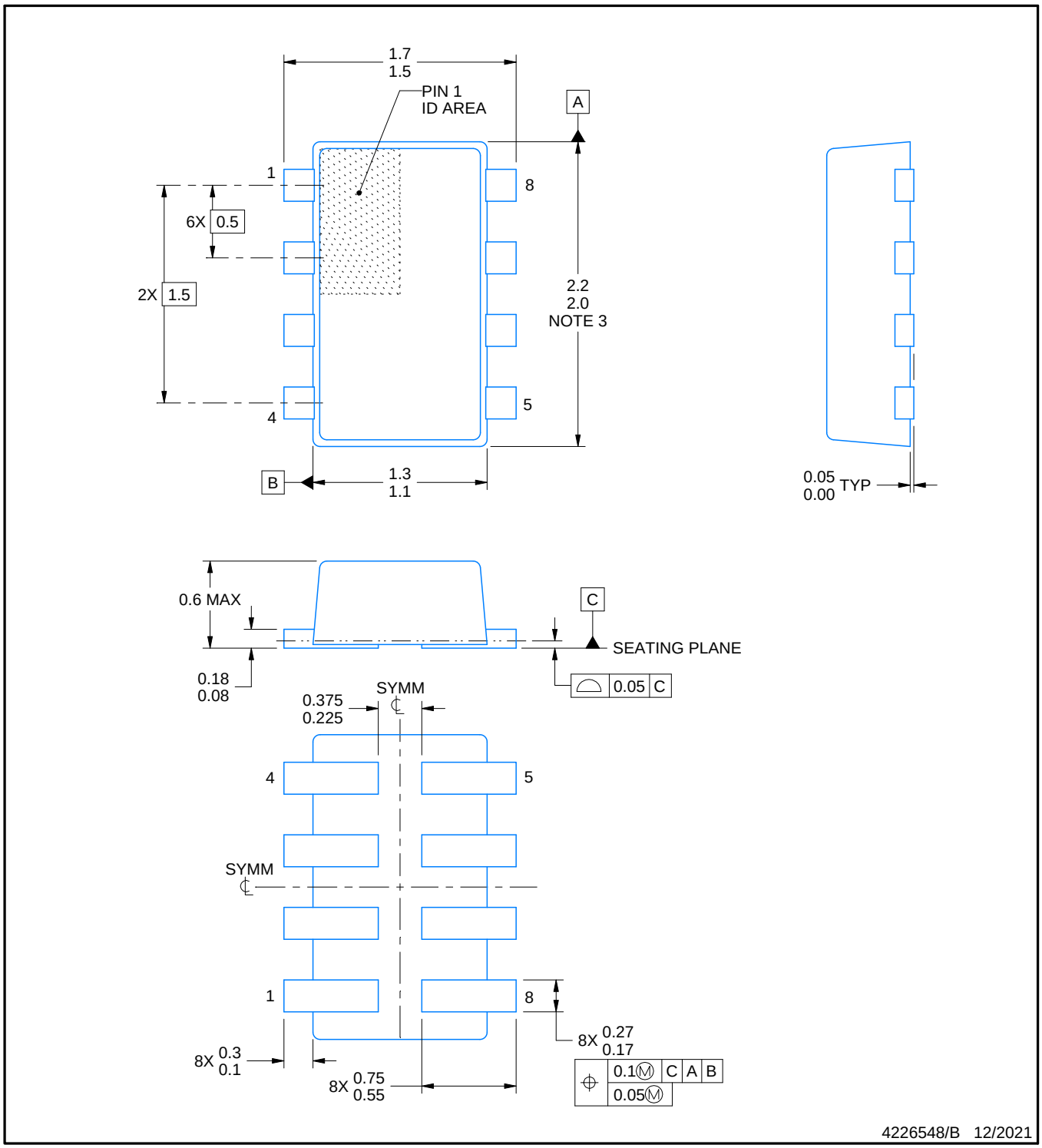
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1HC120CQDYCRQ1	SOT-5X3	DYC	8	4000	210.0	185.0	35.0

DYC0008A

PACKAGE OUTLINE

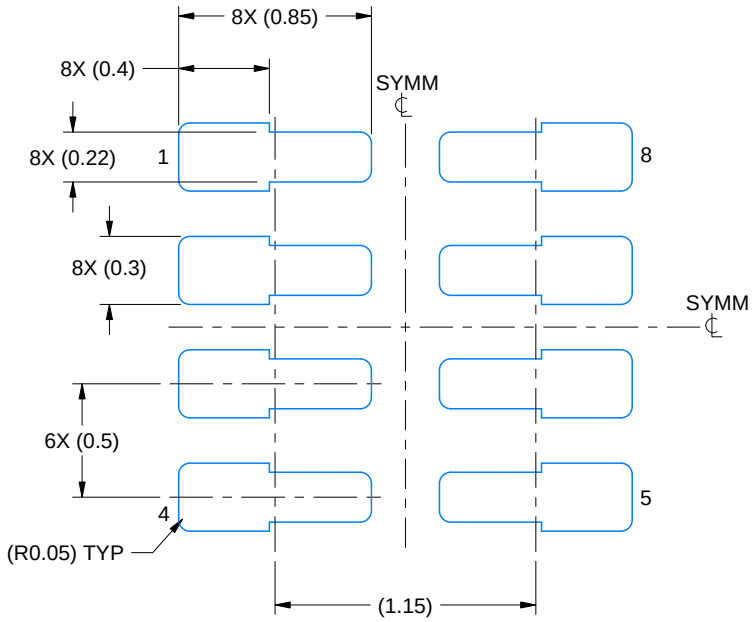
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

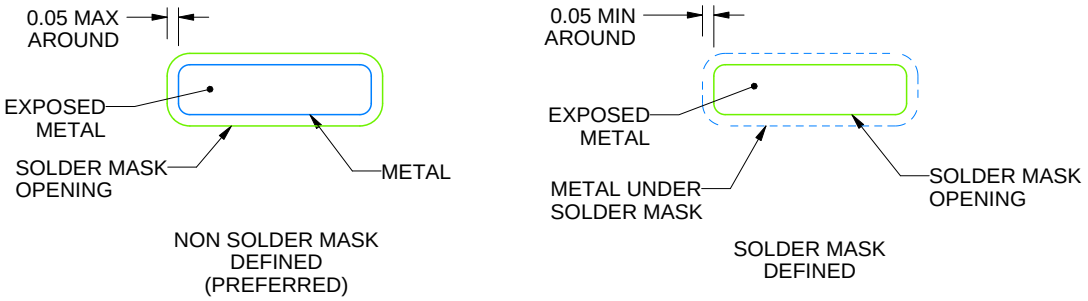


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X

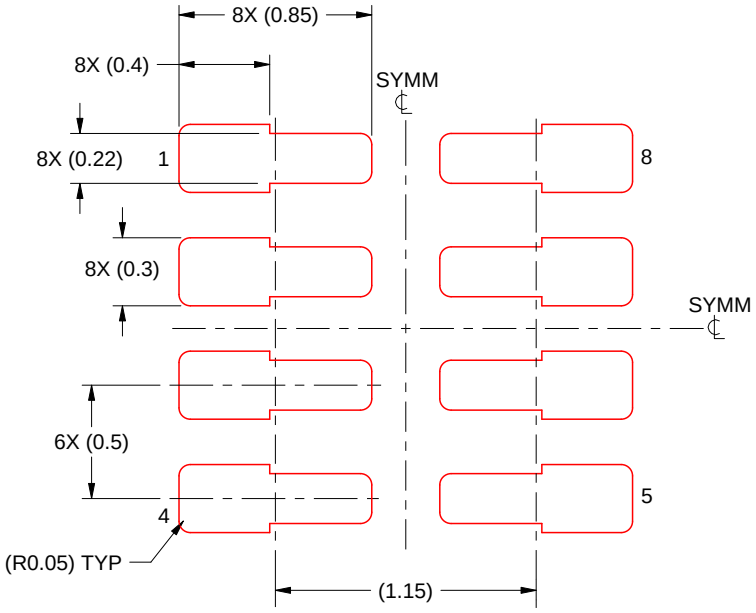


SOLDERMASK DETAILS

4226548/B 12/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4226548/B 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025