用于电源门控应用的 TPL5111 毫微功耗系统计时器

1 特性

- 可选计时间隔：100ms 至 7200s
- 计时器精度：1%（典型值）
- 电压为 2.5V 时，电流消耗为 35nA（典型值）
- 可通过电阻选择时间间隔
- 手动上电输入
- 单次触发功能
- 电源电压范围：1.8V 至 5.5V

2 应用

- 电池供电类系统的占空比控制
- 物联网 (IoT)
- 出入探测
- 篡改检测
- 家庭自动化传感器
- 温度调节装置
- 消费类电子产品
- 远程传感器
- 白色家电

3 说明

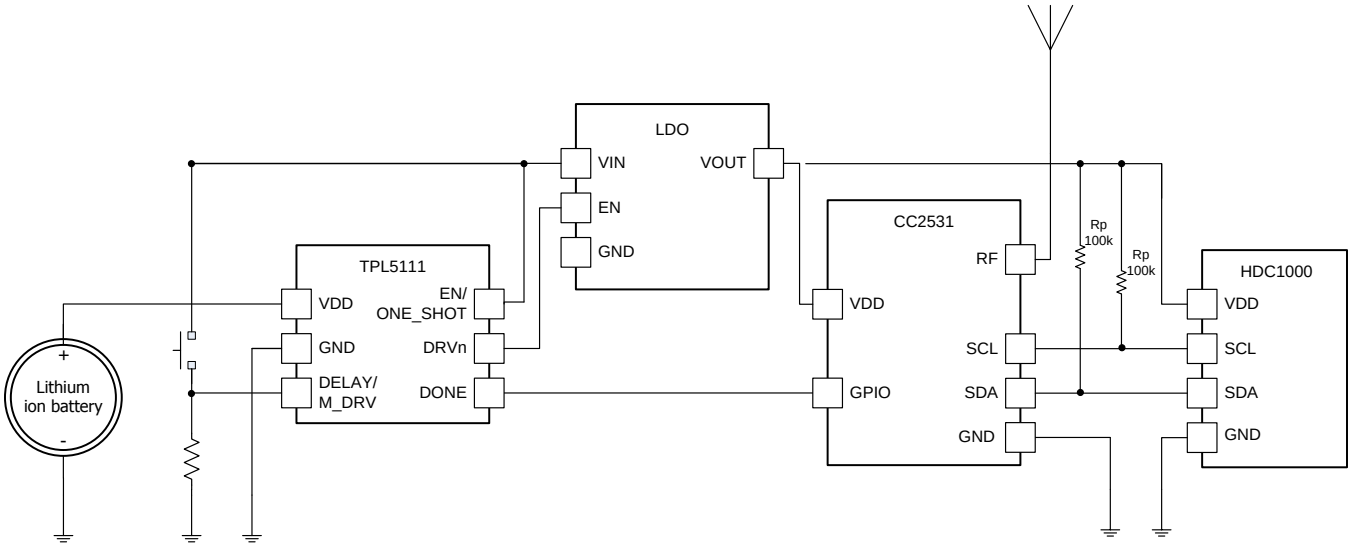
TPL5111 毫微功耗计时器是一种低功耗系统计时器，专为占空比或电池供电型应用中的电源门控而 设计。TPL5111 的电流消耗仅为 35nA，可用于启用或禁用微控制器或其他系统器件的电源，从而大幅降低休眠期间的总系统待机电流。这一节能特性可以大幅减小能量采集或无线传感器应用中所使用的电池 尺寸。TPL5111 提供 100ms 至 7200s 的可选计时间隔。此外，TPL5111 还具有独特的单次触发功能，计时器可仅在一个周期内发送启动脉冲。TPL5111 采用 6 引脚小外形尺寸晶体管 (SOT23) 封装。

器件信息(1)

器件编号	封装	封装尺寸（标称值）
TPL5111	SOT (6) DDC	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化应用电路原理图



目录

4 修订历史记录

Changes from Revision A (July 2015) to Revision B **Page**

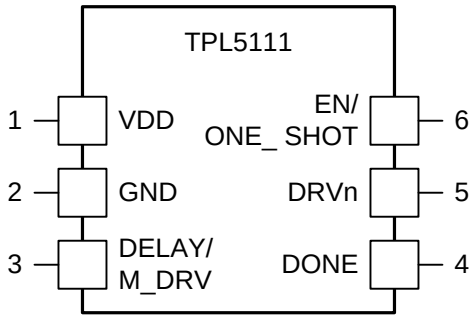
- Changed T_{ADC} and R_D equations in the *Quantization Error* section ... 14
- 添加了*接收文档更新通知* 部分 ... 18

Changes from Original (June 2015) to Revision A **Page**

- 添加了 完整数据表。 ... 1

5 Pin Configuration and Functions

DDC Package
6-Lead SOT-23
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	VDD	P	Supply voltage	
2	GND	G	Ground	
3	DELAY/ M_DRV	I	Time interval configuration (during power on) and logic input for manual Power ON	Resistance between this pin and GND is used to select the time interval. The manual Power ON signal (logic HIGH) can also connected to this pin.
4	DONE	I	Logic Input for watchdog functionality	Digital signal driven by the µC to indicate successful processing.
5	DRVn	O	Power Gating output signal generated every t_{IP}	The ENABLE pin of the LDO or DC-DC converter is connected to this pin. DRVn is active HIGH.
6	EN/ ONE_SHOT	I	Select mode of operation	When EN/ONE_SHOT = HIGH, the TPL5111 works as a TIMER. When EN/ONE_SHOT = LOW, the TPL5111 asserts DRVn one time for the programmed time interval. In this mode, the DRVn signal may be manually asserted by applying a logic HIGH to the DELAY/M_DRV pin.

(1) G= Ground, P= Power, O= Output, I= Input.

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	–0.3	6.0	V
Input Voltage at any pin(2)	–0.3	VDD + 0.3	V
Input Current on any pin	–5	5	mA
Junction Temperature, T_J(3)		150	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage between any two pins should not exceed 6 V.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is PDMAX = ($T_{J(MAX)}$ - T_A)/ $R_{\theta JA}$. All numbers apply for packages soldered directly onto a printed-circuit board (PCB).

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human Body Model, per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Ratings

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	1.8	5.5	V
Temperature	–40	105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPL5111 DDC (SOT-23) DDC 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics(1)

Specifications are for T_A= 25°C, VDD-GND = 2.5 V, unless otherwise stated.

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
POWER SUPPLY							
IDD	Supply current(4)	Operation mode			35	50	nA
		Digital conversion of external resistance (Rext)			200	400	µA
TIMER							
t_{IP}	Time interval Period	1650 selectable Time intervals	Minimum time interval		100		ms
			Maximum time interval		7200		s
	Time interval Setting Accuracy(5)	Excluding the precision of Rext			±0.6%		
	Time interval Setting Accuracy over supply voltage	1.8 V ≤ VDD ≤ 5.5 V			±25		ppm/V
t_{OSC}	Oscillator Accuracy			–0.5%		0.5%	
	Oscillator Accuracy over temperature(6)	–40°C ≤ T_A≤ 105°C			±100	±400	ppm/°C
	Oscillator Accuracy over supply voltage	1.8 V ≤ VDD ≤ 5.5 V			±0.4		%/V
	Oscillator Accuracy over life time(7)				±0.24%		
t_{DONE}	DONE Pulse width (6)			100			ns
t_{DRVn}	DRVn Pulse width	DONE signal not received			t_{IP}-50 ms		
t_Rext	Time to convert Rext				100	120	ms
DIGITAL LOGIC LEVELS							
VIH	Logic High Threshold DONE pin			0.7 × VDD			V
VIL	Logic Low Threshold DONE pin					0.3 × VDD	V
VOH	Logic output High Level DRVn pin	I_{out} = 100 µA		VDD – 0.3			V
		I_{out} = 1 mA		VDD – 0.7			V
VOL	Logic output Low Level DRVn pin	I_{out} = -100 µA				0.3	V
		I_{out} = –1 mA				0.7	V
VIH_{M_DRV}	Logic High Threshold DELAY/M_DRV pin			1.5			V

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_{A.}$ No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) The supply current excludes load and pullup resistor current. Input pins are at GND or VDD.
(5) The accuracy for time interval settings below 1second is ±10 0ms.
(6) This parameter is specified by design and/or characterization and is not tested in production.
(7) Operational life time test procedure equivalent to10 years.

6.6 Timing Requirements

			MIN(1)	NOM(2)	MAX(1)	UNIT
tr_{DRVn}	Rise Time DRVn(3)	Capacitive load 50 pF		50		ns
tf_{DRVn}	Fall Time DRVn(3)	Capacitive load 50 pF		50		ns
tD_{DONE}	DONE to DRVn delay	Minimum delay(4)		100		ns
		Maximum delay (4)		t_{DRVn}		
t_{M_DRV}	Valid manual MOSFET Power ON	Observation time 30 ms	20			ms
t_{DB}	De-bounce manual MOSFET Power ON			20		ms

(1) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(3) This parameter is specified by design and/or characterization and is not tested in production.
(4) From DRVn rising edge.

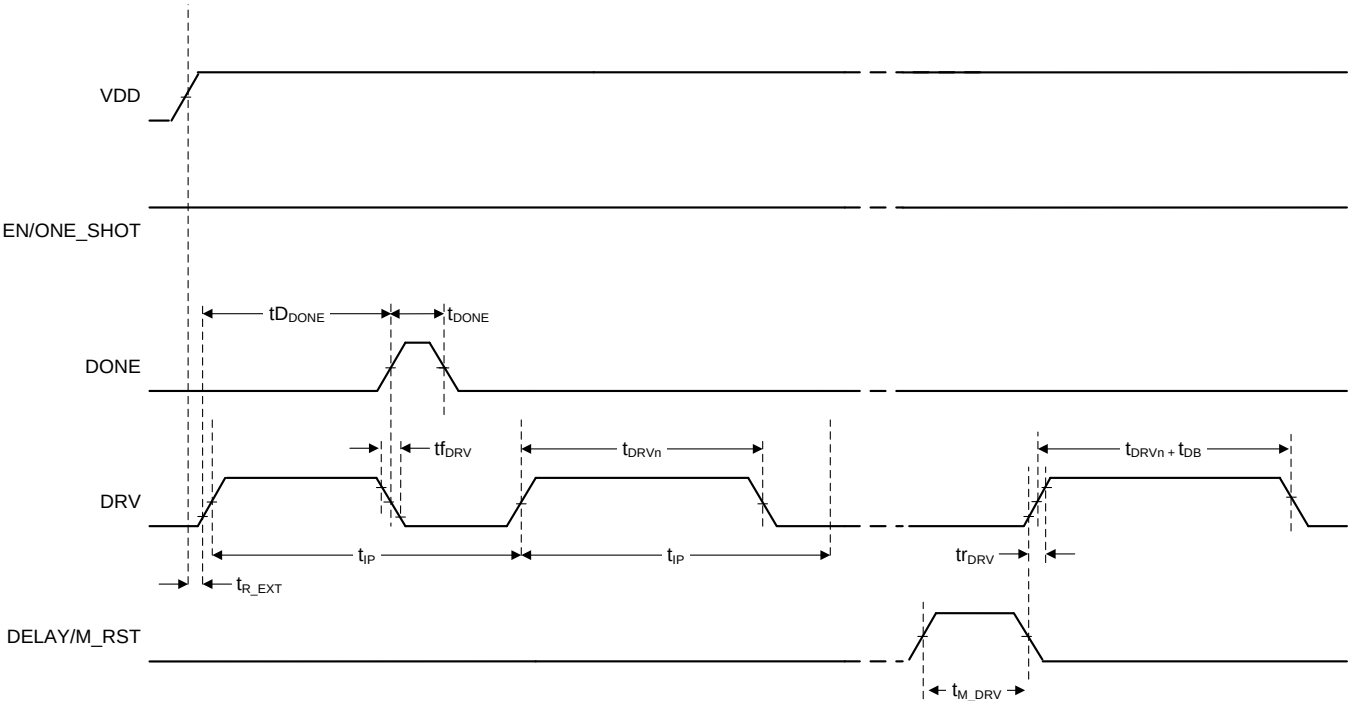


Figure 1. TPL5111 Timing

6.7 Typical Characteristics

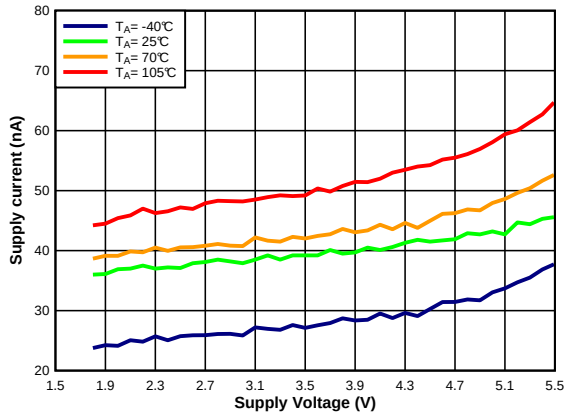


Figure 2. I_{DD} vs. V_{DD}

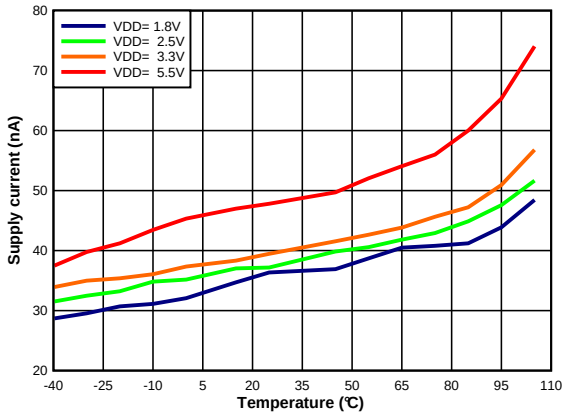


Figure 3. I_{DD} vs. Temperature

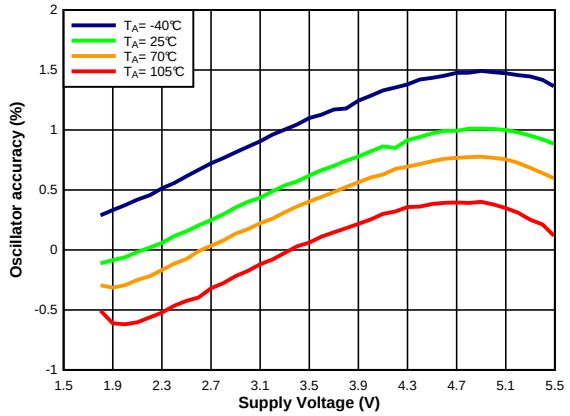


Figure 4. Oscillator Accuracy vs. V_{DD}

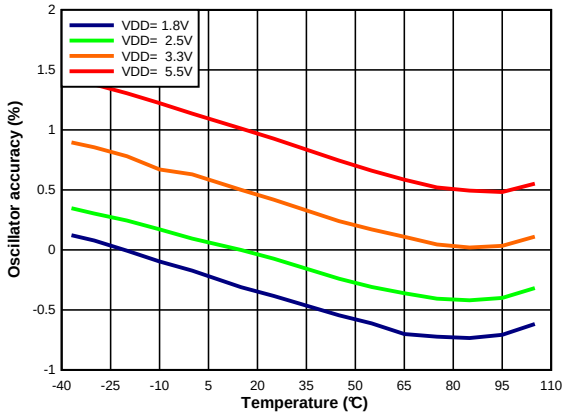


Figure 5. Oscillator Accuracy vs. Temperature

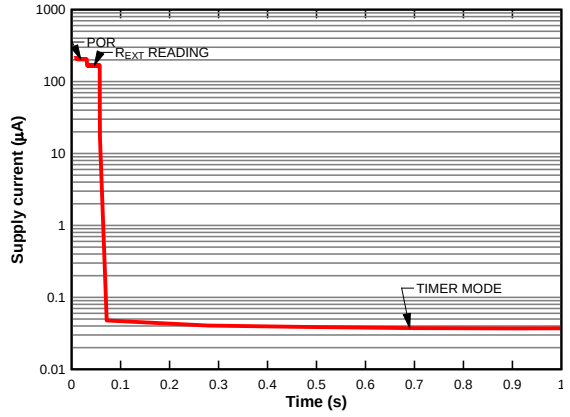


Figure 6. I_{DD} vs. Time

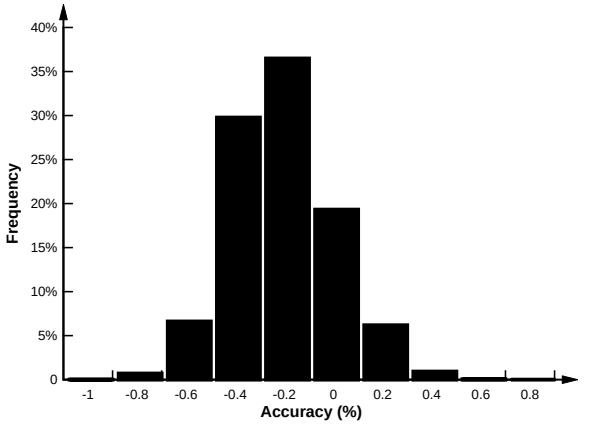


Figure 7. Time Interval Setting Accuracy

7 Detailed Description

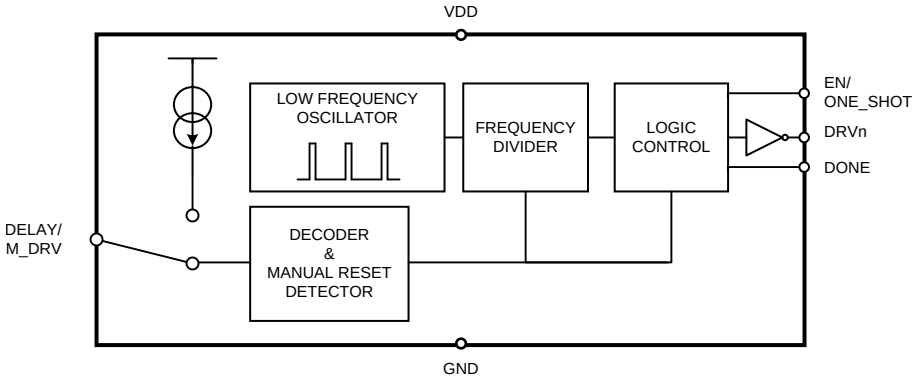
7.1 Overview

The TPL5111 is a timer with power gating feature. The TPL5111 can be used in power-cycled applications and provides selectable timing from 100 ms to 7200 s.

When configured in timer mode (EN/ONE_SHOT= HIGH), the TPL5111 periodically asserts a DRVn signal to an LDO or DC-DC converter that is used to turn on a microcontroller. If the microcontroller replies with a DONE signal within the programmed time interval (< t_{DRVn}), the TPL5111 de-asserts DRVn. Otherwise, the TPL5111 asserts DRVn for a time equal to t_{DRVn}.

The TPL5111 can also work in a one-shot mode (EN/ONE_SHOT= LOW). In this mode, the DRVn signal is asserted just one time at the power on of the TPL5111. If the µC replies with a DONE signal within the programmed time interval (< t_{DRVn}), the TPL5111 de-asserts DRVn. Otherwise the TPL5111 asserts DRVn for a time equal to t_{DRVn}.

7.2 Functional Block Diagram



7.3 Feature Description

The TPL5111 implements a periodic power gating feature or one-shot power gating according to the EN/ONE_SHOT voltage. A manual Power ON function is realized by momentarily pulling the DELAY/M_DRV pin to VDD.

7.3.1 DRVn

The DRVn pin may be connected to the enable input of an LDO or DC-DC converter. The pulse generated at DRVn is equal to the programmed time interval period (t_{IP}), minus 50 ms. It is shorter if a DONE signal is received from the µC before t_{IP} – 50 ms. If the DONE signal is not received within t_{IP} – 50 ms, the DRVn signal will be LOW for the last 50 ms of t_{IP} before the next cycle starts.

The default value (after resistance reading) is HIGH. The signal is sent out from the TPL5111 when the programmed time interval starts. When the DRVn is HIGH, the manual power ON signal is ignored.

7.3.2 DONE

The DONE pin is driven by a µC to signal that the µC is working properly. The TPL5111 recognizes a valid DONE signal as a low to high transition. If two or more DONE signals are received within the time interval, only the first DONE signal is processed. The minimum DONE signal pulse length is 100 ns. When the TPL5111 receives the DONE signal it asserts DRVn logic LOW.

7.4 Device Functional Modes

7.4.1 Start-Up

During start-up after POR, the TPL5111 executes a one-time measurement of the resistance attached to the DELAY/M_DRV pin in order to determine the desired time interval for DRVn. This measurement interval is t_{R_EXT}. During this measurement a constant current is temporarily flowing into R_{EXT}.

Once the reading of the external resistance is complete, the TPL5111 enters automatically in one of the two modes according to the EN/ONE_SHOT value. The EN/ONE_SHOT pin must be hard wired to GND or VDD according to the required mode of operation.

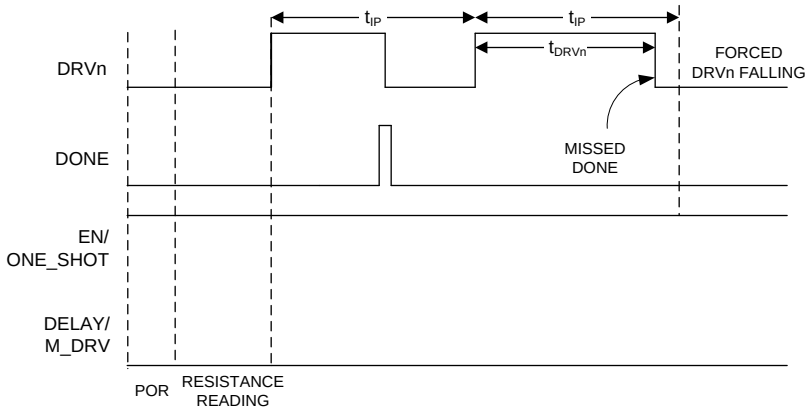


Figure 8. Startup - Timer Mode

7.4.2 Timer Mode

During timer mode (EN/ONE_SHOT = HIGH), the TPL5111 asserts periodic DRVn pulses according to the programmed time interval. The length of the DRVn pulses is set by the receiving of a DONE pulse from the µC. See Figure 8.

7.4.3 One-Shot Mode

During one-shot mode (EN/ONE_SHOT = LOW), the TPL5111 generates just one pulse at the DRVn pin which lasts according to the programmed time interval. In one-shot mode, other DRVn pulses can be triggered using the DELAY/M_DRV pin. If a valid manual power ON occurs when EN/ONE_SHOT is LOW, the TPL5111 generates just one pulse at the DRVn pin. The duration of the pulse is set by the programmed time interval. Also in this case, if a DONE signal is received within the programmed time interval (minus 50 ms), the DRVn output is asserted LOW. See Figure 9 and Figure 10.

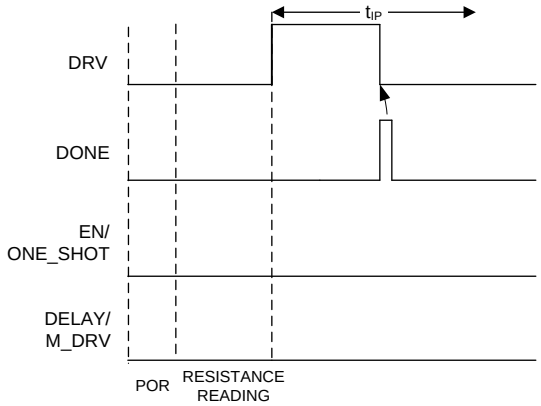


Figure 9. Start-Up One-Shot Mode (DONE Received Within t_{IP})

Device Functional Modes (continued)

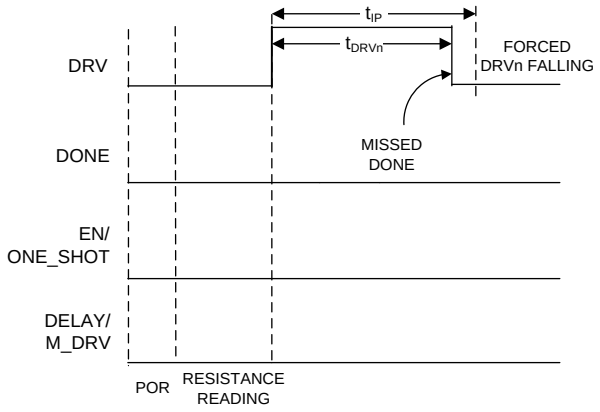


Figure 10. Start-Up One-Shot Mode (No DONE Received Within t_{IP})

7.5 Programming

7.5.1 Configuring the Time Interval With the DELAY/M_DRV Pin

The time interval between two adjacent DRVn pulses (rising edges, in timer mode) is selectable through an external resistance (R_{EXT}) between the DELAY/M_DRV pin and ground. The resistance (R_{EXT}) must be in the range between 500 Ω and 170 kΩ. At least a 1% precision resistance is recommended. See *Selection of the External Resistance* on how to set the time interval using R_{EXT}. During start-up, the external resistance is read immediately after POR.

7.5.2 Manual Power ON Applied to the DELAY/M_DRV Pin

If VDD is applied to the DELAY/M_DRV pin after start-up is completed, the TPL5111 recognizes this as a manual Power ON condition. In this case R_{EXT} is not re-read. If the manual Power ON is asserted during the POR or during the R_{EXT} reading procedure, the reading procedure is aborted and is restarted as soon as the manual Power ON switch is released. A pulse on the DELAY/M_DRV pin is recognized as a valid manual Power ON only if it lasts at least 20 ms (observation time is 30 ms). If DRVn is already HIGH the manual Power ON is ignored. The manual Power ON may be implemented using a switch (momentary mechanical action).

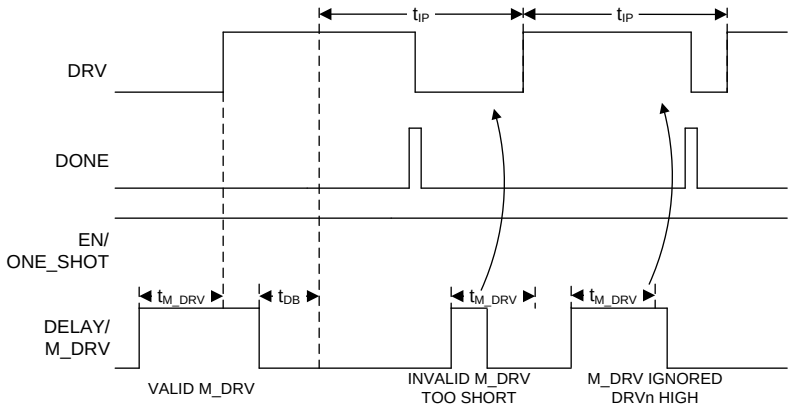


Figure 11. Manual Power ON in Timer Mode

Programming (continued)

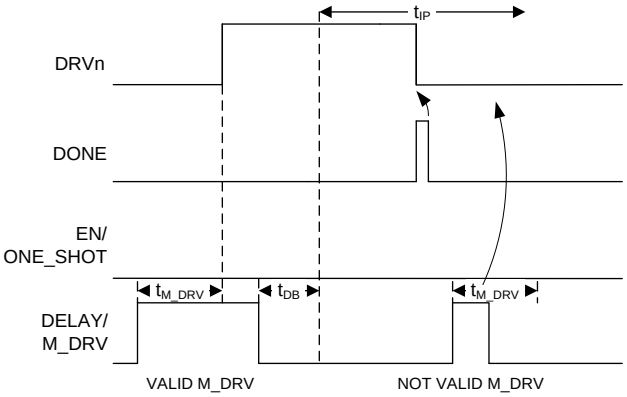


Figure 12. Manual Power ON in One-Shot Mode

7.5.2.1 DELAY/M_DRV

A resistance in the range between 500 Ω and 170 kΩ must to be connected to the DELAY/M_DRV pin to select a valid time interval. At POR and during the reading of R_{EXT}, the DELAY/M_DRV pin is internally connected to an analog signal chain through a multiplexer. After the reading of R_{EXT}, the analog circuit is switched off and the DELAY/M_DRV pin is internally connected to a digital circuit.

In this state, a logic HIGH applied to the DELAY/M_DRV pin is interpreted by the TPL5111 as a manual power ON. The manual power ON detection is provided with a de-bounce feature (on both edges) which makes the TPL5111 insensitive to the glitches on the DELAY/M_DRV.

The DELAY/M_DRV pin must stay HIGH for at least 20 ms to be valid. Once a valid signal at DELAY/M_DRV is understood as a manual power on, the DRVn signal will be asserted within the next 10 ms. Its duration will be according to the programmed time interval (minus 50 ms), or less if the DONE is received.

A manual power ON signal resets all the counters. The counters will restart as soon as a valid manual power ON signal is recognized and the signal at DELAY/M_DRV pin is asserted LOW. Due to the asynchronous nature of the manual power ON signal and its arbitrary duration, the HIGH status of the DRVn signal may have an uncertainty of about ±5 ms.

An extended assertion of a logic HIGH at the DELAY/M_DRV pin will turn on DRVn for a time longer than the programmed time interval. DONE signals received while the DELAY/M_DRV is HIGH are ignored. If the DRVn is already HIGH the manual power ON is ignored.

7.5.2.2 Circuitry

The manual Power ON may be implemented using a switch (momentary mechanical action). Using a single-pole single-throw (SPST) switch offers a low cost solution. The DELAY/M_DRV pin may be directly connected to V_{DD} with R_{EXT} in the circuit. The current drawn from the supply voltage during the manual power ON is given by V_{DD}/R_{EXT}.

Programming (continued)

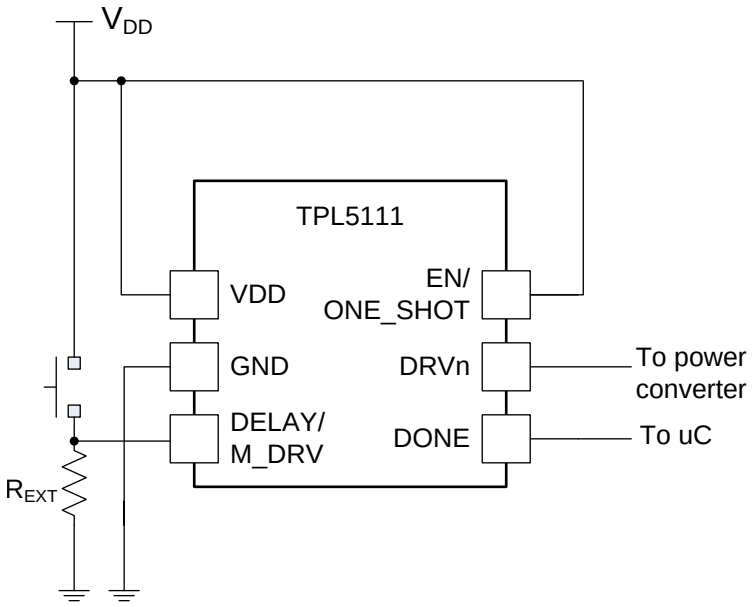


Figure 13. Manual Power ON With SPST Switch

7.5.3 Selection of the External Resistance

To set the time interval, the external resistance R_{EXT} is selected according to Equation 1:

$$R_{EXT} = 100 \left(\frac{-b + \sqrt{b^2 - 4a(c - 100\,T)}}{2a} \right) \quad (1)$$

where

- T is the desired time interval (t_{IP}) in seconds.
- R_{EXT} is the resistance value in Ω.
- a, b, c are coefficients depending on the value of the desired time interval. The coefficients are selected from Table 1 based on the range in which the desired t_{IP} falls.

Table 1. Coefficients for Equation 1

SET	TIME INTERVAL RANGE (S)	a	b	c
1	1 < T ≤ 5	0.2253	–20.7654	570.5679
2	5 < T ≤ 10	–0.1284	46.9861	–2651.8889
3	10 < T ≤ 100	0.1972	–19.3450	692.1201
4	100 < T ≤ 1000	0.2617	–56.2407	5957.7934
5	T > 1000	0.3177	–136.2571	34522.4680

EXAMPLE

Required time interval: 8 s

Coefficient set number 2 is used in this case. The formula becomes Equation 2.

$$R_{EXT} = 100 \left(\frac{46.9861 - \sqrt{46.9861^2 + 4*0.1284(-2561.8889 - 100*8)}}{2*0.1284} \right) \quad (2)$$

The resistance value is 10.18 kΩ.

Table 2 and Table 3 contain example values of t_{IP} and their corresponding value of R_{EXT}.

Table 2. First 9 Time Intervals

t_{IP} (ms)	RESISTANCE (Ω)	CLOSEST REAL VALUE (Ω)	PARALLEL of TWO 1% TOLERANCE RESISTORS, (kΩ)
100	500	500	1.0 // 1.0
200	1000	1000	-
300	1500	1500	2.43 // 3.92
400	2000	2000	-
500	2500	2500	4.42 // 5.76
600	3000	3000	5.36 // 6.81
700	3500	3500	4.75 // 13.5
800	4000	4000	6.19 // 11.3
900	4500	4501	6.19 // 16.5

Table 3. Most Common Time Intervals Between 1s to 2h

t_{IP}	CALCULATED RESISTANCE (kΩ)	CLOSEST REAL VALUE (kΩ)	PARALLEL of TWO 1% TOLERANCE RESISTORS,(kΩ)
1s	5.20	5.202	7.15 // 19.1
2s	6.79	6.788	12.4 // 15.0
3s	7.64	7.628	12.7// 19.1
4s	8.30	8.306	14.7 // 19.1
5s	8.85	8.852	16.5 // 19.1
6s	9.27	9.223	18.2 // 18.7
7s	9.71	9.673	19.1 // 19.6
8s	10.18	10.180	11.5 // 8.87
9s	10.68	10.68	17.8 // 26.7
10s	11.20	11.199	15.0 // 44.2
20s	14.41	14.405	16.9 // 97.6
30s	16.78	16.778	32.4 // 34.8
40s	18.75	18.748	22.6 // 110.0
50s	20.047	20.047	28.7 // 66.5
1min	22.02	22.021	40.2 // 48.7
2min	29.35	29.349	35.7 // 165.0
3min	34.73	34.729	63.4 // 76.8
4min	39.11	39.097	63.4 // 102.0
5min	42.90	42.887	54.9 // 196.0
6min	46.29	46.301	75.0 // 121.0
7min	49.38	49.392	97.6 // 100.0
8min	52.24	52.224	88.7 // 127.0
9min	54.92	54.902	86.6 // 150.0
10min	57.44	57.437	107.0 // 124.0
20min	77.57	77.579	140.0 // 174.0
30min	92.43	92.233	182.0 // 187.0
40min	104.67	104.625	130.0 // 536.00
50min	115.33	115.331	150.0 // 499.00
1h	124.91	124.856	221.0 // 287.00
1h30min	149.39	149.398	165.0 // 1580.0
2h	170.00	170.00	340.0 // 340.0

7.5.4 Quantization Error

The TPL5111 can generate 1650 discrete timer intervals in the range of 100 ms to 7200 s. The first 9 intervals are multiples of 100 ms. The remaining 1641 intervals cover the range between 1 s to 7200 s. Because they are discrete intervals, there is a quantization error associated with each value.

The quantization error can be evaluated according to Equation 3:

$$Err = 100\frac{(T_{DESIRED} - T_{ADC})}{T_{DESIRED}}$$

where

- $T_{ADC} = INT\left[\frac{1}{100}\left(aR_D^2 + bR_D + c\right)\right]$
- $R_D = \frac{R_{EXT}}{100}$

(3)

R_{EXT} is the resistance calculated with Equation 1 and a, b, c are the coefficients of the equation listed in Table 1.

7.5.5 Error Due to Real External Resistance

R_{EXT} is a theoretical value and may not be available in standard commercial resistor values. It is possible to closely approach the theoretical R_{EXT} using two or more standard values in parallel. However, standard values are characterized by a certain tolerance. This tolerance will affect the accuracy of the time interval.

The accuracy can be evaluated using the following procedure:

1. Evaluate the min and max values of R_{EXT} (R_{EXT_MIN}, R_{EXT_MAX} with Equation 1 using the selected commercial resistance values and their tolerances.
2. Evaluate the time intervals ($T_{ADC\_MIN}[R_{EXT\_MIN}]$, $T_{ADC\_MAX}[R_{EXT\_MAX}]$) with the T_{ADC} equation mentioned in Equation 3.
3. Find the errors using Equation 3 with T_{ADC_MIN}, T_{ADC_MAX}.

The results of the formula indicate the accuracy of the time interval.

The example below illustrates the procedure.

- Desired time interval, T_desired = 600 s,
- Required R_{EXT} from Equation 1, R_{EXT}= 57.44 kΩ.

From Table 3 R_{EXT} can be built with a parallel combination of two commercial values with 1% tolerance: R1 = 107 kΩ, R2 = 124 kΩ. The uncertainty of the equivalent parallel resistance can be found using Equation 4:

$$uR_{//} = R_{//}\sqrt{\left(\frac{u_{R1}}{R1}\right)^2 + \left(\frac{u_{R2}}{R2}\right)^2}$$

where

- uRn (n=1,2) represent the uncertainty of a resistance (see Equation 5)

(4)

$$u_{Rn} = Rn\frac{Tolerance}{\sqrt{3}}$$

(5)

The uncertainty of the parallel resistance is 0.82%, which means the value of R_{EXT} may range between R_{EXT_MIN} = 56.96 kΩ and R_{EXT_MAX} = 57.90 kΩ.

Using these value of R_{EXT}, the digitized timer intervals calculated by T_{ADC} equation mentioned in Equation 3 are respectively T_{ADC_MIN} = 586.85 s and T_{ADC_MAX} = 611.3 s, giving an error range of –1.88% / +2.19%. The asymmetry of the error range is due to the quadratic transfer function of the resistance digitizer.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

In battery-powered applications one design constraint is the need for low current consumption. The TPL5111 is suitable in applications where there is a need to monitor environmental conditions at a fixed time interval, but at a very low rate. In these applications a watchdog or other internal timer in a µC is often used to implement a wake-up function. Typically, the power consumption of these timers is not optimized. Using the TPL5111 to implement a periodic power gating of the µC or of the entire system can reduce current consumption to only tens of nA.

8.2 Typical Application

The TPL5111 can be used in environment sensor nodes such as humidity and temperature sensor node. The measured the humidity and temperature data may be transmitted to a host controller through a low power RF micro such as the CC2531. The temperature and the humidity in a home application do not change quickly, so the measurement and the transmission of the data can be done at very low rate, such as every 30 seconds. Using the TPL5111 as a system timer it is possible to completely turn off the RF micro when not transmitting and extend the battery life, as shown in Figure 14. The TPL5111 will turn on the LDO when the programmed time interval elapses. The manual Power ON switch can also be used to override the periodic turn-on behavior and enable on-demand power on.

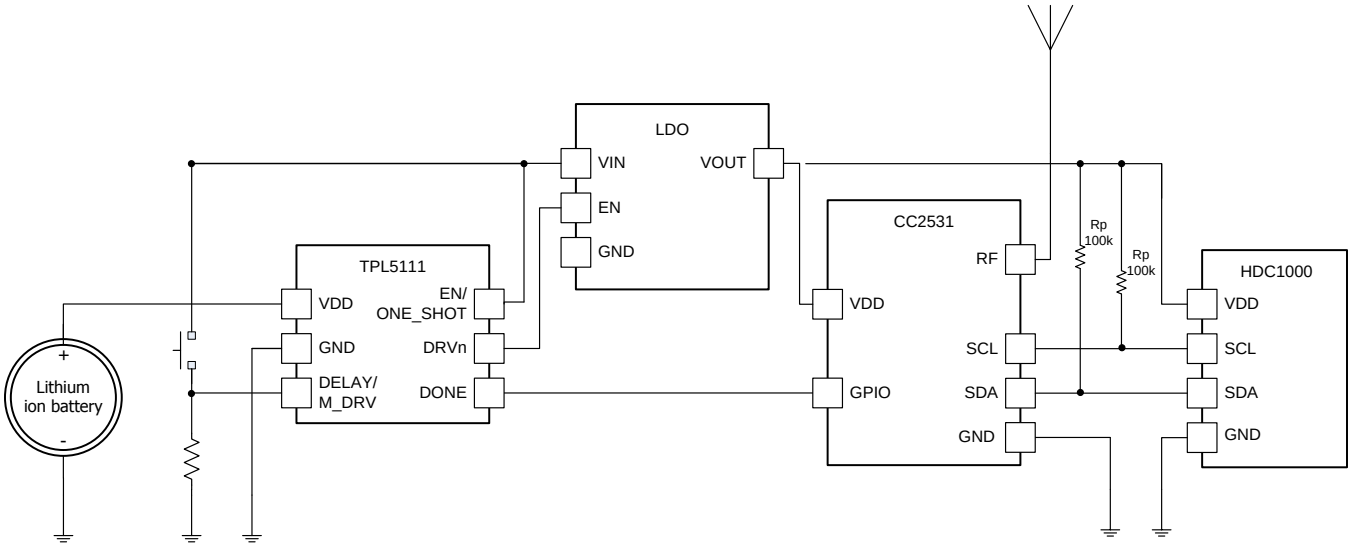


Figure 14. Sensor Node

8.2.1 Design Requirements

Assume that the system design requirements include a low current consumption constraint to maximize battery life. The data may be acquired at a rate which is in the range between 30 s and 60 s, so the programmability of the TPL5111 allows optimization of system power consumption.

Typical Application (continued)

8.2.2 Detailed Design Procedure

When the primary constraint is battery life, the selection of a low power voltage regulator or DC-DC converter to power the µC is mandatory. The first step in the design is to calculate the power consumption of each device in the different modes of operation. An example is the HDC1000 digital humidity and temperature sensor combined with an RF micro. In measurement mode, the RF micro is in normal operating and transmission mode. The LDO or DC-DC converter should be selected to provide the necessary current source. For example, the HDC1000 consumes a maximum of 220 µA during a humidity measurement, and 300 µA during start-up. The CC2531 consumes 29 mA in TX mode. The LDO should be capable of sourcing > 30 mA, which is an easy requirement to meet.

Assuming the desired wake-up interval is 30 seconds, then referring to Table 3, the values for parallel R_{EXT} resistors are 32.4 kΩ and 34.8 kΩ.

8.2.3 Application Curve

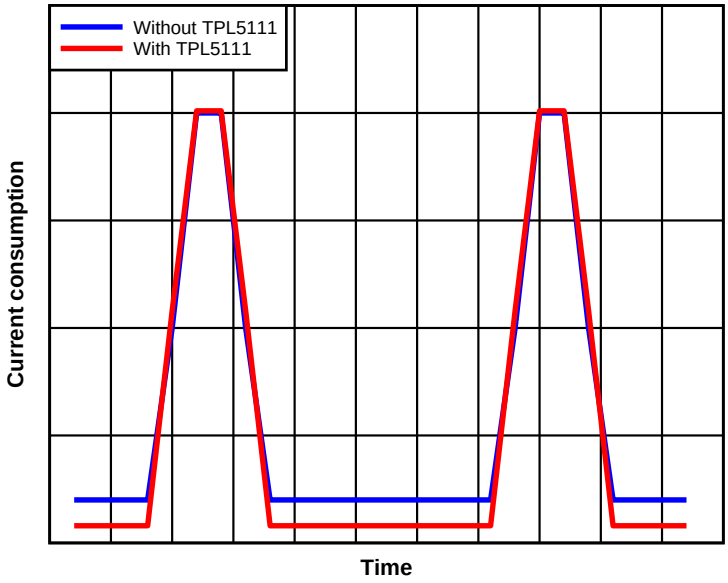


Figure 15. Effect of TPL5111 on Current Consumption

9 Power Supply Recommendations

The TPL5111 requires a voltage supply within 1.8 V and 5.5 V. A multilayer ceramic bypass X7R capacitor of 0.1 µF between VDD and GND pin is recommended.

10 Layout

10.1 Layout Guidelines

The DELAY/M_DRV pin is sensitive to parasitic capacitance. TI recommends that the traces connecting the resistance on this pin to GROUND be kept as short as possible to minimize parasitic capacitance. This capacitance can affect the initial set up of the time interval. Signal integrity on the DRVn pin is also improved by keeping the trace length between the TPL5111 and the enable input of the LDO/DC-DC converter short to reduce the parasitic capacitance. The EN/ONE_SHOT should to be tied to GND or VDD with short traces, and should never be left floating. The DONE input should never be left floating. If not tied to a µC GPIO, the DONE pin should be tied to ground.

10.2 Layout Example

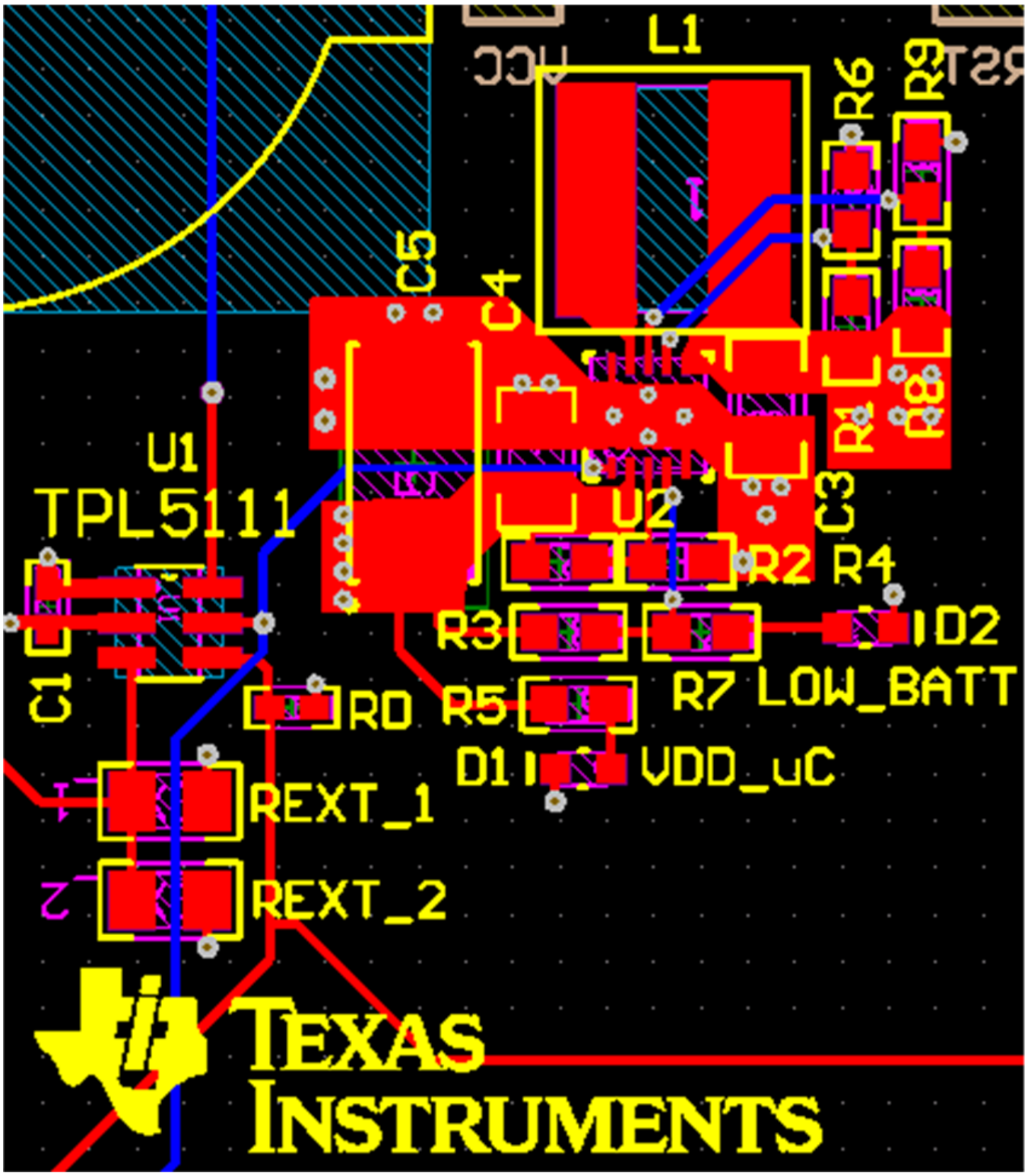


Figure 16. Layout

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.3 商标

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11.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPL5111DDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZFVX
TPL5111DDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZFVX
TPL5111DDCRG4	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZFVX
TPL5111DDCRG4.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZFVX
TPL5111DDCT	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZFVX
TPL5111DDCT.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZFVX

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

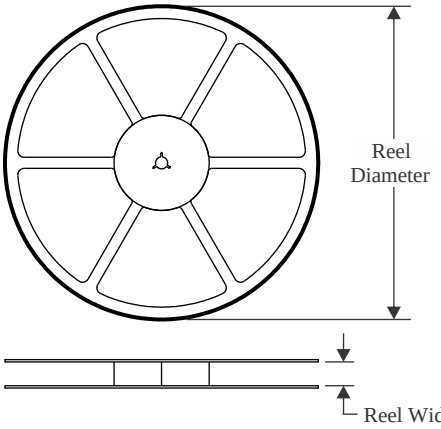
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

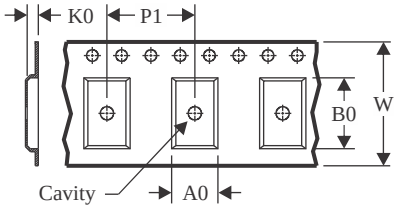
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

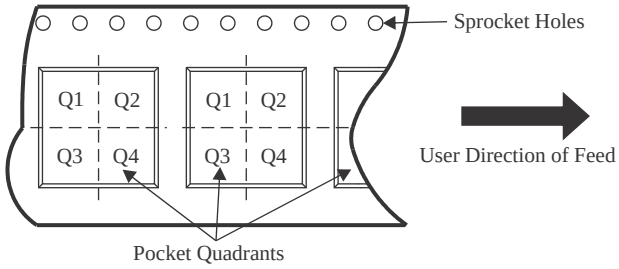


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

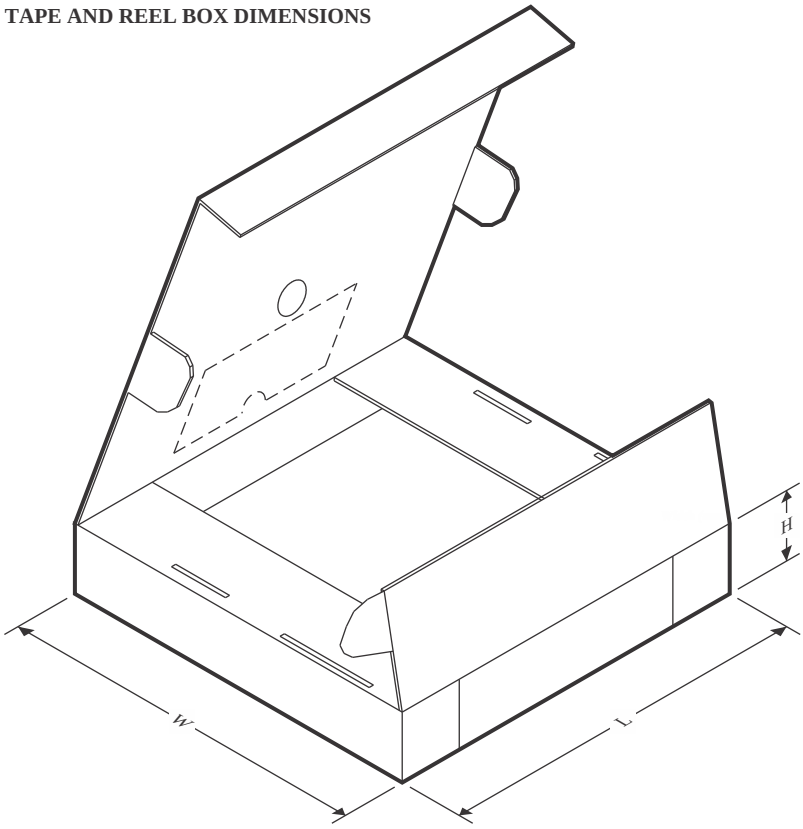
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL5111DDCR	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPL5111DDCRG4	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPL5111DDCT	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

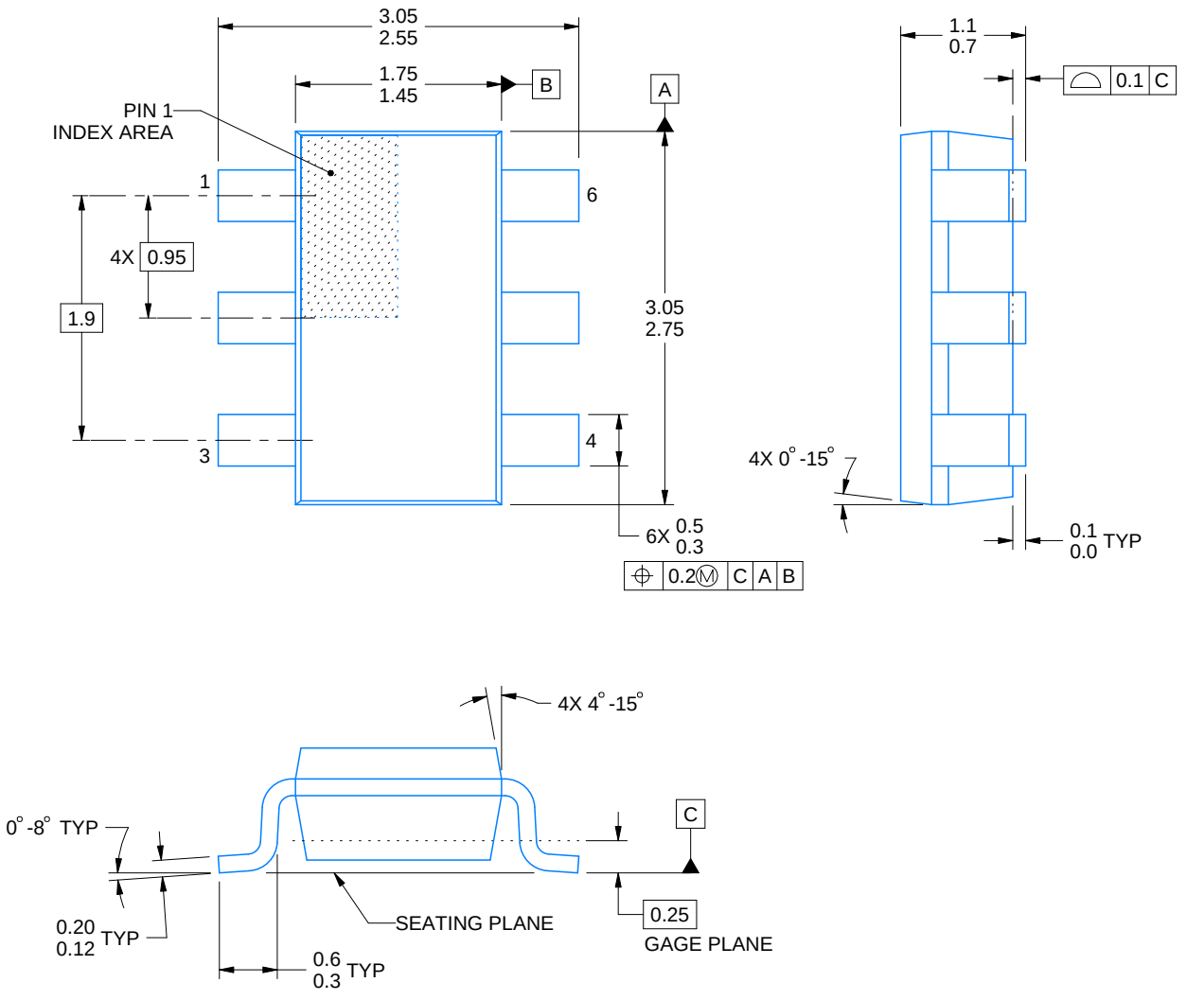
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL5111DDCR	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
TPL5111DDCRG4	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
TPL5111DDCT	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

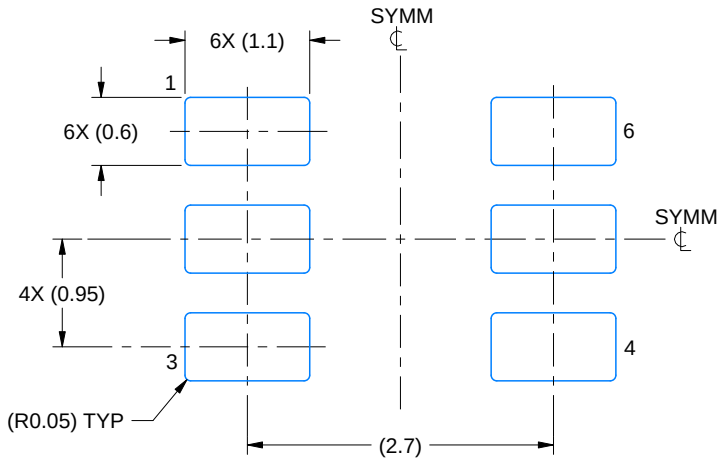
SMALL OUTLINE TRANSISTOR



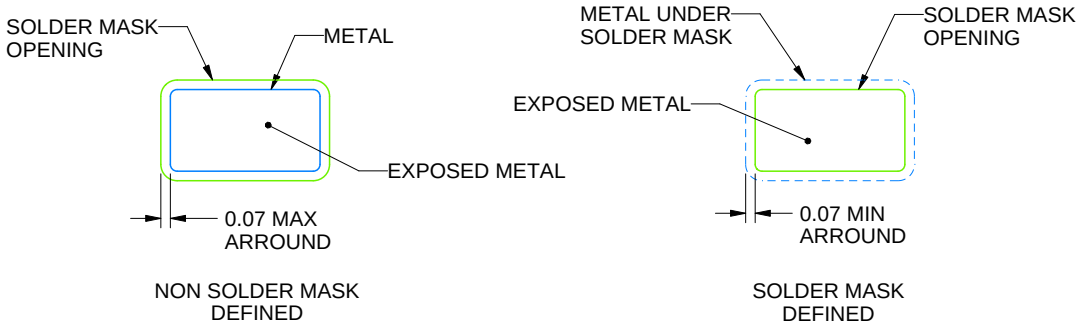
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

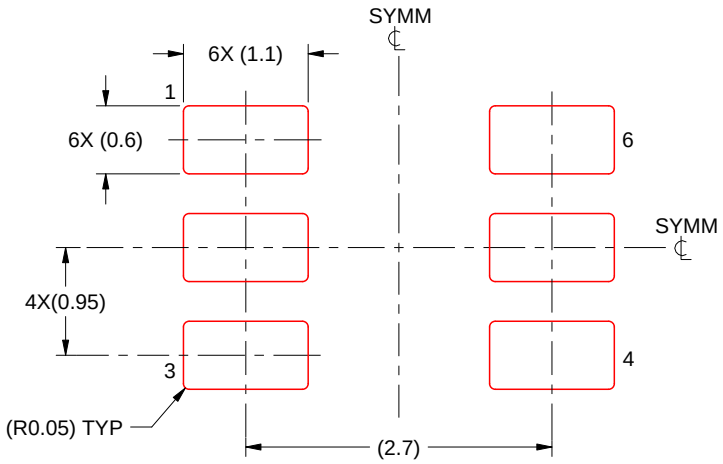


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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