TPL5100 具有 MOS 驱动器的毫微功耗可编程定时器

1 特性

- 电源电压范围为 1.8V 至 5.0V
- 可选定时器间隔 16s 至 1024s
- 流耗 30nA（2.5V 时的典型值）

2 应用

- 电池供电系统
- 能量收集系统
- 远程数据记录器
- 传感器节点
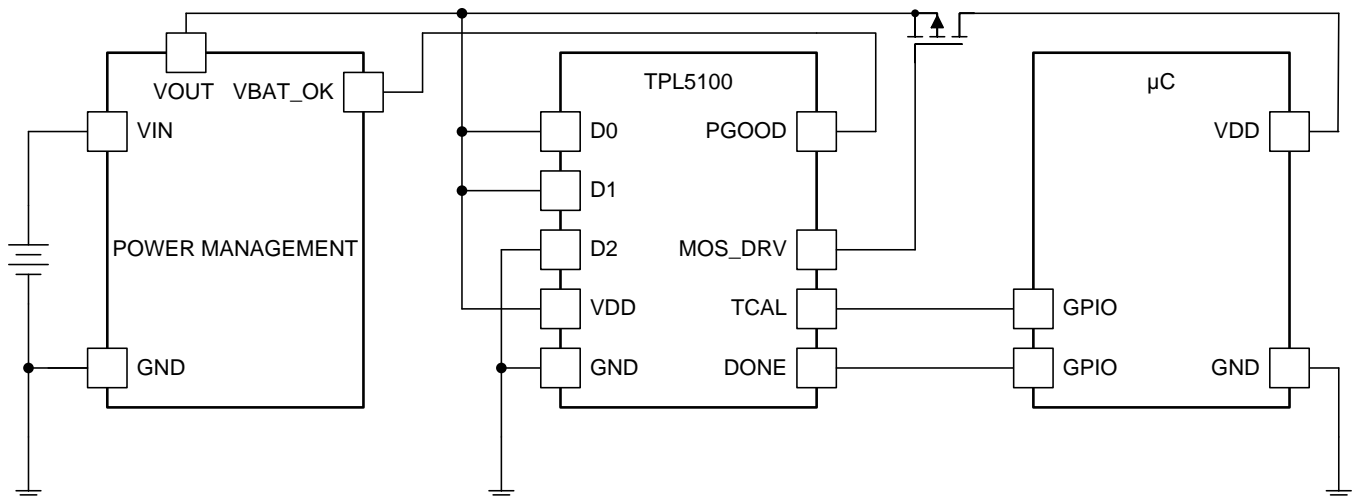- 电源选通应用
- 楼宇自动化
- 低功耗无线系统
- 消费类电子产品

3 说明

TPL5100 是一个长期定时器集成电路 (IC)，针对低功耗应用进行了优化。 TPL5100 能够替代一个微型控制器 (µC) 的内部定时器，使 µC 能够完全关闭，而不用运行一个定时器，从而减少 60% 至 80% 的总功耗。TPL5100 适用于循环供电应用，并且提供 16 秒至 1024 秒的可选定时间隔。 TPL5100 还可通过一个电源正常数字输入监视电池管理 IC，并在存在正常电源电压时仅为微控制器供电。 此器件采用 10 引脚超薄小外形尺寸 (VSSOP) 封装。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
TPL5100	VSSOP (10)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化应用电路原理图

English Data Sheet: SNAS629

目录

4 修订历史记录

Changes from Revision B (August 2013) to Revision C   **Page**

- Added *ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device* and *Documentation Support section,* and *Mechanical, Packaging*, and *Orderable Information section* 3
- Removed T_A value. 4

5 Pin Configuration and Functions

VSSOP
10 Pins
Top View
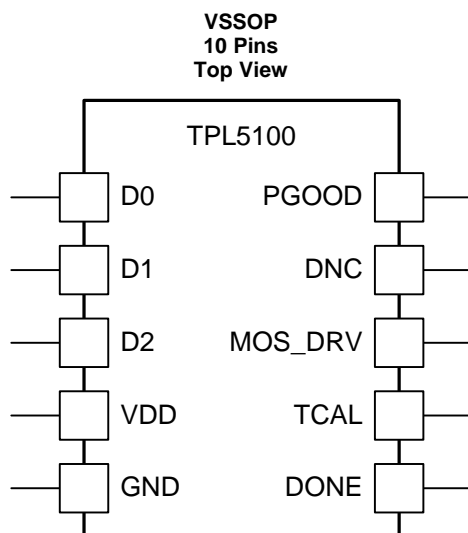
Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NAME	NO.			
D0	1	I	Logic Input to set period delay (t_{DP})	Connect to GND (low logic value) or to VDD (high logic value)
D1	2	I	Logic Input to set period delay (t_{DP})	Connect to GND (low logic value) or to VDD (high logic value)
D2	3	I	Logic Input to set period delay (t_{DP})	Connect to GND (low logic value) or to VDD (high logic value)
VDD	4	P	Supply voltage	
GND	5	G	Ground	
DONE	6	I	Logic input for Watchdog functionality	
TCAL	7	O	Short duration pulse output for estimation of TPL5100 timer delay.	
MOS_DRV	8	O	Drives external MOSFET to power cycle the remaining system.	
DNC	9	–	Do Not Connect	Leave this pin floating
PGOOD	10	I	Digital power good input	

6 Specifications

6.1 Absolute Maximum Ratings[(1)(2)]

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	-0.3	6	V
Input voltage	-0.3	VDD+0.3	V
Voltage between any two pins [(3)]	-0.3	VDD+0.3	V
Input Current on any pin	-5	5	mA
Junction Temperature, T_J[(4)]		150	°C
Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to ground unless otherwise noted.
(3) When the input voltage (VIN) at any pin exceeds the power supply (VDD), the current on that pin must not exceed 5 mA and the voltage must also not exceed 6.0 V.
(4) The maximum power dissipation is a function of TJ(MAX), ÎˌJA, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is PDMAX = (TJ(MAX) - TA)/ ÎˌJA. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Ratings

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	1.8	5.0	V
Temperature Range	-40	105	°C

6.4 Thermal Information

THERMAL METRIC[(1)]	TPL5100	UNIT
	VSSOP	
	10 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	196.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics[1]

Specifications are for $T_A = T_J = 25°C$, VDD-GND=2.5 V, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN[2]	TYP[3]	MAX[2]	UNIT
POWER SUPPLY						
IVDD	Supply current[4]	PGOOD=VDD		30	50	nA
		PGOOD=GND		12		nA
TIMER						
t_{DP}	Timer Delay Period			16, 32, 64, 100, 128, 256, 512, 1024		s
	Timer Delay Period drift over life time[5]			0.06 %		
	Timer Delay Period drift over temperature			400		ppm/°C
t_{CAL}	Calibration pulse width		14.063	15.625	17.188	ms
	t_{DP} to t_{CAL} matching error[6]	VDD<=3.0 V			0.1%	
t_{DONE}	DONE Pulse width[6]		100			ns
t_{MOS_DRV}	MOS_DRV Pulse width			31.25		ms
DIGITAL LOGIC LEVELS						
VIH	Logic High Threshold	PGOOD, DONE	0.7xVDD			V
VIL	Logic Low Threshold	PGOOD, DONE			0.3xVDD	V
VOH	Logic output High Level	MOS_DRV, TCAL Iout = 100 uA	VDD-0.3			V
		MOS_DRV, TCAL Iout = 1 mA	VDD-0.7			V
VOL	Logic output Low Level	MOS_DRV, TCAL Iout = -100 uA			0.3	V
		MOS_DRV, TCAL Iout = -1 mA			0.7	V

(1) *Electrical Characteristics* table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$.
(2) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) The supply current doesn't take in account load and pull-up resistor current. Input pins are at GND or VDD.
(5) Operational life time test procedure equivalent to 10 years.
(6) Ensured by design.

6.6 Timing Requirements TCAL, MOS_DRV, DONE, PGOOD

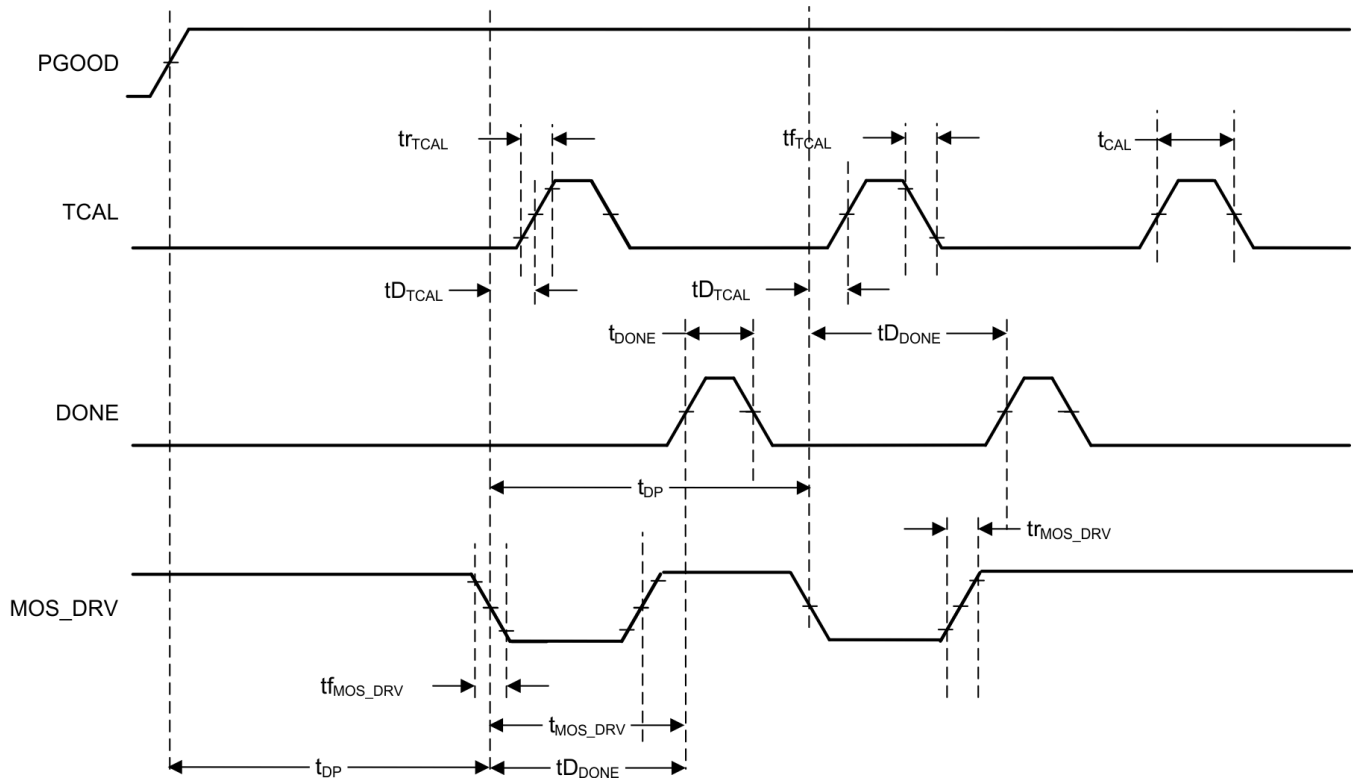|			MIN	NOM	MAX	UNIT
tr_{TCAL}	Rise Time TCAL	Capacitve load 15 pF		50		ns
tf_{TCAL}	Fall Time TCAL	Capacitve load 15 pF		50		ns
tr_{MOS_DRV}	Rise Time MOS_DRV	Capacitve load 50 pF		4		ns
tf_{MOS_DRV}	Fall Time MOS_DRV	Capacitve load 50 pF		50		ns
tD_{DONE}	DONE to MOS_DRV delay	Min delay		100		ns
		Max delay		t_{DP}-5 × t_{CAL}		ms
tD_{TCAL}	TCAL to MOS_DRV delay			t_{CAL}/2		ms

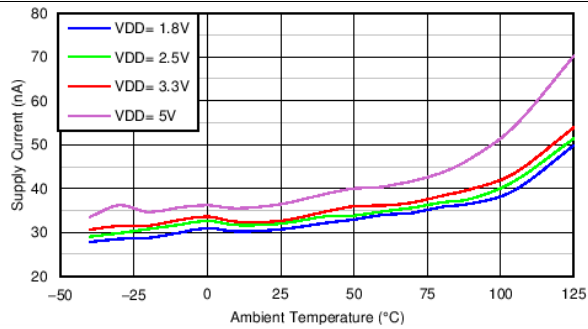**Figure 1. Timing Diagram**

6.7 Typical Characteristics
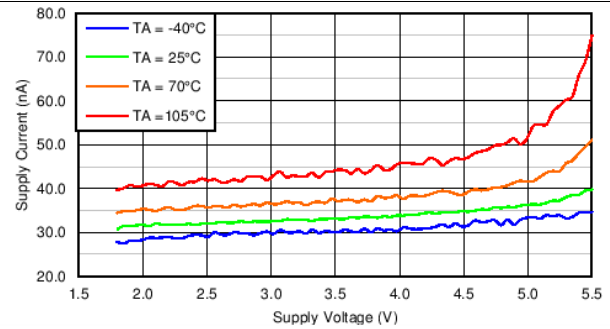

Figure 2. I$_{DD}$ vs Temperature
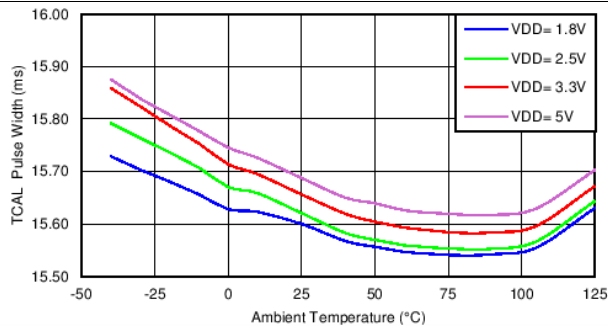
Figure 3. I$_{DD}$ vs V$_{DD}$

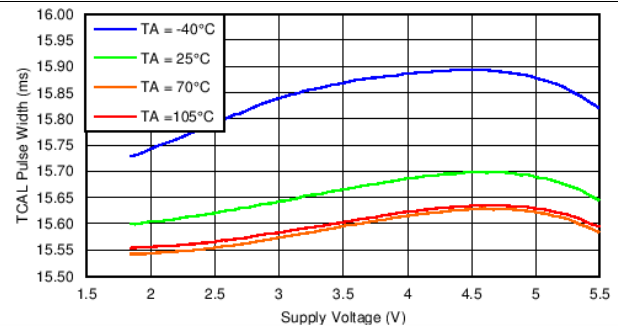Figure 4. TCAL Pulse Width vs Temperature

Figure 5. TCAL Pulse Width vs V$_{DD}$

7 Detailed Description

7.1 Overview

The TPL5100 is a long-term timer for low-power applications. The TPL5100 is designed for use in power cycled applications and provides selectable timing from 16 s to 1024 s. An additional feature is interfacing which is achieved through the TPL5100 to a power-management IC.

7.2 Functional Block Diagram
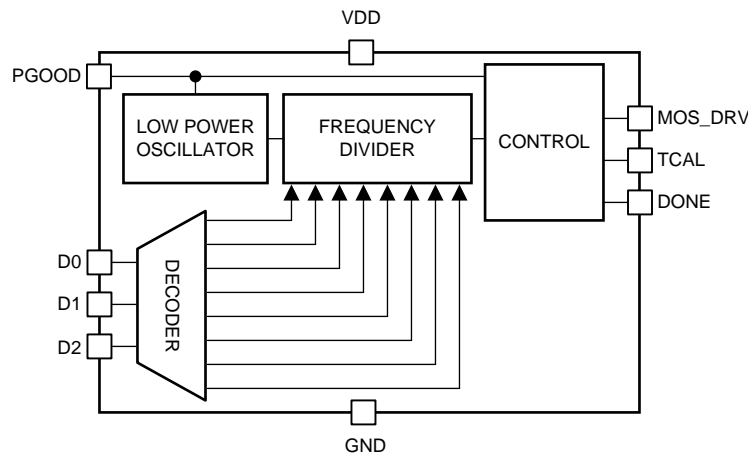
7.3 Feature Description

7.3.1 Supervisor Feature

A critical event that can corrupt the memory of a microcontroller is a voltage supply drop (supply lower than minimum operating range), and a reset of the microcontroller is mandatory if this occurs. Since the TPL5100 is the right choice in systems which stay most of the time in deep sleep or completely OFF, due to its ultra-low power consumption, it is fundamental that it takes into account the voltage drop events. The TPL5100 implements the supervisor feature when working with some power-management ICs, which indicate the status of the supply voltage with a power-good or battery-good output. The supervisory functionality is enabled by simply connecting the Battery management power-good output to the TPL5100 PGOOD pin. If this feature is not used connect the PGOOD pin to VDD.

In case the power-management IC detects a voltage drop while the microcontroller is OFF, consequently lowering the PGOOD line, the TPL5100 resets its internal counter and does not allow the micro to turn ON until the PGOOD is high again. This series of events allows the microcontroller to avoid working in an unsafe voltage supply condition. If the PGOOD signal is lowered while the microcontroller is ON, the TPL51000 turns the microcontroller OFF. The micro will be turned ON when PGOOD is high again and the selected delay is elapsed.

7.3.2 Calibration Pulse

The TPL5100 is based on an ultra-low power oscillator, which has a relatively low frequency and low accuracy; however, it shows very good cycle-to-cycle repeatability and very low temperature drift. In most of the applications, the accuracy of the oscillator is enough, but if a more accurate measure of the delay period is required, it is possible to measure the base period of the internal oscillator. A single pulse, which has the same duration as the base period of the internal oscillator, is present at the TCAL pin of the TPL5100. This pulse starts after a half period of the internal oscillator, from the falling edge of the MOS_DRV pulse.

A microcontroller-connected to the TPL5100 can routinely measure the width of the TCAL pulse, using a counter and an external crystal. Once the base period of the TPL5100 is measured, the actual time delay is calculated by multiplying the measured period by a factor, N (see Table 1), dependent upon the nominal selected time delay.

The resolution and the accuracy of the measurement depend upon the external crystal. Since the frequency of the internal oscillator of the TPL5100 is very stable, the measurement of the calibration pulse is suggested only when a high gradient of ambient temperature is observed. The measurement of the TCAL pulse is useful in battery-powered applications that implement a precise battery life counter in the microcontroller.

Feature Description (continued)

7.3.2.1 Overview of the Timing Signals MOS_DRV, TCAL, and DONE

Figure 6 shows the timing of PGOOD, MOS_DRV, and TCAL with respect to DONE. The frame, A, shows a typical sequence after the PGOOD, low to high, transition. As soon as PGOOD is high, the internal oscillator is powered ON. At the end of the delay period (t_{DP}), a MOS enable signal (MOS_DRV), followed by a calibration pulse, TCAL, is sent out. The calibration pulse starts after a half period of the internal oscillator from the falling edge of the MOS_DRV signal, and lasts one internal oscillator period. A "DONE" signal is received before the end of the MOS_DRV pulse. As soon as the TPL5100 receives the DONE signal, the counter resets and MOS_DRV and TCAL return to default conditions (MOS_DRV signal high and TCAL signal low).

The frame, B, shows a non-standard sequence. A "DONE" signal has not been received before the end of the MOS_DRV pulse. The MOS_DRV signal stays low for 2 internal oscillator periods. The calibration pulse starts after a half period of the internal oscillator from the falling edge of the MOS_DRV signal, and lasts one internal oscillator period. The external power gating MOS stays ON for 2 internal oscillator periods.

The frame, C, shows a standard sequence, but in this case, the TPL5100 receives the DONE signal when MOS_DRV is high and TCAL pulse is still high. As soon as the TPL5100 recognizes the DONE signal, the counter resets and MOS_DRV and TCAL return to default conditions (MOS_DRV signal high and TCAL signal low).The external power-gating MOS stays ON for the execution time of the program of the connected microcontroller.

The frame, D, shows a typical PGOOD, high to low transition. As soon as PGOOD is low, the internal oscillator is powered OFF and the digital output pins, TCAL and MOS_DRV, are asynchronously reset by the falling edge of the PGOOD signal, such that TCAL resets at low logical values, while MOS_DRV resets at a high logical value. The external power gating MOS stays ON less than the execution time of the program of the connected microcontroller.
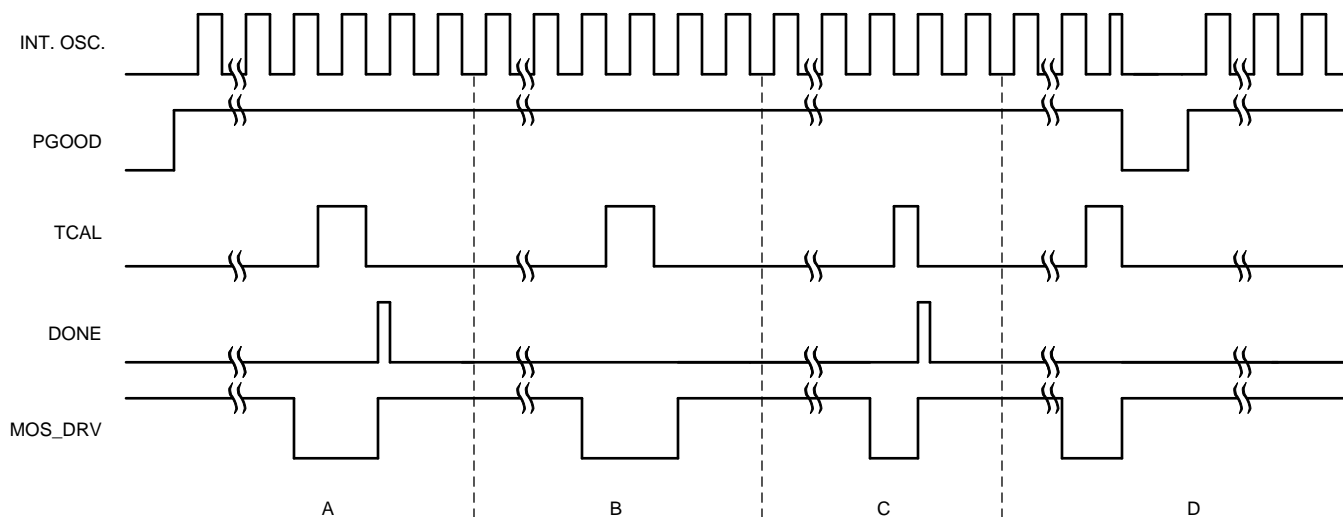

Figure 6. Timing MOS_DRV, TCAL

7.3.3 Configuration and Interface

The time interval between 2 adjacent pulses is selectable through 3 digital input pins (D0, D1, D2) that can be strapped to either VDD (1) or GND (0). Eight possible time delays can be selected, as shown in Table 1.

Table 1. Timer Delay Period

D2	D1	D0	Time (s)	Factor N
0	0	0	16	2^{10}
0	0	1	32	2^{11}
0	1	0	64	2^{12}
0	1	1	100	$100*2^{6}$

Feature Description (continued)

Table 1. Timer Delay Period (continued)

D2	D1	D0	Time (s)	Factor N
1	0	0	128	2^{13}
1	0	1	256	2^{14}
1	1	0	512	2^{15}
1	1	1	1024	2^{16}

7.4 Device Functional Modes

The TPL5100 is a long-term timer with a watchdog feature for low-power applications. The TPL5100 is designed for use in interrupt-driven applications and provides selectable timing from 1 s to 64 s. An additional supervisor feature is achieved through interfacing the TPL5100 to a power-management IC.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

In battery powered applications the design of the system is driven by low-current consumption. The TPL5100 is suitable in the applications where there is the needs to monitor environment conditions in remote site at long fixed timer interval. Occasionally in these applications the micro is kept on to enable the watchdog and count the elapsed time. Often due to the high frequency clock of the microcontrollers, a special structure must be configured to count for several seconds. The TPL5100 can mimic the same job, by completely turning off the micro and sometimes the entire power channel; this results in burning only tens of nA.

8.2 Typical Application

The TPL5100 can be used in environment sensor nodes such as humidity and temperature sensor node. The sensor node has to measure the humidity and the temperature and transmit the data through a low power RF micro such as the CC2530. Since the temperature and the humidity in home application do not change so fast, the measurement and the transmission of the data can be done at very low rate, such as every 30 seconds. The RF micro should spend most of the time in counting the elapsed time, but using the TPL5100 it is possible to complete turn off the RF micro and enlarge the battery life. The TPL5100 will turn on the RF micro when the programmed timer interval elapses.
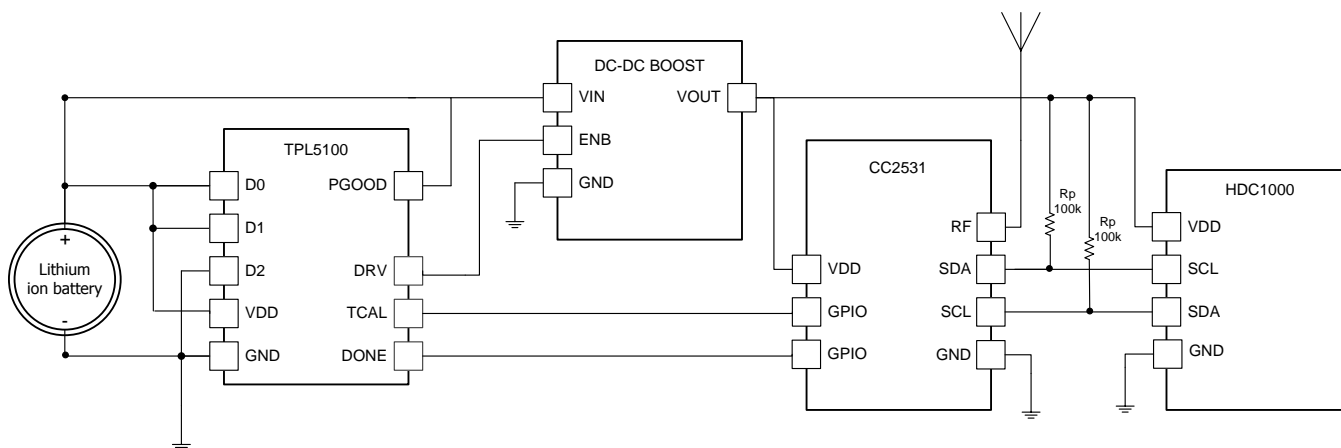

Figure 7. Sensor Node

8.2.1 Design Requirements

The design is driven by the low current consumption constraint. The data are usually acquired at a rate between 30 s to 60 s. The highest necessity is the maximization of the battery life. The TPL5100 helps achieve this goal because it allows turning off the RF micro.

8.2.2 Detailed Design Procedure

When the focal constraint is the battery life, the selection of a low-power voltage regulator and low-leakage MOSFET to power gate the microcontroller is mandatory. The first step in the design is the calculation of the power consumption of each device in the different mode of operations. An example is the HDC1000, in measurement mode the RF micro is in normal operation and transmission. The different modes offer the possibility to select the appropriate timer interval which respect the application constraint and maximize the life of the battery.

Typical Application (continued)
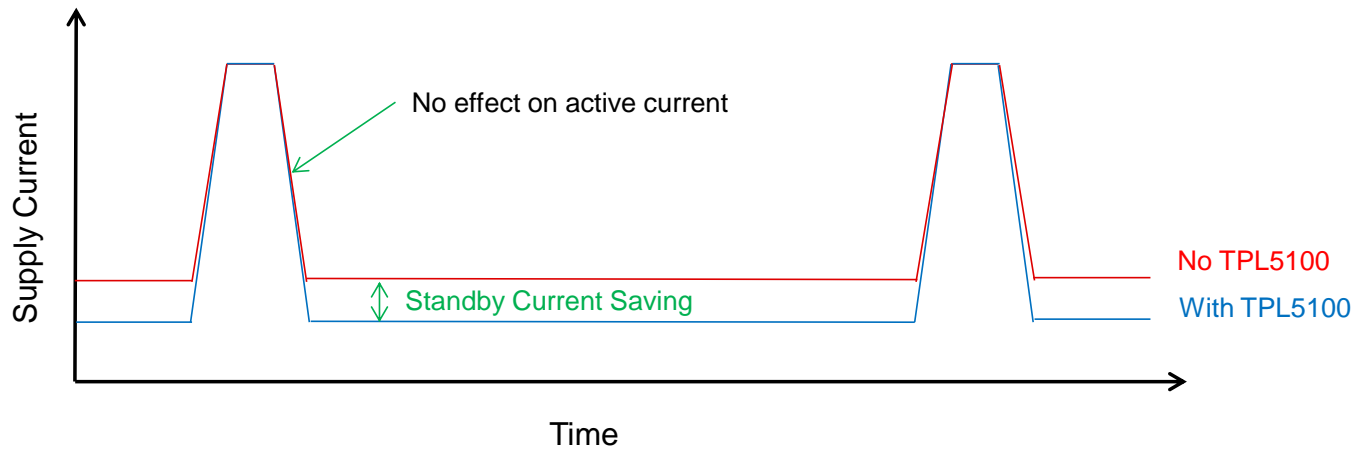
8.2.3 Application Curve

Figure 8. Effect of TPL5100 on Current Consumption

9 Power Supply Recommendations

The TPL5100 requires a voltage supply within 2.7 V and 5.5 V. A multilayer, ceramic-bypass X7R capacitor of 0.1μF between VDD and GND pin is recommended.

10 Layout

10.1 Layout Guidelines

The more sensitive pins of the TPL5100 are the digital input pins D0, D1, D2 to select the timer interval. It is mandatory to connect them to VDD or GND through short traces avoiding series resistance. Moreover, it is mandatory to keep these pins far from traces of high frequency signals, such as clock or communication bus. Signal integrity of DRV and TCAL signal is achieved reducing parasitic capacitance on the traces between the TPL5100 and the microcontroller.

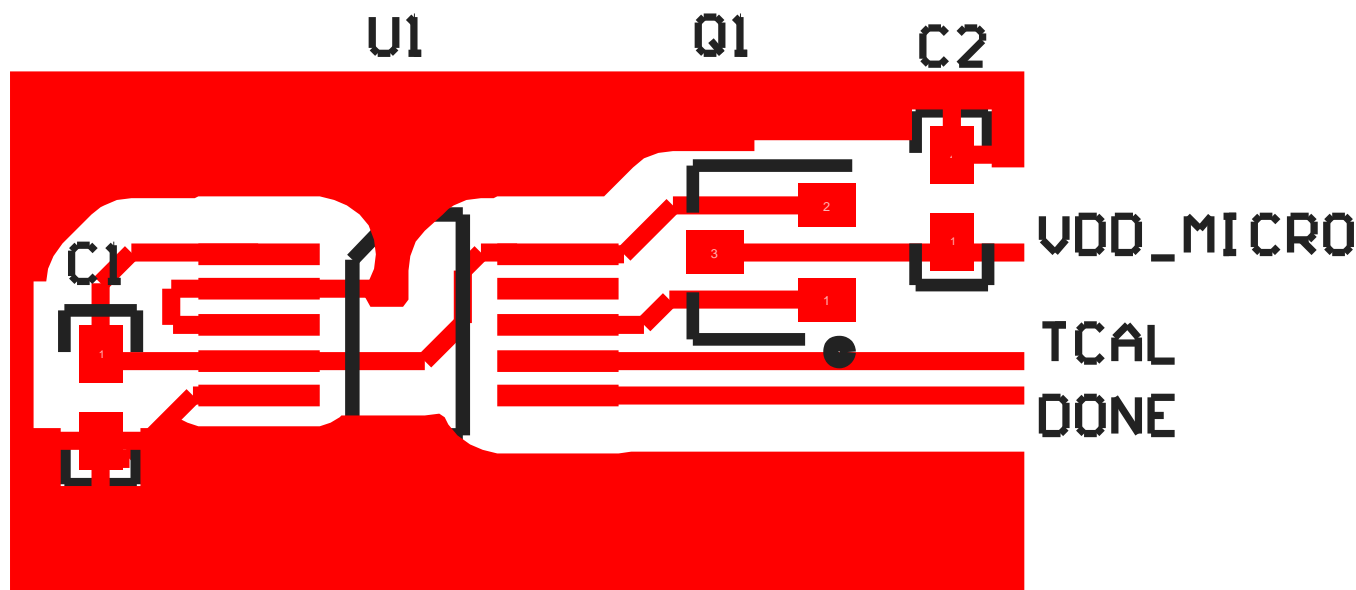## 10.2 Layout Example

Figure 9. Board Layout

11 器件和文档支持

11.1 商标

All trademarks are the property of their respective owners.

11.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPL5100DGSR	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	ASAA
TPL5100DGSR.A	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	ASAA
TPL5100DGST	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	ASAA
TPL5100DGST.A	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	ASAA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL5100DGSR	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPL5100DGST	VSSOP	DGS	10	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL5100DGSR	VSSOP	DGS	10	3500	367.0	367.0	35.0
TPL5100DGST	VSSOP	DGS	10	250	208.0	191.0	35.0

C

SEATING PLANE

5.05 TYP
4.75

A

PIN 1 ID
AREA

8X 0.5

10

2X
2

1

3.1
2.9
NOTE 3

5

6

10X 0.27
0.17

⌖ 0.1 Ⓜ C AⓈ BⓈ

⌂ 0.1 C

1.1 MAX

B

3.1
2.9
NOTE 4

SEE DETAIL A

0.23 TYP
0.13

0.25

GAGE PLANE

0° - 8°

0.7
0.4

0.15
0.05

DETAIL A
TYPICAL

4221984/A   05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
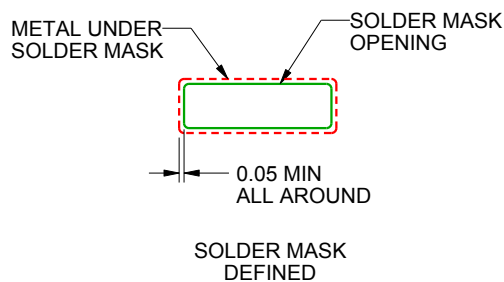5. Reference JEDEC registration MO-187, variation BA.

TEXAS INSTRUMENTS
www.ti.com

10X (1.45)

10X (0.3)

1

SYMM

(R0.05)
TYP

10

SYMM

8X (0.5)

5

6

(4.4)

LAND PATTERN EXAMPLE
SCALE:10X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221984/A   05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.