TPD4E02B04 用于 USB Type-C 和 HDMI 2.0 的 4 通道 ESD 保护二极管

1 特性

- IEC 61000-4-2 4 级静电放电 (ESD) 保护
  - ±12kV 接触放电
  - ±15kV 气隙放电
- IEC 61000-4-4 瞬态放电 (EFT) 保护
  - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
  - 2A (8/20µs)
- IO 电容：0.27pF（典型值）、0.37pF（最大值）
- 直流击穿电压：5.5V（最小值）
- 超低泄漏电流：10nA（最大值）
- 低静电放电 (ESD) 钳位电压：5A 传输线路脉冲 (TLP) 时为 8.8V
- 支持速率高达 10Gbps 的高速接口
- 工业温度范围：–40°C 至 125°C
- 简易直通布线封装

2 应用

- 终端设备
  - 便携式计算机和台式机
  - 机顶盒
  - 电视和监视器
  - 手机和平板电脑
  - 数字视频录像机 (DVR) 和网络视频录像机 (NVR)
- 接口
  - USB Type-C
  - USB 3.1 第 2 代
  - 高清多媒体接口 (HDMI) 2.0/1.4
  - USB 3.0
  - DisplayPort 1.3
  - PCI Express 3.0

3 说明

TPD4E02B04 是一款双向瞬态电压抑制器 (TVS) ESD 保护二极管阵列，用于为 USB Type-C 和 HDMI 2.0 电路提供保护。TPD4E02B04 的额定 ESD 冲击消散值等于 IEC 61000-4-2（4 级）国际标准中规定的最高水平。

该器件 的每条 通道具有一个 0.27pF IO 电容，适用于保护速率高达 10Gbps 的高速接口（例如 USB 3.1 第 2 代）。低动态电阻和低钳位电压可针对瞬变事件提供系统级保护。

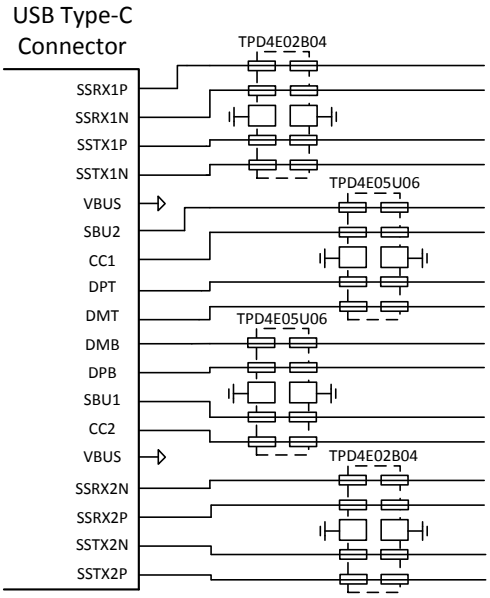
TPD4E02B04 采用符合工业标准的 USON-10 (DQA) 封装。该封装 采用 直通布线，其引脚间距为 0.5mm，能够简化应用实现并缩短设计时间。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD4E02B04	USON (10)	2.50mm x 1.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



目录

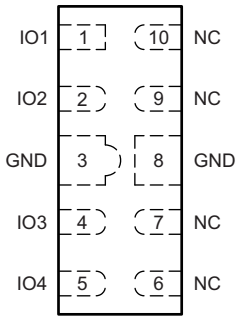
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (Novemeber 2015) to Revision A	Page
• 已将器件状态由“*产品预览*”更改为“*量产数据*”	1

5 Pin Configuration and Functions

DQA Package
10-Pin USON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	3	Ground	Ground. Connect to ground.
GND	8	Ground	
IO1	1	I/O	ESD Protected Channel
IO2	2		
IO3	4		
IO4	5		
NC	6	NC	Not Connected; Used for optional straight-through routing. Can be left floating or grounded.
NC	7		
NC	9		
NC	10		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Electrical Fast Transient	IEC 61000-4-5 (5/50 ns)		80	A
Peak Pulse	IEC 61000-4-5 Power (t_p - 8/20 µs)		17	W
	IEC 61000-4-5 Current (t_p - 8/20 µs)		2	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	
	IEC 61000-4-2 contact discharge	±12000	
	IEC 61000-4-2 air-gap discharge	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–3.6	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPD4E02B04 DQA (USON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	348.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	214.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	270.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	81.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	270.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	-3.6		3.6	V
V_{BRF}	Breakdown Voltage, any IO pin to GND (1)	I_{IO} = 1 mA, T_A = 25°C	5.5	6.4	7.5	V
V_{BRR}	Breakdown Voltage, GND to any IO pin (1)	I_{IO} = 1 mA, T_A = 25°C	-5.5	-6.4	-7.5	V
V_{HOLD}	Holding voltage (2)	I_{IO} = 1 mA		5.8		V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND		6.6		V
		I_{PP} = 5 A, TLP, from IO to GND		8.8		
		I_{PP} = 1 A, TLP, from GND to IO		6.6		
		I_{PP} = 5A, TLP, from GND to IO		8.8		
I_{LEAK}	Leakage current, any IO to GND	V_{IO} = ±2.5 V			10	nA
R_{DYN}	Dynamic Resistance	IO to GND		0.47		Ω
		GND to IO		0.47		
C_L	Line Capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND, T_A = 25°C		0.27	0.37	pF
ΔC_L	Variation of Line Capacitance	Delta of capacitance between any two IO pins, V_{IO} = 0 V, f = 1 MHz, T_A = 25°C, GND = 0 V		0.01	0.07	pF
C_{CROSS}	Channel to Channel Capacitance	Capacitance from one IO to another, V_{IO} = 0 V, f = 1 MHz, GND = 0 V		0.13		pF

(1) V_{BRF} and V_{BRR} are defined as the voltage when 1mA is applied in the positive-going direction, before the device latches into the snapback state
(2) V_{HOLD} is defined as the voltage when 1mA is applied in the negative-going direction, after the device has successfully latched into the snapback state

6.6 Typical Characteristics

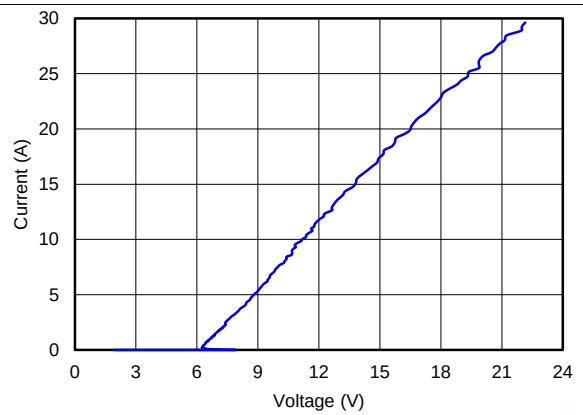


Figure 1. Positive TLP Curve

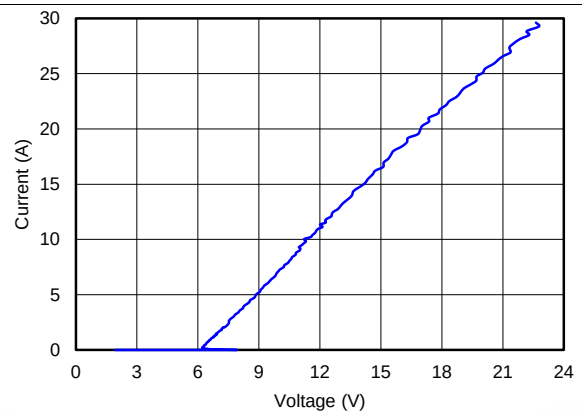


Figure 2. Negative TLP Curve

Typical Characteristics (continued)

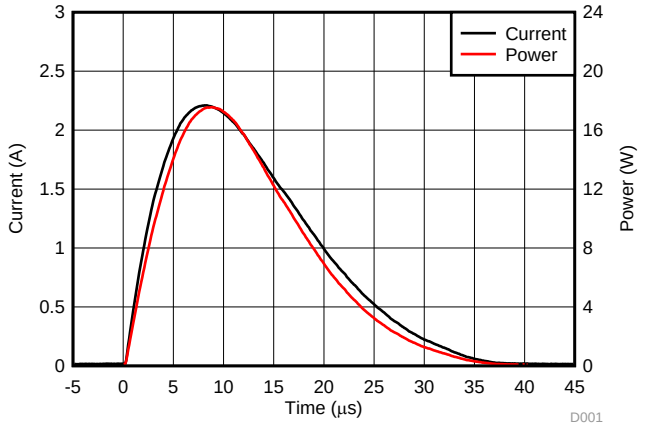


Figure 3. Surge Curve (t_p = 8/20µs), any IO pin to GND

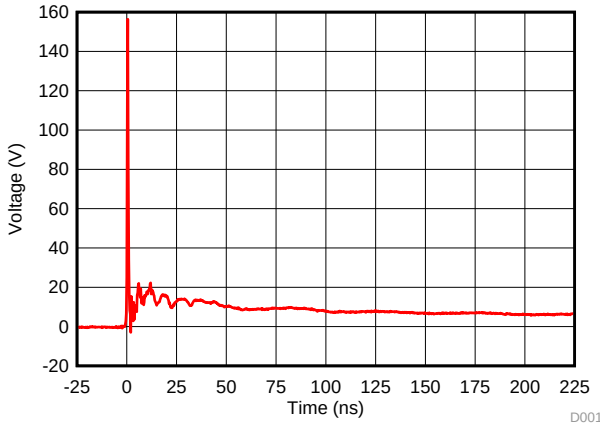


Figure 4. 8-kV IEC Waveform

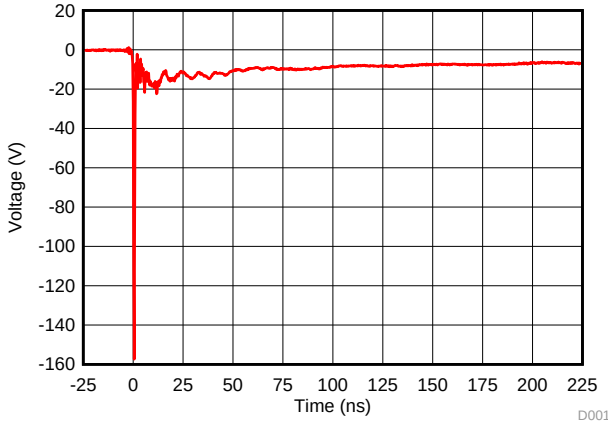


Figure 5. –8-kV IEC Waveform

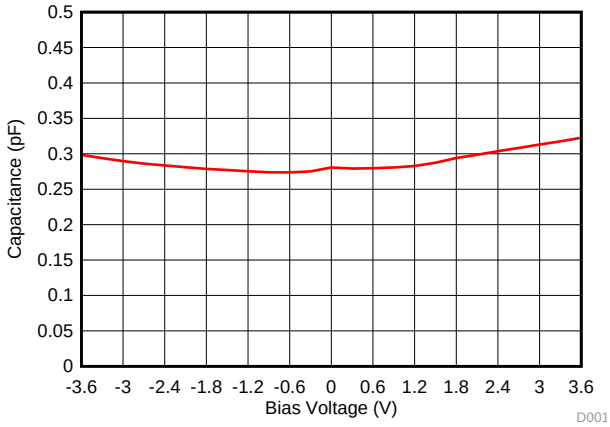


Figure 6. Capacitance vs. Bias Voltage

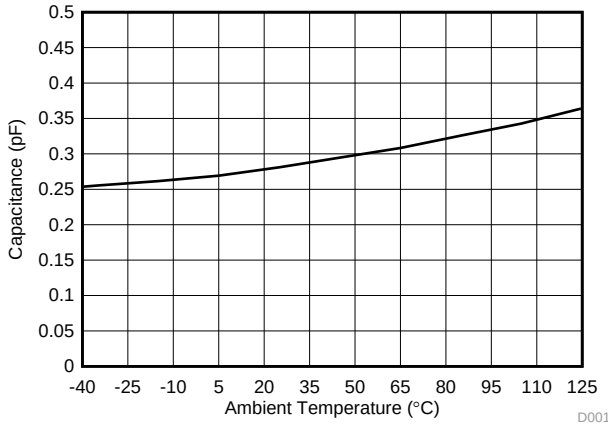


Figure 7. Capacitance vs. Ambient Temperature

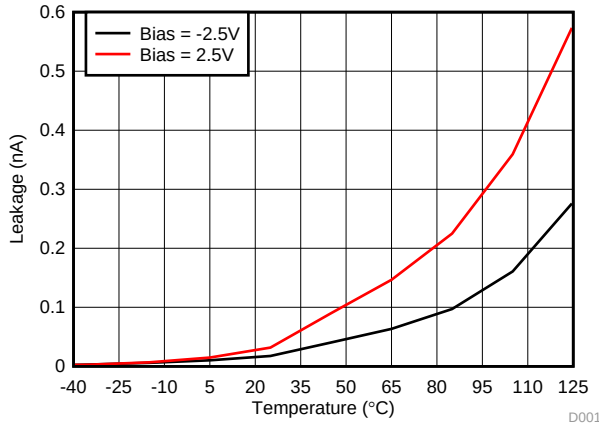


Figure 8. Leakage Current vs. Temperature

Typical Characteristics (continued)

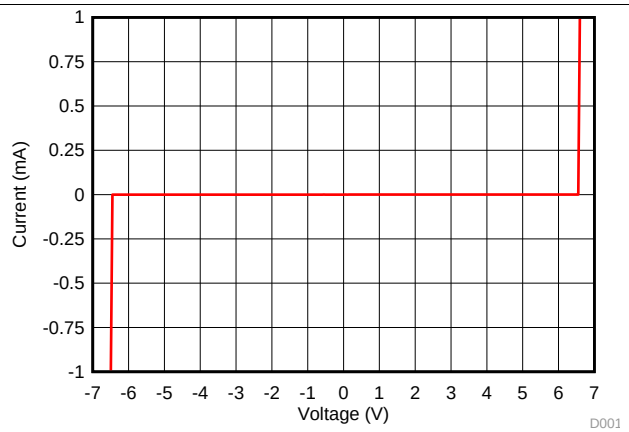


Figure 9. DC Voltage Sweep I-V Curve

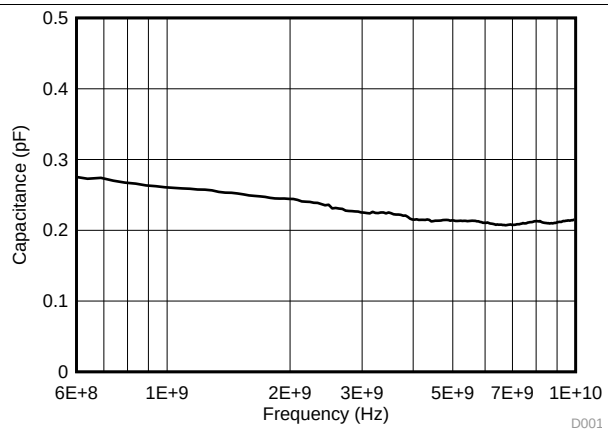


Figure 10. Capacitance vs. Frequency

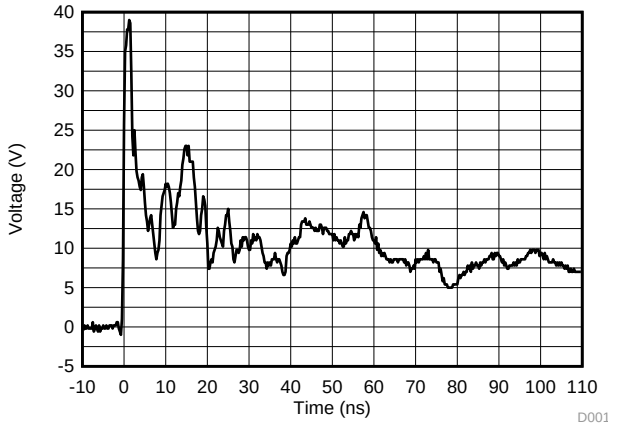


Figure 11. 8-kV IEC Waveform through 2m HDMI Cable

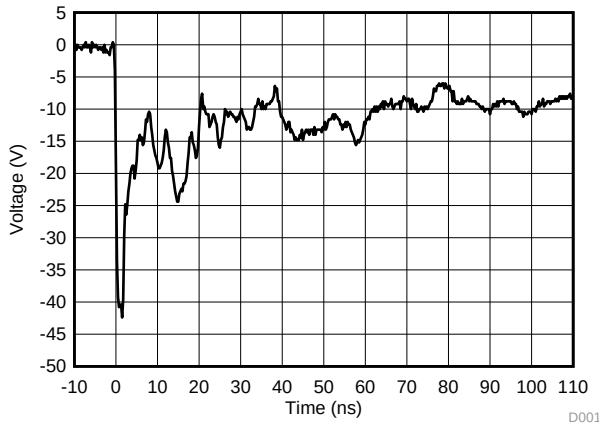


Figure 12. –8-kV IEC Waveform through 2m HDMI Cable

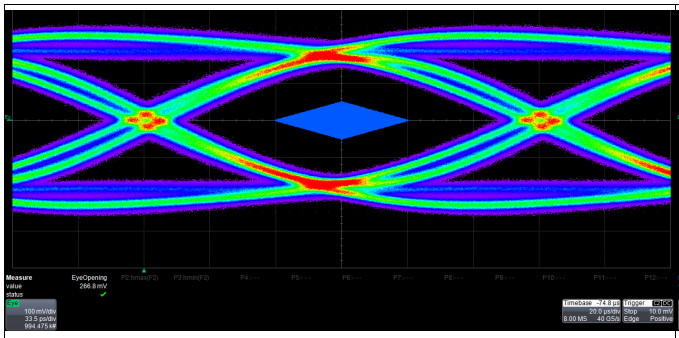


Figure 13. USB3.0 Eye Diagram (Bare Board)

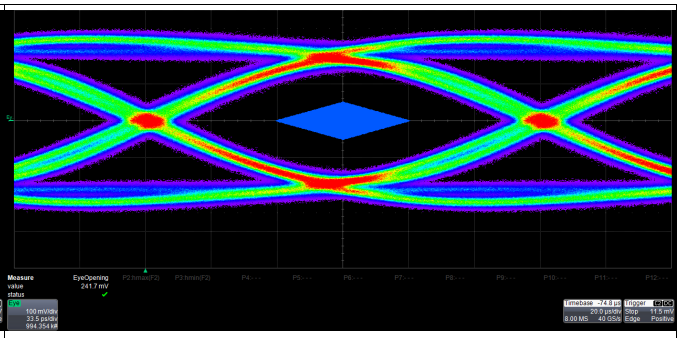


Figure 14. USB3.0 Eye Diagram (with TPD4E02B04)

Typical Characteristics (continued)

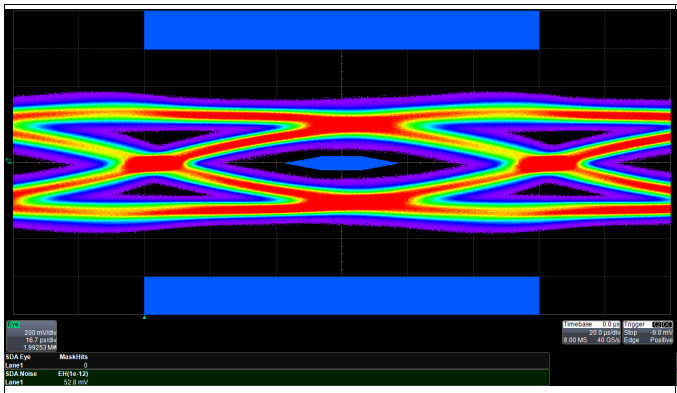


Figure 15. USB3.1 Gen 2 Eye Diagram (Bare Board)

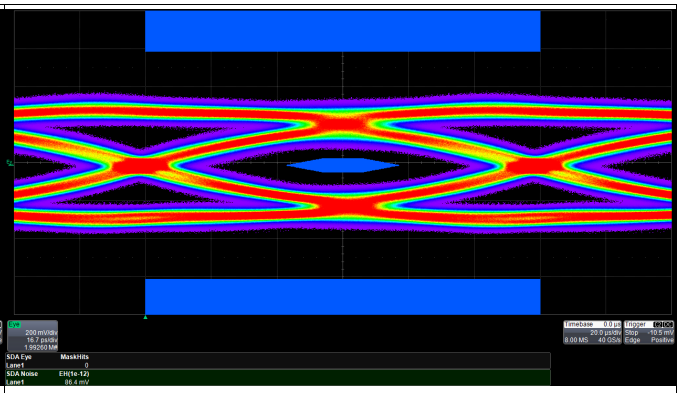


Figure 16. USB3.1 Gen 2 Eye Diagram (with TPD4E02B04)

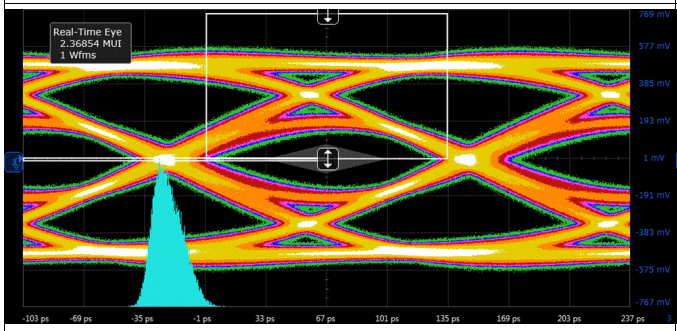


Figure 17. HDMI2.0 6Gbps TP2 Eye Diagram (Bare Board)

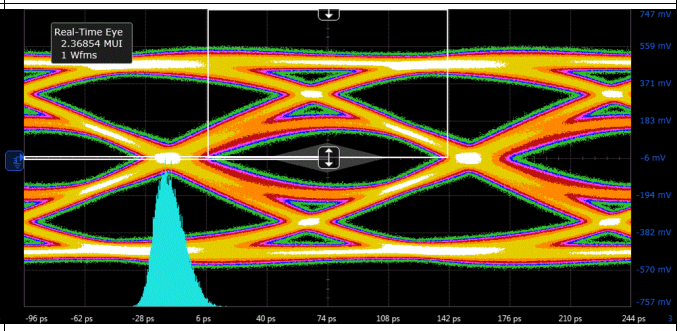


Figure 18. HDMI2.0 6Gbps TP2 Eye Diagram (with TPD4E02B04)

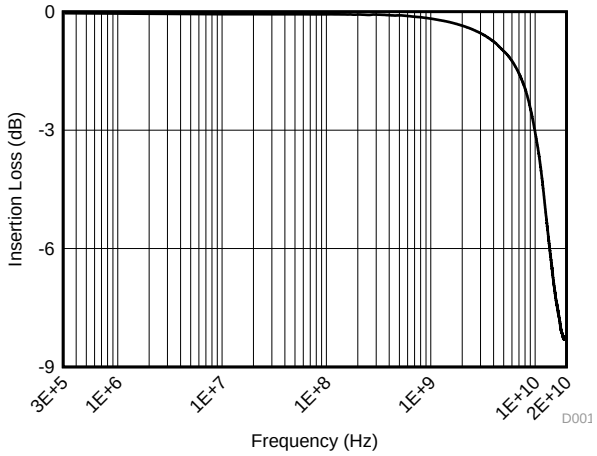


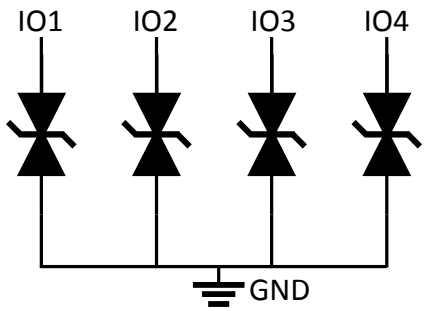
Figure 19. Differential Insertion Loss

7 Detailed Description

7.1 Overview

The TPD4E02B04 is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±12-kV contact and ±15-kV air gap. An ESD/surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50 Ω impedance). An ESD/surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2 A and 17 W (8/20 µs waveform). An ESD/surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.27 pF (typical) and 0.37 pF (maximum). This device supports data rates up to 10 Gbps.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of ±5.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

7.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (max) with a bias of ±2.5 V

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 8.8 V (I_{PP} = 5 A).

7.3.8 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 10 Gbps, because of the extremely low IO capacitance.

Feature Description (continued)

7.3.9 Industrial Temperature Range

This device features an industrial operating range of –40°C to 125°C.

7.3.10 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPD4E02B04 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±15 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD4E02B04 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4E02B04 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

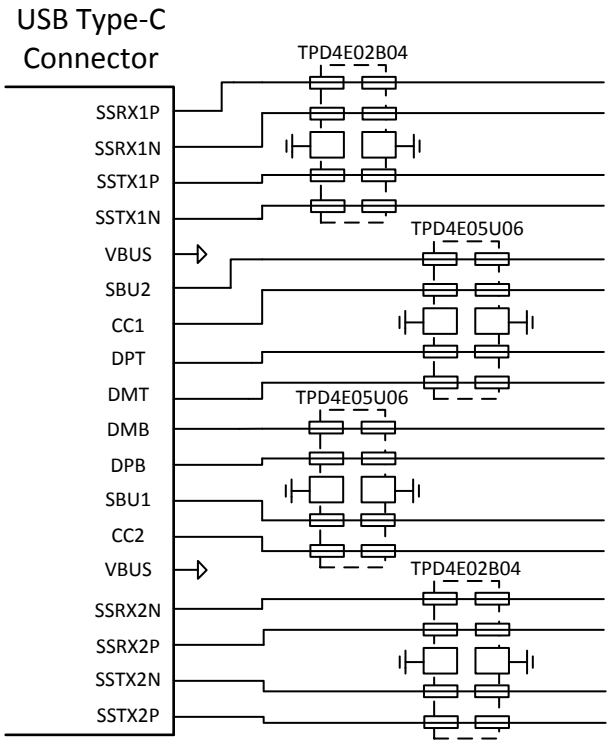


Figure 20. USB 3.1 Gen 2 Type-C ESD Schematic

Typical Application (continued)

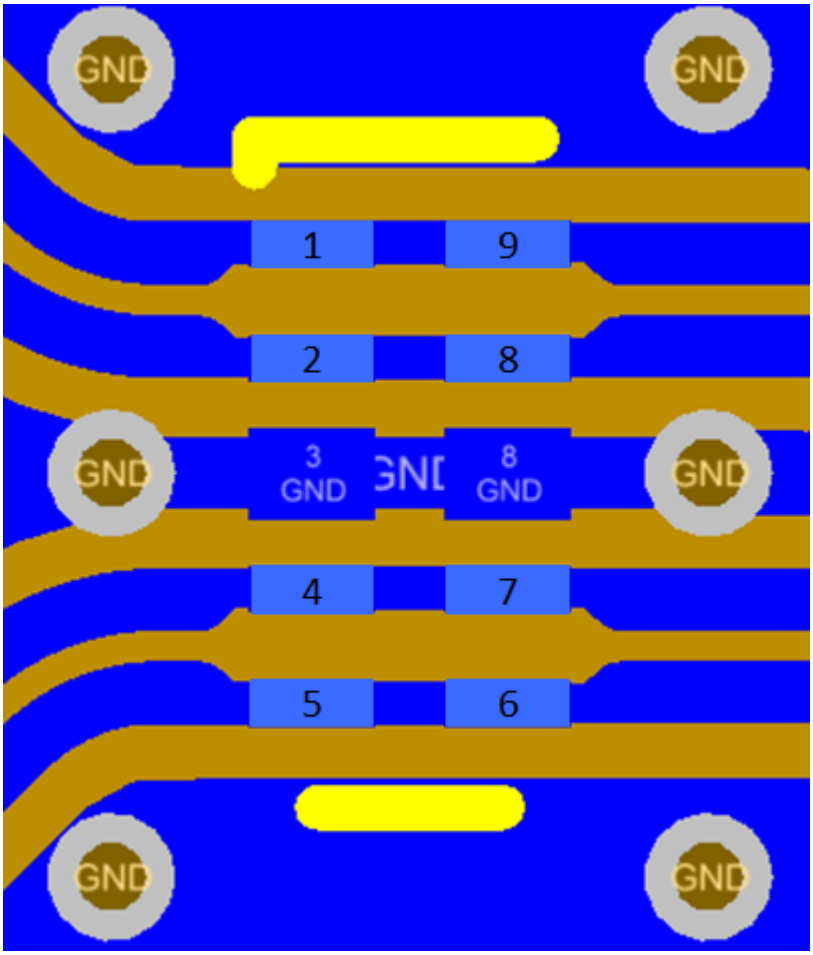


Figure 21. USB 3.1 Gen 2 SuperSpeed Layout

8.2.1 Design Requirements

For this design example two TPD4E02B04 devices and two TPD4E05U06 devices are being used in a USB 3.1 Gen 2 Type-C application. This will provide a complete ESD protection scheme.

Given the USB 3.1 Gen 2 Type-C application, the parameters listed in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal Range on SuperSpeed+ Lines	0 V to 3.6 V
Operating Frequency on SuperSpeed+ Lines	5 GHz
Signal Range on CC, SBU, and DP/DM Lines	0 V to 5 V
Operating Frequency on CC, SBU, and DP/DM Lines	up to 480 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD4E02B04 supports signal ranges between -3.6 V and 3.6 V, which supports the SuperSpeed+ pairs on the USB Type-C application. The TPD4E05U06 supports signal ranges between 0 and 5.5 V, which supports the CC, SBU, and DP/DM lines.

8.2.2.2 Operating Frequency

The TPD4E02B04 has a 0.27 pF (typ) capacitance, which supports the USB3.1 Gen 2 data rates of 10 Gbps. The layout example in Figure 21 is intended to negate some of the loading capacitance of the TPD4E02B04 by narrowing the traces slightly over the device itself. The TPD4E05U06 has a 0.5 pF (typical) capacitance, which easily supports the CC, SBU, and DP/DM data rates.

8.2.3 Application Curves

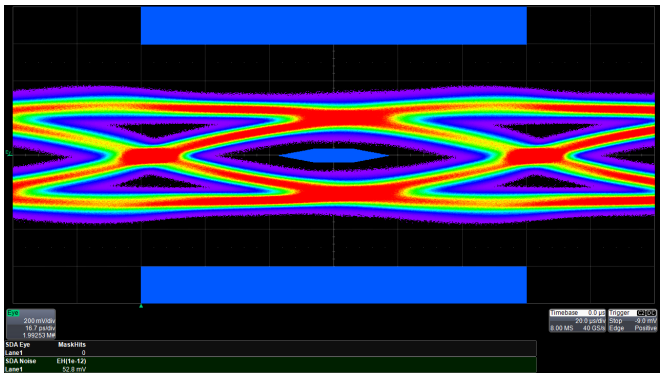


Figure 22. USB 3.1 Gen 2 10Gbps Eye Diagram (Bare Board)

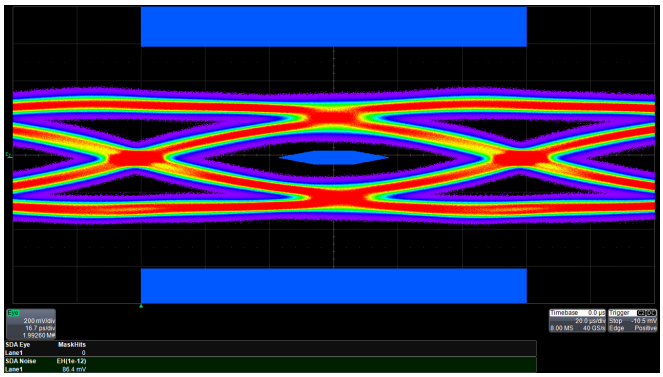


Figure 23. USB 3.1 Gen 2 10Gbps Eye Diagram (with TPD4E02B04)

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (-3.6 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Examples

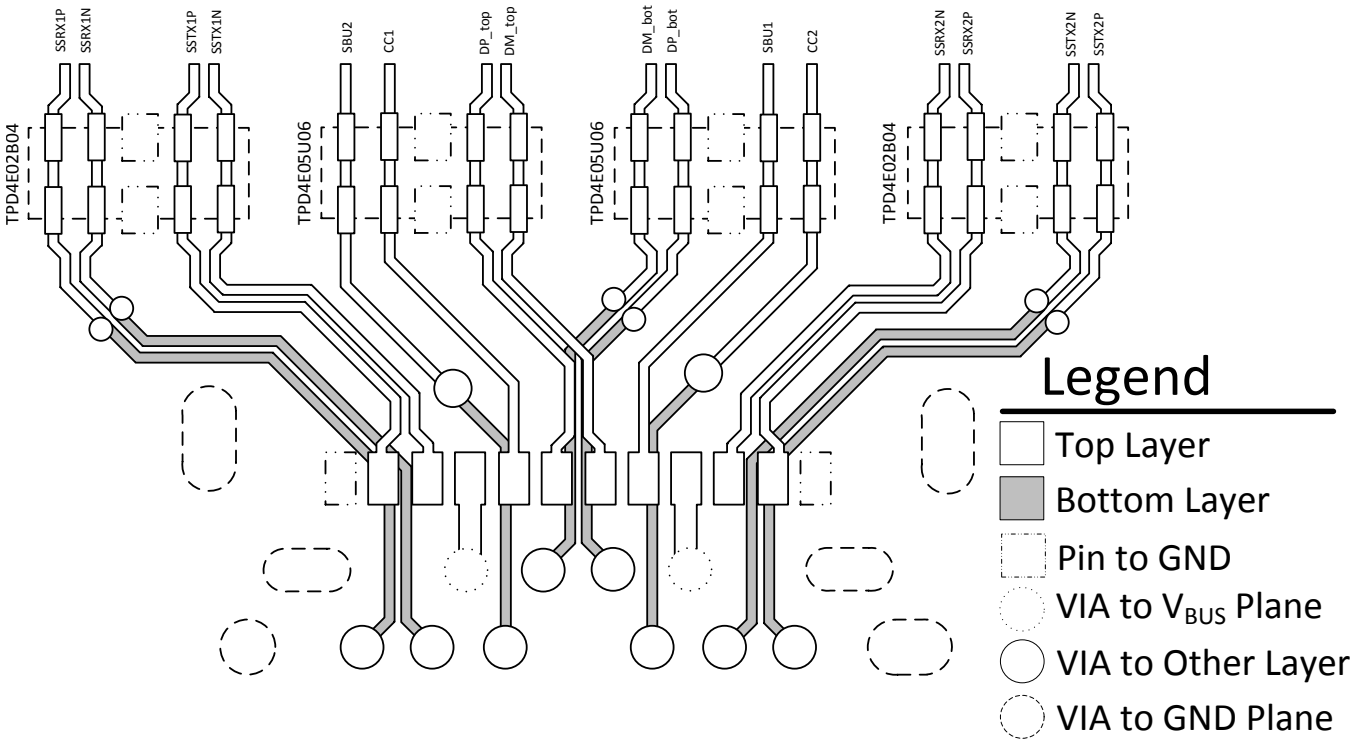


Figure 24. USB Type-C Mid-Mount, Hybrid Connector with One-Sided ESD Layout

Layout Examples (continued)

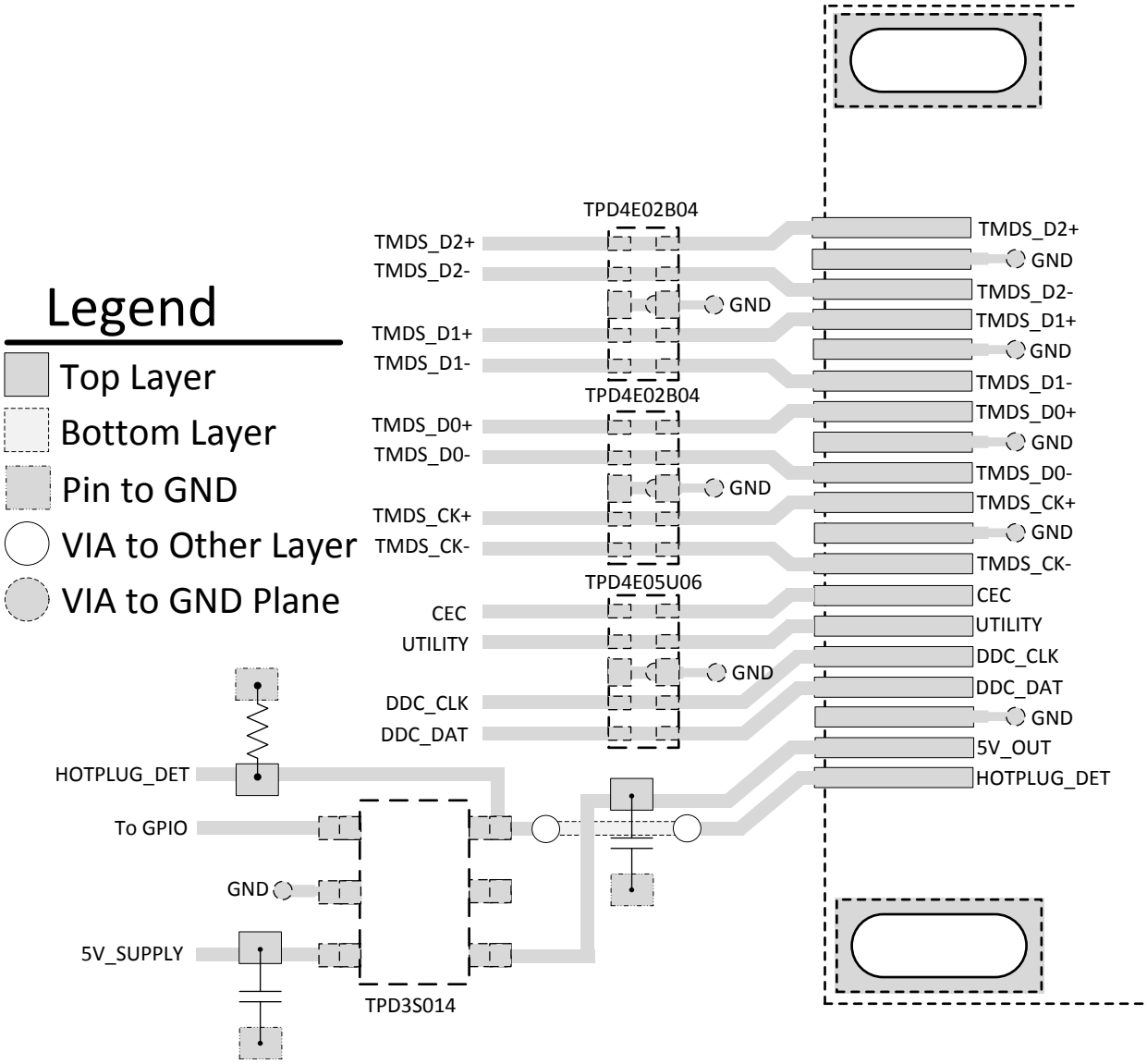


Figure 25. HDMI2.0 Type-A Transmitter Port Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档请参见以下部分：

- *《阅读并理解 ESD 保护数据表》*，SLLA305
- *《ESD 布局布线指南》*，SLVA680
- *《TPD4E02B04EVM 用户指南》*，SLVUAH6

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4E02B04DQAR	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1SG 1SY
TPD4E02B04DQAR.B	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1SG 1SY
TPD4E02B04DQARG4.B	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1SY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPD4E02B04 :

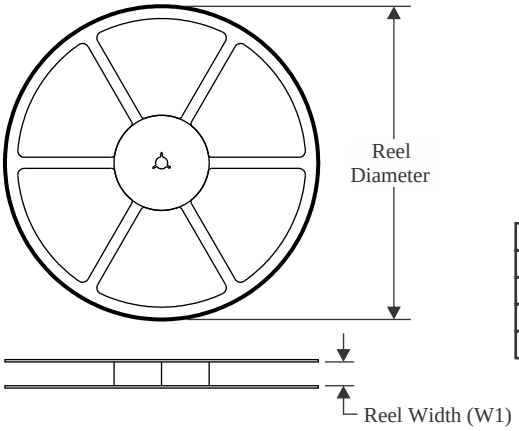
- Automotive : TPD4E02B04-Q1

NOTE: Qualified Version Definitions:

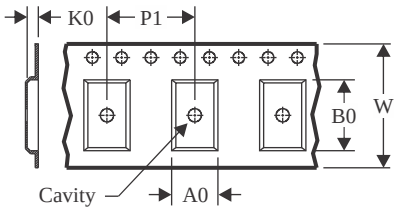
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

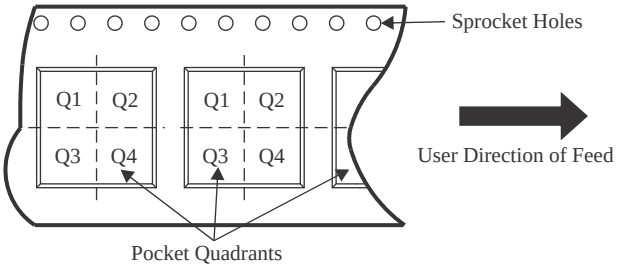


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

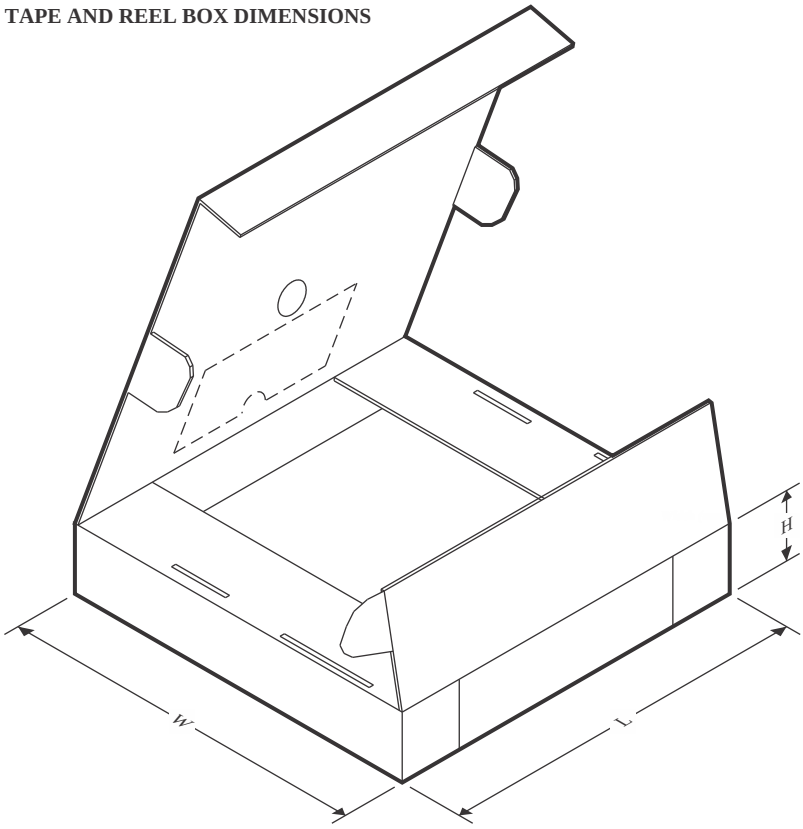
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E02B04DQAR	USON	DQA	10	3000	180.0	9.5	1.18	2.68	0.72	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E02B04DQAR	USON	DQA	10	3000	189.0	185.0	36.0

GENERIC PACKAGE VIEW

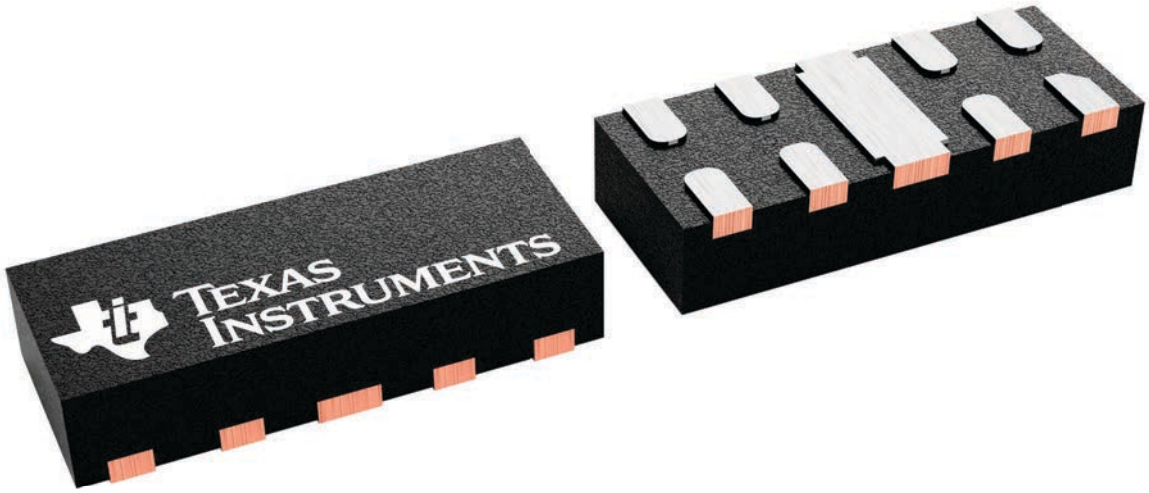
DQA 10

USON - 0.55 mm max height

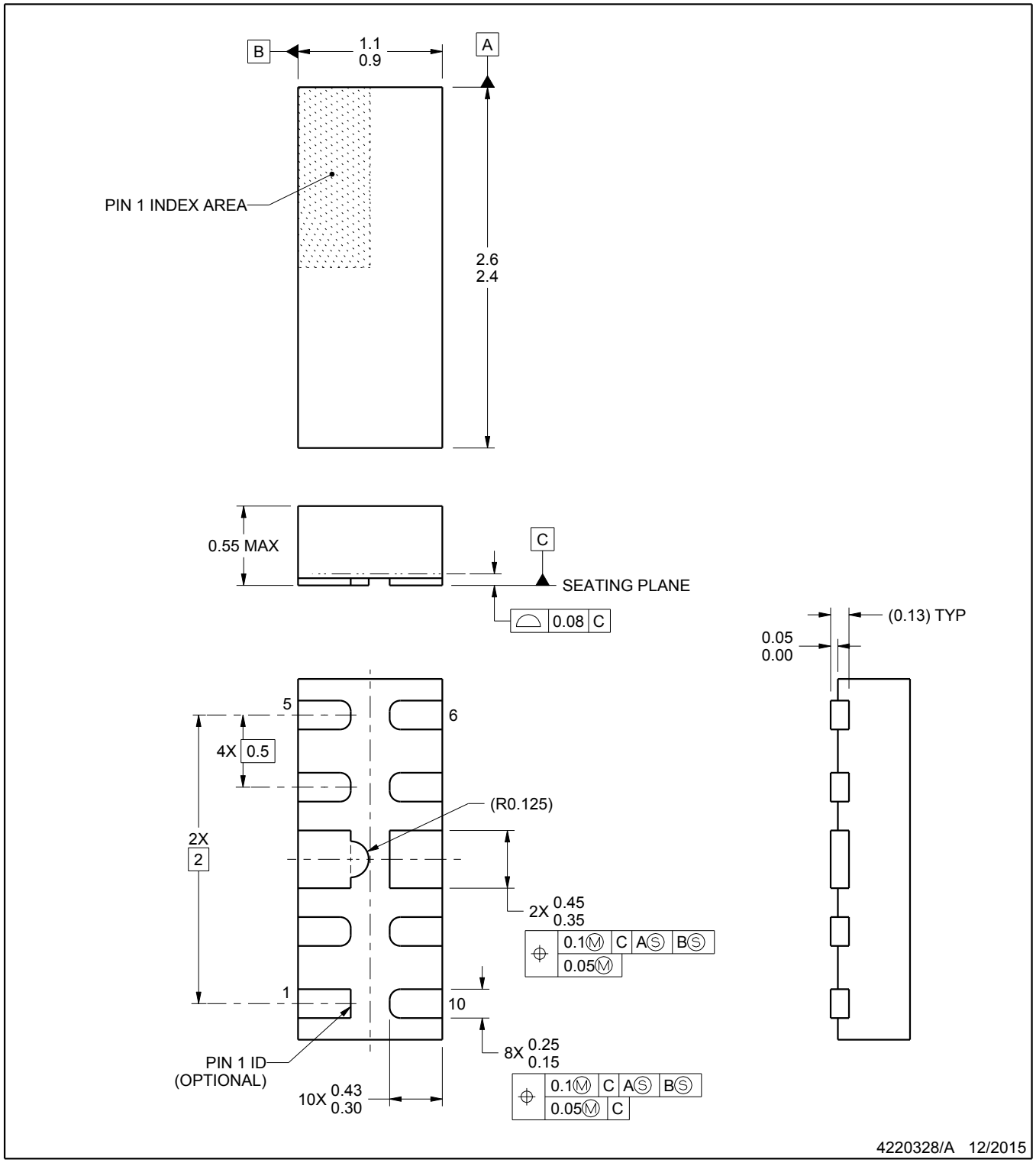
1 x 2.5, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

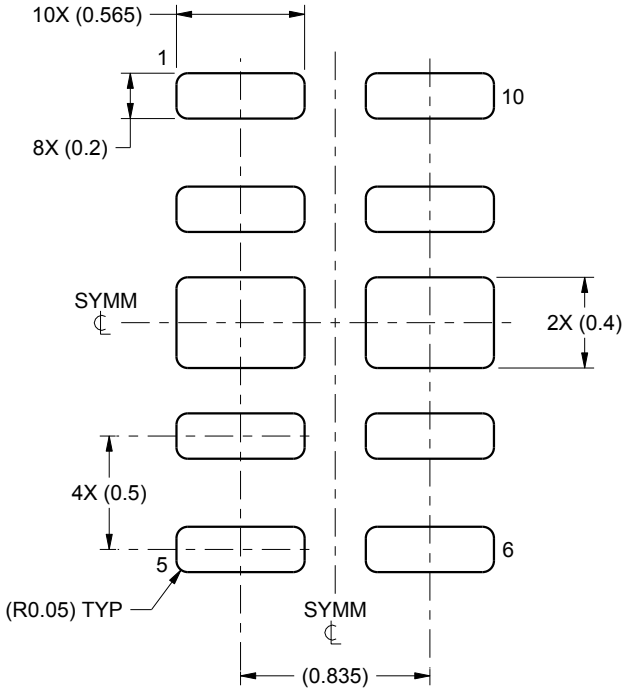


4230320/A

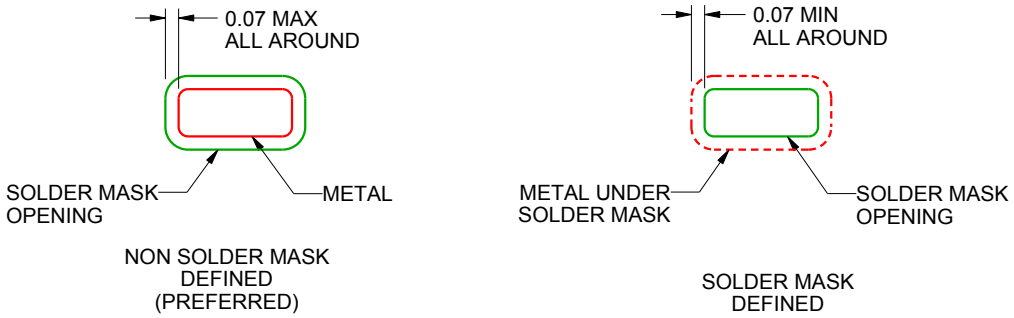


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

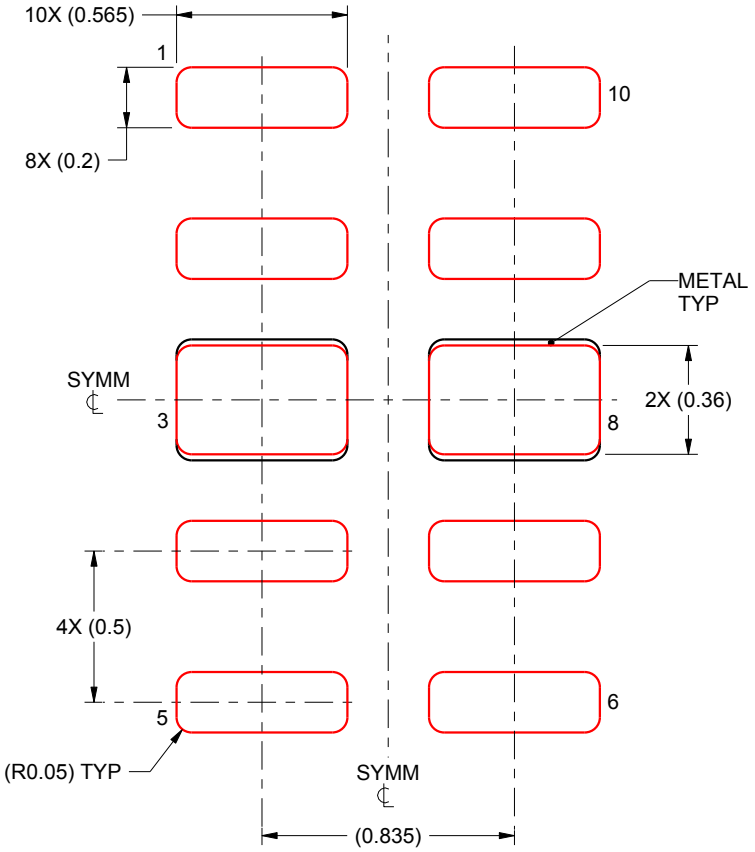


SOLDER MASK DETAILS

4220328/A 12/2015

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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