双通道高速静电放电 (ESD) 保护器件

查询样品: TPD2E1B06

特性

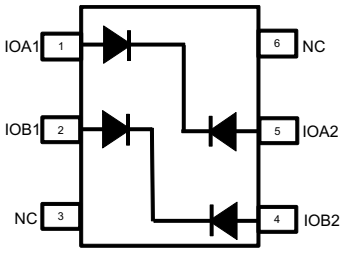
- 为低压输入输出 **(IO)** 接口提供系统级的静电放电 **(ESD)** 保护
- **IEC 61000-4-2 4** 级接触 **ESD** 额定值
- **IO** 电容值 **1pF**（典型值）
- 直流 **(DC)** 击穿电压 **7V**（最小值）
- 超低泄漏电流 **10nA**（最大值）
- 低 **ESD** 钳位电压
- 车用温度范围：**–40°C** 至 **125°C**
- 小型易于走线的 **DRL** 封装

应用范围

- 游戏机
- 电子书
- 便携式媒体播放器
- 数码摄像机

说明

TPD2E1B06 是一款双通道超低电容 ESD 保护器件。它提供 ±10KV IEC 接触 ESD 保护。 其 1pF 线路电容值使得这款器件适合于广泛应用。 典型应用接口为 USB 2.0，低压差分信令 (LVDS) 和 I2C。 有两个针对 TPD2E1B06 的常见布局布线方法并且都在应用信息部分中突出显示。



DRL
1.6 mm x 1.2 mm x 0.55mm
(0.5-mm pitch)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

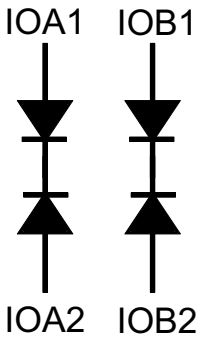


Figure 1. CIRCUIT SCHEMATIC DIAGRAM

TERMINAL FUNCTIONS

PIN		PIN TYPE	DESCRIPTION	USAGE
NAME	NO.			
IOA1	1	I/O	ESD protected channel	Please refer to the Application Information Section.
IOA2	5	I/O		
IOB1	2	I/O		
IOB2	4	I/O		
NC	3, 6	NC	No connect	Can be left floating, grounded, or connected to VCC

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	Operating temperature range	–40 to 125	°C
	Storage temperature	–65 to 155	°C
	IEC 61000-4-2 contact ESD(1)	±10	kV
I_{PP}	Peak pulse current (tp = 8/20μs)(1)	2.5	A
P_{PP}	Peak pulse power (tp = 8/20μs)(1)	35	W

(1) Using Routing Option 1 or 2 as shown in Figure 2 or Figure 3.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		TPD2E1B06 DRL (6) PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	349.7	ºC/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	120.5	
θ_{JB}	Junction-to-board thermal resistance	171.4	
ψ_{JT}	Junction-to-top characterization parameter	10.8	
ψ_{JB}	Junction-to-board characterization parameter	169.4	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage				5.5	V
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 1 A, TLP, I/O to GND (1)(2)		11		V
		I_{PP} = 5 A, TLP, I/O to GND (1)(2)		15		V
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 1 A, TLP, GND to I/O (1)(2)		11		V
		I_{PP} = 5 A, TLP, GND to I/O (1)(2)		15		V
R_{DYN}	Dynamic resistance			0.9		Ω
C_{L1}	Pin 2 and 5 capacitance	Pin 1 and 4 = GND, f = 1MHz, V_{BIAS} = +2.5V (2)(3)		0.85		pF
C_{L2}	Pin 1 and 4 capacitance	Pin 2 and 5 = GND, f = 1MHz, V_{BIAS} = +2.5V (2)(4)		1.05		pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA	7		9.5	V
I_{LEAK}	Leakage current	V_{BIAS} = +2.5 V		1	10	nA

(1) Transmission line pulse with rise time 10ns and pulse width 100ns.
(2) T_A = 25°C
(3) Using Routing Option 1, Figure 2.
(4) Using Routing Option 2, Figure 3.

APPLICATION INFORMATION

There are 2 channels of back-to-back diodes in TPD2E1B06DRL. The device should be routed in one of the two ways shown below. Routing option 1 is recommended because TPD2E1B06 is designed to maximize signal integrity in this configuration while still comply with IEC 61000-4-2 level 4 contact ESD rating.

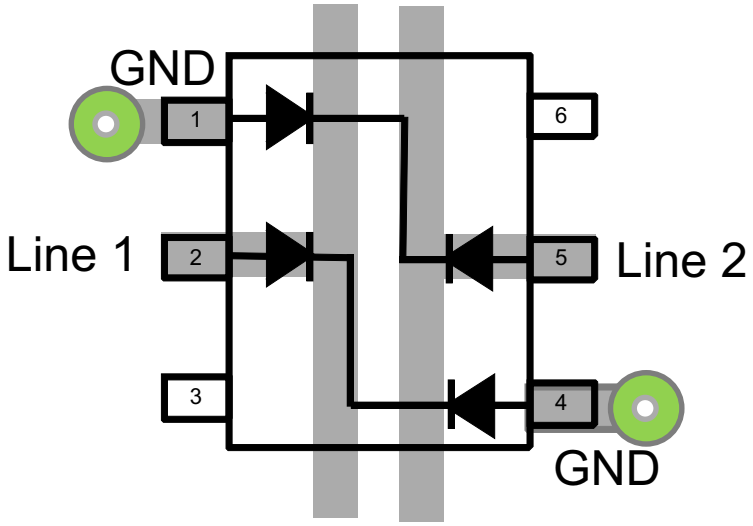


Figure 2. Routing Option 1

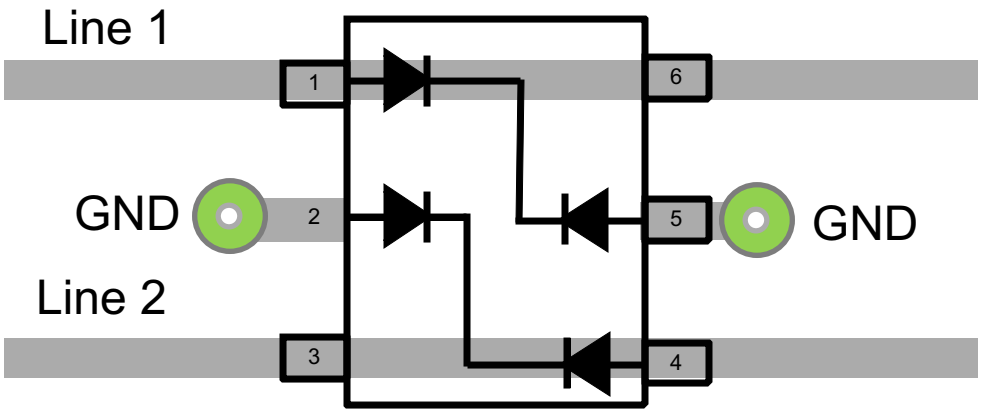


Figure 3. Routing Option 2

REVISION HISTORY

Changes from Original (July 2013) to Revision A	Page
• 将文档从预览改为生产数据。	1

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD2E1B06DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(DUH, DUL) DUG
TPD2E1B06DRLR.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(DUH, DUL) DUG
TPD2E1B06DRLRG4	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DUL
TPD2E1B06DRLRG4.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DUL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

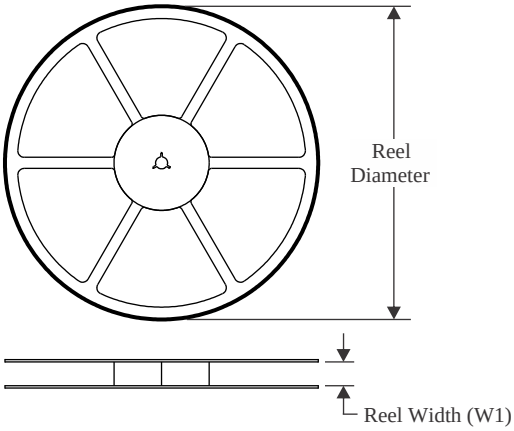
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

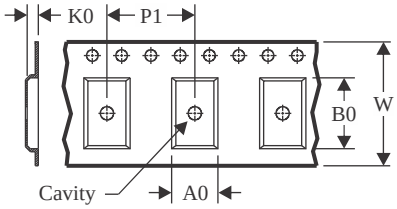
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

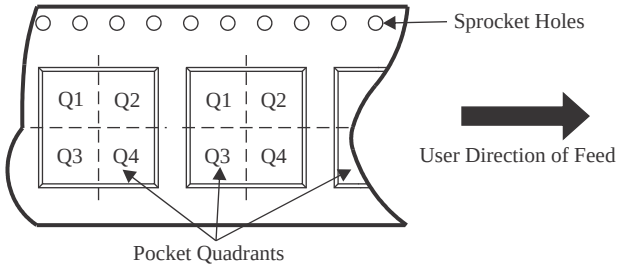


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

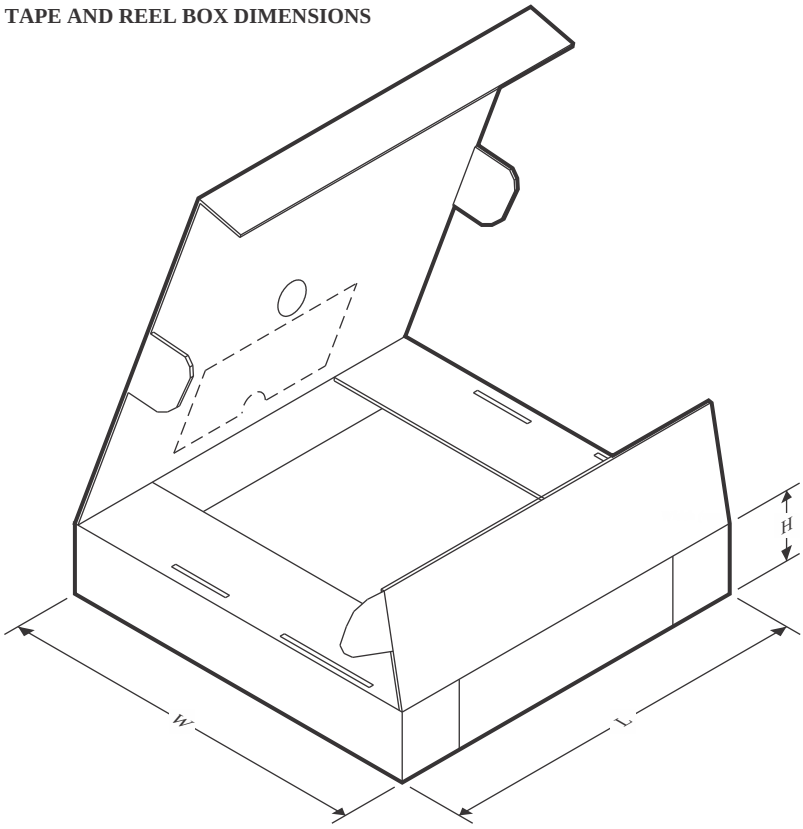
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E1B06DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPD2E1B06DRLRG4	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

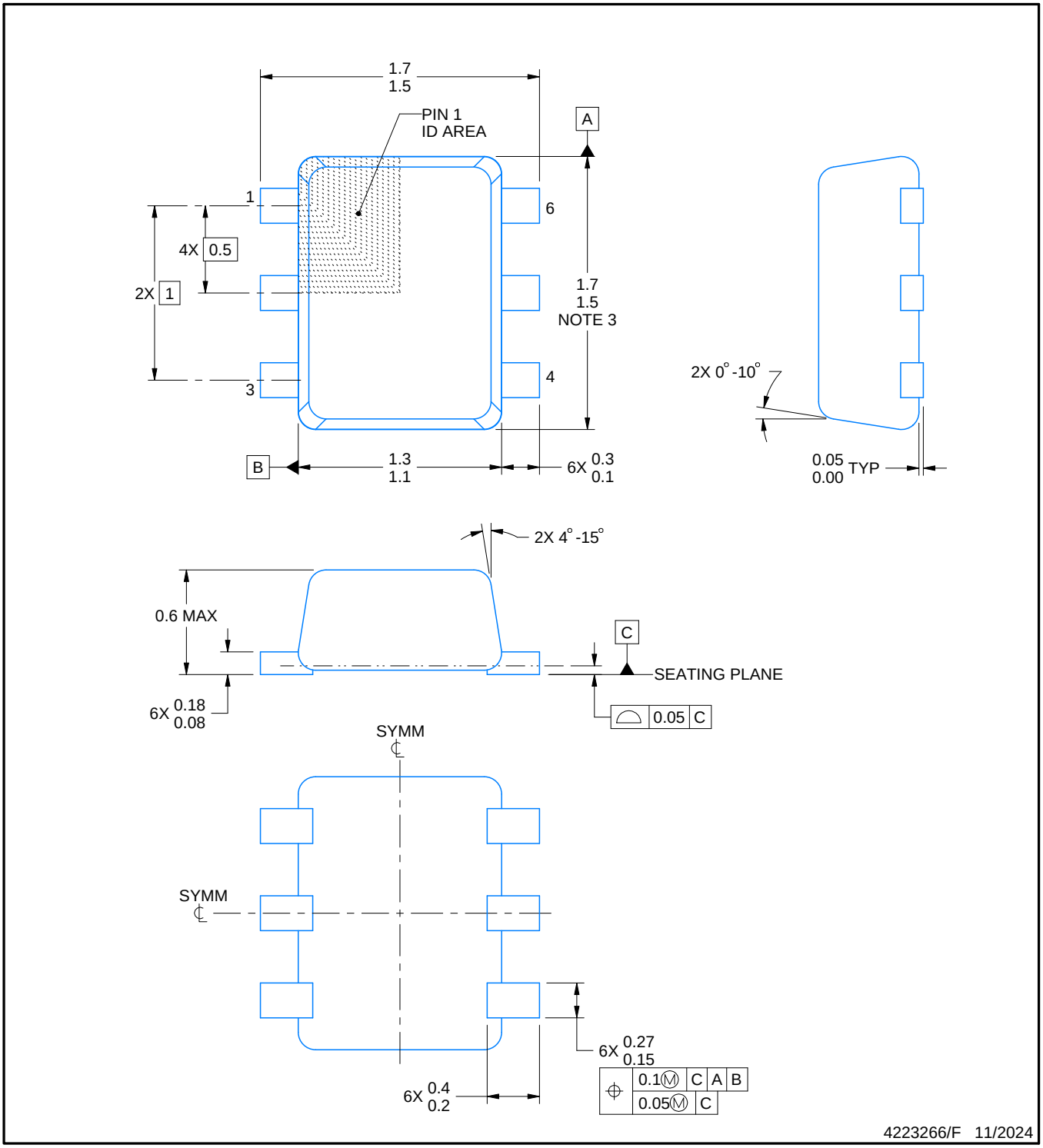
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E1B06DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPD2E1B06DRLRG4	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

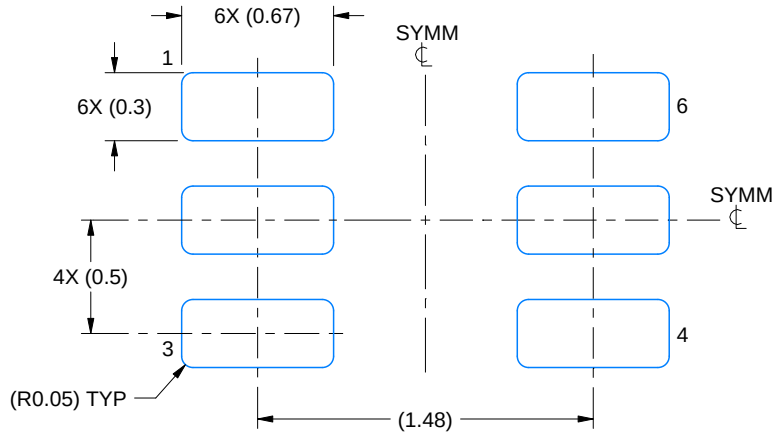
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

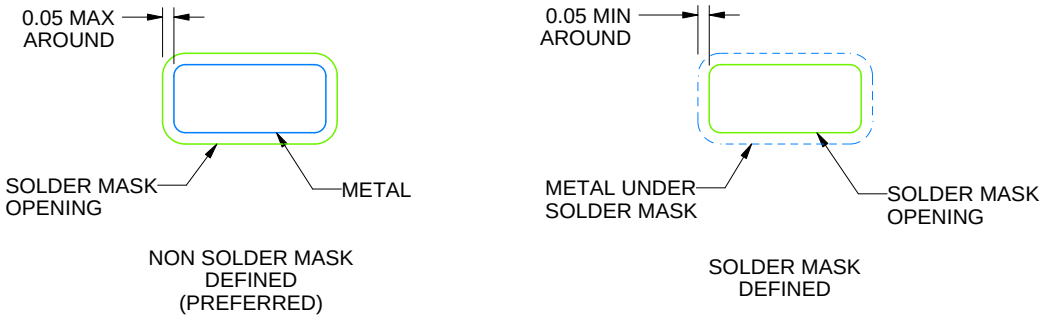
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

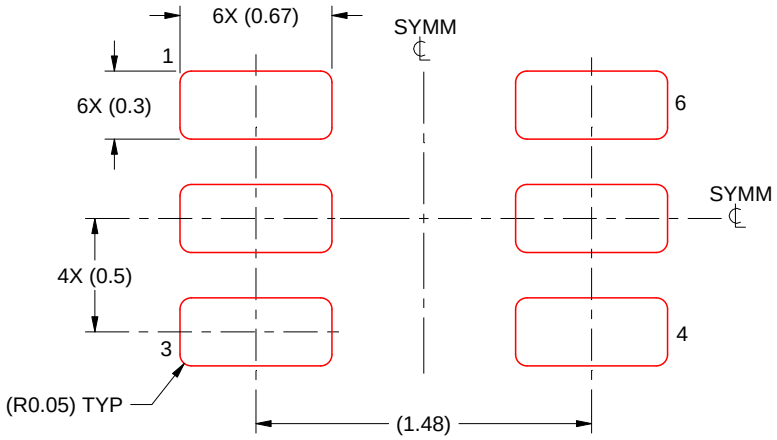
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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