www.ti.com.cn ZHCSBQ5A – OCTOBER 2013 – REVISED OCTOBER 2013

支持静电放电 (ESD)，用于 V_{BUS_CON} 引脚的 USB 充电器过压保护 (OVP) 开关

查询样品: **TPD1S414**

特性

- V_{BUS_CON} 上的输入直流电压保护高达 **30V**
- 低 R_{ON} **nFET** 开关支持主机和充电模式
- 耐受高达 **100V** 开路浪涌电压（按照 **IEC61000-4-5** 标准）
- 内部 **15ms** 启动延迟
- 内部 **30ms** 软启动延迟以最大限度地减小 **USB** 涌入电流
- **ESD** 性能 V_{BUS_CON}
  - **±15kV** 接触放电 **(IEC 61000-4-2)**
  - **±15kV** 空气间隙放电 **(IEC 61000-4-2)**
- 集成输入启用和状态输出信号
- 热关断特性
- 节省空间的晶圆芯片级 **(WCSP)** 封装 **(1.4mm x 1.89mm)**

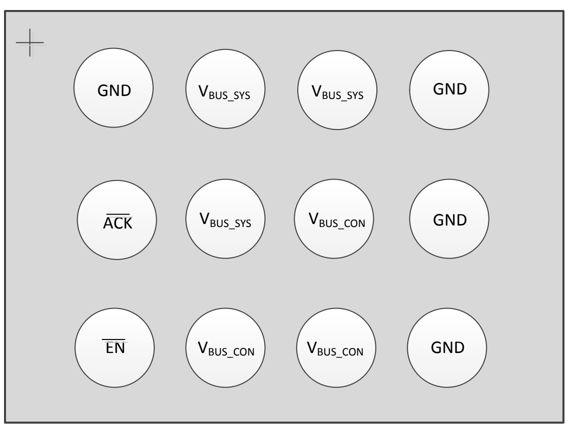
应用范围

- 手机
- 电子书
- 便携式媒体播放器

说明

TPD1S414 是一款用于 USB 连接器的 V_{BUS} 线路保护的单芯片解决方案。 此双向 nFET 开关在保护内部系统电路不受任何 V_{BUS_CON} 引脚上过压情况影响的同时，可确保充电和主机模式下的安全电流流量。 在 V_{BUS_CON} 引脚上，这个器件能够处理高达 30V 超压保护。在 $\overline{EN}$ 引脚切换为低电平时，TPD1S414 在接通 nFET 之前通过一个软启动延迟来等待 20ms。 $\overline{ACK}$ 引脚表示 FET 完全接通。

YZ PACKAGE
(TOP VIEW - SEE THROUGH)



12-YZ Pin Mapping

	1	2	3	4
A	GND	V_{BUS_SYS}	V_{BUS_SYS}	GND
B	$\overline{ACK}$	V_{BUS_SYS}	V_{BUS_CON}	GND
C	$\overline{EN}$	V_{BUS_CON}	V_{BUS_CON}	GND

English Data Sheet: SLLSEH9

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM

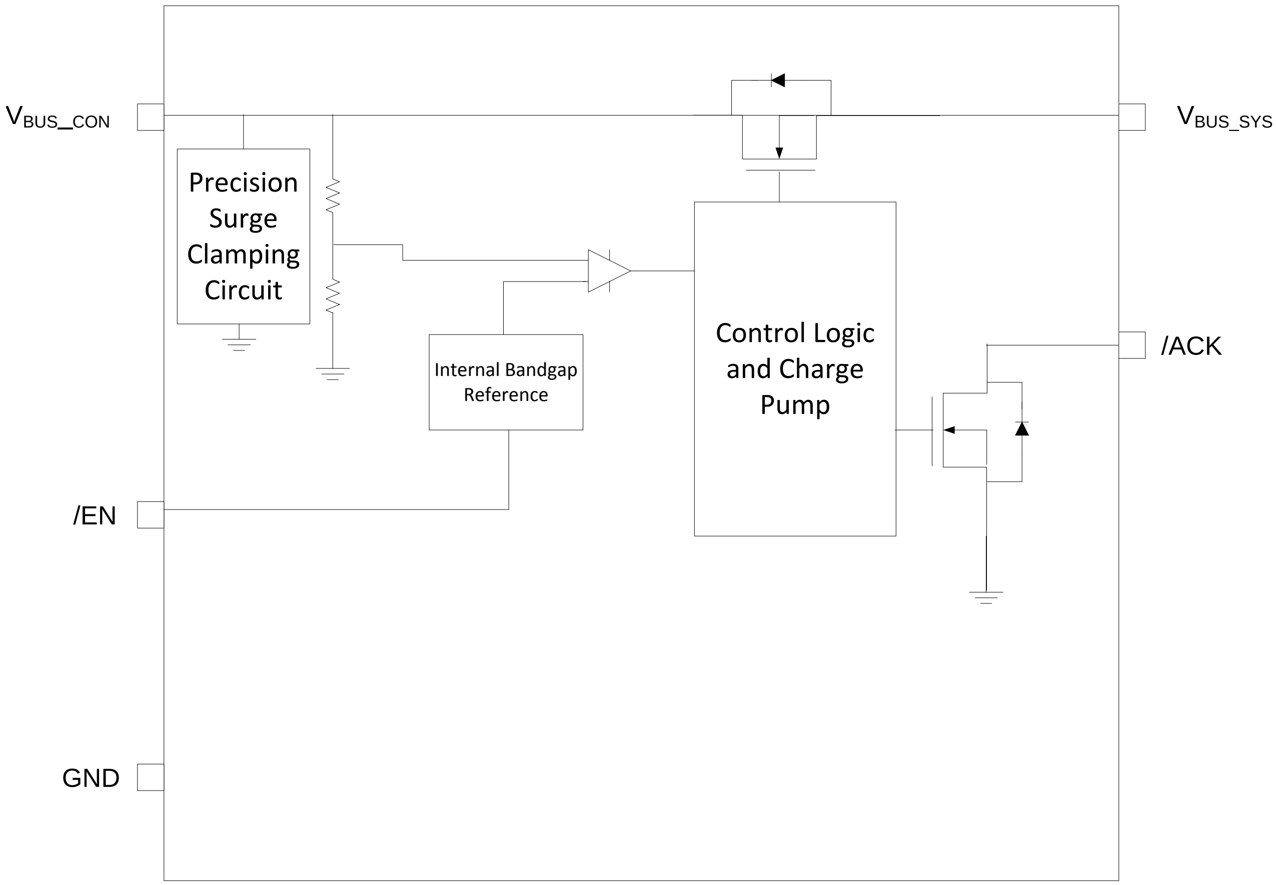


Table 1. DEVICE OPERATION

Voltage Condition			Current Condition		
V_{BUS_CON}	V_{BUS_SYS}	$\overline{EN}$	Current Flow	Comment	$\overline{ACK}$ Pin
X	<V_{BUS_CON}	High	No Flow	Switch off	High-Z
X	>V_{BUS_CON}	High	V_{BUS_SYS} to V_{BUS_CON}	Switch off, current flows through the body diode	High-Z
<OVP	<V_{BUS_CON}	Low	V_{BUS_CON} to V_{BUS_SYS}	Current flows through the switch, normal device charging mode	Low
<OVP	>V_{BUS_CON}	Low	V_{BUS_SYS} to V_{BUS_CON}	Current flows through the switch, normal host mode	Low
>OVP	<V_{BUS_CON}	Low	No Flow	Switch off due to OVP	High-Z
>OVP	>V_{BUS_CON}	Low	V_{BUS_SYS} to V_{BUS_CON}	Switch off, current flows through the body diode	High-Z
X	X	X	No Flow/ Current thru Body Diode	THERMAL SHUTDOWN CONDITION	High-Z
<V_{UVLO}	<V_{BUS_CON}	Low	No Flow	Low Voltage is cut-off from the system	High-Z

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
$\overline{ACK}$	B1	O	Open-Drain Acknowledge pin. See the Device Operation section.
$\overline{EN}$	C1	I	Enable Active-Low Input. Drive $\overline{EN}$ low to enable the switch. Drive $\overline{EN}$ high to disable the switch.
V_{BUS_CON}	C3, C2, B3	I/O	Connect to USB connector V_{BUS_CON}; IEC61000-4-2 ESD protection IEC61000-4-5 Surge protection
V_{BUS_SYS}	A3, A2, B2	I/O	Connect to internal V_{BUS} plane
GND	A1, A4, B4, C4	Ground	Connect to PCB ground plane

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS [(1)(2)]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage from USB connector, V_{BUS_CON}		–0.3	30	V
Internal Supply DC voltage Rail on the PCB, V_{BUS_SYS}		–0.5	7	V
Voltage on Input pin ($\overline{EN}$). V_{EN}		–0.5	7	V
Voltage on $\overline{ACK}$ pin		–0.5	7	V
Storage temperature range, T_{STG}		–40	150	°C
Operating Free Air Temperature, T_A		–40	85	°C
IEC 61000-4-2 Contact Discharge	V_{BUS_CON} pin		±15	kV
IEC 61000-4-2 Air-gap Discharge	V_{BUS_CON} pin		±15	kV
Human-Body Model	ALL Pins		±2	kV
IEC 61000-4-5 Peak Pulse Current (t_p = 8/20 μs)	V_{BUS_CON} pin		21	A
IEC 61000-4-5 Peak Pulse Power (t_p = 8/20 μs)	V_{BUS_CON} pin		700	W
IEC 61000-4-5 Open circuit voltage (t_p = 1.2/50 μs)	V_{BUS_CON} pin		100	V
Output load capacitance, C_{LOAD}	V_{BUS_SYS} pin	0.1	50	μF
Input capacitance, C_{ON}	V_{BUS_CON} pin	0.1	50	μF

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

THERMAL INFORMATION

THERMAL METRIC [(1)]		YZ	UNITS
		12 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	89	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	0.6	
θ_{JB}	Junction-to-board thermal resistance	16.3	
ψ_{JT}	Junction-to-top characterization parameter	2.7	
ψ_{JB}	Junction-to-board characterization parameter	16.2	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/A	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：ZHCA543）。

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{BUS_CON}	Supply voltage from USB connector				5.9	V
V_{BUS_SYS}	Internal Supply DC voltage Rail on the PCB				5.9	V
C_{LOAD}	Output load capacitance	V_{BUS_SYS} pin		2.2		µF
C_{IN}	Input capacitance	V_{BUS_CON} pin		1		µF
R_{PULLUP}	Pull up resistor	$\overline{ACK}$ pin		4.3	100	kΩ
I_{VBUS}	Continuous current on V_{BUS_CON} and V_{BUS_SYS} pins	V_{BUS_CON} V_{BUS_SYS}			3.5	A
I_{DIODE}	Continuous current through the FET body diode				1	A

SUPPLY CURRENT CONSUMPTION

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBUS_SLEEP}	V_{BUS_CON} Operating Current Consumption	Measured at V_{BUS_CON} pin, V_{BUS_CON} = 5 V, $\overline{EN}$ =5V		30	70	µA
I_{VBUS}		Measured at V_{BUS_CON} pin, V_{BUS_CON} = 5 V, $\overline{EN}$ 0 V and no load		175	373	µA
I_{VBUS_SYS}	V_{BUS_CON} Operating Current Consumption	Measured at V_{BUS_SYS} pin, V_{BUS_SYS} = 5 V, $\overline{EN}$ = 0 V and V_{BUS_CON} = Hi Z		175	373	µA
I_{HOST_LEAK}	Host Mode Leakage current	Measured at V_{BUS_SYS}. V_{BUS_CON} = Hi Z, $\overline{EN}$ = 5 V, V_{BUS_SYS} = 5V	90		200	µA

ELECTRICAL CHARACTERISTICS ($\overline{EN}$, $\overline{ACK}$ PINS)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage, $\overline{EN}$		1.2		6	V
V_{IL}	Low-level input voltage, $\overline{EN}$				0.8	V
I_{IL}	Input Leakage Current $\overline{EN}$	V_I = 3.3 V			1	µA
V_{OL}	Low-level output voltage, $\overline{ACK}$	I_{OL} = 3 mA			0.4	V

ELECTRICAL CHARACTERISTICS (OVP CIRCUIT)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP_RISING}	Input overvoltage protection threshold, V_{BUS_CON}	V_{BUS_CON} increasing from 5 V	6	6.2	6.4	V
V_{HYS_OVP}	Hysteresis on OVP, V_{BUS_CON}	V_{BUS_CON} decreasing from 7 V to 5 V		50		mV
$V_{OVP\_FALLING}$	Input overvoltage protection threshold, V_{BUS_CON}	V_{BUS_CON} decreasing from 7 V to 5 V	5.93		6.37	V
V_{UVLO}	Input under voltage lockout, V_{BUS_CON}	V_{BUS_CON} voltage rising from 0 V to 5 V	3.1	3.3	3.5	V
V_{HYS_UVLO}	Hysteresis on UVLO, V_{BUS_CON}	Difference between rising and falling UVLO thresholds		100		mV
$V_{UVLO\_FALLING}$	Input under voltage lockout, V_{BUS_CON}	V_{BUS_CON} voltage rising from 5 V to 0 V	3	3.2	3.4	V
V_{UVLO_SYS}	V_{BUS_SYS} under voltage lockout, V_{BUS_SYS}	V_{BUS_SYS} voltage rising from 0 V to 5 V	3.1	3.6	4.3	V

ELECTRICAL CHARACTERISTICS (OVP CIRCUIT) (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HYS\_UVLO\_SYS}$	V_{BUS_SYS} UVLO Hysteresis, V_{BUS_SYS}	Difference between rising and falling UVLO thresholds on V_{BUS_SYS}		480		mV
$V_{UVLO\_SYS\_FALL}$	V_{BUS_SYS} undervoltage lockout, V_{BUS_SYS}	V_{BUS_SYS} voltage falling from 7 V to 5 V	3	3.2	3.4	V

THERMAL SHUTDOWN FEATURE

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SHDN}	Thermal Shutdown	Junction temperature		145		°C
	Thermal-Shutdown Hysteresis	Junction temperature		35		°C

SWITCHING CHARACTERISTICS (nFET)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	Switch ON Resistance	V_{BUS_CON} = 5 V, I_{OUT} = 1 A, T_A = 25˚C		39	50	mΩ

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DELAY}	USB Charging Turn-ON Delay	Measured from $\overline{EN}$ asserted LOW to nFET beginning to Turn ON(1) excluding soft-start time		20		ms
t_{SS}	USB Charging rise time (Soft Start Delay)	Measure from V_{BUS_SYS} rises above 25% (with 1 MΩ load/ NO C_{LOAD}) until $\overline{ACK}$ goes Low (10%)		25		ms
t_{OFF_DELAY}	USB Charging Turn-OFF time	Measured from $\overline{EN}$ asserted High to V_{BUS_SYS} falling to 10% with R_{LOAD} = 10 Ω and No C_{LOAD} on V_{BUS_SYS}		4		µs
Over Voltage Protection						
$t_{OVP\_response}$	OVP Response time	Measured from OVP Condition to FET Turn OFF(1)(2). V_{BUS_CON} rises at 1V / 100ns			100	ns
t_{OVP_Recov}	Recovery Time	Measured from OVP Clear to FET Turn ON(1)(3)		20		ms

(1) Shown in TIMING DIAGRAM Plots
(2) Parameters provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(3) Excludes soft start time

TYPICAL CHARACTERISTICS

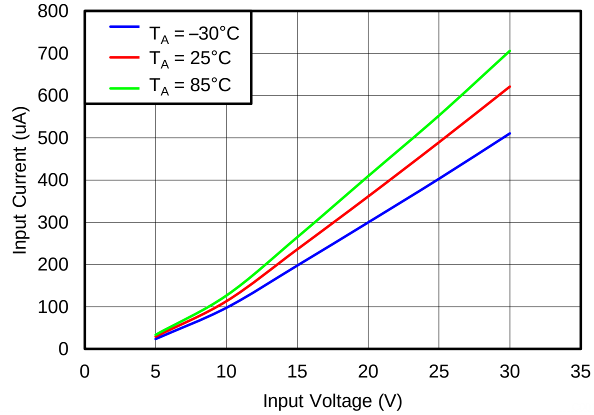


Figure 1. Input Supply Current vs. Supply Voltage

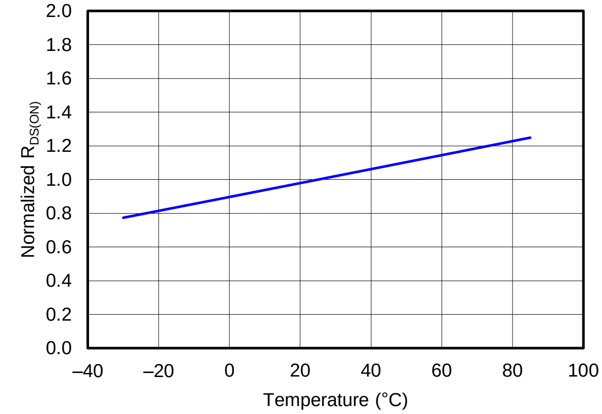


Figure 2. Normalized $R_{DS(ON)}$ vs. Temperature

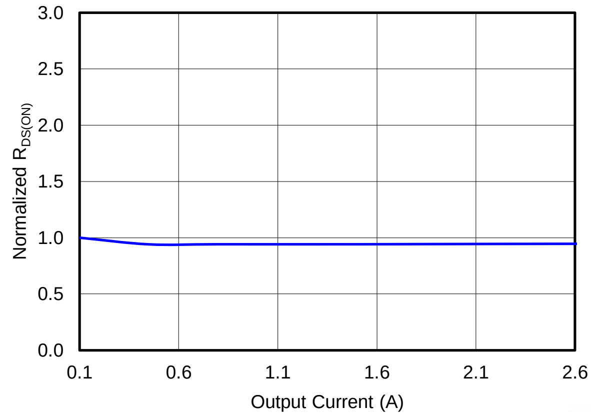


Figure 3. Normalized $R_{DS(ON)}$ vs. Output Current

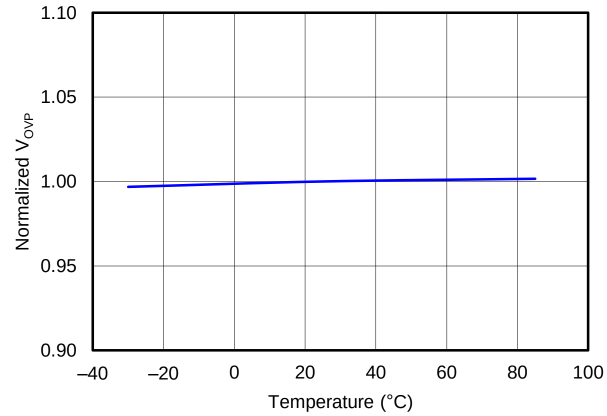


Figure 4. Normalized V_{OVP}

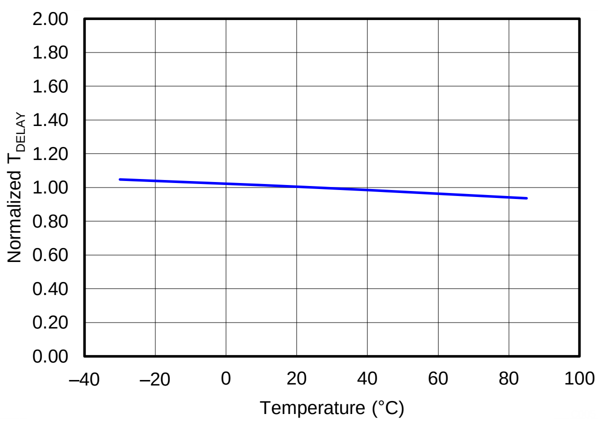


Figure 5. Normalized T_{DELAY}

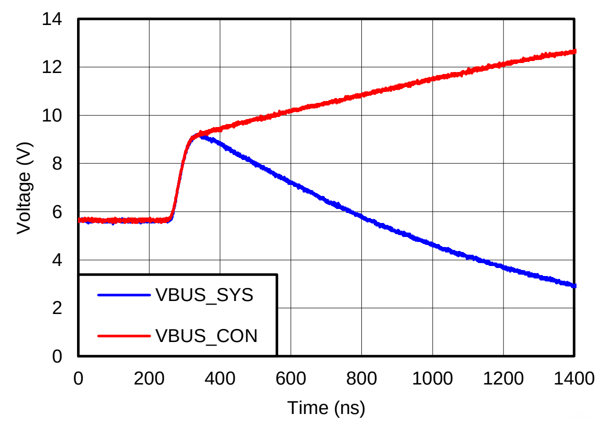


Figure 6. V_{OVP} Response Time

TYPICAL CHARACTERISTICS (continued)

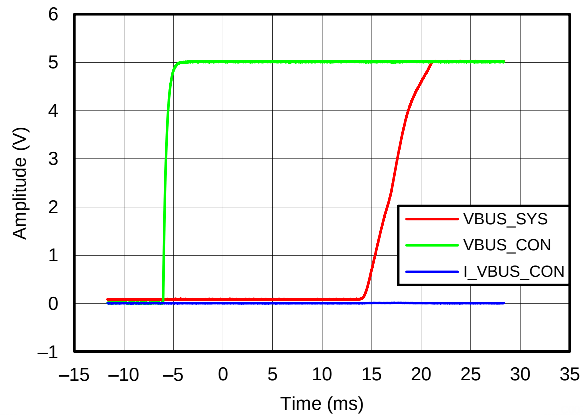


Figure 7. Power Up With 2.2 µF on V_{BUS_SYS}

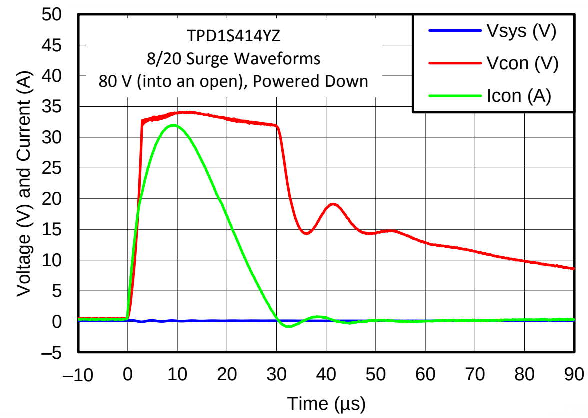


Figure 8. Response to a 100-V Surge

DEVICE INFORMATION

DEVICE OPERATION

The TPD1S414 provides a single-chip ESD protection, surge protection and over voltage protection solution for portable USB charging and Host interfaces. It offers over voltage protection at the V_{BUS_CON} pin up to 30 V. The TPD1S414 also provides a $\overline{ACK}$ pin that indicates to the system if a fault condition has occurred. The TPD1S414 offers an ESD clamp and a Surge Clamp for V_{BUS_CON} pin, thus eliminating the need for external TVS clamp circuits in the application.

The TPD1S414 has an internal oscillator and charge pump that controls the turn-on of the internal nFET switch. The internal oscillator controls the timers that enable the charge pump and resets the open-drain $\overline{ACK}$ output. If V_{BUS_CON} is less than V_{OVP}, the internal charge pump is enabled. After a 15 ms internal delay, the charge-pump starts-up, turns on the internal nFET switch through a soft start. Once the nFET is completely turned ON, TPD1S414 asserts $\overline{ACK}$ pin LOW. At any time, if V_{BUS_CON} rises above V_{OVP}, the $\overline{ACK}$ pin is in High-Z and is pulled HIGH through external resistors. The nFET switch is turned OFF.

OVP OPERATION

When the V_{BUS_CON} voltage rises above V_{OVP}, the internal nFET switch is turned OFF, removing power from the system. The response is rapid, with the FET switch turning off in less than 100 ns. The $\overline{ACK}$ pin is set to High-Z when an overvoltage condition is detected and the nFET is turned OFF. This pin can be pulled up through external resistors to indicate a OVP condition. When the V_{BUS_CON} voltage returns below V_{OVP} – $V_{HYS\text{-}OVP}$, the nFET switch is turned on again after the internal delay of tO_{VP_Recov}. This delay time ensures that the V_{BUS_CON} supply has stabilized before turning the switch back on. After t_{OVP_Recov}, the TPD1S414 turns ON the nFET through a soft start to ensure that the USB Inrush current compliance is met. When the OVP condition is cleared and the nFET is completely turned ON, the $\overline{ACK}$ is reset LOW.

TIMING DIAGRAMS

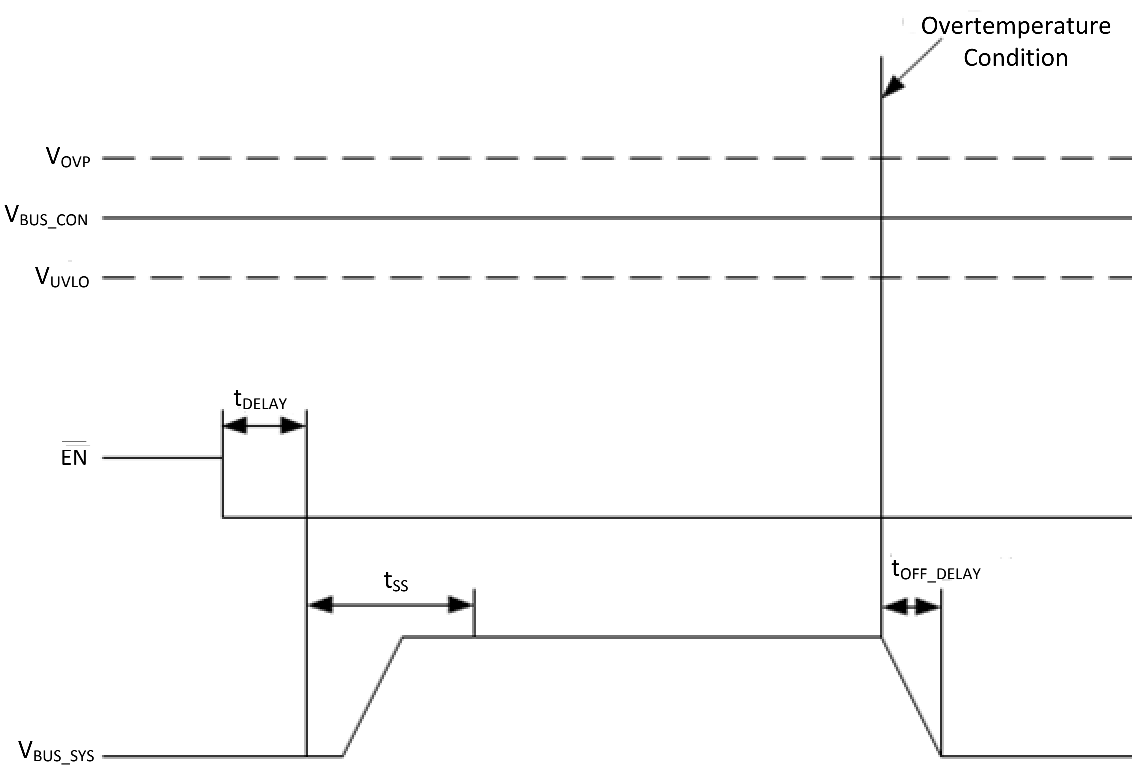


Figure 9. Thermal Shutdown Operation

APPLICATION INFORMATION

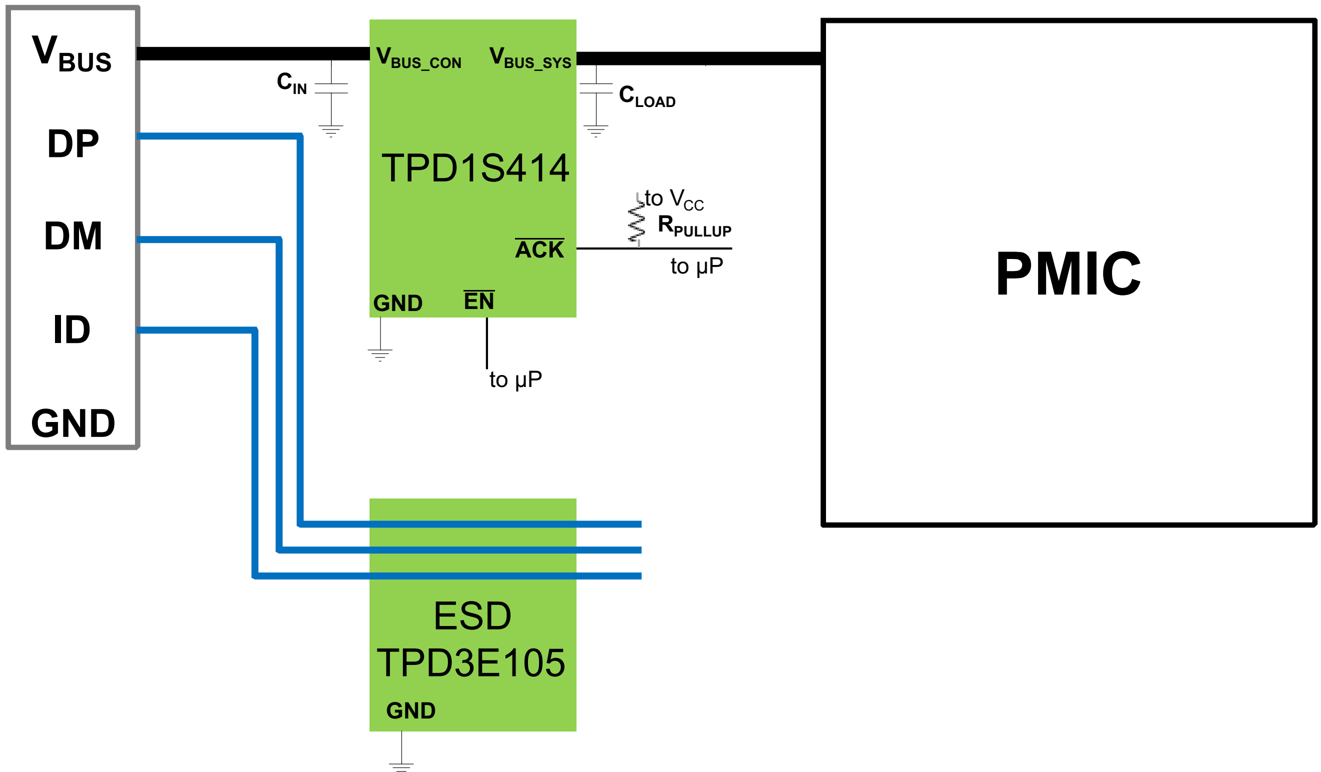


Figure 10. Typical Application Configuration for TPD1S414

The IEC 61000-4-5 standard specifies the lightning and industrial surge model. Power lines like the V_{BUS} line on the USB port is subject to switching and lightning transients. Power supply switching transients can enter the system due to capacitor bank switching on the rail, minor load switching on the system and various system faults like arcing to the grounding system of the installation. Direct lightning to the outer installations cause an over voltage condition on the V_{BUS} line. In the event of an over voltage condition, the OVP block of the Processor or the protection circuitry turns off isolating the system from these transients. Abruptly turning off the Load, causes a further ripple due to the inductive nature of the charging cable. End systems require protection against these transients. These transients have greater energy than the ESD events. Systems cannot be protected from these transients using simple ESD diodes. The TPD1S414 has a precision trigger and precision clamping circuit that ensures a DC tolerance of 30 V while suppressing surge voltage up to 100V under 35 V.

BOARD LAYOUT

TPD1S414 can be routed in a single layer PCB. PCB traces to V_{BUS_SYS}, V_{BUS_CON}, and GND can be routed in the fashion shown in Figure 11.

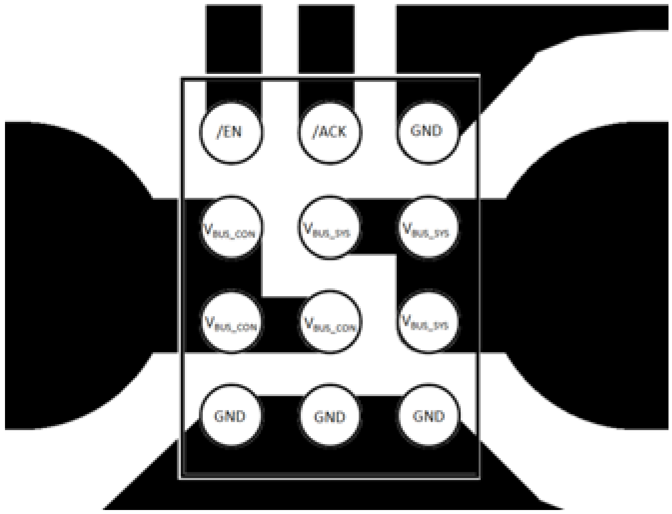


Figure 11. V_{BUS_SYS}, V_{BUS_CON}, and GND pins tied together

Tying V_{BUS_SYS}, V_{BUS_CON}, and GND pins respectively together provides lower resistance connectivity between the USB connector and the PMIC. For this example, the trace widths to V_{BUS_SYS}, V_{BUS_CON} are 25 mils (0.635 mm) under TPD1S414. There are no VIAs required within the SMD pads in this design. Stitching VIAs for GND can be placed near the component instead.

The decoupling capacitors per the recommended operating settings should be placed as close as possible to the TPD1S414. There should be a short path from the device ground pins to the system ground plane. This ensures best protection under ESD and surge transients.

REVISION HISTORY

Changes from Original (October 2013) to Revision A **Page**

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD1S414YZR	Active	Production	DSBGA (YZ) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RH414
TPD1S414YZR.A	Active	Production	DSBGA (YZ) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RH414

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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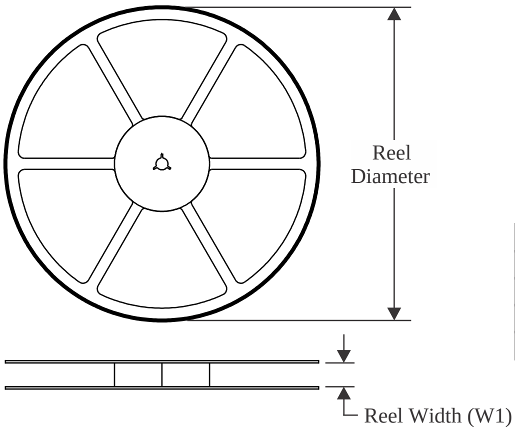
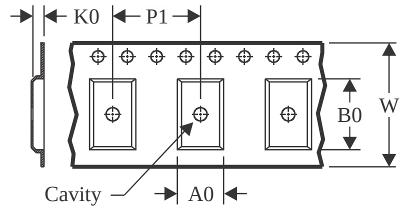
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

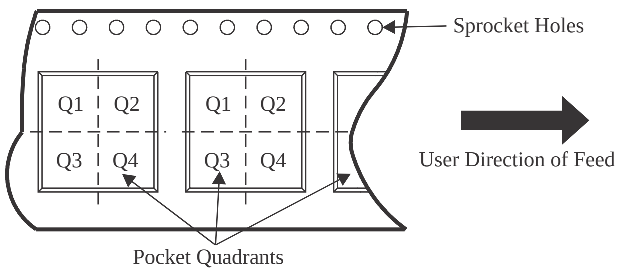


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

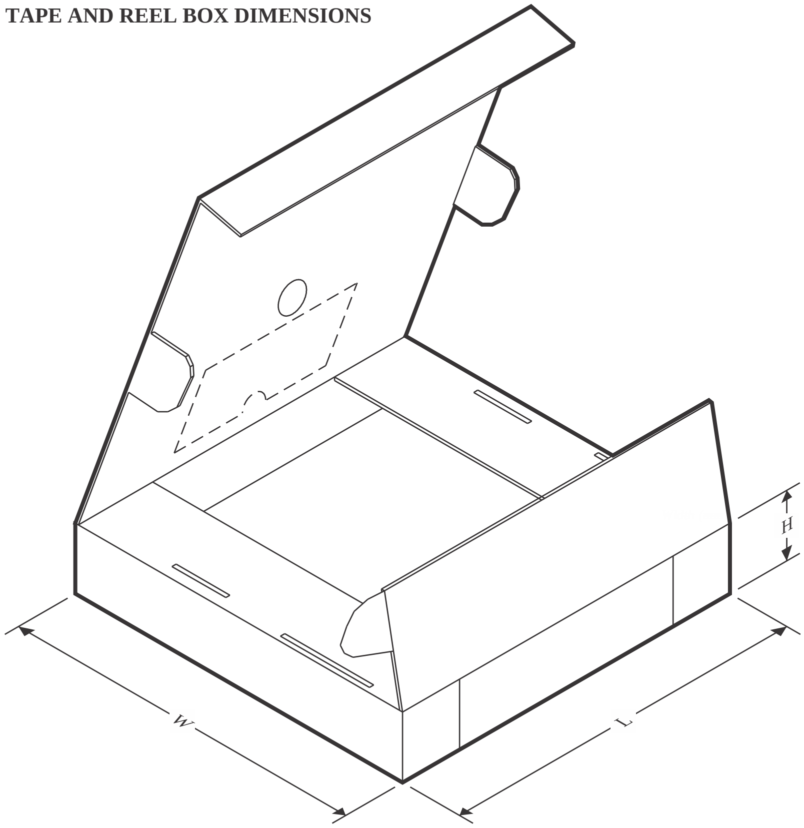
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1S414YZR	DSBGA	YZ	12	3000	180.0	8.4	1.5	1.99	0.75	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1S414YZR	DSBGA	YZ	12	3000	182.0	182.0	20.0