TEXAS INSTRUMENTS
TPD1E01B04-Q1
ZHCSN54A – MAY 2021 – REVISED DECEMBER 2021

TPD1E01B04-Q1 采用 0402 封装的汽车类 0.2pF、±3.6V、±15kV ESD 保护二极管

1 特性

- IEC 61000-4-2 4 级 ESD 保护
  - ±15kV 接触放电
  - ±17kV 空气间隙放电
- IEC 61000-4-4 EFT 保护
  - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
  - 2.5A (8/20μs)
- IO 电容：
  - 0.20pF（典型值）
  - 0.23pF（最大值）
- 直流击穿电压：6.4V（典型值）
- 超低泄漏电流：10nA（最大值）
- 低 ESD 钳位电压：16A TLP 时为 15V
- 低插入损耗：20 GHz
- 支持速率高达 20Gbps 的高速接口
- 业界通用 0402 封装
- 符合 AEC-Q101 标准
  - 器件 HBM 分类等级 H2
  - 器件 CDM 分类等级 C5
  - 器件工作温度范围：–40°C 至 +125°C

2 应用

- 终端设备
  - 环视系统
  - ADAS 视觉系统
  - 后视摄像头
  - 信息娱乐系统与仪表组
  - 车身控制模块
  - 音响主机
- 接口
  - 汽车串行器/解串器：FPD-Link
  - USB Type-C
  - USB 3.1 Gen 2/3.0/2.0
  - HDMI 2.0/1.4
  - 10/100/1000Mbps 以太网

3 说明

TPD1E01B04-Q1 是一款双向 TVS ESD 保护二极管，用于为 USB Type-C 和 FPD-Link 电路提供保护。TPD1E01B04-Q1 的额定 ESD 冲击消散值等于 IEC 61000-4-2 国际标准（4 级）规定的最高水平。

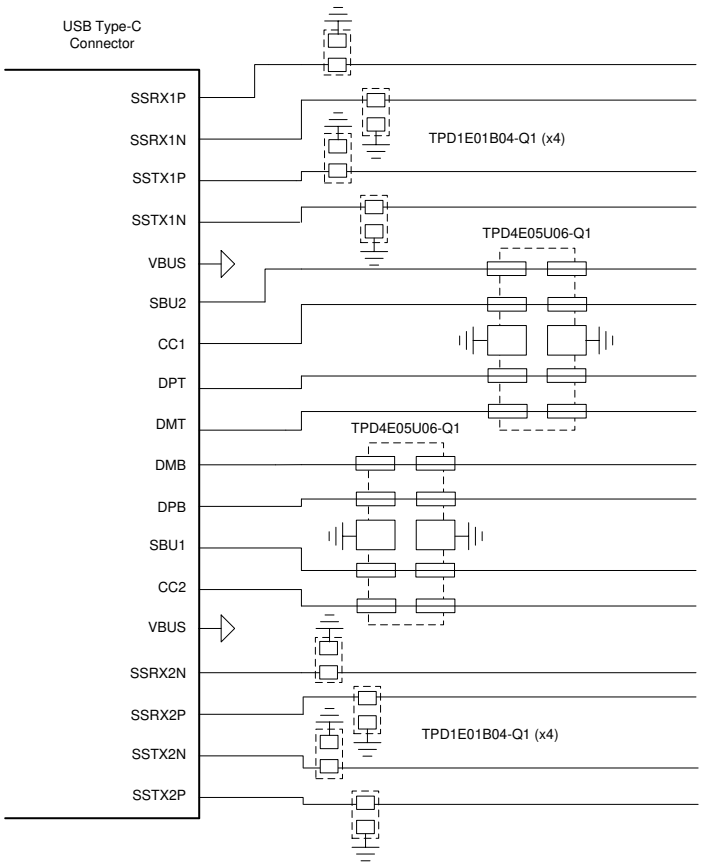
该器件采用一个 0.20pF（典型值）的 IO 电容，适用于保护速率高达 20Gbps 的高速接口（例如 USB 3.1 Gen2 和 FPD-Link）。低动态电阻和低钳位电压确保系统级抗瞬变事件保护。

TPD1E01B04-Q1 采用业界通用的 0402 (DPY) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD1E01B04-Q1	X1SON (2)	1.00mm x 0.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (May 2021) to Revision A (December 2021)	Page
• 将数据表的状态从*预告信息*更改为*量产数据*	1

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5 Pin Configuration and Functions

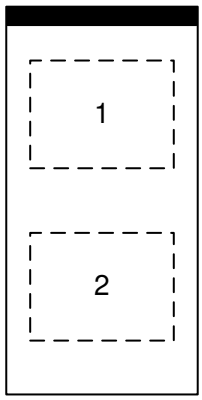

图 5-1. DPY Package 2-Pin X1SON Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
2	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

(1) I = input, O = output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-5 (5/50 ns) at 25°C		80	A
Peak pulse	IEC 61000-4-5 power (t_p - 8/20 µs) at 25°C		27	W
	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C		2.5	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001	±2500	V
		Charged device model (CDM), per AEC Q101-005	±1000	

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±15000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±17000	

6.4 ESD Ratings—ISO Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ISO 10605, 330-pF, 330-Ω, IO	Contact discharge	± 12500	V
			Air-gap discharge	±15000	

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IO}	Input pin voltage	–3.6		3.6	V
T_A	Operating free-air temperature	–40		125	°C

6.6 Thermal Information

THERMAL METRIC(1)		TPD1E01B04-Q1 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	442.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	243.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	162.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	154.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	163.0	°C/W

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6.6 Thermal Information (continued)

THERMAL METRIC[1]		TPD1E01B04-Q1 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	−3.6		3.6	V
V_{BRF}	Breakdown voltage, IO pin to GND	Measured as the maximum voltage before device snaps back into V_{HOLD} voltage		6.4		V
V_{BRR}	Breakdown voltage, GND to IO pin			−6.4		V
V_{HOLD}	Holding voltage	I_{IO} = 1 mA, T_A = 25°C	5	5.9	6.5	V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND		7		V
		I_{PP} = 5 A, TLP, from IO to GND		9.2		
		I_{PP} = 16 A, TLP, from IO to GND		15		
		I_{PP} = 1 A, TLP, from GND to IO		7		
		I_{PP} = 5 A, TLP, from GND to IO		9.2		
		I_{PP} = 16 A, TLP, from GND to IO		15		
I_{LEAK}	Leakage current, IO to GND	V_{IO} = ±2.5 V			10	nA
R_{DYN}	Dynamic resistance	IO to GND		0.57		Ω
		GND to IO		0.57		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND, T_A = 25°C		0.2	0.23	pF

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6.8 Typical Characteristics

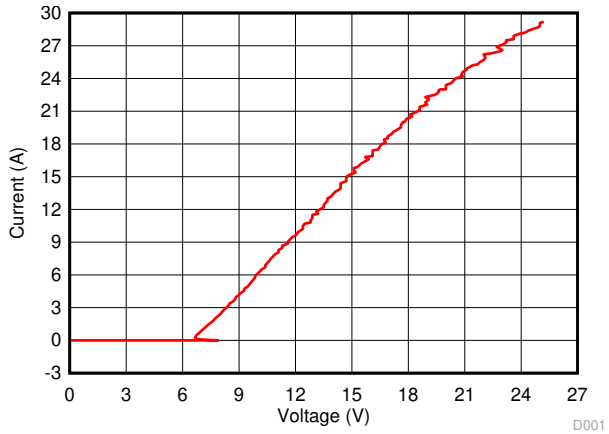

图 6-1. Positive TLP Curve

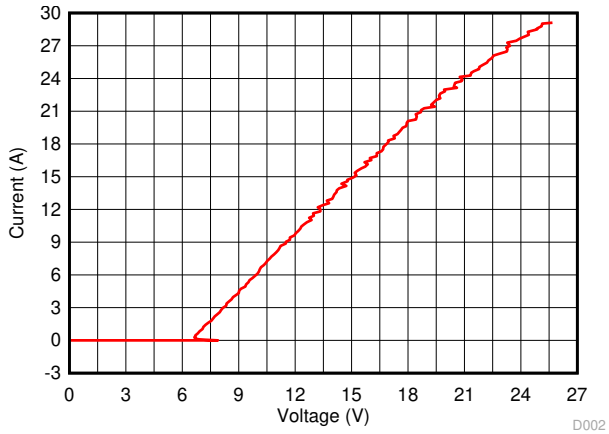

图 6-2. Negative TLP Curve

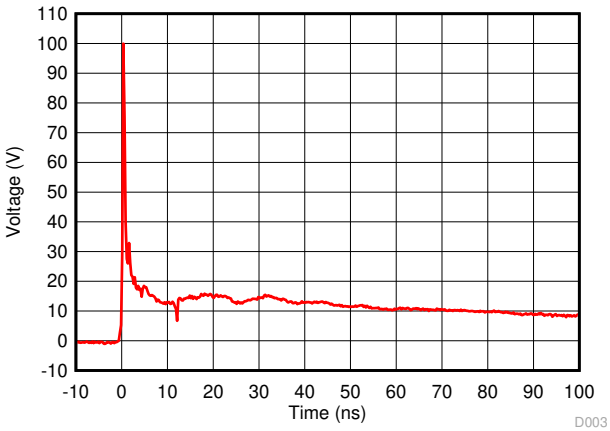

图 6-3. 8-kV IEC Waveform

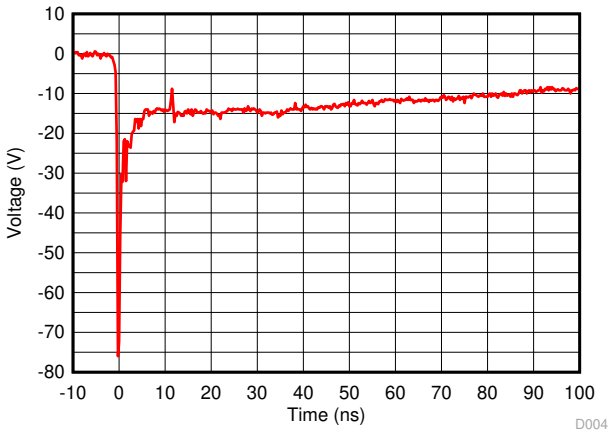

图 6-4. – 8-kV IEC Waveform

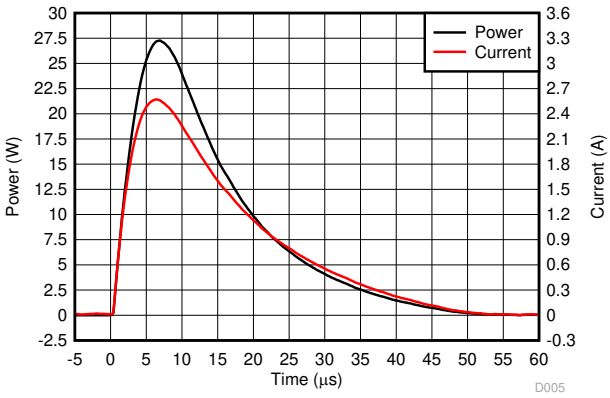

图 6-5. Surge Curve (t_p = 8/20µs), IO pin to GND

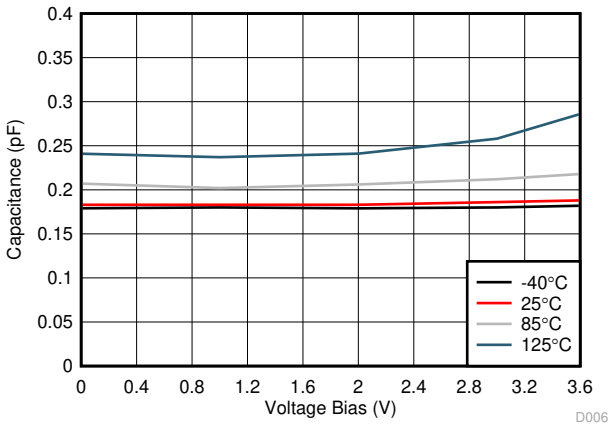

图 6-6. Capacitance vs. Bias Voltage

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6.8 Typical Characteristics (continued)

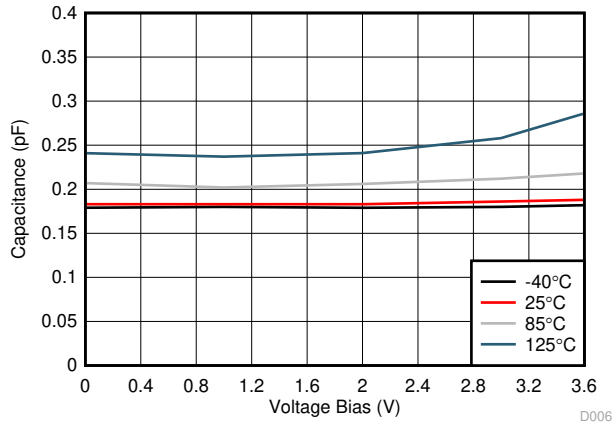

图 6-7. Capacitance vs. Bias Voltage (DPY Package)

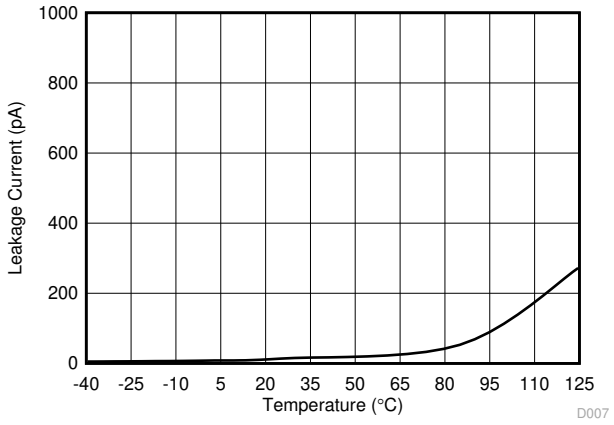

图 6-8. Leakage Current vs. Temperature

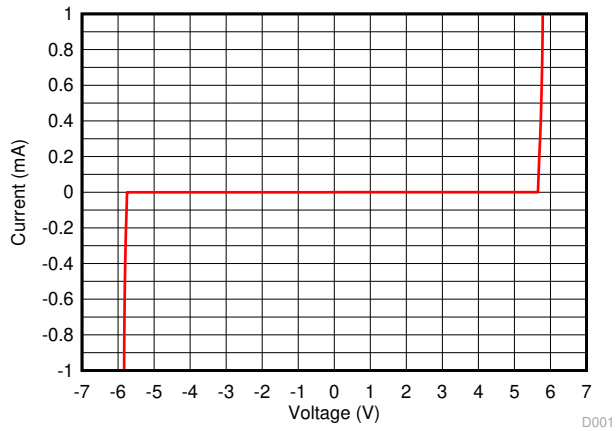

图 6-9. DC Voltage Sweep I-V Curve

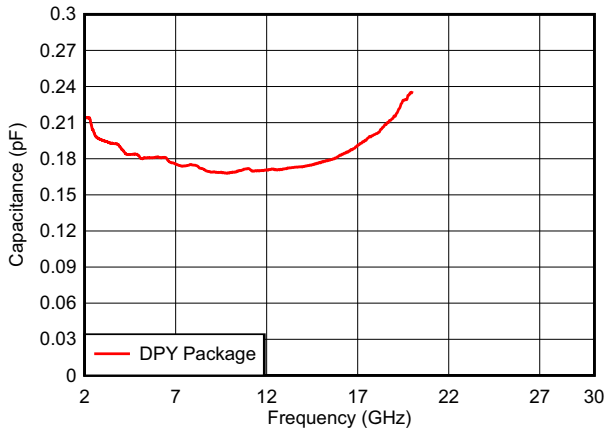

图 6-10. Capacitance vs. Frequency

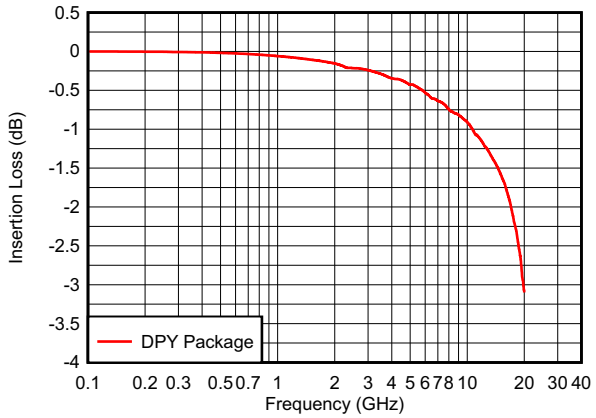

图 6-11. Insertion Loss

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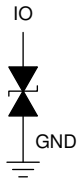
7 Detailed Description

7.1 Overview

The TPD1E01B04-Q1 device is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins including Thunderbolt 3. The low capacitance allows for extremely low losses even at RF frequencies such as USB 3.1 Gen 2, Thunderbolt 3, or antenna applications.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±15-kV contact and ±17-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 27 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.2 pF (typical) and 0.23 pF (maximum). This device supports data rates up to 20 Gbps.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is ±6.4 V (typical). This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

7.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) at a bias voltage of ±2.5 V.

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 9.2 V (I_{PP} = 5 A).

7.3.8 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 20 Gbps, because of the extremely low IO capacitance.

7.3.9 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.10 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

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7.4 Device Functional Modes

The TPD1E01B04-Q1 device is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±17 kV (air) can be directed to ground through the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD1E01B04-Q1 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPD1E01B04-Q1 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

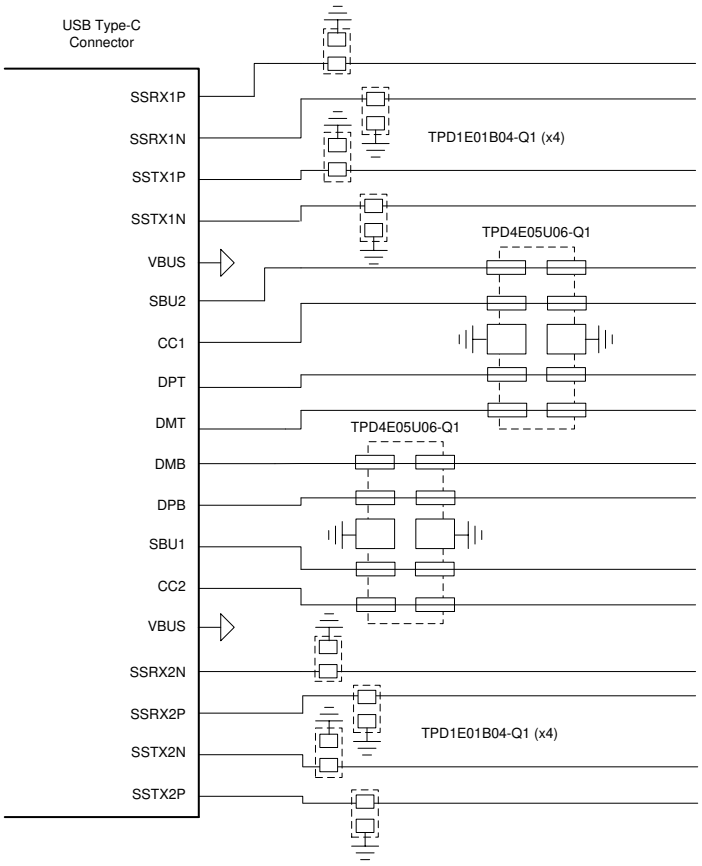

图 8-1. USB Type-C for Thunderbolt 3 ESD Schematic

8.2.1 Design Requirements

For this design example eight TPD1E01B04-Q1 devices and two TPD4E05U06-Q1 devices are being used in a USB Type-C for Thunderbolt 3 application. This provides a complete ESD protection scheme.

Given the Thunderbolt 3 application, the parameters listed in 表 8-1 are known.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on superspeed Lines	0 V to 3.6 V
Operating frequency on superspeed Lines	up to 10 GHz
Signal range on CC, SBU, and DP/DM Lines	0 V to 5 V
Operating frequency on CC, SBU, and DP/DM Lines	up to 480 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD1E01B04-Q1 supports signal ranges between – 3.6 V and 3.6 V, which supports the SuperSpeed pairs on the USB Type-C application. The TPD4E05U06-Q1 supports signal ranges between 0 V and 5.5 V, which supports the CC, SBU, and DP-DM lines.

8.2.2.2 Operating Frequency

The TPD1E01B04-Q1 has a 0.2 pF (typical) capacitance, which supports the Thunderbolt 3 data rates of 20 Gbps. The TPD4E05U06-Q1 has a 0.5-pF (typical) capacitance, which easily supports the CC, SBU, and DP-DM data rates.

8.2.3 Application Curves

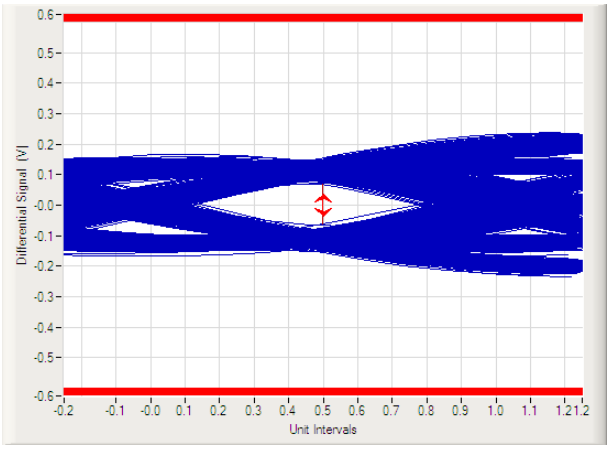

图 8-2. USB 3.1 Gen 2 10-Gbps Eye Diagram (Bare Board)

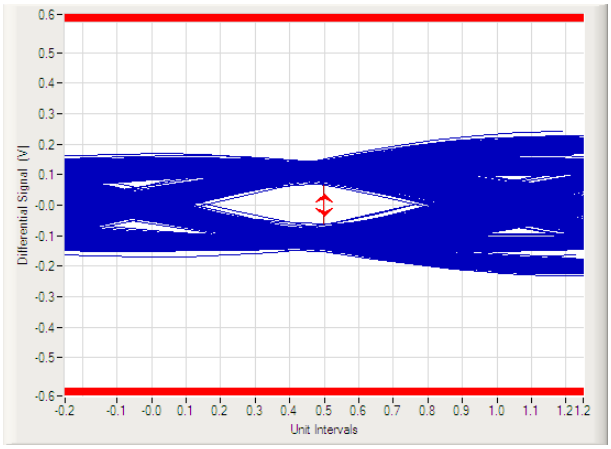

图 8-3. USB 3.1 Gen 2 10-Gbps Eye Diagram (with TPD1E01B04-Q1)

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification to ensure the device functions properly.

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10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

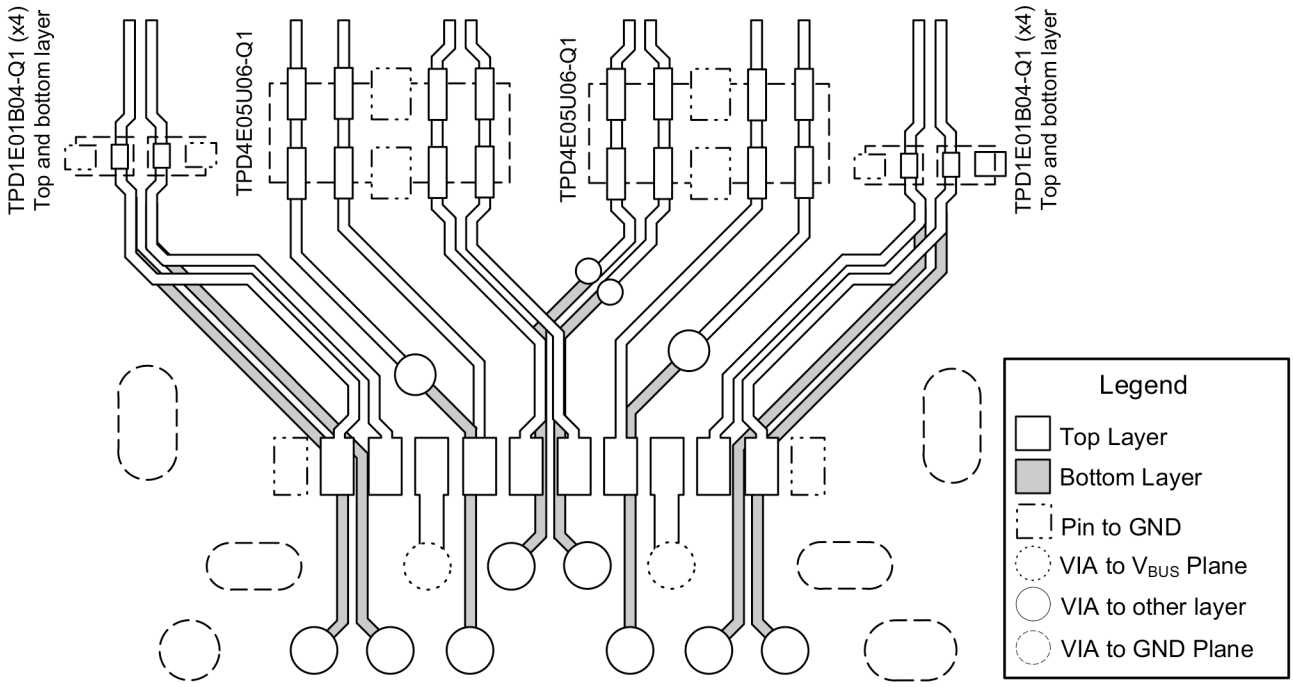

图 10-1. USB Type-C Mid-Mount, Hybrid Connector ESD Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Generic ESD Evaluation Module* user's guide

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD1E01B04DPYRQ1	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	LR
TPD1E01B04DPYRQ1.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	LR

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPD1E01B04-Q1 :

- Catalog : TPD1E01B04

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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