# TPD12S015 HDMI Companion Chip With Step-Up DC-DC, I²C Level Shifter, and High-Speed ESD Clamps for Portable Applications

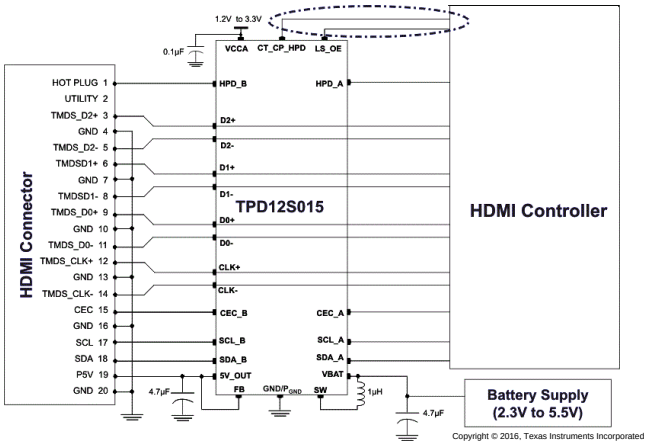
## 1 Features

- HDMI 1.3 and HDMI 1.4 Data Rate
- HDMI High-Speed Differential Signals –3-dB Bandwidth Exceeds 6.4 Gbps
- Excellent Matching Capacitance (0.05 pF) in Each Differential Signal Pair
- Internal Boost Converter to Generate 5 V From a 2.3-V to 5.5-V Battery Voltage
- HDMI Minimum Current Limit and Short-Circuit Protection at 5VOUT Pin
- Flexible Power-Saving Modes Through Separate Control Pins
- Auto-Direction Sensing Level Shifting in the CEC, SDA, and SCL Lines Drive up to 750-pF Load
- Seamless Type C and Type D Connector Routing With Flow-Through Pin Mapping
- IEC 61000-4-2 (Level 4) System Level ESD Compliance
- Integrated $I_{OFF}$ and Backdrive Current Protection
- Space-Saving 1.6-mm × 2.8-mm DSBGA (YFF) Package

## 2 Applications

- Smart Phones
- Multimedia Phones
- Digital Camcorders
- Digital Still Cameras
- Portable Game Consoles

### Typical System Diagram




## 3 Description

The TPD12S015 device is an integrated HDMI ESD solution. The device pin mapping matches the HDMI Type C and Type D connector with four differential pairs. This device offers eight low-capacitance ESD clamps, allowing HDMI 1.3 or 1.4 data rates. The integrated ESD clamps and resistors provide good matching between each differential signal pair, which allows an advantage over discrete ESD clamp solutions where variations between ESD clamps degrade the differential signal quality.

The TPD12S015 provides a regulated 5-V output (5VOUT) for sourcing the HDMI power line. The regulated 5-V output supplies up to 55 mA to the HDMI receiver. The control of 5VOUT and the hot plug detect (HPD) circuitry is independent of the LS_OE control signal and is controlled by the CT_CP_HPD pin. This independent control enables the detection scheme (5VOUT + HPD) to be active before enabling the HDMI link.

There are three noninverting, bidirectional translation circuits for the SDA, SCL, and CEC lines. Each have a common power rail ($V_{CCA}$) on the A side from 1.1 V to 3.6 V . On the B side, the SCL_B and SDA_B each have an internal 1.75-kΩ pullup connected to the regulated 5-V rail (5VOUT). The SCL and SDA pins meet the I²C specification and drive up to 750-pF loads. The CEC_B pin has an internal 27-kΩ pullup to an internal 3.3-V supply.

The HPD_B port has a glitch filter to avoid false detection due to the bouncing while inserting the HDMI plug.

The TPD12S015 provides IEC61000-4-2 (Level 4) ESD protection. This device is offered in a space-saving 1.6-mm × 2.8-mm wafer-level chip scale package [DSBGA (YFF)] with a 0.4-mm pitch.

### Device Information(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPD12S015 | DSBGA (28) | 1.56 mm × 2.76 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision E (June 2013) to Revision F** **Page**

- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

**Changes from Revision D (April 2012) to Revision E** **Page**

- Updated test $I_{OH}$ and $I_{OL}$ test conditions for $V_{OHA}$, $V_{OLA}$, and $V_{OHB}$ ... 9
- Updated test $I_{OH}$ and $I_{OL}$ test conditions for $V_{OHA}$, $V_{OLA}$, and $V_{OHB}$ ... 9

**Changes from Revision C (November 2010) to Revision D** **Page**

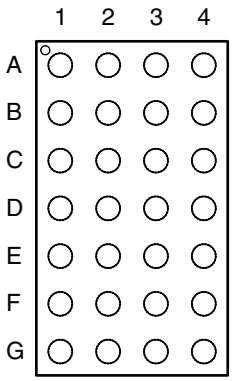
- Changed $V_{IH}$ MAX value for CT_CP_HPD, LS_OE parameter from $V_{CCA}$ to 3.6. ..... 6

**Changes from Revision B (July 2010) to Revision C** **Page**

- Added Type D connecter specification to "FEATURES" ..... 1
- Added Type D connecter specification to "DESCRIPTION/ORDERING INFORMATION" ..... 1

# 5 Pin Configuration and Functions

**YFF Package**
**28-Pin DSBGA**
**Top View**




For package dimensions, see the *Mechanical, Packaging, and Orderable Information* section.

**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 5VOUT | F1 | Pwr O | DC-DC output. The 5-V power pin can supply 55-mA regulated current to the HDMI receiver. Separate DC-DC converter control pin CT_CP_HPD disables the DC-DC converter when operating at low-power mode. |
| CEC_A | B2 | I/O | System-side CEC bus I/O. This pin is bidirectional and referenced to $V_{CCA}$. |
| CEC_B | D3 | I/O | HDMI-side CEC bus I/O. This pin is bidirectional and referenced to the 3.3-V internal supply. |
| CLK– | G4 | ESD | High-speed ESD clamp: provides ESD protection to the high-speed HDMI differential data lines. |
| CLK+ | F4 | | |
| CT_CP_HPD | D1 | Ctrl | DC-DC Enable. Enables the DC-DC converter and HPD circuitry when CT_CP_HPD = H. The CT_CP_HPD is referenced to $V_{CCA}$. |
| D0– | E4 | ESD | High-speed ESD clamp: provides ESD protection to the high-speed HDMI differential data lines. |
| D0+ | D4 | | |
| D1– | C4 | | |
| D1+ | B4 | | |
| D2– | A4 | | |
| D2+ | A3 | | |
| FB | E1 | I | Feedback input. This pin is a feedback control pin for the DC-DC converter. It must be connected to 5VOUT. |
| GND | B3, C3, D2, E2 | — | Device ground |
| HPD_A | C2 | O | System-side output for the hot plug detect. This pin is unidirectional and is referenced to $V_{CCA}$. |
| HPD_B | G3 | I | HDMI-side input for the hot plug detect. This pin is unidirectional and is referenced to 5VOUT. |
| LS_OE | A1 | Ctrl | Level shifter enable. This pin is referenced to $V_{CCA}$. Enables level shifters and LDO when OE = H. |
| $P_{GND}$ | G1 | — | DC-DC converter ground. This pin should be tied externally to the system GND plane. See *Layout Guidelines*. |
| SCL_A | B1 | I/O | System-side input and output for $I^2C$ bus. This pin is bidirectional and referenced to $V_{CCA}$. |
| SCL_B | E3 | I/O | HDMI-side input and output for $I^2C$ bus. This pin is bidirectional and referenced to 5VOUT. |

## Pin Functions (continued)

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SDA_A | C1 | I/O | System-side input and output for $I^2C$ bus. This pin is bidirectional and referenced to $V_{CCA}$. |
| SDA_B | F3 | I/O | HDMI-side input and output for $I^2C$ bus. This pin is bidirectional and referenced to 5VOUT. |
| SW | F2 | I | Switch input. This pin is the inductor input for the DC-DC converter. |
| $V_{BAT}$ | G2 | Supply | Battery supply. This voltage is typically 2.3 V to 5.5 V. |
| $V_{CCA}$ | A2 | Supply | System-side supply. This voltage is typically 1.2 V to 3.3 V from the core microcontroller. |

## Table 1. YFF Package Pin Mapping

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| **A** | LS_OE | $V_{CCA}$ | D2+ | D2– |
| **B** | SCL_A | CEC_A | GND | D1+ |
| **C** | SDA_A | HPD_A | GND | D1– |
| **D** | CT_CP_HPD | GND | CEC_B | D0+ |
| **E** | FB | GND | SCL_B | D0– |
| **F** | 5VOUT | SW | SDA_B | CLK+ |
| **G** | $P_{GND}$ | $V_{BAT}$ | HPD_B | CLK– |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | | 4 | V |
| $V_{BAT}$ | Supply voltage | | –0.3 | 6.5 | V |
| $V_I$ | Input voltage | SCL_A, SDA_A, CEC_A , CT_CP_HPD, LS_OE | –0.3 | 4 | V |
| | | SCL_B, SDA_B, CEC_B, D, CLK | –0.3 | 6 | |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state(2) | SCL_A, SDA_A, CEC_A, HPD_A | –0.3 | 4 | V |
| | | SCL_B, SDA_B, CEC_B | –0.3 | 6 | |
| | Voltage applied to any output in the high or low state(2) | SCL_A, SDA_A, CEC_A, HPD_A | –0.3 | $V_{CCA}$ + 0.3 | |
| | | SCL_B, SDA_B, CEC_B | –0.5 | 6 | |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_{OUTMAX}$ | Continuous current through 5VOUT or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | All pins except E4, D4, C4, B4, A4, A3, G4, F4, D3, G3, E3, F3 F1, and E1 | ±2500 | V |
| | | | Pins E4, D4, C4, B4, A4, A3, G4, F4, D3, G3, E3, F3 F1, and E1 | ±15000 | |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | | ±1000 | |
| | | IEC 61000-4-2 contact discharge | Pins E4, D4, C4, B4, A4, A3, G4, F4, D3, G3, E3, F3 F1, and E1 | ±8000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)

| | | | SUPPLY | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | | 1.1 | | 3.6 | V |
| $V_{BAT}$ | Supply voltage | | | 2.3 | | 5.5 | V |
| $V_{IH}$ | High-level input voltage | SCL_A, SDA_A, CEC_A | $V_{CCA}$ = 1.1 V to 3.6 V | 0.7 × $V_{CCA}$ | | $V_{CCA}$ | V |
| | | CT_CP_HPD, LS_OE | | 1 | | 3.6 | |
| | | SCL_B, SDA_B | 5VOUT = 5 V | 0.7 × 5VOUT | | 5VOUT | |
| | | CEC_B | | 0.7 × 3.3 (internal) | | 3.3 (internal) | |
| | | HPD_B | | 2.4 | | 5VOUT | |

## Recommended Operating Conditions (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| | | | SUPPLY | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level input voltage | SCL_A, SDA_A, CEC_A | $V_{CCA}$ = 1.1 V to 3.6 V | –0.5 | | 0.082 × $V_{CCA}$ | V |
| | | CT_CP_HPD, LS_OE | | –0.5 | | 0.4 | |
| | | SCL_B, SDA_B | 5VOUT = 5 V | –0.5 | | 0.3 × 5VOUT | |
| | | CEC_B | | –0.5 | | 0.3 × $V_{3P3}$ | |
| | | HPD_B | | 0 | | 0.8 | |
| $V_{ILC}$ | Low-level input voltage (contention) | SCL_A, SDA_A, CEC_A | $V_{CCA}$ = 1.1 V to 3.6 V | –0.5 | | 0.065 × $V_{CCA}$ | V |
| $V_{OL}$ – $V_{ILC}$ | Delta between $V_{OL}$ and $V_{ILC}$ | SCL_A, SDA_A, CEC_A | $V_{CCA}$ = 1.1 V to 3.6 V | 0.1 × $V_{CCA}$ | | | V |
| $T_A$ | Operating free-air temperature | | | –40 | | 85 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPD12S015 YFF (DSBGA) 28 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 63 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 0.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 9.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.6 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 9.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics: $I_{CC}$

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CCA}$ | Standby | $V_{CCA}$ | I/O = High | | | 2 | µA |
| | Active | | | | | 15 | |
| $I_{CCB}$ | Standby | $V_{BAT}$ | CT_CP_HPD=L, LS_OE=L, HPD_B=L | | 2 | | µA |
| | DC-DC and HPD active | | CT_CP_HPD=H, LS_OE=L, HPD_B=L | | 30 | 50 | |
| | DC-DC, HPD, DDC, CEC active | | CT_CP_HPD=H LS_OE=H, HPD_B=L, I/O =H | | 225 | 300 | |

## 6.6 Electrical Characteristics: High-Speed ESD Lines: Dx, CLK

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{OFF}$ | Current from IO port to supply pins | $V_{CC}$ = 0 V, $V_{IO}$ = 3.3 V | | | 0.01 | 0.5 | µA |
| $V_{DL}$ | Diode forward voltage | $I_D$ = 8 mA, | Lower clamp diode | | 0.85 | 1 | V |
| $R_{DYN}$ | Dynamic resistance | I = 1 A | D, CLK | | 1 | | Ω |
| $C_{IO}$ | IO capacitance | $V_{IO}$ = 2.5 V | D, CLK | | 1.3 | | pF |
| $V_{BR}$ | Break-down voltage | $I_{IO}$ = 1 mA | | 9 | | 12 | V |

## 6.7 Electrical Characteristics: DC-DC Converter

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{BAT}$ | Input voltage range | | 2.3 | | 5.5 | V |
| 5VOUT | Total DC output voltage | Includes voltage references, DC load and line regulations, process and temperature | 4.9 | 5 | 5.13 | V |
| TOVA | Total output voltage accuracy | Includes voltage references, DC load and line regulations, transient load and line regulations, ripple, process and temperature | 4.8 | 5 | 5.3 | V |
| $V_{O\_Ripple}$ | Output voltage ripple, loaded | $I_O$ = 65 mA | | | 20 | mVp-p |
| F_clk | Internal operating frequency | $V_{BAT}$ = 2.3 V to 5.5 V | | 3.5 | | MHz |
| $t_{start}$ | Start-up time | From CT_CP_HPD input to 5-V power output 90% point | | | 300 | µs |
| $I_O$ | Output current | $V_{BAT}$ = 2.3 V to 5.5 V | 55 | | | mA |
| | Reverse leakage current $V_O$ | CT_CP_HPD= L, $V_O$ = 5.5 V | | | 2.5 | µA |
| | Leakage current from battery to $V_O$ | CT_CP_HPD= L | | | 5 | µA |
| $V_{BATUV}$ | Undervoltage lockout threshold | Falling | | 2 | | V |
| | | Rising | | 2.1 | | |
| $V_{OVC}$ | Input overvoltage threshold | Falling | | 5.9 | | V |
| | | Rising | | 6 | | |
| | Line transient response | $V_{BAT}$ = 3.6 V, a pulse of 217-Hz 600 mVp-p square wave, $I_O$ = 20/65 mA | | ±25 | ±50 | mVpk |
| | Load transient response | $V_{BAT}$ = 3.6 V, $I_O$ = 5 to 65 mA, pulse of 10 µs, $t_r = t_f$ = 0.1 µs | | 50 | | mVpk |
| $I_{DD\ (idle)}$ | Power supply current from $V_{BAT}$ to DC-DC, enabled, unloaded | $I_O$ = 0 mA | | 30 | 50 | µA |
| $I_{DD\ (disabled)}$ | Power supply current from $V_{BAT}$, DC-DC Disabled, Unloaded | $V_{BAT}$ = 2.3 V to 5.5 V, $I_O$ = 0 mA, CT_CP_HPD Low | | | 2 | µA |
| $I_{DD(system\ off)}$ | Power supply current from $V_{BAT}$, $V_{CCA}$ =0 V | $V_{CCA}$ = 0 V | | | 5 | µA |
| I_inrush (start-up) | Inrush current, average over T_startup time | $V_{BAT}$ = 2.3 V to 5.5 V, $I_O$ = 65 mA | | 100 | | mA |
| $T_{SD}$ | Thermal shutdown | Increasing junction temperature | | 140 | | °C |
| | Thermal shutdown hysteresis | Decreasing junction temperature | | 20 | | |
| $I_{SC}$ | Short-circuit current limit from output | 5-Ω short to GND | | | 500 | mA |

## 6.8 Electrical Characteristics: Passive Components

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TYP | UNIT |
|---|---|---|---|
| $L_{IN}$ | External inductor, 0805 footprint | 1 | µH |
| $C_{IN}$ | Input capacitor, 0603 footprint | 4.7 | µF |
| $C_{OUT}$ | Output capacitor, 0603 footprint | 4.7 | µF |
| $C_{VCCA}$ | Input capacitor, 0402 footprint | 0.1 | µF |

## 6.9 Electrical Characteristics: Voltage Level Shifter: SCL, SDA Lines (x_A/x_B Ports)

$T_A$ = –40°C to 85°C unless otherwise specified

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OHA}$ | | $I_{OH}$ = –10 µA, | $V_I = V_{IH}$ | 1.1 V to 3.6 V | $V_{CCA}$ × 0.8 | | | V |
| $V_{OLA}$ | | $I_{OL}$ = 10 µA, | $V_I = V_{IL}$ | 1.1 V to 3.6 V | | $V_{CCA}$ × 0.17 | | V |
| $V_{OHB}$ | | $I_{OH}$ = –10 µA, | $V_I = V_{IH}$ | | 5VOUT × 0.9 | | | V |
| $V_{OLB}$ | | $I_{OL}$ = 3 mA, | $V_I = V_{IL}$ | | | | 0.4 | V |
| $\Delta V_T$ hysteresis | SDx_A ($V_{T+} – V_{T–}$) | | | 1.1 V to 3.6 V | | 40 | | mV |
| | SDx_B ($V_{T+} – V_{T–}$) | | | 1.1 V to 3.6 V | | 400 | | |
| $R_{PU}$ | (Internal pullup) | SCL_A, SDA_A, | Internal pullup connected to $V_{CCA}$ rail | | | 10 | | kΩ |
| | | SCL_B, SDA_B, | Internal pullup connected to 5-V rail | | | 1.75 | | |
| $I_{PULLUPAC}$ | Transient boosted pullup current (rise time accelerator) | SCL_B, SDA_B, | Internal pullup connected to 5-V rail | | | 15 | | mA |
| $I_{OFF}$ | A port | $V_{CCA}$ = 0 V, $V_I$ or $V_O$ = 0 to 3.6 V | | 0 V | | | ±5 | µA |
| | B port | 5VOUT = 0 V, $V_I$ or $V_O$ = 0 to 5.5 V | | 0 V to 3.6 V | | | ±5 | |
| $I_{OZ}$ | B port | $V_O = V_{CCO}$ or GND | | 1.1 V to 3.6 V | | | ±5 | µA |
| | A port | $V_I = V_{CCI}$ or GND | | 1.1 V to 3.6 V | | | ±5 | |

## 6.10 Electrical Characteristics: Voltage Level Shifter: CEC Lines (x_A/x_B Ports)

$T_A$ = –40°C to 85°C unless otherwise specified

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OHA}$ | | $I_{OH}$ = –10 µA, | $V_I = V_{IH}$ | 1.1 V to 3.6 V | $V_{CCA}$ × 0.8 | | | V |
| $V_{OLA}$ | | $I_{OL}$ = 10 µA, | $V_I = V_{IL}$ | 1.1 V to 3.6 V | | $V_{CCA}$ × 0.17 | | V |
| $V_{OHB}$ | | $I_{OH}$ = –10 µA, | $V_I = V_{IH}$ | | $V_{3P3}$ × 0.9 | | | V |
| $V_{OLB}$ | | $I_{OL}$ = 3 mA, | $V_I = V_{IL}$ | | | | 0.4 | V |
| $\Delta V_T$ hysteresis | CEC_A ($V_{T+} – V_{T–}$) | | | 1.1 V to 3.6 V | | 40 | | mV |
| | CEC_B ($V_{T+} – V_{T–}$) | | | 1.1 V to 3.6 V | | 300 | | |
| $R_{PU}$ | (Internal pullup) | CEC_A | Internal pullup connected to $V_{CCA}$ rail | | | 10 | | kΩ |
| | | CEC_B | Internal pullup connected to internal 3.3-V rail | | | 26 | | |
| $I_{OFF}$ | A port | $V_{CCA}$ = 0 V, $V_I$ or $V_O$ = 0 to 3.6 V | | 0 V | | | ±5 | µA |
| | B port | 5VOUT = 0 V, $V_I$ or $V_O$ = 0 to 5.5 V | | 0 V to 3.6 V | | | ±1.8 | |
| $I_{OZ}$ | B port | $V_O = V_{CCO}$ or GND | | 1.1 V to 3.6 V | | | ±5 | µA |
| | A port | $V_I = V_{CCI}$ or GND | | 1.1 V to 3.6 V | | | ±5 | |

## 6.11 Electrical Characteristics: Voltage Level Shifter: HPD Line (x_A/x_B Ports)

$T_A$ = –40°C to 85°C unless otherwise specified

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OHA}$ | | $I_{OH}$ = –3 mA, | $V_I = V_{IH}$ | 1.1 V to 3.6 V | $V_{CCA}$ × 0.7 | | | V |
| $V_{OLA}$ | | $I_{OL}$ = 3 mA, | $V_I = V_{IL}$ | 1.1 V to 3.6 V | | $V_{CCA}$ ×0.17 | | V |
| $\Delta V_T$ hysteresis | HPD_B ($V_{T+} – V_{T–}$) | | | 1.1 V to 3.6 V | | 700 | | mV |
| $R_{PD}$ | (Internal pulldown) | HPD_B, | Internal pulldown connected to GND | | | 11 | | kΩ |
| $I_{OFF}$ | A port | $V_O = V_{CCO}$ or GND | | 0 V | | | ±5 | µA |
| $I_{OZ}$ | A port | $V_I = V_{CCI}$ or GND | | 3.6 V | | | ±5 | µA |

## 6.12 Electrical Characteristics: LS_OE, CT_CP_HPD

$T_A$ = –40°C to 85°C unless otherwise specified

| PARAMETER | TEST CONDITIONS | $V_{CCA}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_I$ | $V_I$ = $V_{CCA}$ or GND | 1.1 V to 3.6 V | | | ±12 | µA |

## 6.13 Electrical Characteristics: I/O Capacitance

$T_A$ = –40°C to 85°C unless otherwise specified

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_I$ | Control inputs | $V_I$ = 1.89 V or GND | 1.1 V to 3.6 V | | 7.1 | 8.5 | pF |
| $C_{IO}$ | A port | $V_O$ = 1.89 V or GND | 1.1 V to 3.6 V | | 8.3 | 9.5 | pF |
| | B port | $V_O$ = 5.0 V or GND | 1.1 V to 3.6 V | | 15 | 16.5 | |

## 6.14 Switching Characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_L$ | Bus load capacitance (B side) | | | | 750 | pF |
| | Bus load capacitance (A side) | | | | 15 | |

## 6.15 Switching Characteristics: Voltage Level Shifter: SCL, SDA Lines (x_A & x_B ports); $V_{CCA}$ = 1.2 V

$V_{CCA}$ = 1.2 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation delay | A to B | DDC Channels Enabled | | 344 | | ns |
| | | B to A | | | 335 | | |
| $t_{PLH}$ | Propagation delay | A to B | DDC Channels Enabled | | 452 | | ns |
| | | B to A | | | 178 | | |
| $t_f$ | A port fall time | A Port | DDC Channels Enabled | | 138 | | ns |
| | B port fall time | B Port | | | 83 | | |
| $t_r$ | A port rise time | A Port | DDC Channels Enabled | | 194 | | ns |
| | B port rise time | B Port | | | 92 | | |
| $f_{MAX}$ | Maximum switching frequency | | DDC Channels Enabled | 400 | | | kHz |

## 6.16 Switching Characteristics: Voltage Level Shifter: CEC Line (x_A & x_B ports); $V_{CCA}$ = 1.2 V

$V_{CCA}$ = 1.2 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | A to B | CEC Channels Enabled | | 445 | | ns |
| | | B to A | | | 337 | | |
| $t_{PLH}$ | | A to B | | | 13 | | µs |
| | | B to A | | | 0.266 | | |
| $t_f$ | A port fall time | A Port | CEC Channels Enabled | | 140 | | ns |
| | B port fall time | B Port | | | 96 | | |
| $t_r$ | A port rise time | A Port | CEC Channels Enabled | | 202 | | ns |
| | B port rise time | B Port | | | 15 | | µs |

## 6.17 Switching Characteristics: Voltage Level Shifter: HPD Line (x_A & x_B ports); $V_{CCA}$ = 1.2 V

$V_{CCA}$ = 1.2 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | B to A | CEC Channels Enabled | | 10 | | µs |
| $t_{PLH}$ | | B to A | | | 9 | | |
| $t_f$ | A port fall time | A Port | CEC Channels Enabled | | 0.67 | | ns |
| $t_r$ | A port rise time | A Port | CEC Channels Enabled | | 0.74 | | ns |

## 6.18 Switching Characteristics: Voltage Level Shifter: SCL, SDA Lines (x_A & x_B ports); $V_{CCA}$ = 1.5 V

$V_{CCA}$ = 1.5 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | A to B | DDC Channels Enabled | | 335 | | ns |
| | | B to A | | | 265 | | |
| $t_{PLH}$ | | A to B | | | 438 | | |
| | | B to A | | | 169 | | |
| $t_f$ | A port fall time | A Port | DDC Channels Enabled | | 110 | | ns |
| | B port fall time | B Port | | | 83 | | |
| $t_r$ | A port rise time | A Port | DDC Channels Enabled | | 190 | | ns |
| | B port rise time | B Port | | | 92 | | |
| $f_{MAX}$ | Maximum switching frequency | | DDC Channels Enabled | 400 | | | kHz |

## 6.19 Switching Characteristics: Voltage Level Shifter: CEC Line (x_A & x_B ports); $V_{CCA}$ = 1.5 V

$V_{CCA}$ = 1.5 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | A to B | CEC Channels Enabled | | 437 | | ns |
| | | B to A | | | 267 | | |
| $t_{PLH}$ | | A to B | | | 13 | | µs |
| | | B to A | | | 0.264 | | |
| $t_f$ | A port fall time | A Port | CEC Channels Enabled | | 110 | | ns |
| | B port fall time | B Port | | | 96 | | |
| $t_r$ | A port rise time | A Port | CEC Channels Enabled | | 202 | | ns |
| | B port rise time | B Port | | | 15 | | µs |

## 6.20 Switching Characteristics: Voltage Level Shifter: HPD Line (x_A & x_B ports); $V_{CCA}$ = 1.5 V

$V_{CCA}$ = 1.5 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | B to A | CEC Channels Enabled | | 10 | | µs |
| $t_{PLH}$ | | B to A | | | 9 | | |
| $t_f$ | A port fall time | A Port | CEC Channels Enabled | | 0.47 | | ns |
| $t_r$ | A port rise time | A Port | CEC Channels Enabled | | 0.51 | | ns |

## 6.21 Switching Characteristics: Voltage Level Shifter: SCL, SDA Lines (x_A & x_B ports); $V_{CCA}$ = 1.8 V

$V_{CCA}$ = 1.8 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | A to B | DDC Channels Enabled | | 334 | | ns |
| | | B to A | | | 229 | | |
| $t_{PLH}$ | | A to B | | | 431 | | |
| | | B to A | | | 169 | | |
| $t_f$ | A port fall time | A Port | DDC Channels Enabled | | 94 | | ns |
| | B port fall time | B Port | | | 83 | | |
| $t_r$ | A port rise time | A Port | DDC Channels Enabled | | 191 | | ns |
| | B port rise time | B Port | | | 92 | | |
| $f_{MAX}$ | Maximum switching frequency | | DDC Channels Enabled | 400 | | | kHz |

## 6.22 Switching Characteristics: Voltage Level Shifter: CEC Line (x_A & x_B ports); $V_{CCA}$ = 1.8 V

$V_{CCA}$ = 1.8 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | A to B | CEC Channels Enabled | | 441 | | ns |
| | | B to A | | | 231 | | |
| $t_{PLH}$ | | A to B | | | 13 | | µs |
| | | B to A | | | 0.26 | | |
| $t_f$ | A port fall time | A Port | CEC Channels Enabled | | 94 | | ns |
| | B port fall time | B Port | | | 96 | | |
| $t_r$ | A port rise time | A Port | CEC Channels Enabled | | 201 | | ns |
| | B port rise time | B Port | | | 15 | | µs |

## 6.23 Switching Characteristics: Voltage Level Shifter: HPD Line (x_A & x_B ports); $V_{CCA}$ = 1.8 V

$V_{CCA}$ = 1.8 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | B to A | CEC Channels Enabled | | 10 | | µs |
| $t_{PLH}$ | | B to A | | | 9 | | |
| $t_f$ | A port fall time | A Port | CEC Channels Enabled | | 0.41 | | ns |
| $t_r$ | A port rise time | A Port | CEC Channels Enabled | | 0.45 | | ns |

## 6.24 Switching Characteristics: Voltage Level Shifter: SCL, SDA Lines (x_A & x_B ports); $V_{CCA}$ = 2.5 V

$V_{CCA}$ = 2.5 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | A to B | DDC Channels Enabled | | 330 | | ns |
| | | B to A | | | 182 | | |
| $t_{PLH}$ | | A to B | | | 423 | | |
| | | B to A | | | 166 | | |
| $t_f$ | A port fall time | A Port | DDC Channels Enabled | | 79 | | ns |
| | B port fall time | B Port | | | 83 | | |
| $t_r$ | A port rise time | A Port | DDC Channels Enabled | | 188 | | ns |
| | B port rise time | B Port | | | 92 | | |
| $f_{MAX}$ | Maximum switching frequency | | DDC Channels Enabled | 400 | | | kHz |

## 6.25 Switching Characteristics: Voltage Level Shifter: CEC Line (x_A & x_B ports); $V_{CCA}$ = 2.5 V

$V_{CCA}$ = 2.5 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | A to B | CEC Channels Enabled | | 454 | | ns |
| | | B to A | | | 184 | | |
| $t_{PLH}$ | | A to B | | | 13 | | µs |
| | | B to A | | | 0.255 | | |
| $t_f$ | A port fall time | A Port | CEC Channels Enabled | | 79 | | ns |
| | B port fall time | B Port | | | 96 | | |
| $t_r$ | A port rise time | A Port | CEC Channels Enabled | | 194 | | ns |
| | B port rise time | B Port | | | 15 | | µs |

## 6.26 Switching Characteristics: Voltage Level Shifter: HPD Line (x_A & x_B ports); $V_{CCA}$ = 2.5 V

$V_{CCA}$ = 2.5 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | B to A | CEC Channels Enabled | | 10 | | µs |
| $t_{PLH}$ | | B to A | | | 9 | | |
| $t_f$ | A port fall time | A Port | CEC Channels Enabled | | 0.37 | | ns |
| $t_r$ | A port rise time | A Port | CEC Channels Enabled | | 0.39 | | ns |

## 6.27 Switching Characteristics: Voltage Level Shifter: SCL, SDA Lines (x_A & x_B ports); $V_{CCA}$ = 3.3 V

$V_{CCA}$ = 3.3 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | A to B | DDC channels enabled | | 323 | | ns |
| | | B to A | | | 158 | | |
| $t_{PLH}$ | | A to B | | | 421 | | |
| | | B to A | | | 162 | | |
| $t_f$ | A port fall time | A Port | DDC channels enabled | | 71 | | ns |
| | B port fall time | B Port | | | 84 | | |
| $t_r$ | A port rise time | A Port | DDC channels enabled | | 188 | | ns |
| | B port rise time | B Port | | | 92 | | |
| $f_{MAX}$ | Maximum switching frequency | | DDC channels enabled | 400 | | | kHz |

## 6.28 Switching Characteristics: Voltage Level Shifter: CEC Line (x_A & x_B ports); $V_{CCA}$ = 3.3 V

$V_{CCA}$ = 3.3 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | A to B | CEC channels enabled | | 450 | | ns |
| | | B to A | | | 160 | | |
| $t_{PLH}$ | | A to B | | | 13 | | µs |
| | | B to A | | | 0.251 | | |
| $t_f$ | A port fall time | A Port | CEC channels enabled | | 71 | | ns |
| | B port fall time | B Port | | | 96 | | |
| $t_r$ | A port rise time | A Port | CEC channels enabled | | 194 | | ns |
| | B port rise time | B Port | | | 15 | | µs |

## 6.29 Switching Characteristics: Voltage Level Shifter: HPD Line (x_A & x_B ports); $V_{CCA}$ = 3.3 V

$V_{CCA}$ = 3.3 V

| PARAMETER | | PINS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | B to A | CEC channels enabled | | 10 | | µs |
| $t_{PLH}$ | | B to A | | | 9 | | |
| $t_f$ | A port fall time | A Port | CEC channels enabled | | 0.35 | | ns |
| $t_r$ | A port rise time | A Port | CEC channels enabled | | 0.37 | | ns |

## 6.30 Typical Characteristics

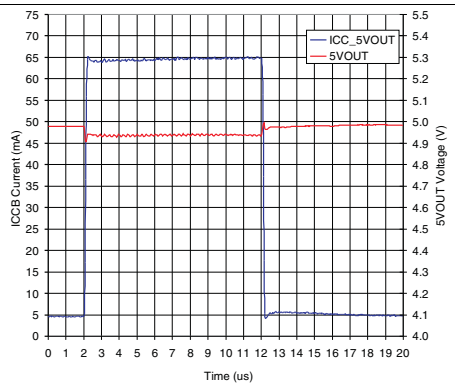



**Figure 1. Load Transient Response**

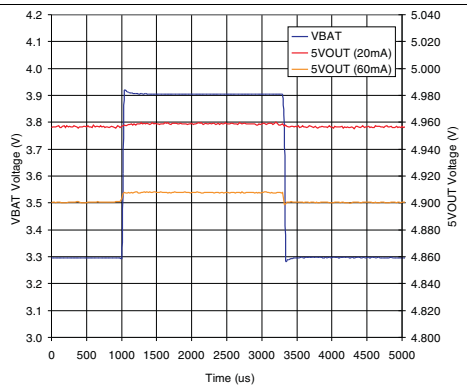



**Figure 2. Line Transient Response**

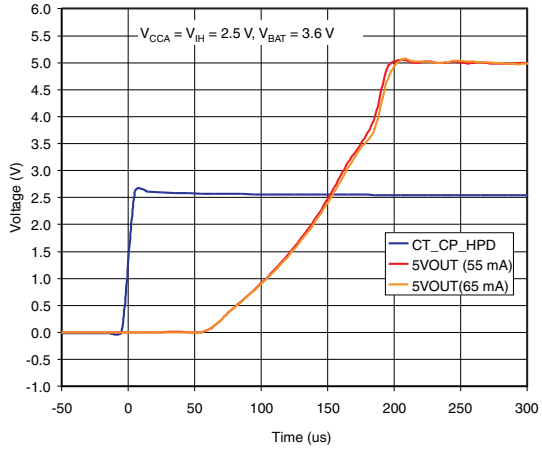



**Figure 3. $t_{START}$**

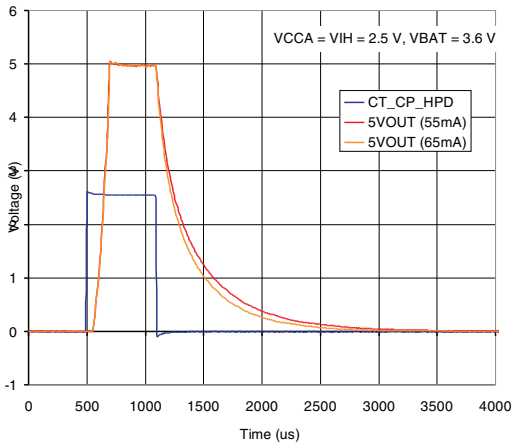



**Figure 4. DC-DC Start-Up and Shutdown**

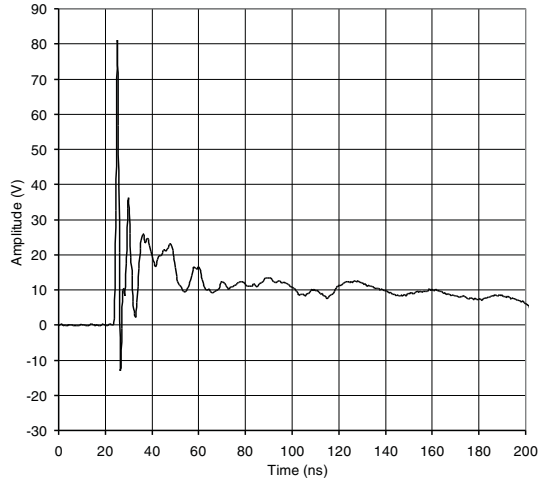



**Figure 5. IEC Clamping Waveforms 8-kV Contact (IEC ESD Pins)**

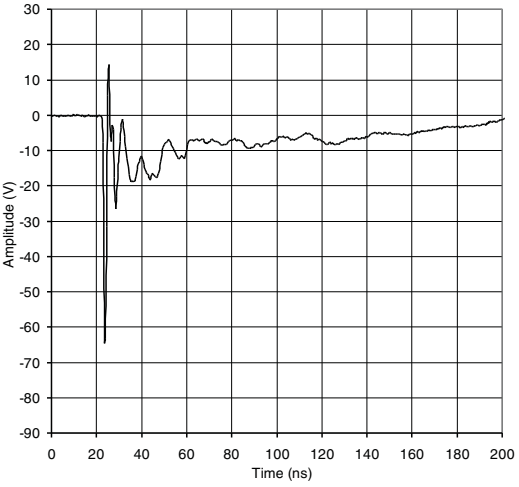



**Figure 6. IEC Clamping Waveforms –8-kV Contact (IEC ESD Pins)**

## Typical Characteristics (continued)

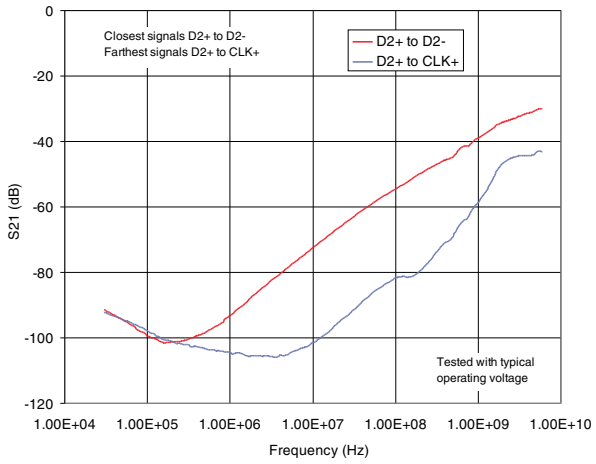



**Figure 7. Channel-to-Channel Crosstalk**

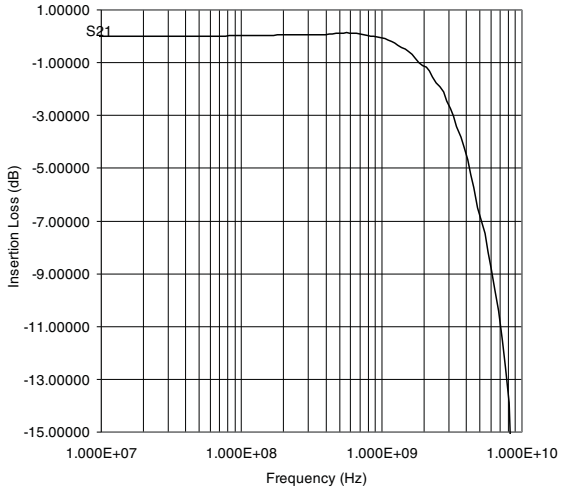



**Figure 8. Insertion Loss Data Line to GND**

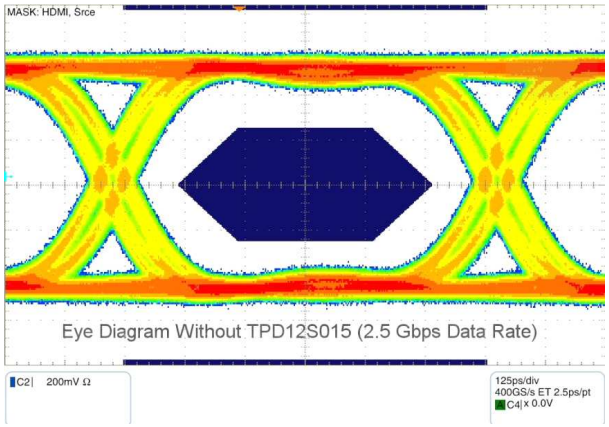



**Figure 9. Eye Diagram Performance on a Test Board for the D+, D– Lines at 2.5 Gbps**

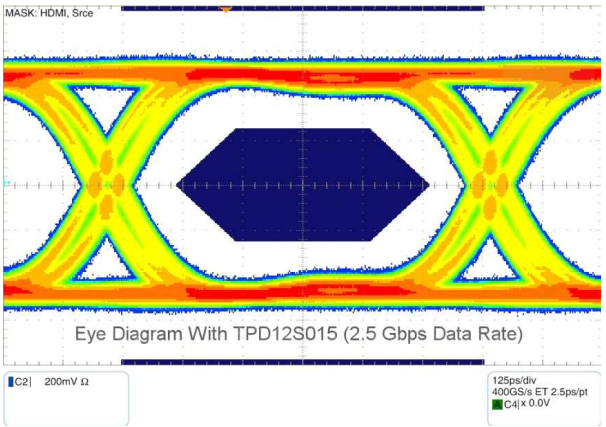



**Figure 10. Eye Diagram Performance on a Test Board for the D+, D– Lines at 2.5 Gbps**

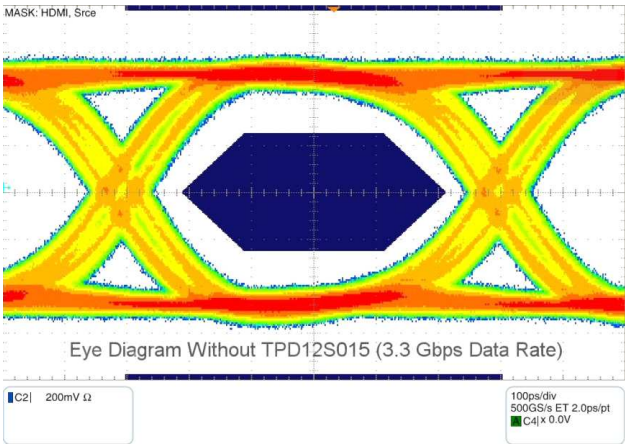



**Figure 11. Eye Diagram Performance on a Test Board for the D+, D– Lines at 3.3 Gbps**

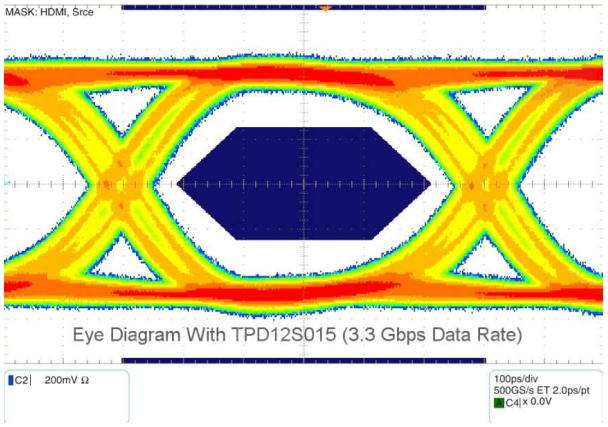



**Figure 12. Eye Diagram Performance on a Test Board for the D+, D– Lines at 3.3 Gbps**

# 7 Parameter Measurement Information

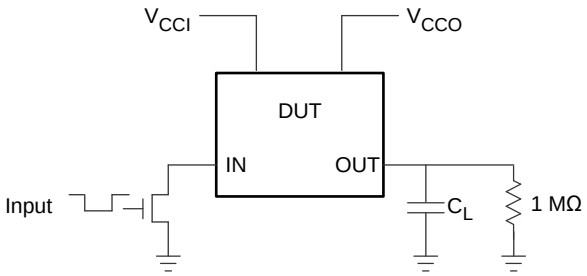
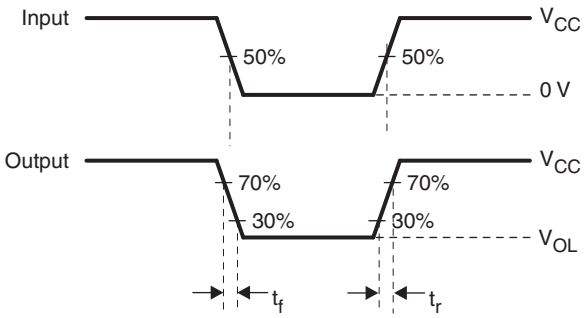





**Figure 13. Test Circuit**

**Table 2. Design Parameters**

| PIN | $C_L$ |
|---|---|
| DDC, CEC (A side) | 750 pF |
| DDC, CEC, HPD (B side) | 15 pF |




A. $R_T$ termination resistance should be equal to $Z_{OUT}$ of pulse generators.

B. $C_L$ includes probe and jig capacitance.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, slew rate ≥ 1 V/ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 14. Test Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

The TPD12S015 is an integrated interface solution for HDMI 1.3 and 1.4 interfaces, for both portable and non-portable electronics applications. The device has a boost DC-DC converter that uses the 2.3-V to 5.5-V internal power supply and outputs regulated 5-V standard compliant power supply to the cable. This power supply output has current limit and short-circuit protection function. There are bidirectional level-shifting and signal-conditioning circuits on CEC, SCL, and SDA with pullup resistors integrated to minimize the external passive discrete component use. There is also a unidirectional level shifter for HPD signal that translates the 5-V HPD down to $V_{CCA}$ level. The HPD_B port has a glitch filter to avoid false detection due to the bouncing while inserting the HDMI plug. For the eight TMDS lines, there are high-speed ESD diodes on each line to make sure that the system pass 8-kV contact ESD.

## 8.2 Functional Block Diagrams

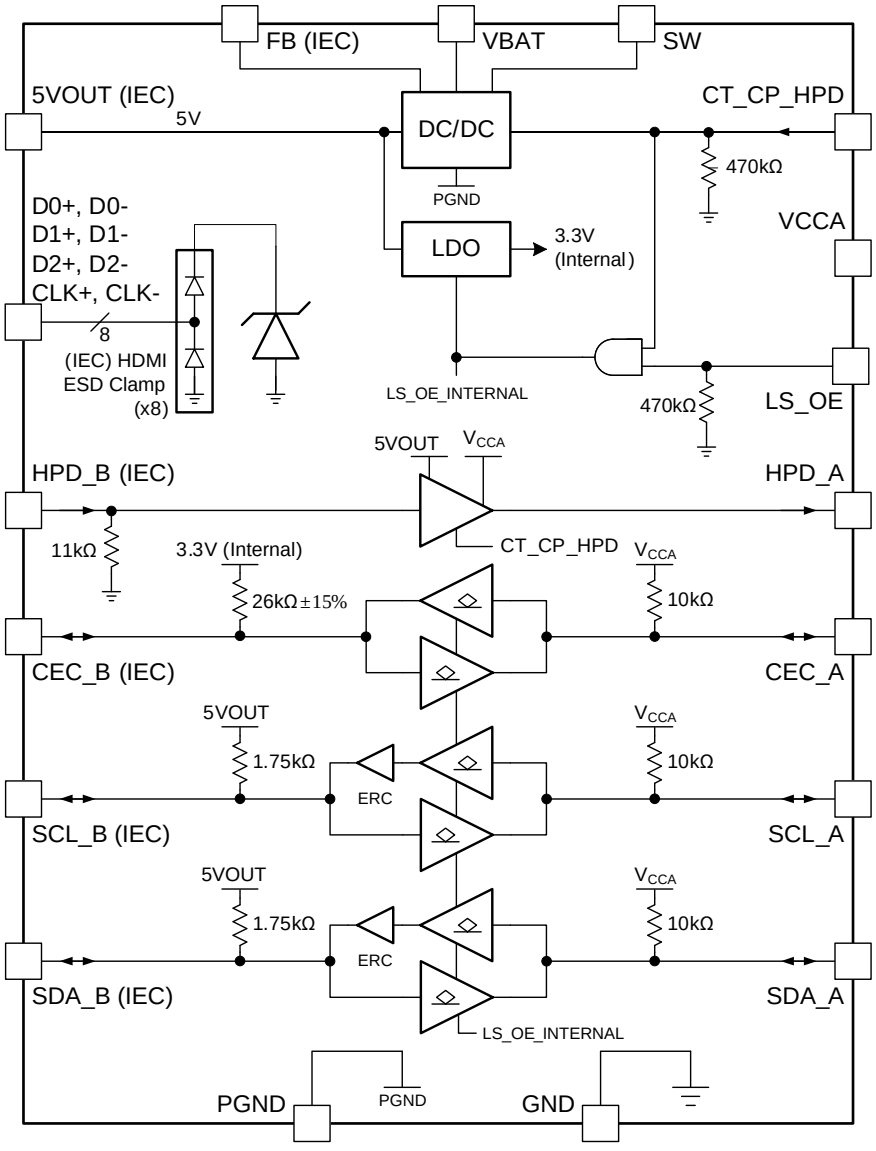





**Figure 15. Circuit Block Diagram**

## Functional Block Diagrams (continued)

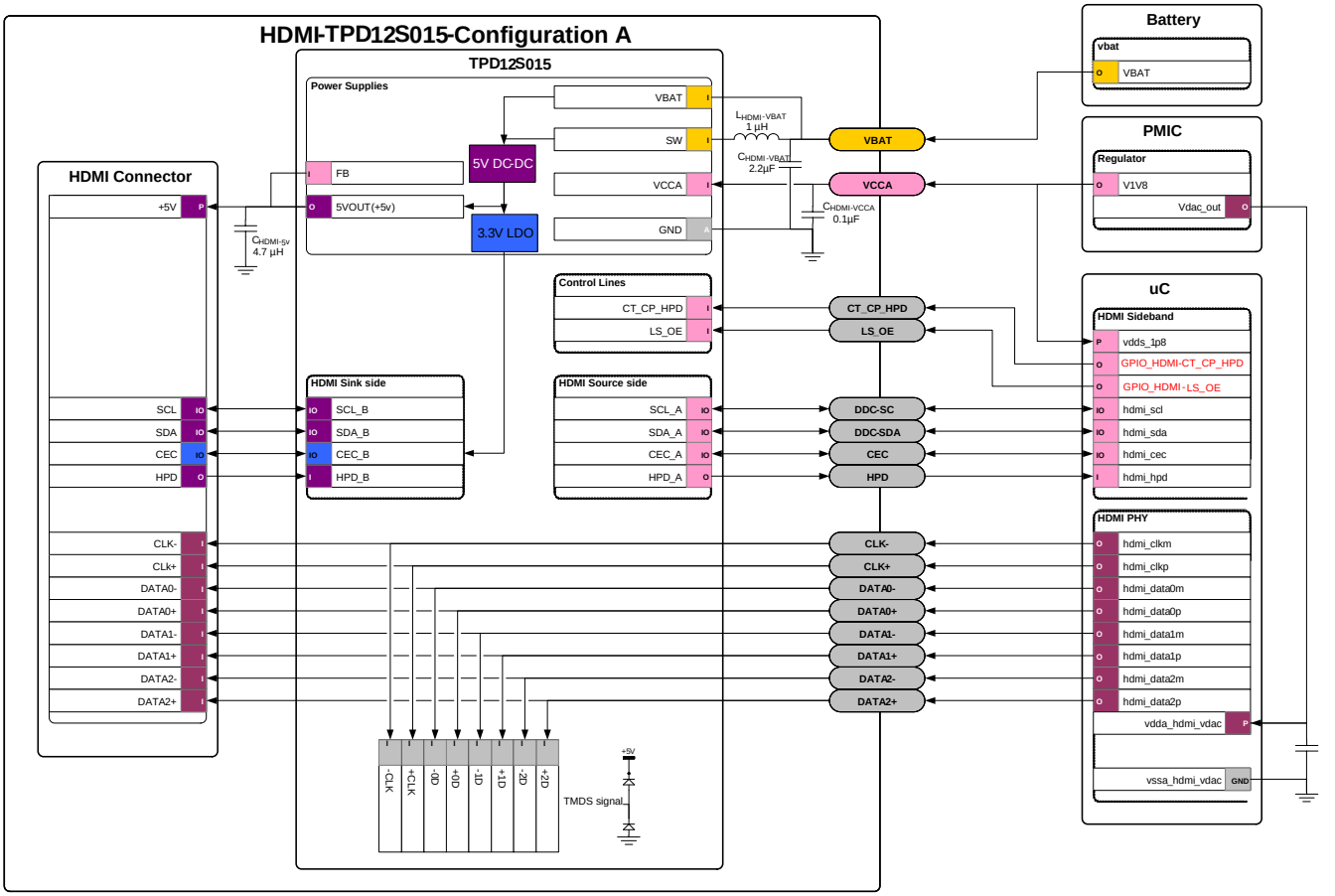





**Figure 16. System-Level Block Diagram**

## 8.3 Feature Description

### 8.3.1 Rise-Time Accelerators

The HDMI cable side of the DDC lines incorporates rise-time accelerators to support the high-capacitive load on the HDMI cable side. The rise-time accelerator boosts the cable side DDC signal, independent to which side of the bus is releasing the signal.

### 8.3.2 Internal Pullup Resistor

The TPD12S015 has incorporated all the required pullup and pulldown resistors at the interface pins. The system is designed to work properly with no external pullup resistors on the DDC, CEC, and HPD lines. For proper system operation, no external resistors are placed at the A and B ports. If there are internal pullups at the host processor, they must be disabled.

### 8.3.3 Undervoltage Lockout

The undervoltage lockout circuit prevents the DC-DC converter from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling $V_{IN}$ trips the undervoltage lockout threshold $V_{BATUV}$. The undervoltage lockout threshold $V_{BATUV}$ for falling $V_{IN}$ is typically 2 V. The device starts operation once the rising VIN trips undervoltage lockout threshold $V_{BATUV}$ again at typical 2.1 V.

## Feature Description (continued)

### 8.3.4 Soft Start

The DC-DC converter has an internal soft-start circuit that controls the ramp-up of the output voltage. The output voltage reaches its nominal value within $t_{Start}$ of typically 250 µs after CT_CP_HPD pin has been pulled to high level. The output voltage ramps up from 5% to its nominal value within $t_{Ramp}$ of 300 µs. This limits the inrush current in the converter during start-up and prevents possible input voltage drops when a battery or high-impedance power source is used. During soft start, the switch current limit is reduced to 300 mA until the output voltage reaches $V_{IN}$. Once the output voltage trips this threshold, the device operates with its nominal current limit ILIMF.

### 8.3.5 DDC and CEC Level-Shifting Circuit Operation

The TPD12S015 enables DDC translation from $V_{CCA}$ (system side) voltage levels to 5-V (HDMI cable side) voltage levels without degradation of system performance. The TPD12S015 contains two bidirectional open-drain buffers specifically designed to support up-translation or down-translation between the low voltage, $V_{CCA}$ side DDC-bus, and the 5-V DDC-bus. The port B I/Os are overvoltage tolerant to 5.5 V even when the device is unpowered. After power up and with the LS_OE and CT_CP_HPD pins high, a low level on port A (below approximately $V_{ILC} = 0.08 \times V_{CCA}$ V) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to $V_{OLB}$ V. When port A rises above approximately $0.10 \times V_{CCA}$ V, the port B pulldown driver is turned off and the internal pullup resistor pulls the pin high. When port B falls first and goes below 0.3 × 5VOUT, a CMOS hysteresis input buffer detects the falling edge, turns on the port A driver, and pulls port A down to approximately $V_{OLA} = 0.16 \times V_{CCA}$ V. The port B pulldown is not enabled unless the port A voltage goes below $V_{ILC}$. If the port A low voltage goes below $V_{ILC}$, the port B pulldown driver is enabled until port A rises above ($V_{ILC} + \Delta V_{T\text{-}HYSTA}$), then port B, if not externally driven LOW, continues to rise being pulled up by the internal pullup resistor.

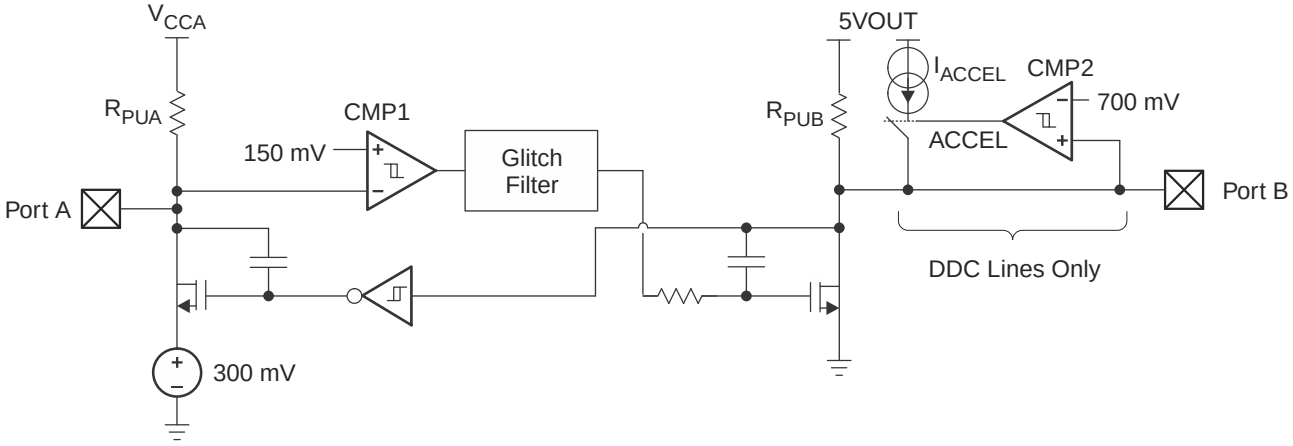





**Figure 17. DDC and CEC Level Shifter Block Diagram**

### 8.3.6 DDC and CEC Level Shifting Operation When $V_{CCA}$ = 1.8 V

- The threshold of CMP1 is approximately 150 mV ± the 40 mV of total hysteresis.
- The comparator trips for a falling waveform at approximately 130 mV
- The comparator trips for a rising waveform at approximately 170 mV
- To be recognized as a zero, the level at Port A must first go below 130 mV (VILC in spec) and then stay below 170 mV (VILA in spec)
- To be recognized as a one, the level at A must first go above 170 mV and then stay above 130 mV
- VILC is set to 110 mV to give some margin to the 130 mV
- VILA is set to 140 mV to give some margin to the 170 mV
- VIHA is set to 70% of $V_{CCA}$ to be consistent with standard CMOS levels

## Feature Description (continued)

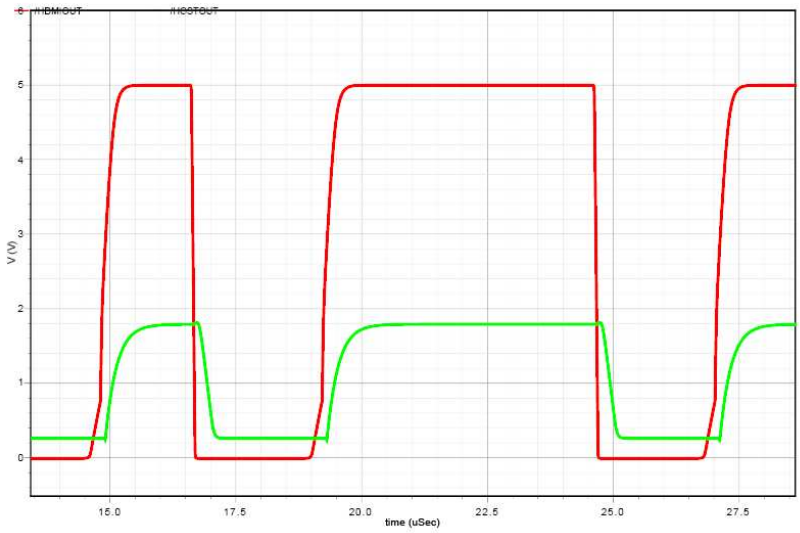



**Figure 18. DDC and CEC Level-Shifting Operation (B to A Direction)**

### 8.3.7 CEC Level-Shifting Operation

The CEC level-shifting function operates in the same manner as the DDC lines except that the CEC line does not need the rise time accelerator function.

## 8.4 Device Functional Modes

### 8.4.1 Enable

The DC-DC converter is enabled when the CT_CP_HPD is set to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltage reaches its nominal value in typically 250 µs after the device has been enabled. The CT_CP_HPD input can be used to control power sequencing in a system with various DC-DC converters. The CT_CP_HPD pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With CT_CP_HPD = GND, the DC-DC enters shutdown mode.

### 8.4.2 Power Save Mode

The TPD12S015 integrates a power save mode to improve efficiency at light load. In power save mode, the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage. The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TPD12S015 is an integrated solution for HDMI 1.3 and 1.4 interface. The device has a boost converter on the power supply, signal conditioning circuits on CEC, SCL, SDA, HPD lines, and ESD protection on the TMDS lines. To get the best performance, see *Design Requirements*, *Detailed Design Procedure*, and *Application Curves*.

## 9.2 Typical Applications

### 9.2.1 TPD12S015 Controlled by Two GPIOs from Controller

Some HDMI controller chips may have two GPIOs to control the HDMI interface chip. Figure 19 shows how TPD12S015 is used in this situation.

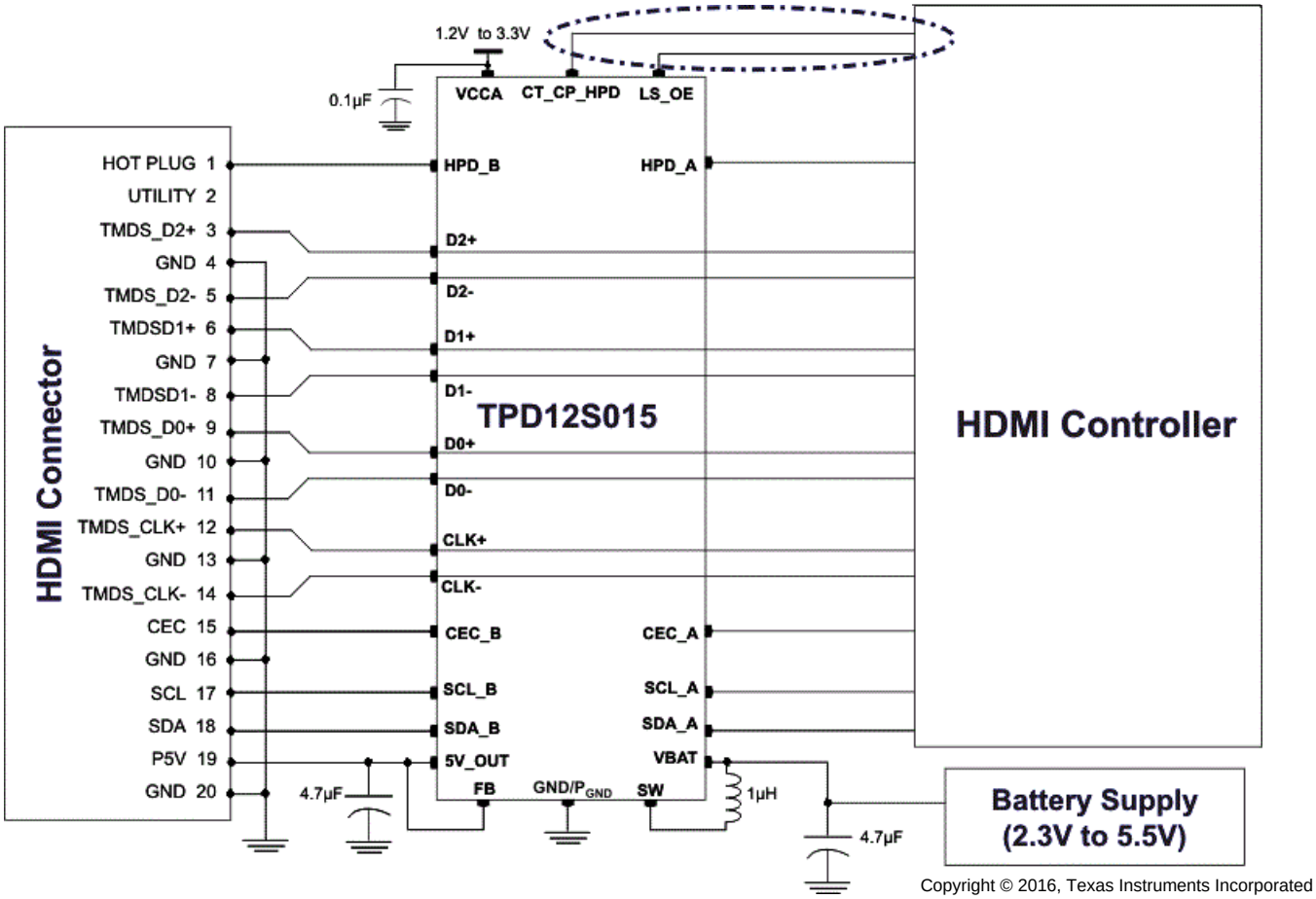



**Figure 19. TPD12S015 Controlled by Two GPIOs from Controller Schematic**

#### *9.2.1.1 Design Requirements*

Table 3 lists the known system parameters for an HDMI 1.4 application.

**Table 3. Design Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| 5V_OUT DC current | 55 mA |
| CEC_A, HPD_A, SCL_A, SDA_A voltage level | $V_{CCA}$ |
| HDMI data rate per TMDS signal pair | 3.4 Gbps |
| Required IEC 61000-4-2 ESD Protection | ±8-kV Contact |

### *9.2.1.2 Detailed Design Procedure*

#### 9.2.1.2.1 Inductor Selection

To make sure that the TPD12S015 devices can operate, an inductor must be connected between pin $V_{BAT}$ and pin SW. A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, TI recommends keeping the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. The highest peak current through the inductor and the switch depends on the output load, the input ($V_{BAT}$), and the output voltage (5VOUT). Estimation of the maximum average inductor current can be done using Equation 1.

$$I_{L\_MAX} \approx I_{OUT} \times \frac{V_{OUT}}{\eta \times V_{IN}} \tag{1}$$

For example, for an output current of 55 mA at 5VOUT, approximately 150 mA of average current flows through the inductor at a minimum input voltage of 2.3 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system size and cost. With these parameters, it is possible to calculate the value of the minimum inductance by using Equation 2.

$$L_{MIN} \approx \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\Delta I_L \times f \times V_{OUT}} \tag{2}$$

where

- f is the switching frequency
- $\Delta I_L$ is the ripple current in the inductor, that is, 20% × $I_L$

With this calculated value and the calculated currents, it is possible to choose a suitable inductor. In typical applications, TI recommends an inductance of 1 µH, even if Equation 2 yields something lower. Take care so that load transients and losses in the circuit can lead to higher currents as estimated in Equation 3. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

With the chosen inductance value, the peak current for the inductor in steady-state operation can be calculated. Equation 3 shows how to calculate the peak current I.

$$I_{L(peak)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1 - D) \times \eta} \tag{3}$$

where

- $D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$

This would be the critical value for the current rating for selecting the inductor. Also consider that load transients and error conditions may cause higher inductor currents.

#### 9.2.1.2.2 Input Capacitor

Because of the nature of the boost converter having a pulsating input current, a low-ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. TI recommends at least a 1.2-µF input capacitor to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. TI recommends placing a ceramic capacitor as close as possible to the $V_{IN}$ and GND pins; to improve the input noise filtering, it is better to use a 4.7-µF capacitor.

#### 9.2.1.2.3 Output Capacitor

For the output capacitor, TI recommends using small ceramic capacitors placed as close as possible to the $V_{OUT}$ and GND pins of the IC. If, for any reason, the application requires the use of large capacitors that cannot be placed close to the IC, TI recommends using a smaller ceramic capacitor in parallel to the large one. This small capacitor must be placed as close as possible to the $V_{OUT}$ and GND pins of the IC. Use Equation 4 to estimate the recommended minimum output capacitance.

$$C_{min} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}}$$

where

- f is the switching frequency
- ΔV is the maximum allowed ripple (4)

With a chosen ripple voltage of 10 mV, a minimum effective capacitance of 2.7 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 5.

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (5)$$

A capacitor with a value in the range of the calculated minimum must be used. This is required to maintain control loop stability. There are no additional requirements regarding minimum ESR. There is no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

**NOTE**

Ceramic capacitors have a DC Bias effect, which have a strong influence on the final effective capacitance needed. Therefore the right capacitor value has to be chosen very carefully.

Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and the effective capacitance. The minimum effective capacitance value should be 1.2 µF, but the preferred value is about 4.7 µF.

**Table 4. Passive Components: Recommended Minimum Effective Values**

| COMPONENT | MIN | TARGET | MAX | UNIT |
|---|---|---|---|---|
| $C_{IN}$ | 1.2 | 4.7 | 6.5 | µF |
| $C_{OUT}$ | 1.2 | 4.7 | 10 | µF |
| $L_{IN}$ | 0.7 | 1 | 1.3 | µH |

#### 9.2.1.2.4 CEC, HPD, SCL, and SDA Level-Shifting Function

To accommodate for the lower logic levels of some processors' control lines, level shifters are needed to translate the interface voltage down to $V_{CCA}$, the voltage level used by the processor. The TPD12S015 has bidirectional level shifters on CEC, SCL, and SDA lines to support the two-way communication. The pullup resistors are integrated to minimize the number of external components. For HPD line, only one way of hot-plug indication is needed, the level shifter is unidirectional. There is a built-in HPD_B pulldown resistor to keep the voltage level low on the connector side when nothing is attached. Apart from the signal level translation, the rise-time accelerators on the connector side increases the load driving capability.

#### 9.2.1.2.5 ESD

To get the best ESD performance on the interface side pins, high-performance ESD diodes are needed. The TPD12S015's ESD diodes on D0+, D0-, D1+, D1-, D2+, D2-, CLK+, CLK-, SCL_B, SDA_B, CEC_B, HPD_B, 5VOUT, and FB ensure passing 8-kV contact IEC, the highest level ESD. Signal integrity on TMDS lines is also a design concern that must be evaluated to meet the HDMI 1.3 or 1.4 data rate. With the typical I/O capacitance of 1.3 pF and a bandwidth above 3 GHz, Figure 11 shows that TPD12S015's ESD structure has enough margin to meet the data rate requirement of HDMI 1.3 or 1.4.

#### 9.2.1.2.6 Ground Offset Consideration

Ground offset between the TPD12S015 ground and the ground of devices on port A of the TPD12S015 must be avoided. The reason for this cautionary remark is that a CMOS or NMOS open-drain capable of sinking 3 mA of current at 0.4 V has an output resistance of 133 Ω or less. Such a driver shares enough current with the port A output pulldown of the TPD12S015 to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Because VILC can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset must not exceed 50 mV. Bus repeaters that use an output offset are not interoperable with the port A of the TPD12S015 as their output LOW levels are not recognized by the TPD12S015 as a LOW. If the TPD12S015 is placed in an application where the VIL of port A of the TPD12S015 does not go below its VILC it pulls port B LOW initially when port A input transitions LOW but the port B returns HIGH, so it does not reproduce the port A input on port B. Such applications must be avoided. Port B is interoperable with all $I^2C$ bus slaves, masters, and repeaters.

### *9.2.1.3 Application Curves*

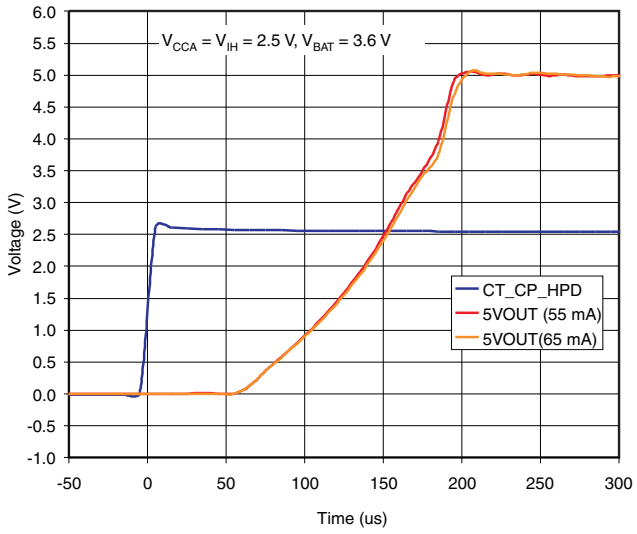



**Figure 20. $t_{START}$**

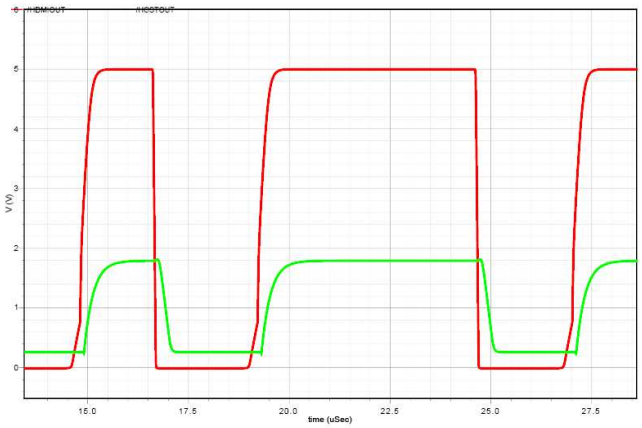



**Figure 21. DDC and CEC Level Shifting Operation (B to A Direction)**

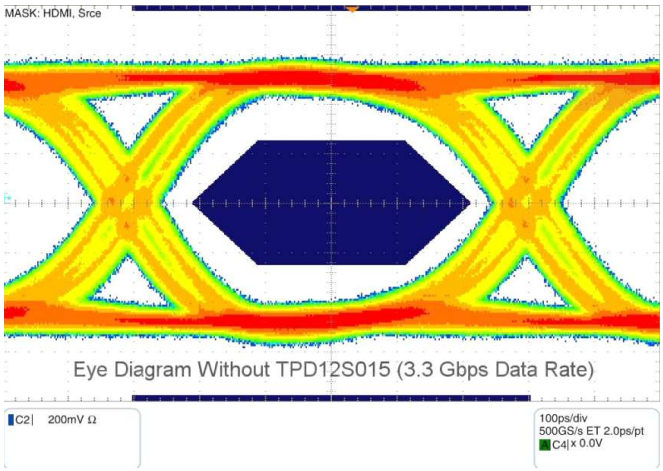



**Figure 22. Eye Diagram Performance on a Test Board for the D+ and D– Lines at 3.3 Gbps**

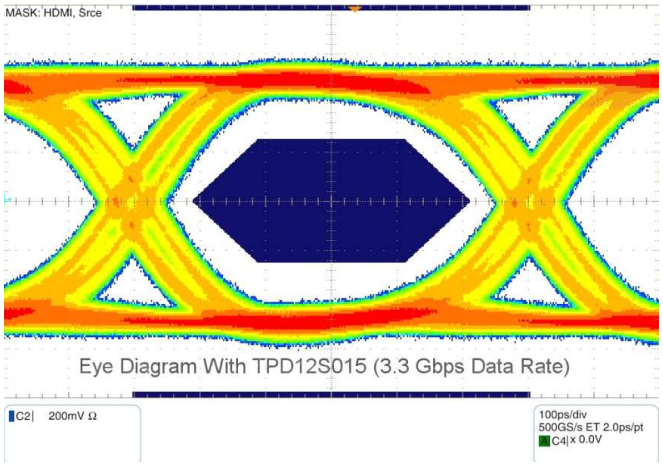



**Figure 23. Eye Diagram Performance on a Test Board for the D+ and D– Lines at 3.3 Gbps**

### 9.2.2 TPD12S015 Controlled by One GPIO from Controller

Some HDMI driver chips may have only one GPIO(CT_CP_HPD) available. In this situation, LE_OE pin is tied to HPD_A instead. Figure 24 shows how TPD12S015 is used in this situation.

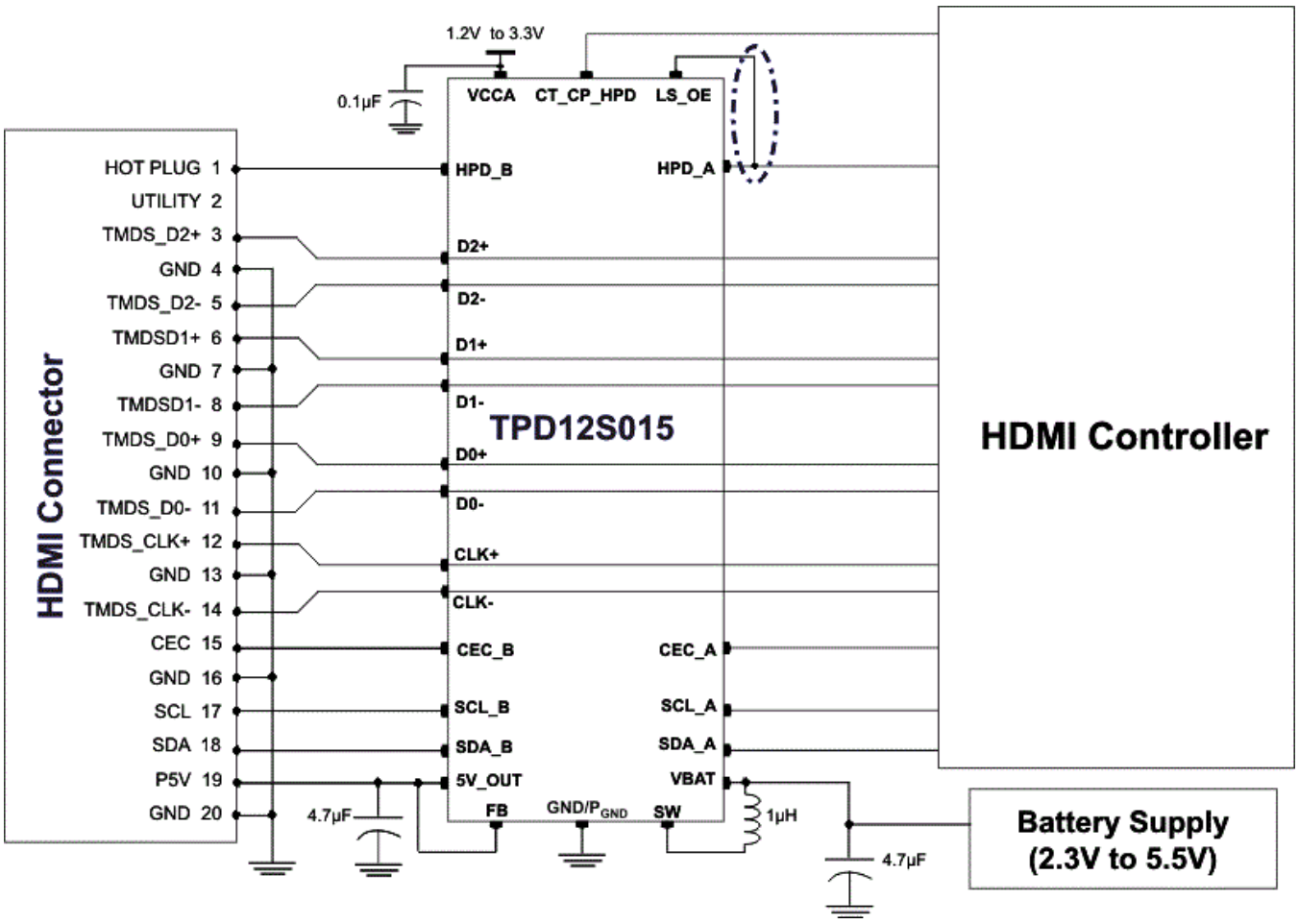





**Figure 24. TPD12S015 Controlled by One GPIO from Controller Schematic**

#### *9.2.2.1 Design Requirements*

See *Design Requirements*.

#### *9.2.2.2 Detailed Design Procedure*

See *Detailed Design Procedure*.

#### *9.2.2.3 Application Curves*

See *Application Curves*.

# 10 Power Supply Recommendations

See *Detailed Design Procedure* for detailed power supply recommendations.

# 11 Layout

## 11.1 Layout Guidelines

For proper operation, follow these layout and design guidelines:

- Place the TPD12S015 as close to the connector as possible. This allows it to remove the energy associated with ESD strike before it reaches the internal circuitry of the system board.
- Place power line capacitors and inductors close to the pins with wide traces to allow enough current to flow through with less trace parasitics.
- Ensure that there is enough metallization for the GND pad. A sufficient current path enables safe discharge of all the energy associated with the ESD strike.
- The critical routing paths for HDMI interface are the high-speed TMDS lines. Make sure to match the lengths of the differential pair. Maintain constant trace width after to avoid impedance mismatches in the transmission lines. Maximize differential pair-to-pair spacing when possible.

For more layout information, see *TPD12S015 PCB Layout Guidelines*.

## 11.2 Layout Example

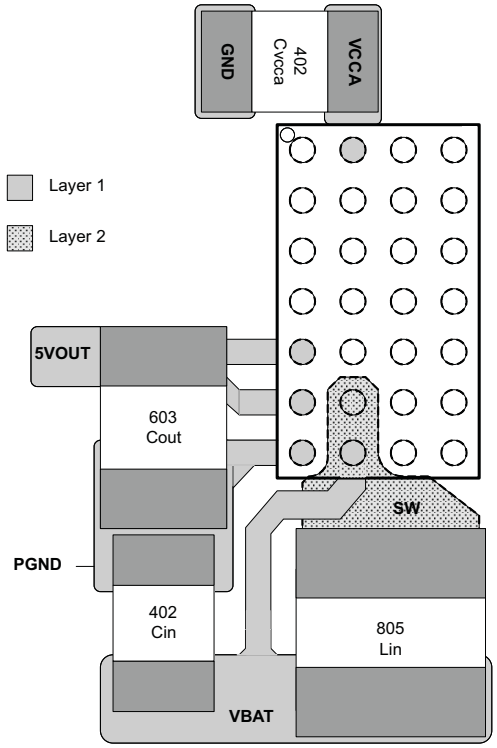



**Figure 25. Board Layout (DC-DC Components) (Top View)**

List of components:

- $L_{IN}$ = MURATA LQM21PN1R0MC0 or $L_{IN}$ = Toko MDT2010-CN1R0
- $C_{IN}$ = MURATA GRM188R60J225ME19 (2.2 µF, 6.3 V, 0603, X5R) or MURATA GRM188R60J475ME19 (4.7 µF, 6.3 V, 0603, X5R)
- $C_{OUT}$ = MURATA GRM188R60J475ME19 (4.7 µF, 6.3 V, 0603, X5R)
- $C_{VCCA}$ = MURATA GRM155R60J104MA01 (0.1 µF, 6.3 V, 0402, X5R)

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

*TPD12S015 PCB Layout Guidelines* (SLVA430)

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

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## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPD12S015YFFR | Active | Production | DSBGA (YFF) \| 28 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | PN015 |
| TPD12S015YFFR.B | Active | Production | DSBGA (YFF) \| 28 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | PN015 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

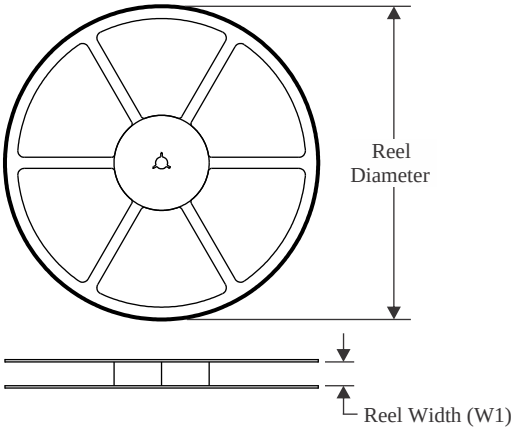
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

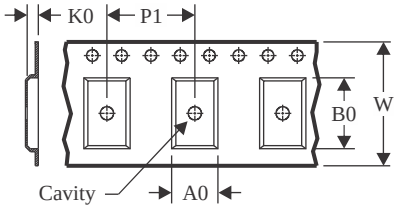
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

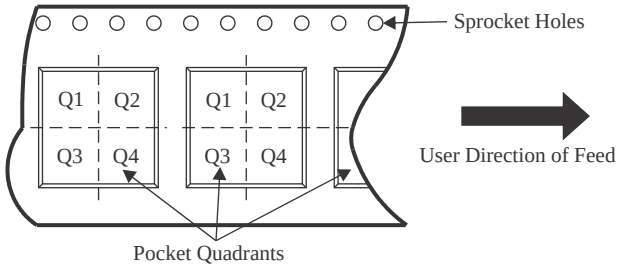



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

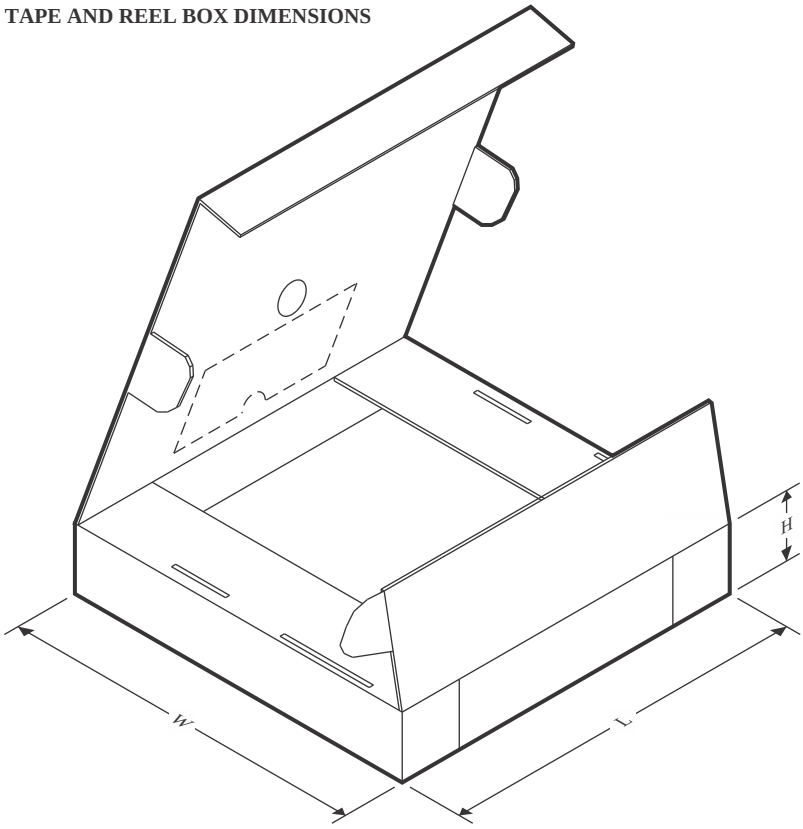
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD12S015YFFR | DSBGA | YFF | 28 | 3000 | 180.0 | 8.4 | 1.73 | 2.93 | 0.81 | 4.0 | 8.0 | Q1 |

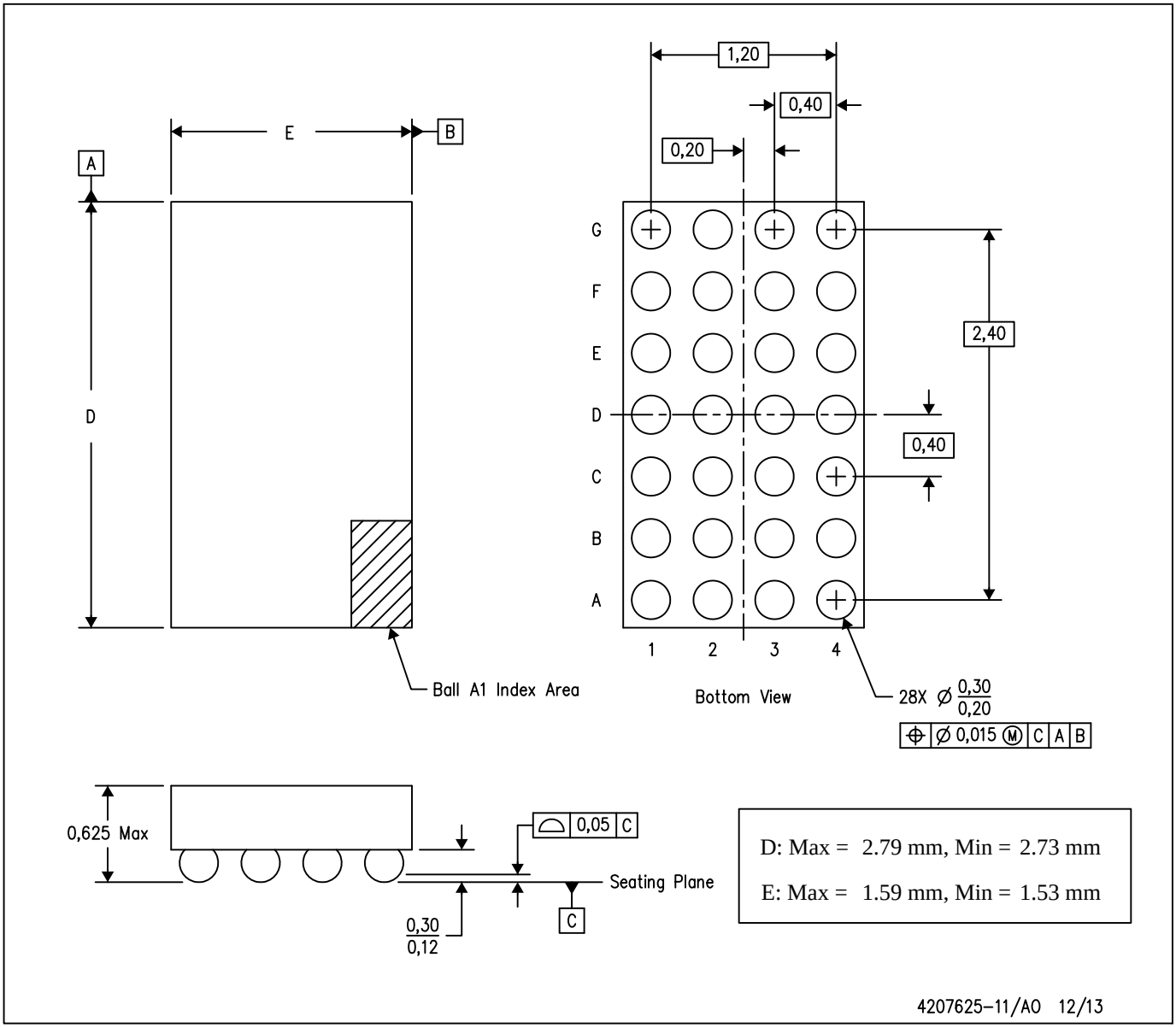
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPD12S015YFFR | DSBGA | YFF | 28 | 3000 | 182.0 | 182.0 | 20.0 |

YFF (R–XBGA–N28) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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