TMUX131 4V、低电容、3:1 2 通道多路复用器

1 特性

- 与高速 I3C 信号兼容
- V_{DD} 范围：2.5V 至 4.3V
- 高性能开关特性：
  - 带宽（–3dB）：6.5GHz
  - R_{ON}（典型值）：5.5Ω
  - C_{ON}（典型值）：1.3pF
- 电流消耗：28μA（典型值）
- 逻辑引脚上带有集成下拉电阻器
- 专有特性：
  - I_{OFF} 保护可防止在断电状态 (V_{DD} = 0V) 下产生漏电流
  - 1.8V 兼容控制输入 (SEL)
  - 所有 I/O 引脚上的过压容限 (OVT) 高达 5.5V，而且无需使用外部元件
- ESD 性能：
  - 2kV 人体放电模型（A114B，II 类）
  - 1kV 带电器件模型 (C101)
- 封装：
  - 12 引脚 VQFN 封装（1.8mm × 1.8mm，间距为 0.5mm）

2 应用

- I3C (SenseWire)
- I3C 和 I2C 外设开关
- 服务器
- 手持终端：智能电话
- 笔记本电脑
- 平板电脑：多媒体
- 电子销售终端
- 现场仪器
- 便携式监视器

3 说明

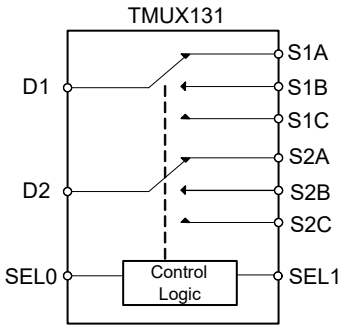
TMUX131 器件是一款高性能双向 2 通道 3:1 多路复用器，同时支持差分和单端信号。TMUX131 是一款具有断电保护功能的模拟无源多路复用器，当 VDD 引脚断电时，强制所有 I/O 引脚进入高阻抗模式。TMUX131 的选择引脚与 1.8V 和 3.3V 控制逻辑兼容，因而能够直接与低电压处理器的通用 I/O (GPIO) 相连。凭借这一特性以及器件的低导通电阻和低导通电容，TMUX131 成为支持切换各种模拟信号和数字通信协议标准（包括 I3C 等高速标准）的理想器件。

TMUX131 采用小型 12 引脚 VQFN 封装，尺寸仅为 1.8mm × 1.8mm，非常适合 PCB 面积有限的情况。

封装信息

器件型号	封装(1)	封装尺寸(2)
TMUX131	RMG（VQFN，12）	1.8mm × 1.8mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



开关图

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4 Revision History

DATE	REVISION	NOTES
August 2023	*	Initial Release

5 Pin Configuration and Functions

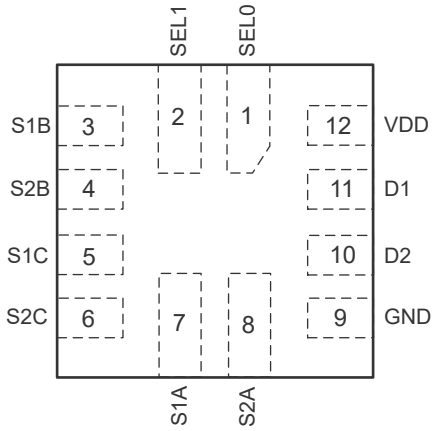


图 5-1. RMG Package, 12-Pin VQFN (Top View)

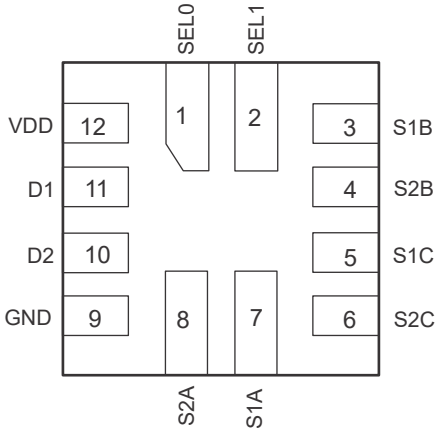


图 5-2. RMG Package, 12-Pin VQFN (Bottom View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SEL0	1	I	Switch logic control. Controls the switch connects as provided in 表 7-1
SEL1	2	I	Switch logic control. Controls the switch connects as provided in 表 7-1
S1B	3	I/O	Source pin 1B. Can be an input or output.
S2B	4	I/O	Source pin 2B. Can be an input or output.
S1C	5	I/O	Source pin 1C. Can be an input or output.
S2C	6	I/O	Source pin 2C. Can be an input or output.
S1A	7	I/O	Source pin 1A. Can be an input or output.
S2A	8	I/O	Source pin 2A. Can be an input or output.
GND	9	G	Ground
D2	10	I/O	Drain pin 2. Can be an input or output.
D1	11	I/O	Drain pin 1. Can be an input or output.
VDD	12	P	Power Supply

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}	Supply voltage(3)	– 0.3	5.5	V
$V_{S/D}$	Input/Output DC voltage(3)	– 0.3	5.5	V
I_K	Input/Output port diode current ($V_{S/D}$ < 0)	– 50		mA
V_I	Digital input voltage (SEL0, SEL1)	– 0.3	5.5	
I_{IK}	Digital logic input clamp current (V_I < 0)(3)	– 50		mA
$I_{I/O}$	Continuous switch DC output current		60	mA
T_{stg}	Storage temperature	– 65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2.5	4.3	V
$V_{S/D}$,	Analog voltage	0	3.6	V
V_{SEL}	Digital input voltage (SEL0, SEL1)	0	V_{DD}	V
$T_{RAMP\ (VDD)}$	Power supply ramp time requirement (VDD)	100	1000	µs/V
$I_{S/D,\ PEAK}$	Peak switch DC output current (1-ms duration pulse at <10% duty cycle)		150	mA
T_A	Operating free-air temperature	– 40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMUX131 RMG (VQFN) 12 PINS	UNIT
$R_{\theta\ JA}$	Junction-to-ambient thermal resistance	160.8	°C/W
$R_{\theta\ JC(top)}$	Junction-to-case (top) thermal resistance	95.5	°C/W
$R_{\theta\ JB}$	Junction-to-board thermal resistance	91.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = –40°C to 85°C, typical values are at V_{DD} = 3.3 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ON}	ON-state resistance	V_{DD} = 2.5 V, V_S = 1.5V, I_{ON} = –8 mA (see 图 7-1)		5.5	7	Ω
ΔR_{ON}	ON-state resistance match between channels	V_{DD} = 2.5 V, V_S = 1.5 V, I_{ON} = –8 mA		0.1		Ω
$R_{ON (FLAT)}$	ON-state resistance flatness	V_{DD} = 2.5 V, V_S = 1.5 V to 3.3 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{DD} = 4.3 V, Switch OFF, V_S = 1.5 V to 3.3 V, V_D= 0 V (see 图 7-2)	–2		2	µA
I_{OFF}	Power-off leakage current	V_{DD} = 0 V, Power off, V_S = 1.5 V to 3.3 V, V_D= NC	–10		10	µA
I_{ON}	ON leakage current	V_{DD} = 4.3 V, Switch ON, V_S = 1.5 V to 3.3 V, V_D= NC	–2		2	µA
DIGITAL CONTROL INPUTS (SEL)						
V_{IH}	Input logic high	V_{DD} = 2.5 V to 4.3 V	1.3			V
V_{IL}	Input logic low	V_{DD} = 2.5 V to 4.3 V			0.6	V
I_{IN}	Input leakage current	V_{DD} = 4.3 V, $V_{S/D}$ = 0 V to 3.6 V, V_{SEL} = 0 V to 4.3 V	–10		10	µA

6.6 Dynamic Characteristics

T_A = –40°C to 85°C, Typical values are at V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	R_L = 50 Ω, CL = 5 pF, V_{DD} = 2.5 V to 4.3 V, V_S = 0.4 V or 3.3 V		50		ps
t_{TRAN}	Switching time from control input	R_L = 50 Ω, CL = 5 pF, V_{DD} = 2.5 V to 4.3 V, V_S = 0.4 V or 3.3 V			400	ns
t_{ON}	Switch turnon time (from disabled to active mode)	R_L = 50 Ω, CL = 5 pF, V_{DD} = 2.5 V to 4.3 V, V_S = 0.4 V or 3.3 V			100	µs
t_{OFF}	Switch turnoff time (from active to disabled mode)	R_L = 50 Ω, CL = 5 pF, V_{DD} = 2.5 V to 4.3 V, V_S = 0.4 V or 3.3 V			100	µs
$C_{S(ON)}$ $C_{D(ON)}$	ON capacitance	V_{DD} = 3.3 V, V_S = 0 V or 3.3 V, f = 240 MHz, Switch ON		1.3		pF
$C_{S(OFF)}$	OFF capacitance	V_{DD} = 3.3 V, V_S = 0 V or 3.3 V, f = 240 MHz, Switch OFF		1		pF
C_I	Digital input capacitance	V_{DD} = 3.3 V, V_I = 0 V or 2 V		2.2		pF
O_{ISO}	Differential OFF isolation	V_S = –10 dBm, V_{DC_BIAS} = 2.4 V, RT = 50 Ω, f = 240 MHz (see 图 7-3), Switch OFF		–38		dB
X_{TALK}	Channel-to-Channel Crosstalk	V_S = –10 dBm, V_{DC_BIAS} = 0.2 V, RT = 50 Ω, f = 240 MHz (see 图 7-4), Switch ON		–38		dB
BW	–3-dB bandwidth	V_{DD} = 2.5 V to 4.3 V, R_L = 50 Ω (see 图 7-5), Switch ON		6.5		GHz
SUPPLY						
V_{DD}	Power supply voltage		2.5		4.3	V
I_{DD}	Positive supply current	V_{DD} = 4.3 V, V_{IN} = V_{DD} or GND, V_S = 0 V, Switch ON or OFF		28	40	µA

6.7 Typical Characteristics

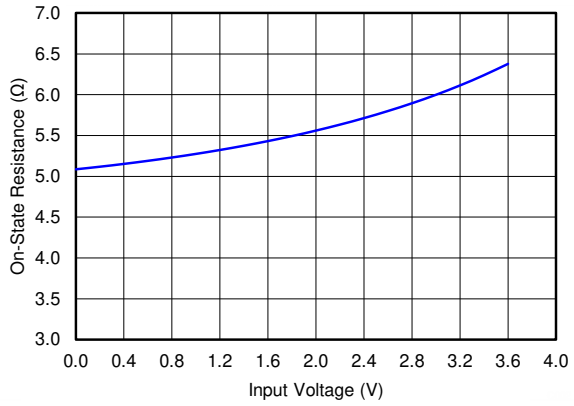


图 6-1. ON-Resistance vs V_S

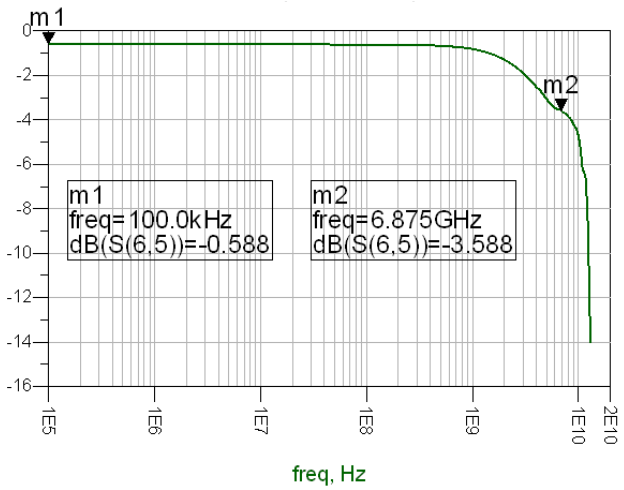


图 6-2. Typical Differential Bandwidth vs Frequency

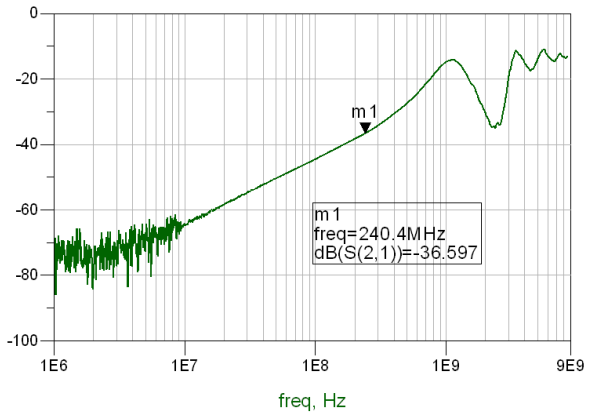


图 6-3. OFF Isolation vs Frequency

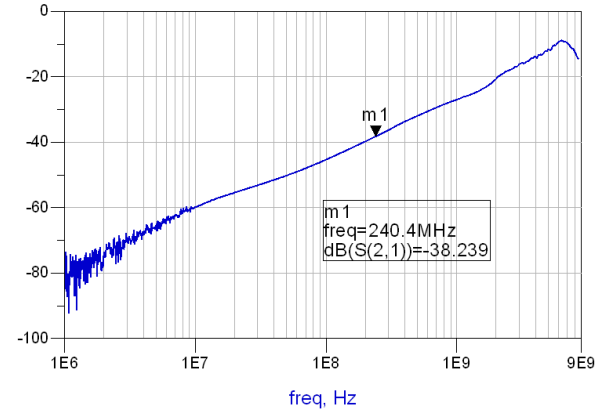


图 6-4. Cross Talk vs Frequency

Parameter Measurement Information

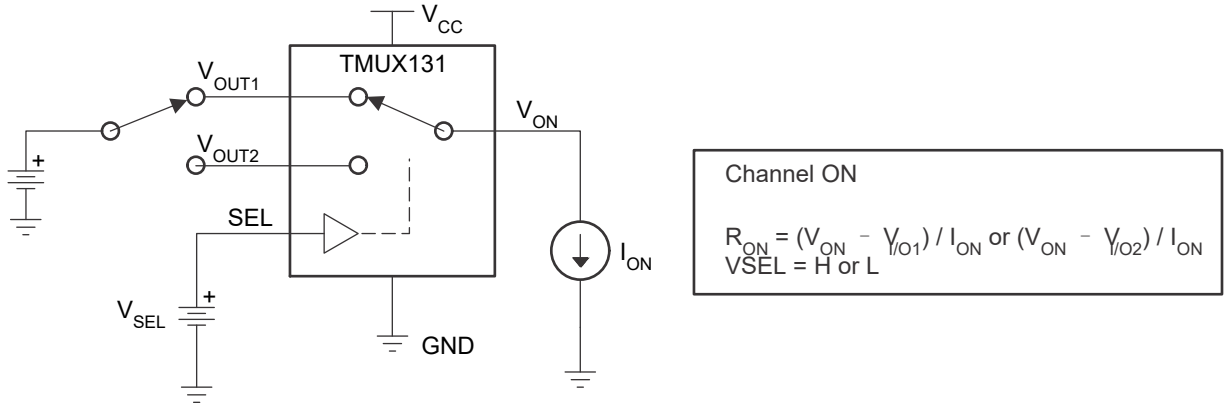


图 7-1. ON-State Resistance (R_{ON})

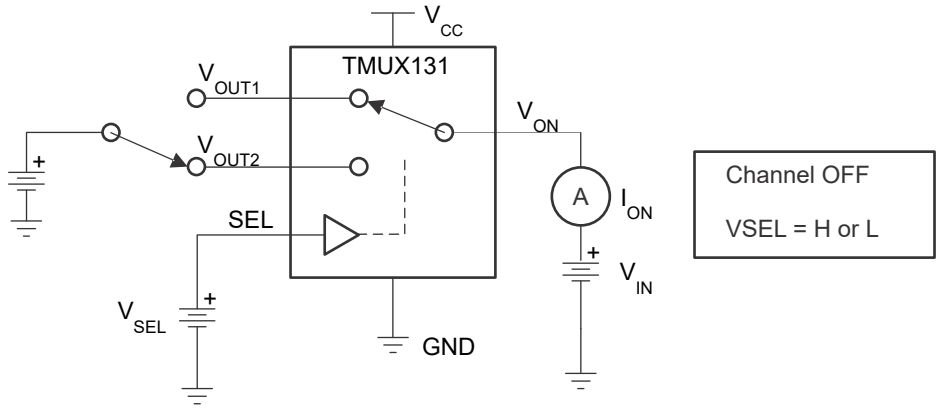


图 7-2. OFF Leakage Current (I_{OZ})

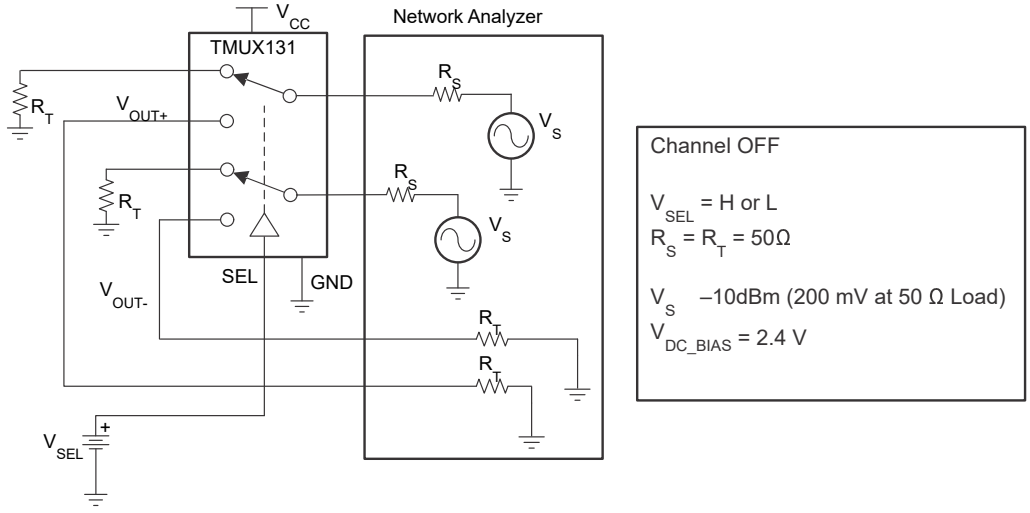


图 7-3. Differential Off-Isolation (O_{ISO})

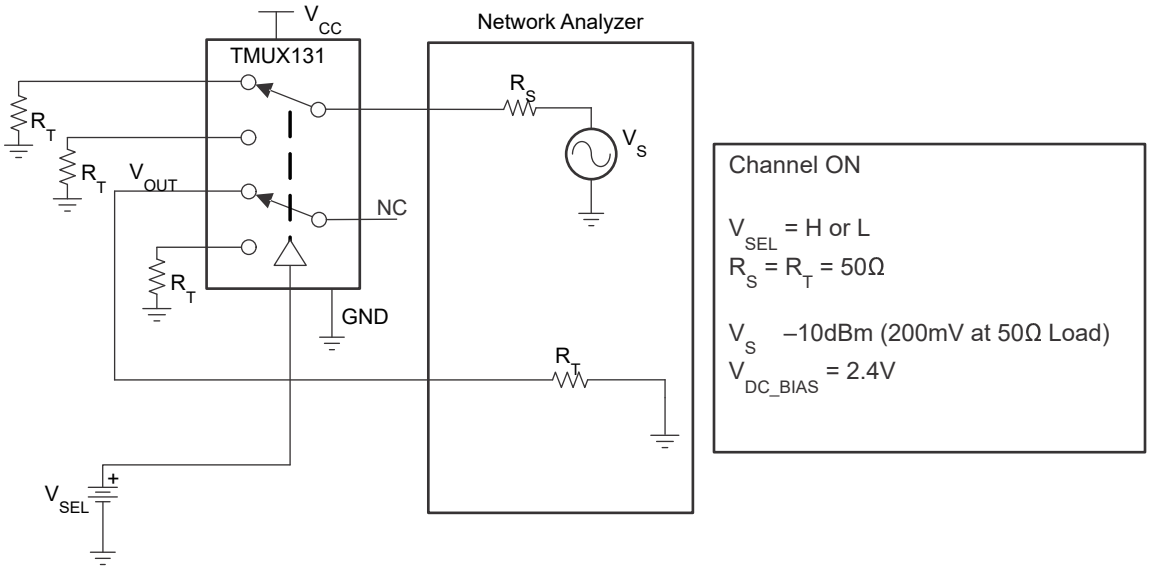


图 7-4. Crosstalk (Xtalk)

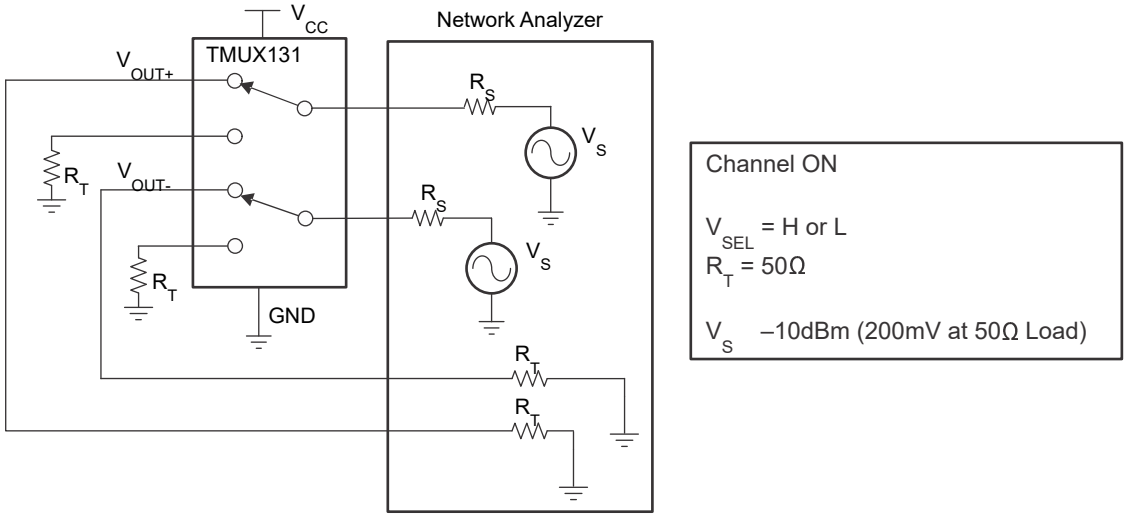


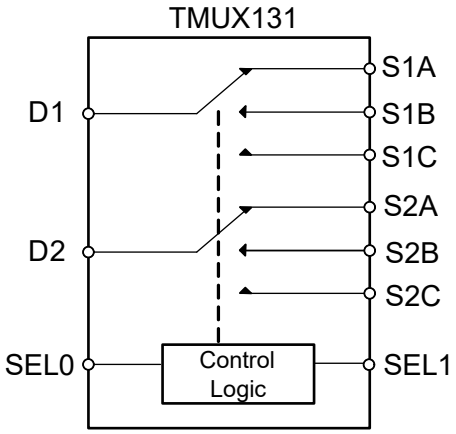
图 7-5. Differential Bandwidth (BW)

7 Detailed Description

7.1 Overview

The TMUX131 device is an analog passive 2 channel, 3:1 multiplexer that can work for any low-speed, high-speed, differential or single ended signals. Excellent low capacitance characteristics of the device allow signal switching with minimal attenuation and very little added jitter. The signals must be within the allowable voltage range of 0 to 3.6 V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 I_{OFF} Protection

I_{OFF} protection percents current leakage through the device when V_{DD} = 0 V This allows signals to be present on the source and drain pins before the device is powered up without damaging the device or system.

7.3.2 1.8-V Compatible Logic

The TMUX131 device supports 1.8-V logic irrespective to the supply voltage applied to the IC.

7.3.3 Overvoltage Tolerant (OVT)

The source and drain pins of the device can support signals up to 5.5 V without damaging the device. This protects the TMUX131 in case of an overvoltage fault event with no extra components needed.

7.3.4 Integrated Pull-Down Resistors

The TMUX131 has internal weak pull-down resistors (6 MΩ) to GND so that the logic pins are not left floating. This feature integrates up to two external components and reduces system size and cost.

7.4 Device Functional Modes

表 7-1 lists the functional modes of the TMUX131.

表 7-1. Function Table

SEL1	SEL0	SWITCH STATUS
Low	Low	D1/D2 connected to S1B/S2B
Low	High	D1/D2 connected to S1C/S2C
High	Low	D1/D2 connected to S1A/S2A
High	High	All switches in High-Z

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUX131 is a passive, bidirectional, 2-channel 1:3 switch, which makes it versatile for many high speed 1:3 switching applications. This device can be used for general protocol switching applications such as I^3C, I^2C, UART, LVDS, and other analog signal applications.

8.2 Typical Application

8.2.1 Signal Expansion (I^3C and I^2C)

There are many applications in which microprocessors or controllers have a limited number of I/Os. The TMUX131 solution can effectively expand the limited I/Os by switching between multiple buses to interface them to a single microprocessor or controller. A common application where the TMUX131 is used as a I^3C 1:3 multiplexer. In this application, the TMUX131 is used to route communicating between different peripherals from a single controller or driver within a server, as shown in 图 8-1. The high bandwidth of the TMUX131 will preserve signal integrity at even the fastest communication protocols that may be used in server applications, such as I^3C. Also, because I^3C is backwards compatible, any of the peripherals can also be I^2C, and the TMUX131 will still support it.

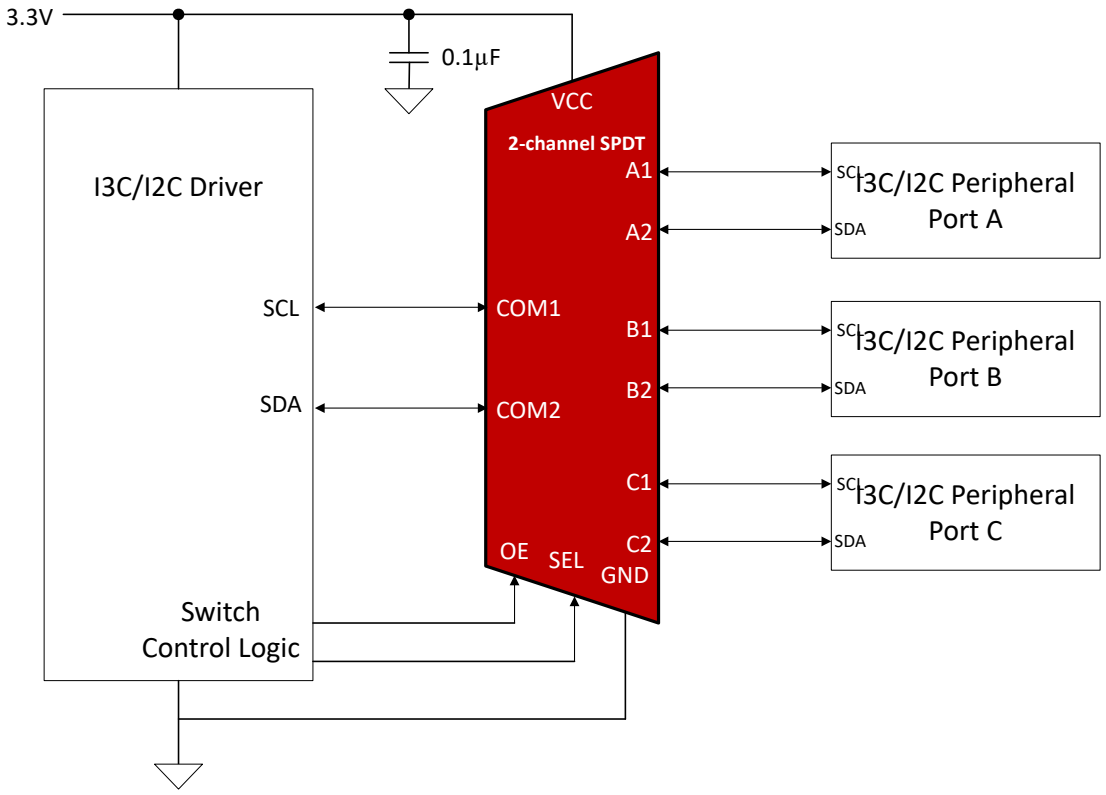


图 8-1. Typical TMUX131 Application

8.2.2 Design Requirements

The TMUX131 supports I^{3}C standard by maintaining signal integrity through the switch. 表 8-1 details how the TMUX131 specifications make this device optimal for switching I^{3}C signals.

表 8-1. TMUX131 I^{3}C Compatibility

	I^{3}C Requirements	TMUX131
Voltage	1.0 V, 1.2 V, 1.8 V, and 3.3 V	0 – 3.6 V
Frequency	Up to 12.5 MHz	6.5 GHz Bandwidth
Capacitance	50 pF maximum bus capacitance	< 2 pF On or Off Capacitance

8.2.3 Detailed Design Procedure

The TMUX131 can operate properly without any external components. However, TI recommends to connect unused signal I/O pins to ground through a 50-Ω resistor to prevent signal reflections back into the device.

8.2.4 Application Curves

图 8-2 shows TMUX131 bandwidth. This bandwidth can easily support the maximum data rate of the I^{3}C standard. A combination of low on-resistance, low capacitance, and low added jitter from the device allows it to be used for I^{3}C.

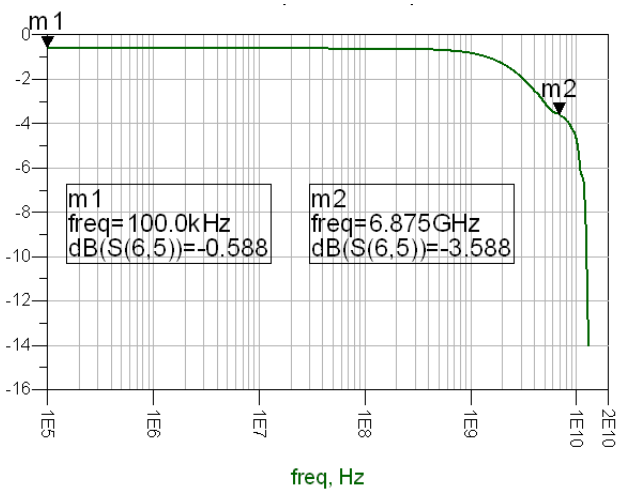


图 8-2. Typical Differential Bandwidth vs Frequency

8.3 Power Supply Recommendations

The TMUX131 does not require a power supply sequence. However, TI recommends to enable the device after VDD is stable and in specification. TI also recommends to place a bypass capacitor as close to the supply pin (VDD) as possible to help smooth out lower frequency noise and provide better load regulation across the frequency spectrum.

8.4 Layout

8.4.1 Layout Guidelines

Place supply bypass capacitors as close to VDD pin as possible and avoid placing the bypass capacitors near the high speed traces.

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’ s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. Doing this reduces reflections on the signal traces by minimizing impedance discontinuities. Avoid stubs on the high-speed signals because they cause signal reflections. Route all high-speed signal traces over continuous planes (VDD or GND) with no interruptions.

Due to high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in 图 8-3.

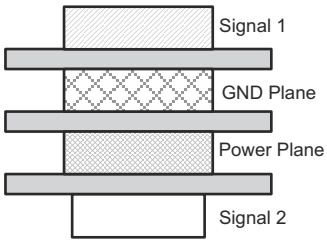


图 8-3. Four-Layer Board Stack-Up

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

For high speed layout guidelines, refer to *High-Speed Layout Guidelines* application note.

8.4.2 Layout Example

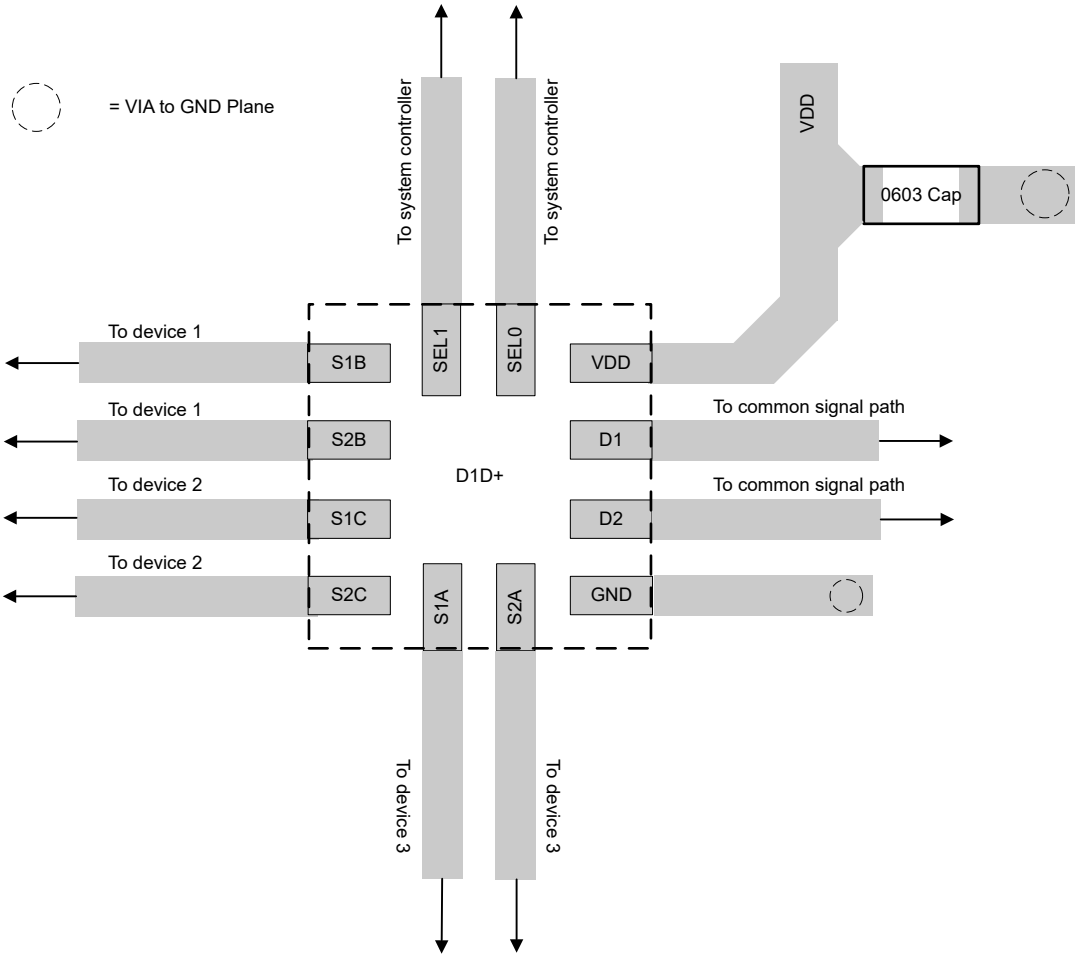


图 8-4. Layout Recommendation

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *High Speed Layout Guidelines*

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX131RMGR	Active	Production	WQFN (RMG) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OH
TMUX131RMGR.A	Active	Production	WQFN (RMG) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

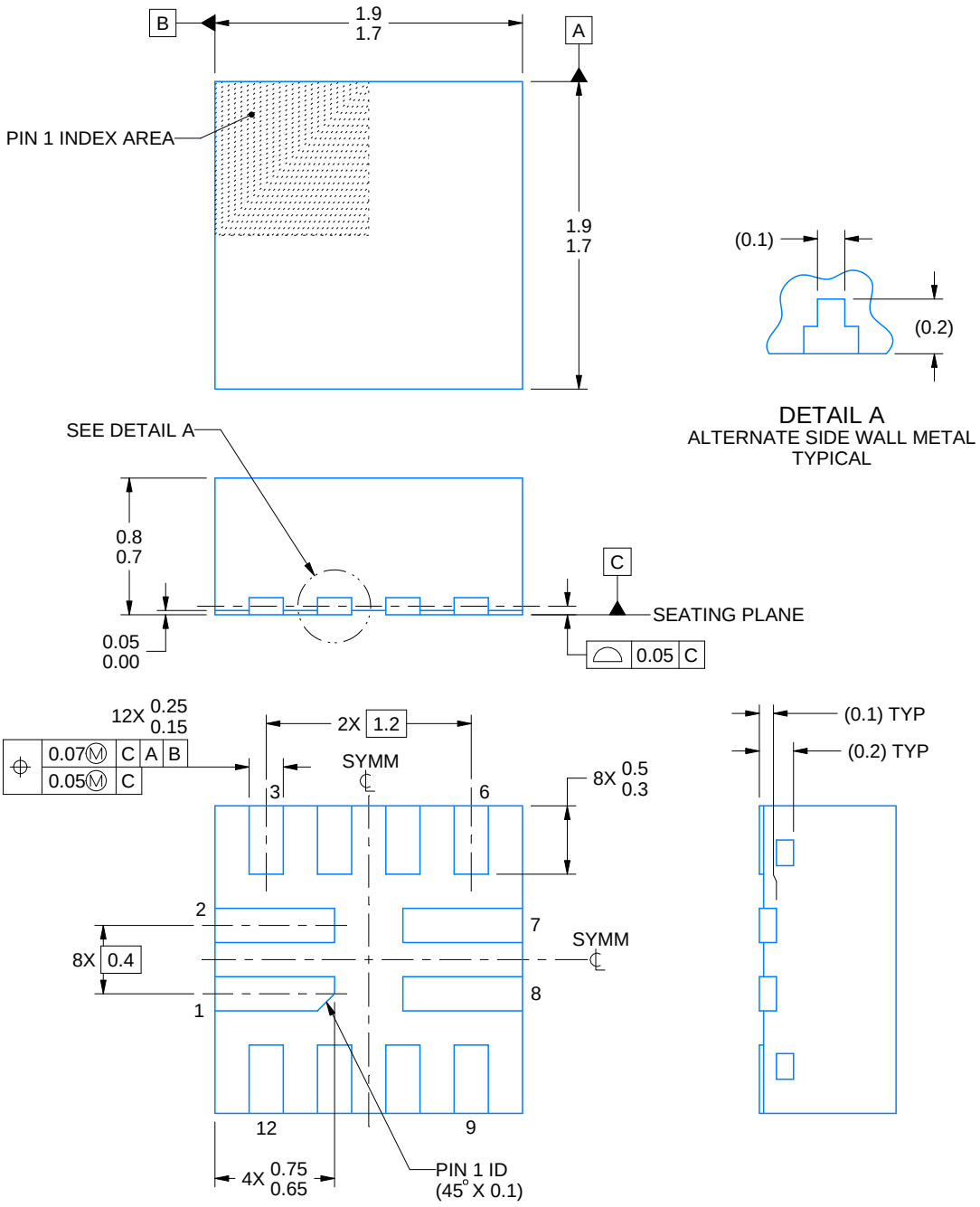
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

RMG0012A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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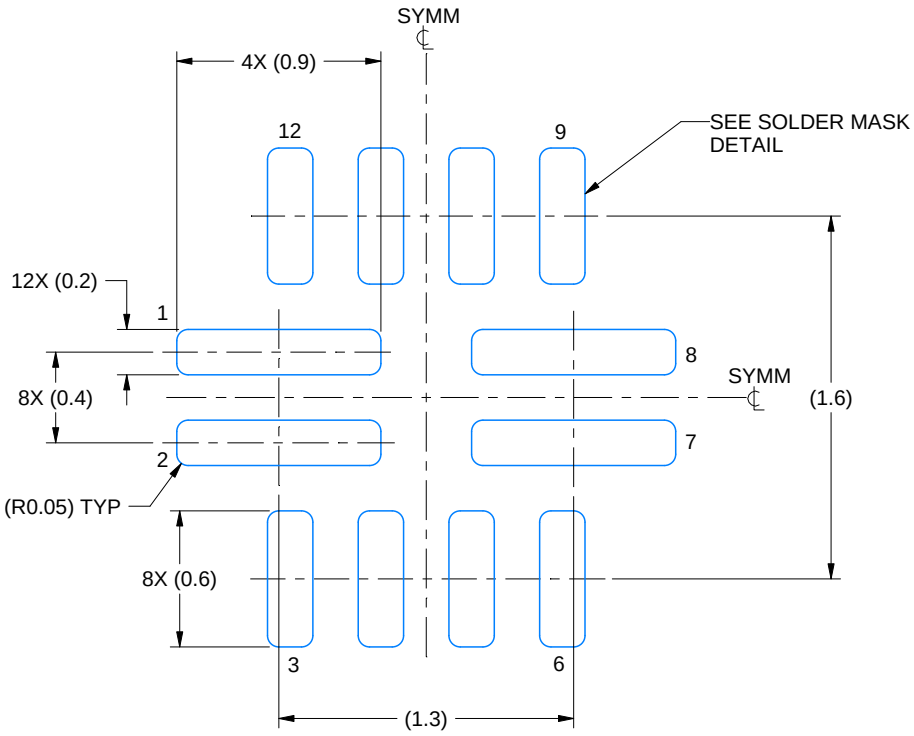
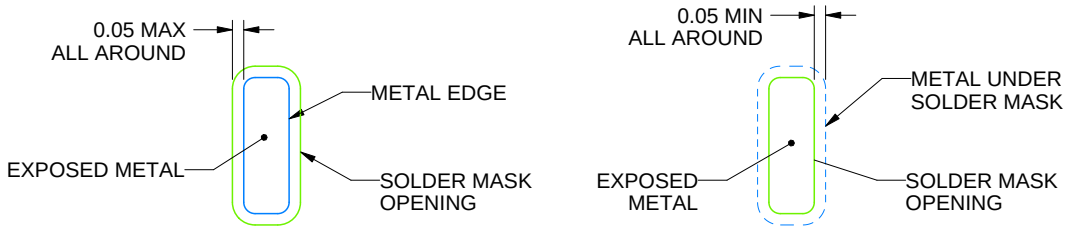
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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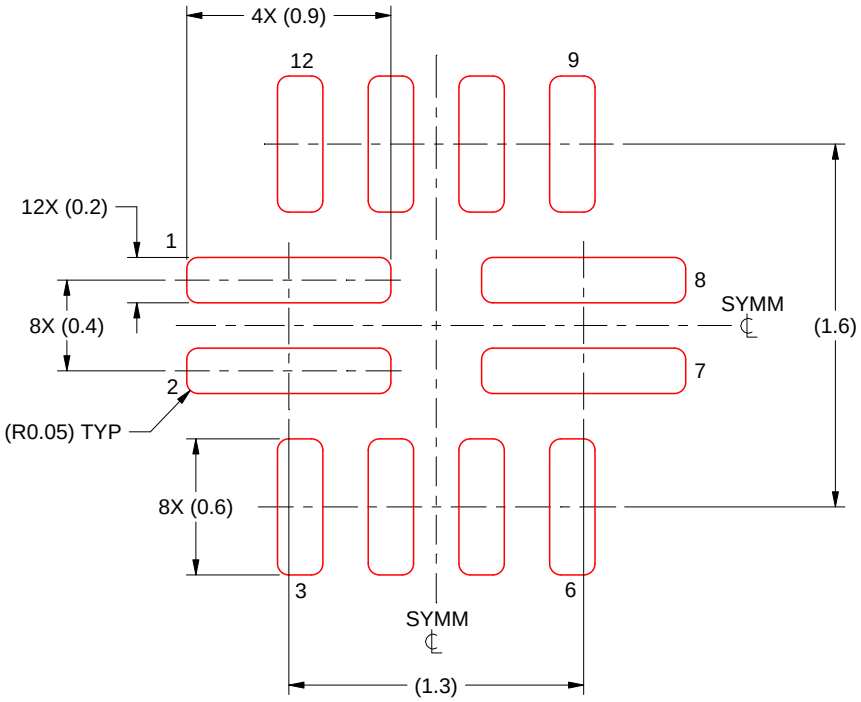
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月