TMS320C5517 定点数字信号处理器

1 器件概述

1.1 特性

- 内核：
  - 高性能、低功耗 TMS320C55x 定点数字信号处理器
    - 13.33ns 至 5ns 指令周期时间
    - 75MHz 至 200MHz 时钟速率
    - 每个周期执行一条或两条指令
    - 两个乘积累积单元（每秒高达 4.5 亿次乘积累积运算 [MMACS]）
    - 两个算术和逻辑单元 (ALU)
    - 三个内部数据或操作数读取总线和两个写入总线
    - 与 C55x 器件软件兼容
    - 提供工业温度器件
  - 320KB 零等待状态片上 RAM：
    - 64KB 双访问 RAM (DARAM)，8 块 4K x 16 位
    - 256KB 单访问 RAM (SARAM)，32 块 4K x 16 位
  - 128KB 零等待状态片上 ROM（4 块 16K x 16 位）
  - 紧密耦合快速傅里叶变换 (FFT) 硬件加速器
- 外设：
  - 一个带有 16 位复用地址或数据总线的通用主机端口接口 (UHPI)
  - 具有三芯片选择的主控和受控多通道串行端口接口 (McSPI)
  - 主控和受控多通道经缓冲串行端口接口 (McBSP)
  - 与下列器件有无缝接口连接的 16 位和 8 位外部存储器接口 (EMIF)
    - 8 位或 16 位 NAND 闪存，1 位或 4 位纠错码 (ECC)
    - 8 位和 16 位 NOR 闪存
    - 异步静态 RAM (SRAM)
    - SDRAM 或 mSDRAM（1.8，2.75 和 3.3 V）
  - 3.84375M x 16 位最大可寻址外部存储器空间（SDRAM 或 mSDRAM）
  - 通用异步收发器 (UART)
  - 带有集成型 2.0 高速物理层 (PHY) 的器件 USB 端口，支持：
    - USB 2.0 全速和高速器件
  - 直接存储器存取 (DMA) 控制器
    - 四个 DMA，各配有四条通道
  - 三个 32 位通用 (GP) 定时器
    - 一个可被选为安全装置或 GP
    - 计时选项，包括外部通用 I/O (GPIO) 时钟输入
  - 两个多媒体卡和安全数字（eMMC，MMC 和 SD）接口
  - 具有四芯片选择的串行端口接口 (SPI)
  - 主控和受控内部集成电路（I^2C 总线）
  - 三个用于数据传输的内部集成电路 (IC) 声音（I^2S 总线）模块
  - 10 位 4 输入逐次逼近 (SAR) ADC
  - IEEE-1149.1 (JTAG) 边界扫描兼容
  - 多达 26 个 GPIO 引脚（与其它功能多路复用）
- 电源：
  - 四个内核隔离的电源域：模拟，RTC，CPU 和外设，以及 USB
  - 四个 I/O 隔离电源域：RTC I/O，EMIF I/O，USB PHY 和 DV_{DDIO}
  - 1.05V 内核，1.8V、2.75V 或 3.3V I/O
  - 1.3V 内核，1.8V、2.75V 或 3.3V I/O
  - 1.4V 内核，1.8V、2.75V 或 3.3V I/O
- 时钟：
  - 具有晶振输入、独立时钟域和电源的实时时钟 (RTC)
  - 软件可编程锁相环 (PLL) 时钟发生器
- 引导加载程序：
  - 片上 ROM 引导加载程序
    - 每个外设均支持不加密启动
- 封装：
  - 196 端子无铅塑料 BGA（球栅阵列）封装（后缀 ZCH），0.65mm 间距

1.2 应用

- 数字双向无线电
- 低功耗分析应用（例如：语音识别、视觉传感和指纹识别）
- 语音应用（例如：录音机、免提套件和语音增强子系统）
- 音频器件（例如：回声抵消耳机和免提电话或者无线耳机和麦克风）
- 便携式医疗设备

1.3 说明

此器件是 TI C5000™ 定点数字信号处理器 (DSP) 产品系列的成员之一，专用于低运行和待机功耗应用。

此器件基于 TMS320C55x DSP 生成 CPU 处理器内核。 C55x DSP 架构通过增加的并行性和重视节能来实现高性能和低功耗。 CPU 支持一个内部总线结构，此结构包含一条程序总线，一条 32 位读取总线和两条 16 位数据读取总线，两条数据写入总线和专门用于外设和 DMA 操作的附加总线。 这些总线可实现在一个单周期内执行高达四次 16 位数据读取和两次 16 位数据写入的功能。 此器件还包含四个 DMA 控制器，每个控制器具有 4 条通道，可在无需 CPU 干预的情况下提供 16 条独立通道的数据传送。 每个 DMA 控制器在每周期可执行一个 32 位数据传输，此数据传输与 CPU 的运行并行并且不受 CPU 运行的影响。

C55x CPU 提供两个乘积累积 (MAC) 单元，每个单元在一个单周期内能够进行 17 位乘以 17 位乘法以及 32 位加法。 一个中央 40 位算术和逻辑单元 (ALU) 由一个附加 16 位 ALU 提供支持。 ALU 的使用受指令集控制，从而提供优化并行运行和功耗的能力。 C55x CPU 内的地址单元 (AU) 和数据单元 (DU) 对这些资源进行管理。

C55x CPU 支持一个可变字节宽度指令集以改进代码密度。 指令单元 (IU) 执行从内部或外部存储器中的 32 位程序取指令并且进行针对程序单元 (PU) 的指令排队。 PU 对指令进行解码，将任务指向地址单元和数据单元资源，并管理受到完全保护的管线。 跳转预测功能避免了条件指令执行时的管线冲刷。

GPIO 功能与 10 位 SAR ADC 一起为状态、中断以及用于键盘和媒体接口的位 I/O 提供足够的引脚。

通过以下器件为串行媒体提供支持：两个多媒体卡和安全数字（MMC 和 SD）外设、三个内部 IC 声音（I2S 总线）模块、一个具有四芯片选择的串行端口接口 (SPI)、一个具有三芯片选择主控和受控多通道经缓冲串行端口接口 (McSPI)、一个多通道串行端口 (McBSP)、一个 I^2C 多主控和受控接口以及一个通用异步收发器 (UART) 接口

该器件的外设集包括一个外部存储器接口 (EMIF)，此接口提供到异步存储器的无缝访问，例如 EPROM，NOR，NAND 和 SRAM，以及高速、高密度存储器，例如同步 DRAM (SDRAM) 和移动 SDRAM (mSDRAM)。

其它外设包括：一个可配置 16 位通用主机端口接口 (UHPI)、一条仅支持器件模式的高速通用串行总线 (USB2.0)、一个实时时钟 (RTC)、三个通用定时器（其中一个可配置为看门狗定时器）和一个模拟锁相环 (APLL) 时钟发生器。

器件还包含一个紧密耦合 FFT 硬件加速器 - 支持 8 至 1024 点（2 的次幂）实值和复值 FFT，三个集成低压降稳压器 (LDO) - 为器件的各部分供电（需要外部电源的 CV_{DDRTC} 除外）：ANA_LDO 为 SAR 和电源管理电路 (V_{DDA_ANA}) 提供 1.3V 电压，DSP_LDO 为 DSP 内核 (CV_{DD})（一旦检测到工作频率范围，便可由软件实时进行选择）提供 1.3V 或 1.05V 电压，USB_LDO 为 USB 内核数字电路 (USB_V_{DD1P3}) 和 PHY 电路 (USB_V_{DDA1P3}) 提供 1.3V 电压。

此器件由业界备受赞誉的 eXpressDSP™、 Code Composer Studio™ 集成开发环境 (IDE)、DSP/BIOS™、德州仪器 (TI) 的算法标准和一个大型第三方网络提供支持。 Code Composer Studio IDE 提供的代码生成工具包括一个 C 语言编译器和连接器、 RTDX™、XDS100、 XDS510™、 XDS560™ 仿真器件驱动程序和评估模块。 此器件也受 C55x DSP 库以及芯片支持库的支持，此库特有超过 50 个基础软件内核（FIR 滤波器、IIR 滤波器、FFT 和多种数学函数）。

器件信息

部件号	封装	封装尺寸
TMS320C5517AZCH20	NFBGA (196)	10.0mm x 10.0mm
TMS320C5517AZCHA20	NFBGA (196)	10.0mm x 10.0mm

1.4 功能方框图

图 1-1可展示器件的功能框图

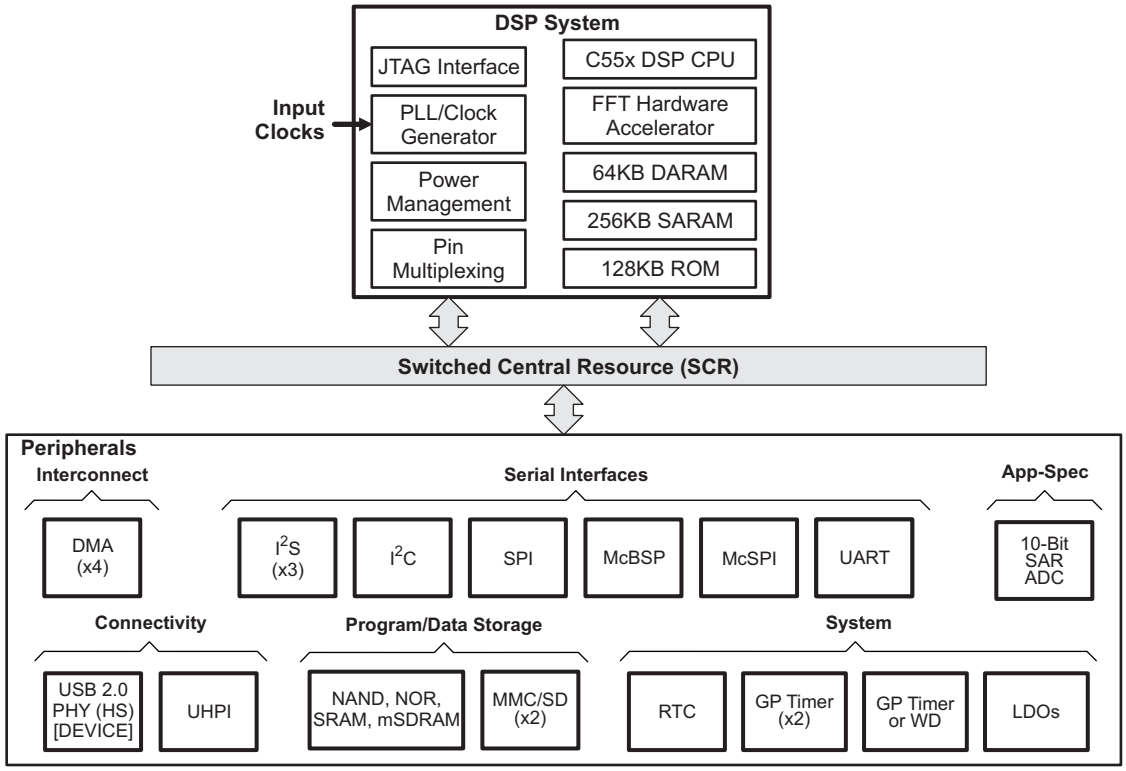


图 **1-1.** 功能方框图

内容

2 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

本数据手册修订历史记录强调了对之前版本的器件专用数据手册所做的技术更改。

参见	新增内容、修改内容和删除内容
全局	删除了 225MHz 器件信息。

3 Device Comparison

Table 3-1 provides characteristics of the C5517 processor.

The table shows significant features of the devices, including the capacity of on-chip RAM, the peripherals, the CPU frequency, and the package type with pin count. For more detailed information on the actual device part number and maximum device operating frequency, see Section 7.1.2, *Device Nomenclature*.

Table 3-1. Characteristics of the Processor

HARDWARE FEATURES			C5517
Peripherals Not all peripheral pins are available at the same time (for more detail, see Section 5).	External Memory Interface (EMIF)		Asynchronous (8- and 16-bit bus width) SRAM, Flash (NOR, NAND), SDRAM and Mobile SDRAM (16-bit bus width)(1)
	DMA		Four DMA controllers each with four channels, for a total of 16 channels
	Timers		2 32-Bit General-Purpose (GP) Timers 1 Additional Timer Configurable as a 32-Bit GP Timer or a Watchdog Each timer is capable of selecting its clock source among the choices of: • External from a GPIO pin • System PLL • 12.00 MHz USB oscillator
	UART		1 (with RTS and CTS flow control)
	SPI		1 with 4 chip selects (Master only)
	McSPI		1 (Master and Slave synchronous serial bus) with 3 chip selects
	UHPI		1 (A configurable 16-bit multiplexed host port interface)
	I^2C		1 (Master and Slave)
	I^2S		3 (Two Channel, Full Duplex Communication)
	USB 2.0		High- and Full-Speed Device (device mode only, host mode not supported)
	MMC and SD		2 MMC and SD, 256 byte read and write buffer, max 50-MHz clock for SD cards, and signaling for DMA transfers
	McBSP		1 (with transmit and receive)
	ADC (Successive Approximation [SAR])		1 (10-bit, 4-input, 16-µs conversion time)
	Real-Time Clock (RTC)		1 (Crystal Input, Separate Clock Domain and Power Supply)
	FFT Hardware Accelerator		1 (Supports 8 to 1024-point 16-bit real and complex FFT)
	General-Purpose Input/Output Port (GPIO)		Up to 26 pins (with 1 Additional General-Purpose Output (XF) and 4 General-Purpose Outputs for Use With SAR)
On-Chip Memory	Size and Organization		• 64KB On-Chip Dual-Access RAM (DARAM) • 256KB On-Chip Single-Access RAM (SARAM) • 128KB On-Chip Single-Access ROM (SAROM)
JTAG BSDL_ID	JTAGID Register (Value is: 0x0B95 602F)		see Figure 6-2
CPU Frequency	MHz	1.05-V Core	75 MHz
		1.3-V Core	175 MHz
		1.4-V Core	200 MHz
Cycle Time	ns	1.05-V Core	13.$\overline{3}$ ns
		1.3-V Core	5.71 ns

(1) For more information on SDRAM devices support, see Section 5.7.6, *External Memory Interface (EMIF)*.

Table 3-1. Characteristics of the Processor (continued)

HARDWARE FEATURES			C5517
		1.4-V Core	5 ns
Voltage	Core (V)		1.05 V (75 MHz)
			1.3 V (175 MHz)
			1.4 V (200 MHz)
	I/O (V)		1.8 V, 2.75 V, 3.3 V
LDOs	DSP_LDO		1.3 V or 1.05 V, 250 mA max current for the digital core (to be used only to supply CV_{DD}). Cannot be used to drive CV_{DD} at the 1.4 V (>200 MHz) operating range.
	ANA_LDO		1.3 V, 4 mA max current for SAR and power management circuits (to be used only to supply V_{DDA_ANA})
	USB_LDO		1.3 V, 25 mA max current for USB core digital and PHY circuits (to be used only to supply USB_V_{DD1P3} and USB_V_{DDA1P3})
Temperature	Commercial Temperature (default)		TMS320C5517AZCH20
	Industrial Temperature		TMS320C5517AZCHA20
PLL	Phase Lock Loop		1 (Software Programmable PLL)
BGA Package	10 x 10 mm		196-Terminal BGA (ZCH), 0.65-mm Pitch
Product Status(2)	Product Preview (PP), Advance Information (AI), or Production Data (PD)		PD

(2) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the bottom view of the package pin assignments.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
P	**EM_DQM1**/ UHPI_HBE1	DV_{DDEMIF}	DV_{DDIO}	**SPI_CS0**/ UHPI_HCNTL0	**SPI_CS2**/ UHPI_HR_NW	**SPI_RX**/ UHPI_HD[0]	**GP[12]**/ UHPI_HD[2]	DV_{DDIO}	**GP[15]**/ UHPI_HD[5]	**GP[17]**/ UHPI_HD[7]	**I2S2_FS**/ UHPI_HD[9]/ GP[19]/ SPI_CS0	**I2S2_DX**/ UHPI_HD[11]/ GP[27]/ SPI_TX	**UART_CTS**/ UHPI_HD[13]/ GP[29]/ I2S3_FS	**UART_TXD**/ UHPI_HD[15]/ GP[31]/ I2S3_DX
N	**GP[21]**/ EM_A[15]	**EM_SDCKE**/ UHPI_HHWIL	**SPI_CLK**/ UHPI_HINT	**SPI_CS1**/ UHPI_HCNTL1	**SPI_CS3**/ UHPI_HRDY	**SPI_TX**/ UHPI_HD[1]	**GP[13]**/ UHPI_HD[3]	**GP[14]**/ UHPI_HD[4]	**GP[16]**/ UHPI_HD[6]	**I2S2_CLK**/ UHPI_HD[8]/ GP[18]/ SPI_CLK	**I2S2_RX**/ UHPI_HD[10]/ GP[20]/ SPI_RX	**UART_RTS**/ UHPI_HD[12]/ GP[28]/ I2S3_CLK	**UART_RXD**/ UHPI_HD[14]/ GP[30]/ I2S3_RX	DV_{DDIO}
M	EM_A[14]	EM_D[5]	EM_SDCLK	$\overline{EM\_CS3}$	EMU1	TCK	TDO	XF	$\overline{TRST}$	**MMC0_D1**/ I2S0_RX/ GP[3]/ McBSP_DR	**MMC0_CMD**/ I2S0_FS/ GP[1]/ McBSP_FSX	**MMC1_D1**/ McSPI_SOMI/ GP[9]	**MMC1_CLK**/ McSPI_CLK/ GP[6]	**MMC1_D0**/ McSPI_SIMO/ GP[8]
L	EM_A[13]	EM_A[10]	EM_D[12]	EM_D[4]	CV_{DD}	EMU0	TDI	TMS	**MMC0_D0**/ I2S0_DX/ GP[2]/ McBSP_DX	**MMC0_CLK**/ I2S0_CLK/ GP[0]/ McBSP_CLKX	**MMC0_D3**/ GP[5]/ McBSP_ CLKR_CLKS	**MMC0_D2**/ GP[4]/ McBSP_FSR	**MMC1_D3**/ McSPI_CS2/ GP[11]	**MMC1_CMD**/ McSPI_CS0/ GP[7]
K	EM_A[12]/ (CLE)	EM_A[11]/ (ALE)	EM_D[14]	EM_D[13]	EM_D[6]	EM_WAIT3	DV_{DDIO}	V_{SS}	V_{SS}	CV_{DD}	V_{SS}	DV_{DDIO}	V_{SS}	**MMC1_D2**/ McSPI_CS1/ GP[10]
J	EM_A[8]	EM_A[9]	**GP[26]**/ EM_A[20]	EM_D[15]	DV_{DDEMIF}	CV_{DD}	V_{SS}	V_{SS}	V_{SS}	RSV1	RSV2	USB_VBUS	USB_V_{DD1P3}	USB_DM
H	$\overline{EM\_WE}$	EM_A[7]	EM_D[7]	EM_WAIT5	DV_{DDEMIF}	V_{SS}	DV_{DDEMIF}	CV_{DD}	USB_ V_{SSA1P3}	USB_ V_{DDA1P3}	USB_ V_{SSA3P3}	USB_ V_{DDA3P3}	USB_V_{SS1P3}	USB_DP
G	EM_WAIT4	**GP[24]**/ EM_A[18]	EM_D[0]	**GP[25]**/ EM_A[19]	DV_{DDEMIF}	V_{SS}	V_{SS}	USB_V_{DDPLL}	USB_R1	USB_V_{SSREF}	USB_V_{SSPLL}	USB_V_{DDOSC}	USB_MXI	USB_MXO
F	EM_A[6]	**GP[23]**/ EM_A[17]	EM_D[2]	EM_D[9]	DV_{DDEMIF}	CV_{DD}	DV_{DDIO}	DV_{DDRTC}	V_{SS}	V_{SS}	USB_V_{SSOSC}	USB_LDOO	LDOI	LDOI
E	EM_A[2]	**GP[22]**/ EM_A[16]	EM_D[8]	$\overline{EM\_OE}$	EM_D[1]	DV_{DDEMIF}	$\overline{INT1}$	WAKEUP	V_{SS}	DSP_LDOO	V_{SS}	V_{SS}	V_{SS}	V_{SS}
D	EM_A[5]	EM_A[3]	EM_D[10]	EM_D[3]	EM_WAIT2	$\overline{RESET}$	V_{SS}	RTC_ CLKOUT	V_{SSA_PLL}	GPAIN0	V_{SS}	$\overline{DSP\_LDO\_EN}$	RSV16	RSV3
C	EM_A[4]	EM_A[1]	$\overline{EM\_CS4}$	EM_D[11]	$\overline{EM\_CS2}$	$\overline{INT0}$	CLK_SEL	CV_{DDRTC}	V_{SSRTC}	V_{DDA_PLL}	GPAIN3	RSV0	RSV5	RSV4
B	EM_BA[1]	EM_A[0]	$\overline{EM\_CS0}$/ $\overline{UHPI\_HDS1}$	$\overline{EM\_SDCAS}$/ $\overline{UHPI\_HCS}$	**EM_DQM0**/ UHPI_HBE0	EM_R/$\overline{W}$	SCL	SDA	RTC_XI	V_{SSA_ANA}	GPAIN2	LDOI	BG_CAP	V_{SSA_ANA}
A	EM_BA[0]	DV_{DDEMIF}	$\overline{EM\_CS5}$	$\overline{EM\_CS1}$/ $\overline{UHPI\_HDS2}$	DV_{DDEMIF}	$\overline{EM\_SDRAS}$/ $\overline{UHPI\_HAS}$	CLKOUT	CLKIN	RTC_XO	V_{DDA_ANA}	GPAIN1	ANA_LDOO	V_{SS}	V_{SS}

Pins with multiple names default to the first, bolded name when reset (for example, **GP[21]**/EM_A[15] defaults to GP[21] when reset).

Figure 4-1. Pin Diagram

4.2 Signal Descriptions

The signal descriptions tables (Table 4-1 through Table 4-19) identify the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more information on pin multiplexing, see Section 4.3, *Pin Multiplexing*.

For proper device operation, external pullup and pulldown resistors may be required on some pins. Section 5.7.20.1.1, *Pullup and Pulldown Resistors* discusses situations where external pullup and pulldown resistors are required.

4.2.1 Oscillator and PLL

Table 4-1. Oscillator and PLL Signal Descriptions

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
CLKOUT	A7	O/Z	IPD DV_{DDIO} BH	DSP clock output signal. For debug purposes, the CLKOUT pin can be used to tap different clocks within the system clock generator. The CLKOUT_SRC bits in the CLKOUT Configuration Register (CLKOUTCR) can be used to specify the CLKOUT pin source. Additionally, the slew rate of the CLKOUT pin can be controlled by the Output Slew Rate Control Register (OSRCR) [0x1C16]. The output driver of the CLKOUT pin is enabled and disabled through the CLKOFF bit in the CPU ST3_55 register. When disabled, the CLKOUT pin's output driver is placed in high-impedance (Hi-Z) and the IPD is automatically enabled. When enabled, the output driver of the pin is enabled and the IPD is automatically disabled. At reset the CLKOUT pin is enabled until the beginning of the boot sequence, at which point the on-chip Bootloader sets CLKOFF = 1 and the CLKOUT pin is disabled (Hi-Z). For more information on the ST3_55 register, see the *C55x 3.0 CPU* Reference Guide [literature number: SWPU073]. The IPD resistor on this pin is enabled when CLKOUT is in Hi-Z state.
CLKIN	A8	I	IPD DV_{DDIO} BH	Input clock. This signal is used to input an external clock when the 12-MHz on-chip USB oscillator is not used as the system clock (CLK_SEL = 1). To appropriately set the various serial port frequencies during bootloading, the bootloader ROM code assumes CLKIN is running at the frequency indicated by the setting (see Section 6.4, *Boot Modes*, for the supported frequencies and details about the bootmode). The CLK_SEL pin selects the source for the system clock generator, with the options being the USB oscillator (CLK_SEL=0) or CLKIN (CLK_SEL=1) pins. When the CLK_SEL pin is low, this pin should be tied to ground (V_{SS}). When CLK_SEL is high, this pin should be driven by an external clock source. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD disabled at reset.
CLK_SEL	C7	I	– DV_{DDIO} BH	Clock input select. This pin selects between the on-chip USB oscillator or CLKIN. 0 = The on-chip USB oscillator is enabled at reset and drives the system clock generator. The CLKIN is ignored. Also, the USB LDOO is enabled at reset (USB_LDO_EN=1). The on-chip USB oscillator and USB_LDO cannot be disabled if CLK_SEL=0. 1 = CLKIN drives the system clock generator. The on-chip USB oscillator and USB LDO are disabled at reset (USB_LDO_EN=1), but they can be enabled by software. This pin is ***not*** allowed to change during device operation; it ***must*** be tied high or low at the board.
V_{DDA_PLL}	C10	PWR	see Section 5.2, ROC	1.3-V Analog PLL power supply for the system clock generator. This supply pin must not be connected to ANA_LDOO pin. The supply pin must be externally powered.
V_{SSA_PLL}	D9	GND	see Section 5.2, ROC	Analog PLL ground for the system clock generator.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

4.2.2 Real-Time Clock (RTC)

Table 4-2. RTC Signal Descriptions

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
RTC_XO	A9	O/Z	– CV_{DDRTC} DV_{DDRTC}	Real-time clock oscillator output. This pin operates at the RTC core voltage, CV_{DDRTC}, and supports a 32.768-kHz crystal. If the RTC oscillator is not used, it can be disabled by connecting RTC_XI to CV_{DDRTC} and RTC_XO to ground (V_{SS}). A voltage `must` still be applied to CV_{DDRTC} by an external power source (see Section 5.2, *Recommended Operating Conditions*). None of the on-chip LDOs can power CV_{DDRTC}. **Note:** When RTC oscillator is disabled, the RTC registers (I/O address range 1900h – 197Fh) are not accessible.
RTC_XI	B9	I	– CV_{DDRTC} DV_{DDRTC}	Real-time clock oscillator input. If the RTC oscillator is not used, it can be disabled by connecting RTC_XI to CV_{DDRTC} and RTC_XO to ground (V_{SS}). A voltage `must` still be applied to CV_{DDRTC} by an external power source (see Section 5.2, *Recommended Operating Conditions*). None of the on-chip LDOs can power CV_{DDRTC}. **Note:** When RTC oscillator is disabled, the RTC registers (I/O address range 1900h – 197Fh) are not accessible.
RTC_CLKOUT	D8	O/Z	– DV_{DDRTC}	Real-time clock output pin. This pin operates at DV_{DDRTC} voltage. The RTC_CLKOUT pin is enabled and disabled through the RTCCLKOUTEN bit in the RTC Power Management Register (RTCPMGT). At reset, the RTC_CLKOUT pin is disabled (high-impedance [Hi-Z]).
WAKEUP	E8	I/O/Z	– DV_{DDRTC}	The active-high pin is used to WAKEUP the core from idle condition. This pin defaults to an input at CV_{DDRTC} powerup, but can also be configured as an active-low open-drain output signal to wakeup an external device from an RTC alarm.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

4.2.3 RESET, Interrupts, and JTAG

Table 4-3. RESET, Interrupts, and JTAG Signal Descriptions

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
RESET				
XF	M8	O/Z	IPU DV_{DDIO} BH	External Flag Output. XF is used for signaling other processors in multiprocessor configurations or XF can be used as a fast general-purpose output pin. XF is set high by the BSET XF instruction and XF is set low by the BCLR XF instruction or by writing to bit 13 of the ST1_55 register. For more information on the ST1_55 register, see the *C55x 3.0 CPU* Reference Guide [literature number: SWPU073]. For the XF pin's states after reset, see Figure 5-9, *BootMode Latching*. XF pin can manually configured as Hi-Z state only in boundary-scan mode. When this pin is in Hi-Z state, the IPU is enabled. The IPU on this pin is disabled at reset.
$\overline{\text{RESET}}$	D6	I	IPU DV_{DDIO} BH	Device reset. $\overline{\text{RESET}}$ causes the DSP to terminate execution and loads the program counter with the contents of the reset vector. When $\overline{\text{RESET}}$ is brought to a high level, the reset vector in ROM at FFFF00h forces the program execution to branch to the location of the on-chip ROM bootloader. $\overline{\text{RESET}}$ affects the various registers and status bits. The IPU resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h). The IPU is disabled at reset.
JTAG				
For more detailed information on emulation header design guidelines, see the *XDS560 Emulator* Technical Reference [literature number: SPRU589].				
TMS	L8	I	IPU DV_{DDIO} BH	IEEE standard 1149.1 test mode select. This serial control input is clocked into the TAP controller on the rising edge of TCK. If the emulation header is located greater than 6 inches from the device, TMS must be buffered. In this case, the input buffer for TMS needs a pullup resistor connected to DV_{DDIO} to hold the signal at a known value when the emulator is not connected. A resistor value of 4.7 kΩ or greater is suggested. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference [literature number: SPRU589]. The IPU resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPU is enabled at reset.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-3. RESET, Interrupts, and JTAG Signal Descriptions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
TDO	M7	I/O/Z	IPU DV_{DDIO} BH	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance (Hi-Z) state except when the scanning of data is in progress. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference [literature number: SPRU589]. If the emulation header is located greater than 6 inches from the device, TDO must be buffered. Despite the fact that the IEEE 1149.1 (JTAG) standard defines the TDO pin as a 3-state output (O/Z), this device has a bidirectional IO-cell. The bidirectional cell's input buffer is used for non-JTAG production test purposes. To achieve the lowest power, this input buffer must not be allowed to float. The IEEE standard defines the pin as tri-stated in the Test-Logic-Reset state and our device obeys that requirement. Therefore, to achieve the lowest power the IPU should remain enabled. The IPU resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPU is enabled at reset.
TDI	L7	I	IPU DV_{DDIO} BH	IEEE standard 1149.1 test data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. If the emulation header is located greater than 6 inches from the device, TDI must be buffered. In this case, the input buffer for TDI needs a pullup resistor connected to DV_{DDIO} to hold this signal at a known value when the emulator is not connected. A resistor value of 4.7 kΩ or greater is suggested. The IPU resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPU is enabled at reset.
TCK	M6	I	IPU DV_{DDIO} BH	IEEE standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK. If the emulation header is located greater than 6 inches from the device, TCK must be buffered. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference [literature number: SPRU589]. The IPU resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPU is enabled at reset.
$\overline{TRST}$	M9	I	IPD DV_{DDIO} BH	IEEE standard 1149.1 reset signal for test and emulation logic. $\overline{TRST}$, when high, allows the IEEE standard 1149.1 scan and emulation logic to take control of the operations of the device. If $\overline{TRST}$ is not connected or is driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. The device will ***not*** operate properly if this reset pin is never asserted low. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference [literature number: SPRU589]. It is recommended that an external pulldown resistor be used in addition to the IPD -- especially if there is a long trace to an emulation header. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is enabled at reset.

Table 4-3. RESET, Interrupts, and JTAG Signal Descriptions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
EMU1	M5	I/O/Z	IPU DV_{DDIO} BH	Emulator 1 pin. EMU1 is used as an interrupt to or from the emulator system and is defined as input/output by way of the emulation logic. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference [literature number: SPRU589]. An external pullup to DV_{DDIO} is required to provide a signal rise time of less than 10 µsec. A 4.7-kΩ resistor is suggested for most applications. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference [literature number: SPRU589]. The IPU resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPU is enabled at reset.
EMU0	L6	I/O/Z	IPU DV_{DDIO} BH	Emulator 0 pin. When $\overline{TRST}$ is driven low and then high, the state of the EMU0 pin is latched and used to connect the JTAG pins (TCK, TMS, TDI, TDO) to either the IEEE1149.1 Boundary-Scan TAP (when the latched value of EMU0 = 0) or to the DSP Emulation TAP (when the latched value of EMU0 = 1). Once $\overline{TRST}$ is high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of the emulation logic. An external pullup to DV_{DDIO} is required to provide a signal rise time of less than 10 µsec. A 4.7-kΩ resistor is suggested for most applications. For board design guidelines related to the emulation header, see the *XDS560 Emulator* Technical Reference [literature number: SPRU589]. The IPU resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPU is enabled at reset.
EXTERNAL INTERRUPTS				
$\overline{INT1}$	E7	I	IPU DV_{DDIO} BH	External interrupt inputs ($\overline{INT1}$ and $\overline{INT0}$). These pins are maskable via their specific Interrupt Mask Register (IMR1, IMR0) and the interrupt mode bit. The pins can be polled and reset by their specific Interrupt Flag Register (IFR1, IFR0). The IPU resistor on these pins can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPU is disabled at reset.
$\overline{INT0}$	C6	I	IPU DV_{DDIO} BH	

4.2.4 External Memory Interface (EMIF)

Table 4-4. EMIF Signal Descriptions

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
EMIF FUNCTIONAL PINS: ASYNC (NOR, SRAM, and NAND)				
				Note: When accessing 8-bit Asynchronous memory: • Connect EM_A[20:0] to memory address pins [22:2] • Connect EM_BA[1:0] to memory address pins [1:0] For 16-bit Asynchronous memory: • Connect EM_A[20:1] to memory address pins [20:1] • Connect EM_BA[1] to memory address pin [0]
GP[26]/ EM_A[20]	J3	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 20. Mux control via the A20_MODE bit in the EBSR (see Figure 5-10). The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is disabled at reset.
GP[25]/ EM_A[19]	G4	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 19. Mux control via the A19_MODE bit in the EBSR (see Figure 5-10). The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is disabled at reset.
GP[24]/ EM_A[18]	G2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 18. Mux control via the A18_MODE bit in the EBSR (see Figure 5-10). The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is disabled at reset.
GP[23]/ EM_A[17]	F2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 17. Mux control via the A17_MODE bit in the EBSR (see Figure 5-10). The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is disabled at reset.
GP[22]/ EM_A[16]	E2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 16. Mux control via the A16_MODE bit in the EBSR (see Figure 5-10). The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is disabled at reset.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal
(5) Pins with multiple names default to the first, bolded name when reset (for example, **GP[21]**/EM_A[15] defaults to GP[21] when reset).

Table 4-4. EMIF Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
GP[21]/ EM_A[15]	N1	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 15. Mux control via the A15_MODE bit in the EBSR (see Figure 5-10). The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is disabled at reset.
EM_A[14]	M1	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 14. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[13]	L1	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 13. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[12]/ (CLE)	K1	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 12. When interfacing with NAND Flash, this pin also acts as Command Latch Enable (CLE). The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[11]/ (ALE)	K2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 11. When interfacing with NAND Flash, this pin also acts as Address Latch Enable (ALE). The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[10]	L2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 10. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[9]	J2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 9. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[8]	J1	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 8. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[7]	H2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 7. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.

Table 4-4. EMIF Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
EM_A[6]	F1	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 6. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[5]	D1	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 5. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[4]	C1	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 4. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[3]	D2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 3. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[2]	E1	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 2. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[1]	C2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 1. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.
EM_A[0]	B2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is the EMIF external address pin 0. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR5 (1C4Dh) register. The IPD is disabled at reset.

Table 4-4. EMIF Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
EM_D[15]	J4	I/O/Z	IPD DV_{DDEMIF} BH	EMIF 16-bit bidirectional bus. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR4 (1C4Ch) register. The IPD is disabled at reset.
EM_D[14]	K3			
EM_D[13]	K4			
EM_D[12]	L3			
EM_D[11]	C4			
EM_D[10]	D3			
EM_D[9]	F4			
EM_D[8]	E3			
EM_D[7]	H3			
EM_D[6]	K5			
EM_D[5]	M2			
EM_D[4]	L4			
EM_D[3]	D4			
EM_D[2]	F3			
EM_D[1]	E5			
EM_D[0]	G3			
$\overline{EM\_CS5}$	A3	O/Z	IPD DV_{DDEMIF} BH	EMIF chip select 5 output for use with asynchronous memories (that is, NOR flash, NAND flash, or SRAM). The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is disabled at reset.
$\overline{EM\_CS4}$	C3	O/Z	IPD DV_{DDEMIF} BH	EMIF chip select 4 output for use with asynchronous memories (that is, NOR flash, NAND flash, or SRAM). The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is disabled at reset.
$\overline{EM\_CS3}$	M4	O/Z	IPD DV_{DDEMIF} BH	EMIF NAND chip select 3 output for use with asynchronous memories (that is, NOR flash, NAND flash, or SRAM). The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is disabled at reset.
$\overline{EM\_CS2}$	C5	O/Z	IPD DV_{DDEMIF} BH	EMIF NAND chip select 2 output for use with asynchronous memories (that is, NOR flash, NAND flash, or SRAM). The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is disabled at reset.
$\overline{EM\_WE}$	H1	O/Z	IPD DV_{DDEMIF} BH	EMIF asynchronous memory write enable output The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is disabled at reset.
$\overline{EM\_OE}$	E4	O/Z	IPD DV_{DDEMIF} BH	EMIF asynchronous memory read enable output The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is disabled at reset.

Table 4-4. EMIF Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
EM_R/$\overline{W}$	B6	O/Z	IPD DV_{DDEMIF} BH	EMIF asynchronous read and write output The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is disabled at reset.
EM_DQM1/ UHPI_HBE1	P1	I/O/Z	IPD DV_{DDEMIF} BH	These pins are multiplexed between EMIF and UHPI. For EMIF, asynchronous data write strobes and byte enables or EMIF SDRAM and mSDRAM data mask bits. Mux control via the PPMODE bits in the EBSR. The IPD resistor on these pins can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is disabled at reset.
EM_DQM0/ UHPI_HBE0	B5	I/O/Z	IPD DV_{DDEMIF} BH	
EM_BA[1]	B1	O/Z	IPD DV_{DDEMIF} BH	EMIF asynchronous bank address 16-bit wide memory: EM_BA[1] forms the device address[0] and BA[0] forms device address [23]. 8-bit wide memory: EM_BA[1] forms the device address[1] and BA[0] forms device address [0]. EMIF SDRAM and mSDRAM bank address. The IPD resistor on these pins can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is disabled at reset.
EM_BA[0]	A1	O/Z	IPD DV_{DDEMIF} BH	
EM_WAIT5	H4	I	IPD DV_{DDEMIF} BH	EMIF wait state extension input 5 for $\overline{EM\_CS5}$ The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is enabled at reset.
EM_WAIT4	G1	I	IPD DV_{DDEMIF} BH	EMIF wait state extension input 4 for $\overline{EM\_CS4}$ The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is enabled at reset.
EM_WAIT3	K6	I	IPD DV_{DDEMIF} BH	EMIF wait state extension input 3 for $\overline{EM\_CS3}$ The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is enabled at reset.
EM_WAIT2	D5	I	IPD DV_{DDEMIF} BH	EMIF wait state extension input 2 for $\overline{EM\_CS2}$ The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is enabled at reset.
EMIF FUNCTIONAL PINS: SDRAM and mSDRAM ONLY				
$\overline{EM\_CS1}$/ UHPI_HDS2	A4	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and UHPI. For EMIF, SDRAM and mSDRAM chip select 1 output Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.

Table 4-4. EMIF Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
$\overline{\text{EM\_CS0}}$/ UHPI_HDS1	B3	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and UHPI. For EMIF, SDRAM and mSDRAM chip select 0 output Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register.
EM_SDCLK	M3	O/Z	IPD DV_{DDEMIF} BH	EMIF SDRAM and mSDRAM clock The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
EM_SDCKE/ UHPI_HHWIL	N2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and UHPI. For EMIF, SDRAM and mSDRAM clock enable Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
$\overline{\text{EM\_SDRAS}}$/ UHPI_HAS	A6	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and UHPI. For EMIF, SDRAM and mSDRAM row address strobe Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
$\overline{\text{EM\_SDCAS}}$/ UHPI_HCS	B4	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and UHPI. For EMIF, SDRAM and mSDRAM column strobe Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.

4.2.5 Inter-Integrated Circuit (I2C)

Table 4-5. Inter-Integrated Circuit (I2C) Signal Descriptions

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
I2C				
SCL	B7	I/O/Z	– DV_{DDIO} BH	This pin is the I2C clock output. Per the I2C standard, an external pullup is required on this pin.
SDA	B8	I/O/Z	– DV_{DDIO} BH	This pin is the I2C bidirectional data signal. Per the I2C standard, an external pullup is required on this pin.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

4.2.6 Inter-IC Sound (I2S)

Table 4-6. Inter-IC Sound (I2S0, I2S2, and I2S3) Signal Descriptions

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
Interface 0 (I2S0)				
MMC0_D0/ I2S0_DX/ GP[2]/ McBSP_DX	L9	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP and GPIO. For I2S, it is I2S0 transmit data output I2S0_DX. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_CLK/ I2S0_CLK/ GP[0]/ McBSP_CLKX	L10	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP and GPIO. For I2S, it is I2S0 clock input/output I2S0_CLK. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_D1/ I2S0_RX/ GP[3]/ McBSP_DR	M10	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP and GPIO. For I2S, it is I2S0 receive data input I2S0_RX. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_CMD/ I2S0_FS/ GP[1]/ McBSP_FSX	M11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP and GPIO. For I2S, it is I2S0 frame synchronization input/output I2S0_FS. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
Interface 1 (I2S2)				
I2S2_DX/ UHPI_HD[11]/ GP[27]/ SPI_TX	P12	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between I2S2, UHPI, GPIO, and SPI. For I2S, it is I2S2 transmit data output I2S2_DX. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is disabled at reset.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal
(5) Pins with multiple names default to the first, bolded name when reset (for example, **GP[21]**/EM_A[15] defaults to GP[21] when reset).

Table 4-6. Inter-IC Sound (I2S0, I2S2, and I2S3) Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
I2S2_CLK/ UHPI_HD[8]/ GP[18]/ SPI_CLK	N10	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between I2S2, UHPI, GPIO, and SPI. For I2S, it is I2S2 clock input/output I2S2_CLK. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
I2S2_RX/ UHPI_HD[10]/ GP[20]/ SPI_RX	N11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI, I2S2, GPIO, and SPI. For I2S, it is I2S2 receive data input I2S2_RX. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
I2S2_FS/ UHPI_HD[9]/ GP[19]/ SPI_CS0	P11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between I2S2, UHPI, GPIO, and SPI. For I2S, it is I2S2 frame synchronization input/output I2S2_FS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
Interface 2 (I2S3)				
UART_TXD/ UHPI_HD[15]/ GP[31]/ I2S3_DX	P14	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UART, UHPI, GPIO, and I2S3. For I2S, it is I2S3 transmit data output I2S3_DX. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is disabled at reset.
UART_RTS/ UHPI_HD[12]/ GP[28]/ I2S3_CLK	N12	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UART, UHPI, GPIO, and I2S3. For I2S, it is I2S3 clock input/output I2S3_CLK. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is disabled at reset.
UART_RXD/ UHPI_HD[14]/ GP[30]/ I2S3_RX	N13	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UART, UHPI, GPIO, and I2S3. For I2S, it is I2S3 receive data input I2S3_RX. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
UART_CTS/ UHPI_HD[13]/ GP[29]/ I2S3_FS	P13	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UART, UHPI, GPIO, and I2S3. For I2S, it is I2S3 frame synchronization input/output I2S3_FS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.

4.2.7 Multichannel Buffered Serial Port (McBSP)

Table 4-7. McBSP Signal Descriptions

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
McBSP				
MMC0_CLK/ I2S0_CLK/ GP[0]/ McBSP_CLKX	L10	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP and GPIO. For McBSP, this is the McBSP transmit clock, McBSP_CLKX. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_CMD/ I2S0_FS/ GP[1]/ McBSP_FSX	M11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP and GPIO. For McBSP, this is the McBSP transmit frame sync, McBSP_FSX. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_D0/ I2S0_DX/ GP[2]/ McBSP_DX	L9	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP and GPIO. For McBSP, this is the McBSP transmit data , McBSP_DX. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_D1/ I2S0_RX/ GP[3]/ McBSP_DR	M10	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP and GPIO. For McBSP, this is the McBSP receive data, McBSP_RX. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_D2/ GP[4]/ McBSP_FSR	L12	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, McBSP and GPIO. For McBSP, this is the McBSP receive frame sync, McBSP_FSR. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal
(5) Pins with multiple names default to the first, bolded name when reset (for example, **GP[21]**/EM_A[15] defaults to GP[21] when reset).

Table 4-7. McBSP Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
MMC0_D3/ GP[5]/ McBSP_CLKR_ CLKS	L11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, McBSP and GPIO. For McBSP, this is the McBSP receive clock, McBSP_CLKR or the McBSP sample rate generator clock input, McBSP_CLKS. The bit 15 of EBSR register determines this port to be McBSP_CLKR or McBSP_CLKS. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.

4.2.8 Multichannel Serial Port Interface (McSPI)

Table 4-8. McSPI Signal Descriptions

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
McSPI				
MMC1_CLK/ McSPI_CLK/ GP[6]	M13	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI and GPIO. For McSPI, this is the McSPI data clock, McSPI_CLK. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC1_CMD/ McSPI_CS0/ GP[7]	L14	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI and GPIO. For McSPI, this is the McSPI chip select 0 signal, McSPI_CS0. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC1_D0/ McSPI_SIMO/ GP[8]	M14	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI and GPIO. For McSPI, this is the McSPI data, McSPI_SIMO (Slave Input Master Output). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC1_D1/ McSPI_SOMI/ GP[9]	M12	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI and GPIO. For McSPI, this is the McSPI data, McSPI_SOMI (Slave Output Master Input). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC1_D2/ McSPI_CS1/ GP[10]	K14	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI and GPIO. For McSPI, this is the McSPI chip select 1 signal, McSPI_CS1. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal
(5) Pins with multiple names default to the first, bolded name when reset (for example, **GP[21]**/EM_A[15] defaults to GP[21] when reset).

Table 4-8. McSPI Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
MMC1_D3/ McSPI_CS2/ GP[11]	L13	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI and GPIO. For McSPI, this is the McSPI chip select 2 signal, McSPI_CS2. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.

4.2.9 Serial Peripheral Interface (SPI)

Table 4-9. SPI Signal Descriptions

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
Serial Port Interface (SPI)				
SPI_CS0/ UHPI_HCNTL0	P4	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS0. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
I2S2_FS/ UHPI_HD[9]/ GP[19]/ SPI_CS0	P11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between I2S2, UHPI, GPIO, and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS0. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
SPI_CS1/ UHPI_HCNTL1	N4	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SPI and UHPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS1. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
SPI_CS2/ UHPI_HR_NW	P5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SPI and UHPI. For SPI, this pin is SPI chip select SPI_CS2. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
SPI_CS3/ UHPI_HRDY	N5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SPI and UHPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS3. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
SPI_CLK / UHPI_HINT	N3	O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SPI and UHPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is clock output SPI_CLK. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal
(5) Pins with multiple names default to the first, bolded name when reset (for example, **GP[21]**/EM_A[15] defaults to GP[21] when reset).

Table 4-9. SPI Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
I2S2_CLK/ UHPI_HD[8]/ GP[18]/ SPI_CLK	N10	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between I2S2, UHPI, GPIO, and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is clock output SPI_CLK. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
SPI_TX / UHPI_HD[1]	N6	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI transmit data output. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
I2S2_DX/ UHPI_HD[11]/ GP[27]/ SPI_TX	P12	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between I2S2, UHPI, GPIO, and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI transmit data output. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is disabled at reset.
SPI_RX/ UHPI_HD[0]	P6	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SPI and UHPI. Mux control via the PPMODE bits in the EBSR. For SPI this pin is SPI receive data input. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
I2S2_RX/ UHPI_HD[10]/ GP[20]/ SPI_RX	N11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between I2S2, UHPI, GPIO, and SPI. Mux control via the PPMODE bits in the EBSR. For SPI this pin is SPI receive data input. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.

4.2.10 Universal Asynchronous Receiver and Transmitter (UART)

Table 4-10. UART Signal Descriptions

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
UART				
UART_RXD/ UHPI_HD[14]/ GP[30]/ I2S3_RX	N13	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UART, UHPI, GPIO, and I2S3. When used by UART, it is the receive data input UART_RXD. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
UART_TXD/ UHPI_HD[15]/ GP[31]/ I2S3_DX	P14	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UART, UHPI, GPIO, and I2S3. In UART mode, it is the transmit data output UART_TXD. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is disabled at reset.
UART_CTS/ UHPI_HD[13]/ GP[29]/ I2S3_FS	P13	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UART, UHPI, GPIO, and I2S3. In UART mode, it is the clear to send input UART_CTS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
UART_RTS/ UHPI_HD[12]/ GP[28]/ I2S3_CLK	N12	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UART, UHPI, GPIO, and I2S3. In UART mode, it is the ready to send output UART_RTS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is disabled at reset.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal
(5) Pins with multiple names default to the first, bolded name when reset (for example, **GP[21]**/EM_A[15] defaults to GP[21] when reset).

4.2.11 Universal Serial Bus (USB) 2.0

Table 4-11. USB2.0 Signal Descriptions

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
USB 2.0				
USB_MXI	G13	I	USB_V_{DDOSC}	12-MHz crystal oscillator input used for the USB subsystem and optionally for the system clock generator. If CLK_SEL=0, the USB oscillator is enabled at reset and is used as the clock source for the system clock generator. In this configuration (CLK_SEL=0), the USB oscillator cannot be disabled. If CLK_SEL=1, the USB oscillator is disabled at reset and the CLKIN pin is used as the source for the system clock generator. In this configuration (CLK_SEL=1), the USB oscillator can be enabled or disabled via software. When using an external 12-MHz oscillator, the external oscillator clock signal should be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V_{IH} requirement (see Section 5.2, *Recommended Operating Conditions*). The USB_MXO is left unconnected and the USB_V_{SSOSC} signal is connected to board ground (V_{SS}).
USB_MXO	G14	O	USB_V_{DDOSC}	12-MHz crystal oscillator output used for the USB subsystem and optionally for the system clock generator. If CLK_SEL=0, the USB oscillator is enabled at reset and is used as the clock source for the system clock generator. In this configuration (CLK_SEL=0), the USB oscillator cannot be disabled. If CLK_SEL=1, the USB oscillator is disabled at reset and the CLKIN pin is used as the source for the system clock generator. In this configuration (CLK_SEL=1), the USB oscillator can be enabled or disabled via software. When using an external 12-MHz oscillator, the external oscillator clock signal should be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V_{IH} requirement (see Section 5.2, *Recommended Operating Conditions*). The USB_MXO is left unconnected and the USB_V_{SSOSC} signal is connected to board ground (V_{SS}).
USB_V_{DDOSC}	G12	S	see Section 5.2, ROC	3.3-V power supply for USB oscillator. When the USB peripheral ***is not*** used, USB_V_{DDOSC} should be connected to ground (V_{SS}).
USB_V_{SSOSC}	F11	S	see Section 5.2, ROC	Ground for USB oscillator. When using a 12-MHz crystal, this pin is a local ground for the crystal and must not be connected to the board ground (See Figure 5-11). When using an external 12-MHz oscillator, the external oscillator clock signal should be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V_{IH} requirement (see Section 5.2, *Recommended Operating Conditions*). The USB_MXO is left unconnected and the USB_V_{SSOSC} signal is connected to board ground (V_{SS}).
USB_VBUS	J12	A	see Section 5.2, ROC	USB power detect. 5-V input that signifies that VBUS is connected. This signal must be powered on in the order listed in Section 5.7.2.2, *Power-Supply Sequencing*. When the USB peripheral ***is not*** used, the USB_VBUS signal should be connected to ground (V_{SS}).
USB_DP	H14	A I/O	USB_V_{DDA3P3}	USB bidirectional Data Differential signal pair [positive and negative].
USB_DM	J14	A I/O	USB_V_{DDA3P3}	When the USB peripheral ***is not*** used, the USB_DP and USB_DM signals should both be tied to ground (V_{SS}).

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-11. USB2.0 Signal Descriptions (continued)

SIGNAL NAME	NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
USB_R1	G9	A I/O	USB_V_{DDA3P3}	External resistor connect. Reference current output. This pin must be connected via a 10-kΩ ±1% resistor to USB_V_{SSREF} and be placed as close to the device as possible. When the USB peripheral ***is not*** used, the USB_R1 signal should be connected via a 10-kΩ resistor to USB_V_{SSREF}.
USB_V_{SSREF}	G10	GND	see Section 5.2, ROC	Ground for reference current. This must be connected via a 10-kΩ ±1% resistor to USB_R1. When the USB peripheral ***is not*** used, the USB_V_{SSREF} signal should be connected directly to ground (V_{ss}).
USB_V_{DDA3P3}	H12	S	see Section 5.2, ROC	Analog 3.3 V power supply for USB PHY. This signal must be powered on in the order listed in Section 5.7.2.2, *Power-Supply Sequencing*. When the USB peripheral ***is not*** used, the USB_V_{DDA3P3} signal should be connected to ground (V_{SS}).
USB_V_{SSA3P3}	H11	GND	see Section 5.2, ROC	Analog ground for USB PHY.
USB_V_{DDA1P3}	H10	S	see Section 5.2, ROC	Analog 1.3 V power supply for USB PHY. [For high-speed sensitive analog circuits] This signal must be powered on in the order listed in Section 5.7.2.2, *Power-Supply Sequencing*. When the USB peripheral ***is not*** used, the USB_V_{DDA1P3} signal should be connected to ground (V_{SS}).
USB_V_{SSA1P3}	H9	GND	see Section 5.2, ROC	Analog ground for USB PHY [For high speed sensitive analog circuits].
USB_V_{DD1P3}	J13	S	see Section 5.2, ROC	1.3-V digital core power supply for USB PHY. This signal must be powered on in the order listed in Section 5.7.2.2, *Power-Supply Sequencing*. When the USB peripheral ***is not*** used, the USB_V_{DD1P3} signal should be connected to ground (V_{SS}).
USB_V_{SS1P3}	H13	GND	see Section 5.2, ROC	Digital core ground for USB PHY.
USB_V_{DDPLL}	G8	S	see Section 5.2, ROC	3.3 V USB Analog PLL power supply. Care should be taken to prevent noise on this supply. Consider using a ferrite bead if the power supply for this pin is shared with digital logic. See the *Filtering Techniques* Application Report [literature number: SCAA048] for more information. When the USB peripheral ***is not*** used, the USB_V_{DDPLL} signal should be connected to ground (V_{SS}).
USB_V_{SSPLL}	G11	GND	see Section 5.2, ROC	USB Analog PLL ground.

4.2.12 Universal Host-Port Interface (UHPI)

Table 4-12. UHPI Signal Descriptions

SIGNAL NAME(5)	NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
SPI_CLK/ UHPI_HINT	N3	O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SPI and UHPI. For UHPI, this pin is UHPI host interrupt, UHPI_HINT. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
SPI_CS0/ UHPI_HCNTL0	P4	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SPI and UHPI. For UHPI, this pin is UHPI access control, UHPI_HCNTL0. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
SPI_CS1/ UHPI_HCNTL1	N4	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SPI and UHPI. For UHPI, this pin is UHPI access control, UHPI_HCNTL1. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
SPI_CS2/ UHPI_HR_NW	P5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SPI and UHPI. For UHPI this pin is UHPI read and write, UHPI_HR_NW. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
SPI_CS3/ UHPI_HRDY	N5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SPI and UHPI. For UHPI, this pin is the UHPI ready, UHPI_HRDY. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
UART_TXD/ UHPI_HD[15]/ GP[31]/ I2S3_DX	P14	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI, UART, SPI, I2S, and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is disabled at reset.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal
(5) Pins with multiple names default to the first, bolded name when reset (for example, **GP[21]**/EM_A[15] defaults to GP[21] when reset).

Table 4-12. UHPI Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
UART_RXD/ UHPI_HD[14]/ GP[30]/ I2S3_RX	N13	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI, UART, SPI, I2S, and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
UART_CTS/ UHPI_HD[13]/ GP[29]/ I2S3_FS	P13	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI, UART, SPI, I2S, and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
UART_RTS/ UHPI_HD[12]/ GP[28]/ I2S3_CLK	N12	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI, UART, SPI, I2S, and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is disabled at reset.
I2S2_DX/ UHPI_HD[11]/ GP[27]/ SPI_TX	P12	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI, UART, SPI, I2S, and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is disabled at reset.
I2S2_RX/ UHPI_HD[10]/ GP[20]/ SPI_RX	N11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI, UART, SPI, I2S, and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
I2S2_FS/ UHPI_HD[9]/ GP[19]/ SPI_CS0	P11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI, UART, SPI, I2S, and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
I2S2_CLK/ UHPI_HD[8]/ GP[18]/ SPI_CLK	N10	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI, UART, SPI, I2S, and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.

Table 4-12. UHPI Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
GP[17]/ UHPI_HD[7]	P10	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
GP[16]/ UHPI_HD[6]	N9	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
GP[15]/ UHPI_HD[5]	P9	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
GP[14]/ UHPI_HD[4]	N8	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
GP[13]/ UHPI_HD[3]	N7	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
GP[12]/ UHPI_HD[2]	P7	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and GPIO. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
SPI_TX/ UHPI_HD[1]	N6	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and SPI. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.

Table 4-12. UHPI Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
SPI_RX/ UHPI_HD[0]	P6	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and SPI. For UHPI, this pin is the UHPI data bus, UHPI_HD[15:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
EM_DQM1/ UHPI_HBE1	P1	I/O/Z	IPD DV_{DDIO} BH	These two pins are multiplexed between UHPI and SDRAM. For UHPI, these two pins are UHPI Byte Enables, UHPI_HBE[1:0]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on these pins can be enabled or disabled via the PUDINHIBR6 (1C4Fh) register. The IPD is disabled at reset.
EM_DQM0/ UHPI_HBE0	B5	I/O/Z	IPD DV_{DDIO} BH	
$\overline{\text{EM\_CS1}}$/ UHPI_HDS2	A4	I/O/Z	IPD DV_{DDIO} BH	These two pins are multiplexed between UHPI and SDRAM. For UHPI, these two pins are UHPI data strobe pins, UHPI_HDS[2:1]. Mux control via the PPMODE bits in the EBSR. The IPD resistor on these pins can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
$\overline{\text{EM\_CS0}}$/ UHPI_HDS1	B3	I/O/Z	IPD DV_{DDIO} BH	
EM_SDCKE/ UHPI_HHWIL	N2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and SDRAM. For UHPI, this pin is Half-word Identification control input pin, UHPI_HHWIL. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
$\overline{\text{EM\_SDRAS}}$/ UHPI_HAS	A6	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and SDRAM. For UHPI, this pin is address strobe pin, UHPI_HAS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.
$\overline{\text{EM\_SDCAS}}$/ UHPI_HCS	B4	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UHPI and SDRAM. For UHPI, this pin is chip select pin, UHPI_HCS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR7 (1C50h) register. The IPD is disabled at reset.

4.2.13 MultiMedia Card (MMC)

Table 4-13. MMC1 and SD Signal Descriptions

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
MMC and SD				
MMC1_CLK/ McSPI_CLK/ GP[6]	M13	O	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI, and GPIO. For MMC and SD, this is the MMC1 data clock output MMC1_CLK. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC1_CMD/ McSPI_CS0/ GP[7]	L14	O	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI, and GPIO. For MMC and SD, this is the MMC1 command I/O output MMC1_CMD. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC1_D3/ McSPI_CS2/ GP[11]	L13	I/O/Z	IPD DV_{DDIO} BH	These pins are multiplexed between MMC1, McSPI, and GPIO. In MMC and SD mode, all these pins are the MMC1 nibble wide bidirectional data bus. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on these pins can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC1_D2/ McSPI_CS1/ GP[10]	K14	I/O/Z	IPD DV_{DDIO} BH	
MMC1_D1/ McSPI_SOMI/ GP[9]	M12	I/O/Z	IPD DV_{DDIO} BH	
MMC1_D0/ McSPI_SIMO/ GP[8]	M14	I/O/Z	IPD DV_{DDIO} BH	

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal
(5) Pins with multiple names default to the first, bolded name when reset (for example, **GP[21]**/EM_A[15] defaults to GP[21] when reset).

Table 4-14. MMC0 and SD Signal Descriptions

SIGNAL NAME(5)	NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
MMC and SD				
MMC0_CLK/ I2S0_CLK/ GP[0]/ McBSP_CLKX	L10	O	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP, and GPIO. For MMC and SD, this is the MMC0 data clock output MMC0_CLK. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_CMD/ I2S0_FS/ GP[1]/ McBSP_FSX	M11	O	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP, and GPIO. For MMC and SD, this is the MMC0 command I/O output MMC0_CMD. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_D3/ GP[5]/ McBSP_CLKR_ CLKS	L11	I/O/Z	IPD DV_{DDIO} BH	These pins are multiplexed between MMC0, I2S0, McBSP and GPIO In MMC and SD mode, these pins are the MMC0 nibble wide bidirectional data bus. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on these pins can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_D2/ GP[4]/ McBSP_FSR	L12	I/O/Z	IPD DV_{DDIO} BH	
MMC0_D1/ I2S0_RX/ GP[3]/ McBSP_DR	M10	I/O/Z	IPD DV_{DDIO} BH	
MMC0_D0/ I2S0_DX/ GP[2]/ McBSP_DX	L9	I/O/Z	IPD DV_{DDIO} BH	

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal
(5) Pins with multiple names default to the first, bolded name when reset (for example, **GP[21]**/EM_A[15] defaults to GP[21] when reset).

4.2.14 Successive Approximation (SAR) Analog-to-Digital Converter (ADC)

Table 4-15. 10-Bit SAR ADC Signal Descriptions

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
SAR ADC				
GPAIN0	D10	I/O	V_{DDA_ANA}	GPAIN0: General -Purpose Output and Analog Input pin 0. This pin is demuxed internally into ADC Channels 0, 1, and 2. GPAIN0 can also be used as a general-purpose open-drain output. This pin is unique among the GPAIN pins in that it is the only pin that is 3.6 V-tolerant to support measuring a battery voltage. GPAIN0 can accommodate input voltages from 0 V to 3.6 V; although, the ADC is unable to accept signals greater than V_{DDA_ANA} without clamping. ADC Channel 1 is capable of switching in an internal resistor divider that has a divide ratio of approximately 1/8.
GPAIN1	A11	I/O	V_{DDA_ANA}	GPAIN1: General -Purpose Output and Analog Input pin 1. This pin is connected to ADC Channel 3. GPAIN1 can be used as a general-purpose output if certain requirements are met (see the following note). GPAIN1 can accommodate input voltages from 0 V to V_{DDA_ANA}. **Note:** If the ANA_LDO is used to supply power to V_{DDA_ANA}, this pin must ***not*** be used as a general-purpose output (driving high) since the max current capability (see the I_{SD} parameter in Section 5.3.2, *Electrical Characteristics*) of the ANA_LDO can be exceeded. Doing so may result in the on-chip power-on reset (POR) resetting the chip.
GPAIN2	B11	I/O	V_{DDA_ANA}	GPAIN2: General -Purpose Output and Analog Input pin 2. This pin is connected to ADC Channel 4. GPAIN2 can be used as a general-purpose output if certain requirements are met (see the following note). GPAIN2 can accommodate input voltages from 0 V to V_{DDA_ANA}. **Note:** If the ANA_LDO is used to supply power to V_{DDA_ANA}, this pin must ***not*** be used as a general-purpose output (driving high) since the max current capability (see the I_{SD} parameter in Section 5.3.2, *Electrical Characteristics*) of the ANA_LDO can be exceeded. Doing so may result in the on-chip POR resetting the chip.
GPAIN3	C11	I/O	V_{DDA_ANA}	GPAIN3: General -Purpose Output and Analog Input pin 3. This pin is connected to ADC Channel 5. GPAIN3 can be used as a general-purpose output if certain requirements are met (see the following note). GPAIN3 can accommodate input voltages from 0 V to V_{DDA_ANA}. **Note:** If the ANA_LDO is used to supply power to V_{DDA_ANA}, this pin must ***not*** be used as a general-purpose output (driving high) since the max current capability (see the I_{SD} parameter in Section 5.3.2, *Electrical Characteristics*) of the ANA_LDO can be exceeded. Doing so may result in the on-chip POR resetting the chip.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

4.2.15 General-Purpose Input and Output (GPIO)

Table 4-16. GPIO Signal Descriptions

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
General-Purpose Input/Output				
XF	M8	O/Z	IPU DV_{DDIO} BH	External Flag Output. XF is used for signaling other processors in multiprocessor configurations or XF can be used as a fast general-purpose output pin. XF is set high by the BSET XF instruction and XF is set low by the BCLR XF instruction or by writing to bit 13 of the ST1_55 register. For more information on the ST1_55 register, see the *C55x 3.0 CPU* Reference Guide [literature number: SWPU073]. For the XF pin's states after reset, see Figure 5-9, *BootMode Latching*. XF pin can manually configured as Hi-Z state only in boundary-scan mode. When this pin is in Hi-Z state, the IPU is enabled. The IPU on this pin is disabled at reset.
MMC0_CLK/ I2S0_CLK/ GP[0]/ McBSP_CLKX	L10	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP, and GPIO. For GPIO, it is general-purpose input/output pin 0 (GP[0]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_CMD/ I2S0_FS/ GP[1]/ McBSP_FSX	M11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP, and GPIO. For GPIO, it is general-purpose input/output pin 1 (GP[1]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_D0/ I2S0_DX/ GP[2]/ McBSP_DX	L9	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP, and GPIO. For GPIO, it is general-purpose input/output pin 2 (GP[2]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_D1/ I2S0_RX/ GP[3]/ McBSP_DR	M10	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, I2S0, McBSP, and GPIO. For GPIO, it is general-purpose input/output pin 3 (GP[3]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal
(5) Pins with multiple names default to the first, bolded name when reset (for example, **GP[21]**/EM_A[15] defaults to GP[21] when reset).

Table 4-16. GPIO Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
MMC0_D2/ GP[4]/ McBSP_FSR	L12	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, McBSP, and GPIO. For GPIO, it is general-purpose input/output pin 4 (GP[4]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC0_D3/ GP[5]/ McBSP_CLKR_ CLKS	L11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC0, McBSP, and GPIO. For GPIO, it is general-purpose input/output pin 5 (GP[5]). Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC1_CLK/ McSPI_CLK/ GP[6]	M13	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI, and GPIO. For GPIO, it is general-purpose input/output pin 6 (GP[6]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC1_CMD/ McSPI_CS0/ GP[7]	L14	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI, and GPIO. For GPIO, it is general-purpose input/output pin 7 (GP[7]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC1_D0/ McSPI_SIMO/ GP[8]	M14	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI, and GPIO. For GPIO, it is general-purpose input/output pin 8 (GP[8]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC1_D1/ McSPI_SOMI/ GP[9]	M12	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI, and GPIO. For GPIO, it is general-purpose input/output pin 9 (GP[9]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
MMC1_D2/ McSPI_CS1/ GP[10]	K14	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI, and GPIO. For GPIO, it is general-purpose input/output pin 10 (GP[10]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.

Table 4-16. GPIO Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
MMC1_D3/ McSPI_CS2/ GP[11]	L13	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between MMC1, McSPI, and GPIO. For GPIO, it is general-purpose input/output pin 11 (GP[11]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR1 (1C17h) register. The IPD is disabled at reset.
GP[12]/ UHPI_HD[2]	P7	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between GPIO and UHPI. For GPIO, it is general-purpose input/output pin 12 (GP[12]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
GP[13]/ UHPI_HD[3]	N7	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between GPIO and UHPI. For GPIO, it is general-purpose input/output pin 13 (GP[13]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
GP[14]/ UHPI_HD[4]	N8	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between GPIO and UHPI. For GPIO, it is general-purpose input/output pin 14 (GP[14]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
GP[15]/ UHPI_HD[5]	P9	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between GPIO and UHPI. For GPIO, it is general-purpose input/output pin 15 (GP[15]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
GP[16]/ UHPI_HD[6]	N9	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between GPIO and UHPI. For GPIO, it is general-purpose input/output pin 16 (GP[16]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
GP[17]/ UHPI_HD[7]	P10	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between GPIO and UHPI. For GPIO, it is general-purpose input/output pin 17 (GP[17]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.

Table 4-16. GPIO Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
I2S2_CLK/ UHPI_HD[8]/ GP[18]/ SPI_CLK	N10	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between I2S2, UHPI, GPIO, and SPI. For GPIO, it is general-purpose input/output pin 18 (GP[18]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
I2S2_FS/ UHPI_HD[9]/ GP[19]/ SPI_CS0	P11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between I2S2, UHPI, GPIO and SPI. For GPIO, it is general-purpose input/output pin 19 (GP[19]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
I2S2_RX/ UHPI_HD[10]/ GP[20]/ SPI_RX	N11	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between I2S2, UHPI, GPIO and SPI. For GPIO, it is general-purpose input/output pin 20 (GP[20]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
GP[21]/ EM_A[15]	N1	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 21 (GP[21]). Mux control via the A15_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is disabled at reset.
GP[22]/ EM_A[16]	E2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 22 (GP[22]). Mux control via the A16_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is disabled at reset.
GP[23]/ EM_A[17]	F2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 23 (GP[23]). Mux control via the A17_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is disabled at reset.
GP[24]/ EM_A[18]	G2	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 24 (GP[24]). Mux control via the A18_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is disabled at reset.

Table 4-16. GPIO Signal Descriptions (continued)

SIGNAL NAME[5]	NO.	TYPE[1] [2]	OTHER[3] [4]	DESCRIPTION
GP[25]/ EM_A[19]	G4	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 25 (GP[25]). Mux control via the A19_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is disabled at reset.
GP[26]/ EM_A[20]	J3	I/O/Z	IPD DV_{DDEMIF} BH	This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 26 (GP[26]). Mux control via the A20_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR2 (1C18h) register. The IPD is disabled at reset.
I2S2_DX/ UHPI_HD[11]/ GP[27]/ SPI_TX	P12	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between I2S2, UHPI, GPIO, and SPI. For GPIO, it is general-purpose input/output pin 27 (GP[27]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is disabled at reset.
UART_RTS/ UHPI_HD[12]/ GP[28]/ I2S3_CLK	N12	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UART, UHPI, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 28 (GP[28]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is disabled at reset.
UART_CTS/ UHPI_HD[13]/ GP[29]/ I2S3_FS	P13	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UART, UHPI, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 29 (GP[29]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
UART_RXD/ UHPI_HD[14]/ GP[30]/ I2S3_RX	N13	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UART, UHPI, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 30 (GP[30]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is enabled at reset.
UART_TXD/ UHPI_HD[15]/ GP[31]/ I2S3_DX	P14	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between UART, UHPI, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 31 (GP[31]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PUDINHIBR3 (1C19h) register. The IPD is disabled at reset.

4.2.16 Regulators and Power Management

Table 4-17. Regulators and Power Management Signal Descriptions

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
Regulators				
DSP_LDOO	E10	S		DSP_LDO output. When enabled, this output provides a regulated 1.3 V or 1.05 V output and up to 250 mA of current (see the I_{SD} parameter in Section 5.3.2, *Electrical Characteristics*). The DSP_LDO is intended to supply current to the digital core circuits only (CV_{DD}) but not to CV_{DDRTC} or external devices. For proper device operation, the external decoupling capacitor of this pin should be 5µF ~ 10µF. For more detailed information, see Section 5.7.2.5, *Power-Supply Decoupling*. When disabled, this pin is in the high-impedance (Hi-Z) state.
LDOI	F14, F13, B12	S		LDO inputs. For proper device operation, LDOI must always be powered. The LDOI pins must be connected to the same power supply source with a voltage range of 1.8 V to 3.6 V. These pins supply power to the internal LDOs, the bandgap reference generator circuits, and serve as the I/O supply for some input pins.
$\overline{\text{DSP\_LDO\_EN}}$	D12	I	_ LDOI	DSP_LDO enable input. This signal is ***not*** intended to be dynamically switched. 0 = DSP_LDO is enabled. The internal POR monitors the DSP_LDOO pin voltage and generates the internal POWERGOOD signal. 1 = DSP_LDO is disabled. The internal POR voltage monitoring is also disabled. The internal POWERGOOD signal is forced high and the external reset signal on the $\overline{\text{RESET}}$ pin (D6) is the only source of the device reset. Note, the device's internal reset signal is generated as the logical AND of the $\overline{\text{RESET}}$ pin and the internal POWERGOOD signal.
USB_LDOO	F12	S		USB_LDO output. This output provides a regulated 1.3 V output and up to 25 mA of current (see the I_{SD} parameter in Section 5.3.2, *Electrical Characteristics*). For proper device operation, this pin must be connected to a 1 µF ~ 2 µF decoupling capacitor to V_{SS}. For more detailed information, see Section 5.7.2.5, *Power-Supply Decoupling*. This LDO is intended to supply power to the USB_V_{DD1P3}, USB_V_{DDA1P3} pins but not to CV_{DDRTC} or external devices. **Note:** The reset state of the register that enables and disables the USB_LDO is dependent on the setting of CLK_SEL pin at reset. If CLK_SEL is high, the USB_LDO is disabled at reset but can be enabled by software. If CLK_SEL is low, the USB LDO is enabled (USB_LDO_EN=1) at reset and cannot be disabled by software. (See Section 5.7.2.1.1.2.1 *LDO Control* for details.)
ANA_LDOO	A12	S		ANA_LDO output. This output provides a regulated 1.3 V output and up to 4 mA of current (see the I_{SD} parameter in Section 5.3.2, *Electrical Characteristics*). For proper device operation, this pin ***must*** be connected to an ~ 1.0 µF decoupling capacitor to V_{SS}. For more detailed information, see Section 5.7.2.5, *Power-Supply Decoupling*. This LDO is intended to supply power to the V_{DDA_ANA} pin but not to VDDA_PLL, CV_{DDRTC} or external devices.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-17. Regulators and Power Management Signal Descriptions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
BG_CAP	B13	A, O		Bandgap reference filter signal. For proper device operation, this pin needs to be bypassed with a 0.1 µF capacitor to analog ground (V_{SSA_ANA}). BG_CAP provides a settling time of 200 ms that must elapse before executing bootloader code. The settling time time is used by Timer0. This external capacitor provides filtering for stable reference voltages and currents generated by the bandgap circuit. The bandgap produces the references for use by the SAR and POR circuits.

4.2.17 Supply Voltage

Table 4-18. Supply Voltage Signal Descriptions

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
SUPPLY VOLTAGES				
CV_{DD}	F6	PWR		1.05-V Digital Core supply voltage (75 MHz) 1.3-V Digital Core supply voltage (175 MHz) 1.4-V Digital Core supply voltage (200 MHz)
	H8			
	J6			
	K10			
	L5			
DV_{DDIO}	F7	PWR		1.8-V, 2.75-V, or 3.3-V I/O power supply for non-EMIF and non-RTC I/Os DV_{DDIO} must always be powered for proper operation.
	K7			
	K12			
	N14			
	P3			
	P8			
DV_{DDEMIF}	A2	PWR		1.8-V, 2.75-V, or 3.3-V EMIF I/O power supply DV_{DDEMIF} must always be powered for proper operation. GP[26:21] are used for boot mode configuration.
	A5			
	E6			
	F5			
	G5			
	H5			
	H7			
	J5			
	P2			
CV_{DDRTC}	C8	PWR		1.05-V RTC digital core and RTC oscillator power supply. **Note:** The CV_{DDRTC} pin must always be powered by an external power source even though RTC is not used. None of the on-chip LDOs can power CV_{DDRTC}.
DV_{DDRTC}	F8	PWR		1.8-V, 2.75-V, or 3.3-V I/O power supply for peripheral pins. DV_{DDRTC} can be tied to ground (V_{SS}) when RTC_CLKOUT and WAKEUP pins are not used permanently. In this case, the WAKEUP pin must be configured as output by software. (See Table 5-1, *RTCPMGT Register Bit Descriptions*.)
V_{DDA_PLL}	C10	PWR	see Section 5.2, ROC	1.3-V Analog PLL power supply for the system clock generator. Care should be taken to prevent noise on this supply. Consider using a ferrite bead if the power supply for this pin is shared with digital logic. See the *Filtering Techniques* Application Report [literature number: SCAA048] for more information. This signal cannot be powered from the ANA_LDOO pin. It must be powered externally.
USB_V_{DDPLL}	G8	S	see Section 5.2, ROC	3.3 V USB Analog PLL power supply. Care should be taken to prevent noise on this supply. Consider using a ferrite bead if the power supply for this pin is shared with digital logic. See the *Filtering Techniques* Application Report [literature number: SCAA048] for more information. When the USB peripheral ***is not*** used, the USB_V_{DDPLL} signal should be connected to ground (V_{SS}).

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-18. Supply Voltage Signal Descriptions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
USB_V_{DD1P3}	J13	S	see Section 5.2, ROC	1.3-V digital core power supply for USB PHY. This signal must be powered on in the order listed in Section 5.7.2.2, *Power-Supply Sequencing*. When the USB peripheral ***is not*** used, the USB_V_{DD1P3} signal should be connected to ground (V_{SS}).
USB_V_{DDA1P3}	H10	S	see Section 5.2, ROC	Analog 1.3 V power supply for USB PHY. [For high-speed sensitive analog circuits] This signal must be powered on in the order listed in Section 5.7.2.2, *Power-Supply Sequencing*. When the USB peripheral ***is not*** used, the USB_V_{DDA1P3} signal should be connected to ground (V_{SS}).
USB_V_{DDA3P3}	H12	S	see Section 5.2, ROC	Analog 3.3 V power supply for USB PHY. This signal must be powered on in the order listed in Section 5.7.2.2, *Power-Supply Sequencing*. When the USB peripheral ***is not*** used, the USB_V_{DDA3P3} signal should be connected to ground (V_{SS}).
USB_V_{DDOSC}	G12	S	see Section 5.2, ROC	3.3-V power supply for USB oscillator. When the USB peripheral ***is not*** used, USB_V_{DDOSC} should be connected to ground (V_{SS}).
V_{DDA_ANA}	A10	PWR		1.3-V supply for power management and 10-bit SAR ADC This signal can be powered from the ANA_LDOO pin.

4.2.18 Ground

Table 4-19. Ground Signal Descriptions

SIGNAL NAME	NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
V_{SS}	A13	GND		Ground pins
	A14			
	D7			
	D11			
	E9			
	E11			
	E12			
	E13			
	E14			
	F9			
	F10			
	G6			
	G7			
	H6			
	J7			
	J8			
	J9			
	K8			
	K9			
	K11			
	K13			
V_{SSRTC}	C9	GND		Ground for RTC oscillator. When using a 32.768-kHz crystal, this pin is a local ground for the crystal and must not be connected to the board ground (See Figure 5-13 and Figure 5-16). When not using RTC and the crystal is not populated on the board, this pin is connected to the board ground.
V_{SSA_PLL}	D9	GND	see Section 5.2, ROC	Analog PLL ground for the system clock generator.
USB_V_{SSPLL}	G11	GND	see Section 5.2, ROC	USB Analog PLL ground.
USB_V_{SS1P3}	H13	GND	see Section 5.2, ROC	Digital core ground for USB PHY.
USB_V_{SSA1P3}	H9	GND	see Section 5.2, ROC	Analog ground for USB PHY [For high speed sensitive analog circuits].
USB_V_{SSA3P3}	H11	GND	see Section 5.2, ROC	Analog ground for USB PHY.
USB_V_{SSOSC}	F11	GND	see Section 5.2, ROC	Ground for USB oscillator.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-19. Ground Signal Descriptions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
USB_V_{SSREF}	G10	GND	see Section 5.2, ROC	Ground for reference current. This must be connected via a 10-kΩ ±1% resistor to USB_R1. When the USB peripheral ***is not*** used, the USB_V_{SSREF} signal should be connected directly to ground (V_{SS}).
V_{SSA_ANA}	B10 B14	GND		Analog ground pins for power management (POR and Bandgap circuits) and 10-bit SAR ADC

4.3 Pin Multiplexing

Extensive pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. The external bus selection register (EBSR) controls all the pin multiplexing functions on the device.

This section discusses how to program the external bus selection register (EBSR) to select the desired peripheral functions and pin muxing. See the individual subsections for muxing details for a specific muxed pin. After changing any of the pin mux control registers, it will be necessary to reset the peripherals that are affected.

4.3.1 UHPI, SPI, UART, I2S2, I2S3, and GP[31:27, 20:12] Pin Multiplexing [EBSR.PPMODE Bits]

The UHPI, SPI, UART, I2S2, I2S3, and GPIO signal muxing is determined by the value of the PPMODE bit fields in the External Bus Selection Register (EBSR) register. For more details on the actual pin functions, see Table 4-20.

Table 4-20. UHPI, SPI, UART, I2S2, I2S3, and GP[31:27, 20:12] Pin Multiplexing

PULLUP and PULLDOWN CONTROL REGISTER BIT	PIN NUMBER	EBSR PPMODE BITS						
		MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6
		000	001 (Reset Default)	010	011	100	101	110
PUDINHIBR7 (0x1C50) Bit 12	N3	UHPI_HINT	SPI_CLK	Reserved	Reserved	Reserved	Reserved	SPI_CLK
PUDINHIBR3 (0x1C19) Bit 0	P6	UHPI_HD[0]	SPI_RX	Reserved	Reserved	Reserved	Reserved	SPI_RX
PUDINHIBR3 (0x1C19) Bit 1	N6	UHPI_HD[1]	SPI_TX	Reserved	Reserved	Reserved	Reserved	SPI_TX
PUDINHIBR3 (0x1C19) Bit 2	P7	UHPI_HD[2]	GP[12]	Reserved	Reserved	Reserved	Reserved	GP[12]
PUDINHIBR3 (0x1C19) Bit 3	N7	UHPI_HD[3]	GP[13]	Reserved	Reserved	Reserved	Reserved	GP[13]
PUDINHIBR3 (0x1C19) Bit 4	N8	UHPI_HD[4]	GP[14]	Reserved	Reserved	Reserved	Reserved	GP[14]
PUDINHIBR3 (0x1C19) Bit 5	P9	UHPI_HD[5]	GP[15]	Reserved	Reserved	Reserved	Reserved	GP[15]
PUDINHIBR3 (0x1C19) Bit 6	N9	UHPI_HD[6]	GP[16]	Reserved	Reserved	Reserved	Reserved	GP[16]
PUDINHIBR3 (0x1C19) Bit 7	P10	UHPI_HD[7]	GP[17]	Reserved	Reserved	Reserved	Reserved	GP[17]
PUDINHIBR3 (0x1C19) Bit 8	N10	UHPI_HD[8]	I2S2_CLK	GP[18]	SPI_CLK	I2S2_CLK	SPI_CLK	I2S2_CLK
PUDINHIBR3 (0x1C19) Bit 9	P11	UHPI_HD[9]	I2S2_FS	GP[19]	SPI_CS0	I2S2_FS	SPI_CS0	I2S2_FS
PUDINHIBR3 (0x1C19) Bit 10	N11	UHPI_HD[10]	I2S2_RX	GP[20]	SPI_RX	I2S2_RX	SPI_RX	I2S2_RX
PUDINHIBR3 (0x1C19) Bit 11	P12	UHPI_HD[11]	I2S2_DX	GP[27]	SPI_TX	I2S2_DX	SPI_TX	I2S2_DX
PUDINHIBR3 (0x1C19) Bit 12	N12	UHPI_HD[12]	UART_RTS	GP[28]	I2S3_CLK	UART_RTS	UART_RTS	I2S3_CLK
PUDINHIBR3 (0x1C19) Bit 13	P13	UHPI_HD[13]	UART_CTS	GP[29]	I2S3_FS	UART_CTS	UART_CTS	I2S3_FS
PUDINHIBR3 (0x1C19) Bit 14	N13	UHPI_HD[14]	UART_RXD	GP[30]	I2S3_RX	UART_RXD	UART_RXD	I2S3_RX
PUDINHIBR3 (0x1C19) Bit 15	P14	UHPI_HD[15]	UART_TXD	GP[31]	I2S3_DX	UART_TXD	UART_TXD	I2S3_DX
PUDINHIBR7 (0x1C50) Bit 8	P4	UHPI_HCNTL0	SPI_CS0	Reserved	Reserved	Reserved	Reserved	SPI_CS0
PUDINHIBR7 (0x1C50) Bit 9	N4	UHPI_HCNTL1	SPI_CS1	Reserved	Reserved	Reserved	Reserved	SPI_CS1
PUDINHIBR7 (0x1C50) Bit 10	P5	UHPI_HR_NW	SPI_CS2	Reserved	Reserved	Reserved	Reserved	SPI_CS2
PUDINHIBR7 (0x1C50) Bit 11	N5	UHPI_HRDY	SPI_CS3	Reserved	Reserved	Reserved	Reserved	SPI_CS3
PUDINHIBR6 (0x1C4F) Bit 7	B5	UHPI_HBE0	EM_DQM0	EM_DQM0	EM_DQM0	EM_DQM0	EM_DQM0	EM_D1M0
PUDINHIBR6 (0x1C4F) Bit 8	P1	UHPI_HBE1	EM_DQM1	EM_DQM1	EM_DQM1	EM_DQM1	EM_DQM1	EM_DQM1
PUDINHIBR7 (0x1C50) Bit 3	A6	UHPI_HAS	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$	$\overline{\text{EM\_SDRAS}}$
PUDINHIBR7 (0x1C50) Bit 2	B4	UHPI_HCS	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$	$\overline{\text{EM\_SDCAS}}$
PUDINHIBR7 (0x1C50) Bit 4	B3	UHPI_HDS1	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$	$\overline{\text{EM\_CS0}}$
PUDINHIBR7 (0x1C50) Bit 5	A4	UHPI_HDS2	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$	$\overline{\text{EM\_CS1}}$
PUDINHIBR7 (0x1C50) Bit 1	N2	UHPI_HHWIL	EM_SDCKE	EM_SDCKE	EM_SDCKE	EM_SDCKE	EM_SDCKE	EM_SDCKE

4.3.2 MMC1, McSPI, and GP[11:6] Pin Multiplexing [EBSR.SP1MODE Bits]

The MMC1, McSPI, and GPIO signal muxing is determined by the value of the SP1MODE bit fields in the External Bus Selection Register (EBSR) register. For more details on the actual pin functions, see Table 4-21.

Table 4-21. MMC1, McSPI, and GP[11:6] Pin Multiplexing

PUDINHIBR1 REGISTER BIT(1)	PIN NUMBER	EBSR SP1MODE BITS		
		MODE 0	MODE 1	MODE 2
		00 (Reset Default)	01	10
Bit 8	M13	MMC1_CLK	McSPI_CLK	GP[6]
Bit 9	L14	MMC1_CMD	McSPI_CS0	GP[7]
Bit 10	M14	MMC1_D0	McSPI_SIMO	GP[8]
Bit 11	M12	MMC1_D1	McSPI_SOMI	GP[9]
Bit 12	K14	MMC1_D2	McSPI_CS1	GP[10]
Bit 13	L13	MMC1_D3	McSPI_CS2	GP[11]

(1) The pin names with PUDINHIBR1 (1C17h) register bit field references can have the pulldown register enabled or disabled via this register. Pin 0 on serial port 1 corresponds to bit 8, pin 1 to bit 9, and so on up to pin 5 which corresponds to bit 13.

4.3.3 MMC0, I2S0, McBSP, and GP[5:0] Pin Multiplexing [EBSR.SP0MODE Bits]

The MMC0, I2S0, McBSP, and GPIO signal muxing is determined by the value of the SP0MODE bit fields in the External Bus Selection Register (EBSR) register. For more details on the actual pin functions, see Table 4-22.

Table 4-22. MMC0, I2S0, McBSP, and GP[5:0] Pin Multiplexing

PUDINHIBR1 REGISTER BIT(1)	PIN NUMBER	EBSR SP0MODE BITS			
		MODE 0	MODE 1	MODE 2	MODE 3
		00 (Reset Default)	01	10	11
Bit 0	L10	MMC0_CLK	I2S0_CLK	GP[0]	McBSP_CLKX
Bit 1	M11	MMC0_CMD	I2S0_FS	GP[1]	McBSP_FSX
Bit 2	L9	MMC0_D0	I2S0_DX	GP[2]	McBSP_DX
Bit 3	M10	MMC0_D1	I2S0_RX	GP[3]	McBSP_DR
Bit 4	L12	MMC0_D2	GP[4]	GP[4]	McBSP_FSR
Bit 5	L11	MMC0_D3	GP[5]	GP[5]	McBSP_CLKR_CLKS(2)

(1) The pin names with PUDINHIBR1 (1C17h) register bit field references can have the pulldown register enabled or disabled via this register. Pin 0 on serial port 0 corresponds to bit 0, pin 1 to bit 1, and so on up to pin 5 which corresponds to bit 5.
(2) Bit 15 of the EBSR register determines this port to be McBSP_CLKR or McBSP_CLKS.

4.3.4 EMIF EM_A[20:15] and GP[26:21] Pin Multiplexing [EBSR.Axx_MODE bits]

The EMIF Address and GPIO signal muxing is determined by the value of the A20_MODE, A19_MODE, A18_MODE, A17_MODE, A16_MODE, and A15_MODE bit fields in the External Bus Selection Register (EBSR) register. For more details on the actual pin functions, see Table 4-23.

Table 4-23. EM_A[20:16] and GP[26:21] Pin Multiplexing

PUDINHIBR2 REGISTER BIT(1)	PIN NUMBER	Axx_MODE BIT	
		0	1
Bit 0	N1	EM_A[15]	GP[21]
Bit 1	E2	EM_A[16]	GP[22]
Bit 2	F2	EM_A[17]	GP[23]
Bit 3	G2	EM_A[18]	GP[24]
Bit 4	G4	EM_A[19]	GP[25]
Bit 5	J3	EM_A[20]	GP[26]

(1) The pin names with PUDINHIBR2 (1C18h) register bit field references can have the pulldown register enabled or disabled via this register.

4.4 Connections for Unused Signals

Table 4-24 lists the signals that are reserved or are not connected on this device.

Table 4-24. Reserved and No Connects Signal Descriptions

SIGNAL NAME	SIGNAL NO.	TYPE(1) (2)	OTHER(3) (4)	DESCRIPTION
Reserved				
RSV0	C12	I	– LDOI	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.
RSV1	J10	PWR		Reserved. For proper device operation, this pin must be tied directly to CV_{DD}.
RSV2	J11	PWR		Reserved. For proper device operation, this pin must be tied directly to CV_{DD}.
RSV3	D14	I	– LDOI	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.
RSV4	C14	I	– LDOI	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.
RSV5	C13	I	– LDOI	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.
RSV16	D13	I	– LDOI	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

5 Specifications

For the device maximum operating frequency, see Section 7.1.2, *Device Nomenclature*.

5.1 Absolute Maximum Ratings

Over Operating Case Temperature Range (Unless Otherwise Noted)(1)

Supply voltage ranges:	Digital Core (CV_{DD}, CV_{DDRTC}, USB_V_{DD1P3})(2)	–0.5 V to 1.7 V
	I/O, 1.8 V, 2.75 V, 3.3 V (DV_{DDIO}, DV_{DDEMIF}, DV_{DDRTC}) 3.3V USB supplies USB PHY (USB_V_{DDOSC}, USB_V_{DDPLL}, USB_V_{DDA3P3})(2)	–0.5 V to 4.2 V
	LDOI	–0.5 V to 4.2 V
	Analog, 1.3 V (V_{DDA_PLL}, USB_V_{DDA1P3}, V_{DDA_ANA})(2)	–0.5 V to 1.7 V
Input and Output voltage ranges:	V_I I/O, All pins with DV_{DDIO} or DV_{DDEMIF} or USB_V_{DDOSC} or USB_V_{DDPLL} or USB_V_{DDA3P3} as supply source	–0.5 V to 4.2 V
	V_O I/O, All pins with DV_{DDIO} or DV_{DDEMIF} or USB_V_{DDOSC} or USB_V_{DDPLL}or USB_V_{DDA3P3} as supply source	–0.5 V to 4.2 V
	RTC_XI and RTC_XO	–0.5 V to 1.7 V
	V_I and V_O, GPAIN[0]	–0.5 V to 4.2 V
	V_I and V_O, GPAIN[3:1]	–0.5 V to 1.7 V
	V_O, BG_CAP	–0.5 V to 1.7 V
	ANA_LDOO, DSP_LDOO, and USB_LDOO	–0.5 V to 1.7 V
	USB_V_{BUS} Input	0 V to 5.5 V
Operating case temperature ranges, T_c:	Commercial Temperature (default)	-10°C to 70°C
	Industrial Temperature	-40°C to 85°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}.

5.2 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
Core Supplies	CV_{DD}	Supply voltage, Digital Core Slew rate < 200 µs for full swing	75 MHz	0.998	1.05	1.15	V
			175 MHz	1.24	1.3	1.43	V
			200 MHz	1.33	1.4	1.47	V
	CV_{DDRTC}	Supply voltage, RTC and RTC OSC	32.768 kHz	0.998		CV_{DD}	V
	USB_V_{DD1P3}	Supply voltage, Digital USB		1.24	1.3	1.43	V
	USB_V_{DDA1P3}	Supply voltage, 1.3 V Analog USB		1.24	1.3	1.43	V
	V_{DDA_ANA}	Supply voltage, 1.3 V SAR and Pwr Mgmt		1.24	1.3	1.43	V
	V_{DDA_PLL}	Supply voltage, System PLL		1.24	1.3	1.43	V
	USB_V_{DDPLL}	Supply voltage, 3.3 V USB PLL		2.97	3.3	3.63	V
I/O Supplies	DV_{DDIO} DV_{DDEMIF} DV_{DDRTC}	Supply voltage, I/O, 3.3 V		2.97	3.3	3.63	V
		Supply voltage, I/O, 2.75 V		2.48	2.75	3.02	V
		Supply voltage, I/O, 1.8 V		1.65	1.8	1.98	V
	USB_V_{DDOSC}	Supply voltage, I/O, 3.3 V USB OSC		2.97	3.3	3.63	V
	USB_V_{DDA3P3}	Supply voltage, I/O, 3.3 V Analog USB PHY		2.97	3.3	3.63	V
	LDOI	Supply voltage, Analog Pwr Mgmt and LDO Inputs		1.8		3.6	V
GND	V_{SS}	Supply ground, Digital I/O		0	0	0	V
	V_{SSRTC}	Supply ground, RTC					
	USB_V_{SSOSC}	Supply ground, USB OSC					
	USB_V_{SSPLL}	Supply ground, USB PLL					
	USB_V_{SSA3P3}	Supply ground, 3.3 V Analog USB PHY					
	USB_V_{SSA1P3}	Supply ground, USB 1.3 V Analog USB PHY					
	USB_V_{SSREF}	Supply ground, USB Reference Current					
	V_{SSA_PLL}	Supply ground, System PLL					
	USB_V_{SS1P3}	Supply ground, 1.3 V Digital USB PHY					
	V_{SSA_ANA}	Supply ground, SAR and Pwr Mgmt					
V_{IH} (1)		High-level input voltage, 3.3, 2.75, 1.8 V I/O (except GPAIN[3:0] pins) (2)		0.7 * DV_{DD}		DV_{DD} + 0.3	V
V_{IL} (1)		Low-level input voltage, 3.3, 2.75, 1.8 V I/O (except GPAIN[3:0] pins) (2)		-0.3		0.3 * DV_{DD}	V
V_{IN}		Input voltage, GPAIN0 pin (3)		-0.3		3.6	V
		Input voltage, GPAIN[3:1] pins		-0.3		V_{DDA_ANA} + 0.3	V
T_c		Operating case temperature	Commercial (default)	-10		70	°C
			Industrial	-40		85	°C
F_{SYSCLK}		DSP Operating Frequency (SYSCLK)	1.05 V	0		75	MHz
			1.3 V	0		175	MHz
			1.4 V	0		200	MHz

(1) DV_{DD} refers to the pin I/O supply voltage. To determine the I/O supply voltage for each pin, see Section 4.2, *Signal Descriptions*.
(2) The I2C pin SDA and SCL do not feature fail-safe I/O buffers. These pin could potentially draw current when the DV_{DDIO} is powered down. Due to the fact that different voltage devices can be connected to I2C bus and the I2C inputs are LVCMOS, the level of logic 0 (low) and logic 1 (high) are not fixed and depend on DV_{DDIO}.
(3) The GNDON bit in the SARPINCTRL register should be set to "1" before SAR channels 0, 1, or 2 are enabled via the CHSEL bit in the SARCTRL register, when V_{IN} greater than V_{DDA_ANA}.

5.3 Electrical Characteristics

5.3.1 Power Consumption

NOTE

Power consumption on this device depends on several operating parameters such as operating voltage, operating frequency, and temperature. Power consumption also varies by end applications that determine the overall processor, CPU, and peripheral activity. For more specific power consumption details, see *Estimating Power Consumption on the TMS320C5517 Digital Signal Processor* [literature number SPRABV3]. This document includes a spreadsheet for estimating power based on parameters that closely resemble the end application to generate a realistic estimate of power consumption on this device based on use-case and operating conditions.

5.3.2 Electrical Characteristics

Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
V_{OH}	Full speed: USB_DN and USB_DP (2)		2.8		USB_V_{DDA3P3}	V
	High speed: USB_DN and USB_DP (2)		360		440	mV
	High-level output voltage, 3.3, 2.75, 1.8 V I/O (except GPAIN[3:0] pins)	IO = I_{OH}	0.8 * DV_{DD}			V
	High-level output voltage, GPAIN[3:1] pins	IO = I_{OH}	0.8 * V_{DDA_ANA}			V
V_{OL}	Full speed: USB_DN and USB_DP (2)		0.0		0.3	V
	High speed: USB_DN and USB_DP (2)		–10		10	mV
	Low-level output voltage, 3.3, 2.75, 1.8V I/O (except I2C and GPAIN[3:0] pins)	IO = I_{OL}			0.2 * DV_{DD}	V
	Low-level output voltage, I2C pins (3)	V_{DD} > 2 V, I_{OL} = 3 mA	0		0.4	V
	Low-level output voltage, GPAIN[3:0] pins	IO = I_{OL}			0.2 * V_{DDA_ANA}	V
V_{HYS}	Input hysteresis (4)	DV_{DD} = 3.3 V		162		mV
		DV_{DD} = 1.8 V		122		mV
V_{LDO}	USB_LDOO voltage		1.24	1.3	1.43	V
	ANA_LDOO voltage		1.24	1.3	1.43	V
	DSP_LDOO voltage	DSP_LDO_V bit in the LDOCNTL register = 1	1.24	1.3	1.43	V
		DSP_LDO_V bit in the LDOCNTL register = 0	0.998	1.05	1.15	V
I_{SD}	DSP_LDO shutdown current (5)	LDOI = V_{MIN}	250			mA
	ANA_LDO shutdown current (5)	LDOI = V_{MIN}	4			mA
	USB_LDO shutdown current (5)	LDOI = V_{MIN}	25			mA
I_{ILPU} (6) (7)	Input current [DC] (except WAKEUP, I2C, and GPAIN[3:0] pins)	Input only pin, internal pulldown or pullup disabled	–5		+5	µA
		DV_{DD} = 3.3 V with internal pullup enabled (8)		–59 to –161		µA
		DV_{DD} = 1.8 V with internal pullup enabled (8)		–14 to –44		µA

(1) For test conditions shown as MIN, MAX, or TYP, use the appropriate value specified in the recommended operating conditions table.
(2) The USB I/Os adhere to the Universal Bus Specification Revision 2.0 (USB2.0 spec).
(3) V_{DD} is the voltage to which the I2C bus pullup resistors are connected.
(4) Applies to all input pins except WAKEUP, I2C pins, GPAIN[3:0], RTC_XI, and USB_MXI.
(5) I_{SD} is the amount of current the LDO is ensured to deliver before shutting down to protect itself.
(6) I_I applies to input-only pins and bidirectional pins. For input-only pins, I_I indicates the input leakage current. For bidirectional pins, I_I indicates the input leakage current and off-state (Hi-Z) output leakage current.
(7) When CV_{DD} power is "ON", the pin bus-holders are disabled. For more detailed information, see Section 5.7.2.3, *Digital I/O Behavior When Core Power (CV_{DD}) is Down*.
(8) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.

Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS (1)		MIN	TYP	MAX	UNIT
I_{IHPD} (6)(7)	Input current [DC] (except WAKEUP, I2C, and GPAIN[3:0] pins)	Input only pin, internal pulldown or pullup disabled		–5		+5	µA
		DV_{DD} = 3.3 V with internal pulldown enabled (8)			52 to 158		µA
		DV_{DD} = 1.8 V with internal pulldown enabled (8)			11 to 35		µA
I_{IH}/ I_{IL} (7)	Input current [DC], ALL pins	V_I = V_{SS} to DV_{DD} with internal pullups and pulldowns disabled.		–5		+5	µA
I_{OH} (7)	High-level output current [DC]	All Pins (except USB, EMIF, CLKOUT, and GPAIN[3:0] pins)		–4			mA
		EMIF pins	DV_{DD} = 3.3 V	–6			mA
			DV_{DD} = 1.8 V	–5			mA
		CLKOUT pin	DV_{DD} = 3.3 V	–6			mA
			DV_{DD} = 1.8 V	–4			mA
		GPAIN[3:1] pins (GPAIN0 is open-drain and cannot drive high)	DV_{DD} = V_{DDA_ANA} = 1.3 V, External Regulator (9)	–4			mA
			DV_{DD} = V_{DDA_ANA} = 1.3 V, Internal Regulator (9)	–100			µA
I_{OL} (7)	Low-level output current [DC]	All Pins (except USB, EMIF, CLKOUT, and GPAIN[3:0] pins)				+4	mA
		EMIF pins	DV_{DD} = 3.3 V			+6	mA
			DV_{DD} = 1.8 V			+5	mA
		CLKOUT pin	DV_{DD} = 3.3 V			+6	mA
			DV_{DD} = 1.8 V			+4	mA
		GPAIN[3:0]	DV_{DD} = V_{DDA_ANA} = 1.3 V, external regulator			+4	mA
			DV_{DD} = V_{DDA_ANA} = 1.3 V, internal regulator (9)			+4	mA
I_{OZ} (10)	I/O Off-state output current	All Pins (except USB and GPAIN[3:0])		–10		+10	µA
		GPAIN[3:0] pins		–10		+10	µA
I_{OLBH} (11)	Bus Holder pull low current when CV_{DD} is powered "OFF"	Supply voltage, I/O, 3.3 V				2.2	mA
		Supply voltage, I/O, 2.75 V				1.6	mA
		Supply voltage, I/O, 1.8 V				0.72	mA
I_{OHBH} (11)	Bus Holder pull high current when CV_{DD} is powered "OFF"	Supply voltage, I/O, 3.3 V		–1.3			mA
		Supply voltage, I/O, 2.75 V		–0.97			mA
		Supply voltage, I/O, 1.8 V		–0.46			mA
I	Analog PLL (V_{DDA_PLL}) supply current	V_{DDA_PLL} = 1.3 V Room Temp, Phase detector = 12 MHz, VCO = 125 MHz			0.93		mA
		V_{DDA_PLL} = 1.3 V Room Temp, Phase detector = 12 MHz, VCO = 175 MHz			1.23		
		V_{DDA_PLL} = 1.3 V Room Temp, Phase detector = 12 MHz, VCO = 200 MHz			1.54		
	SAR Analog (V_{DDA_ANA}) supply current	V_{DDA_ANA} = 1.3 V, SAR clock = 2 MHz, Temp (70 °C)				1	mA
C_I	Input capacitance					4	pF
C_o	Output capacitance					4	pF

(9) When the ANA_LDO supplies V_{DDA_ANA}, it is not recommended to use the GPAIN[3:1] signals for general-purpose outputs (driving high). The I_{SD} parameter of the ANA_LDO is too low to drive any realistic load on the GPAIN[3:1] pins while also supplying the PLL through V_{DDA_PLL} and the SAR through V_{DDA_ANA}.
(10) I_{OZ} applies to output-only pins, indicating off-state (Hi-Z) output leakage current.
(11) This parameter specifies the maximum strength of the Bus Holder and is needed to calculate the minimum strength of external pullups and pulldowns.

5.4 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range (default)	–65	150	ºC
Electrostatic Discharge (ESD) Stress Voltage(1)	Human Body Model (HBM)(2)	0	>1000	V
	Charged Device Model (CDM)(3)	0	>250	V

(1) ESD to measure device sensitivity and immunity to damage caused by electrostatic discharges into the device.
(2) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001-2010. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500 V HBM is possible if the necessary precautions are taken. Pins listed as 1000 V may actually have higher performance.
(3) Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 250 V may actually have higher performance.

Section 5.5 shows the thermal resistance characteristics for the PBGA–ZCH mechanical package.

5.5 Thermal Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.				°C/W(1)	AIR FLOW (m/s)(2)
1	RT_{JC}	Junction-to-case	1S0P	6.74	N/A
2	RT_{JB}	Junction-to-board	1S0P	14.5	N/A
			2S2P	13.8	
3	RT_{JA}	Junction-to-free air	1S0P	57.0	0.00
			2S2P	33.4	
4	RT_{JMA}	Junction-to-moving air			0.50
5					1.00
6					2.00
7					3.00
8	Psi_{JT}	Junction-to-package top		0.09	0.00
9					0.50
10					1.00
11					2.00
12					3.00
13	Psi_{JB}	Junction-to-board		13.7	0.00
14					0.50
15					1.00
16					2.00
17					3.00

(1) These measurements were conducted in a JEDEC defined 2S2P system and will change based on environment as well as application. For more information, see these EIA/JEDEC standards – EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)* and JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
(2) m/s = meters per second

5.6 Power-On Hours

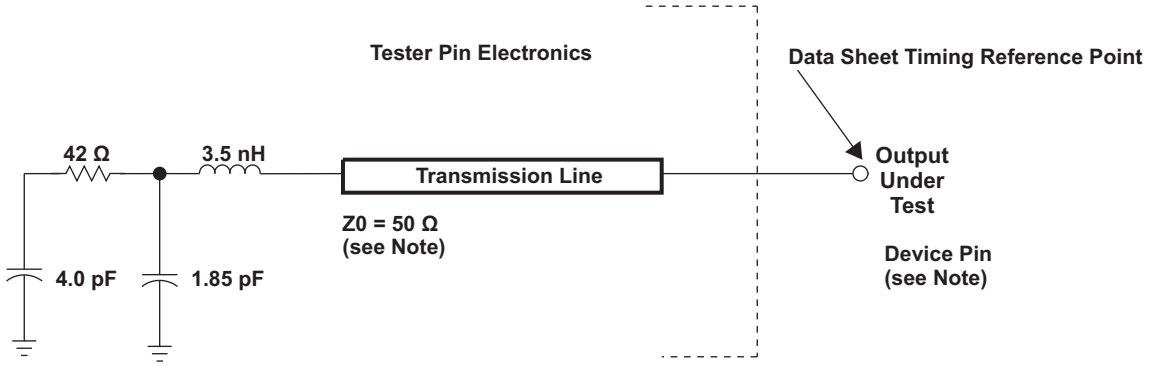
Over Operating Case Temperature Range (Unless Otherwise Noted)

Device Operating Life Power-On Hours (POH)(1)	DSP Operating Frequency (SYSCLK): ≤200 MHz	Commercial	-10 to 70°C	100,000 POH(2)
		Industrial	-40 to 85°C	

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) POH = 100,000 when the Maximum Core Supply Voltages are limited to 105% of the Nominal Core Supply Voltages (For details on the Core Supplies, see Section 5.2, *Recommended Operating Conditions*).

5.7 Timing and Switching Characteristics

5.7.1 Parameter Information



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 5-1. 3.3-V Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

5.7.1.1 1.8-V, 2.75-V, and 3.3-V Signal Transition Levels

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

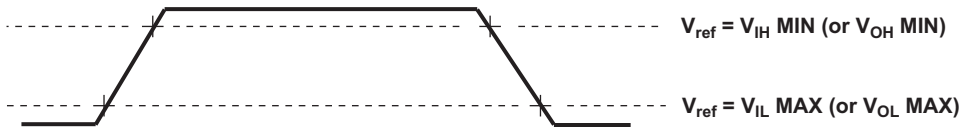


Figure 5-2. Rise and Fall Transition Time Voltage Reference Levels

5.7.1.2 3.3-V Signal Transition Rates

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

5.7.1.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do *not* include delays by board routing. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing and decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report [literature number SPRA839]. If needed, external logic hardware such as buffers may be used to compensate any timing differences.

5.7.2 Power Supplies

5.7.2.1 Power Considerations

The device provides several means of managing power consumption.

To minimize power consumption, the device divides its circuits into nine main isolated supply domains:

- LDOI (LDOs and Bandgap Power Supply)
- Analog POR, SAR, and PLL (V_{DDA_ANA} and V_{DDA_PLL})
- RTC Core (CV_{DDRTC}) — **Note:** CV_{DDRTC} must always be powered by an external power source. None of the on-chip LDOs can be used to power CV_{DDRTC}.
- Digital Core (CV_{DD})
- USB Core (USB_V_{DD1P3} and USB_V_{DDA1P3})
- USB PHY and USB PLL (USB_V_{DDOSC}, USB_V_{DDA3P3}, and USB_V_{DDPLL})
- EMIF I/O (DV_{DDEMIF})
- RTC I/O (DV_{DDRTC})
- Rest of the I/O (DV_{DDIO})

5.7.2.1.1 LDO Configuration

The device includes three Low-Dropout Regulators (LDOs) which can be used to regulate the power supplies of the SAR ADC and Power Management (ANA_LDO), Digital Core (DSP_LDO), and USB Core (USB_LDO).

These LDOs are controlled by a combination of pin configuration and register settings. For more detailed information see the following sections.

5.7.2.1.1.1 LDO Inputs

The LDOI pins (B12, F13, F14) provide power to the internal Analog LDO, DSP LDO, USB LDO, the bandgap reference generator, and some I/O input pins, and can range from 1.8 V to 3.6 V. The bandgap provides accurate voltage and current references to the POR, LDOs, PLL, and SAR; therefore, for proper device operation, power **must** always be applied to the LDOI pins even if the LDO outputs are ***not*** used.

5.7.2.1.1.2 LDO Outputs

The ANA_LDOO pin (A12) is the output of the internal ANA_LDO and can provide regulated 1.3 V power of up to 4 mA. The ANA_LDOO pin is intended to be connected, on the board, to the V_{DDA_ANA} pin to provide a regulated 1.3 V to the 10-bit SAR ADC and Power Management Circuits. V_{DDA_ANA} may be powered by this LDO output, which is recommended, to take advantage of the device's power management techniques, or by an external power supply. The ANA_LDO cannot be disabled individually (see Section 5.7.2.1.1.2.1, *LDO Control*).

The DSP_LDOO pin (E10) is the output of the internal DSP_LDO and provides software-selectable regulated 1.3 V or regulated 1.05 V power of up to 250 mA. The DSP_LDOO pin is intended to be connected, on the board, to the CV_{DD} pins. In this configuration, the DSP_LDO_EN pin should be tied to the board V_{SS}, thus enabling the DSP_LDO.

Optionally, the CV_{DD} pins may be powered by an external power supply. In this configuration the DSP_LDO_EN pin should be tied (high) to LDOI, disabling DSP_LDO.

The DSP_LDO_EN also affects how reset is generated to the chip (for more details, see the DSP_LDO_EN pin description in Table 4-17, *Regulators and Power Management Signal Descriptions*). When the DSP_LDO is disabled, its output pin is in a high-impedance state.

The LDOs cannot supply power to CV_{DDRTC}, which requires an external power source because CV_{DDRTC} must always be on for proper operation.

NOTE

DSP_LDO can only provide a regulated 1.05 V or 1.3 V. When the DSP Core (CV_{DD}) requires 1.4 V, an external supply is required to supply 1.4 V to the DSP Core (CV_{DD}) and the $\overline{\text{DSP\_LDO\_EN}}$ pin should be tied to LDOI.

The USB_LDOO pin (F12) is the output of the internal USB_LDO and provides regulated 1.3 V, software-switchable (on and off) power of up to 25 mA. The USB_LDOO pin is intended to be connected, on the board, to the USB_V_{DD1P3} and USB_V_{DDA1P3} pins to provide power to portions of the USB. Optionally, the USB_V_{DD1P3} and USB_V_{DDA1P3} may be powered by an external power supply and the USB_LDO can be left disabled. When the USB_LDO is disabled, its output pin is in a high-impedance state.

5.7.2.1.1.2.1 LDO Control

All three LDOs can be simultaneously disabled via software by writing to either the BG_PD bit or the LDO_PD bit in the RTCPMGT register (see Figure 5-3). When the LDOs are disabled via this mechanism, the only way to re-enable them is by cycling power to the CV_{DDRTC} pin.

ANA_LDO: The ANA_LDO is only disabled by the BG_PD and the LDO_PD mechanism described above. Otherwise, it is always enabled.

DSP_LDO: The DSP_LDO can be statically disabled by the $\overline{\text{DSP\_LDO\_EN}}$ pin as described in Section 5.7.2.1.1.2, *LDO Outputs*. The DSP_LDO can also be dynamically enabled and disabled via the BG_PD and the LDO_PD mechanism described above. The DSP_LDO can change its output voltage dynamically by software via the DSP_LDO_V bit in the LDOCNTL register (see Figure 5-4). The DSP_LDO output voltage is set to 1.3 V at reset.

USB_LDO: The reset state of the USB_LDO is dependent on the setting of CLK_SEL pin. If CLK_SEL is high, the USB_LDO is disabled but can be independently and dynamically enabled or disabled by software via the USB_LDO_EN bit in the LDOCNTL register (see Figure 5-4). If CLK_SEL is low, the USB LDO is enabled at reset and can never be disabled. This is to ensure the USB oscillator has power when it is the source of the system clock.

Table 5-3 shows the ON and OFF control of each LDO and its register control bit configurations.

Figure 5-3. RTC Power Management Register (RTCPMGT) [1930h]

15	14	13	12	11	10	9	8
Reserved							
R-0							
7	6	5	4	3	2	1	0
Reserved			WU_DOUT	WU_DIR	BG_PD	LDO_PD	RTCCLKOUTEN
			R/W-1	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-1. RTCPMGT Register Bit Descriptions

Bit	Name	Description
15:5	Reserved	Reserved. Read-only, writes have no effect.
4	WU_DOUT	Wakeup output, active low, open-drain. 0 = WAKEUP pin driven low. 1 = WAKEUP pin is in high-impedance (Hi-Z).
3	WU_DIR	Wakeup pin direction control. 0 = WAKEUP pin configured as a input. 1 = WAKEUP pin configured as a output. Note: When the WAKEUP pin is configured as an input, it is active high. When the WAKEUP pin is configured as an output, is an open-drain that is active low and should be externally pulled-up via a 10-kΩ resistor to DV_{DDRTC}. WU_DIR must be configured as an input to allow the WAKEUP pin to wake the device up from idle modes.

Table 5-1. RTCPMGT Register Bit Descriptions (continued)

Bit	Name	Description
2	BG_PD	Bandgap, on-chip LDOs, and the analog POR power down bit. This bit shuts down the on-chip LDOs (ANA_LDO, DSP_LDO, and USB_LDO), the Analog POR, and Bandgap reference. BG_PD and LDO_PD are only intended to be used when the internal LDOs supply power to the chip. If the internal LDOs are bypassed and not used then the BG_PD and LDO_PD power-down mechanisms should not be used. After this bit is asserted, the on-chip LDOs, Analog POR, and the Bandgap reference can be re-enabled by the WAKEUP pin (high) or the RTC alarm interrupt. The Bandgap circuit will take about 100 msec to charge the external 0.1 uF capacitor via the internal 326-kΩ resistor. 0 = On-chip LDOs, Analog POR, and Bandgap reference are enabled. 1 = On-chip LDOs, Analog POR, and Bandgap reference are disabled (shutdown).
1	LDO_PD	On-chip LDOs and Analog POR power down bit. This bit shuts down the on-chip LDOs (ANA_LDO, DSP_LDO, and USB_LDO) and the Analog POR. BG_PD and LDO_PD are only intended to be used when the internal LDOs supply power to the chip. If the internal LDOs are bypassed and not used then the BG_PD and LDO_PD power-down mechanisms should not be used. After this bit is asserted, the on-chip LDOs and Analog POR can be re-enabled by the WAKEUP pin (high) or the RTC alarm interrupt. This bit keeps the Bandgap reference turned on to allow a faster wake-up time with the expense power consumption of the Bandgap reference. 0 = On-chip LDOs and Analog POR are enabled. 1 = On-chip LDOs and Analog POR are disabled (shutdown).
0	RTCCLKOUTEN	Clockout output enable bit. 0 = Clock output disabled. 1 = Clock output enabled.

Figure 5-4. LDO Control Register (LDOCNTL) [7004h]

15	14	13	12	11	10	9	8
Reserved							
R-0							
7	6	5	4	3	2	1	0
Reserved						DSP_LDO_V	USB_LDO_EN
R-0						R/W-0	R/W-CLK_SEL

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-2. LDOCNTL Register Bit Descriptions

Bit	Name	Description
15:2	Reserved	Reserved. Read-only, writes have no effect.
1	DSP_LDO_V	DSP_LDO voltage select bit. 0 = DSP_LDOO is regulated to 1.3 V. 1 = DSP_LDOO is regulated to 1.05 V.
0	USB_LDO_EN	USB_LDO enable bit. The reset state of this bit is dependent on the setting of CLK_SEL pin at reset. If CLK_SEL is high, the USB_LDO is disabled (USB_LEO_EN = 0). If CLK_SEL is low, the USB LDO is enabled (USB_LDO_EN=1). 0 = USB_LDO output is disabled. USB_LDOO pin is placed in high-impedance (Hi-Z) state. 1 = USB_LDO output is enabled. USB_LDOO is regulated to 1.3 V. **Note:** When CLK_SEL = 0, this bit will not be able to be set to 0 and the USB_LDO will stay enabled.

Table 5-3. LDO Controls Matrix

RTCPMGT Register (0x1930)		LDOCNTL Register (0x7004)	$\overline{\text{DSP\_LDO\_EN}}$ (Pin D12)	CLK_SEL (Pin C7)	ANA_LDO	DSP_LDO	USB_LDO
BG_PD Bit	LDO_PD Bit	USB_LDO_EN Bit					
1	Don't Care	Don't Care	Don't Care	0	OFF	OFF	ON
Don't Care	1	Don't Care	Don't Care	0	OFF	OFF	ON
0	0	Don't Care	Low	0	ON	ON	ON
0	0	Don't Care	High	0	ON	OFF	ON
1	Don't Care	Don't Care	Don't Care	1	OFF	OFF	OFF
Don't Care	1	Don't Care	Don't Care	1	OFF	OFF	OFF
0	0	0	Low	1	ON	ON	OFF
0	0	0	High	1	ON	OFF	OFF
0	0	1	Low	1	ON	ON	ON
0	0	1	High	1	ON	OFF	ON

5.7.2.2 Power-Supply Sequencing

The device includes four core voltage-level supplies (CV_{DD}, CV_{DDRTC}, USB_V_{DD1P3}, USB_V_{DDA1P3}), and several I/O supplies including—DV_{DDIO}, DV_{DDEMIF}, DV_{DDRTC}, USB_V_{DDOSC}, and USB_V_{DDA3P3}.

Some TI power-supply devices include features that facilitate power sequencing—for example, Auto-Track and Slow-Start and Enable features. For more information regarding TI's power management products and suggested devices to power TI DSPs, visit www.ti.com/processorpower.

The device does not require a specific power-up sequence. However, if the DSP_LDO is disabled ($\overline{DSP\_LDO\_EN}$ = high) and an external regulator supplies power to the CPU Core (CV_{DD}), the external reset signal ($\overline{RESET}$) must be held asserted until all of the supply voltages reach their valid operating ranges.

Note: the external reset signal on the $\overline{RESET}$ pin must be held low until all of the power supplies reach their operating voltage conditions.

The I/O design allows either the core supplies (CV_{DD}, CV_{DDRTC}, USB_V_{DD1P3}, USB_V_{DDA1P3}) or the I/O supplies (DV_{DDIO}, DV_{DDEMIF}, DV_{DDRTC}, USB_V_{DDOSC}, and USB_V_{DDA3P3}) to be powered up for an indefinite period of time while the other supply is not powered if the following constraints are met:

1. All maximum ratings and recommended operating conditions are satisfied.
2. All warnings about exposure to maximum rated and recommended conditions, particularly junction temperature are satisfied. These apply to power transitions as well as normal operation.
3. Bus contention while core supplies are powered must be limited to 100 hours over the projected lifetime of the device.
4. Bus contention while core supplies are powered down does not violate the absolute maximum ratings.

If the USB subsystem is used, the subsystem must be powered up in the following sequence:

1. USB_V_{DDA1P3} and USB_V_{DD1P3}
2. USB_V_{DDA3P3}
3. USB_V_{BUS}

If the USB subsystem is not used, the following can be powered off:

- USB Core
  - USB_V_{DD1P3}
  - USB_V_{DDA1P3}
- USB PHY and I/O Level Supplies
  - USB_V_{DDOSC}
  - USB_V_{DDA3P3}
  - USB_V_{DDPLL}

A supply bus is powered up when the voltage is within the recommended operating range. The supply bus is powered down when the voltage is below that range, either stable or while in transition.

5.7.2.3 Digital I/O Behavior When Core Power (CV_{DD}) is Down

With some exceptions (listed below), all digital I/O pins on the device have special features to allow powering down of the Digital Core Domain (CV_{DD}) without causing I/O contentions or floating inputs at the pins (see Figure 5-5). The device asserts the internal signal called HHV high when power has been removed from the Digital Core Domain (CV_{DD}). Asserting the internal HHV signal causes the following conditions to occur in any order:

- All output pin strong drivers to go to the high-impedance (Hi-Z) state
- Weak bus holders to be enabled to hold the pin at a valid high or low
- The internal pullups or pulldowns (IPUs and IPDs) on the I/O pins will be disabled

The exception pins that ***do not*** have this special feature are:

- Pins driven by the CV_{DDRTC} Power Domain [This power domain is "Always On"; therefore, the pins driven by CV_{DDRTC} *do not* need these special features]:
  - RTC_XI, RTC_XO, RTC_CLKOUT, and WAKEUP
- USB Pins:
  - USB_DP, USB_DM, USB_R1, USB_VBUS, USB_MXI, and USB_MXO
- Pins for the Analog Block:
  - GPAIN[3:0], $\overline{\text{DSP\_LDO\_EN}}$, and BG_CAP

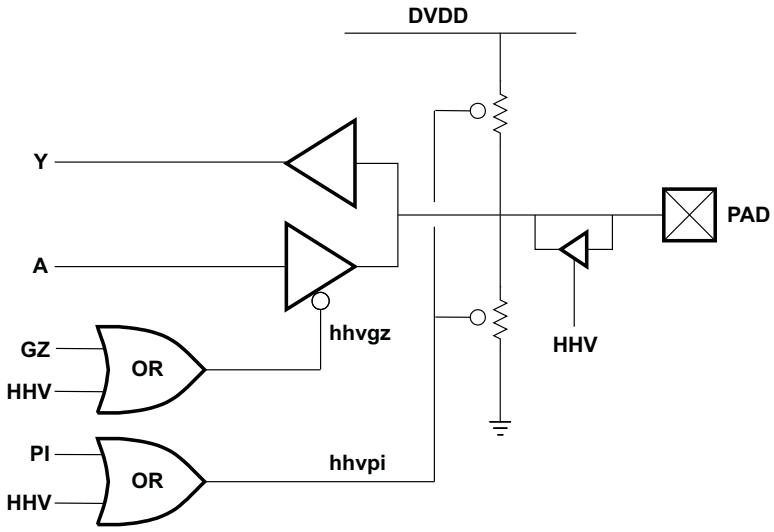


Figure 5-5. Bus Holder I/O Circuit

NOTE

Figure 5-5 shows both a pullup and pulldown but pins only have one, not both.

PI = Pullup and Pulldown Inhibit

GZ = Output Enable (active low)

HHV = Described in Section 5.7.2.3

5.7.2.4 Power-Supply Design Considerations

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the device, the PC board should include separate power planes for core, I/O, V_{DDA_ANA} and V_{DDA_PLL} (which can share the same PCB power plane), and ground; all bypassed with high–quality low–ESL and ESR capacitors.

5.7.2.5 Power-Supply Decoupling

In order to properly decouple the supply planes from system noise, place capacitors (caps) as close as possible to the device. These caps need to be no more than 1.25 cm maximum distance from the device power pins to be effective. Physically smaller caps, such as 0402, are better but need to be evaluated from a yield and manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors, therefore physically smaller capacitors should be used while maintaining the largest available capacitance value.

Larger caps for each supply can be placed further away for bulk decoupling. Large bulk caps (on the order of 10 µF) should be furthest away, but still as close as possible. Large caps for each supply should be placed outside of the BGA footprint.

As with the selection of any component, verification of capacitor availability over the product's production lifetime should be considered.

The recommended decoupling capacitance for the DSP core supplies should be 1 µF in parallel with 0.01-µF capacitor per supply pin.

5.7.2.6 LDO Input Decoupling

The LDO inputs should follow the same decoupling guidelines as other power-supply pins above.

5.7.2.7 LDO Output Decoupling

The LDO circuits implement a voltage feedback control system which has been designed to optimize gain and stability tradeoffs. As such, there are design assumptions for the amount of capacitance on the LDO outputs. For proper device operation, the following external decoupling capacitors should be used when the on-chip LDOs are enabled:

- ANA_LDOO– 1µF
- DSP_LDOO – 5µF ~ 10µF
- USB_LDOO – 1µF ~ 2µF

5.7.3 Reset

The device has two main types of reset: hardware reset and software reset.

Hardware reset is responsible for initializing all key states of the device. The hardware reset occurs whenever the RESET pin is asserted or when the internal power-on-reset (POR) circuit deasserts an internal signal called POWERGOOD. The device's internal POR is a voltage comparator that monitors the DSP_LDOO pin voltage and generates the internal POWERGOOD signal when the DSP_LDO is enabled externally by the DSP_LDO_EN pin. POWERGOOD is asserted when the DSP_LDOO voltage is above a minimum threshold voltage provided by the bandgap. When the DSP_LDO is disabled (DSP_LDO_EN is high), the internal voltage comparator becomes inactive, and the POWERGOOD signal logic level is immediately set high. The RESET pin and the POWERGOOD signal are internally combined with a logical AND gate to produce an (active low) hardware reset (see Figure 5-6, *Power-On Reset Timing Requirements* and Figure 5-7, *Reset Timing Requirements*).

There are two types of software reset: the CPU's software reset instruction and the software control of the peripheral reset signals. For more information on the CPU's software reset instruction, see the *C55x CPU 3.0 CPU* Reference Guide [literature number: SWPU073]. In all the device documentation, all references to "reset" refer to hardware reset. Any references to software reset will explicitly state software reset.

The device RTC has one additional type of reset, a power-on-reset (POR) for the registers in the RTC core. This POR monitors the voltage of CV_{DDRTC} and resets the RTC registers when power is first applied to the RTC core.

5.7.3.1 Power-On Reset (POR) Circuits

The device includes two power-on reset (POR) circuits, one for the RTC (RTC POR) and another for the rest of the chip (MAIN POR).

5.7.3.1.1 RTC Power-On Reset (POR)

The RTC POR ensures that the flip-flops in the CV_{DDRTC} power domain have an initial state upon powerup. In particular, the RTCNOPWR register is reset by this POR and is used to indicate that the RTC time registers need to be initialized with the current time and date when power is first applied.

5.7.3.1.2 Main Power-On Reset (POR)

The device includes an analog power-on reset (POR) circuit that keeps the DSP in reset until specific voltages have reached predetermined levels. When the DSP_LDO is enabled externally by the DSP_LDO_EN pin, the output of the POR circuit, POWERGOOD, is held low until the following conditions are satisfied:

- LDOI is powered and the bandgap is active for at least approximately 8 ms
- VDD_ANA is powered for at least approximately 4 ms
- DSP_LDOO is above a threshold of approximately 950 mV (see the following **Note:**)

Note: The POR comparator has hysteresis, so the threshold voltage becomes approximately 850 mV after POWERGOOD signal is set high.

Once these conditions are met, the internal POWERGOOD signal is set high. The POWERGOOD signal is internally combined with the RESET pin signal, via an AND-gate, to produce the DSP subsystem's global reset. This global reset is the hardware reset for the whole chip, except the RTC. When the global reset is deasserted (high), the boot sequence starts. For more detailed information on the boot sequence, see Section 6.4.1, *Boot Sequence*.

When the DSP_LDO is disabled (DSP_LDO_EN pin = 1), the voltage monitoring on the DSP_LDOO pin is de-activated and the POWERGOOD signal is immediately set high. The RESET pin will be the sole source of hardware reset.

5.7.3.1.3 Reset Pin (RESET)

The device can receive an external reset signal on the RESET pin. As specified above in Section 5.7.3.1.2, *Main Power-On Reset*, the RESET pin is combined with the internal POWERGOOD signal, that is generated by the MAIN POR, via an AND-gate. The output of the AND gate provides the hardware reset to the chip. The RESET pin may be tied high and the MAIN POR can provide the hardware reset in case DSP_LDO is enabled (DSP_LDO_EN = 0), but an external hardware reset must be provided via the RESET pin when the DSP_LDO is disabled (DSP_LDO_EN = 1).

Once the hardware reset is applied, the system clock generator is enabled and the DSP starts the boot sequence. For more information on the boot sequence, see Section 6.4.1, *Boot Sequence*.

5.7.3.2 Pin Behavior at Reset

All pins are in Hi-Z state when RESET is applied, and pins are held in Hi-Z state for the first two clock cycles after RESET is de-asserted (set to high).

During normal operation, pins are controlled by the respective peripheral selected in the External Bus Selection Register (EBSR) register. During power-on reset and reset, the behavior of the output pins changes and is categorized as follows:

- **Z, High Group:** EM_CS2, EM_CS3, EM_CS4, EM_CS5, EM_DQM0/UHPI_HBE0, EM_DQM1/UHPI_HBE1, EM_OE, EM_SDCAS/UHPI_HCS, EM_SDRAS/UHPI_HAS, EM_WE, XF
- **Z, Low Group:** SPI_CLK/UHPI_HINT, I2S2_DX/UHPI_HD[11]/GP[27]/SPI_TX, EM_R/W, MMC0_CLK/I2S0_CLK/GP[0]/McBSP_CLKX, MMC1_CLK/McSPI_CLK/GP[6], EM_SDCLK
- **Z Group:** EM_D[0:15], GP[21:26]/EM_A[15:20], GP[12:17]/UHPI_HD[2:7], EM_WAIT2, EM_WAIT3, EM_WAIT4, EM_WAIT5, EMU0, EMU1, SCL, SDA, TDO, USB_MXO, WAKEUP, RTC_CLKOUT

  I2S2_CLK/UHPI_HD[8]/GP[18]/SPI_CLK, I2S2_FS/UHPI_HD[9]/GP[19]/SPI_CS0, I2S2_RX/UHPI_HD[10]/GP[20]/SPI_RX

  MMC0_CMD/I2S0_FS/GP[1]/McBSP_FSX, MMC0_D0/I2S0_DX/GP[2]/McBSP_DX, MMC0_D1/I2S0_RX/GP[3]/McBSP_DR, MMC0_D2/GP[4]/McBSP_FSR, MMC0_D3/GP[5]/McBSP_CLKR_CLKS

  MMC1_CMD/McSPI_CS0/GP[7], MMC1_D0/McSPI_SIMO/GP[8], MMC1_D1/McSPI_SOMI/GP[9], MMC1_D2/McSPI_CS1/GP[10], MMC1_D3/McSPI_CS2/GP[11]

  UART_CTS/UHPI_HD[13]/GP[29]/I2S3_FS, UART_RXD/UHPI_HD[14]/GP[30]/I2S3_RX, SPI_TX/UHPI_HD[1], SPI_RX/UHPI_HD[0]
- **Z, CLKOUT Group:** CLKOUT
- **Z Group - Analog**: GPAIN0, GPAIN1, GPAIN2, GPAIN3
- **Z, SYNCH 0→1 Group:** EM_SDCKE/UHPI_HHWIL
- **Z, SYNCH 1→0 Group:** EM_CS0/UHPI_HDS1, EM_CS1/UHPI_HDS2
- **Z, SYNCH22 0→1 Group:** SPI_CS0/UHPI_HCNTL0, SPI_CS1/UHPI_HCNTL1, SPI_CS2/UHPI_HR_NW, SPI_CS3/UHPI_HRDY
- **Z, SYNCH X→1 Group:** EM_BA[0], EM_BA[1], UART_RTS/UHPI_HD[12]/GP[28]/I2S3_CLK, UART_TXD/UHPI_HD[15]/GP[31]/I2S3_DX
- **Z, SYNCH X→0 Group:** EM_A[0:10], EM_A[11]/(ALE), EM_A[12]/(CLE), EM_A[13], EM_A[14]

5.7.3.3 Reset Electrical Data and Timing

Table 5-4. Timing Requirements for Reset(1) (see Figure 5-6 and Figure 5-7)

NO.			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{w(RSTL)}$	Pulse duration, $\overline{RESET}$ low	3P		3P		ns

(1) P = 1/SYSCLK clock frequency in ns. For example, if SYSCLK = 12 MHz, use P = 83.3 ns. In IDLE3 mode the system clock generator is bypassed and the SYSCLK frequency is equal to either CLKIN or the RTC clock frequency depending on CLK_SEL.
For a description of IDLE3 mode, see the *System* chapter in the *TMS320C5517 Digital Signal Processor Technical Reference Manual* [literature number SPRUH16].

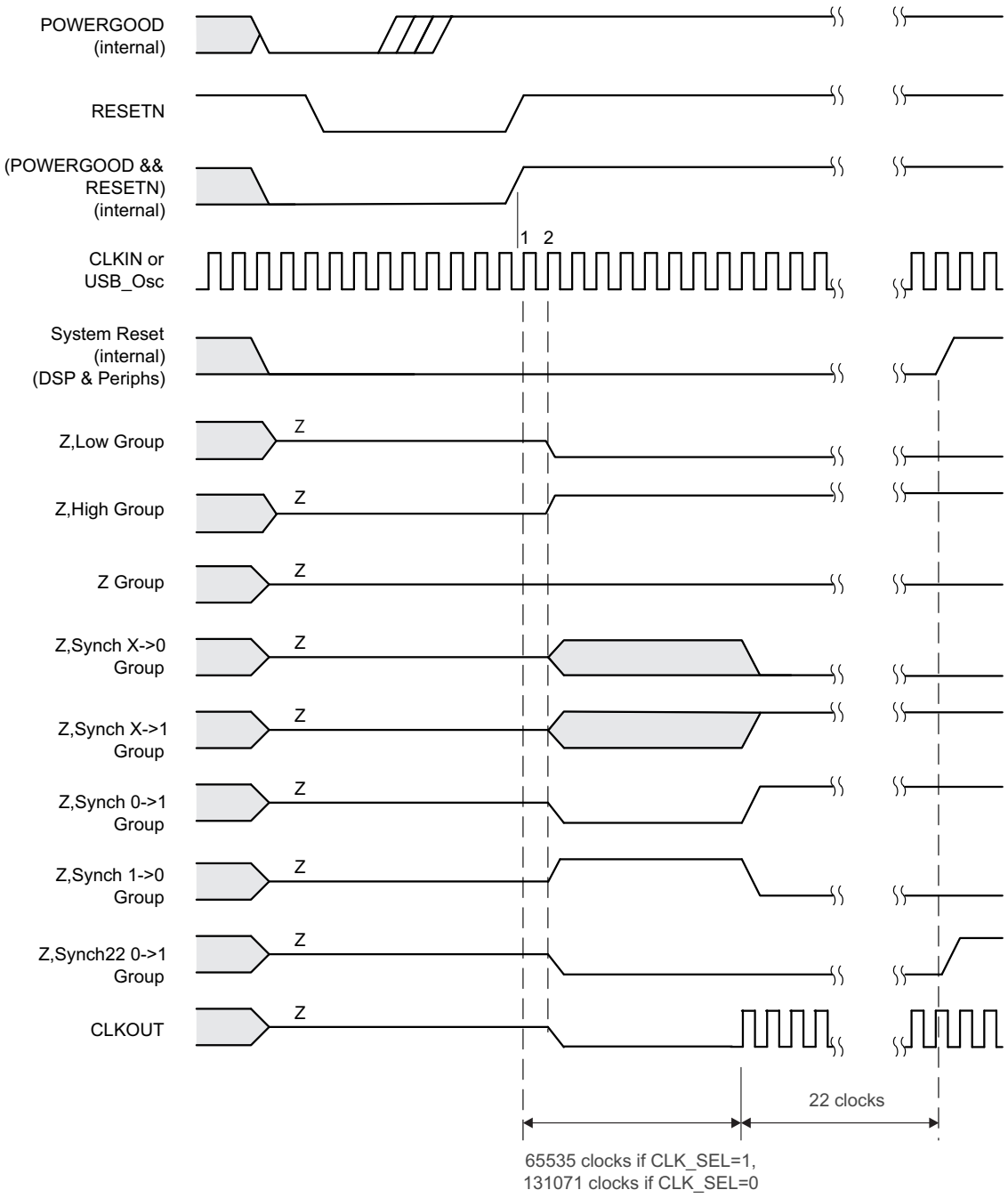


Figure 5-6. Reset Timing When DSP_LDO_EN = 0

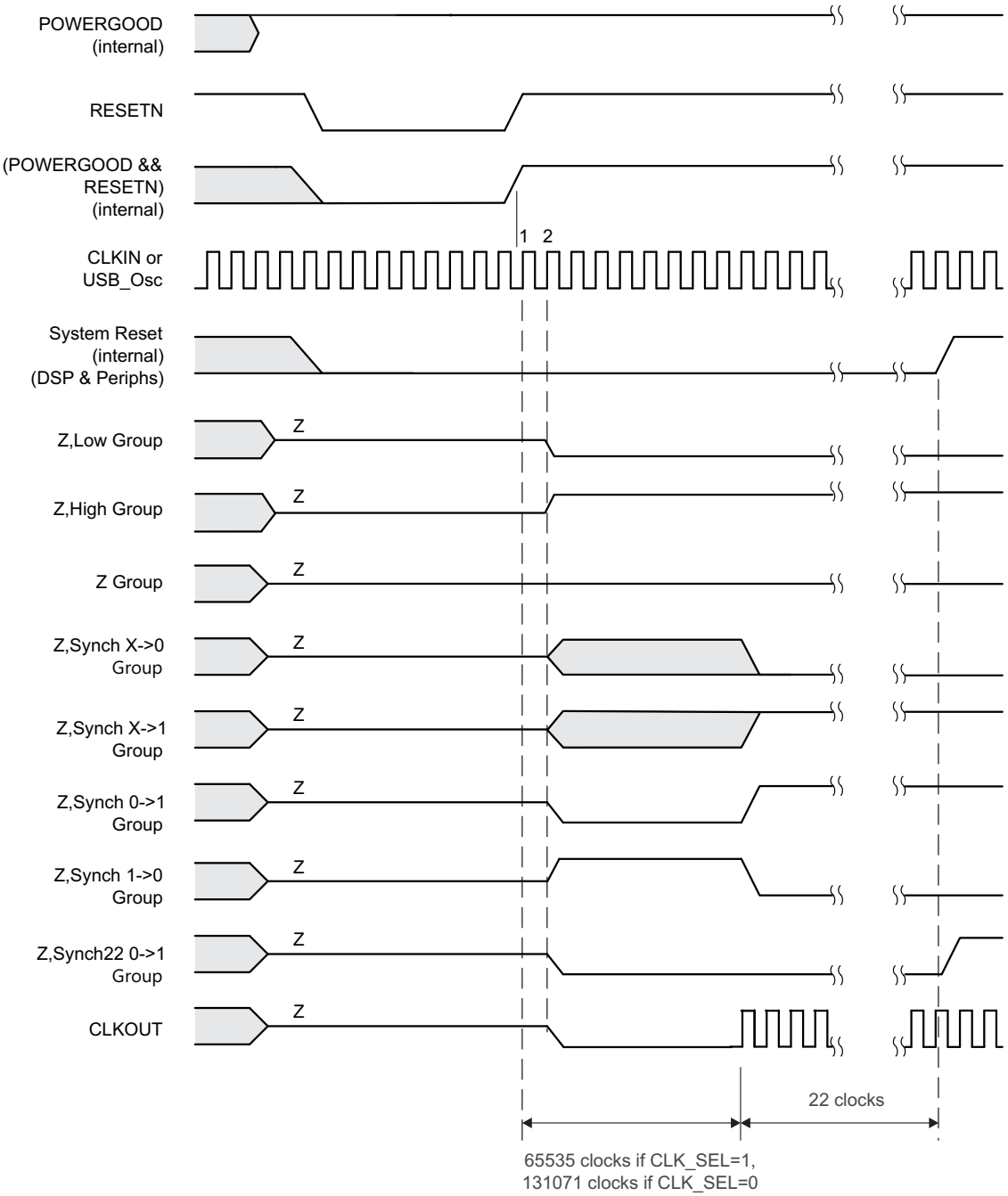


Figure 5-7. Reset Timing When DSP_LDO_EN = 1

5.7.3.4 Configurations at Reset

Some device configurations are determined at reset. The following subsections give more details.

5.7.3.4.1 Device and Peripheral Configurations at Device Reset

Table 5-5 summarizes the device boot and configuration pins that are required to be statically tied high, tied low, or left unconnected during device operation. For proper device operation, a device reset should be initiated after changing any of these pin functions.

Table 5-5. Default Functions Affected by Device Configuration Pins

CONFIGURATION PINS	SIGNAL NO.	IPU and IPD	FUNCTIONAL DESCRIPTION
$\overline{\text{DSP\_LDO\_EN}}$	D12	–	DSP_LDO enable input. This signal is ***not*** intended to be dynamically switched. 0 = DSP_LDO is enabled. The internal DSP LDO is enabled to regulate power on the DSP_LDOO pin at either 1.3 V or 1.05 V according to the LDO_DSP_V bit in the LDOCNTL register, see Figure 5-4). At power-on-reset, the internal POR monitors the DSP_LDOO pin voltage and generates the internal POWERGOOD signal when the DSP_LDO voltage is above a minimum threshold voltage. The internal device reset is generated by the AND of POWERGOOD and the $\overline{\text{RESET}}$ pin. 1 = DSP_LDO is disabled and the DSP_LDOO pin is in high-impedance (Hi-Z). The internal voltage monitoring on the DSP_LDOO is bypassed and the internal POWERGOOD signal is immediately set high. The $\overline{\text{RESET}}$ pin (D6) will act as the sole reset source for the device. If an external power supply is used to provide power to CV_{DD}, then $\overline{\text{DSP\_LDO\_EN}}$ should be tied to LDOI, DSP_LDOO should be left unconnected, and the $\overline{\text{RESET}}$ pin must be asserted appropriately for device initialization after powerup. **Note:** to pullup this pin, connect it to the same supply as LDOI pins.
CLK_SEL	C7	–	Clock input select. 0 = The on-chip USB oscillator is enabled and drives the system clock generator. Also, the USB LDOO is enabled at reset (USB_LDO_EN=1). In this configuration, CLKIN must be tied to GND. 1 = CLKIN drives the system clock generator. The on-chip USB oscillator and USB_LDO are disabled at reset (USB_LDO_EN=0) but can be enabled by software This pin is ***not*** allowed to change during device operation; it ***must*** be tied to DV_{DDIO} or GND at the board.

For proper device operation, external pullup and pulldown resistors may be required on these device configuration pins. For discussion on situations where external pullup and pulldown resistors are required, see Section 5.7.20.1.1, *Pullup and Pulldown Resistors*.

This device also has RESERVED pins that need to be configured correctly for proper device operation (statically tied high, tied low, or left unconnected at all times). For more details on these pins, see Table 4-24, *Reserved and No Connects Signal Descriptions*.

5.7.3.4.2 BootMode Implementation and Requirements

The EM_A[20:15]/GP[26:21] pins are used to latch the bootmode, as defined in Table 6-34. These pins are defined as GPIO function at reset and they are in input state. Therefore these pins can be driven to the desired bootmode terminations at reset. Approximately 10 system cycles after the rising edge of the RESET pin, the state on these pins will be latched into registers readable by the DSP at IO-space address 0x1C5A.

As the bootloader code starts executing, it reads the latched value in the bootmode register and uses that value to determine from which peripheral or method to boot. In any case where the ASYNC modes (except for NAND) are used as the source data for bootloading (for example, bootload from external NOR flash to internal memory), the bootloader routine in ROM will change the EM_A[20:15] or GP[26:21] pins from GPIO mode to EMIF mode by writing to the EBSR (0x1C00). When this occurs, no signal contentions must be on the EM_A[20:15] or GP[26:21] pins. Passive static terminations by external pullup or pulldown resistors should also be considered.

Note: Bootloading directly to external peripherals on the EMIF is not supported because the EMIF clock is turned off before jumping to bootloaded code.

The bootloader must enable the EMIF function on these pins in order to increase the address reach from 15-bits (EM_A[14:0] 32 kW) to the full 21-bits (EM_A[20:0] 2 MW). The bootloader does not have to enable the EMIF mode on the EM_A[20:15] or GP[26:21] pins for the following external memory types:

NAND: Uses the EM_D[15:0] pins for both address and data and command signaling.

SDRAM: Uses column and row addressing using no more than 11 bits of EM_A pins

The following image contains two BootMode termination scenarios. Other options are also possible.

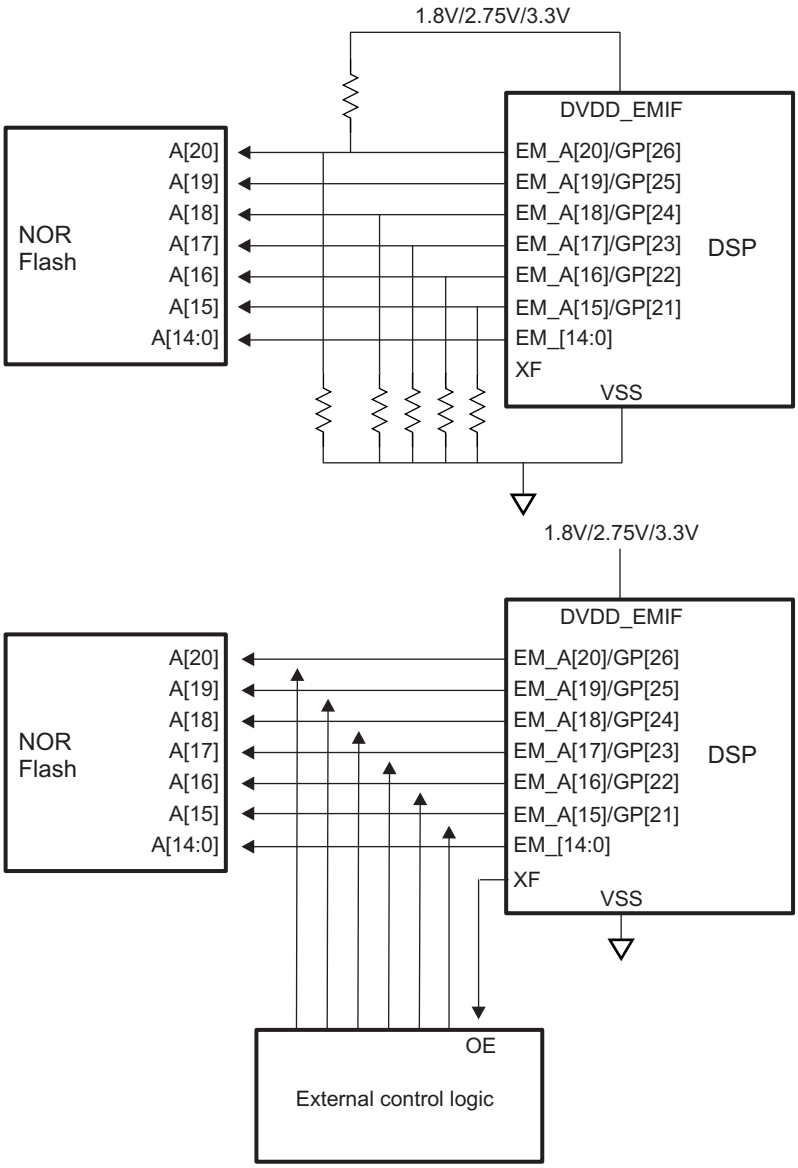
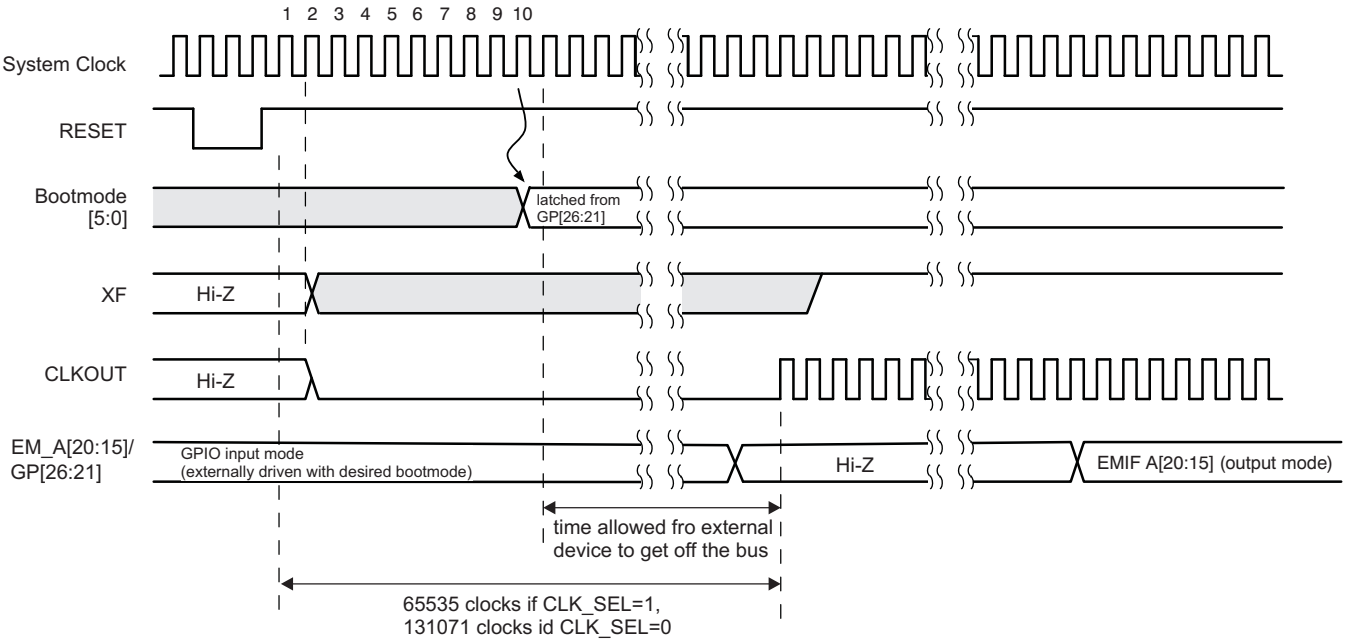


Figure 5-8. BootMode Termination Scenarios



A. DSP changes the pin mode to EMIF Address (outputs) only if needed for the selected bootmode.

Figure 5-9. BootMode Latching

5.7.3.5 Configurations After Reset

The following sections provide details on configuring the device after reset. Multiplexed pin functions are selected by software after reset. For more details on multiplexed pin function control, see Section 4.3, *Pin Multiplexing*.

5.7.3.5.1 External Bus Selection Register (EBSR)

The External Bus Selection Register (EBSR) determines the mapping of the UHPI, I2S2, I2S3, UART, SPI, McBSP, McSPI, and GPIO signals to 28 signals of the external parallel port pins. The EBSR also determines the mapping of the I2S, McBSP, McSPI, GPIO, or MMC and SD ports to serial port 0 pins and serial port 1 pins. The EBSR register is located at IO-space 0x1C00. Once the bit fields of this register are changed, the routing of the signals takes place on the next CPU clock cycle.

In addition, the EBSR controls the function of the upper bits of the EMIF address bus. Pins EM_A[20:15] or GP[26:21] can be individually configured as GPIO pins through the Axx_MODE bits. When Axx_MODE = 1, the EM_A[xx] pin functions as a GPIO pin. When Axx_MODE = 0, the EM_A[xx] pin has EMIF address output functionality.

Before modifying the values of the external bus selection register, you must clock gate all affected peripherals through the Peripheral Clock Gating Control Register. After the external bus selection register has been modified, you must reset the peripherals before using them through the Peripheral Software Reset Counter Register.

Figure 5-10. External Bus Selection Register (EBSR) [1C00h]

15	14	13	12	11	10	9	8
McBSP_CLKS Selection	PPMODE			SP1MODE		SP0MODE	
R/W-0	R/W-001			R/W-00		R/W-00	
7	6	5	4	3	2	1	0
Reserved		A20_MODE	A19_MODE	A18_MODE	A17_MODE	A16_MODE	A15_MODE
R-0		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-6. EBSR Register Field Descriptions

Bit	Field	Description
15	McBSP_CLKS Selection	McBSP_CLKS Selection 0 = McBSP_CLKR signal is routed to MMC0_D3/GP[5]/McBSPCLKR_CLKS (L11) when SP0MODE=3 1 = McBSP_CLKS signal is routed to MMC0_D3/GP[5]/McBSPCLKR_CLKS (L11) when SP0MODE=3
14:12	PPMODE	Parallel Port Mode Control Bits. These bits control the pin multiplexing of the UHPI, SPI, UART, I2S2, I2S3, and GP[31:27, 20:12] pins on the parallel port. For more details, see Table 4-20. 000 = Mode 0 (16-bit UHPI bus). All 28 signals of the UHPI bus module are routed to the 28 external signals of the parallel port. Note: SDRAM control signals are multiplexed with UHPI bus control signals. In this mode, UHPI bus signals are routed to the control ports, so SDRAM cannot be accessible. 001 = Mode 1 (SPI, GPIO, UART, I2S2, and SDRAM). 7 signals of the SPI module, 6 GPIO signals, 4 signals of the UART module, 4 signals of the I2S2 module, and 7 SDRAM control signals are routed to the 28 external signals of the parallel port. 010 = Mode 2 (GPIO and SDRAM). 8 GPIO and 7 SDRAM control signals are routed to the 28 external signals of the parallel port. 011 = Mode 3 (SPI, I2S3, and SDRAM). 4 signals of the SPI module, 4 signals of the I2S3 module, and 7 SDRAM control signals are routed to the 28 external signals of the parallel port. 100 = Mode 4 (I2S2, UART, and SDRAM). 4 signals of the I2S2 module, 4 signals of the UART module, and 7 SDRAM control signals are routed to the 28 external signals of the parallel port. 101 = Mode 5 (SPI, UART, and SDRAM). 4 signals of the SPI module, 4 signals of the UART module, and 7 SDRAM control signals are routed to the 28 external signals of the parallel port. 110 = Mode 6 (SPI, I2S2, I2S3, GPIO, and SDRAM). 7 signals of the SPI module, 4 signals of the I2S2 module, 4 signals of the I2S3 module, 6 GPIO, and 7 SDRAM control signals are routed to the 28 external signals of the parallel port. 111 = Reserved.
11:10	SP1MODE	Serial Port 1 Mode Control Bits. The bits control the pin multiplexing of the MMC1, McSPI, and GPIO pins on serial port 1. For more details, see Table 4-21. 00 = Mode 0 (MMC1 and SD1). All 6 signals of the MMC1 and SD1 module are routed to the 6 external signals of the serial port 1. 01 = Mode 1 (McSPI). 6 signals of the McSPI module signals are routed to the 6 external signals of the serial port 1. 10 = Mode 2 (GP[11:6]). 6 GPIO signals (GP[11:6]) are routed to the 6 external signals of the serial port 1. 11 = Reserved.
9:8	SP0MODE	Serial Port 0 Mode Control Bits. The bits control the pin multiplexing of the MMC0, I2S0, McBSP, and GPIO pins on serial port 0. For more details, see Section 4.3.3. 00 = Mode 0 (MMC0 and SD0). All 6 signals of the MMC0 and SD0 module are routed to the 6 external signals of the serial port 0. 01 = Mode 1 (I2S0 and GP[5:4]). 4 signals of the I2S0 module and 2 GP[5:4] signals are routed to the 6 external signals of the serial port 0. 10 = Mode 2 (GP[5:0]). 6 GPIO signals (GP[5:0]) are routed to the 6 external signals of the serial port 0. 11 = Mode 3 (McBSP). 6 signals of the McBSP module are routed to the 6 external signal port 0.
7-6	Reserved	Reserved. Read-only, writes have no effect.

Table 5-6. EBSR Register Field Descriptions (continued)

Bit	Field	Description
5	A20_MODE	A20 Pin Mode Bit. This bit controls the pin multiplexing of the EMIF address 20 (EM_A[20]) and general-purpose input/output pin 26 (GP[26]) pin functions. 0 = Pin function is EMIF address pin 20 (EM_A[20]). 1 = Pin function is general-purpose input/output pin 26 (GP[26]). This is the default mode at reset and the pin is configured as an Input. Approximately 10 cycles after the rising edge of RESET, the state on this pin is latched into the BootMode register to specify the boot method.
4	A19_MODE	A19 Pin Mode Bit. This bit controls the pin multiplexing of the EMIF address 19 (EM_A[19]) and general-purpose input/output pin 25 (GP[25]) pin functions. 0 = Pin function is EMIF address pin 19 (EM_A[19]). 1 = Pin function is general-purpose input/output pin 25 (GP[25]). This is the default mode at reset and the pin is configured as an Input. Approximately 10 cycles after the rising edge of RESET, the state on this pin is latched into the BootMode register to specify the boot method.
3	A18_MODE	A18 Pin Mode Bit. This bit controls the pin multiplexing of the EMIF address 18 (EM_A[18]) and general-purpose input/output pin 24 (GP[24]) pin functions. 0 = Pin function is EMIF address pin 18 (EM_A[18]). 1 = Pin function is general-purpose input/output pin 24 (GP[24]). This is the default mode at reset and the pin is configured as an Input. Approximately 10 cycles after the rising edge of RESET, the state on this pin is latched into the BootMode register to specify the boot method.
2	A17_MODE	A17 Pin Mode Bit. This bit controls the pin multiplexing of the EMIF address 17 (EM_A[17]) and general-purpose input/output pin 23 (GP[23]) pin functions. For more details, see Table 4-22, *MMC0, I2S0, McBSP, and GP[5:0] Pin Multiplexing*. 0 = Pin function is EMIF address pin 17 (EM_A[17]). 1 = Pin function is general-purpose input/output pin 23 (GP[23]). This is the default mode at reset and the pin is configured as an Input. Approximately 10 cycles after the rising edge of RESET, the state on this pin is latched into the BootMode register to specify the boot method.
1	A16_MODE	A16 Pin Mode Bit. This bit controls the pin multiplexing of the EMIF address 16 (EM_A[16]) and general-purpose input/output pin 22 (GP[22]) pin functions. For more details, see Table 4-22, *MMC0, I2S0, McBSP, and GP[5:0] Pin Multiplexing*. 0 = Pin function is EMIF address pin 16 (EM_A[16]). 1 = Pin function is general-purpose input/output pin 22 (GP[22]). This is the default mode at reset and the pin is configured as an Input. Approximately 10 cycles after the rising edge of RESET, the state on this pin is latched into the BootMode register to specify the boot method.
0	A15_MODE	A15 Pin Mode Bit. This bit controls the pin multiplexing of the EMIF address 15 (EM_A[15]) and general-purpose input/output pin 21 (GP[21]) pin functions. For more details, see Table 4-22, *MMC0, I2S0, McBSP, and GP[5:0] Pin Multiplexing*. 0 = Pin function is EMIF address pin 15 (EM_A[15]). 1 = Pin function is general-purpose input/output pin 21 (GP[21]). This is the default mode at reset and the pin is configured as an Input. Approximately 10 cycles after the rising edge of RESET, the state on this pin is latched into the BootMode register to specify the boot method.

5.7.3.5.2 LDO Control Register [7004h]

When the DSP_LDO is enabled by the $\overline{\text{DSP\_LDO\_EN}}$ pin being tied low, the DSP_LDOO voltage is set by the DSP_LDO_V bit in this register. The reset state of this bit causes the DSP_LDOO output to be set to 1.3 V at boot. The DSP_LDOO voltage can be programmed to be either 1.05 V or 1.3 V via the DSP_LDO_V bit (bit 1) in the LDO Control Register (LDOCNTL).

At reset, the USB_LDO state is dependent on the CLK_SEL pin. At reset, if CLK_SEL is high (CLK_SEL=1), the USB LDO is disabled but can be enabled via the USBLDOEN bit (bit 0) in the LDOCNTL register. If CLK_SEL is low (CLK_SEL=0), the USB LDO is enabled and cannot be disabled.

For more detailed information on the LDOs, see Section 5.7.2.1.1, *LDO Configuration*.

5.7.3.5.3 EMIF and USB System Control Registers (ESCR and USBSCR) [1C33h and 1C32h]

After reset, by default, the CPU performs 16-bit accesses to the EMIF and USB registers and data space. To perform 8-bit accesses to the EMIF data space, the user must set the BYTEMODE bits to 01b for the "high byte" or 10b for the "low byte" in the EMIF System Control Register (ESCR). Similarly, the BYTEMODE bits in the USB System Control Register (USBSCR) must also be configured for byte access.

5.7.3.5.4 Peripheral Clock Gating Control Registers (PCGCR1 and PCGCR2) [1C02h and 1C03h]

After hardware reset, the DSP executes the on-chip bootloader from ROM. Depending on the BootMode used, the bootloader may leave the PCGCR1 and the PCGCR2 registers in various states. This is also true of the ICR and the ISR registers.

Programmers should always verify the state of these registers and appropriately set them. Their states after boot loading are not determined by their reset conditions.

5.7.3.5.5 Pullup and Pulldown Inhibit Registers (PUDINHIBR1, 2, 3, 4, 5, 6, and 7) [1C17h, 1C18h, 1C19h, 1C4Ch, 1C4Dh, 1C4Fh, and 1C50h, respectively]

Each internal pullup and pulldown (IPU and IPD) resistor on the device can be individually controlled through the IPU and IPD registers (PUDINHIBR1 [1C17h] , PUDINHIBR2 [1C18h], PUDINHIBR3 [1C19h], PUDINHIBR4 [1C4Ch], PUDINHIBR5 [1C4Dh], PUDINHIBR6 [1C4Fh], and PUDINHIBR7 [1C50h]). To minimize power consumption, internal pullup or pulldown resistors should be disabled in the presence of an external pullup or pulldown resistor or external driver. Most internal pullups and pulldowns are enabled at reset to help ensure no pins are left floating. Section 5.7.20.1.1, *Pullup and Pulldown Resistors*, describes other situations in which an pullup and pulldown resistors are required.

When CV_{DD} is powered down, pullup and pulldown resistors will be forced disabled and an internal bus-holder will be enabled. For more detailed information, see Section 5.7.2.3, *Digital I/O Behavior When Core Power (CV_{DD}) is Down*.

5.7.3.5.6 Output Slew Rate Control Register (OSRCR) [1C16h]

To provide the lowest power consumption setting, the DSP has configurable slew rate control on the EMIF and CLKOUT output pins. The output slew rate control register (OSRCR) is used to set a subset of the device I/O pins, namely CLKOUT and EMIF pins, to either fast or slow slew rate. The slew rate feature is implemented by staging and delaying turn-on times of the parallel p-channel drive transistors and parallel n-channel drive transistors of the output buffer. In the slow slew rate configuration, the delay is longer, but ultimately the same number of parallel transistors are used to drive the output high or low. Thus, the drive strength is ultimately the same. The slower slew rate control can be used for power savings and has the greatest effect at lower DV_{DDIO} and DV_{DDEMIF} voltages.

5.7.4 Clock Specifications

5.7.4.1 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

5.7.4.2 Clock Considerations

The system clock, which is used by the CPU and most of the DSP peripherals, is controlled by the system clock generator. The system clock generator features a software-programmable PLL multiplier and several dividers. The clock generator accepts an input reference clock from the CLKIN pin or the output clock of the on-chip USB oscillator. The selection of the input reference clock is based on the state of the CLK_SEL pin. The CLK_SEL pin is required to be statically tied high or low and cannot change dynamically after reset.

If CLK_SEL=0 at reset, the on-chip USB oscillator is selected as the source of the system clock generator and the USB PLL as well. In this configuration, the on-chip USB oscillator cannot be turned off.

If CLK_SEL=1 at reset, the external clock via the CLKIN pin will be used as the source of the system clock generator and the on-chip USB oscillator is used only for the USB PLL input. In this configuration, the on-chip USB oscillator can be turned off if the USB peripheral is not being used.

In addition, the DSP requires a reference clock for the real-time clock (RTC). The RTC reference clock is generated using a dedicated on-chip oscillator with a 32.768-kHz external crystal connected to the RTC_XI and RTC_XO pins.

The 32.768-kHz crystal can be disabled if the RTC peripheral is not being used. However, when the RTC oscillator is disabled, the RTC peripheral will not operate and the RTC registers (I/O address range 1900h – 197Fh) will not be accessible. This includes the RTC power management register (RTCPMGT) which controls the RTCLKOUT and WAKEUP pins. To disable the RTC oscillator, connect the RTC_XI pin to CV_{DDRTC} and the RTC_XO pin to ground.

For more information on crystal specifications for the RTC oscillator and the USB oscillator, see Section 5.7.4.3.3, *External Clock Input From RTC_XI, CLKIN, and USB_MXI Pins*.

5.7.4.2.1 Clock Configurations After Device Reset

After reset, the on-chip Bootloader programs the system clock generator based on the value of EM_A[20:15] or GP[26:21], which are latched into the BootMode[5:0] bits in the BootMode register ([1C34h]) at reset. (See Section 6.4, *Boot Modes,* for details.)

5.7.4.2.1.1 Device Clock Frequency

After the boot process is complete, the user is allowed to re-program the system clock generator to bring the device up to the desired clock frequency and the desired peripheral clock state (clock gating or not). The user must adhere to various clock requirements when programming the system clock generator. For more information, see Section 5.7.4.3, *Clock PLLs*.

Note: The on-chip Bootloader allows for DSP registers to be configured during the boot process. However, this feature ***must not*** be used to change the output frequency of the system clock generator during the boot process. The bootloader also uses Timer0 to calculate the settling time of BG_CAP until executing bootloader code. The bootloader register modification feature ***must not*** modify the Timer0 registers.

5.7.4.2.1.2 Peripheral Clock State

The clock and reset state of each of peripheral is controlled through a set of system registers. The peripheral clock gating control registers (PCGCR1 and PCGCR2) are used to enable and disable peripheral clocks. The peripheral software reset counter register (PSRCR) and the peripheral reset control register (PRCR) are used to assert and de-assert peripheral reset signals.

After hardware reset, the DSP boots via the bootloader code in ROM. During the boot process, the bootloader chooses a peripheral or method to boot from based on the value of BootMode[5:0] bits in the BootMode register ([1C34h]) and queries the peripheral to determine if it can boot from that peripheral. At that time, the individual peripheral clock will be enabled for the query and then disabled again when the bootloader is finished with the peripheral. By the time the bootloader releases control to the user code, all peripheral clocks will be off and all domains in the ICR, except the CPU domain, will be idled.

5.7.4.2.1.3 USB Oscillator Control

At reset, if CLK_SEL = 0, the on-chip USB oscillator is enabled and is used as the clock source of the system clock generator. Since the USB oscillator is the system's clock source, it is not possible to disable the USB oscillator when CLK_SEL = 0.

When CLK_SEL = 1, the USB Oscillator is disabled at reset but can be enabled or disabled by writing to the USB system control register (USBSCR). To enable the oscillator, the USBOSCDIS and USBOSCBIASDIS bits must be cleared to 0. The user must wait until the USB oscillator stabilizes before proceeding with the USB configuration. The USB oscillator stabilization time is typically 100 µs, with a 10 ms maximum. (**Note:** The startup time is highly dependent on the ESR and capacitive load on the crystal.)

5.7.4.3 PLLs

The device DSP uses a software-programmable PLL to generate frequencies required by the CPU, DMA, and peripherals. The reference clock for the PLL is taken from either the CLKIN pin or the USB on-chip oscillator (as specified through the CLK_SEL pin).

5.7.4.3.1 PLL Device-Specific Information

There is a minimum and maximum operating frequency for CLKIN, PLLIN, and the system clock (SYSCLK). The system clock generator must be configured not to exceed any of these constraints documented in this section (certain combinations of external clock inputs, internal dividers, and PLL multiply ratios are not supported).

Table 5-7. PLL Clock Frequency Ranges

CLOCK SIGNAL NAME	CV_{DD} = 1.05 V, V_{DDA_PLL} = 1.3 V			CV_{DD} = 1.3 V, V_{DDA_PLL} = 1.3 V			CV_{DD} = 1.4 V, V_{DDA_PLL} = 1.3 V			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CLKIN(1)		11.2896, 12.0, 12.288, 16.8, or 19.2			11.2896, 12.0, 12.288, 16.8, or 19.2			11.2896, 12.0, 12.288, 16.8, or 19.2		MHz
PLLIN	1.7		6.79	1.7		6.79	1.7		6.79	MHz
PLLOUT	60		120	60		120	60		120	
VCO Output(2) (before output divider OD and OD2)	125		625	125		625	125		625	MHz
SYSCLK	0		75	0		175	0		200	MHz
PLL_LOCKTIME			4			4			4	ms

(1) These CLKIN values are used when the CLK_SEL pin = 1.
(2) To use less PLL power, ensure VCO max is close to the SYSCLK max.

The PLL has lock time requirements that must be followed. The PLL lock time is the amount of time needed for the PLL to complete its phase-locking sequence.

5.7.4.3.2 Clock PLL Considerations With External Clock Sources

If the CLKIN pin is used to provide the reference clock to the PLL, to minimize the clock jitter a single clean power supply should power both the device and the external clock oscillator circuit. The minimum CLKIN rise and fall times should also be observed. For the input clock timing requirements, see Section 5.7.4.4, *Input and Output Clocks Electrical Data and Timing*.

Rise and fall times, duty cycles (high and low pulse durations), and the load capacitance of the external clock source must meet the device requirements in this data manual (see Section 5.3.2, *Electrical Characteristics*, and Section 5.7.4.4, *Input and Output Clocks Electrical Data and Timing*.

5.7.4.3.3 External Clock Input From RTC_XI, CLKIN, and USB_MXI Pins

The device DSP includes two options to provide an external clock input to the system clock generator:

- Use the on-chip USB oscillator with an external 12-MHz crystal connected to the USB_MXO and USB_MXI pins.
- Use an external LVCMOS clock input fed into the CLKIN pin that operates at the same voltage as the DV_{DDIO} supply (1.8-, 2.75-, or 3.3-V).

The CLK_SEL pin determines which input is used as the clock source for the system clock generator. For more details, see Section 5.7.3.4.1.

If CLK_SEL = 0 at reset, the on-chip USB oscillator is used as the source of the system clock generator and the USB PLL as well.

If CLK_SEL= 1 at reset, the external LVCMOS clock input fed into the CLKIN pin will be used as the source of the system clock generator and the on-chip USB oscillator is used only for the USB PLL source. In this configuration, the on-chip USB oscillator can be turned off if the USB peripheral is not being used.

Additionally, the DSP requires a reference clock for the on-chip real time clock (RTC). The RTC reference clock is generated using a dedicated on-chip oscillator with a 32.768-kHz external crystal connected to the RTC_XI and RTC_XO pins. The crystal for the RTC oscillator is not required if the RTC is not used, however the RTC must still be powered by an external power source. None of the on-chip LDOs can power CV_{DDRTC}. The RTC registers starting at I/O address 1900h will not be accessible without an RTC clock. This includes the RTC Power Management Register which provides control to the on-chip LDOs and WAKEUP and RTC_CLKOUT pins. Section 5.7.4.3.3.2, *Real-Time Clock (RTC) On-Chip Oscillator With External Crystal*, provides more details on using the RTC on-chip oscillator with an external crystal.

5.7.4.3.3.1 USB On-Chip Oscillator With External Crystal

The USB on-chip oscillator requires an external 12-MHz crystal connected across the USB_MXI and USB_MXO pins, along with two load capacitors, as shown in Figure 5-11. The external crystal load capacitors must be connected only to the USB oscillator ground pin (USB_V_{SSOSC}). ***Do not*** connect to board ground (V_{SS}). The USB_V_{DDOSC} pin can be connected to the same power supply as USB_V_{DDA3P3}.

If the external clock input via the CLKIN pin is used as the source of the system clock generator (CLK_SEL =1 at reset) and the USB peripheral is not being used, then the on-chip USB oscillator can be permanently disabled. To permanently disable the USB oscillator, connect the USB_MXI pin to ground (V_{SS}) and leave the USB_MXO pin unconnected. The USB oscillator power pins (USB_V_{DDOSC} and USB_V_{SSOSC}) should also be connected to ground, as shown in Figure 5-12.

When using an external 12-MHz oscillator, the external oscillator clock signal should be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V_{IH} requirement (see Section 5.2, *Recommended Operating Conditions*). The USB_MXO is left unconnected and the USB_V_{SSOSC} signal is connected to board ground (V_{SS}).

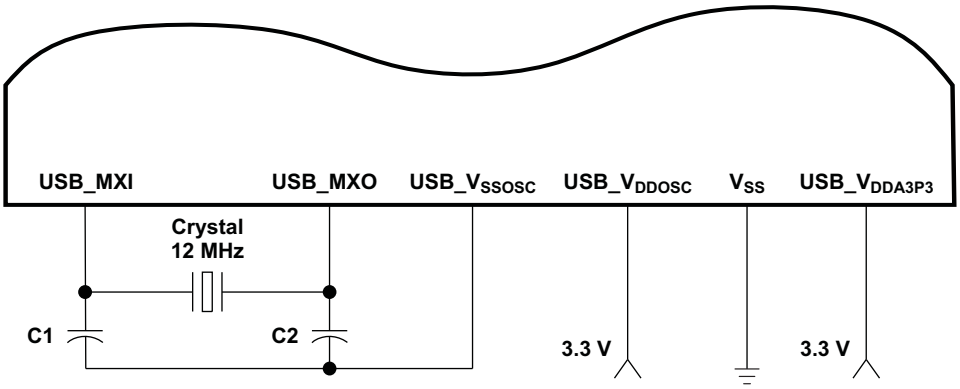


Figure 5-11. 12-MHz USB Oscillator

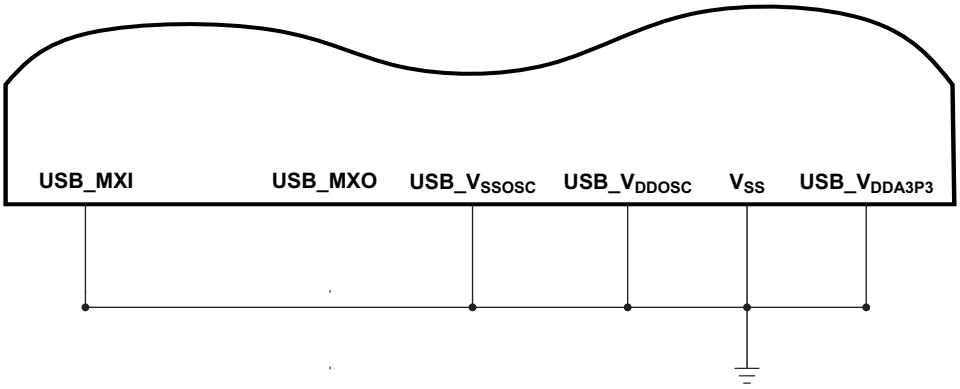


Figure 5-12. Connections when USB Oscillator is Permanently Disabled

The crystal should be in fundamental-mode operation, and parallel resonant, with a maximum effective series resistance (ESR) specified in Table 5-8. The load capacitors, C1 and C2 are the total capacitance of the circuit board and components, excluding the IC and crystal. The load capacitor value is usually approximately twice the value of the crystal's load capacitance, CL, which is specified in the crystal manufacturer's datasheet and should be chosen such that the equation below is satisfied. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (USB_MXI and USB_MXO) and to the USB_V_{SSOSC} pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

Table 5-8. Input Requirements for Crystal on the 12-MHz USB Oscillator

PARAMETER	MIN	NOM	MAX	UNIT
Start-up time (from power up until oscillating at stable frequency of 12 MHz)(1)		0.100	10	ms
Oscillation frequency		12		MHz
ESR			100	kΩ
Frequency stability (2)			±100	ppm
Maximum shunt capacitance			5	pF
Maximum crystal drive			330	µW

(1) The startup time is highly dependent on the ESR and the capacitive load of the crystal.
(2) If the USB is used, a 12-MHz, ±100-ppm crystal is recommended.

5.7.4.3.3.2 Real-Time Clock (RTC) On-Chip Oscillator With External Crystal

The on-chip RTC oscillator requires an external 32.768-kHz crystal connected across the RTC_XI and RTC_XO pins, along with two load capacitors, as shown in Figure 5-13. The external crystal load capacitors must be connected only to the RTC oscillator ground pin (V_{SSRTC}). ***Do not*** connect to board ground (V_{SS}). Position the V_{SS} lead on the board between RTC_XI and RTC_XO as a shield to reduce direct capacitance between RTC_XI and RTC_XO leads on the board. The CV_{DDRTC} pin can be connected to the same power supply as CV_{DD}, or may be connected to a different supply that meets the recommended operating conditions (see Section 5.2, *Recommended Operating Conditions*), if desired.

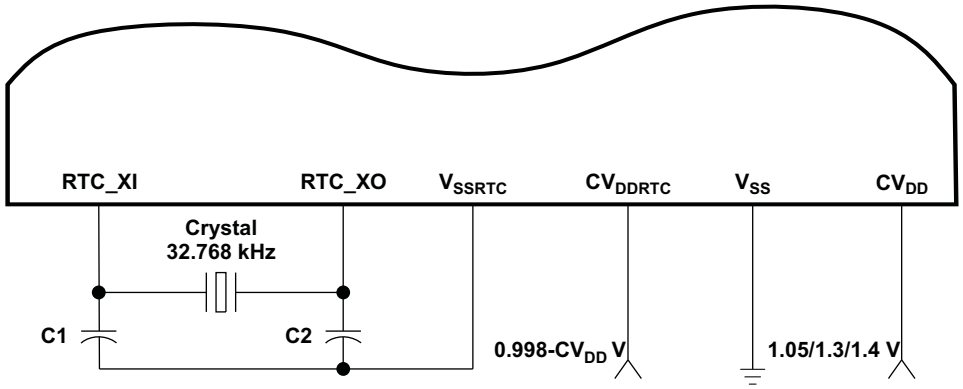


Figure 5-13. 32.768-kHz RTC Oscillator

The RTC oscillator can be optionally disabled by connecting RTC_XI to CV_{DDRTC} and RTC_XO to ground (V_{SS}). However, when the RTC oscillator is disabled the RTC registers starting at I/O address 1900h will not be accessible. This includes the RTC Power Management Register which provides control to the on-chip LDOs and WAKEUP and RTC_CLKOUT pins. **Note:** The RTC must still be powered even if the RTC oscillator is disabled.

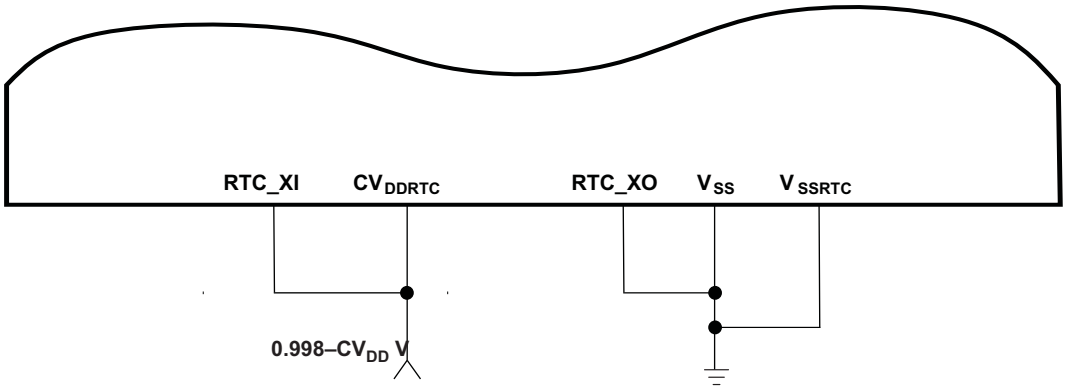


Figure 5-14. Connections when RTC Oscillator is Permanently Disabled

The crystal should be in fundamental-mode function, and parallel resonant, with a maximum effective series resistance (ESR) specified in Table 5-9. The load capacitors, C1 and C2, are the total capacitance of the circuit board and components, excluding the IC and crystal. The load capacitors values are usually approximately twice the value of the crystal's load capacitance, CL, which is specified in the crystal manufacturer's datasheet and should be chosen such that the equation is satisfied. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (RTC_XI and RTC_XO) and to the V_{SSRTC} pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

Table 5-9. Input Requirements for Crystal on the 32.768-kHz RTC Oscillator

PARAMETER	MIN	NOM	MAX	UNIT
Start-up time (from power up until oscillating at stable frequency of 32.768-kHz)(1)	0.2		2	sec
Oscillation frequency		32.768		kHz
ESR			100	kΩ
Maximum shunt capacitance			1.6	pF
Maximum crystal drive			1.0	µW

(1) The startup time is highly dependent on the ESR and the capacitive load of the crystal.

5.7.4.3.3.3 CLKIN Pin With LVCMOS-Compatible Clock Input (Optional)

Note: If CLKIN is not used, the pin ***must*** be tied low.

A LVCMOS-compatible clock can be fed into the CLKIN pin for use by the DSP system clock generator. The external connections are shown in Figure 5-15 and Figure 5-16. The bootloader assumes that the CLKIN pin is connected to the LVCMOS-compatible clock source with a frequency of 11.2896, 12.0, 12.288, 16.8, or 19.2 MHz based on the value of BootMode[5:4] bits at reset. (See Section 6.4, *Boot Mode*, for details.) **Note:** The CLKIN pin operates at the same voltage as the DV_{DDIO} supply (1.8, 2.75, or 3.3 V).

In this configuration the RTC oscillator can be optionally disabled by connecting RTC_XI to CV_{DDRTC} and RTC_XO to ground (V_{SS}). However, when the RTC oscillator is disabled the RTC registers starting at I/O address 1900h will not be accessible. This includes the RTC Power Management Register which provides control to the on-chip LDOs and WAKEUP and RTC_CLKOUT pins. **Note:** The RTC must still be powered by an external power source even if the RTC oscillator is disabled. None of the on-chip LDOs can power CV_{DDRTC}.

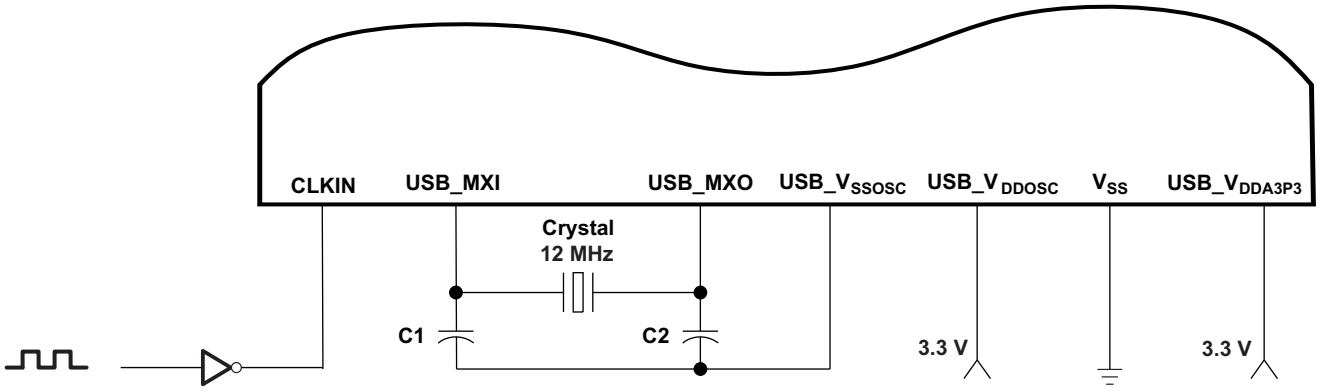


Figure 5-15. LVCMOS-Compatible Clock Input With USB Oscillator Enabled

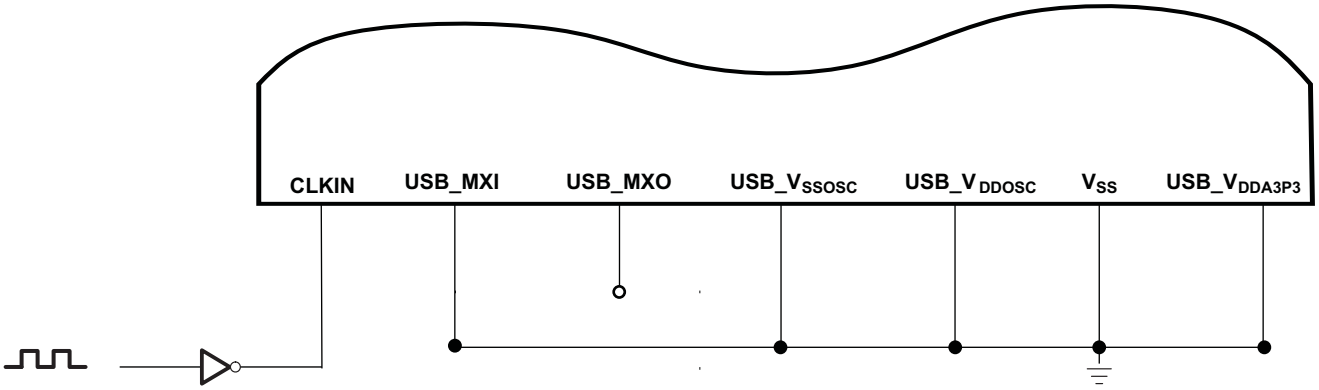


Figure 5-16. LVCMOS-Compatible Clock Input With USB Oscillator Disabled

5.7.4.4 Input and Output Clocks Electrical Data and Timing

Table 5-10. Timing Requirements for CLKIN(1) (2) (see Figure 5-17)

NO.			CV_{DD} = 1.05/1.3/1.4 V			UNIT
			MIN	NOM	MAX	
1	$t_{c(CLKIN)}$	Cycle time, external clock driven on CLKIN		11.2896 12.0, 12.288, 16.8, or 19.2		MHz
2	$t_{w(CLKINH)}$	Pulse duration, CLKIN high	0.466 * $t_{c(CLKIN)}$			ns
3	$t_{w(CLKINL)}$	Pulse duration, CLKIN low	0.466 * $t_{c(CLKIN)}$			ns
4	$t_{t(CLKIN)}$	Transition time, CLKIN			4	ns

(1) The CLKIN frequency and PLL multiply factor should be chosen such that the resulting clock frequency is within the specific range for CPU operating frequency.
(2) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

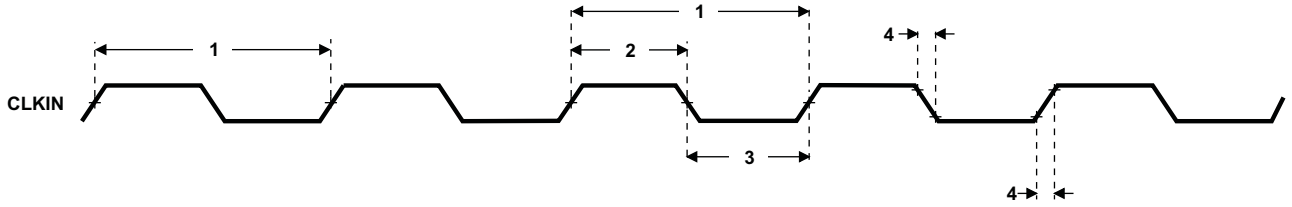


Figure 5-17. CLKIN Timing

Table 5-11. Switching Characteristics Over Recommended Operating Conditions for CLKOUT [I/O = 3.3/2.75 V](1) (2) (see Figure 5-18)

NO.	PARAMETER		CV_{DD} = 1.05/1.3/1.4 V V_{DDA_PLL} = 1.3 V		UNIT
			MIN	MAX	
1	$t_{c(CLKOUT)}$	Cycle time, CLKOUT	10		ns
2	$t_{w(CLKOUTH)}$	Pulse duration, CLKOUT high	0.466 * $t_{c(CLKOUT)}$		ns
3	$t_{w(CLKOUTL)}$	Pulse duration, CLKOUT low	0.466 * $t_{c(CLKOUT)}$		ns
4	$t_{t(CLKOUTR)}$	Transition time (rise), CLKOUT		5	ns
5	$t_{t(CLKOUTF)}$	Transition time (fall), CLKOUT		5	ns

(1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
(2) P = 1/SYSCLK clock frequency in nanoseconds (ns). For example, when SYSCLK frequency is 100 MHz, use P = 10 ns.

Table 5-12. Switching Characteristics Over Recommended Operating Conditions for CLKOUT [I/O = 1.8 V](1) (2) (see Figure 5-18)

NO.	PARAMETER		CV_{DD} = 1.05/1.3/1.4 V V_{DDA_PLL} = 1.3 V		UNIT
			MIN	MAX	
1	$t_{c(CLKOUT)}$	Cycle time, CLKOUT	20		ns
2	$t_{w(CLKOUTH)}$	Pulse duration, CLKOUT high	0.466 * $t_{c(CLKOUT)}$		ns
3	$t_{w(CLKOUTL)}$	Pulse duration, CLKOUT low	0.466 * $t_{c(CLKOUT)}$		ns
4	$t_{t(CLKOUTR)}$	Transition time (rise), CLKOUT		5	ns
5	$t_{t(CLKOUTF)}$	Transition time (fall), CLKOUT		5	ns

(1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
(2) P = 1/SYSCLK clock frequency in nanoseconds (ns). For example, when SYSCLK frequency is 100 MHz, use P = 10 ns.

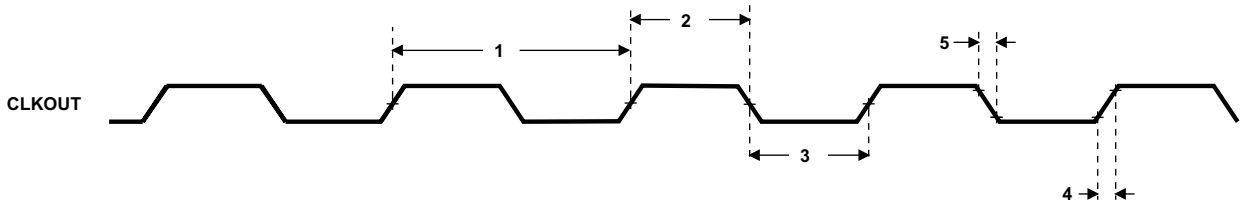


Figure 5-18. CLKOUT Timing

5.7.4.5 Wake-up Events, Interrupts, and XF

The device has a number of interrupts to service the needs of its peripherals. The interrupts can be selectively enabled or disabled.

5.7.4.5.1 Interrupts Electrical Data and Timing

Table 5-13. Timing Requirements for Interrupts(1) (see Figure 5-19)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V CV_{DD} = 1.4 V		UNIT
			MIN	MAX	
1	$t_{w(INTH)}$	Pulse duration, interrupt high CPU active	2P		ns
2	$t_{w(INTL)}$	Pulse duration, interrupt low CPU active	2P		ns

(1) P = 1/SYSCLK clock frequency in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns. For example, when the CPU core is clocked at 175 MHz, use P = 5.71 ns.

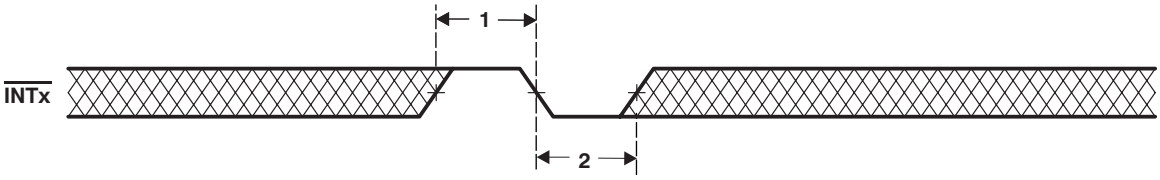


Figure 5-19. External Interrupt Timings

5.7.4.5.2 Wake-Up From IDLE Electrical Data and Timing

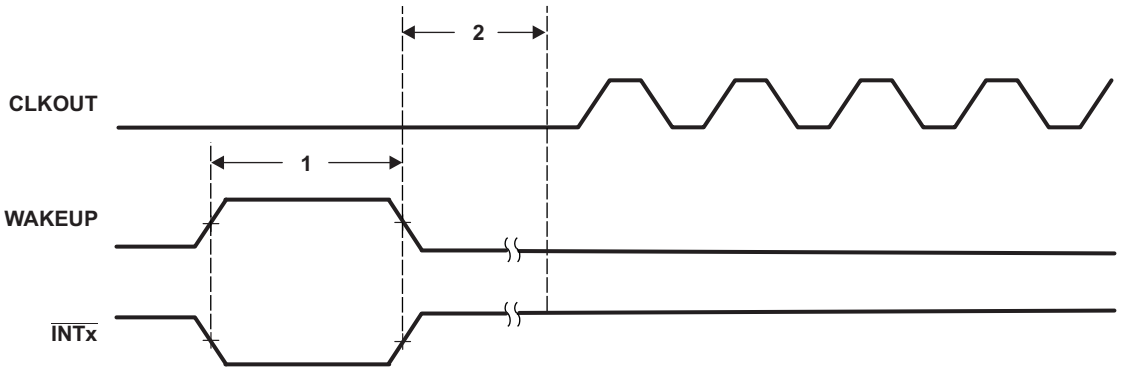
Table 5-14. Timing Requirements for Wake-Up From IDLE (see Figure 5-20)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V CV_{DD} = 1.4 V		UNIT
			MIN	MAX	
1	$t_{w(WKPL)}$	Pulse duration, WAKEUP or $\overline{INTx}$ low, SYSCLKDIS = 1	30.5		µs

Table 5-15. Switching Characteristics Over Recommended Operating Conditions For Wake-Up From IDLE(1)(2)(3)(4) (see Figure 5-20)

NO.	PARAMETER			CV_{DD} = 1.05 V CV_{DD} = 1.3 V CV_{DD} = 1.4 V			UNIT
				MIN	TYP	MAX	
2	$t_{d(WKEVTH-CKLGEN)}$	Delay time, WAKEUP pulse complete to CPU active	IDLE3 Mode(5) with SYSCLKDIS = 1, WAKEUP or $\overline{INTx}$ event, CLK_SEL = 1	D			ns
			IDLE3 Mode(5) with SYSCLKDIS = 1, WAKEUP or $\overline{INTx}$ event, CLK_SEL = 0	C			ns
			IDLE2 Mode(5); $\overline{INTx}$ event	3P			ns

(1) D = 1/ External Clock Frequency (CLKIN).
(2) C = 1/RTCCLK= 30.5 µs. RTCCLK is the clock output of the 32.768-kHz RTC oscillator.
(3) P = 1/SYSCLK clock frequency in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(4) Assumes the internal LDOs are used with a 0.1uF bandgap capacitor.
(5) For a description of IDLE2 and IDLE3 mode, see the *System* chapter in the *TMS320C5517 Digital Signal Processor Technical Reference Manual* [literature number SPRUH16].



A. INT[1:0] can only be used as a wake-up event for IDLE3 and IDLE2 modes. For a description of IDLE2 and IDLE3 mode, see the *System* chapter in the *TMS320C5517 Digital Signal Processor Technical Reference Manual* [literature number SPRUH16].
B. RTC interrupt (internal signal) can be used as wake-up event for IDLE3 and IDLE2 modes.
C. Any unmasked interrupt can be used to exit the IDLE2 mode.
D. CLKOUT reflects either the CPU clock, SAR, USB PHY, or PLL clock dependent on the setting of the CLOCKOUT Clock Source Register. For this diagram, CLKOUT refers to the CPU clock.

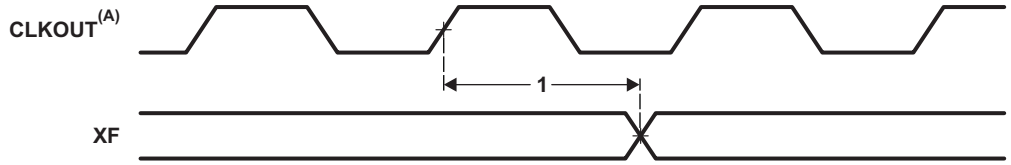
Figure 5-20. Wake-Up From IDLE Timings

5.7.4.5.3 XF Electrical Data and Timing

Table 5-16. Switching Characteristics Over Recommended Operating Conditions For XF(1) (2) (see Figure 5-21)

NO.	PARAMETER		CV_{DD} = 1.05 V CV_{DD} = 1.3 V CV_{DD} = 1.4 V		UNIT
			MIN	MAX	
1	$t_{d(XF)}$	Delay time, CLKOUT high to XF high	0	10.2	ns

(1) P = 1/SYSCLK clock frequency in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) C = 1/RTCCLK= 30.5 µs. RTCCLK is the clock output of the 32.768-kHz RTC oscillator.



A. CLKOUT reflects either the CPU clock, SAR, USB PHY, or PLL clock dependent on the setting of the CLOCKOUT Clock Source Register. For this diagram, CLKOUT refers to the CPU clock.

Figure 5-21. XF Timings

5.7.5 Direct Memory Access (DMA) Controller

The DMA controller is used to move data among internal memory, external memory, and peripherals without intervention from the CPU and in the background of CPU operation.

The DSP includes a total of four DMA controllers. Aside from the DSP resources they can access, all four DMA controllers are identical.

The DMA controller has the following features:

- Operation that is independent of the CPU.
- Four channels, which allow the DMA controller to keep track of the context of four independent block transfers.
- Event synchronization. DMA transfers in each channel can be made dependent on the occurrence of selected events.
- An interrupt for each channel. Each channel can send an interrupt to the CPU on completion of the programmed transfer.
- Ping-Pong mode allows the DMA controller to keep track of double buffering context without CPU intervention.
- A dedicated clock idle domain. The four device DMA controllers can be put into a low-power state by independently turning off their input clocks.

5.7.5.1 DMA Channel Synchronization Events

The DMA controllers allow activity in their channels to be synchronized to selected events. The DSP supports 20 separate synchronization events and each channel can be tied to separate sync events independent of the other channels. Synchronization events are selected by programming the CHnEVT field in the DMAn channel event source registers (DMAnCESR1 and DMAnCESR2).

5.7.6 External Memory Interface (EMIF)

The device supports several memories and external device interfaces, including: NOR Flash, NAND Flash, SRAM, Non-Mobile SDRAM, and Mobile SDRAM (mSDRAM).

Note: The device can support non-mobile SDRAM under certain circumstances. The device also always uses mobile SDRAM initialization, but it is able to support SDRAM memories that ignore the BA0 and BA1 pins for the 'load mode register' command. During the mobile SDRAM initialization, the device issues the 'load mode register' initialization command to two different addresses that differ in only the BA0 and BA1 address bits. These registers are the Extended Mode register and the Mode register. The Extended mode register exists only in mSDRAM and not in non-mSDRAM. If a non-mobile SDRAM memory ignores bits BA0 and BA1, the second loaded register value overwrites the first, leaving the desired value in the Mode register and the non-mobile SDRAM will work with the device.

The EMIF provides an 8-bit or 16-bit data bus, an address bus width up to 21 bits, and 6 chip selects, along with memory control signals.

The EM_A[20:15] address signals are multiplexed with the GPIO peripheral and controlled by the External Bus Selection Register (EBSR). For more detail on the pin muxing, see Section 5.7.3.5.1, *External Bus Selection Register (EBSR)*.

5.7.6.1 EMIF Asynchronous Memory Support

The EMIF supports asynchronous:

- SRAM memories
- NAND Flash memories
- NOR Flash memories

The EMIF data bus can be configured for both 8- or 16-bit width. The device supports up to 21 address lines and four external wait and interrupt inputs. Up to four asynchronous chip selects are supported by EMIF (EM_CS[5:2]).

Each chip select has the following individually programmable attributes:

- Data bus width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turn around time
- Select Strobe Option
- NAND flash controller supports 1-bit and 4-bit ECC calculation on blocks of 512 bytes

Each chip select shares the following programmable attribute: Extended Wait Option with Programmable Timeout.

5.7.6.2 EMIF Non-Mobile and Mobile Synchronous DRAM Memory Supported

The EMIF supports 16-bit non-mobile and mobile single data rate (SDR) SDRAM in addition to the asynchronous memories listed in Section 5.7.6.1, *EMIF Asynchronous Memory Support*. The supported SDRAM and mobile SDRAM configurations are:

- One, two, and four bank SDRAM and mSDRAM devices
- Supports devices with eight, nine, ten, and eleven column addresses
- CAS latency of two or three clock cycles
- 16-bit data-bus width
- 3.3-, 2.75-, and 1.8 -V LVCMOS interface that is separate from the rest of the chip I/Os.
- One (EM_CS0) or two (EM_CS[1:0]) chip selects

Additionally, the SDRAM and mSDRAM interface of EMIF supports placing the SDRAM and mSDRAM in "Self-Refresh" and "Powerdown Modes". Self-Refresh mode allows the SDRAM and mSDRAM to be put into a low-power state while still retaining memory contents; since the SDRAM and mSDRAM will continue to refresh itself even without clocks from the DSP. Powerdown mode achieves even lower power, except the DSP must periodically wake the SDRAM and mSDRAM up and issue refreshes if data retention is required. To achieve the lowest power consumption, the SDRAM and mSDRAM interface has configurable slew rate on the EMIF pins.

The device has limitations to the clock frequency on the EM_SDCLK pin based on the CV_{DD} and DV_{DDEMIF}:

- The clock frequency on the EM_SDCLK pin can be configured either as SYSCLK (DSP operating frequency) or SYSCLK/2 via bit 0 of the ECDR Register (1C26h).
- When CV_{DD} = 1.3 V or 1.4 V, and DV_{DDEMIF} = 3.3 V or 2.75 V, the max clock frequency on the EM_SDCLK pin is limited to 100 MHz (EM_SDCLK = 100 MHz). Therefore, if SYSCLK ≤ 100 MHz, the EM_SDCLK can be configured either as SYSCLK or SYSCLK/2. If SYSCLK > 100 MHz, the EM_SDCLK must be configured as SYSCLK/2 and ≤ 100 MHz.
- When CV_{DD} =1.05 V, and DV_{DDEMIF} = 3.3 V or 2.75 V, the max clock frequency on the EM_SDCLK pin is limited to 75 MHz (EM_SDCLK = 75 MHz). Therefore, if SYSCLK ≤ 75 MHz, the EM_SDCLK can be configured as either SYSCLK or SYSCLK/2. If SYSCLK > 75 MHz, the EM_SDCLK must be configured as SYSCLK/2 and ≤ 75 MHz.
- When DV_{DDEMIF} = 1.8 V, regardless of the CV_{DD} voltage, the clock frequency on the EM_SDCLK pin must be configured as SYSCLK/2 and ≤ 50 MHz.

5.7.6.3 EMIF Electrical Data and Timing CV_{DD} = 1.05 V, DV_{DDEMIF} = 3.3/2.75/1.8 V

Table 5-17. Timing Requirements for EMIF SDRAM and mSDRAM Interface(1) (see Figure 5-22 and Figure 5-23)

NO.			CV_{DD} = 1.05 V DV_{DDEMIF} = 3.3/2.75 V		CV_{DD} = 1.05 V DV_{DDEMIF} = 1.8 V		UNIT
			MIN	MAX	MIN	MAX	
19	$t_{su(DV-CLKH)}$	Input setup time, read data valid on EM_D[15:0] before EM_SDCLK rising	4.07		5.86		ns
20	$t_{h(CLKH-DIV)}$	Input hold time, read data valid on EM_D[15:0] after EM_SDCLK rising	2.1		2.6		ns

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.

Table 5-18. Switching Characteristics Over Recommended Operating Conditions for EMIF SDRAM and mSDRAM Interface(1)(2) (see Figure 5-22 and Figure 5-23)

NO.	PARAMETER		CV_{DD} = 1.05 V DV_{DDEMIF} = 3.3/2.75 V			CV_{DD} = 1.05 V DV_{DDEMIF} = 1.8 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
1	$t_{c(CLK)}$	Cycle time, EMIF clock EM_SDCLK	13.33(3)			20(4)			ns
2	$t_{w(CLK)}$	Pulse duration, EMIF clock EM_SDCLK high or low		6.67			10		ns
3	$t_{d(CLKH-CSV)}$	Delay time, EM_SDCLK rising to EMA_CS[1:0] valid	1.1		10.67	1.1		13.46	ns
5	$t_{d(CLKH-DQMV)}$	Delay time, EM_SDCLK rising to EM_DQM[1:0] valid	1.1		10.67	1.1		13.46	ns
7	$t_{d(CLKH-AV)}$	Delay time, EM_SDCLK rising to EM_A[20:0] and EM_BA[1:0] valid	1.1		10.67	1.1		13.46	ns
9	$t_{d(CLKH-DV)}$	Delay time, EM_SDCLK rising to EM_D[15:0] valid	1.1		10.67	1.1		13.46	ns
11	$t_{d(CLKH-RASV)}$	Delay time, EM_SDCLK rising to $\overline{\text{EM\_SDRAS}}$ valid	1.1		10.67	1.1		13.46	ns
13	$t_{d(CLKH-CASV)}$	Delay time, EM_SDCLK rising to $\overline{\text{EM\_SDCAS}}$ valid	1.1		10.67	1.1		13.46	ns
15	$t_{d(CLKH-WEV)}$	Delay time, EM_SDCLK rising to $\overline{\text{EM\_WE}}$ valid	1.1		10.67	1.1		13.46	ns
21	$t_{d(CLKH-CKEV)}$	Delay time, EM_SDCLK rising to EM_SDCKE valid	1.1		10.67	1.1		13.46	ns

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.
(2) E = SYSCLK period in ns. For example, when SYSCLK is set to 75 or 100 MHz, E = 13.33 or 10 ns, respectively. For more detail on the EM_SDCLK speed see Section 5.7.6.2, *EMIF Non-Mobile and Mobile Synchronous DRAM Memory Supported*.
(3) When CV_{DD} = 1.05 V, and DV_{DDEMIF} = 3.3 V or 2.75 V, the max clock frequency on the EM_SDCLK pin is limited to 75 MHz (EM_SDCLK = 75 MHz). For more information, see the *EMIF* chapter in the *TMS320C5517 Digital Signal Processor Technical Reference Manual* [literature number SPRUH16].
(4) When DV_{DDEMIF} = 1.8 V, the max clock frequency on the EM_SDCLK pin is limited to 50 MHz (EM_SDCLK = 50 MHz). For more information, see the *EMIF* chapter in the *TMS320C5517 Digital Signal Processor Technical Reference Manual* [literature number SPRUH16].

Table 5-19. Timing Requirements for EMIF Asynchronous Memory, DV_{DDEMIF} = 1.8 V(1)(2) (see Figure 5-24, Figure 5-26, and Figure 5-27)

NO.			CV_{DD} = 1.05 V DV_{DDEMIF} = 1.8 V			UNIT
			MIN	NOM	MAX	
READS and WRITES						
2	$t_{w(EM\_WAIT)}$	Pulse duration, EM_WAITx assertion and deassertion		2E		ns

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.
(2) E = SYSCLK period in ns. For example, when SYSCLK is set to 75 or 100 MHz, E = 13.33 or 10 ns, respectively.

Table 5-19. Timing Requirements for EMIF Asynchronous Memory, DV_{DDEMIF} = 1.8 V(1)(2) (see Figure 5-24, Figure 5-26, and Figure 5-27) (continued)

NO.			CV_{DD} = 1.05 V DV_{DDEMIF} = 1.8 V			UNIT
			MIN	NOM	MAX	
READS						
12	$t_{su(EMDV-EMOEH)}$	Setup time, EM_D[15:0] valid before $\overline{EM\_OE}$ high	18			ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EM_D[15:0] valid after $\overline{EM\_OE}$ high	0			ns
14	$t_{su\ (EMOEL-EMWAIT)}$	Setup time, EM_WAITx asserted before end of Strobe Phase(3)	4E + 18			ns
WRITES						
28	$t_{su\ (EMWEL-EMWAIT)}$	Setup time, EM_WAITx asserted before end of Strobe Phase(3)	4E + 18			ns

(3) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAITx must be asserted to add extended wait states. Figure 5-26 and Figure 5-27 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 5-20. Timing Requirements for EMIF Asynchronous Memory, DV_{DDEMIF} = 3.3/2.75 V(1)(2) (see Figure 5-24, Figure 5-26, and Figure 5-27)

NO.			CV_{DD} = 1.05 V DV_{DDEMIF} = 3.3/2.75 V			UNIT
			MIN	NOM	MAX	
READS and WRITES						
2	$t_{w(EM\_WAIT)}$	Pulse duration, EM_WAITx assertion and deassertion	2E			ns
READS						
12	$t_{su(EMDV-EMOEH)}$	Setup time, EM_D[15:0] valid before $\overline{EM\_OE}$ high	17			ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EM_D[15:0] valid after $\overline{EM\_OE}$ high	0			ns
14	$t_{su\ (EMOEL-EMWAIT)}$	Setup time, EM_WAITx asserted before end of Strobe Phase(3)	4E + 17			ns
WRITES						
28	$t_{su\ (EMWEL-EMWAIT)}$	Setup time, EM_WAITx asserted before end of Strobe Phase(3)	4E + 17			ns

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.
(2) E = SYSCLK period in ns. For example, when SYSCLK is set to 75 or 100 MHz, E = 13.33 or 10 ns, respectively.
(3) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAITx must be asserted to add extended wait states. Figure 5-26 and Figure 5-27 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 5-21. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory, DV_{DDEMIF} = 1.8 V(1)(2) (3) (see Figure 5-25 and Figure 5-27)(4)

NO.	PARAMETER		CV_{DD} = 1.05 V DV_{DDEMIF} = 1.8 V			UNIT
			MIN	TYP	MAX	
READS and WRITES						
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E - 18	(TA)*E	(TA)*E + 18	ns
READS						
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E - 18	(RS+RST+RH)*E	(RS+RST+RH)*E + 18	ns
		EMIF read cycle time (EW = 1)	(RS+RST+RH+(EWC*16))*E - 18	(RS+RST+RH+(EWC*16))*E	(RS+RST+RH+(EWC*16))*E + 18	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_OE}$ low (SS = 0)	(RS)*E - 11	(RS)*E	(RS)*E + 11	ns
		Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_OE}$ low (SS = 1)	-11	0	+11	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{EM\_OE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 0)	(RH)*E - 11	(RH)*E	(RH)*E + 11	ns
		Output hold time, $\overline{EM\_OE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 1)	-11	0	+11	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_BA[1:0] valid to $\overline{EM\_OE}$ low	(RS)*E - 11	(RS)*E	(RS)*E + 11	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, $\overline{EM\_OE}$ high to EM_BA[1:0] invalid	(RH)*E - 18	(RH)*E	(RH)*E + 18	ns
8	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_A[20:0] valid to $\overline{EM\_OE}$ low	(RS)*E - 11	(RS)*E	(RS)*E + 11	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, $\overline{EM\_OE}$ high to EM_A[20:0] invalid	(RH)*E - 18	(RH)*E	(RH)*E + 18	ns
10	$t_{w(EMOEL)}$	$\overline{EM\_OE}$ active low pulse (EW = 0)	(RST)*E - 18	(RST)*E	(RST)*E + 18	ns
		$\overline{EM\_OE}$ active low pulse (EW = 1)	(RST+(EWC*16))*E - 18	(RST+(EWC*16))*E	(RST+(EWC*16))*E + 11	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EM_WAITx deasserted to $\overline{EM\_OE}$ high	4E - 18	4E	4E + 18	ns
WRITES						
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)*E - 18	(WS+WST+WH)*E	(WS+WST+WH)*E + 18	ns
		EMIF write cycle time (EW = 1)	(WS+WST+WH+(EWC*16))*E - 18	(WS+WST+WH+(EWC*16))*E	(WS+WST+WH+(EWC*16))*E + 18	ns
16	$t_{su(EMCSL-EMWEL)}$	Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_WE}$ low (SS = 0)	(WS)*E - 18	(WS)*E	(WS)*E + 18	ns
		Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_WE}$ low (SS = 1)	-18	0	+18	ns
17	$t_{h(EMWEH-EMCSH)}$	Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 0)	(WH)*E - 11	(WH)*E	(WH)*E + 11	ns
		Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 1)	-11	0	+11	ns
18	$t_{su(EMBAV-EMWEL)}$	Output setup time, EM_BA[1:0] valid to $\overline{EM\_WE}$ low	(WS)*E - 11	(WS)*E	(WS)*E + 11	ns
19	$t_{h(EMWEH-EMBAIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_BA[1:0] invalid	(WH)*E - 11	(WH)*E	(WH)*E + 11	ns
20	$t_{su(EMAV-EMWEL)}$	Output setup time, EM_A[20:0] valid to $\overline{EM\_WE}$ low	(WS)*E - 11	(WS)*E	(WS)*E + 11	ns
21	$t_{h(EMWEH-EMAIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_A[20:0] invalid	(WH)*E - 11	(WH)*E	(WH)*E + 11	ns

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.
(2) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Configuration and Asynchronous Wait Cycle Configuration Registers.
(3) E = SYSCLK period in ns. For example, when SYSCLK is set to 75 or 100 MHz, E = 13.33 or 10 ns, respectively.
(4) EWC = external wait cycles determined by EM_WAITx input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register.

Table 5-21. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory, DV_{DDEMIF} = 1.8 V(1)(2) (3) (see Figure 5-25 and Figure 5-27)(4) (continued)

NO.	PARAMETER		CV_{DD} = 1.05 V DV_{DDEMIF} = 1.8 V			UNIT
			MIN	TYP	MAX	
22	$t_{w(EMWEL)}$	$\overline{EM\_WE}$ active low pulse (EW = 0)	(WST)*E - 18	(WST)*E	(WST)*E + 18	ns
		$\overline{EM\_WE}$ active low pulse (EW = 1)	(WST+(EWC*16))*E - 18	(WST+(EWC*16))*E	(WST+(EWC*16))*E + 18	ns
23	$t_{d(EMWAITH-EMWEH)}$	Delay time from EM_WAITx deasserted to $\overline{EM\_WE}$ high	3E - 18	4E	4E + 18	ns
24	$t_{su(EMDV-EMWEL)}$	Output setup time, EM_D[15:0] valid to $\overline{EM\_WE}$ low	(WS)*E - 18	(WS)*E	(WS)*E + 18	ns
25	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_D[15:0] invalid	(WH)*E - 11	(WH)*E	(WH)*E + 11	ns

Table 5-22. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory, DV_{DDEMIF} = 3.3/2.75 V(1)(2) (3) (see Figure 5-25 and Figure 5-27)(4)

NO.	PARAMETER		CV_{DD} = 1.05 V DV_{DDEMIF} = 3.3/2.75 V			UNIT
			MIN	TYP	MAX	
READS and WRITES						
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E - 17	(TA)*E	(TA)*E + 17	ns
READS						
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E - 17	(RS+RST+RH)*E	(RS+RST+RH)*E + 17	ns
		EMIF read cycle time (EW = 1)	(RS+RST+RH+(EWC*16))*E - 17	(RS+RST+RH+(EWC*16))*E	(RS+RST+RH+(EWC*16))*E + 17	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_OE}$ low (SS = 0)	(RS)*E - 9	(RS)*E	(RS)*E + 9	ns
		Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_OE}$ low (SS = 1)	-9	0	+9	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{EM\_OE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 0)	(RH)*E - 9	(RH)*E	(RH)*E + 9	ns
		Output hold time, $\overline{EM\_OE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 1)	-9	0	+9	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_BA[1:0] valid to $\overline{EM\_OE}$ low	(RS)*E - 9	(RS)*E	(RS)*E + 9	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, $\overline{EM\_OE}$ high to EM_BA[1:0] invalid	(RH)*E - 17	(RH)*E	(RH)*E + 17	ns
8	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_A[20:0] valid to $\overline{EM\_OE}$ low	(RS)*E - 9	(RS)*E	(RS)*E + 9	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, $\overline{EM\_OE}$ high to EM_A[20:0] invalid	(RH)*E - 17	(RH)*E	(RH)*E + 17	ns
10	$t_{w(EMOEL)}$	$\overline{EM\_OE}$ active low pulse (EW = 0)	(RST)*E - 17	(RST)*E	(RST)*E + 17	ns
		$\overline{EM\_OE}$ active low pulse (EW = 1)	(RST+(EWC*16))*E - 17	(RST+(EWC*16))*E	(RST+(EWC*16))*E + 9	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EM_WAITx deasserted to $\overline{EM\_OE}$ high	4E - 17	4E	4E + 17	ns
WRITES						
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)*E - 17	(WS+WST+WH)*E	(WS+WST+WH)*E + 17	ns
		EMIF write cycle time (EW = 1)	(WS+WST+WH+(EWC*16))*E - 17	(WS+WST+WH+(EWC*16))*E	(WS+WST+WH+(EWC*16))*E + 17	ns
16	$t_{su(EMCSL-EMWEL)}$	Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_WE}$ low (SS = 0)	(WS)*E - 17	(WS)*E	(WS)*E + 17	ns
		Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_WE}$ low (SS = 1)	-17	0	+17	ns
17	$t_{h(EMWEH-EMCSH)}$	Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 0)	(WH)*E - 9	(WH)*E	(WH)*E + 9	ns
		Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 1)	-9	0	+9	ns
18	$t_{su(EMBAV-EMWEL)}$	Output setup time, EM_BA[1:0] valid to $\overline{EM\_WE}$ low	(WS)*E - 9	(WS)*E	(WS)*E + 9	ns
19	$t_{h(EMWEH-EMBAIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_BA[1:0] invalid	(WH)*E - 9	(WH)*E	(WH)*E + 9	ns
20	$t_{su(EMAV-EMWEL)}$	Output setup time, EM_A[20:0] valid to $\overline{EM\_WE}$ low	(WS)*E - 9	(WS)*E	(WS)*E + 9	ns
21	$t_{h(EMWEH-EMAIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_A[20:0] invalid	(WH)*E - 9	(WH)*E	(WH)*E + 9	ns

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.
(2) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Configuration and Asynchronous Wait Cycle Configuration Registers.
(3) E = SYSCLK period in ns. For example, when SYSCLK is set to 75 or 100 MHz, E = 13.33 or 10 ns, respectively.
(4) EWC = external wait cycles determined by EM_WAITx input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register.

Table 5-22. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory, DV_{DDEMIF} = 3.3/2.75 V(1)(2) (3) (see Figure 5-25 and Figure 5-27)(4) (continued)

NO.	PARAMETER		CV_{DD} = 1.05 V DV_{DDEMIF} = 3.3/2.75 V			UNIT
			MIN	TYP	MAX	
22	$t_{w(EMWEL)}$	$\overline{EM\_WE}$ active low pulse (EW = 0)	(WST)*E - 17	(WST)*E	(WST)*E + 17	ns
		$\overline{EM\_WE}$ active low pulse (EW = 1)	(WST+(EWC*16))*E - 17	(WST+(EWC*16))*E	(WST+(EWC*16))*E + 17	ns
23	$t_{d(EMWAITH-EMWEH)}$	Delay time from EM_WAITx deasserted to $\overline{EM\_WE}$ high	3E - 17	4E	4E + 17	ns
24	$t_{su(EMDV-EMWEL)}$	Output setup time, EM_D[15:0] valid to $\overline{EM\_WE}$ low	(WS)*E - 17	(WS)*E	(WS)*E + 17	ns
25	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_D[15:0] invalid	(WH)*E - 9	(WH)*E	(WH)*E + 9	ns

5.7.6.4 EMIF Electrical Data and Timing CV_{DD} = 1.3/1.4 V, DV_{DDEMIF} = 3.3/2.75/1.8 V

Table 5-23. Timing Requirements for EMIF SDRAM and mSDRAM Interface(1) (see Figure 5-22 and Figure 5-23)

NO.			CV_{DD} = 1.3/1.4 V DV_{DDEMIF} = 3.3/2.75 V		CV_{DD} = 1.3/1.4 V DV_{DDEMIF} = 1.8 V		UNIT
			MIN	MAX	MIN	MAX	
19	$t_{su(DV-CLKH)}$	Input setup time, read data valid on EM_D[15:0] before EM_SDCLK rising	4.07		3.28		ns
20	$t_{h(CLKH-DIV)}$	Input hold time, read data valid on EM_D[15:0] after EM_SDCLK rising	2.1		3.1		ns

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.

Table 5-24. Switching Characteristics Over Recommended Operating Conditions for EMIF SDRAM and mSDRAM Interface(1)(2) (see Figure 5-22 and Figure 5-23)

NO.	PARAMETER		CV_{DD} = 1.3/1.4 V DV_{DDEMIF} = 3.3/2.75 V			CV_{DD} = 1.3/1.4 V DV_{DDEMIF} = 1.8 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
1	$t_{c(CLK)}$	Cycle time, EMIF clock EM_SDCLK	10(3)			20(4)			ns
2	$t_{w(CLK)}$	Pulse duration, EMIF clock EM_SDCLK high or low		5			10		ns
3	$t_{d(CLKH-CSV)}$	Delay time, EM_SDCLK rising to EMA_CS[1:0] valid	0.9		7.88	1.1		10.67	ns
5	$t_{d(CLKH-DQMV)}$	Delay time, EM_SDCLK rising to EM_DQM[1:0] valid	0.9		7.88	1.1		10.67	ns
7	$t_{d(CLKH-AV)}$	Delay time, EM_SDCLK rising to EM_A[20:0] and EM_BA[1:0] valid	0.9		7.88	1.1		10.67	ns
9	$t_{d(CLKH-DV)}$	Delay time, EM_SDCLK rising to EM_D[15:0] valid	0.9		7.88	1.1		10.67	ns
11	$t_{d(CLKH-RASV)}$	Delay time, EM_SDCLK rising to $\overline{\text{EM\_SDRAS}}$ valid	0.9		7.88	1.1		10.67	ns
13	$t_{d(CLKH-CASV)}$	Delay time, EM_SDCLK rising to $\overline{\text{EM\_SDCAS}}$ valid	0.9		7.88	1.1		10.67	ns
15	$t_{d(CLKH-WEV)}$	Delay time, EM_SDCLK rising to $\overline{\text{EM\_WE}}$ valid	0.9		7.88	1.1		10.67	ns
21	$t_{d(CLKH-CKEV)}$	Delay time, EM_SDCLK rising to EM_SDCKE valid	0.9		7.88	1.1		10.67	ns

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.
(2) E = SYSCLK period in ns. For example, when SYSCLK is set to 75 or 100 MHz, E = 13.33 or 10 ns, respectively. For more detail on the EM_SDCLK speed see Section 5.7.6.2, *EMIF Non-Mobile and Mobile Synchronous DRAM Memory Supported*.
(3) The maximum clock frequency on the EM_SDCLK pin is limited to 100 MHz (EM_SDCLK = 100 MHz). For more information, see the *EMIF* chapter in the *TMS320C5517 Digital Signal Processor Technical Reference Manual* [literature number SPRUH16].
(4) When DV_{DDEMIF} = 1.8 V, the max clock frequency on the EM_SDCLK pin is limited to 50 MHz (EM_SDCLK = 50 MHz). For more information, see the *EMIF* chapter in the *TMS320C5517 Digital Signal Processor Technical Reference Manual* [literature number SPRUH16].

Table 5-25. Timing Requirements for EMIF Asynchronous Memory, DV_{DDEMIF} = 1.8 V (1) (2) (see Figure 5-24, Figure 5-26, and Figure 5-27)

NO.			CV_{DD} = 1.3/1.4 V DV_{DDEMIF} = 1.8 V			UNIT
			MIN	NOM	MAX	
READS and WRITES						
2	$t_{w(EM\_WAIT)}$	Pulse duration, EM_WAITx assertion and deassertion	2E			ns
READS						
12	$t_{su(EMDV-EMOEH)}$	Setup time, EM_D[15:0] valid before $\overline{EM\_OE}$ high	11			ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EM_D[15:0] valid after $\overline{EM\_OE}$ high	0			ns
14	$t_{su\ (EMOEL-EMWAIT)}$	Setup Time, EM_WAITx asserted before end of Strobe Phase (3)	4E + 10			ns
WRITES						
28	$t_{su\ (EMWEL-EMWAIT)}$	Setup Time, EM_WAITx asserted before end of Strobe Phase (3)	4E + 10			ns

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.
(2) E = SYSCLK period in ns. For example, when SYSCLK is set to 75 or 100 MHz, E = 13.33 or 10 ns, respectively.
(3) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAITx must be asserted to add extended wait states. Figure 5-26 and Figure 5-27 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 5-26. Timing Requirements for EMIF Asynchronous Memory, DV_{DDEMIF} = 3.3/2.75 V(1)(2) (see Figure 5-24, Figure 5-26, and Figure 5-27)

NO.			CV_{DD} = 1.3/1.4 V DV_{DDEMIF} = 3.3/2.75 V			UNIT
			MIN	NOM	MAX	
READS and WRITES						
2	$t_{w(EM\_WAIT)}$	Pulse duration, EM_WAITx assertion and deassertion	2E			ns
READS						
12	$t_{su(EMDV-EMOEH)}$	Setup time, EM_D[15:0] valid before $\overline{EM\_OE}$ high	11			ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EM_D[15:0] valid after $\overline{EM\_OE}$ high	0			ns
14	$t_{su\ (EMOEL-EMWAIT)}$	Setup Time, EM_WAITx asserted before end of Strobe Phase(3)	4E + 9			ns
WRITES						
28	$t_{su\ (EMWEL-EMWAIT)}$	Setup Time, EM_WAITx asserted before end of Strobe Phase(3)	4E + 9			ns

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.
(2) E = SYSCLK period in ns. For example, when SYSCLK is set to 75 or 200 MHz, E = 13.33 or 5 ns, respectively.
(3) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAITx must be asserted to add extended wait states. Figure 5-26 and Figure 5-27 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 5-27. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory, DV_{DDEMIF} = 1.8 V(1)(2) (3) (4) (see Figure 5-24, Figure 5-26, and Figure 5-27)

NO.	PARAMETER		CV_{DD} = 1.3/1.4 V DV_{DDEMIF} = 1.8 V			UNIT
			MIN	TYP	MAX	
READS and WRITES						
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E - 10	(TA)*E	(TA)*E + 10	ns
READS						
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E - 10	(RS+RST+RH)*E	(RS+RST+RH)*E + 10	ns
		EMIF read cycle time (EW = 1)	(RS+RST+RH+(EWC*16))*E - 10	(RS+RST+RH+(EWC*16))*E	(RS+RST+RH+(EWC*16))*E + 10	ns
4	$t_{su(EMCSL-EMOEL)}$	Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_OE}$ low (SS = 0)	(RS)*E - 4	(RS)*E	(RS)*E + 4	ns
		Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_OE}$ low (SS = 1)	-4	0	+4	ns
5	$t_{h(EMOEH-EMCSH)}$	Output hold time, $\overline{EM\_OE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 0)	(RH)*E - 4	(RH)*E	(RH)*E + 4	ns
		Output hold time, $\overline{EM\_OE}$ high to $\overline{EM\_CE[5:2]}$ high (SS = 1)	-4	0	+4	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_BA[1:0] valid to $\overline{EM\_OE}$ low	(RS)*E - 4	(RS)*E	(RS)*E + 4	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, $\overline{EM\_OE}$ high to EM_BA[1:0] invalid	(RH)*E - 10	(RH)*E	(RH)*E + 10	ns
8	$t_{su(EMAV-EMOEL)}$	Output setup time, EM_A[20:0] valid to $\overline{EM\_OE}$ low	(RS)*E - 4	(RS)*E	(RS)*E + 4	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, $\overline{EM\_OE}$ high to EM_A[20:0] invalid	(RH)*E - 10	(RH)*E	(RH)*E + 10	ns
10	$t_{w(EMOEL)}$	$\overline{EM\_OE}$ active low pulse (EW = 0)	(RST)*E - 10	(RST)*E	(RST)*E + 10	ns
		$\overline{EM\_OE}$ active low pulse (EW = 1)	(RST+(EWC*16))*E - 10	(RST+(EWC*16))*E	(RST+(EWC*16))*E + 10	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EM_WAITx deasserted to $\overline{EM\_OE}$ high	4E - 10	4E	4E + 10	ns
WRITES						
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)*E - 10	(WS+WST+WH)*E	(WS+WST+WH)*E + 10	ns
		EMIF write cycle time (EW = 1)	(WS+WST+WH+(EWC*16))*E - 10	(WS+WST+WH+(EWC*16))*E	(WS+WST+WH+(EWC*16))*E + 10	ns
16	$t_{su(EMCSL-EMWEL)}$	Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_WE}$ low (SS = 0)	(WS)*E - 10	(WS)*E	(WS)*E +10	ns
		Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_WE}$ low (SS = 1)	-10	0	+10	ns
17	$t_{h(EMWEH-EMCSH)}$	Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 0)	(WH)*E - 4	(WH)*E	(WH)*E + 4	ns
		Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 1)	-4	0	+4	ns
18	$t_{su(EMBAV-EMWEL)}$	Output setup time, EM_BA[1:0] valid to $\overline{EM\_WE}$ low	(WS)*E - 4	(WS)*E	(WS)*E + 4	ns
19	$t_{h(EMWEH-EMBAIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_BA[1:0] invalid	(WH)*E - 4	(WH)*E	(WH)*E + 4	ns
20	$t_{su(EMAV-EMWEL)}$	Output setup time, EM_A[20:0] valid to $\overline{EM\_WE}$ low	(WS)*E - 4	(WS)*E	(WS)*E + 4	ns
21	$t_{h(EMWEH-EMAIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_A[20:0] invalid	(WH)*E - 4	(WH)*E	(WH)*E + 4	ns

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.
(2) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Configuration and Asynchronous Wait Cycle Configuration Registers.
(3) E = SYSCLK period in ns. For example, when SYSCLK is set to 75 or 200 MHz, E = 13.33 or 5 ns, respectively.
(4) EWC = external wait cycles determined by EM_WAITx input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register.

Table 5-27. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory, DV_{DDEMIF} = 1.8 V(1)(2) (3) (4) (see Figure 5-24, Figure 5-26, and Figure 5-27) (continued)

NO.	PARAMETER		CV_{DD} = 1.3/1.4 V, DV_{DDEMIF} = 1.8 V			UNIT
			MIN	TYP	MAX	
22	$t_{w(EMWEL)}$	$\overline{EM\_WE}$ active low pulse (EW = 0)	(WST)*E - 10	(WST)*E	(WST)*E + 10	ns
		$\overline{EM\_WE}$ active low pulse (EW = 1)	(WST+(EWC*16))*E - 10	(WST+(EWC*16))*E	(WST+(EWC*16))*E + 10	ns
23	$t_{d(EMWAITH-EMWEH)}$	Delay time from EM_WAITx deasserted to $\overline{EM\_WE}$ high	3E - 10	4E	4E + 10	ns
24	$t_{su(EMDV-EMWEL)}$	Output setup time, EM_D[15:0] valid to $\overline{EM\_WE}$ low	(WS)*E - 10	(WS)*E	(WS)*E + 10	ns
25	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_D[15:0] invalid	(WH)*E - 4	(WH)*E	(WH)*E + 4	ns

Table 5-28. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory, DV_{DDEMIF} = 3.3/2.75 V(1)(2) (3) (4) (see Figure 5-24, Figure 5-26, and Figure 5-27)

NO.	PARAMETER		CV_{DD} = 1.3/1.4 V DV_{DDEMIF} = 3.3/2.75 V			UNIT
			MIN	TYP	MAX	
READS and WRITES						
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E - 9	(TA)*E	(TA)*E + 9	ns
READS						
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E - 9	(RS+RST+RH)*E	(RS+RST+RH)*E + 9	ns
		EMIF read cycle time (EW = 1)	(RS+RST+RH+(EWC*16))*E - 9	(RS+RST+RH+(EWC*16))*E	(RS+RST+RH+(EWC*16))*E + 9	ns
4	$t_{su(EMCSL-EMOEL)}$	Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_OE}$ low (SS = 0)	(RS)*E - 4	(RS)*E	(RS)*E + 4	ns
		Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_OE}$ low (SS = 1)	-4	0	+4	ns
5	$t_{h(EMOEH-EMCSH)}$	Output hold time, $\overline{EM\_OE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 0)	(RH)*E - 4	(RH)*E	(RH)*E + 4	ns
		Output hold time, $\overline{EM\_OE}$ high to $\overline{EM\_CE[5:2]}$ high (SS = 1)	-4	0	+4	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_BA[1:0] valid to $\overline{EM\_OE}$ low	(RS)*E - 4	(RS)*E	(RS)*E + 4	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, $\overline{EM\_OE}$ high to EM_BA[1:0] invalid	(RH)*E - 9	(RH)*E	(RH)*E + 9	ns
8	$t_{su(EMAV-EMOEL)}$	Output setup time, EM_A[20:0] valid to $\overline{EM\_OE}$ low	(RS)*E - 4	(RS)*E	(RS)*E + 4	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, $\overline{EM\_OE}$ high to EM_A[20:0] invalid	(RH)*E - 9	(RH)*E	(RH)*E + 9	ns
10	$t_{w(EMOEL)}$	$\overline{EM\_OE}$ active low pulse (EW = 0)	(RST)*E - 9	(RST)*E	(RST)*E + 9	ns
		$\overline{EM\_OE}$ active low pulse (EW = 1)	(RST+(EWC*16))*E - 9	(RST+(EWC*16))*E	(RST+(EWC*16))*E + 9	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EM_WAITx deasserted to $\overline{EM\_OE}$ high	4E - 9	4E	4E + 9	ns
WRITES						
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)*E - 9	(WS+WST+WH)*E	(WS+WST+WH)*E + 9	ns
		EMIF write cycle time (EW = 1)	(WS+WST+WH+(EWC*16))*E - 9	(WS+WST+WH+(EWC*16))*E	(WS+WST+WH+(EWC*16))*E + 9	ns
16	$t_{su(EMCSL-EMWEL)}$	Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_WE}$ low (SS = 0)	(WS)*E - 9	(WS)*E	(WS)*E +9	ns
		Output setup time, $\overline{EM\_CS[5:2]}$ low to $\overline{EM\_WE}$ low (SS = 1)	-9	0	+9	ns
17	$t_{h(EMWEH-EMCSH)}$	Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 0)	(WH)*E - 4	(WH)*E	(WH)*E + 4	ns
		Output hold time, $\overline{EM\_WE}$ high to $\overline{EM\_CS[5:2]}$ high (SS = 1)	-4	0	+4	ns
18	$t_{su(EMBAV-EMWEL)}$	Output setup time, EM_BA[1:0] valid to $\overline{EM\_WE}$ low	(WS)*E - 4	(WS)*E	(WS)*E + 4	ns
19	$t_{h(EMWEH-EMBAIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_BA[1:0] invalid	(WH)*E - 4	(WH)*E	(WH)*E + 4	ns
20	$t_{su(EMAV-EMWEL)}$	Output setup time, EM_A[20:0] valid to $\overline{EM\_WE}$ low	(WS)*E - 4	(WS)*E	(WS)*E + 4	ns
21	$t_{h(EMWEH-EMAIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_A[20:0] invalid	(WH)*E - 4	(WH)*E	(WH)*E + 4	ns
22	$t_{w(EMWEL)}$	$\overline{EM\_WE}$ active low pulse (EW = 0)	(WST)*E - 9	(WST)*E	(WST)*E + 9	ns
		$\overline{EM\_WE}$ active low pulse (EW = 1)	(WST+(EWC*16))*E - 9	(WST+(EWC*16))*E	(WST+(EWC*16))*E + 9	ns

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.
(2) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Configuration and Asynchronous Wait Cycle Configuration Registers.
(3) E = SYSCLK period in ns. For example, when SYSCLK is set to 75 or 200 MHz, E = 13.33 or 5 ns, respectively.
(4) EWC = external wait cycles determined by EM_WAITx input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register.

Table 5-28. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory, DV_{DDEMIF} = 3.3/2.75 V(1)(2) (3) (4) (see Figure 5-24, Figure 5-26, and Figure 5-27) (continued)

NO.	PARAMETER		CV_{DD} = 1.3/1.4 V DV_{DDEMIF} = 3.3/2.75 V			UNIT
			MIN	TYP	MAX	
23	$t_{d(EMWAITH-EMWEH)}$	Delay time from EM_WAITx deasserted to $\overline{EM\_WE}$ high	3E - 9	4E	4E + 9	ns
24	$t_{su(EMDV-EMWEL)}$	Output setup time, EM_D[15:0] valid to $\overline{EM\_WE}$ low	(WS)*E - 9	(WS)*E	(WS)*E + 9	ns
25	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EM\_WE}$ high to EM_D[15:0] invalid	(WH)*E - 4	(WH)*E	(WH)*E + 4	ns

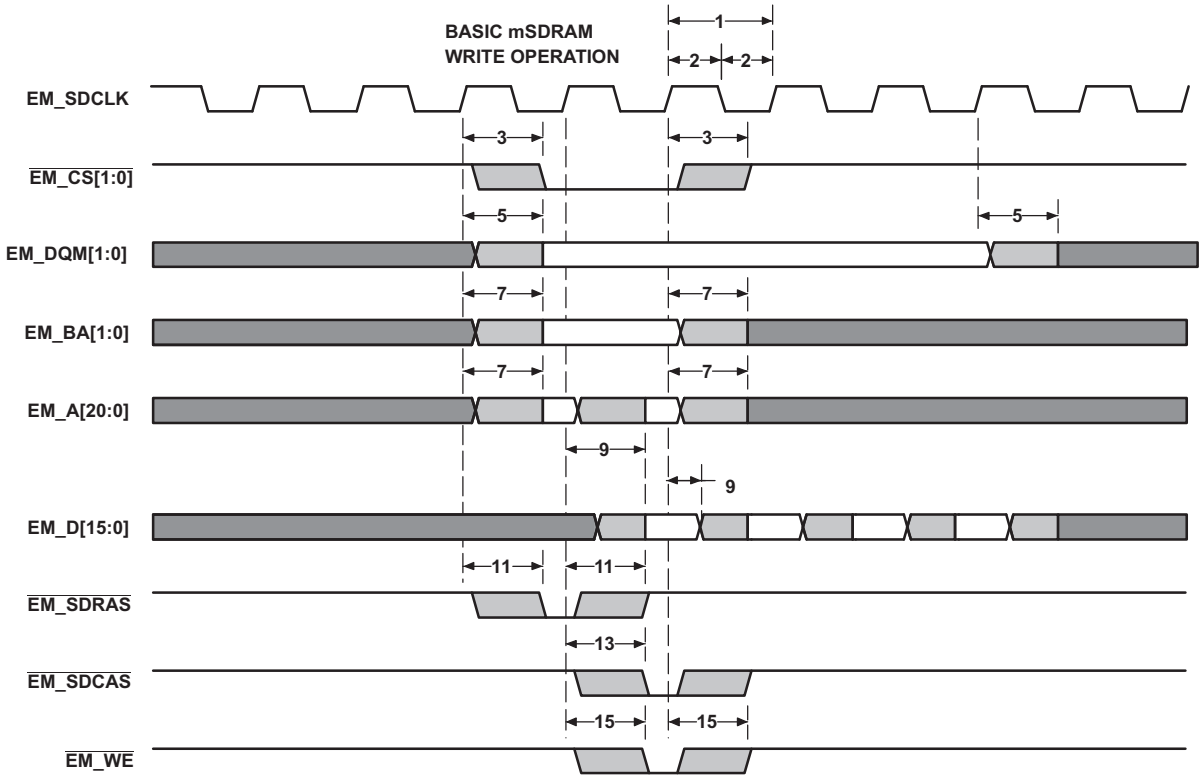


Figure 5-22. EMIF Basic SDRAM and mSDRAM Write Operation

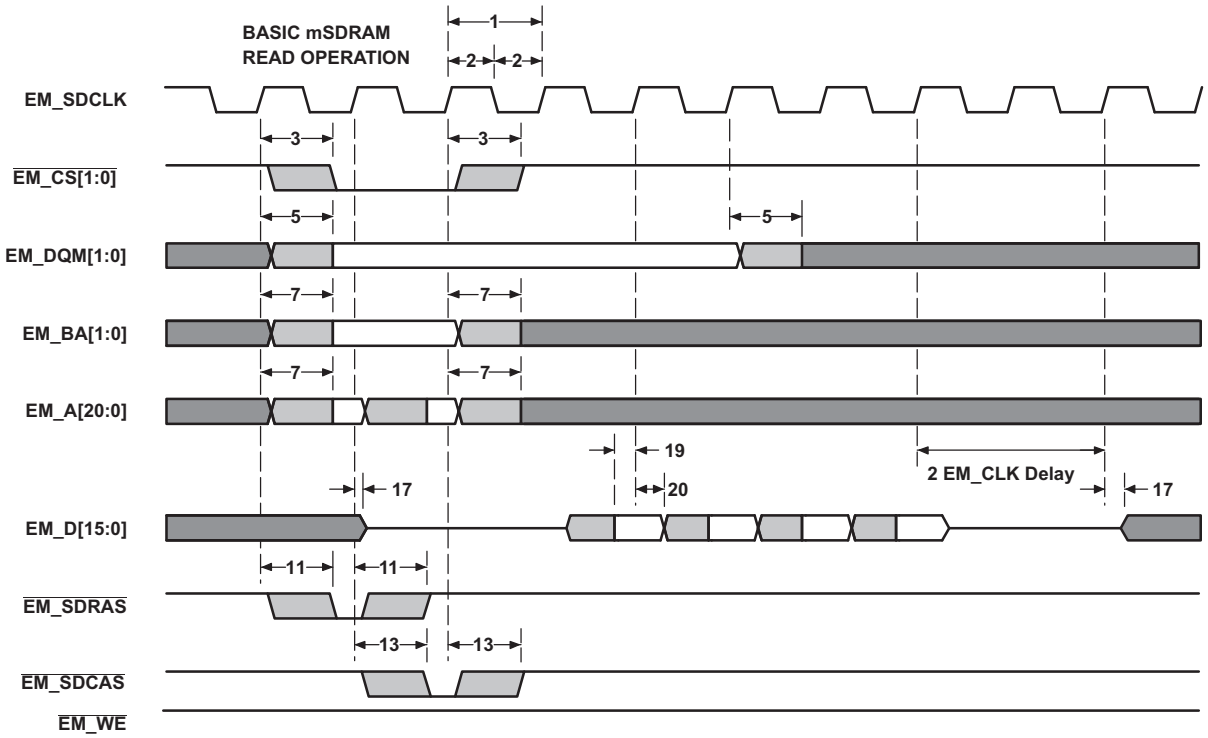


Figure 5-23. EMIF Basic SDRAM and mSDRAM Read Operation

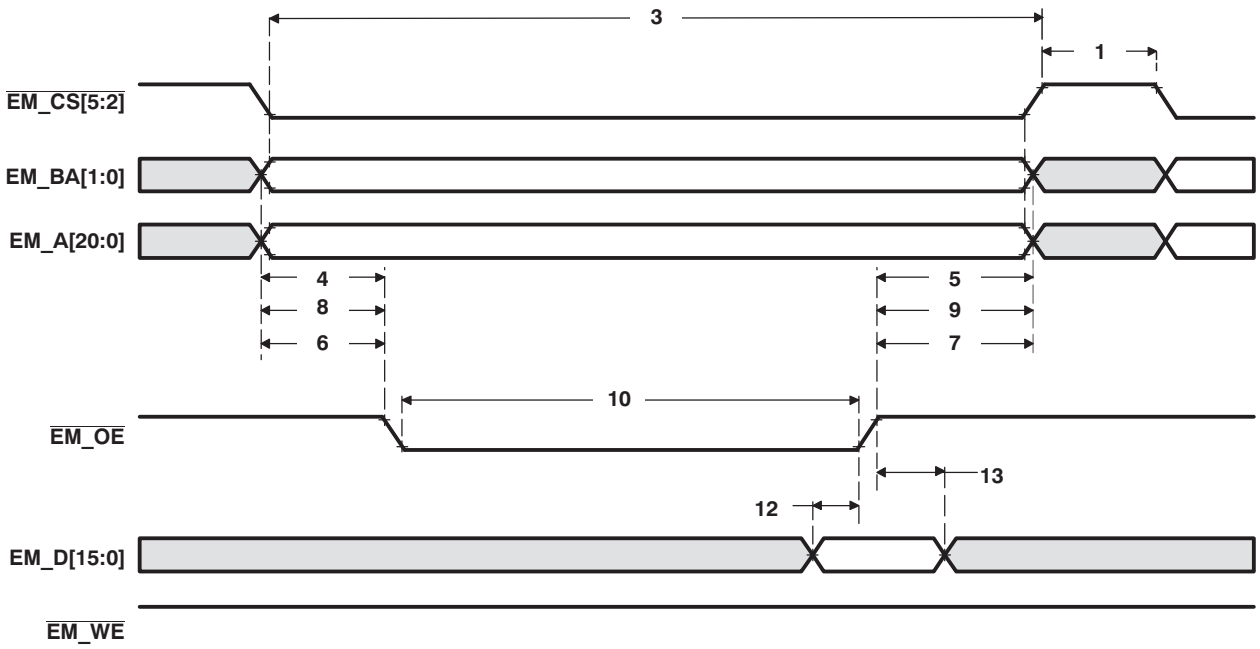


Figure 5-24. Asynchronous Memory Read Timing for EMIF

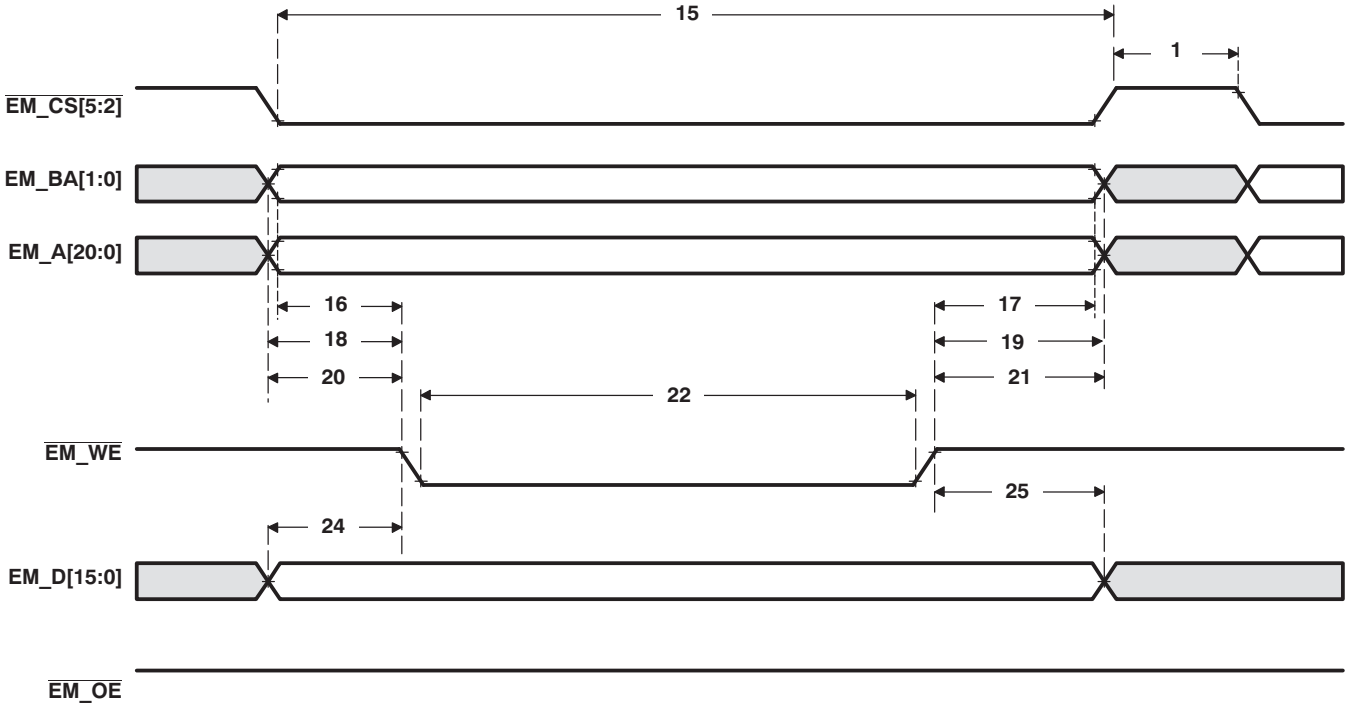


Figure 5-25. Asynchronous Memory Write Timing for EMIF

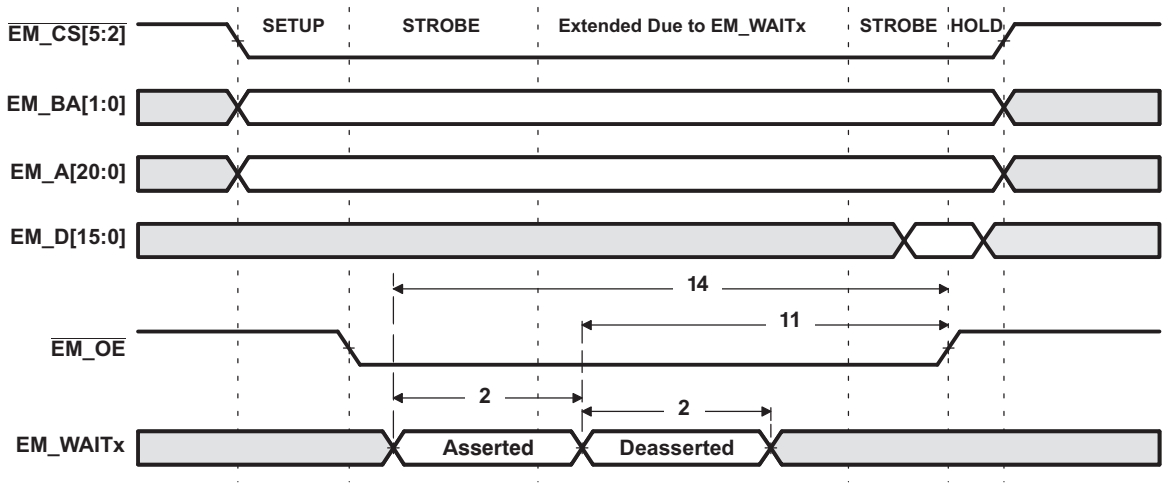


Figure 5-26. EM_WAITx Read Timing Requirements

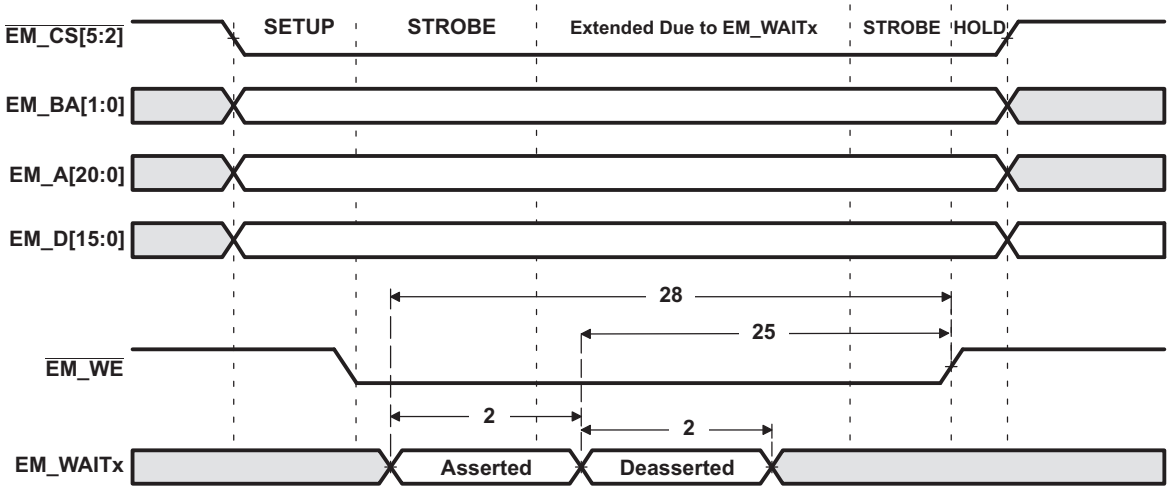


Figure 5-27. EM_WAITx Write Timing Requirements

5.7.7 General-Purpose Input/Output (GPIO)

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of the internal register. External input clocks on certain GPIOs can also be used to drive the timers on this device. The GPIO can also be used to send interrupts to the CPU.

The GPIO peripheral supports the following:

- Up to 26 GPIOs plus 1 general-purpose output (XF and 4 Special-Purpose Outputs for Use With SAR)
- The 26 GPIO pins have internal pulldowns (IPDs) which can be individually disabled
- The 26 GPIOs can be configured to generate edge detected interrupts to the CPU on either the rising or falling edge

The device GPIO pin functions are multiplexed with various other signals. For more detailed information on what signals are multiplexed with the GPIO and how to configure them, see Section 4.2, *Signal Descriptions* and Section 4.3, *Pin Multiplexing* of this document.

5.7.7.1 GPIO Peripheral Input/Output Electrical Data and Timing

Table 5-29. Timing Requirements for GPIO Inputs(1) (see Figure 5-28)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V/1.4 V		UNIT
			MIN	MAX	
1	$t_{w(ACTIVE)}$	Pulse duration, GPIO input/external interrupt pulse active	2C(1)(2)		ns
2	$t_{w(INACTIVE)}$	Pulse duration, GPIO input/external interrupt pulse inactive	C(1)(2)		ns

(1) The pulse duration given is sufficient to get latched into the GPIO_IFR register and to generate an interrupt. However, if a user wants to have the device recognize the GPIO changes through software polling of the GPIO Data In (GPIO_DIN) register, the GPIO duration must be extended to allow the device enough time to access the GPIO register through the internal bus.
(2) C = SYSCLK period in ns. For example, when running parts at 100 MHz, use C = 10 ns.

Table 5-30. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs (see Figure 5-28)

NO.	PARAMETER		CV_{DD} = 1.05 V CV_{DD} = 1.3 V/1.4 V		UNIT
			MIN	MAX	
3	$t_{w(GPOH)}$	Pulse duration, GP[x] output high	3C(1)(2)		ns
4	$t_{w(GPOL)}$	Pulse duration, GP[x] output low	3C(1)(2)		ns

(1) This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
(2) C = SYSCLK period in ns. For example, when running parts at 100 MHz, use C = 10 ns.

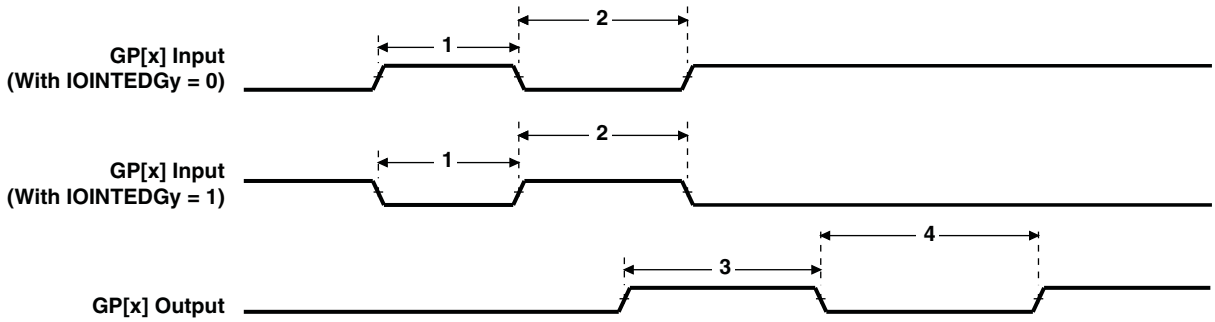


Figure 5-28. GPIO Port Timing

5.7.7.2 GPIO Peripheral Input Latency Electrical Data and Timing

Table 5-31. Timing Requirements for GPIO Input Latency(1)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V CV_{DD} = 1.4 V		UNIT
			MIN	MAX	
1	$t_{L(GPI)}$ Latency, GP[x] input	Polling GPIO_DIN register	5		cyc
		Polling GPIO_IFR register	7		cyc
		Interrupt Detection	8		cyc

(1) The pulse duration given is sufficient to generate a CPU interrupt. However, if a user wants to have the device recognize the GP[x] input changes through software polling of the GPIO register, the GP[x] input duration must be extended to allow device enough time to access the GPIO register through the internal bus.

5.7.8 Inter-Integrated Circuit (I2C)

The inter-integrated circuit (I2C) module provides an interface between the device and other devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit and receive 2 to 8-bit data to and from the DSP through the I2C module. The I2C port *does not* support CBUS compatible devices.

The I2C port supports the following features:

- Compatible with Philips I2C Specification Version 2.1 (January 2000)
- Data Transfer Rate from 10 kbps to 400 kbps (Philips Fast-Mode Rate)
- Noise Filter to Remove Noise 50 ns or Less
- Seven- and Ten-Bit Device Addressing Modes
- Master (Transmit and Receive) and Slave (Transmit and Receive) Functionality
- One Read DMA Event and One Write DMA Event, which can be used by the DMA Controller
- One Interrupt that can be used by the CPU
- Slew-Rate Limited Open-Drain Output Buffers

The I2C module clock must be in the range from 6.7 MHz to 13.3 MHz. This is necessary for proper operation of the I2C module. With the I2C module clock in this range, the noise filters on the SDA and SCL pins suppress noise that has a duration of 50 ns or shorter. The I2C module clock is derived from the DSP clock divided by a programmable prescaler.

5.7.8.1 I2C Electrical Data and Timing

Table 5-32. Timing Requirements for I2C Timings(1) (see Figure 5-29)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V CV_{DD} = 1.4 V				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
3	$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100(2)		ns
7	$t_{h(SDA-SCLL)}$	Hold time, SDA valid after SCL low	0(3)		0(3)	0.9(4)	µs
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
9	$t_{r(SDA)}$	Rise time, SDA(5)		1000	20 + 0.1C_b(6)	300	ns
10	$t_{r(SCL)}$	Rise time, SCL(5)		1000	20 + 0.1C_b(6)	300	ns

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down. Also these pins are not 3.6 V-tolerant (their V_{IH} cannot go above DV_{DDIO} + 0.3 V).
(2) A Fast-mode I^2C-bus™ device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{su(SDA-SCLH)}$= 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$= 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-Bus Specification) before the SCL line is released.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
(5) The rise and fall times are measured at 30% and 70% of DV_{DDIO}. The fall time is only slightly influenced by the external bus load ©$_b$) and external pullup resistor. However, the rise time (t_r) is mainly determined by the bus load capacitance and the value of the pullup resistor. The pullup resistor must be selected to meet the I2C rise and fall time values specified.
(6) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

Table 5-32. Timing Requirements for I2C Timings[1] (see Figure 5-29) (continued)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V CV_{DD} = 1.4 V				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
11	$t_{f(SDA)}$	Fall time, SDA[5]		300	$20 + 0.1C_b$[6]	300	ns
12	$t_{f(SCL)}$	Fall time, SCL[5]		300	$20 + 0.1C_b$[6]	300	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
15	C_b[6]	Capacitive load for each bus line		400		400	pF

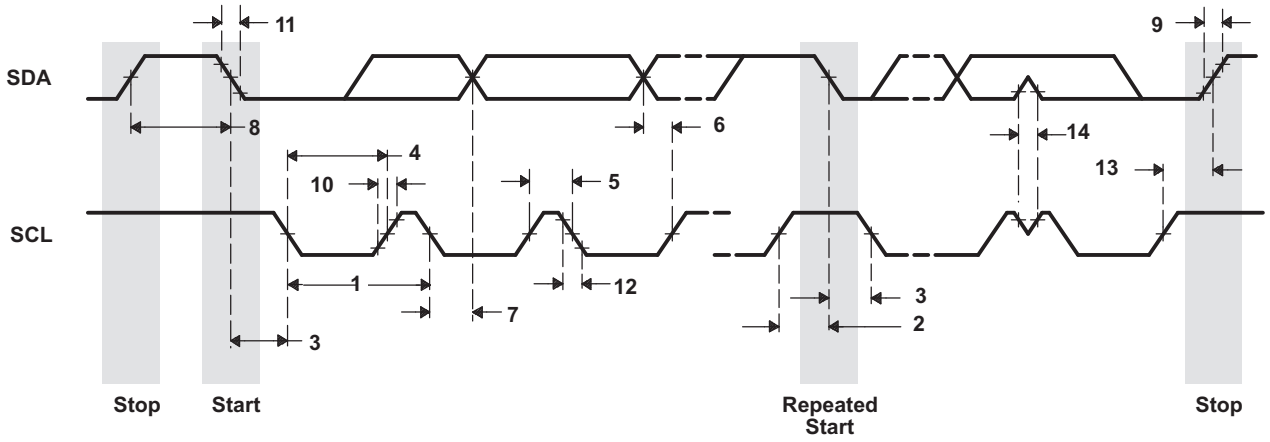


Figure 5-29. I2C Receive Timings

Table 5-33. Switching Characteristics for I2C Timings[1] (see Figure 5-30)

NO.	PARAMETER		CV_{DD} = 1.05 V CV_{DD} = 1.3 V CV_{DD} = 1.4 V				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
16	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
17	$t_{d(SCLH-SDAL)}$	Delay time, SCL high to SDA low (for a repeated START condition)	4.7		0.6		µs
18	$t_{d(SDAL-SCLL)}$	Delay time, SDA low to SCL low (for a START and a repeated START condition)	4		0.6		µs
19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
20	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
21	$t_{d(SDAV-SCLH)}$	Delay time, SDA valid to SCL high	250		100		ns
22	$t_{v(SCLL-SDAV)}$	Valid time, SDA valid after SCL low	0		0	0.9	µs
23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
24	$t_{r(SDA)}$	Rise time, SDA[2]		1000	$20 + 0.1C_b$[1]	300	ns
25	$t_{r(SCL)}$	Rise time, SCL[2]		1000	$20 + 0.1C_b$[1]	300	ns
26	$t_{f(SDA)}$	Fall time, SDA[2]		300	$20 + 0.1C_b$[1]	300	ns
27	$t_{f(SCL)}$	Fall time, SCL[2]		300	$20 + 0.1C_b$[1]	300	ns
28	$t_{d(SCLH-SDAH)}$	Delay time, SCL high to SDA high (for STOP condition)	4		0.6		µs
29	C_p	Capacitance for each I2C pin		10		10	pF

(1) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.
(2) The rise and fall times are measured at 30% and 70% of DV_{DDIO}. The fall time is only slightly influenced by the external bus load (C_b) and external pullup resistor. However, the rise time (t_r) is mainly determined by the bus load capacitance and the value of the pullup resistor. The pullup resistor must be selected to meet the I2C rise and fall time values specified.

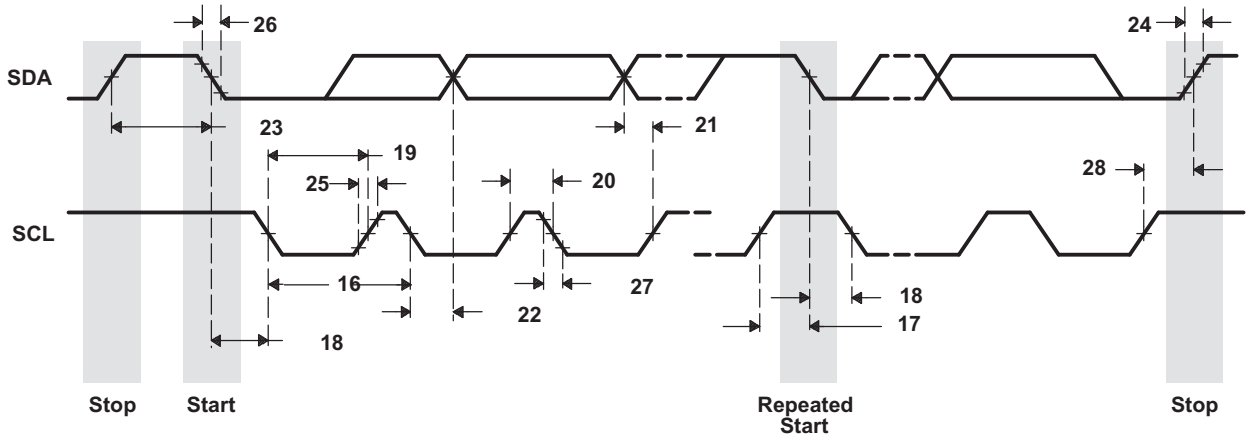


Figure 5-30. I2C Transmit Timings

5.7.9 Inter-IC Sound (I2S)

The device I2S peripherals allow serial transfer of full-duplex streaming data, usually audio data, between the device and an external I2S peripheral device such as an audio codec.

The device supports three independent dual-channel I2S peripherals, each with the following features:

- Full-duplex (transmit and receive) dual-channel communication
- Double buffered data registers that allow for continuous data streaming
- I2S/Left-justified and DSP data format with a data delay of 1 or 2 bits
- Data word-lengths of 8, 10, 12, 14, 16, 18, 20, 24, or 32 bits
- Ability to sign-extend received data samples for easy use in signal processing algorithms
- Programmable polarity for both frame synchronization and bit clocks
- Stereo (in I2S/Left-justified or DSP data formats) or mono (in DSP data format) mode
- Detection of over-run, under-run, and frame-sync error conditions

5.7.9.1 Inter-IC Sound (I2S) Electrical Data and Timing

Table 5-34. Timing Requirements for I2S [I/O = 3.3 and 2.75 V](1) (see Figure 5-31)

NO.			MASTER				SLAVE				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, I2S_CLK	2P(1)(2)		2P(1)(2)		2P(1)(2)		2P(1)(2)		ns
2	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high	P(1)(2)		P(1)(2)		P(1)(2)		P(1)(2)		ns
3	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low	P(1)(2)		P(1)(2)		P(1)(2)		P(1)(2)		ns
7	$t_{su(RXV-CLKH)}$	Setup time, I2S_RX valid before I2S CLK high (CLKPOL = 0)	5		3		5		3		ns
	$t_{su(RXV-CLKL)}$	Setup time, I2S_RX valid before I2S_CLK low (CLKPOL = 1)	5		3		5		3		ns
8	$t_{h(CLKH-RXV)}$	Hold time, I2S_RX valid after I2S_CLK high (CLKPOL = 0)	3		3		3		3		ns
	$t_{h(CLKL-RXV)}$	Hold time, I2S_RX valid after I2S_CLK low (CLKPOL = 1)	3		3		3		3		ns
9	$t_{su(FSV-CLKH)}$	Setup time, I2S_FS valid before I2S_CLK high (CLKPOL = 0)	–		–		12.5		6.5		ns
	$t_{su(FSV-CLKL)}$	Setup time, I2S_FS valid before I2S_CLK low (CLKPOL = 1)	–		–		12.5		6.5		ns
10	$t_{h(CLKH-FSV)}$	Hold time, I2S_FS valid after I2S_CLK high (CLKPOL = 0)	–		–		$t_{w(CLKH)}$ + 0.7(3)		$t_{w(CLKH)}$ + 0.7(3)		ns
	$t_{h(CLKL-FSV)}$	Hold time, I2S_FS valid after I2S_CLK low (CLKPOL = 1)	–		–		$t_{w(CLKL)}$ + 0.7(3)		$t_{w(CLKL)}$ + 0.7(3)		ns

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.
(3) In Slave Mode, I2S_FS is required to be latched on both edges of I2S input clock (I2S_CLK).

Table 5-35. Timing Requirements for I2S [I/O = 1.8 V](1) (see Figure 5-31)

NO.			MASTER				SLAVE				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, I2S_CLK	2P(1) (2)		2P(1) (2)		2P(1) (2)		2P(1) (2)		ns
2	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high	P(1) (2)		P(1) (2)		P(1) (2)		P(1) (2)		ns
3	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low	P(1) (2)		P(1) (2)		P(1) (2)		P(1) (2)		ns
7	$t_{su(RXV-CLKH)}$	Setup time, I2S_RX valid before I2S CLK high (CLKPOL = 0)	5		3		5		3.5		ns
	$t_{su(RXV-CLKL)}$	Setup time, I2S_RX valid before I2S_CLK low (CLKPOL = 1)	5		3		5		3.5		ns
8	$t_{h(CLKH-RXV)}$	Hold time, I2S_RX valid after I2S_CLK high (CLKPOL = 0)	3		3		3		3		ns
	$t_{h(CLKL-RXV)}$	Hold time, I2S_RX valid after I2S_CLK low (CLKPOL = 1)	3		3		3		3		ns
9	$t_{su(FSV-CLKH)}$	Setup time, I2S_FS valid before I2S_CLK high (CLKPOL = 0)	–		–		12.5		15		ns
	$t_{su(FSV-CLKL)}$	Setup time, I2S_FS valid before I2S_CLK low (CLKPOL = 1)	–		–		12.5		15		ns
10	$t_{h(CLKH-FSV)}$	Hold time, I2S_FS valid after I2S_CLK high (CLKPOL = 0)	–		–		$t_{w(CLKH)} + 0.7$(3)		$t_{w(CLKH)} + 0.71$(3)		ns
	$t_{h(CLKL-FSV)}$	Hold time, I2S_FS valid after I2S_CLK low (CLKPOL = 1)	–		–		$t_{w(CLKL)} + 0.7$(3)		$t_{w(CLKL)} + 0.71$(3)		ns

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.
(3) In Slave Mode, I2S_FS is required to be latched on both edges of I2S input clock (I2S_CLK).

Table 5-36. Switching Characteristics Over Recommended Operating Conditions for I2S Output [I/O = 3.3 and 2.75 V] (see Figure 5-31)

NO.	PARAMETER		MASTER				SLAVE				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, I2S_CLK	P(1) (2)		P(1) (2)		P(1) (2)		P(1) (2)		ns
2	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high (CLKPOL = 0)	P(1) (2)		P(1) (2)		P(1) (2)		P(1) (2)		ns
	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low (CLKPOL = 1)	P(1) (2)		P(1) (2)		P(1) (2)		P(1) (2)		ns
3	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low (CLKPOL = 0)	P(1) (2)		P(1) (2)		P(1) (2)		P(1) (2)		ns
	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high (CLKPOL = 1)	P(1) (2)		P(1) (2)		P(1) (2)		P(1) (2)		ns
4	$t_{dmax(CLKL-DXV)}$	Output Delay time, I2S_CLK low to I2S_DX valid (CLKPOL = 0)	0	14.5	0	11	0	14.5	0	11	ns
	$t_{dmax(CLKH-DXV)}$	Output Delay time, I2S_CLK high to I2S_DX valid (CLKPOL = 1)	0	14.5	0	11	0	14.5	0	11	ns
5	$t_{dmax(CLKL-FSV)}$	Delay time, I2S_CLK low to I2S_FS valid (CLKPOL = 0)	-2	7	-1.74	5		–		–	ns
	$t_{dmax(CLKH-FSV)}$	Delay time, I2S_CLK high to I2S_FS valid (CLKPOL = 1)	-2	7	-1.74	5		–		–	ns

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.

Table 5-37. Switching Characteristics Over Recommended Operating Conditions for I2S Output [I/O = 1.8 V] (see Figure 5-31)

NO.	PARAMETER		MASTER				SLAVE				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, I2S_CLK	50 or 2P(1) (2)		40 or 2P(1) (2)		50 or 2P(1) (2)		40 or 2P(1) (2)		ns
2	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high (CLKPOL = 0)	P(1) (2)		P(1) (2)		P(1) (2)		P(1) (2)		ns
	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low (CLKPOL = 1)	P(1) (2)		P(1) (2)		P(1) (2)		P(1) (2)		ns
3	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low (CLKPOL = 0)	P(1) (2)		P(1) (2)		P(1) (2)		P(1) (2)		ns
	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high (CLKPOL = 1)	P(1) (2)		P(1) (2)		P(1) (2)		P(1) (2)		ns
4	$t_{dmax(CLKL-DXV)}$	Output Delay time, I2S_CLK low to I2S_DX valid (CLKPOL = 0)	0	17.7	0	14.5	0	17.7	0	14.5	ns
	$t_{dmax(CLKH-DXV)}$	Output Delay time, I2S_CLK high to I2S_DX valid (CLKPOL = 1)	0	17.7	0	14.5	0	17.7	0	14.5	ns
5	$t_{dmax(CLKL-FSV)}$	Delay time, I2S_CLK low to I2S_FS valid (CLKPOL = 0)	-2	7	-2	5		–		–	ns
	$t_{dmax(CLKH-FSV)}$	Delay time, I2S_CLK high to I2S_FS valid (CLKPOL = 1)	-2	7	-2	5		–		–	ns

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.

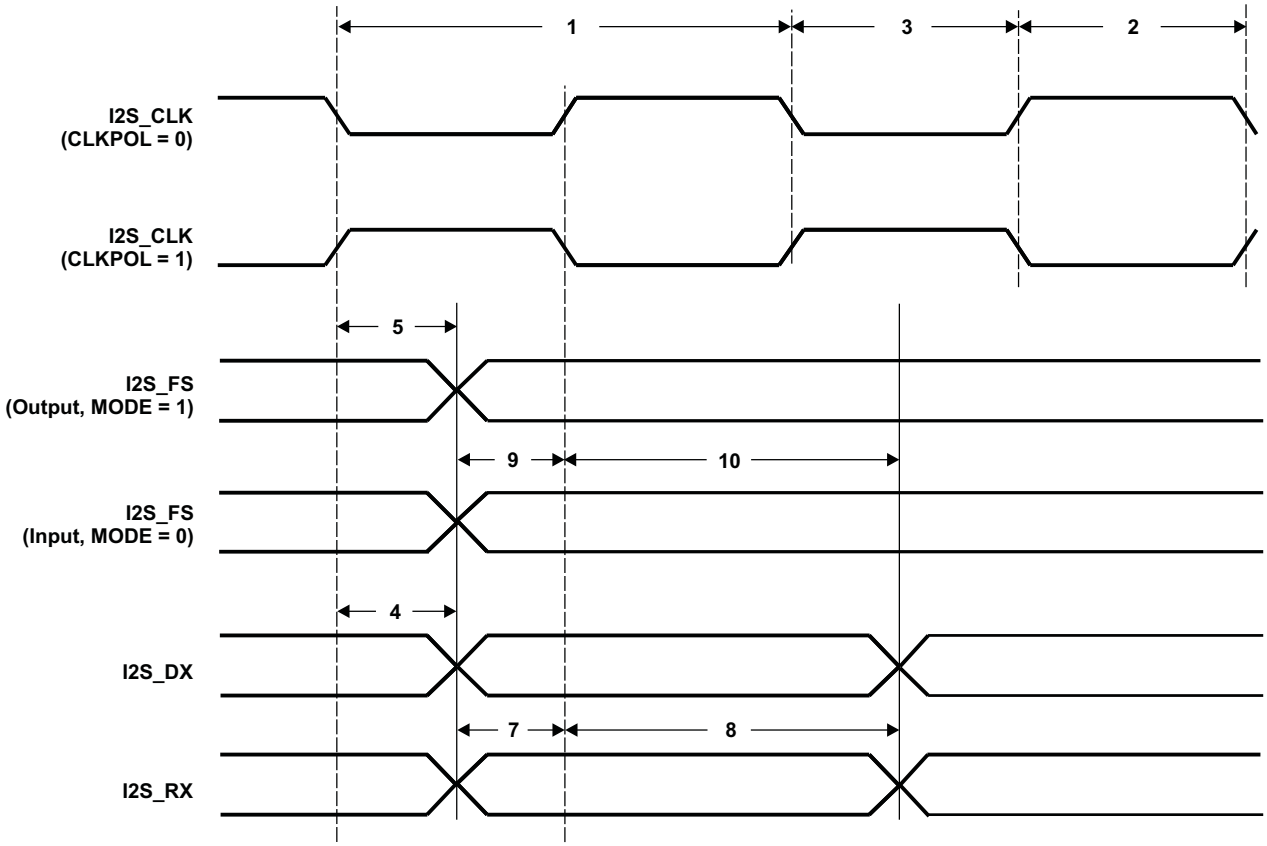


Figure 5-31. I2S Input and Output Timings

5.7.10 Multichannel Serial Port Interface (McSPI)

The multichannel SPI (McSPI) is a master and slave synchronous serial bus. McSPI allows a duplex, synchronous, serial communication to SPI-compliant external devices (slaves and masters).

The McSPI instances include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths ranging from 4 to 32 bits
- Up to three master channels or single channel in slave mode
- Master multichannel mode:
  - Full duplex and half duplex
  - Transmit-only and receive-only and transmit-and-receive modes
  - Flexible I/O port controls per channel
  - Two direct memory access (DMA) requests (read and write) per channel
- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for SPI transfer per channel (start-bit mode)
- Support start-bit write command
- 128-bytes built-in FIFO available for a single channel
- Force CS mode for continuous transfers

5.7.10.1 McSPI Electrical Data and Timing

The multichannel SPI is a master and slave synchronous serial bus.

The following tables assume testing over the recommended operating conditions.

5.7.10.1.1 McSPI in Slave Mode

Table 5-38. McSPI Interface Timing Requirements – Slave Mode

NO.			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
			MIN	MAX	MIN	MAX	
SS2	$t_{su(SIMOV-CLKAE)}$	Setup time, McSPI_SIMO valid before McSPI_CLK active edge	4		3		ns
SS3	$t_{h(SIMOV-CLKAE)}$	Hold time, McSPI_SIMO valid after McSPI_CLK active edge	3.8		2.8		ns
SS4	$t_{su(CS0V-CLKFE)}$	Setup time, McSPI_CS0 valid before McSPI_CLK first edge	6.9		6.9		ns
SS5	$t_{h(CS0I-CLKLE)}$	Hold time, McSPI_CS0 invalid after McSPI_CLK last edge	6.9		6.9		ns

Table 5-39. McSPI Interface Switching Characteristics — Slave Mode [I/O = 3.3 V]

NO.	PARAMETER		CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
			MIN	MAX	MIN	MAX	
SS0		Clock period		14		22	MHz
SS1	t_w(CLK)	Pulse duration, McSPI_CLK high or low	0.45*P(1)	0.55*P(1)	0.45*P(1)	0.55*P(1)	ns
SS6		Output Delay time, McSPI_CLK active edge to McSPI_SOMI valid	0	31	0	19	ns
SS7		Delay time, McSPI_CSn active edge to McSPIn_SOMI shifted, Mode 0		15		8.7	ns
SS7		Delay time, McSPI_CSn active edge to McSPIn_SOMI shifted, Mode 2		15		8.7	ns

(1) P = McSPI_CLK clock period.

Table 5-40. McSPI Interface Switching Characteristics — Slave Mode [I/O = 2.75 V]

NO.	PARAMETER			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
				MIN	MAX	MIN	MAX	
SS0		Clock period			12		19	MHz
SS1	t_w(CLK)	Pulse duration, McSPI_CLK high or low		0.45*P(1)	0.55*P(1)	0.45*P(1)	0.55*P(1)	ns
SS6		Output Delay time, McSPI_CLK active edge to McSPI_SOMI valid		0	36	0	22.5	ns
SS7		Delay time, McSPI_CSn active edge to McSPIn_SOMI shifted	Modes 0 and 2		15		12	ns

(1) P = McSPI_CLK clock period.

Table 5-41. McSPI Interface Switching Characteristics — Slave Mode [I/O = 1.8 V]

NO.	PARAMETER			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
				MIN	MAX	MIN	MAX	
SS0		Clock period			12		18	MHz
SS1	t_w(CLK)	Pulse duration, McSPI_CLK high or low		0.45*P(1)	0.55*P(1)	0.45*P(1)	0.55*P(1)	ns
SS6		Output Delay time, McSPI_CLK active edge to McSPI_SOMI valid		0	36	0	24	ns
SS7		Delay time, McSPI_CSn active edge to McSPIn_SOMI shifted	Modes 0 and 2		17		15	ns

(1) P = McSPI_CLK clock period.

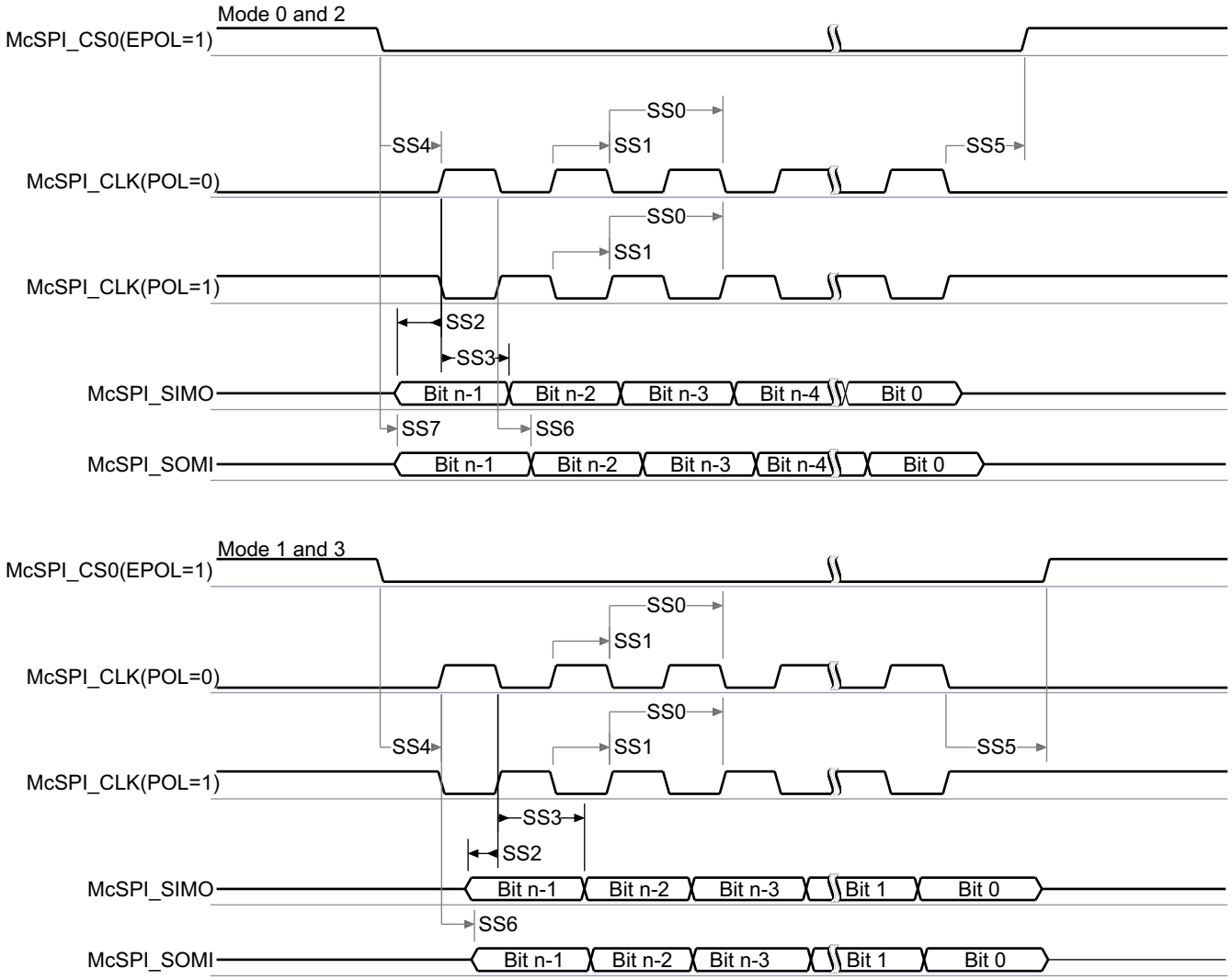


Figure 5-32. McSPI Interface — Transmit and Receive in Slave Mode

5.7.10.1.2 McSPI in Master Mode

The following tables assume testing over the recommended operating conditions (see Figure 5-33).

Table 5-42. McSPI Interface Timing Requirements – Master Mode [I/O = 3.3, 2.75 V]

NO.		CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
		MIN	MAX	MIN	MAX	
SM2	Setup time, McSPI_SOMI valid before McSPI_CLK active edge	4		3		ns
SM3	Hold time, McSPI_SOMI valid after McSPI_CLK active edge	3.8		2.8		ns

Table 5-43. McSPI Interface Timing Requirements – Master Mode [I/O = 1.8 V]

NO.		CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
		MIN	MAX	MIN	MAX	
SM2	Setup time, McSPI_SOMI valid before McSPI_CLK active edge	7.5		3		ns
SM3	Hold time, McSPI_SOMI valid after McSPI_CLK active edge	3.8		2.8		ns

Table 5-44. McSPI Interface Switching Characteristics – Master Mode [I/O = 3.3 V]

NO.	PARAMETER		CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
			MIN	MAX	MIN	MAX	
SM0	Clock period			22		42	MHz
SM1	Pulse duration, McSPI_CLK high or low		0.45*P(1)	0.55*P(1)	0.45*P(1)	0.55*P(1)	ns
SM4	Delay time, McSPI_CLK active edge to McSPI_SIMO valid		0	18	-1	8.9	ns
SM5	Delay time, McSPI_CSx active to McSPI_CLK first edge	Modes 0–3	3.1		3.1		ns
SM6	Delay time, McSPI_CLK last edge to McSPI_CSx inactive	Modes 0–3	3.1		3.1		ns
SM7	Delay time, McSPI_CSx active edge to McSPI_SIMO shifted	Modes 0 and 2		10		6	ns

(1) P = McSPI_CLK clock period

Table 5-45. McSPI Interface Switching Characteristics – Master Mode [I/O = 2.75 V]

NO.	PARAMETER		CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
			MIN	MAX	MIN	MAX	
SM0	Clock period			22		38	MHz
SM1	Pulse duration, McSPI_CLK high or low		0.45*P(1)	0.55*P(1)	0.45*P(1)	0.55*P(1)	ns
SM4	Delay time, McSPI_CLK active edge to McSPI_SIMO valid		0	18	-1	10	ns
SM5	Delay time, McSPI_CSx active to McSPI_CLK first edge	Modes 0–3	3.1		3.1		ns
SM6	Delay time, McSPI_CLK last edge to McSPI_CSx inactive	Modes 0–3	3.1		3.1		ns
SM7	Delay time, McSPI_CSx active edge to McSPI_SIMO shifted	Modes 0 and 2		10		6	ns

(1) P = McSPI_CLK clock period

Table 5-46. McSPI Interface Switching Characteristics – Master Mode [I/O = 1.8 V]

NO.	PARAMETER		CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
			MIN	MAX	MIN	MAX	
SM0	Clock period			19		38	MHz
SM1	Pulse duration, McSPI_CLK high or low		0.45*P(1)	0.55*P(1)	0.45*P(1)	0.55*P(1)	ns
SM4	Delay time, McSPI_CLK active edge to McSPI_SIMO valid		0	18.5	-1	10	ns
SM5	Delay time, McSPI_CSx active to McSPI_CLK first edge	Modes 0–3	2.75		3		ns
SM6	Delay time, McSPI_CLK last edge to McSPI_CSx inactive	Modes 0–3	2.75		3		ns
SM7	Delay time, McSPI_CSx active edge to McSPI_SIMO shifted	Modes 0 and 2		11		5	ns

(1) P = McSPI_CLK clock period

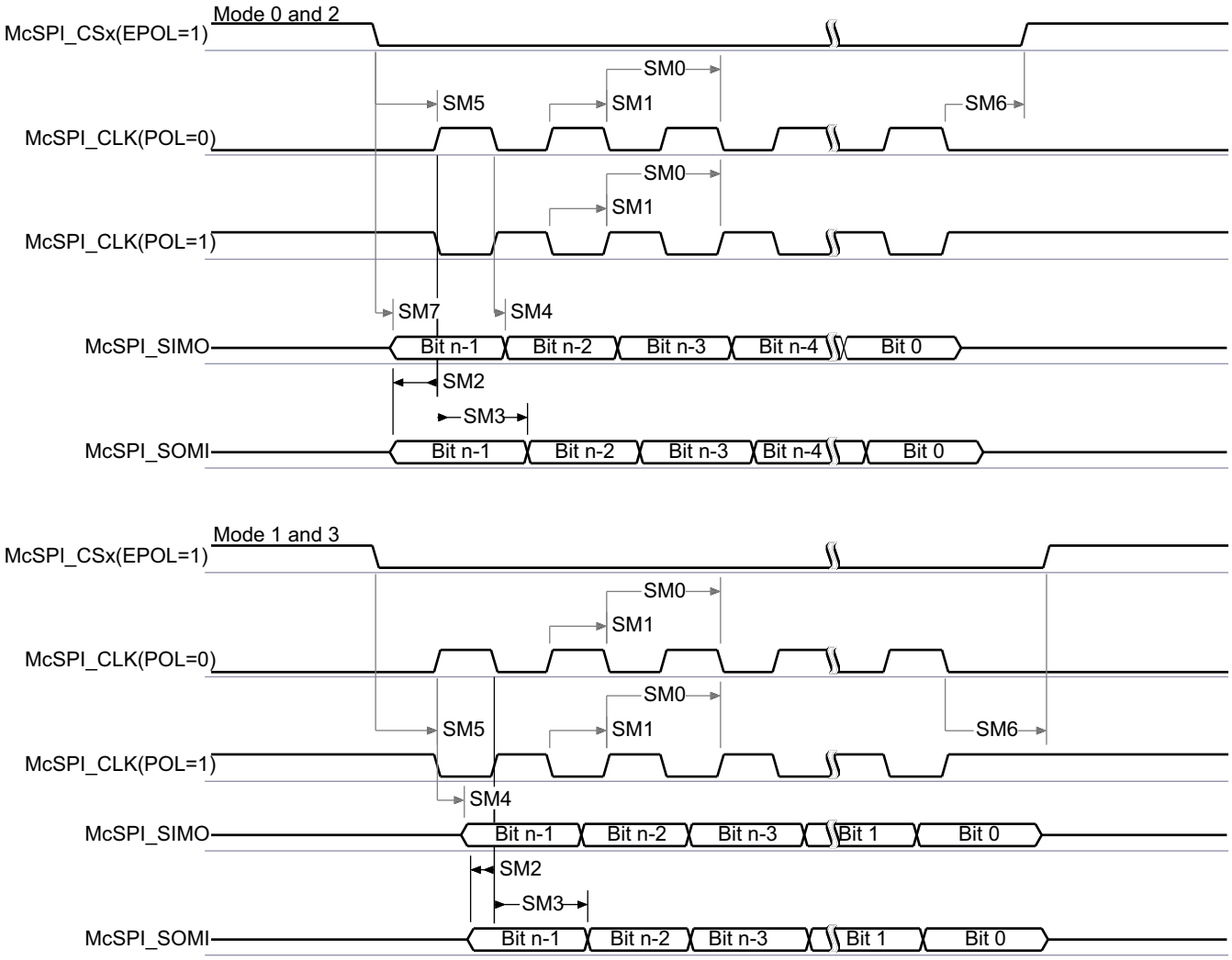


Figure 5-33. McSPI Interface — Transmit and Receive in Master Mode

5.7.11 Multichannel Buffered Serial Port (McBSP)

The McBSP provides these functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- External shift clock or an internal, programmable frequency shift clock for data transfer
- Transmit and Receive FIFO Buffers allow the McBSP to operate at a higher sample rate by making it more tolerant to DMA latency

If the internal clock is used, the CLKGDV field of the Sample Rate Generator Register (SRGR) must always be set to a value of 3 or greater.

5.7.11.1 McBSP Electrical Data and Timing

Table 5-47. Timing Requirements for McBSP, DV_{DDIO} 1.8 V (see Figure 5-34)

NO.				CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
				DV_{DDIO} 1.8 V				
				MIN	MAX	MIN	MAX	
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	15		9		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P-1 (1)		P-1 (1)		ns
5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	29.5		29.5		ns
			CLKR ext	3.5		3.5		
6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	4.5		4.5		ns
			CLKR ext	4.5		4.5		
7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	18.5		18.5		ns
			CLKR ext	2.5		2.5		
8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	-4		-4		ns
			CLKR ext	5.5		5.5		
10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	26.5		26.5		ns
			CLKX ext	7.5		7.5		
11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	0.5		0.5		ns
			CLKX ext	2.5		2.5		

(1) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

Table 5-48. Timing Requirements for McBSP, DV_{DDIO} 3.3/2.75 V (see Figure 5-34)

NO.				CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
				DV_{DDIO} 3.3/2.75 V				
				MIN	MAX	MIN	MAX	
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	18		9		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P-1 (1)		P-1 (1)		ns
5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	24		24		ns
			CLKR ext	4		4		
6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	4		4		ns
			CLKR ext	5		5		
7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	22.5		22.5		ns
			CLKR ext	2.5		2.5		
8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	-3		-3		ns
			CLKR ext	6		6		
10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	23		23		ns
			CLKX ext	7		7		
11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	2		2		ns
			CLKX ext	3		3		

(1) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

Table 5-49. Switching Characteristics Over Recommended Operating Conditions for McBSP, DV_{DDIO} 1.8 V (see Figure 5-34)

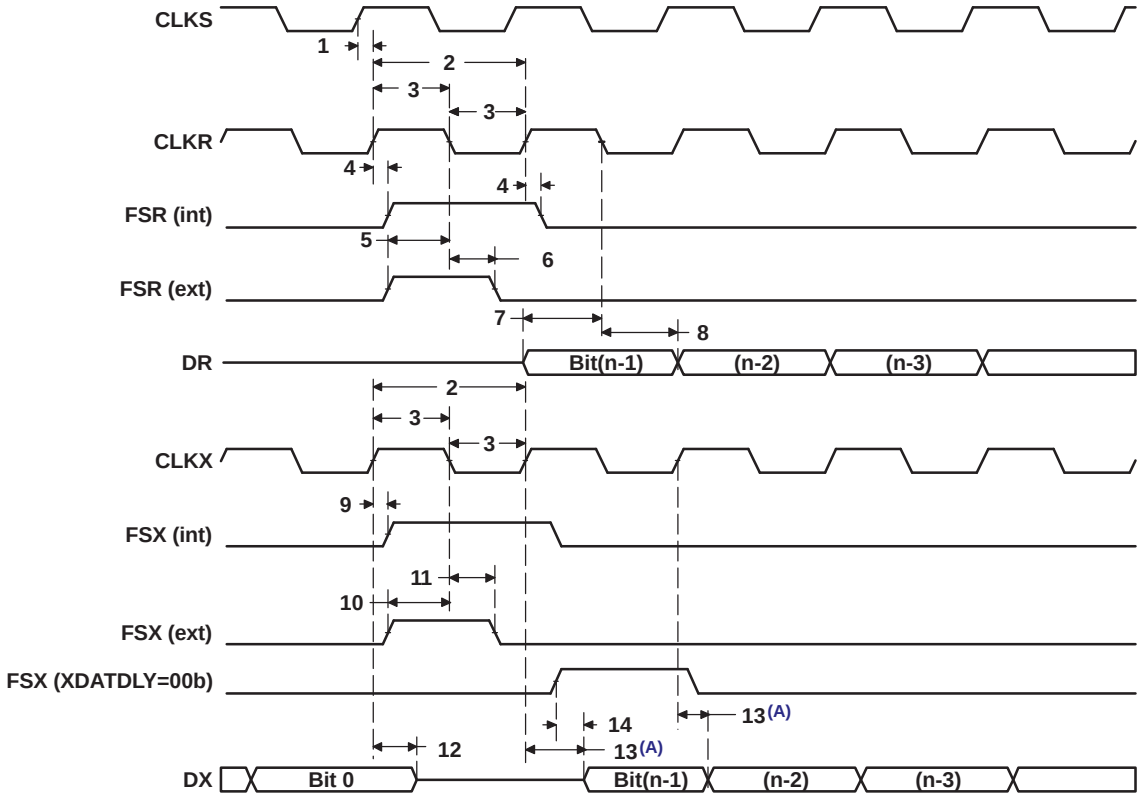
NO.	PARAMETER			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
				DV_{DDIO} 1.8 V				
				MIN	MAX	MIN	MAX	
1	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input		5.5	25	5.5	25	ns
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int	15		9		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int	C+2 (1)		C+2 (1)		ns
4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int	-6.5	6	-6.5	6	ns
9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int	-2	1	-2	1	ns
			CLKX ext	4	23	4	23	
12	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	CLKX int	-5	3	-5	3	ns
			CLKX ext	3	24.5	3	24.5	
13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int	-4.5	4	-4.5	4	ns
			CLKX ext	3.5	25.5	3.5	25.5	
14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	FSX int	-4	4	-4	4	ns
			FSX ext	-2	3	-2	3	

(1) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = SYSCLK period)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse duration = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse duration = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see (4) above).

Table 5-50. Switching Characteristics Over Recommended Operating Conditions for McBSP, DV_{DDIO} 3.3/2.75 V (see Figure 5-34)

NO.	PARAMETER			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
				DV_{DDIO} 3.3/2.75 V				
				MIN	MAX	MIN	MAX	
1	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input		4.25	24	4.5	24	ns
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int	18		9		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int	C-2 (1)		C-2 (1)		ns
4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int	-4	8	-4	8	ns
9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int	-2	2	-2	2	ns
			CLKX ext	3.5	20	3.5	20	
12	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	CLKX int	-2.5	4	-2.5	4	ns
			CLKX ext	3	21	-3	21	
13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int	-2.5	5	-2.5	5	ns
			CLKX ext	3	22.5	3	22.5	
14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	FSX int	-1.5	4	-1.5	4	ns
			FSX ext	-1.5	3.5	-1.5	3.5	

(1) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = SYSCLK period)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse duration = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse duration = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see (4) above).



A. Parameter No. 13 applies to the first data bit *only* when XDATDLY ≠ 0.

B. McBSP_CLKS and McBSP_CLKR are shared on the same pin. See Table 4-7, *Multichannel Buffered Serial Ports (McBSP) Signal Descriptions*, for how each is selected.

Figure 5-34. McBSP Timing

Table 5-51. Timing Requirements for FSR When GSYNC = 1 (see Figure 5-35)

NO.			CV_{DD} = 1.05 V DV_{DDIO} 3.3/2.75/1.8 V		CV_{DD} = 1.3/1.4 V DV_{DDIO} 3.3/2.75/1.8 V		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{su(FRH-CKSH)}$	Setup time, FSR high before CLKS high	5		5		ns
2	$t_{h(CKSH-FRH)}$	Hold time, FSR high after CLKS high	4		4		ns

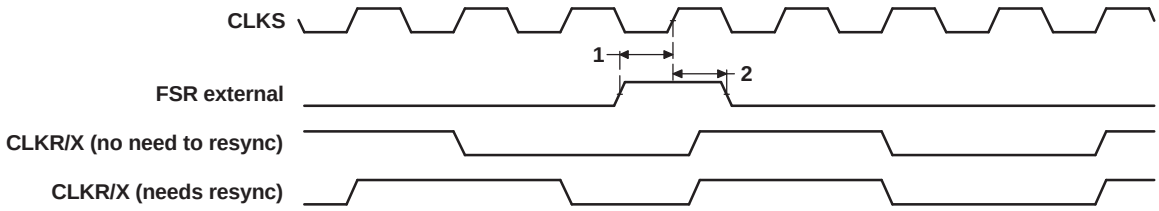


Figure 5-35. FSR Timing When GSYNC = 1

5.7.12 Multimedia Card and Secure Digital (eMMC, MMC, SD, and SDHC)

The device includes two MMC and SD controllers which are compliant with eMMC V4.3, MMC V3.31, Secure Digital Part 1 Physical Layer Specification V2.0, and Secure Digital Input Output (SDIO) V2.0 specifications. The MMC and SD card controller supports these industry standards and assumes the reader is familiar with these standards.

Each MMC and SD Controller in the device has the following features:

- Multimedia Card and Secure Digital (eMMC, MMC, SD, and SDHC) protocol support
- Programmable clock frequency
- 256-bit Read and Write FIFO to lower system overhead
- Slave DMA transfer capability

The MMC and SD card controller transfers data between the CPU and DMA controller on one side and MMC and SD card on the other side. The CPU and DMA controller can read and write the data in the card by accessing the registers in the MMC and SD controller.

The MMC and SD controller on this device, does not support the SPI mode of operation.

5.7.12.1 MMC and SD Electrical Data and Timing

Table 5-52. Timing Requirements for MMC and SD (see Figure 5-36 and Figure 5-39)

NO.			CV_{DD} = 1.3/1.4 V		CV_{DD} = 1.05 V		UNIT
			FAST MODE		STD MODE		
			MIN	MAX	MIN	MAX	
1	$t_{su(CMDV-CLKH)}$	Setup time, MMCx_CMD data input valid before MMCx_CLK high	3		3		ns
2	$t_{h(CLKH-CMDV)}$	Hold time, MMCx_CMD data input valid after MMCx_CLK high	3		3		ns
3	$t_{su(DATV-CLKH)}$	Setup time, MMC_Dx data input valid before MMCx_CLK high	3		3.1		ns
4	$t_{h(CLKH-DATV)}$	Hold time, MMC_Dx data input valid after MMCx_CLK high	3		3		ns

Table 5-53. Switching Characteristics Over Recommended Operating Conditions for MMC Output(1) (see Figure 5-36 and Figure 5-39)

NO.	PARAMETER		CV_{DD} = 1.3/1.4 V		CV_{DD} = 1.05 V		UNIT
			FAST MODE		STD MODE		
			MIN	MAX	MIN	MAX	
7	$f_{(CLK)}$	Operating frequency, MMCx_CLK	0	50(2)	0	25(2)	MHz
8	$f_{(CLK\_ID)}$	Identification mode frequency, MMCx_CLK	0	400	0	400	kHz
9	$t_{w(CLKL)}$	Pulse duration, MMCx_CLK low	7		10		ns
10	$t_{w(CLKH)}$	Pulse duration, MMCx_CLK high	7		10		ns
11	$t_{r(CLK)}$	Rise time, MMCx_CLK		3		3	ns
12	$t_{f(CLK)}$	Fall time, MMCx_CLK		3		3	ns
13	$t_{d(MDCLKL-CMDIV)}$	Delay time, MMCx_CLK low to MMC_CMD data output invalid	-4.53		-4.77		ns
14	$t_{d(MDCLKL-CMDV)}$	Delay time, MMCx_CLK low to MMC_CMD data output valid		4.1		5.4	ns
15	$t_{d(MDCLKL-DATIV)}$	Delay time, MMCx_CLK low to MMC_Dx data output invalid	-4.53		-4.77		ns
16	$t_{d(MDCLKL-DATV)}$	Delay time, MMCx_CLK low to MMC_Dx data output valid		4.1		5.4	ns

(1) For MMC and SD, the parametric values are measured at DV_{DDIO} = 3.3 V and 2.75 V.
(2) Use this value or SYS_CLK/2 whichever is smaller.

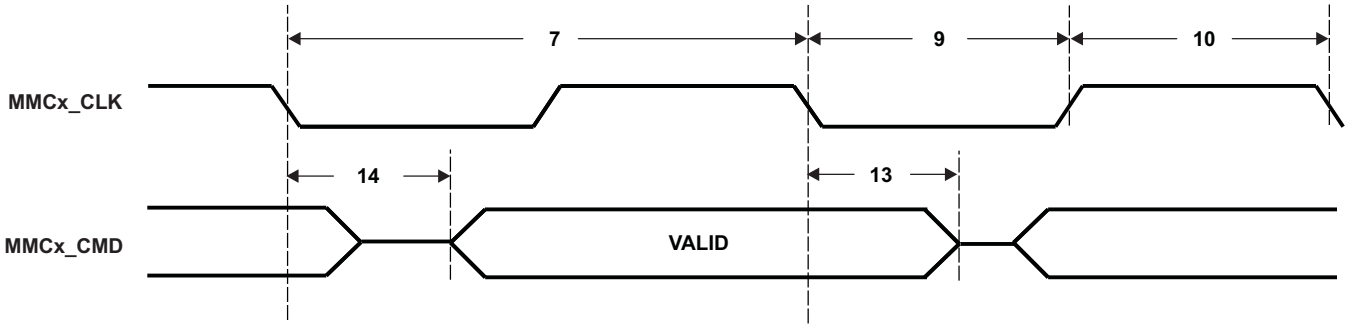


Figure 5-36. MMC and SD Host Command Write Timing

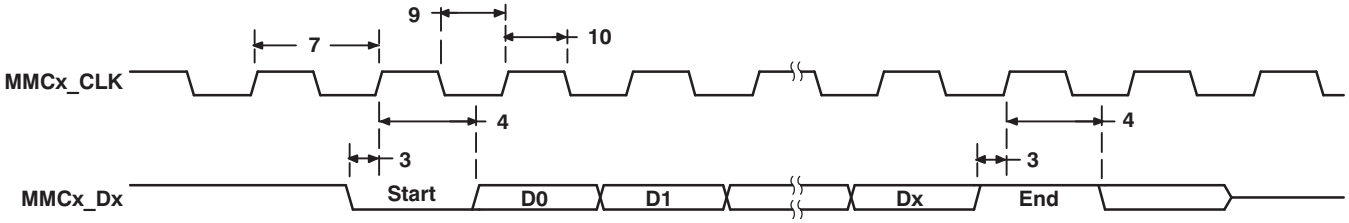


Figure 5-37. MMC and SD Card Response Timing

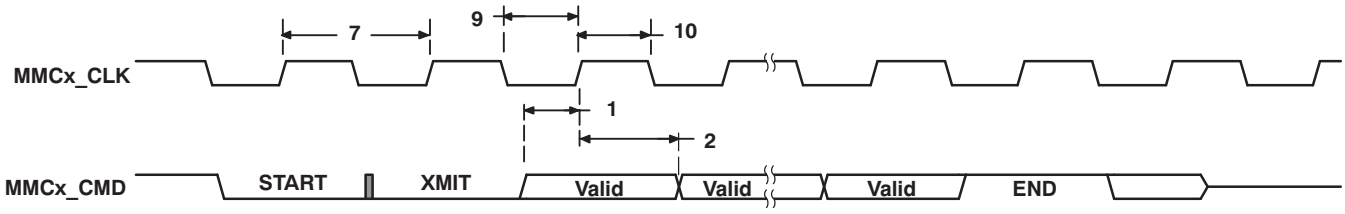


Figure 5-38. MMC and SD Host Write Timing

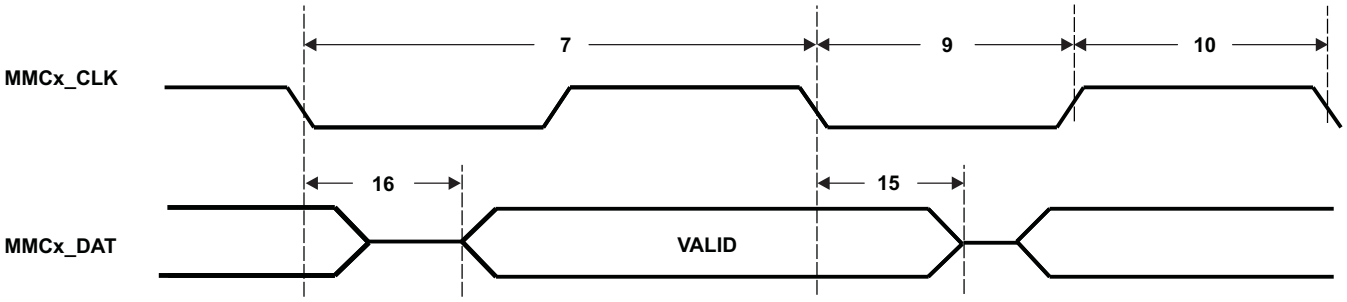


Figure 5-39. MMC and SD Data Write Timing

5.7.13 Real-Time Clock (RTC)

The device includes a Real-Time Clock (RTC) with its own separate power supply and isolation circuits. The RTC has the capability to wake up the device from idle states via alarms, periodic interrupts, or an external WAKEUP input.

To prevent unintentional access to the RTC registers, gate-keeper registers must be programmed with a specific signature—0x95A4_F1E0—before changing the RTC registers.

Note: The RTC Core (CV_{DDRTC}) must be powered by an external power source even though RTC is not used. None of the on-chip LDOs can power CV_{DDRTC}.

The device RTC provides the following features:

- 100-year calendar up to year 2099.
- Counts milliseconds, seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Millisecond time correction
- Binary-coded-decimal (BCD) representation of time, calendar, and alarm
- 24-hour clock mode
- Second, minute, hour, or day alarm interrupt
- Periodic interrupt: every millisecond, second, minute, hour, or day
- Alarm interrupt: precise time of day
- Single interrupt to the DSP CPU
- 32.768-kHz crystal oscillator with frequency calibration
- Bidirectional IO pin that can be set up as:
  - Input for an external device to wake up the DSP
  - Output to wake up an external device

Control of the RTC is maintained through a set of I/O memory mapped registers (see Table 6-19). Note that any write to these registers will be synchronized to the RTC 32.768-kHz clock; thus, the CPU must run at least 3X faster than the RTC. Writes to these registers will not be evident until the next two 32.768-kHz clock cycles later.

Furthermore, three conditions must be met to write to the RTC registers:

1. The RTC oscillator must be enabled.
2. A 1 must be written to the RTC system control register (RSCR) to bring the RTC out of isolation.
3. The gate-keeper registers (RGKR_LSW and RGKR_MSW) must contain the key 0x95A4_F1E0.

If these conditions are not met, the RTC remains isolated and protected from power glitches.

For more information, see the *Static Power Management* section of the *TMS320C5517 Digital Signal Processor Technical Reference Manual* [literature number SPRUH16].

The RTC has its own power-on-reset (POR) circuit which resets the registers in the RTC core domain when power is first applied to the CV_{DDRTC} power pin. The RTC flops are not reset by the device's $\overline{\text{RESET}}$ pin nor the digital core's POR (powergood signal).

The scratch registers in the RTC can be used to take advantage of this unique reset domain to keep track of when the DSP boots and whether the RTC time registers have already been initialized to the current clock time or whether the software needs to go into a routine to prompt the user to set the time and date.

5.7.13.1 RTC Electrical Data and Timing

For more detailed information on RTC electrical timings, specifically WAKEUP, see Section 5.7.3.3, *Reset Electrical Data and Timing*.

5.7.14 SAR ADC (10-Bit)

The device includes a 10-bit SAR ADC using a switched capacitor architecture which converts an analog input signal to a digital value at a maximum rate of 62.5-k samples per second (ksps) for use by the DSP. This SAR module supports six channels that are connected to four general purpose analog pins (GPAIN [3:0]) which can be used as general purpose outputs.

The device SAR supports the following features:

- Up to 62.5 ksps (2-MHz clock with 32 cycles per conversion)
- Single conversion and continuous back-to-back conversion modes
- Interrupt driven or polling conversion or DMA event generation
- Internal configurable bandgap reference voltages of 1 V or 0.8 V; or external V_{ref} of V_{DDA_ANA}
- One 3.6-V Tolerant analog input (GPAIN0) with internal voltage division for conversion of battery voltage
- Software controlled power down
- Individually configurable general-purpose digital outputs

5.7.14.1 SAR ADC Electrical Data and Timing

Table 5-54. Switching Characteristics Over Recommended Operating Conditions for ADC Characteristics

NO.	PARAMETER		CV_{DD} = 1.4 V CV_{DD} = 1.3 V CV_{DD} = 1.05 V			UNIT
			MIN	TYP	MAX	
1	$t_{C(SCLC)}$	Cycle time, ADC internal conversion clock			2	MHz
3	$t_{d(CONV)}$	Delay time, ADC conversion time			$32t_{C(SCLC)}$	ns
4	S_{DNL}	Static differential non-linearity error (DNL measured for 9 bits)		±0.6		LSB
5	S_{INL}	Static integral non-linearity error		±1		LSB
6	Z_{set}	Zero-scale offset error (INL measured for 9 bits)			2	LSB
7	F_{set}	Full-scale offset error			2	LSB
8		Analog input impedance	1			MΩ
9		Signal-to-noise ratio		54		dB

5.7.15 Serial Port Interface (SPI)

The device serial port interface (SPI) is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI supports multi-chip operation of up to four SPI slave devices. The SPI can operate as a master device only, slave mode is not supported. **Note:** The SPI is not supported by the device DMA controller, so DMA cannot be used in transferring data between the SPI and the on-chip RAM.

The SPI is normally used for communication between the DSP and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EEPROMs, and analog-to-digital converters.

The SPI has the following features:

- Programmable divider for serial data clock generation
- Four pin interface (SPI_CLK, SPI_CSn, SPI_RX, and SPI_TX)
- Programmable data length (1 to 32 bits)
- 4 external chip select signals
- Programmable transfer or frame size (1 to 4096 characters)
- Optional interrupt generation on character completion
- Optional interrupt generation on frame completion
- Programmable SPI_CSn to SPI_TX delay from 0 to 3 SPI_CLK cycles
- Programmable signal polarities
- Programmable active clock edge
- Internal loopback mode for testing

5.7.15.1 SPI Electrical Data and Timing

Table 5-55. Timing Requirements for SPI Inputs (see Figure 5-40 through Figure 5-43)

NO.				CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
				MIN	MAX	MIN	MAX	
4	$t_{C(SCLK)}$	Cycle time, SPI_CLK		4P (1) (2)		4P (1) (2)		ns
5	$t_{w(SCLKH)}$	Pulse duration, SPI_CLK high		30		19		ns
6	$t_{w(SCLKL)}$	Pulse duration, SPI_CLK low		30		19		ns
7	$t_{su(SRXV-SCLK)}$	Setup time, SPI_RX valid before SPI_CLK high	Modes 0, 2, and 3	16.1		13.9		ns
		Setup time, SPI_RX valid before SPI_CLK low	Mode 1	16.1		13.9		ns
8	$t_{h(SCLK-SRXV)}$	Hold time, SPI_RX valid after SPI_CLK high	Modes 0 and 3	0		0		ns
		Hold time, SPI_RX valid after SPI_CLK low	Modes 1 and 2	0		0		ns

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.

Table 5-56. Switching Characteristics Over Recommended Operating Conditions for SPI Outputs [I/O = 2.75 and 3.3 V] (see Figure 5-40 through Figure 5-43)

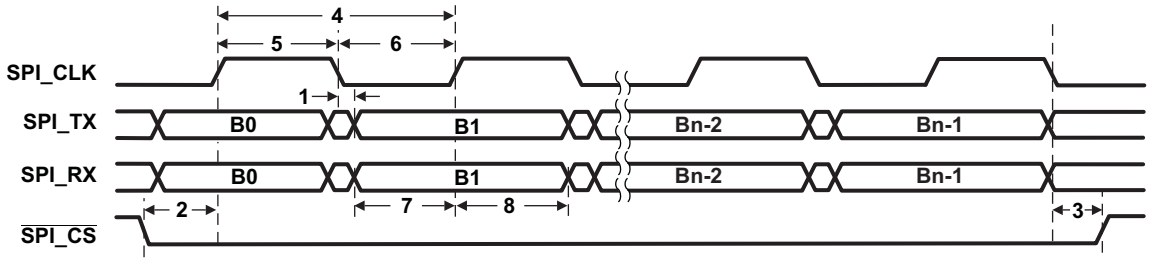
NO.	PARAMETER			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
				MIN	MAX	MIN	MAX	
1	$t_{d(SCLK-STXV)}$	Delay time, SPI_CLK low to SPI_TX valid	Modes 0 and 3	-4.2	8.9	-4.9	5.3	ns
		Delay time, SPI_CLK high to SPI_TX valid	Modes 1 and 2	-4.2	8.9	-4.9	5.3	ns
2	$t_{d(SPICS-SCLK)}$	Delay time, $\overline{SPI\_CS}$ active to SPI_CLK active			t_c - 8 + D(1)		t_c - 8 + D(1)	ns
3	$t_{oh(SCLKI-SPICSI)}$	Output hold time, $\overline{SPI\_CS}$ inactive to SPI_CLK inactive		$0.5t_c$ - 1.9		$0.5t_c$ - 1.9		ns

(1) D is the programable data delay in ns. Data delay can be programmed to 0, 1, 2, or 3 SPICLK clock cycles.

Table 5-57. Switching Characteristics Over Recommended Operating Conditions for SPI Outputs [I/O = 1.8 V] (see Figure 5-40 through Figure 5-43)

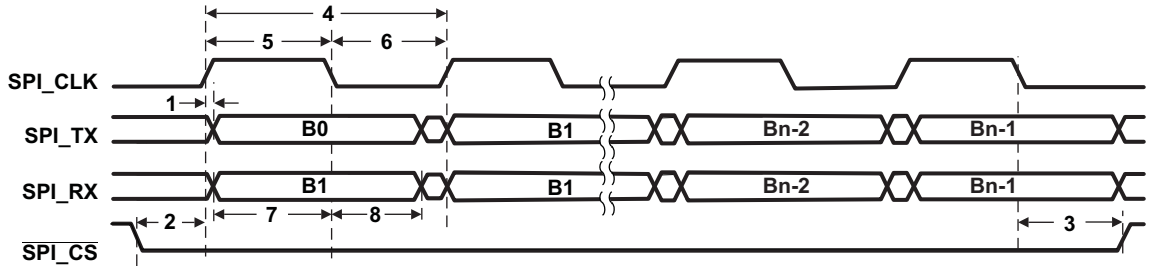
NO.	PARAMETER			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		UNIT
				MIN	MAX	MIN	MAX	
1	$t_{d(SCLK-STXV)}$	Delay time, SPI_CLK low to SPI_TX valid	Modes 0 and 3	-6.7	8.9	-6.7	5.8	ns
		Delay time, SPI_CLK high to SPI_TX valid	Modes 1 and 2	-6.7	8.9	-6.7	5.8	ns
2	$t_{d(SPICS-SCLK)}$	Delay time, $\overline{SPI\_CS}$ active to SPI_CLK active			t_c - 9.2 + D(1)		t_c - 8 + D(1)	ns
3	$t_{oh(SCLKI-SPICSI)}$	Output hold time, $\overline{SPI\_CS}$ inactive to SPI_CLK inactive		$0.5t_c$ - 1.9		$0.5t_c$ - 1.9		ns

(1) D is the programable data delay in ns. Data delay can be programmed to 0, 1, 2, or 3 SPICLK clock cycles.



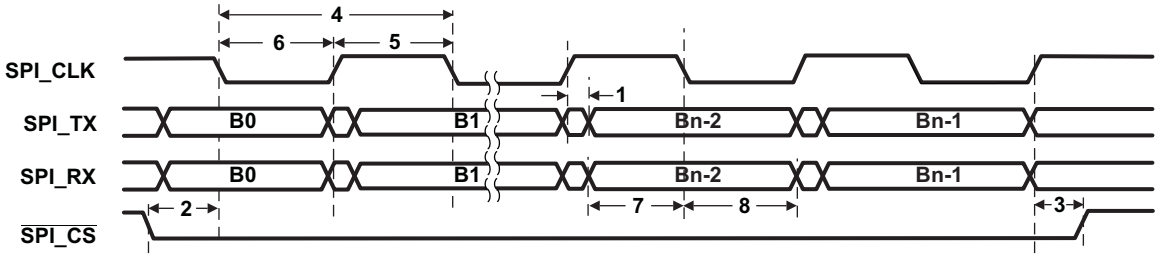
A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 5-40. SPI Mode 0 Transfer (CKP*n* = 0, CKPH*n* = 0)



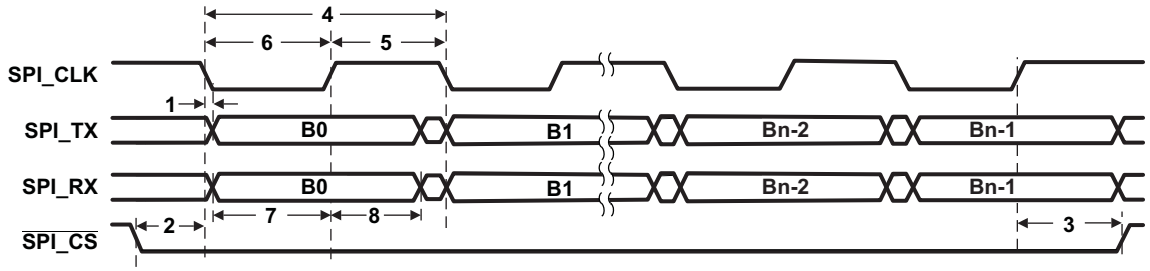
A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 5-41. SPI Mode 1 Transfer (CKP*n* = 0, CKPH*n* = 1)



A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 5-42. SPI Mode 2 Transfer (CKP*n* = 1, CKPH*n* = 0)



A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 5-43. SPI Mode 3 Transfer (CKP*n* = 1, CKPH*n* = 1)

5.7.16 Timers

The device has three 32-bit software programmable Timers. Each timer can be used as a general-purpose (GP) timer. Timer2 can be configured as either a GP or a Watchdog (WD) or both. General-purpose timers are typically used to provide interrupts to the CPU to schedule periodic tasks or a delayed task. A watchdog timer is used to reset the CPU in case it gets into an infinite loop. The GP timers are 32-bit timers with a 13-bit prescaler that can divide the CPU clock and uses this scaled value as a reference clock. These timers can be used to generate periodic interrupts. The Watchdog Timer is a 16-bit counter with a 16-bit prescaler used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

The device Timers support the following:

- 32-bit Programmable Countdown Timer
- 13-bit Prescaler Divider
- Timer Modes:
  - 32-bit General-Purpose Timer
  - 32-bit Watchdog Timer (Timer2 only)
- Auto Reload Option
- Generates a single interrupt to the CPU, which can be configured as a timer interrupt (TINT) or as a non-maskable interrupt (NMI). The interrupt is individually latched to determine which timer triggered the interrupt.
- Generates an active low pulse to the hardware reset (Watchdog *only*)
- Interrupt can be used for DMA Event

5.7.17 Universal Asynchronous Receiver and Transmitter (UART)

The UART performs serial-to-parallel conversions on data received from an external peripheral device and parallel-to-serial conversions on data transmitted to an external peripheral device via a serial bus.

The device has one UART peripheral with the following features:

- Programmable baud rates (frequency pre-scale values from 1 to 65535)
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no PARITY bit generation and detection
  - 1, 1.5, or 2 STOP bit generation
- 16-byte depth transmitter and receiver FIFOs:
  - The UART can be operated with or without the FIFOs
  - 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- DMA signaling capability for both received and transmitted data
- CPU interrupt capability for both received and transmitted data
- False START bit detection
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, and framing error simulation
- Programmable autoflow control using CTS and RTS signals

5.7.17.1 UART Electrical Data and Timing [Receive and Transmit]

Table 5-58. Timing Requirements for UART Receive(1)(2) (see Figure 5-44)

NO.			CV_{DD} = 1.05/1.3/1.4 V		UNIT
			MIN	MAX	
4	$t_{w(URXDB)}$	Pulse duration, receive data bit (UART_RXD) [15/30 pF]	U - 3.5	U + 3	ns
5	$t_{w(URXSB)}$	Pulse duration, receive start bit [15/30 pF]	U - 3.5	U + 3	ns

(1) U = UART baud time = 1/programmed baud rate.
(2) These parametric values are measured at DV_{DDIO} = 3.3 V, 2.75 V, and 1.8 V.

Table 5-59. Switching Characteristics Over Recommended Operating Conditions for UART Transmit(1) (2) (see Figure 5-44)

NO.	PARAMETER		CV_{DD} = 1.05/1.3/1.4 V		UNIT
			MIN	MAX	
1	$f_{(baud)}$	Maximum programmable bit rate		fmax/16	MHz
2	$t_{w(UTXDB)}$	Pulse duration, transmit data bit (UART_TXD) [15/30 pF]	U - 3.5	U + 4	ns
3	$t_{w(UTXSB)}$	Pulse duration, transmit start bit [15/30 pF]	U - 3.5	U + 4	ns

(1) U = UART baud time = 1/programmed baud rate.
(2) These parametric values are measured at DV_{DDIO} = 3.3 V, 2.75 V, and 1.8 V.

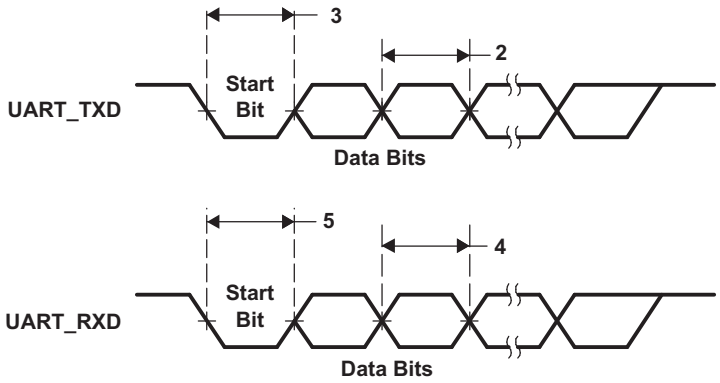


Figure 5-44. UART Transmit and Receive Timing

5.7.18 Universal Host-Port Interface (UHPI)

The device includes a user-configurable 16-bit universal host-port interface (UHPI16). The UHPI provides a parallel port interface through which an external host processor can directly access the processor's resources (configuration and program and data memories). The external host device is asynchronous to the CPU clock and functions as a master to the UHPI interface. The UHPI enables a host device and the processor to exchange information via internal memory. Dedicated address (UHPIA) and data (UHPID) registers within the UHPI provide the data path between the external host interface and the processor resources. A UHPI control register (UHPIC) is available to the host and the CPU for various configuration and interrupt functions.

5.7.18.1 UHPI Electrical Data and Timing

Table 5-60. Timing Requirements for Host-Port Interface, DV_{DDIO} = 3.3/2.75 V

NO.			DV_{DDIO} = 3.3/2.75 V				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		
			MIN	MAX	MIN	MAX	
1	$t_{su(SELV-HSTBL)}$	Setup time, select signals(1) valid before $\overline{HSTROBE}$ low	6.5		5		ns
2	$t_{h(HSTBL-SELV)}$	Hold time, select signals(1) valid after $\overline{HSTROBE}$ low	3		2		ns
3	$t_{w(HSTBL)}$	Pulse duration, $\overline{HSTROBE}$ active low	19		17		ns
4	$t_{w(HSTBH)}$	Pulse duration, $\overline{HSTROBE}$ inactive high between consecutive accesses	2P(2)		2P(2)		ns
11	$t_{su(HDV-HSTBH)}$	Setup time, host data valid before $\overline{HSTROBE}$ high	7.8		5		ns
12	$t_{h(HSTBH-HDV)}$	Hold time, host data valid after $\overline{HSTROBE}$ high	3.3		2.5		ns
13	$t_{h(HRDYL-HSTBH)}$	Hold time, $\overline{HSTROBE}$ high after UHPI_HRDY high. $\overline{HSTROBE}$ should not be inactivated until UHPI_HRDY is active (high); otherwise, UHPI writes will not complete properly.	2		2		ns

(1) Select signals include: UHPI_HCNTL[1:0], UHPI_HR_NW and UHPI_HHWIL.
(2) P = SYSCLK period in ns. For example, when the CPU core is clocked at 200 MHz, P = 5 ns.

Table 5-61. Timing Requirements for Host-Port Interface, DV_{DDIO} = 1.8 V

NO.			DV_{DDIO} = 1.8 V				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		
			MIN	MAX	MIN	MAX	
1	$t_{su(SELV-HSTBL)}$	Setup time, select signals(1) valid before $\overline{HSTROBE}$ low	7.3		5		ns
2	$t_{h(HSTBL-SELV)}$	Hold time, select signals(1) valid after $\overline{HSTROBE}$ low	3		2		ns
3	$t_{w(HSTBL)}$	Pulse duration, $\overline{HSTROBE}$ active low	24		19		ns
4	$t_{w(HSTBH)}$	Pulse duration, $\overline{HSTROBE}$ inactive high between consecutive accesses	2P(2)		2P(2)		ns
11	$t_{su(HDV-HSTBH)}$	Setup time, host data valid before $\overline{HSTROBE}$ high	8.6		5		ns
12	$t_{h(HSTBH-HDV)}$	Hold time, host data valid after $\overline{HSTROBE}$ high	3.3		2.5		ns
13	$t_{h(HRDYL-HSTBH)}$	Hold time, $\overline{HSTROBE}$ high after UHPI_HRDY high. $\overline{HSTROBE}$ should not be inactivated until UHPI_HRDY is active (high); otherwise, UHPI writes will not complete properly.	2		2		ns

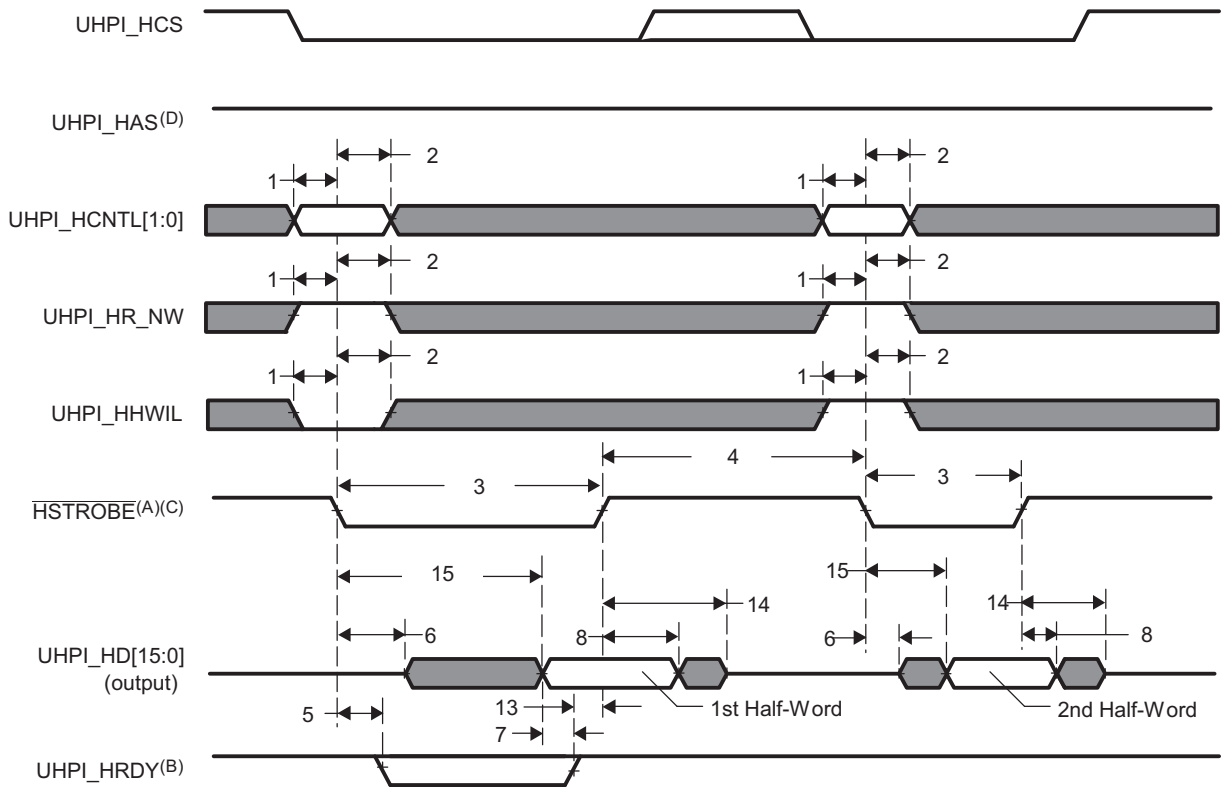
(1) Select signals include: UHPI_HCNTL[1:0], UHPI_HR_NW and UHPI_HHWIL.
(2) P = SYSCLK period in ns. For example, when the CPU core is clocked at 200 MHz, P = 5 ns.

Table 5-62. Switching Characteristics Over Recommended Operating Conditions for Host-Port Interface, DV_{DDIO} = 3.3/2.75 V

NO.	PARAMETER			DV_{DDIO} = 3.3/2.75 V				UNIT
				CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		
				MIN	MAX	MIN	MAX	
5	$t_{d(HSTBL-HRDYV)}$	Delay time, HSTROBE low to UHPI_HRDY valid	For UHPI Write, UHPI_HRDY can go low (*not ready*) for these UHPI Write conditions; otherwise, UHPI_HRDY stays high (*ready*): *Case 1*: Back-to-back HPIA writes (can be either first or second half-word) *Case 2*: HPIA write following a PREFETCH command (can be either first or second half-word) *Case 3*: HPID write when FIFO is full or flushing (can be either first or second half-word) *Case 4*: HPIA write and Write FIFO not empty For UHPI Read, UHPI_HRDY can go low (*not ready*) for these UHPI Read conditions: *Case 1*: UHPID read (with auto-increment) and data not in Read FIFO (can only happen to first half-word of HPID access) *Case 2*: First half-word access of HPID Read without auto-increment For UHPI Read, UHPI_HRDY stays high (*ready*) for these UHPI Read conditions: *Case 1*: HPID read with auto-increment and data is already in Read FIFO (applies to either half-word of HPID access) *Case 2*: HPID read without auto-increment and data is already in Read FIFO (always applies to second half-word of HPID access) *Case 3*: HPIC or HPIA read (applies to either half-word access)	0	22.3	0	15.5	ns
6	$t_{en(HSTBL-HDLZ)}$	Enable time, UHPI_HD driven from HSTROBE low		1.5		1.5		ns
7	$t_{d(HRDYL-HDV)}$	Delay time, UHPI_HRDY high to HD valid			0		1.1	ns
8	$t_{oh(HSTBH-HDV)}$	Output hold time, UHPI_HD valid after HSTROBE high		1.5		1.5		ns
14	$t_{dis(HSTBH-HDHZ)}$	Disable time, HD high-impedance from HSTROBE high			24.3		15.8	ns
15	$t_{d(HSTBL-HDV)}$	Delay time, HSTROBE low to HD valid	For UHPI Read. Applies to conditions where data is already residing in HPID/FIFO: *Case 1*: HPIC or HPIA read *Case 2*: First half-word of HPID read with auto-increment and data is already in Read FIFO *Case 3*: Second half-word of HPID read with or without auto-increment		24.3		15.8	ns
18	$t_{d(HSTBH-HRDYV)}$	Delay time, HSTROBE high to UHPI_HRDY valid	For UHPI Write, UHPI_HRDY can go low (*not ready*) for these UHPI Write conditions; otherwise, UHPI_HRDY stays high (*ready*): *Case 1*: HPID write when Write FIFO is full (can happen to either half-word) *Case 2*: HPIA write (can happen to either half-word) *Case 3*: HPID write without auto-increment (only happens to second half-word)		24.3		15.8	ns

Table 5-63. Switching Characteristics Over Recommended Operating Conditions for Host-Port Interface, DV_{DDIO} = 1.8 V

NO.	PARAMETER			DV_{DDIO} = 1.8 V				UNIT
				CV_{DD} = 1.05 V		CV_{DD} = 1.3/1.4 V		
				MIN	MAX	MIN	MAX	
5	$t_{d(HSTBL-HRDYV)}$	Delay time, HSTROBE low to UHPI_HRDY valid	For UHPI Write, UHPI_HRDY can go low (*not ready*) for these UHPI Write conditions; otherwise, UHPI_HRDY stays high (*ready*): *Case 1*: Back-to-back HPIA writes (can be either first or second half-word) *Case 2*: HPIA write following a PREFETCH command (can be either first or second half-word) *Case 3*: HPID write when FIFO is full or flushing (can be either first or second half-word) *Case 4*: HPIA write and Write FIFO not empty For UHPI Read, UHPI_HRDY can go low (*not ready*) for these UHPI Read conditions: *Case 1*: UHPID read (with auto-increment) and data not in Read FIFO (can only happen to first half-word of HPID access) *Case 2*: First half-word access of HPID Read without auto-increment For UHPI Read, UHPI_HRDY stays high (*ready*) for these UHPI Read conditions: *Case 1*: HPID read with auto-increment and data is already in Read FIFO (applies to either half-word of HPID access) *Case 2*: HPID read without auto-increment and data is already in Read FIFO (always applies to second half-word of HPID access) *Case 3*: HPIC or HPIA read (applies to either half-word access)	0	26.5	0	19	ns
6	$t_{en(HSTBL-HDLZ)}$	Enable time, UHPI_HD driven from HSTROBE low		1.5		1.5		ns
7	$t_{d(HRDYL-HDV)}$	Delay time, UHPI_HRDY high to HD valid			1.1		1.1	ns
8	$t_{oh(HSTBH-HDV)}$	Output hold time, UHPI_HD valid after HSTROBE high		1.5		1.5		ns
14	$t_{dis(HSTBH-HDHZ)}$	Disable time, HD high-impedance from HSTROBE high			26.8		20.5	ns
15	$t_{d(HSTBL-HDV)}$	Delay time, HSTROBE low to HD valid	For UHPI Read. Applies to conditions where data is already residing in HPID or FIFO: *Case 1*: HPIC or HPIA read *Case 2*: First half-word of HPID read with auto-increment and data is already in Read FIFO *Case 3*: Second half-word of HPID read with or without auto-increment		26.8		20.5	ns
18	$t_{d(HSTBH-HRDYV)}$	Delay time, HSTROBE high to UHPI_HRDY valid	For UHPI Write, UHPI_HRDY can go low (*not ready*) for these UHPI Write conditions; otherwise, UHPI_HRDY stays high (*ready*): *Case 1*: HPID write when Write FIFO is full (can happen to either half-word) *Case 2*: HPIA write (can happen to either half-word) *Case 3*: HPID write without auto-increment (only happens to second half-word)		26.5		19	ns



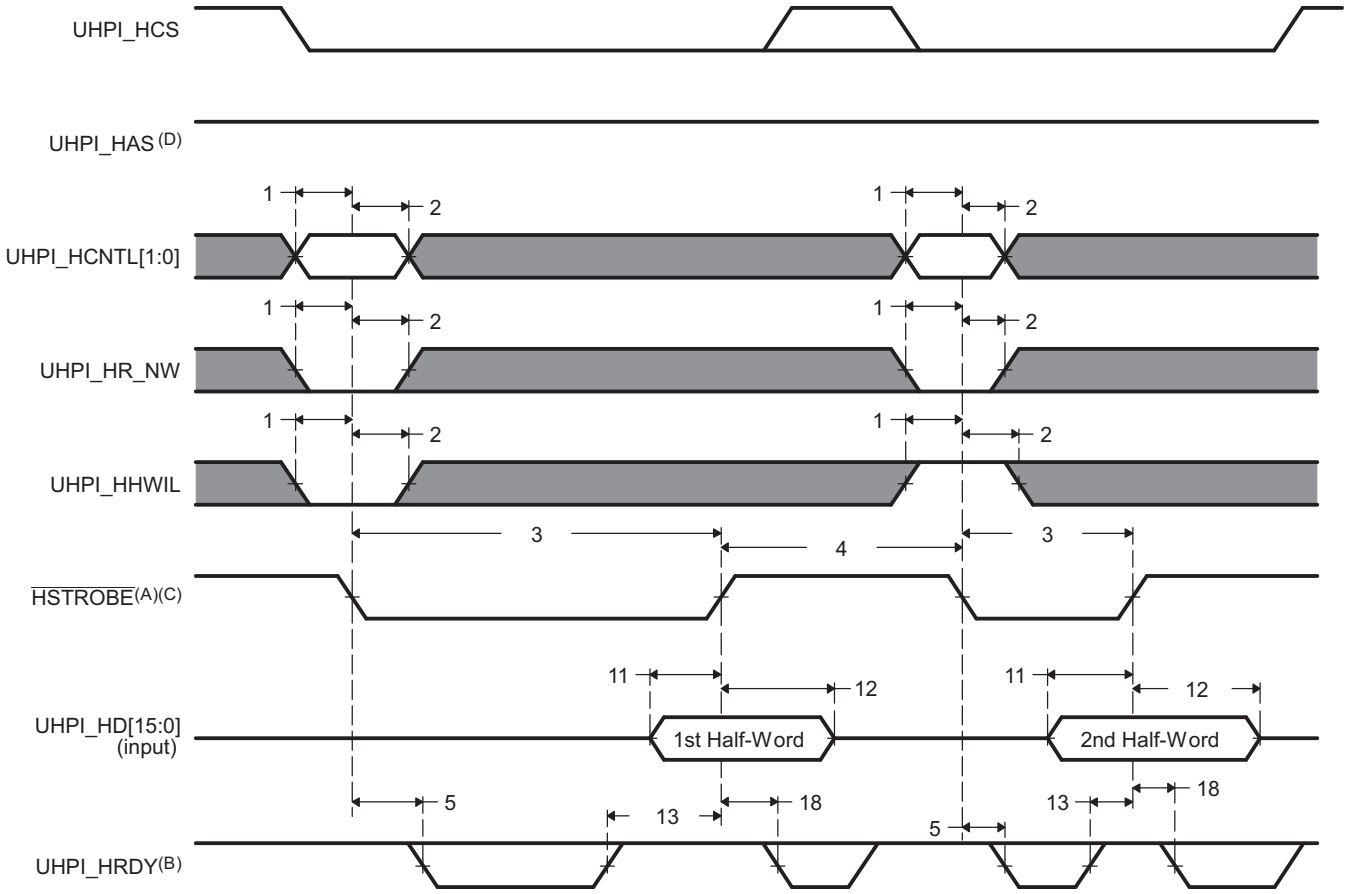
A. HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(UHPI_HDS1 XOR UHPI_HDS2)] OR UHPI_HCS.

B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on UHPI_HRDY may or may not occur. For more information on the UHPI peripheral, see the *UHPI* chapter in the *TMS320C5517 Technical Reference Manual* [literature number SPRUH16].

C. Typical UHPI_HCS behavior is reflected when HSTROBE assertion is caused by UHPI_HDS1 or UHPI_HDS2. UHPI_HCS timing requirements are reflected by parameters for HSTROBE.

D. For proper UHPI operation, UHPI_HAS must be pulled up via an external resistor.

Figure 5-45. UHPI Read Timing (UHPI_HAS Not Used, Tied High)



A. HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(UHPI_HDS1 XOR UHPI_HDS2)] OR UHPI_HCS.

B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on UHPI_HRDY may or may not occur. For more information on the UHPI peripheral, see the *UHPI* chapter in the *TMs320C5517 Technical Reference Manual* [literature number SPRUH16].

C. Typical UHPI_HCS behavior is reflected when HSTROBE assertion is caused by UHPI_HDS1 or UHPI_HDS2. UHPI_HCS timing requirements are reflected by parameters for HSTROBE.

D. For proper UHPI operation, UHPI_HAS must be pulled up via an external resistor.

Figure 5-46. UHPI Write Timing (UHPI_HAS Not Used, Tied High)

5.7.19 Universal Serial Bus (USB) 2.0 Controller

The device USB2.0 peripheral supports the following features:

- USB2.0 peripheral at speeds high-speed (480Mb/s) and full-speed (12Mb/s)
- All transfer modes (control, bulk, interrupt, and isochronous mode)
- 4 Transmit (TX) and 4 Receive (RX) Endpoints in addition to Control Endpoint 0
- FIFO RAM
  - 4K endpoint
  - Programmable size
- Integrated USB2.0 High Speed PHY
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB

The USB2.0 peripheral on this device, does *not* support:

- Host Mode (Peripheral and Device Modes supported *only*)
- On-Chip Charge Pump
- On-the-Go (OTG) Mode

5.7.19.1 USB 2.0 Electrical Data and Timing

Table 5-64. Switching Characteristics Over Recommended Operating Conditions for USB 2.0 (see Figure 5-47)

NO.	PARAMETER		CV_{DD} = 1.05 V CV_{DD} = 1.3 V CV_{DD} = 1.4 V				UNIT
			FULL SPEED 12 Mbps		HIGH SPEED 480 Mbps(1)		
			MIN	MAX	MIN	MAX	
1	$t_{r(D)}$	Rise time, USB_DP and USB_DM signals(2)	4	20	0.5		ns
2	$t_{f(D)}$	Fall time, USB_DP and USB_DM signals(2)	4	20	0.5		ns
3	t_{rfM}	Rise and Fall time, matching(3)	90	111	–	–	%
4	V_{CRS}	Output signal cross-over voltage(2)	1.3	2	–	–	V
7	$t_{w(EOPT)}$	Pulse duration, EOP transmitter(4)	160	175	–	–	ns
8	$t_{w(EOPR)}$	Pulse duration, EOP receiver(4)	82		–		ns
9	$t_{(DRATE)}$	Data Rate		12		480	Mb/s
10	Z_{DRV}	Driver Output Resistance	40.5	49.5	40.5	49.5	Ω
11	Z_{INP}	Receiver Input Impedance	100k		-	-	Ω

(1) For more detailed information, see the Universal Serial Bus Specification, Revision 2.0, Chapter 7.
(2) Full Speed and High Speed C_L = 50 pF
(3) $t_{RFM} = (t_r/t_f) \times 100$. [Excluding the first transaction from the Idle state.]
(4) Must accept as valid EOP

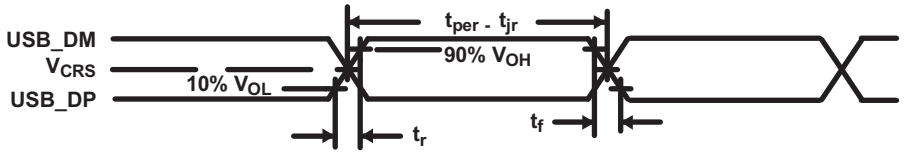


Figure 5-47. USB2.0 Integrated Transceiver Interface Timing

5.7.20 Emulation and Debug

5.7.20.1 Debugging Considerations

5.7.20.1.1 Pullup and Pulldown Resistors

Proper board design should ensure that input pins to the DSP are always at a valid logic level and not floating. This may be achieved via pullup and pulldown resistors. The DSP features internal pullup (IPU) and internal pulldown (IPD) resistors on many pins to eliminate the need, unless otherwise noted, for external pullup and pulldown resistors.

An external pullup and pulldown resistor may need to be used in the following situations:

- Configuration Pins: An external pullup and pulldown resistor is recommended to set the desired value or state (see the configuration pins listed in Table 5-5, *Default Functions Affected by Device Configuration Pins*). Note that some configuration pins must be connected directly to ground or to a specific supply voltage.
- Input Pins (I, I/O, I/O/Z): They are required to be driven at all times. To achieve the lowest power, input pins must not be allowed to float. When they are configured as input or tri-stated, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD and IPU, if applicable.
- Other Input Pins: If the IPU and IPD does not match the desired value or state, use an external pullup and pulldown resistor to pull the signal to the opposite rail.

For the configuration pins (listed in Table 5-5, *Default Functions Affected by Device Configuration Pins*), if they are both routed out and 3-stated (not driven), it is strongly recommended that an external pullup and pulldown resistor be implemented. In addition, applying external pullup and pulldown resistors on the configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

When an external pullup or pulldown resistor is used on a pin, the pin's internal pullup or pulldown resistor should be disabled through the Pullup and Pulldown Inhibit Registers (PUDINHIBR1, 2, 3, 4, 5, 6, and 7) to minimize power consumption.

Tips for choosing an external pullup and pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Make sure to include the leakage currents of all the devices connected to the net, as well as any internal pullup or pulldown (IPU and IPD) resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest V_{IL} level of all inputs connected to the net. For a pullup resistor, this should be above the highest V_{IH} level of all inputs on the net. A reasonable choice would be to target the V_{OL} or V_{OH} levels for the logic family of the limiting device; which, by definition, have margin to the V_{IL} and V_{IH} levels.
- Select a pullup and pulldown resistor with the largest possible value; but, which can still ensure that the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current plus, any other internal and external pullup and pulldown resistors on the net.
- For bidirectional nets, there is an additional consideration which sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the DV_{DD} rail.

For most systems, a 1-kΩ resistor can be used to oppose the IPU and IPD while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For most systems, a 20-kΩ resistor can be used to compliment the IPU and IPD on the configuration pins while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For more detailed information on input current (I_I), and the low- and high-level input voltages (V_{IL} and V_{IH}) for the device DSP, see Section 5.3.2, *Electrical Characteristics*.

For the internal pullup and pulldown resistors for all device pins, see the peripheral and system-specific signal descriptions table in this document.

5.7.20.1.2 Bus Holders

The device has special I/O bus-holder structures to ensure pins are not left floating when CV_{DD} power is removed while I/O power is applied. When CV_{DD} is "ON", the bus-holders are disabled and the internal pullups or pulldowns, if applicable, function normally. But when CV_{DD} is "OFF" and the I/O supply is "ON", the bus-holders become enabled and any applicable internal pullups and pulldowns are disabled.

The bus-holders are weak drivers on the pin and, for as long as CV_{DD} is "OFF" and I/O power is "ON", they hold the last state on the pin. If an external device is strongly driving the device I/O pin to the opposite state then the bus-holder will flip state to match the external driver and DC current will stop.

This bus-holder feature prevents unnecessary power consumption when CV_{DD} is "OFF"and I/O supply is "ON". For example, current caused by undriven pins (input buffer oscillation) or DC current flowing through pullups or pulldowns.

If external pullup or pulldown resistors are implemented, then care should be taken that those pullup and pulldown resistors can exceed the internal bus-holder's max current and thereby cause the bus-holder to flip state to match the state of the external pullup or pulldown. Otherwise, DC current will flow unnecessarily. When CV_{DD} power is applied, the bus holders are disabled (for further details on bus holders, see Section 5.7.2.3, *Digital I/O Behavior When Core Power (CV_{DD}) is Down*).

5.7.20.1.3 CLKOUT Pin

For debug purposes, the DSP includes a CLKOUT pin which can be used to tap different clocks within the clock generator. The SRC bits of the CLKOUT Configuration Register (CLKOUTCR) can be used to specify the source for the CLKOUT pin.

Note: The bootloader disables the CLKOUT pin via CLKOFF bit in the ST3_55 CPU register.

For more information on the ST3_55 CPU register, see the *C55x 3.0 CPU* Reference Guide (literature number: SWPU073).

5.7.21 IEEE 1149.1 JTAG

The JTAG interface is used for Boundary-Scan testing and emulation of the device.

$\overline{\text{TRST}}$ should only to be deasserted when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality.

The device includes an internal pulldown (IPD) on the $\overline{\text{TRST}}$ pin to ensure that $\overline{\text{TRST}}$ will always be asserted upon power up and the device's internal emulation logic will always be properly initialized. An external pulldown should also be added to ensure proper device operation when an emulation or boundary scan JTAG controller is not connected to the JTAG pins. JTAG controllers from Texas Instruments actively drive $\overline{\text{TRST}}$ high. However, some third-party JTAG controllers may not drive $\overline{\text{TRST}}$ high but expect the use of a pullup resistor on $\overline{\text{TRST}}$. When using this type of JTAG controller, assert $\overline{\text{TRST}}$ to initialize the device after powerup and externally drive $\overline{\text{TRST}}$ high before attempting any emulation or boundary scan operations. The device will not operate properly if $\overline{\text{TRST}}$ is not asserted low during powerup.

5.7.21.1 JTAG Test_port Electrical Data and Timing

Table 5-65. Timing Requirements for JTAG Test Port (see Figure 5-48)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V CV_{DD} = 1.4 V		UNIT
			MIN	MAX	
2	$t_{c(TCK)}$	Cycle time, TCK	60		ns
3	$t_{w(TCKH)}$	Pulse duration, TCK high	24		ns
4	$t_{w(TCKL)}$	Pulse duration, TCK low	24		ns
5	$t_{su(TDIV-TCKH)}$	Setup time, TDI valid before TCK high	10		ns
6	$t_{su(TMSV-TCKH)}$	Setup time, TMS valid before TCK high	6		ns
7	$t_{h(TCKH-TDIV)}$	Hold time, TDI valid after TCK high	5		ns
8	$t_{h(TCKH-TDIV)}$	Hold time, TMS valid after TCK high	4		ns

Table 5-66. Switching Characteristics Over Recommended Operating Conditions for JTAG Test Port (see Figure 5-48)

NO.	PARAMETER		CV_{DD} = 1.05 V CV_{DD} = 1.3 V CV_{DD} = 1.4 V		UNIT
			MIN	MAX	
1	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid		30.5	ns

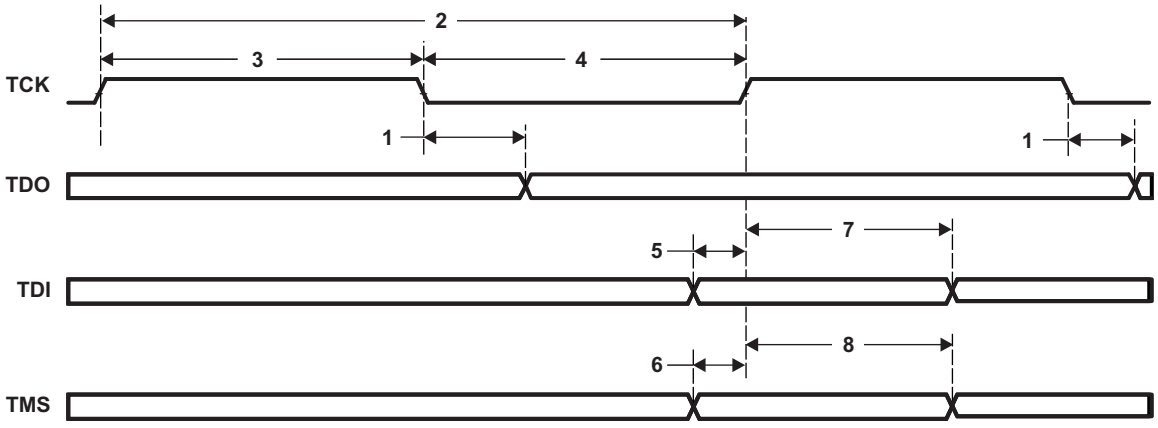


Figure 5-48. JTAG Test-Port Timing

6 Detailed Description

6.1 CPU

This fixed-point digital signal processor (DSP) is based on the C55x CPU 3.3 generation processor core. The C55x DSP architecture achieves high performance and low power through increased parallelism and total focus on power savings. The CPU supports an internal bus structure that is composed of one program bus, three data read buses (one 32-bit data read bus and two 16-bit data read buses), two 16-bit data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to four data reads and two data writes in a single cycle. Each DMA controller can perform one 32-bit data transfer per cycle, in parallel and independent of the CPU activity.

The C55x CPU provides two multiply-accumulate (MAC) units, each capable of 17-bit x 17-bit multiplication in a single cycle. A central 40-bit arithmetic and logic unit (ALU) is supported by an additional 16-bit ALU. Use of the ALUs is under instruction set control, providing the ability to optimize parallel activity and power consumption. These resources are managed in the Address Unit (AU) and Data Unit (DU) of the C55x CPU.

The C55x DSP generation supports a variable byte width instruction set for improved code density. The Instruction Unit (IU) performs 32-bit program fetches from internal or external memory, stores them in a 128-byte Instruction Buffer Queue, and queues instructions for the Program Unit (PU). The Program Unit decodes the instructions, directs tasks to AU and DU resources, and manages the fully protected pipeline. Predictive branching capability avoids pipeline flushes on execution of conditional instruction calls.

For more detailed information on the CPU, see the *C55x CPU 3.0 CPU* Reference Guide [literature number SWPU073].

The C55x core of the device can address 16M bytes of unified data and program space. The core also addresses 64K words of I/O space and includes three types of on-chip memory: 128 KB read-only memory (ROM), 256 KB single-access random access memory (SARAM), 64 KB dual-access random access memory (DARAM). The memory map is shown in Figure 6-1 .

6.2 Memory

6.2.1 Internal Memory

6.2.1.1 On-Chip Dual-Access RAM (DARAM)

The DARAM is located in the byte address range 000000h - 00FFFFh and is composed of eight blocks of 4K words each (see Table 6-1). Each DARAM block can support two accesses per cycle (two reads, two writes, or a read and a write). The DARAM can be accessed by the internal program, data, or DMA buses.

Table 6-1. DARAM Blocks

CPU BYTE ADDRESS RANGE	DMA CONTROLLER BYTE ADDRESS RANGE	MEMORY BLOCK
000000h – 001FFFh	0001 0000h – 0001 1FFFh	DARAM 0 (1)
002000h – 003FFFh	0001 2000h – 0001 3FFFh	DARAM 1
004000h – 005FFFh	0001 4000h – 0001 5FFFh	DARAM 2
006000h – 007FFFh	0001 6000h – 0001 7FFFh	DARAM 3
008000h – 009FFFh	0001 8000h – 0001 9FFFh	DARAM 4
00A000h – 00BFFFh	0001 A000h – 0001 BFFFh	DARAM 5
00C000h – 00DFFFh	0001 C000h – 0001 DFFFh	DARAM 6
00E000h – 00FFFFh	0001 E000h – 0001 FFFFh	DARAM 7

(1) The first 192 bytes are reserved for memory-mapped registers (MMRs). See Figure 6-1 , Memory Map Summary.

6.2.1.2 On-Chip Single-Access RAM (SARAM)

The SARAM is located at the byte address range 010000h – 04FFFFh and is composed of 32 blocks of 4K words each (see Table 6-2). Each SARAM block can support one access per cycle (one read or one write). SARAM can be accessed by the internal program, data, or DMA buses. SARAM is also accessed by the USB DMA buses.

Table 6-2. SARAM Blocks

CPU BYTE ADDRESS RANGE	DMA and USB CONTROLLER BYTE ADDRESS RANGE	MEMORY BLOCK
010000h - 011FFFh	0009 0000h – 0009 1FFFh	SARAM 0
012000h - 013FFFh	0009 2000h – 0009 3FFFh	SARAM 1
014000h - 015FFFh	0009 4000h – 0009 5FFFh	SARAM 2
016000h - 017FFFh	0009 6000h – 0009 7FFFh	SARAM 3
018000h - 019FFFh	0009 8000h – 0009 9FFFh	SARAM 4
01A000h - 01BFFFh	0009 A000h – 0009 BFFFh	SARAM 5
01C000h - 01DFFFh	0009 C000h – 0009 DFFFh	SARAM 6
01E000h - 01FFFFh	0009 E000h – 0009 FFFFh	SARAM 7
020000h - 021FFFh	000A 0000h – 000A 1FFFh	SARAM 8
022000h - 023FFFh	000A 2000h – 000A 3FFFh	SARAM 9
024000h - 025FFFh	000A 4000h – 000A 5FFFh	SARAM 10
026000h - 027FFFh	000A 6000h – 000A 7FFFh	SARAM 11
028000h - 029FFFh	000A 8000h – 000A 9FFFh	SARAM 12
02A000h - 02BFFFh	000A A000h – 000A BFFFh	SARAM 13
02C000h - 02DFFFh	000A C000h – 000A DFFFh	SARAM 14
02E000h - 02FFFFh	000A E000h – 000A FFFFh	SARAM 15
030000h - 031FFFh	000B 0000h – 000B 1FFFh	SARAM 16
032000h - 033FFFh	000B 2000h – 000B 3FFFh	SARAM 17
034000h - 035FFFh	000B 4000h – 000B 5FFFh	SARAM 18
036000h - 037FFFh	000B 6000h – 000B 7FFFh	SARAM 19
038000h - 039FFFh	000B 8000h – 000B 9FFFh	SARAM 20
03A000h - 03BFFFh	000B A000h – 000B BFFFh	SARAM 21
03C000h - 03DFFFh	000B C000h – 000B DFFFh	SARAM 22
03E000h - 03FFFFh	000B E000h – 000B FFFFh	SARAM 23
040000h – 041FFFh	000C 0000h – 000C 1FFFh	SARAM 24
042000h – 043FFFh	000C 2000h – 000C 3FFFh	SARAM 25
044000h – 045FFFh	000C 4000h – 000C 5FFFh	SARAM 26
046000h – 047FFFh	000C 6000h – 000C 7FFFh	SARAM 27
048000h – 049FFFh	000C 8000h – 000C 9FFFh	SARAM 28
04A000h – 04BFFFh	000C A000h – 000C BFFFh	SARAM 29
04C000h – 04DFFFh	000C C000h – 000C DFFFh	SARAM 30
04E000h – 04FFFFh	000C E000h – 000C FFFFh	SARAM 31 (1)

(1) SARAM31 (byte address range: 0x4E000 – 0x4EFFF) is reserved for the bootloader. After the boot process is complete, this memory space can be used.

6.2.1.3 On-Chip Read-Only Memory (ROM)

The zero-wait-state ROM is located at the byte address range FE0000h – FFFFFFh. The ROM is composed of four 16K-word blocks, for a total of 128K bytes of ROM. Each on-chip ROM block can support one read per cycle. The ROM address space can be mapped by software to the EMIF external memory or to the internal ROM.

The standard device includes a Bootloader program resident in the ROM.

When the MPNMC bit field of the ST3 status register is cleared (by default), the byte address range FE0000h – FFFFFFh is used for the on-chip ROM. When the MPNMC bit field of the ST3 status register is set through software, the on-chip ROM is disabled and not present in the memory map, and byte address range FE0000h – FFFFFFh is directed to the EMIF's external memory space on $\overline{\text{EM\_CS5}}$. A hardware reset always clears the MPNMC bit, so it is not possible to disable the ROM at reset. However, the software reset instruction does not affect the MPNMC bit. The ROM can be accessed by the CPU program and data buses.

6.2.1.4 I/O Memory

The device includes a 64K byte I/O space for the memory-mapped registers of the DSP peripherals and system registers used for idle control, status monitoring and system configuration. I/O space is separate from program and memory space and is accessed with separate instruction opcodes or via the DMA's.

Table 6-3 lists the memory-mapped registers of the device. Note that not all addresses in the 64K byte I/O space are used; these addresses should be treated as RESERVED and not accessed by the CPU nor DMA. For the expanded tables of each peripheral, see Section 6.2.4, *Register Map*.

Some of the DMA controllers have access to the I/O-Space memory-mapped registers of the following peripherals registers: I2C, UART, I2S, MMC and SD, EMIF, McBSP, McSPI, USB, and SAR ADC.

Before accessing any peripheral memory-mapped register, make sure the peripheral being accessed is not held in reset via the Peripheral Reset Control Register (PRCR) and its internal clock is enabled via the Peripheral Clock Gating Control Registers (PCGCR1 and PCGCR2).

Table 6-3. Peripheral I/O-Space Control Registers

WORD ADDRESS	PERIPHERAL
0x0000 – 0x0004	Idle Control
0x0005 – 0x0BFF	Reserved
0x0C00 – 0x0C7F	DMA0
0x0C80 – 0x0CFF	Reserved
0x0D00 – 0x0D7F	DMA1
0x0D80 – 0x0DFF	Reserved
0x0E00 – 0x0E7F	DMA2
0x0E80 – 0x0EFF	Reserved
0x0F00 – 0x0F7F	DMA3
0x0F80 – 0x0FFF	Reserved
0x1000 – 0x10DD	EMIF
0x10DE – 0x17FF	Reserved
0x1800 – 0x181F	Timer0
0x1820 – 0x183F	Reserved
0x1840 – 0x185F	Timer1
0x1860 – 0x187F	Reserved
0x1880 – 0x189F	Timer2
0x18A0 – 0x18FF	Reserved
0x1900 – 0x197F	RTC

Table 6-3. Peripheral I/O-Space Control Registers (continued)

WORD ADDRESS	PERIPHERAL
0x1980 – 0x19FF	Reserved
0x1A00 – 0x1A6C	I2C
0x1A6D – 0x1AFF	Reserved
0x1B00 – 0x1B1F	UART
0x1B20 – 0x1BFF	Reserved
0x1C00 – 0x1CFF	System Control
0x1D00 – 0x1FFF through 0x2600 – 0x27FF	Reserved
0x2800 – 0x2840	I2S0
0x2841 – 0x29FF	Reserved
0x2A00 – 0x2A40	I2S2
0x2A41 – 0x2AFF	Reserved
0x2B00 – 0x2B40	I2S3
0x2B41 – 0x2DFF	Reserved
0x2E00 – 0x2E81	UHPI
0x2E82 – 0x2FFF	Reserved
0x3000 – 0x300F	SPI
0x3010 – 0x33FF	Reserved
0x3400 – 0x3749	McSPI
0x3750 –0x39FF	Reserved
0x3A00 – 0x3A7F	MMC0 and SD0
0x3A80 – 0x3AFF	Reserved
0x3B00 – 0x3B7F	MMC1 and SD1
0x3B80 – 0x3FFF	Reserved
0x4000 – 0x407F	McBSP
0x4080 – 0x5FFF	Reserved
0x6000 – 0x60FF	McBSP DMA
0x6100 – 0x6FFF	Reserved
0x7000 – 0x70FF	SAR and Analog Control Registers
0x7100 – 0x7FFF	Reserved
0x8000 – 0xFFFF	USB

6.2.2 External Memory

The external memory space of the device is located at the byte address range 050000h – FFFFFFh. The external memory space is divided into five chip select spaces: one dedicated to SDRAM and mobile SDRAM (EMIF CS0 or CS[1:0] space), and the remainder (EMIF CS2 through CS5 space) dedicated to asynchronous devices including flash. Each chip select space has a corresponding chip select pin (called $\overline{\text{EM\_CSx}}$) that is activated during an access to the chip select space.

The external memory interface (EMIF) provides the means for the DSP to access external memories and other devices including: mobile single data rate (SDR) synchronous dynamic RAM (SDRAM and mSDRAM), NOR Flash, NAND Flash, and asynchronous static RAM (SRAM). Before accessing external memory, you must configure the EMIF through its memory-mapped registers.

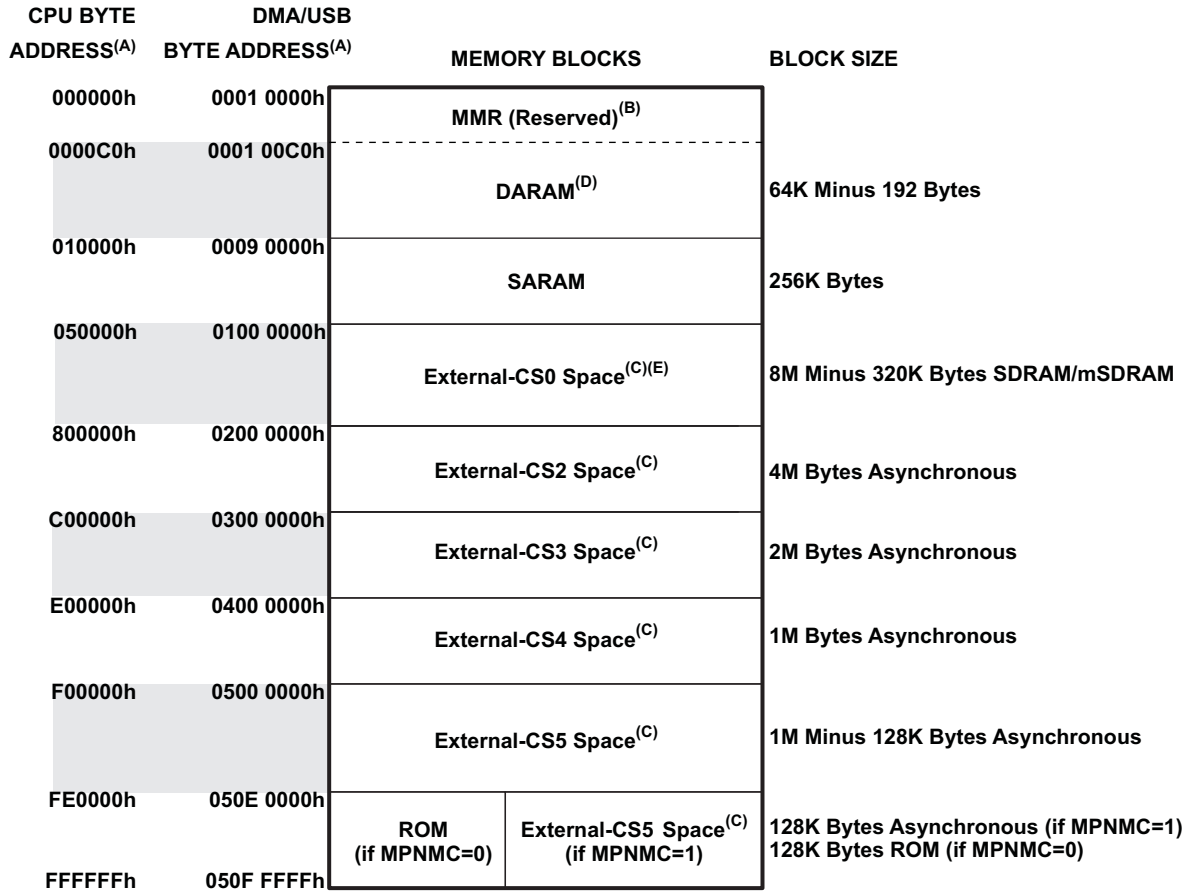
The EMIF provides a configurable 16- or 8-bit data bus, an address bus width of up to 21-bits, and 5 dedicated chip selects, along with memory control signals. To maximize power savings, the I/O pins of the EMIF can be operated at an independent voltage from the other I/O pins on the device.

6.2.3 Memory Map

The device provides 16M bytes of total memory space composed of on-chip RAM, on-chip ROM, and external memory space supporting a variety of memory types. The on-chip, dual-access RAM allows two accesses to a given block during the same cycle. There are 8 blocks of 8K bytes of dual-access RAM. The on-chip, single-access RAM allows one access to a given block per cycle. In addition, there are 32 blocks of 8K bytes of single-access RAM.

The remainder of the memory map is divided into five external spaces, and on-chip ROM. Each external space has a chip select decode signal (called $\overline{\text{EM\_CS0}}$, $\overline{\text{EM\_CS}}$[2:5]) that indicates an access to the selected space. The external memory interface (EMIF) supports access to asynchronous memories such as SRAM, NAND, or NOR and Flash, and mobile single data rate (mSDR) and single data rate (SDR) SDRAM.

The DSP memory is accessible by different master modules within the DSP, including the C55x CPU, the four DMA controllers, the UHPI, and the CDMA of USB (see Figure 6-1). However, only the UHPI and USB CDMA can access the SARAM.



A. Address shown represents the first byte address in each block.
B. The first 192 bytes are reserved for memory-mapped registers (MMRs).
C. Out of the four DMA controllers, *only* DMA controller 3 has access to the external memory space.
D. The USB controller and UHPI do not have access to DARAM.
E. The CS0 space can be accessed by CS0 *only* or by CS0 *and* CS1.

Figure 6-1. Memory Map

6.2.4 Register Map

6.2.4.1 DMA Peripheral Register Description

The following tables show the registers associated with the four direct memory access (DMA) controllers.

Table 6-4. System Registers Related to the DMA Controllers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
1C30h	DMAIFR	DMA Interrupt Flag Register
1C31h	DMAIER	DMA Interrupt Enable Register
1C1Ah	DMA0CESRL	DMA0 Channel Event Source Register Lower
1C1Bh	DMA0CESRU	DMA0 Channel Event Source Register Upper
1C1Ch	DMA1CESRL	DMA1 Channel Event Source Register Lower
1C1Dh	DMA1CESRU	DMA1 Channel Event Source Register Upper
1C36h	DMA2CESRL	DMA2 Channel Event Source Register Lower
1C37h	DMA2CESRU	DMA2 Channel Event Source Register Upper
1C38h	DMA3CESRL	DMA3 Channel Event Source Register Lower
1C39h	DMA3CESRU	DMA3 Channel Event Source Register Upper

Table 6-5. DMA Controller 0 (DMA0) Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
0C00h	DMACH0SSAL	Channel 0 Source Start Address Register Lower
0C01h	DMACH0SSAU	Channel 0 Source Start Address Register Upper
0C02h	DMACH0DSAL	Channel 0 Destination Start Address Register Lower
0C03h	DMACH0DSAU	Channel 0 Destination Start Address Register Upper
0C04h	DMACH0TCRL	Channel 0 Transfer Control Register Lower
0C05h	DMACH0TCRU	Channel 0 Transfer Control Register Upper
0C20h	DMACH1SSAL	Channel 1 Source Start Address Register Lower
0C21h	DMACH1SSAU	Channel 1 Source Start Address Register Upper
0C22h	DMACH1DSAL	Channel 1 Destination Start Address Register Lower
0C23h	DMACH1DSAU	Channel 1 Destination Start Address Register Upper
0C24h	DMACH1TCRL	Channel 1 Transfer Control Register Lower
0C25h	DMACH1TCRU	Channel 1 Transfer Control Register Upper
0C40h	DMACH2SSAL	Channel 2 Source Start Address Register Lower
0C41h	DMACH2SSAU	Channel 2 Source Start Address Register Upper
0C42h	DMACH2DSAL	Channel 2 Destination Start Address Register Lower
0C43h	DMACH2DSAU	Channel 2 Destination Start Address Register Upper
0C44h	DMACH2TCRL	Channel 2 Transfer Control Register Lower
0C45h	DMACH2TCRU	Channel 2 Transfer Control Register Upper
0C60h	DMACH3SSAL	Channel 3 Source Start Address Register Lower
0C61h	DMACH3SSAU	Channel 3 Source Start Address Register Upper
0C62h	DMACH3DSAL	Channel 3 Destination Start Address Register Lower
0C63h	DMACH3DSAU	Channel 3 Destination Start Address Register Upper
0C64h	DMACH3TCRL	Channel 3 Transfer Control Register Lower
0C65h	DMACH3TCRU	Channel 3 Transfer Control Register Upper

Table 6-6. DMA Controller 1 (DMA1) Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
0D00h	DMACH0SSAL	Channel 0 Source Start Address Register Lower
0D01h	DMACH0SSAU	Channel 0 Source Start Address Register Upper
0D02h	DMACH0DSAL	Channel 0 Destination Start Address Register Lower
0D03h	DMACH0DSAU	Channel 0 Destination Start Address Register Upper
0D04h	DMACH0TCRL	Channel 0 Transfer Control Register Lower
0D05h	DMACH0TCRU	Channel 0 Transfer Control Register Upper
0D20h	DMACH1SSAL	Channel 1 Source Start Address Register Lower
0D21h	DMACH1SSAU	Channel 1 Source Start Address Register Upper
0D22h	DMACH1DSAL	Channel 1 Destination Start Address Register Lower
0D23h	DMACH1DSAU	Channel 1 Destination Start Address Register Upper
0D24h	DMACH1TCRL	Channel 1 Transfer Control Register Lower
0D25h	DMACH1TCRU	Channel 1 Transfer Control Register Upper
0D40h	DMACH2SSAL	Channel 2 Source Start Address Register Lower
0D41h	DMACH2SSAU	Channel 2 Source Start Address Register Upper
0D42h	DMACH2DSAL	Channel 2 Destination Start Address Register Lower
0D43h	DMACH2DSAU	Channel 2 Destination Start Address Register Upper
0D44h	DMACH2TCRL	Channel 2 Transfer Control Register Lower
0D45h	DMACH2TCRU	Channel 2 Transfer Control Register Upper
0D60h	DMACH3SSAL	Channel 3 Source Start Address Register Lower
0D61h	DMACH3SSAU	Channel 3 Source Start Address Register Upper
0D62h	DMACH3DSAL	Channel 3 Destination Start Address Register Lower
0D63h	DMACH3DSAU	Channel 3 Destination Start Address Register Upper
0D64h	DMACH3TCRL	Channel 3 Transfer Control Register Lower
0D65h	DMACH3TCRU	Channel 3 Transfer Control Register Upper

Table 6-7. DMA Controller 2 (DMA2) Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
0E00h	DMACH0SSAL	Channel 0 Source Start Address Register Lower
0E01h	DMACH0SSAU	Channel 0 Source Start Address Register Upper
0E02h	DMACH0DSAL	Channel 0 Destination Start Address Register Lower
0E03h	DMACH0DSAU	Channel 0 Destination Start Address Register Upper
0E04h	DMACH0TCRL	Channel 0 Transfer Control Register Lower
0E05h	DMACH0TCRU	Channel 0 Transfer Control Register Upper
0E20h	DMACH1SSAL	Channel 1 Source Start Address Register Lower
0E21h	DMACH1SSAU	Channel 1 Source Start Address Register Upper
0E22h	DMACH1DSAL	Channel 1 Destination Start Address Register Lower
0E23h	DMACH1DSAU	Channel 1 Destination Start Address Register Upper
0E24h	DMACH1TCRL	Channel 1 Transfer Control Register Lower
0E25h	DMACH1TCRU	Channel 1 Transfer Control Register Upper
0E40h	DMACH2SSAL	Channel 2 Source Start Address Register Lower
0E41h	DMACH2SSAU	Channel 2 Source Start Address Register Upper
0E42h	DMACH2DSAL	Channel 2 Destination Start Address Register Lower
0E43h	DMACH2DSAU	Channel 2 Destination Start Address Register Upper
0E44h	DMACH2TCRL	Channel 2 Transfer Control Register Lower
0E45h	DMACH2TCRU	Channel 2 Transfer Control Register Upper

Table 6-7. DMA Controller 2 (DMA2) Registers (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
0E60h	DMACH3SSAL	Channel 3 Source Start Address Register Lower
0E61h	DMACH3SSAU	Channel 3 Source Start Address Register Upper
0E62h	DMACH3DSAL	Channel 3 Destination Start Address Register Lower
0E63h	DMACH3DSAU	Channel 3 Destination Start Address Register Upper
0E64h	DMACH3TCRL	Channel 3 Transfer Control Register Lower
0E65h	DMACH3TCRU	Channel 3 Transfer Control Register Upper

Table 6-8. DMA Controller 3 (DMA3) Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
0F00h	DMACH0SSAL	Channel 0 Source Start Address Register Lower
0F01h	DMACH0SSAU	Channel 0 Source Start Address Register Upper
0F02h	DMACH0DSAL	Channel 0 Destination Start Address Register Lower
0F03h	DMACH0DSAU	Channel 0 Destination Start Address Register Upper
0F04h	DMACH0TCRL	Channel 0 Transfer Control Register Lower
0F05h	DMACH0TCRU	Channel 0 Transfer Control Register Upper
0F20h	DMACH1SSAL	Channel 1 Source Start Address Register Lower
0F21h	DMACH1SSAU	Channel 1 Source Start Address Register Upper
0F22h	DMACH1DSAL	Channel 1 Destination Start Address Register Lower
0F23h	DMACH1DSAU	Channel 1 Destination Start Address Register Upper
0F24h	DMACH1TCRL	Channel 1 Transfer Control Register Lower
0F25h	DMACH1TCRU	Channel 1 Transfer Control Register Upper
0F40h	DMACH2SSAL	Channel 2 Source Start Address Register Lower
0F41h	DMACH2SSAU	Channel 2 Source Start Address Register Upper
0F42h	DMACH2DSAL	Channel 2 Destination Start Address Register Lower
0F43h	DMACH2DSAU	Channel 2 Destination Start Address Register Upper
0F44h	DMACH2TCRL	Channel 2 Transfer Control Register Lower
0F45h	DMACH2TCRU	Channel 2 Transfer Control Register Upper
0F60h	DMACH3SSAL	Channel 3 Source Start Address Register Lower
0F61h	DMACH3SSAU	Channel 3 Source Start Address Register Upper
0F62h	DMACH3DSAL	Channel 3 Destination Start Address Register Lower
0F63h	DMACH3DSAU	Channel 3 Destination Start Address Register Upper
0F64h	DMACH3TCRL	Channel 3 Transfer Control Register Lower
0F65h	DMACH3TCRU	Channel 3 Transfer Control Register Upper

6.2.4.2 EMIF Peripheral Register Description

Table 6-9 shows the EMIF registers.

Table 6-9. External Memory Interface (EMIF) Peripheral Registers(1)

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
1000h	REV	Revision Register
1001h	STATUS	Status Register
1004h	AWCCR1	Asynchronous Wait Cycle Configuration Register 1
1005h	AWCCR2	Asynchronous Wait Cycle Configuration Register 2
1008h	SDCR1	SDRAM and mSDRAM Configuration Register 1
1009h	SDCR2	SDRAM and mSDRAM Configuration Register 2
100Ch	SDRCR	SDRAM and mSDRAM Refresh Control Register
1010h	ACS2CR1	Asynchronous CS2 Configuration Register 1
1011h	ACS2CR2	Asynchronous CS2 Configuration Register 2
1014h	ACS3CR1	Asynchronous CS3 Configuration Register 1
1015h	ACS3CR2	Asynchronous CS3 Configuration Register 2
1018h	ACS4CR1	Asynchronous CS4 Configuration Register 1
1019h	ACS4CR2	Asynchronous CS4 Configuration Register 2
101Ch	ACS5CR1	Asynchronous CS5 Configuration Register 1
101Dh	ACS5CR2	Asynchronous CS5 Configuration Register 2
1020h	SDTIMR1	SDRAM and mSDRAM Timing Register 1
1021h	SDTIMR2	SDRAM and mSDRAM Timing Register 2
103Ch	SDSRETR	SDRAM and mSDRAM Self Refresh Exit Timing Register
1040h	EIRR	EMIF Interrupt Raw Register
1044h	EIMR	EMIF Interrupt Mask Register
1048h	EIMSR	EMIF Interrupt Mask Set Register
104Ch	EIMCR	EMIF Interrupt Mask Clear Register
1060h	NANDFCR	NAND Flash Control Register
1064h	NANDFSR1	NAND Flash Status Register 1
1065h	NANDFSR2	NAND Flash Status Register 2
1068h	PAGEMODCTRL1	Page Mode Control Register 1
1069h	PAGEMODCTRL2	Page Mode Control Register 2
1070h	NCS2ECC1	NAND Flash CS2 1-Bit ECC Register 1
1071h	NCS2ECC2	NAND Flash CS2 1-Bit ECC Register 2
1074h	NCS3ECC1	NAND Flash CS3 1-Bit ECC Register 1
1075h	NCS3ECC2	NAND Flash CS3 1-Bit ECC Register 2
1078h	NCS4ECC1	NAND Flash CS4 1-Bit ECC Register 1
1079h	NCS4ECC2	NAND Flash CS4 1-Bit ECC Register 2
107Ch	NCS5ECC1	NAND Flash CS5 1-Bit ECC Register 1
107Dh	NCS5ECC2	NAND Flash CS5 1-Bit ECC Register 2
10BCh	NAND4BITECCLOAD	NAND Flash 4-Bit ECC Load Register
10C0h	NAND4BITECC1	NAND Flash 4-Bit ECC Register 1
10C1h	NAND4BITECC2	NAND Flash 4-Bit ECC Register 2
10C4h	NAND4BITECC3	NAND Flash 4-Bit ECC Register 3
10C5h	NAND4BITECC4	NAND Flash 4-Bit ECC Register 4
10C8h	NAND4BITECC5	NAND Flash 4-Bit ECC Register 5
10C9h	NAND4BITECC6	NAND Flash 4-Bit ECC Register 6

(1) Before reading or writing to the EMIF registers, be sure to set the BYTEMODE bits to 00b in the EMIF system control register to enable word accesses to the EMIF registers.

Table 6-9. External Memory Interface (EMIF) Peripheral Registers[(1)] (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
10CCh	NAND4BITECC7	NAND Flash 4-Bit ECC Register 7
10CDh	NAND4BITECC8	NAND Flash 4-Bit ECC Register 8
10D0h	NANDERRADD1	NAND Flash 4-Bit ECC Error Address Register 1
10D1h	NANDERRADD2	NAND Flash 4-Bit ECC Error Address Register 2
10D4h	NANDERRADD3	NAND Flash 4-Bit ECC Error Address Register 3
10D5h	NANDERRADD4	NAND Flash 4-Bit ECC Error Address Register 4
10D8h	NANDERRVAL1	NAND Flash 4-Bit ECC Error Value Register 1
10D9h	NANDERRVAL2	NAND Flash 4-Bit ECC Error Value Register 2
10DCh	NANDERRVAL3	NAND Flash 4-Bit ECC Error Value Register 3
10DDh	NANDERRVAL4	NAND Flash 4-Bit ECC Error Value Register 4

6.2.4.3 GPIO Peripheral Register Description

The external parallel port interface includes a 16-bit general purpose I/O that can be individually programmed as input or output with interrupt capability. Control of the general purpose I/O is maintained through a set of I/O memory-mapped registers shown in Table 6-10.

Table 6-10. GPIO Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
1C06h	IODIR1	GPIO Direction Register 1
1C07h	IODIR2	GPIO Direction Register 2
1C08h	IOINDATA1	GPIO Data In Register 1
1C09h	IOINDATA2	GPIO Data In Register 2
1C0Ah	IODATAOUT1	GPIO Data Out Register 1
1C0Bh	IODATAOUT2	GPIO Data Out Register 2
1C0Ch	IOINTEDG1	GPIO Interrupt Edge Trigger Enable Register 1
1C0Dh	IOINTEDG2	GPIO Interrupt Edge Trigger Enable Register 2
1C0Eh	IOINTEN1	GPIO Interrupt Enable Register 1
1C0Fh	IOINTEN2	GPIO Interrupt Enable Register 2
1C10h	IOINTFLG1	GPIO Interrupt Flag Register 1
1C11h	IOINTFLG2	GPIO Interrupt Flag Register 2

6.2.4.4 I2C Peripheral Register Description

Table 6-11 shows the Inter-Integrated Circuit (I2C) registers.

Table 6-11. Inter-Integrated Circuit (I2C) Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
1A00h	ICOAR	I2C Own Address Register
1A04h	ICIMR	I2C Interrupt Mask Register
1A08h	ICSTR	I2C Interrupt Status Register
1A0Ch	ICCLKL	I2C Clock Low-Time Divider Register
1A10h	ICCLKH	I2C Clock High-Time Divider Register
1A14h	ICCNT	I2C Data Count Register
1A18h	ICDRR	I2C Data Receive Register
1A1Ch	ICSAR	I2C Slave Address Register
1A20h	ICDXR	I2C Data Transmit Register
1A24h	ICMDR	I2C Mode Register
1A28h	ICIVR	I2C Interrupt Vector Register
1A2Ch	ICEMDR	I2C Extended Mode Register
1A30h	ICPSC	I2C Prescaler Register
1A34h	ICPID1	I2C Peripheral Identification Register 1
1A38h	ICPID2	I2C Peripheral Identification Register 2

6.2.4.5 I2S Peripheral Register Description

Table 6-12 through Table 6-14 show the I2S0, I2S2, and I2S3 registers.

Table 6-12. I2S0 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
2800h	I2S0SCTRL	I2S0 Serializer Control Register
2804h	I2S0SRATE	I2S0 Sample Rate Generator Register
2808h	I2S0TXLT1	I2S0 Transmit Left Data Register 1
2809h	I2S0TXLT2	I2S0 Transmit Left Data Register 2
280Ch	I2S0TXRT1	I2S0 Transmit Right Data Register 1
280Dh	I2S0TXRT2	I2S0 Transmit Right Data Register 2
2810h	I2S0INTFL	I2S0 Interrupt Flag Register
2814h	I2S0INTMASK	I2S0 Interrupt Mask Register
2828h	I2S0RXLT1	I2S0 Receive Left Data Register 1
2829h	I2S0RXLT2	I2S0 Receive Left Data Register 2
282Ch	I2S0RXRT1	I2S0 Receive Right Data Register 1
282Dh	I2S0RXRT2	I2S0 Receive Right Data Register 2

Table 6-13. I2S2 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
2A00h	I2S2SCTRL	I2S2 Serializer Control Register
2A04h	I2S2SRATE	I2S2 Sample Rate Generator Register
2A08h	I2S2TXLT1	I2S2 Transmit Left Data Register 1
2A09h	I2S2TXLT2	I2S2 Transmit Left Data Register 2
2A0Ch	I2S2TXRT1	I2S2 Transmit Right Data Register 1
2A0Dh	I2S2TXRT2	I2S2 Transmit Right Data Register 2
2A10h	I2S2INTFL	I2S2 Interrupt Flag Register
2A14h	I2S2INTMASK	I2S2 Interrupt Mask Register
2A28h	I2S2RXLT1	I2S2 Receive Left Data Register 1
2A29h	I2S2RXLT2	I2S2 Receive Left Data Register 2
2A2Ch	I2S2RXRT1	I2S2 Receive Right Data Register 1
2A2Dh	I2S2RXRT2	I2S2 Receive Right Data Register 2

Table 6-14. I2S3 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
2B00h	I2S3SCTRL	I2S3 Serializer Control Register
2B04h	I2S3SRATE	I2S3 Sample Rate Generator Register
2B08h	I2S3TXLT1	I2S3 Transmit Left Data Register 1
2B09h	I2S3TXLT2	I2S3 Transmit Left Data Register 2
2B0Ch	I2S3TXRT1	I2S3 Transmit Right Data Register 1
2B0Dh	I2S3TXRT2	I2S3 Transmit Right Data Register 2
2B10h	I2S3INTFL	I2S3 Interrupt Flag Register
2B14h	I2S3INTMASK	I2S3 Interrupt Mask Register
2B28h	I2S3RXLT1	I2S3 Receive Left Data Register 1
2B29h	I2S3RXLT2	I2S3 Receive Left Data Register 2
2B2Ch	I2S3RXRT1	I2S3 Receive Right Data Register 1

Table 6-14. I2S3 Registers (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
2B2Dh	I2S3RXRT2	I2S3 Receive Right Data Register 2

6.2.4.6 McBSP Peripheral Register Descriptions

Table 6-15 shows the McBSP peripheral registers.

Table 6-15. McBSP Module Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
4000h	DRRL	Data Receive Register Lower
4001h	DRRU	Data Receive Register Upper
4004h	DXRL	Data Transmit Register Lower
4005h	DXRU	Data Transmit Register Upper
4008h	SPCRL	Serial Port Control Register Lower
4009h	SPCRU	Serial Port Control Register Upper
400Ch	RCRL	Receive Control Register Lower
400Dh	RCRU	Receive Control Register Upper
4010h	XCRL	Transmit Control Register Lower
4011h	XCRU	Transmit Control Register Upper
4014h	SRGRL	Sample Rate Generator Register Lower
4015h	SRGRU	Sample Rate Generator Register Upper
4018h	MCRL	Multichannel Control Register Lower
4019h	MCRU	Multichannel Control Register Upper
401Ch	RCERA	Enhanced Receive Channel Enable Register Partition A
401Dh	RCERB	Enhanced Receive Channel Enable Register Partition B
4020h	XCERA	Enhanced Transmit Channel Enable Register Partition A
4021h	XCERB	Enhanced Transmit Channel Enable Register Partition B
4024h	PCRL	Pin Control Register Lower
4025h	PCRU	Pin Control Register Upper
4028h	RCERC	Enhanced Receive Channel Enable Register Partition C
4029h	RCERD	Enhanced Receive Channel Enable Register Partition D
402Ch	XCERC	Enhanced Transmit Channel Enable Register Partition C
402Dh	XCERD	Enhanced Transmit Channel Enable Register Partition D
4030h	RCERE	Enhanced Receive Channel Enable Register Partition E
4031h	RCERF	Enhanced Receive Channel Enable Register Partition F
4034h	XCERE	Enhanced Transmit Channel Enable Register Partition E
4035h	XCERF	Enhanced Transmit Channel Enable Register Partition F
4038h	RCERG	Enhanced Receive Channel Enable Register Partition G
4039h	RCERH	Enhanced Receive Channel Enable Register Partition H
403Ch	XCERG	Enhanced Transmit Channel Enable Register Partition G
403Dh	XCERH	Enhanced Transmit Channel Enable Register Partition H

6.2.4.7 McSPI Peripheral Register Descriptions

Table 6-16 shows the McSPI peripheral registers.

Table 6-16. McSPI Module Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
3500h	REVISIONL	Revision Register Lower
3510h	SYSCONFIGL	System Configuration Register Lower
3514h	SYSSTATUSL	System Status Register Lower
3518h	IRQSTATUSL	Interrupt Status Register Lower
3519h	IRQSTATUSU	Interrupt Status Register Upper
351Ch	IRQENABLEL	Interrupt Enable Register Lower
351Dh	IRQENABLEU	Interrupt Enable Register Upper
3520h	WAKEUPENABLEL	Wakeup Enable Register Lower
3528h	MODULCTRLL	Module Control Register Lower
352Ch	CH0CONFL	Channel 0 Configuration Register Lower
352Dh	CH0CONFU	Channel 0 Configuration Register Upper
3530h	CH0STATL	Channel 0 Status Register Lower
3534h	CH0CTRLL	Channel 0 Control Register Lower
3538h	CH0TXL	Channel 0 Transmitter Register Lower
3539h	CH0TXU	Channel 0 Transmitter Register Upper
353Ch	CH0RXL	Channel 0 Receiver Register Lower
353Dh	CH0RXU	Channel 0 Receiver Register Upper
3540h	CH1CONFL	Channel 1 Configuration Register Lower
3541h	CH1CONFU	Channel 1 Configuration Register Upper
3544h	CH1STATL	Channel 1 Status Register Lower
3548h	CH1CTRLL	Channel 1 Control Register Lower
354Ch	CH1TXL	Channel 1 Transmitter Register Lower
354Dh	CH1TXU	Channel 1 Transmitter Register Upper
3550h	CH1RXL	Channel 1 Receiver Register Lower
3551h	CH1RXU	Channel 1 Receiver Register Upper
3554h	CH2CONFL	Channel 2 Configuration Register Lower
3555h	CH2CONFU	Channel 2 Configuration Register Upper
3558h	CH2STATL	Channel 2 Status Register Lower
355Ch	CH2CTRLL	Channel 2 Control Register Lower
3560h	CH2TXL	Channel 2 Transmitter Register Lower
3561h	CH2TXU	Channel 2 Transmitter Register Upper
3564h	CH2RXL	Channel 2 Receiver Register Lower
3565h	CH2RXU	Channel 2 Receiver Register Upper
357Ch	XFERLEVELL	Transfer Levels Register Lower
357Dh	XFERLEVELU	Transfer Levels Register Upper
3580h	DAFTXL	DMA Address Aligned FIFO Transmitter Register Lower
3581h	DAFTXU	DMA Address Aligned FIFO Transmitter Register Upper
35A0h	DAFRXL	DMA Address Aligned FIFO Receiver Register Lower
35A1h	DAFRXU	DMA Address Aligned FIFO Receiver Register Upper

6.2.4.8 MMC and SD Peripheral Register Description

Table 6-17 and Table 6-18 show the MMC and SD registers. The MMC0 and SD0 registers start at address 0x3A00 and the MMC1 and SD1 registers start at address 0x3B00.

Table 6-17. MMC0 and SD0 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
3A00h	MMCCTL	MMC Control Register
3A04h	MMCCLK	MMC Memory Clock Control Register
3A08h	MMCST0	MMC Status Register 0
3A0Ch	MMCST1	MMC Status Register 1
3A10h	MMCIM	MMC Interrupt Mask Register
3A14h	MMCTOR	MMC Response Time-Out Register
3A18h	MMCTOD	MMC Data Read Time-Out Register
3A1Ch	MMCBLEN	MMC Block Length Register
3A20h	MMCNBLK	MMC Number of Blocks Register
3A24h	MMCNBLC	MMC Number of Blocks Counter Register
3A28h	MMCDRRL	MMC Data Receive Register Lower
3A29h	MMCDRRU	MMC Data Receive Register Upper
3A2Ch	MMCDXRL	MMC Data Transmit Register Lower
3A2Dh	MMCDXRU	MMC Data Transmit Register Upper
3A30h	MMCCMDL	MMC Command Register Lower
3A31h	MMCCMDU	MMC Command Register Upper
3A34h	MMCARGL	MMC Argument Register Lower
3A35h	MMCARGU	MMC Argument Register Upper
3A38h	MMCRSP0	MMC Response Register 0
3A39h	MMCRSP1	MMC Response Register 1
3A3Ch	MMCRSP2	MMC Response Register 2
3A3Dh	MMCRSP3	MMC Response Register 3
3A40h	MMCRSP4	MMC Response Register 4
3A41h	MMCRSP5	MMC Response Register 5
3A44h	MMCRSP6	MMC Response Register 6
3A45h	MMCRSP7	MMC Response Register 7
3A48h	MMCDRSP	MMC Data Response Register
3A50h	MMCCIDX	MMC Command Index Register
3A64h	SDIOCTL	SDIO Control Register
3A68h	SDIOST0	SDIO Status Register 0
3A6Ch	SDIOIEN	SDIO Interrupt Enable Register
3A70h	SDIOIST	SDIO Interrupt Status Register
3A74h	MMCFIFOCTL	MMC FIFO Control Register

Table 6-18. MMC1 and SD1 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
3B00h	MMCCTL	MMC Control Register
3B04h	MMCCLK	MMC Memory Clock Control Register
3B08h	MMCST0	MMC Status Register 0
3B0Ch	MMCST1	MMC Status Register 1
3B10h	MMCIM	MMC Interrupt Mask Register
3B14h	MMCTOR	MMC Response Time-Out Register
3B18h	MMCTOD	MMC Data Read Time-Out Register
3B1Ch	MMCBLEN	MMC Block Length Register
3B20h	MMCNBLK	MMC Number of Blocks Register
3B24h	MMCNBLC	MMC Number of Blocks Counter Register
3B28h	MMCDRRL	MMC Data Receive Register Lower
3B29h	MMCDRRU	MMC Data Receive Register Upper
3B2Ch	MMCDXRL	MMC Data Transmit Register Lower
3B2Dh	MMCDXRU	MMC Data Transmit Register Upper
3B30h	MMCCMDL	MMC Command Register Lower
3B31h	MMCCMDU	MMC Command Register Upper
3B34h	MMCARGL	MMC Argument Register Lower
3B35h	MMCARGU	MMC Argument Register Upper
3B38h	MMCRSP0	MMC Response Register 0
3B39h	MMCRSP1	MMC Response Register 1
3B3Ch	MMCRSP2	MMC Response Register 2
3B3Dh	MMCRSP3	MMC Response Register 3
3B40h	MMCRSP4	MMC Response Register 4
3B41h	MMCRSP5	MMC Response Register 5
3B44h	MMCRSP6	MMC Response Register 6
3B45h	MMCRSP7	MMC Response Register 7
3B48h	MMCDRSP	MMC Data Response Register
3B50h	MMCCIDX	MMC Command Index Register
3B64h	SDIOCTL	SDIO Control Register
3B68h	SDIOST0	SDIO Status Register 0
3B6Ch	SDIOIEN	SDIO Interrupt Enable Register
3B70h	SDIOIST	SDIO Interrupt Status Register
3B74h	MMCFIFOCTL	MMC FIFO Control Register

6.2.4.9 RTC Peripheral Register Description

Table 6-19 shows the RTC registers.

Table 6-19. Real-Time Clock (RTC) Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
1900h	RTCINTEN	RTC Interrupt Enable Register
1901h	RTCUPDATE	RTC Update Register
1904h	RTCMIL	Milliseconds Register
1905h	RTCMILA	Milliseconds Alarm Register
1908h	RTCSEC	Seconds Register
1909h	RTCSECA	Seconds Alarm Register
190Ch	RTCMIN	Minutes Register
190Dh	RTCMINA	Minutes Alarm Register
1910h	RTCHOUR	Hours Register
1911h	RTCHOURA	Hours Alarm Register
1914h	RTCDAY	Days Register
1915h	RTCDAYA	Days Alarm Register
1918h	RTCMONTH	Months Register
1919h	RTCMONTHA	Months Alarm Register
191Ch	RTCYEAR	Years Register
191Dh	RTCYEARA	Years Alarm Register
1920h	RTCINTFL	RTC Interrupt Flag Register
1921h	RTCNOPWR	RTC Lost Power Status Register
1924h	RTCINTREG	RTC Interrupt Register
1928h	RTCDRIFT	RTC Compensation Register
192Ch	RTCOSC	RTC Oscillator Register
1930h	RTCPMGT	RTC Power Management Register
1960h	RTCSCR1	RTC LSW Scratch Register 1
1961h	RTCSCR2	RTC MSW Scratch Register 2
1964h	RTCSCR3	RTC LSW Scratch Register 3
1965h	RTCSCR4	RTC MSW Scratch Register 4
196Ch	RGKR_LSW	RTC LSW Gate-Keeper Register
196Dh	RGKR_MSW	RTC MSW Gate-Keeper Register

6.2.4.10 SAR ADC Peripheral Register Description

Table 6-20 shows the SAR ADC peripheral registers.

Table 6-20. SAR Analog Control Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
7012h	SARCTRL	SAR A/D Control Register
7014h	SARDATA	SAR A/D Data Register
7016h	SARCLKCTRL	SAR A/D Clock Control Register
7018h	SARPINCTRL	SAR A/D Reference and Pin Control Register
701Ah	SARGPOCTRL	SAR A/D GPO Control Register

6.2.4.11 SPI Peripheral Register Descriptions

Table 6-21 shows the SPI registers.

Table 6-21. SPI Module Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
3000h	SPICDR	Clock Divider Register
3001h	SPICCR	Clock Control Register
3002h	SPIDCR1	Device Configuration Register 1
3003h	SPIDCR2	Device Configuration Register 2
3004h	SPICMD1	Command Register 1
3005h	SPICMD2	Command Register 2
3006h	SPISTAT1	Status Register 1
3007h	SPISTAT2	Status Register 2
3008h	SPIDAT1	Data Register 1
3009h	SPIDAT2	Data Register 2

6.2.4.12 System Registers

The system registers are used to configure the device and monitor its status. Brief descriptions of the various system registers are shown in Table 6-22.

Table 6-22. Idle Control, Status, and System Registers

CPU WORD ADDRESS	ACRONYM	Register Description	COMMENTS
0001h	ICR	Idle Control Register	
0002h	ISTR	Idle Status Register	
1C00h	EBSR	External Bus Selection Register	see Section 5.7.3.5.1 of this document.
1C02h	PCGCR1	Peripheral Clock Gating Control Register 1	
1C03h	PCGCR2	Peripheral Clock Gating Control Register 2	
1C04h	PSRCR	Peripheral Software Reset Counter Register	
1C05h	PRCR	Peripheral Reset Control Register	
1C14h	TIAFR	Timer Interrupt Aggregation Flag Register	
1C15h	MSIAFR	McSPI Interrupt Aggregation Flag Register	
1C16h	OSRCR	Output Slew Rate Control Register	
1C17h	PUDINHIBR1	Pullup and Pulldown Inhibit Register 1	
1C18h	PUDINHIBR2	Pullup and Pulldown Inhibit Register 2	
1C19h	PUDINHIBR3	Pullup and Pulldown Inhibit Register 3	
1C1Ah	DMA0CESR1	DMA0 Channel Event Source Register 1	
1C1Bh	DMA0CESR2	DMA0 Channel Event Source Register 2	
1C1Ch	DMA1CESR1	DMA1 Channel Event Source Register 1	
1C1Dh	DMA1CESR2	DMA1 Channel Event Source Register 2	
1C1Eh	CCR1	Clock Configuration Register 1	
1C1Fh	CCR2	Clock Configuration Register 2	
1C20h	PMR	PLL Multiplier Register	
1C21h	PICR	PLL Input Control Register	
1C22h	PCR	PLL Control Register	
1C23h	PODCR	PLL Output Divider Control Register	
1C24h	CLKOUTCR	CLKOUT Configuration Register	
1C26h	ECDR	EMIF Clock Divider Register	
1C27h	RSCR	RTC System Control Register	
1C28h	RAMSLPMDCNTLR1	RAM Sleep Mode Control Register 1	
1C2Ah	RAMSLPMDCNTLR2	RAM Sleep Mode Control Register 2	
1C2Bh	RAMSLPMDCNTLR3	RAM Sleep Mode Control Register 3	
1C2Ch	RAMSLPMDCNTLR4	RAM Sleep Mode Control Register 4	
1C2Dh	RAMSLPMDCNTLR5	RAM Sleep Mode Control Register 5	
1C2Eh	PLLSSCR1	PLL Spread Spectrum Control Register 1	
1C2Fh	PLLSSCR2	PLL Spread Spectrum Control Register 2	
1C30h	DMAIFR	DMA Interrupt Flag Aggregation Register	
1C31h	DMAIER	DMA Interrupt Enable Register	
1C32h	USBSCR	USB System Control Register	
1C33h	ESCR	EMIF System Control Register	
1C34h	BMR	BootMode Register	
1C36h	DMA2CESR1	DMA2 Channel Event Source Register 1	
1C37h	DMA2CESR2	DMA2 Channel Event Source Register 2	
1C38h	DMA3CESR1	DMA3 Channel Event Source Register 1	
1C39h	DMA3CESR2	DMA3 Channel Event Source Register 2	

Table 6-22. Idle Control, Status, and System Registers (continued)

CPU WORD ADDRESS	ACRONYM	Register Description	COMMENTS
1C3Ah	CLKSTOP1	Peripheral Clock Stop Request and Acknowledge Register 1	
1C3Bh	CLKSTOP2	Peripheral Clock Stop Request and Acknowledge Register 2	
1C3Ch	MSPIFCDR	McSPI Reference Clock Divider Register	
1C3Dh	MSIAER	McSPI Aggregation Interrupt Mask Register	
1C3Eh	TISR	Timer Interrupt Selection Register	
1C40h	DIEIDR0	Die ID Register 0	
1C41h	DIEIDR1	Die ID Register 1	
1C42h	DIEIDR2	Die ID Register 2	
1C43h	DIEIDR3	Die ID Register 3	
1C44h	DIEIDR4	Die ID Register 4	
1C45h	DIEIDR5	Die ID Register 5	
1C46h	DIEIDR6	Die ID Register 6	
1C47h	DIEIDR7	Die ID Register 7	
1C4Ch	PUDINHIBR4	Pullup and Pulldown Inhibit Register 4	
1C4Dh	PUDINHIBR5	Pullup and Pulldown Inhibit Register 5	
1C4Eh	UHPICR	UHPI Configuration Register	
1C4Fh	PUDINHIBR6	Pullup and Pulldown Inhibit Register 6	
1C50h	PUDINHIBR7	Pullup and Pulldown Inhibit Register 7	
1C58h	JTAGIDLSW	JTAG ID Code LSW Register	
1C59h	JTAGIDMSW	JTAG ID Code MSW Register	
7004h	LDOCNTL	LDO Control Register	see Section 5.7.2.1.1.2.1 of this document.

6.2.4.13 Timers Peripheral Register Description

Table 6-23 through Table 6-26 show the Timer and Watchdog registers.

Table 6-23. Watchdog Timer Registers (Timer2 *only*)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1880h	WDKCKLK	Watchdog Kick Lock Register
1882h	WDKICK	Watchdog Kick Register
1884h	WDSVLR	Watchdog Start Value Lock Register
1886h	WDSVR	Watchdog Start Value Register
1888h	WDENLOK	Watchdog Enable Lock Register
188Ah	WDEN	Watchdog Enable Register
188Ch	WDPSLR	Watchdog Prescaler Lock Register
188Eh	WDPS	Watchdog Prescaler Register

Table 6-24. General-Purpose Timer 0 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1810h	T0CR	Timer 0 Control Register
1812h	TIM0PRD1	Timer 0 Period Register 1
1813h	TIM0PRD2	Timer 0 Period Register 2
1814h	TIM0CNT1	Timer 0 Counter Register 1
1815h	TIM0CNT2	Timer 0 Counter Register 2
1816h	T0INSR	Timer 0 Input Selection Register

Table 6-25. General-Purpose Timer 1 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1850h	T1CR	Timer 1 Control Register
1852h	TIM1PRD1	Timer 1 Period Register 1
1853h	TIM1PRD2	Timer 1 Period Register 2
1854h	TIM1CNT1	Timer 1 Counter Register 1
1855h	TIM1CNT2	Timer 1 Counter Register 2
1856h	T1INSR	Timer 1 Input Selection Register

Table 6-26. General-Purpose Timer 2 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1890h	T2CR	Timer 2 Control Register
1892h	TIM2PRD1	Timer 2 Period Register 1
1893h	TIM2PRD2	Timer 2 Period Register 2
1894h	TIM2CNT1	Timer 2 Counter Register 1
1895h	TIM2CNT2	Timer 2 Counter Register 2
1896h	T2INSR	Timer 2 Input Selection Register

Table 6-27. Timer Interrupt Selection Register

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1C3Eh	TISR	Timer Interrupt Selection Register

6.2.4.14 UART Peripheral Register Description

Table 6-28 shows the UART registers.

Table 6-28. UART Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
1B00h	RBR	Receiver Buffer Register (read only)
1B00h	THR	Transmitter Holding Register (write only)
1B02h	IER	Interrupt Enable Register
1B04h	IIR	Interrupt Identification Register (read only)
1B04h	FCR	FIFO Control Register (write only)
1B06h	LCR	Line Control Register
1B08h	MCR	Modem Control Register
1B0Ah	LSR	Line Status Register
1B0Eh	SCR	Scratch Register
1B10h	DLL	Divisor LSB Latch
1B12h	DLH	Divisor MSB Latch
1B18h	PWREMU_MGMT	Power and Emulation Management Register

6.2.4.15 UHPI Peripheral Register Descriptions

Table 6-29 shows the UHPI peripheral registers.

Table 6-29. UHPI Module Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
2E00h	PIDL	Peripheral Identification Register Lower
2E01h	PIDU	Peripheral Identification Register Upper
2E04h	PWREMU_MGMT	Power Management and Emulation Register
2E08h	GPINT_CTRLL	GPINT Control Register Lower
2E09h	GPINT_CTRLU	GPINT Control Register Upper
2E0Ch	GPIO_ENL	GPIO Enable Register Lower
2E0Dh	GPIO_ENU	GPIO Enable Register Upper
2E10h	GPIO_DIR1L	GPIO Direction Register 1 Lower
2E11h	GPIO_DIR1U	GPIO Direction Register 1 Upper
2E14h	GPIO_DAT1L	GPIO Data Register 1 Lower
2E15h	GPIO_DAT1U	GPIO Data Register 1 Upper
2E18h	GPIO_DIR2L	GPIO Direction Register 2 Lower
2E19h	GPIO_DIR2U	GPIO Direction Register 2 Upper
2E1Ch	GPIO_DAT2L	GPIO Data Register 2 Lower
2E1Dh	GPIO_DAT2U	GPIO Data Register 2 Upper
2E20h	GPIO_DIR3L	GPIO Direction Register 3 Lower
2E21h	GPIO_DIR3U	GPIO Direction Register 3 Upper
2E24h	GPIO_DAT3L	GPIO Data Register 3 Lower
2E25h	GPIO_DAT3U	GPIO Data Register 3 Upper
2E30h	UHPICL	Universal Host-Port Interface Control Register
2E34h	UHPIAWL	Universal Host-Port Interface Write Address Register Lower
2E35h	UHPIAWU	Universal Host-Port Interface Write Address Register Upper
2E38h	UHPIARL	Universal Host-Port Interface Read Address Register Lower
2E39h	UHPIARU	Universal Host-Port Interface Read Address Register Upper

6.2.4.16 USB2.0 Peripheral Register Descriptions

Table 6-30 lists of the USB2.0 peripheral registers.

Table 6-30. Universal Serial Bus (USB) Registers(1)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
8000h	REVID1	Revision Identification Register 1
8001h	REVID2	Revision Identification Register 2
8004h	CTRLR	Control Register
800Ch	EMUR	Emulation Register
8010h	MODE1	Mode Register 1
8011h	MODE2	Mode Register 2
8014h	AUTOREQ	Auto Request Register
801Ch	TEARDOWN1	Teardown Register 1
801Dh	TEARDOWN2	Teardown Register 2
8020h	INTSRCR1	USB Interrupt Source Register 1
8021h	INTSRCR2	USB Interrupt Source Register 2
8024h	INTSETR1	USB Interrupt Source Set Register 1
8025h	INTSETR2	USB Interrupt Source Set Register 2
8028h	INTCLRR1	USB Interrupt Source Clear Register 1
8029h	INTCLRR2	USB Interrupt Source Clear Register 2
802Ch	INTMSKR1	USB Interrupt Mask Register 1
802Dh	INTMSKR2	USB Interrupt Mask Register 2
8030h	INTMSKSETR1	USB Interrupt Mask Set Register 1
8031h	INTMSKSETR2	USB Interrupt Mask Set Register 2
8034h	INTMSKCLRR1	USB Interrupt Mask Clear Register 1
8035h	INTMSKCLRR2	USB Interrupt Mask Clear Register 2
8038h	INTMASKEDR1	USB Interrupt Source Masked Register 1
8039h	INTMASKEDR2	USB Interrupt Source Masked Register 2
803Ch	EOIR	USB End of Interrupt Register
8040h	INTVECTR1	USB Interrupt Vector Register 1
8041h	INTVECTR2	USB Interrupt Vector Register 2
8050h	GREP1SZR1	Generic RNDIS EP1Size Register 1
8051h	GREP1SZR2	Generic RNDIS EP1Size Register 2
8054h	GREP2SZR1	Generic RNDIS EP2 Size Register 1
8055h	GREP2SZR2	Generic RNDIS EP2 Size Register 2
8058h	GREP3SZR1	Generic RNDIS EP3 Size Register 1
8059h	GREP3SZR2	Generic RNDIS EP3 Size Register 2
805Ch	GREP4SZR1	Generic RNDIS EP4 Size Register 1
805Dh	GREP4SZR2	Generic RNDIS EP4 Size Register 2

(1) Before reading or writing to the USB registers, be sure to set the BYTEMODE bits to "00b" in the USB system control register to enable word accesses to the USB registers .

Table 6-30. Universal Serial Bus (USB) Registers[(1)] (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
		Common USB Registers
8401h	FADDR_POWER	Function Address Register, Power Management Register
8402h	INTRTX	Interrupt Register for Endpoint 0 plus Transmit Endpoints 1 to 4
8405h	INTRRX	Interrupt Register for Receive Endpoints 1 to 4
8406h	INTRTXE	Interrupt enable register for INTRTX
8409h	INTRRXE	Interrupt Enable Register for INTRRX
840Ah	INTRUSB_INTRUSBE	Interrupt Register for Common USB Interrupts, Interrupt Enable Register
840Dh	FRAME	Frame Number Register
840Eh	INDEX_TESTMODE	Index Register for Selecting the Endpoint Status and Control Registers, Register to Enable the USB 2.0 Test Modes
		USB Indexed Registers
8411h	TXMAXP_INDX	Maximum Packet Size for Peripheral and Host Transmit Endpoint. (Index register set to select Endpoints 1-4)
8412h	PERI_CSR0_INDX	Control Status Register for Endpoint 0 in Peripheral Mode. (Index register set to select Endpoint 0)
	PERI_TXCSR_INDX	Control Status Register for Peripheral Transmit Endpoint. (Index register set to select Endpoints 1-4)
8415h	RXMAXP_INDX	Maximum Packet Size for Peripheral and Host Receive Endpoint. (Index register set to select Endpoints 1-4)
8416h	PERI_RXCSR_INDX	Control Status Register for Peripheral Receive Endpoint. (Index register set to select Endpoints 1-4)
8419h	COUNT0_INDX	Number of Received Bytes in Endpoint 0 FIFO. (Index register set to select Endpoint 0)
	RXCOUNT_INDX	Number of Bytes in Host Receive Endpoint FIFO. (Index register set to select Endpoints 1- 4)
841Ah	-	Reserved
841Dh	-	Reserved
841Eh	CONFIGDATA_INDC (Upper byte of 841Eh)	Returns details of core configuration. (index register set to select Endpoint 0)
		USB FIFO Registers
8421h	FIFO0R1	Transmit and Receive FIFO Register 1 for Endpoint 0
8422h	FIFO0R2	Transmit and Receive FIFO Register 2 for Endpoint 0
8425h	FIFO1R1	Transmit and Receive FIFO Register 1 for Endpoint 1
8426h	FIFO1R2	Transmit and Receive FIFO Register 2 for Endpoint 1
8429h	FIFO2R1	Transmit and Receive FIFO Register 1 for Endpoint 2
842Ah	FIFO2R2	Transmit and Receive FIFO Register 2 for Endpoint 2
842Dh	FIFO3R1	Transmit and Receive FIFO Register 1 for Endpoint 3
842Eh	FIFO3R2	Transmit and Receive FIFO Register 2 for Endpoint 3
8431h	FIFO4R1	Transmit and Receive FIFO Register 1 for Endpoint 4
8432h	FIFO4R2	Transmit and Receive FIFO Register 2 for Endpoint 4
		Dynamic FIFO Control Registers
8461h	-	Reserved
8462h	TXFIFOSZ_RXFIFOSZ	Transmit Endpoint FIFO Size, Receive Endpoint FIFO Size (Index register set to select Endpoints 1-4)
8465h	TXFIFOADDR	Transmit Endpoint FIFO Address (Index register set to select Endpoints 1-4)
8466h	RXFIFOADDR	Receive Endpoint FIFO Address (Index register set to select Endpoints 1-4)
846Dh	HWVERS	Hardware Version Register (See *TMS320C5517 Digital Signal Processor Technical Reference Manual* [SPRUH16].)

Table 6-30. Universal Serial Bus (USB) Registers[(1)] (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
		Control and Status Register for Endpoint 0
8501h	-	Reserved
8502h	PERI_CSR0	Control Status Register for Peripheral Endpoint 0
8505h	-	Reserved
8506h	-	Reserved
8509h	COUNT0	Number of Received Bytes in Endpoint 0 FIFO
850Ah	-	Reserved
850Dh	-	Reserved
850Eh	CONFIGDATA (Upper byte of 850Eh)	Returns details of core configuration.
		Control and Status Register for Endpoint 1
8511h	TXMAXP	Maximum Packet Size for Peripheral and Host Transmit Endpoint
8512h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8515h	RXMAXP	Maximum Packet Size for Peripheral and Host Receive Endpoint
8516h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8519h	RXCOUNT	Number of Bytes in the Receiving Endpoint's FIFO
851Ah	-	Reserved
851Dh	-	Reserved
851Eh	-	Reserved
		Control and Status Register for Endpoint 2
8521h	TXMAXP	Maximum Packet Size for Peripheral and Host Transmit Endpoint
8522h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8525h	RXMAXP	Maximum Packet Size for Peripheral and Host Receive Endpoint
8526h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8529h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
852Ah	-	Reserved
852Dh	-	Reserved
852Eh	-	Reserved
		Control and Status Register for Endpoint 3
8531h	TXMAXP	Maximum Packet Size for Peripheral and Host Transmit Endpoint
8532h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8535h	RXMAXP	Maximum Packet Size for Peripheral and Host Receive Endpoint
8536h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8539h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
853Ah	-	Reserved
853Dh	-	Reserved
853Eh	-	Reserved
		Control and Status Register for Endpoint 4
8541h	TXMAXP	Maximum Packet Size for Peripheral and Host Transmit Endpoint
8542h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8545h	RXMAXP	Maximum Packet Size for Peripheral and Host Receive Endpoint
8546h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8549h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
854Ah	-	Reserved
854Dh	-	Reserved
854Eh	-	Reserved

Table 6-30. Universal Serial Bus (USB) Registers[(1)] (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
		CPPI DMA (CMDA) Registers
9000h	DMAREVID1	CDMA Revision Identification Register 1
9001h	DMAREVID2	CDMA Revision Identification Register 2
9004h	TDFDQ	CDMA Teardown Free Descriptor Queue Control Register
9008h	DMAEMU	CDMA Emulation Control Register
9800h	TXGCR1[0]	Transmit Channel 0 Global Configuration Register 1
9801h	TXGCR2[0]	Transmit Channel 0 Global Configuration Register 2
9808h	RXGCR1[0]	Receive Channel 0 Global Configuration Register 1
9809h	RXGCR2[0]	Receive Channel 0 Global Configuration Register 2
980Ch	RXHPCR1A[0]	Receive Channel 0 Host Packet Configuration Register 1 A
980Dh	RXHPCR2A[0]	Receive Channel 0 Host Packet Configuration Register 2 A
9810h	RXHPCR1B[0]	Receive Channel 0 Host Packet Configuration Register 1 B
9811h	RXHPCR2B[0]	Receive Channel 0 Host Packet Configuration Register 2 B
9820h	TXGCR1[1]	Transmit Channel 1 Global Configuration Register 1
9821h	TXGCR2[1]	Transmit Channel 1 Global Configuration Register 2
9828h	RXGCR1[1]	Receive Channel 1 Global Configuration Register 1
9829h	RXGCR2[1]	Receive Channel 1 Global Configuration Register 2
982Ch	RXHPCR1A[1]	Receive Channel 1 Host Packet Configuration Register 1 A
982Dh	RXHPCR2A[1]	Receive Channel 1 Host Packet Configuration Register 2 A
9830h	RXHPCR1B[1]	Receive Channel 1 Host Packet Configuration Register 1 B
9831h	RXHPCR2B[1]	Receive Channel 1 Host Packet Configuration Register 2 B
9840h	TXGCR1[2]	Transmit Channel 2 Global Configuration Register 1
9841h	TXGCR2[2]	Transmit Channel 2 Global Configuration Register 2
9848h	RXGCR1[2]	Receive Channel 2 Global Configuration Register 1
9849h	RXGCR2[2]	Receive Channel 2 Global Configuration Register 2
984Ch	RXHPCR1A[2]	Receive Channel 2 Host Packet Configuration Register 1 A
984Dh	RXHPCR2A[2]	Receive Channel 2 Host Packet Configuration Register 2 A
9850h	RXHPCR1B[2]	Receive Channel 2 Host Packet Configuration Register 1 B
9851h	RXHPCR2B[2]	Receive Channel 2 Host Packet Configuration Register 2 B
9860h	TXGCR1[3]	Transmit Channel 3 Global Configuration Register 1
9861h	TXGCR2[3]	Transmit Channel 3 Global Configuration Register 2
9868h	RXGCR1[3]	Receive Channel 3 Global Configuration Register 1
9869h	RXGCR2[3]	Receive Channel 3 Global Configuration Register 2
986Ch	RXHPCR1A[3]	Receive Channel 3 Host Packet Configuration Register 1 A
986Dh	RXHPCR2A[3]	Receive Channel 3 Host Packet Configuration Register 2 A
9870h	RXHPCR1B[3]	Receive Channel 3 Host Packet Configuration Register 1 B
9871h	RXHPCR2B[3]	Receive Channel 3 Host Packet Configuration Register 2 B
A000h	DMA_SCHED_CTRL1	CDMA Scheduler Control Register 1
A001h	DMA_SCHED_CTRL2	CDMA Scheduler Control Register 1
A800h + 4 × *N*	ENTRYLSW[*N*]	CDMA Scheduler Table Word *N* Registers LSW (*N* = 0 to 63)
A801h + 4 × *N*	ENTRYMSW[*N*]	CDMA Scheduler Table Word *N* Registers MSW (*N* = 0 to 63)

Table 6-30. Universal Serial Bus (USB) Registers[1] (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
		Queue Manager (QMGR) Registers
C000h	QMGRREVID1	Queue Manager Revision Identification Register 1
C001h	QMGRREVID2	Queue Manager Revision Identification Register 2
C008h	DIVERSION1	Queue Manager Queue Diversion Register 1
C009h	DIVERSION2	Queue Manager Queue Diversion Register 2
C020h	FDBSC0	Queue Manager Free Descriptor and Buffer Starvation Count Register 0
C021h	FDBSC1	Queue Manager Free Descriptor and Buffer Starvation Count Register 1
C024h	FDBSC2	Queue Manager Free Descriptor and Buffer Starvation Count Register 2
C025h	FDBSC3	Queue Manager Free Descriptor and Buffer Starvation Count Register 3
C028h	FDBSC4	Queue Manager Free Descriptor and Buffer Starvation Count Register 4
C029h	FDBSC5	Queue Manager Free Descriptor and Buffer Starvation Count Register 5
C02Ch	FDBSC6	Queue Manager Free Descriptor and Buffer Starvation Count Register 6
C02Dh	FDBSC7	Queue Manager Free Descriptor and Buffer Starvation Count Register 7
C080h	LRAM0BASE1	Queue Manager Linking RAM Region 0 Base Address Register 1
C081h	LRAM0BASE2	Queue Manager Linking RAM Region 0 Base Address Register 2
C084h	LRAM0SIZE	Queue Manager Linking RAM Region 0 Size Register
C085h	-	Reserved
C088h	LRAM1BASE1	Queue Manager Linking RAM Region 1 Base Address Register 1
C089h	LRAM1BASE2	Queue Manager Linking RAM Region 1 Base Address Register 2
C090h	PEND0	Queue Manager Queue Pending 0
C091h	PEND1	Queue Manager Queue Pending 1
C094h	PEND2	Queue Manager Queue Pending 2
C095h	PEND3	Queue Manager Queue Pending 3
C098h	PEND4	Queue Manager Queue Pending 4
C099h	PEND5	Queue Manager Queue Pending 5
D000h + 16 × *R*	QMEMRBASE1[*R*]	Queue Manager Memory Region *R* Base Address Register 1 (*R* = 0 to 15)
D001h + 16 × *R*	QMEMRBASE2[*R*]	Queue Manager Memory Region *R* Base Address Register 2 (*R* = 0 to 15)
D004h + 16 × *R*	QMEMRCTRL1[*R*]	Queue Manager Memory Region *R* Control Register 1 (*R* = 0 to 15)
D005h + 16 × *R*	QMEMRCTRL2[*R*]	Queue Manager Memory Region *R* Control Register 2 (*R* = 0 to 15)
E000h + 16 × *N*	CTRL1A	Queue Manager Queue *N* Control Register 1A (*N* = 0 to 63)
E001h + 16 × *N*	CTRL2A	Queue Manager Queue *N* Control Register 2A (*N* = 0 to 63)
E004h + 16 × *N*	CTRL1B	Queue Manager Queue *N* Control Register 1B (*N* = 0 to 63)
E005h + 16 × *N*	CTRL2B	Queue Manager Queue *N* Control Register 2B (*N* = 0 to 63)
E008h + 16 × *N*	CTRL1C	Queue Manager Queue *N* Control Register 1C (*N* = 0 to 63)
E009h + 16 × *N*	CTRL2C	Queue Manager Queue *N* Control Register 2C (*N* = 0 to 63)
E00Ch + 16 × *N*	CTRL1D	Queue Manager Queue *N* Control Register 1D (*N* = 0 to 63)
E00Dh + 16 × *N*	CTRL2D	Queue Manager Queue *N* Control Register 2D (*N* = 0 to 63)
E800h + 16 × *N*	QSTAT1A	Queue Manager Queue *N* Status Register 1A (*N* = 0 to 63)
E801h + 16 × *N*	QSTAT2A	Queue Manager Queue *N* Status Register 2A (*N* = 0 to 63)
E804h + 16 × *N*	QSTAT1B	Queue Manager Queue *N* Status Register 1B (*N* = 0 to 63)
E805h + 16 × *N*	QSTAT2B	Queue Manager Queue *N* Status Register 2B (*N* = 0 to 63)
E808h + 16 × *N*	QSTAT1C	Queue Manager Queue *N* Status Register 1C (*N* = 0 to 63)
E809h + 16 × *N*	QSTAT2C	Queue Manager Queue *N* Status Register 2C (*N* = 0 to 63)

6.3 Identification

6.3.1 JTAG Identification

Table 6-31. JTAG Identification Register

CPU WORD ADDRESS	ACRONYM	REGISTER NAME	COMMENTS
N/A	JTAGID	JTAG Identification Register	Read-only. Provides 32-bit JTAG ID of the device.

The JTAG ID register is a read-only register that identifies to the customer the JTAG and Device ID. The register hex value for the device is: 0x0B95 602F. For the actual register bit names and their associated bit field descriptions, see Figure 6-2 and Table 6-32.

31-28	27-12	11-1	0
VARIANT (4-Bit)	PART NUMBER (16-Bit)	MANUFACTURER (11-Bit)	LSB
R-0000	R-1011 1001 0101 0110	R-0000 0010 111	R-1

LEGEND: R = Read, W = Write, n = value at reset

Figure 6-2. JTAG ID Register Description - Register Value - 0x0B95 602F

Table 6-32. JTAG Identification Register Selection Bit Descriptions

BIT	NAME	DESCRIPTION
31:28	VARIANT	Variant (4-Bit) value: 0000
27:12	PART NUMBER	Part Number (16-Bit) value: 1011 1001 0101 0110
11:1	MANUFACTURER	Manufacturer (11-Bit) value: 0000 0010 111
0	LSB	LSB. This bit is read as a "1".

6.4 Boot Modes

The device supports the following boot modes:

- NOR Flash
- NAND Flash
- SPI 16- and 24-bit EEPROM or Flash
- I2C 16-bit EEPROM
- eMMC Controller/MMC/SD/SDHC Card
- USB
- UART
- McSPI
- UHPI

The boot mode or method is determined by checking the value of the BootMode[5:0] bits in the BootMode register ([1C34h]) and the CLKSELSTAT bit in the CCR2 register ([1C1Fh]), which reflect the configurations of the EM_A[20:15] or GP[26:21] pins and CLK_SEL pin at reset. See Section 5.7.3.4.2, *BootMode Implementation and Requirements*.

Figure 6-3. BootMode Register [1C34h]

15	11	10	5	4	0
Reserved		BootMode[5:0]		Reserved	
R-0		R-EM_A[20:15]/GP[26:21]		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-33. BootMode Register Field Descriptions

Bit	Name	Description
15:11	Reserved	Reserved
10:9	BootMode[5:4]	Read-only bits that reflect the latched state of the EM_A[20:19] or GP[26:25] pins on the 10th clock edge after RESET pin goes high.(1) The Bootloader reads this register value to determine the frequency of the clock input to the system clock generator. The bootloader requires this frequency to appropriately program the system clock generator and other peripheral clock dividers. 00: CLK_SEL = 0: 12 MHz via the on-chip USB oscillator CLK_SEL = 1: 11.2896 MHz via the CLK_IN pin 01: CLK_SEL = 0: 12 MHz via the on-chip USB oscillator CLK_SEL = 1: 12.00 MHz or 12.288 MHz via the CLK_IN pin 10: CLK_SEL = 0: 12 MHz via the on-chip USB oscillator CLK_SEL = 1: 16.8 MHz via the CLK_IN pin 11: CLK_SEL = 0: 12 MHz via the on-chip USB oscillator CLK_SEL = 1: 19.2 MHz via the CLK_IN pin

(1) The $\overline{\text{RESET}}$ pin is asynchronous to the selected system clock (CLKIN or USB_OSC). The pin could be 10, 11, or even 12 clock cycles after the rising edge of RESETN due to possible metastability.

Table 6-33. BootMode Register Field Descriptions (continued)

Bit	Name	Description
8:5	BootMode[3:0]	Read-only bits that reflect the latched state of the EM_A[18:15] or GP[24:21] pins on the first clock edge after RESET pin goes high. The Bootloader determines boot mode based on this value. 0000: Boot mode: 16-bit NOR flash data boot, system clock generator is in bypass mode. 0001: Boot mode: 16-bit or 8-bit NAND flash data boot, system clock generator is in bypass mode. 0010: Boot mode: UART 9600 baud boot, system clock generator output = input clock x 3 0011: Boot mode: UART 57600 baud boot, system clock generator output = input clock x 3 0100: Boot mode: UART 115200 baud boot, system clock generator output = input clock x 3 0101: Boot mode: SPI 16-bit or 24-bit address Boot (SPI_CLK < 1 MHz), system clock generator output = input clock x 3 0110: Boot mode: SPI 16-bit or 24-bit address Boot (SPI_CLK < 10 MHz), system clock generator output = input clock x 3 0111: Polling Mode 2: Check for valid boot image from peripherals in the following order: NOR, NAND, SPI, I2C, SD/SDHC/MMC/eMMC Controller 0, McSPI, and UART/USB (infinite retry).(2) 1000: Boot mode: I2C 16-bit address Boot, 400 kHz, system clock generator is in bypass mode. 1001: Boot mode: SD or SDHC, MMC, or eMMC Controller 0 card boot, system clock generator is in bypass mode 1010: Boot mode: SD or SDHC, MMC, or eMMC Controller 1 card boot, system clock generator is in bypass mode 1011: Polling Mode 1: Check for valid boot image from peripherals in the following order: NOR, NAND, SPI, I2C, SD/SDHC/MMC/eMMC Controller 0, SD/SDHC/MMC/eMMC Controller 1, and UART/USB (infinite retry).(2) 1100: Boot mode: UHPI 16-bit multiplexed mode boot, system clock generator output = input clock x 3 1101: Boot mode: McSPI 24-bit address serial flash at 10-MHz mode 1110: Boot mode: McSPI 24-bit address serial flash at 40-MHz mode 1111: Boot mode: USB boot, system clock generator output = input clock x 3
4:0	Reserved	Reserved

(2) If MMCx_CMD is low, the bootloader continues to check for a valid boot image in the card controller. MMCx_CMD must be high or toggle in order to move from the card controller to the next peripheral for a valid boot image.

Figure 6-4. Clock Configuration Register 2 (CCR2) [1C1Fh]

15 6	5 4	3	2	1	0
Reserved	Reserved	Reserved	CLKSELSTAT	Reserved	SYSCLKSEL
R-0	R-x	R/W-0	R-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset; -x = value undetermined

Table 6-34. Clock Configuration Register 2 (CCR2) Field Descriptions

BIT	NAME	VALUE	DESCRIPTION
15:6	RESERVED	0	Reserved
5:4	RESERVED	0	Reserved
3	RESERVED	0	Reserved. This bit must be written to 0.
2	CLKSELSTAT		CLK_SEL pin status bit. This reflects the state of the CLK_SEL pin.
		0	CLK_SEL pin is low (USB Oscillator clock selected).
		1h	CLK_SEL pin is high (CLKIN input clock selected).
1	RESERVED	0	Reserved. This bit must be written to 0.
0	SYSCLKSEL		System clock source select bit. This bit is used to select between the two main clocking modes for the DSP: bypass and PLL mode. In bypass mode, the system clock generator is bypassed and the system clock is set to either CLKIN or the USB oscillator output (as determined by the CLKSEL pin). In PLL mode, the system clock is set to the output of the system clock generator.
		0	Bypass mode is selected.
		1	PLL mode is selected.

6.4.1 Invocation Sequence

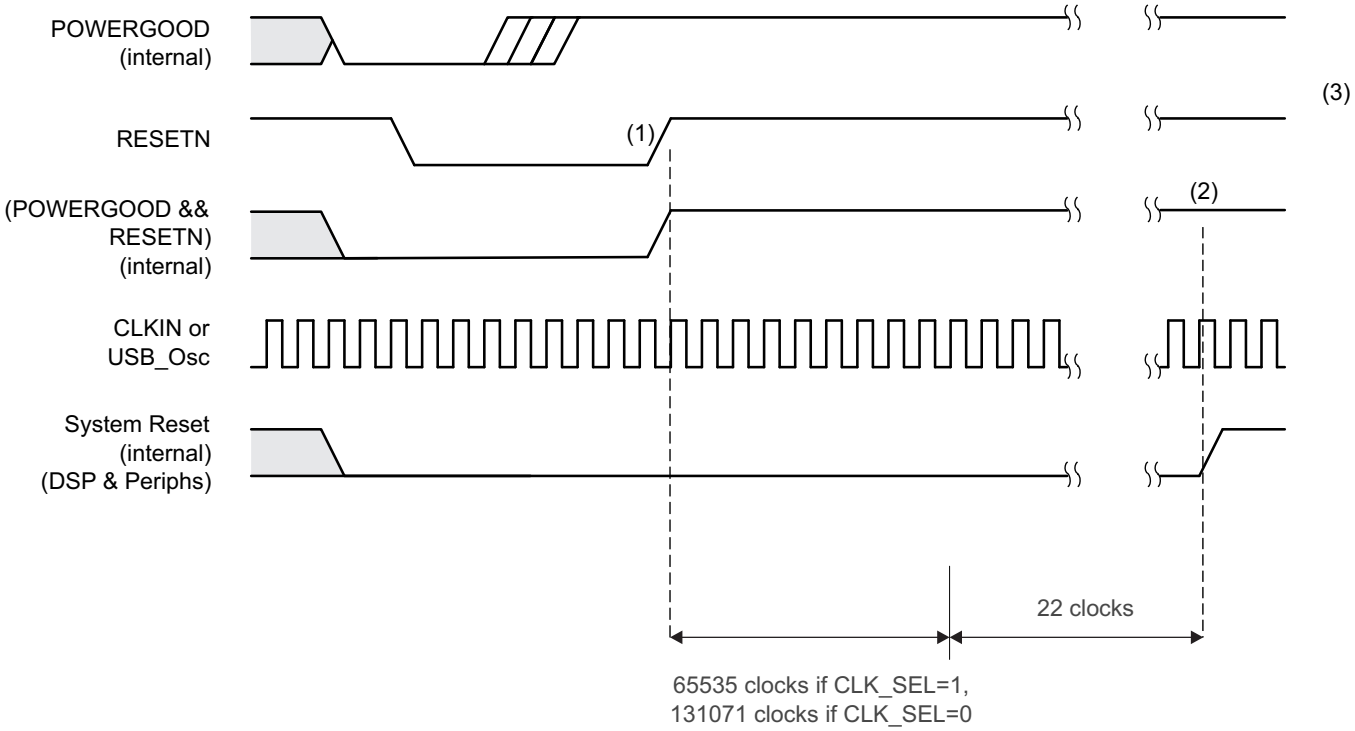
The boot sequence is a process by which the device's on-chip memory is loaded with program and data sections from an external image file (in flash memory, for example). The boot sequence also allows, optionally, for some of the device's internal registers to be programmed with predetermined values. The boot sequence is started automatically after each device reset. For more details on device reset, see Section 5.7.3, *Reset.*

This device can boot from EMIF, UART, SPI, I2C, eMMC, MMC, SD, SDHC, UHPI, McSPI, or USB interface. For a complete description of the boot options, see *Using the TMS320C5517 Bootloader* [literature number SPRABP1].

The peripheral interface that the device boots from is determined by the configuration of the EM_A[20:15] or GP[26:21] pins at reset. The values of EM_A[20:15] or GP[26:21] are latched at reset into the BootMode[5:0] bits in the BootMode register (1C34h) and the Bootloader reads the bits to determine a peripheral interface for booting.

The on-chip Bootloader allows the DSP registers to be configured during the boot process, if the optional register configuration section is present in the boot image. For more information on the boot modes supported, see Section 6.4, *Boot Modes*.

See Figure 6-5, *Boot Timing*, and the notes at the bottom of the figure, for an illustration of the boot sequence.



(1) Enter the boot sequence described in boot sequence Step 1.
(2) The maximum wait time from reset between (1) and (2) until the reset is released is 20 ms.
(3) The bootloaded code starts. The best-case time is 200 ms from the start of the boot sequence (see note 2) due to the BG_CAP settling time in Step 18. The worst-case time is the loading time for the bootloaded code when it exceeds 200 ms.

Figure 6-5. Boot Timing

The device bootloader follows the following steps:

1. Immediately after reset, the CPU fetches the reset vector from 0xFFFF00. MP or $\overline{MC}$ is 0 by default, so 0xFFFF00 is mapped to internal ROM. The PLL is in bypass mode. The input clock is assumed to be in the range of 11.2896–19.2 MHz.
2. Set CLKOUT slew rate control to slow slew rate.
3. Idle all peripherals and HWA.
4. Apply manufacturing trim to the bandgap references.
5. Disable CLKOUT.
6. The Bootloader configures the system clock generator based on boot mode (see Section 6.4, *Boot Modes*, for details on boot mode) and enables TIMER0 to count the settling time of BG_CAP. Bootloader will try this main loop infinitely if it cannot get the correct boot signature.

   [Main Loop]
7. If McSPI boot, test for 24-bit McSPI flash boot on SPI_CS[0] using a clock-rate close to, but not over, 10 MHz, or a clock-rate close to, but not over, 40 MHz based on the boot mode. Set Serial Port 1 Mode on the External Bus Selection Register to 1:
   (a) Check the first two bytes read from the boot table for a boot signature match using 24-bit address mode.
   (b) If the boot signature is not valid, go to step 18.
   (c) Set Register Configuration, if present in boot image.
   (d) Attempt McSPI Serial Memory boot and go to step 19.
8. If UHPI boot, the external host has to communicate in 16-bit multiplexed mode:
   Note: The bootloader sets up the UHPI slave to handshake with an external UHPI master.
   (a) The external host power up the device and must wait for the settling time of BG_CAP to elapse before executing the next step.
   (b) The bootloader waits for the external host to finish transferring the data.
   (c) External Host writes to device on-chip memory. The code or data sections are directly loaded to the desired locations on device by the external host.
   (d) External Host interrupts the device through the DSP_INT in the UHPIC register after code transfer complete.
   (e) Bootloader branches to the entry point. The entry point is located in the last block of SARAM, word addresses 0x27FFA and 0x27FFB. To ensure data integrity, the external host writes two 16-bit signatures in 0x27FFC and 0x27FFD with respective values of 0x1234 and 0xABCD. If the address of the entry point is in DARAM space or incorrect signatures are detected in 0x27FFC and 0x27FFD, go to step 18.
   (f) Go to step 19.
9. If NOR boot, test for NOR boot on all asynchronous CS spaces ($\overline{EM\_CS[2:5]}$) with 16-bit access:
   Note: The booatloader requires NOR flash that supports a reset command (0xF0 on data).
   (a) Check the first 2 bytes read from boot signature.
   (b) If the boot signature is not valid, go to step 18.
   (c) Set Register Configuration, if present in boot image.
   (d) Attempt NOR boot and go to step 19.
10. If NAND boot, test for NAND boot on all asynchronous CS spaces ($\overline{EM\_CS[2:5]}$) with 16-bit access:
    (a) Check the first 2 bytes read from boot table for a boot signature match. If the boot signature is not valid, read the first 2 bytes again using 8-bit access on all asynchronous CS spaces ($\overline{EM\_CS[2:5]}$)
    (b) If the boot signature is still not valid, go to step 18.
    (c) Set Register Configuration, if present in boot image.
    (d) Attempt NAND boot and go to step 19.

11. If SPI boot, test for 16- and 24-bit SPI EEPROM or Flash boot on SPI_CS[0] using a clock-rate close to, but not over, 1 MHz, or a clock-rate close to, but not over, 10 MHz based on the boot mode. Set Parallel Port Mode on the External Bus Selection Register to 5, then set to 6:
    (a) Check the first 2 bytes read from boot table for a boot signature match using 16-bit address mode.
    (b) If the boot signature is not valid, read the first 2 bytes again using 24-bit address mode.
    (c) If the boot signature is not valid from either case (16-bit and 24-bit address modes), go to step 18.
    (d) Set Register Configuration, if present in boot image.
    (e) Attempt SPI Serial Memory boot and go to step 19.
12. If I2C boot, test for 16-bit I2C EEPROM boot with a 7-bit slave address 0x50 and 400-kHz clock rate.
    (a) Check the first 2 bytes read from boot table for a boot signature match using 16-bit address mode.
    (b) If the boot signature is not valid, go to step 18.
    (c) Set Register Configuration, if present in boot image.
    (d) Attempt I2C EEPROM boot and go to step 19.
13. If eMMC, MMC, SD, or SDHC Controller 0 boot, program SD0 and search for the filename “bootimg.bin" under the first partition’s root directory. For SD or SDHC, the device must comply with SD/SDHC specification v1.1 or v2.0 for FAT16 or FAT32 using SD or SDHC unsecure mode.
    If eMMC, the bootloader will check the boot partition for a bootable image before checking the root directory for "bootimg.bin". For eMMC or MMC, the device must comply with eMMC/MMC specification v4.3 for FAT32 using eMMC or MMC nonencrypted mode.
    (a) Check the first 2 bytes read from boot table for a boot signature match.
    (b) If the boot signature is not valid, go to step 18.
    (c) Set Register Configuration, if present in boot image.
    (d) Attempt eMMC, MMC, SD, or SDHC boot and go to step 19.
14. If eMMC, MMC, SD, or SDHC Controller 1 boot, program SD1 and search for the filename “bootimg.bin" under the first partition’s root directory. For SD or SDHC, the device must comply with SD/SDHC specification v1.1 or v2.0 for FAT16 or FAT32 using SD or SDHC unsecure mode.
    If eMMC, the bootloader will check the boot partition for a bootable image before checking the root directory for "bootimg.bin". For eMMC or MMC the device must comply with eMMC/MMC specification v4.3 for FAT32 using eMMC or MMC nonencrypted mode.
    Note: Do not boot from eMMC if no valid image is present. Booting from eMMC without a valid image will put the card into an inactive state.
    (a) Check the first two bytes read from boot table for a boot signature match.
    (b) If the boot signature is not valid, go to step 18.
    (c) Set Register Configuration, if present in boot image.
    (d) Attempt eMMC, MMC, SD, or SDHC boot and go to step 19.
15. If UART boot, set PLL to multiply the input clock by 3 and adjust TIMER0 for the settling time of BG_CAP. Program UART with 9600-, 57600-, or 115200-baud based on boot mode, 8-bit data, odd parity, one stop-bit, and auto flow control using CTS or RTS:
    (a) Check the first 2 bytes read from boot table for a boot signature match.
    (b) If the boot signature is not valid, return to the beginning of step 15.
    (c) Attempt UART boot and go to step 19.

16. If USB boot, set PLL to multiply the input clock by 3 and adjust TIMER0 for the settling time of BG_CAP. Use USB on endpoint 1. The device has vendor-ID 0x0451 and product-ID 0x9010 and uses Bulk Endpoint 1 OUT to receive the boot image from the USB host:
    (a) Check the first 2 bytes read from boot table for a boot signature match.
    (b) If the boot signature is not valid, return to the beginning of step 16.
    (c) Attempt USB boot and go to step 19.
17. If polling mode, there is a fixed order of supported boot devices on which a valid image is checked.
    – Polling Mode 1:
        (a) NOR
        (b) NAND
        (c) SPI
        (d) I2C
        (e) SD/SDHC, MMC/eMMC Controller 0 (see note below)
        (f) SD/SDHC, MMC/eMMC Controller 1 (see note below)
        (g) UART/USB
    – Polling Mode 2:
        (a) NOR
        (b) NAND
        (c) SPI
        (d) I2C
        (e) SD/SDHC, MMC/eMMC Controller 0 (see note below)
        (f) McSPI
        (g) UART/USB

    The first device with a valid boot image is used to load and execute user code. If none of these devices has a valid boot image, the bootloader modifies the CPU clock setup as follows:
    – If CLK_SEL=0, the bootloader powers up the PLL and sets its frequency to 36 MHz (12 MHz multiplied by 3).
    – If CLK_SEL=1, the bootloader powers up the PLL and sets it to multiply CLKIN by 3.

    This change in the CPU clock setup is required to meet the minimum frequency needed by the USB module. After the CPU clock setup changes, the bootloader enters an endless loop and checks for data received on the UART/USB. If a valid boot image is received, the image is used to load and execute user code. If no valid boot image is received, the bootloader continues to monitor the boot devices. If the time since the trim setup exceeds 200 ms during this endless loop, the bootloader re-enables the low-voltage detection circuit to ensure the circuit is not disabled for an extended period.

    Note: If MMCx_CMD is low, the bootloader continues to check for a valid boot image in the card controller. MMCx_CMD must be high or toggle in order to move from the card controller to the next peripheral for a valid boot image.
18. If the boot signature is not valid, toggle XF when the retry count reaches 100.
19. Copy the boot image sections to system memory. Then set the XF port low to indicate that boot-up is complete. Ensure the settling time of BG_CAP has elapsed since step 6 before proceeding to execute the bootloaded code.
20. Jump to the specified entry point.

6.4.2 DSP Resources Used By the Bootloader

The Bootloader uses SARAM block 31 for the storing of temporary data. This block of memory is reserved during the boot process. However, after the boot process is complete, it can be used by the user application.

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

TI offers an extensive line of development tools for the TMS320C55x DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio Integrated Development Environment (IDE).

The following products support development of TMS320C55x fixed-point DSP-based applications:

Software Development Tools:

Code Composer Studio Integrated Development Environment (IDE): Version 5.5.0 or later

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP/BIOS Version 5.33 or later), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:

Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the TMS320C55x DSP platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

7.1.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, TMS320C5517AZCHA20). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX or TMDX) through fully qualified production devices or tools (TMS or TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully-qualified production device.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

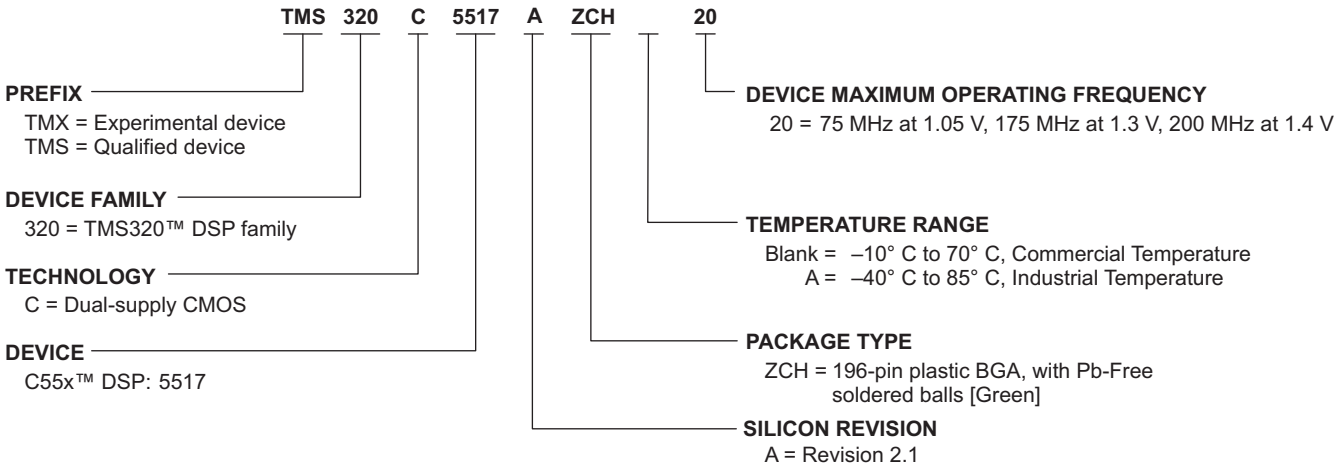
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZCH), and the temperature range (for example, "Blank" is the commercial temperature range).

Figure 7-1 provides a legend for reading the complete device name for any DSP platform member.



A. For actual device part numbers (P/Ns) and ordering information, see the TI website (http://www.ti.com)

Figure 7-1. Device Nomenclature

7.2 Documentation Support

7.2.1 Related Documentation

The following documents describe the DSP. To access the documents, click the literature number (e.g., SPRUH16) or wiki link.

The current documentation that describes the DSP, related peripherals, and other technical collateral, is available in the product folder at www.ti.com.

SPRUH16 ***TMS320C5517 Digital Signal Processor Technical Reference Manual.*** Collection of documents providing detailed information on the device including system control, FFT implementation, and memory access. Detailed information on the device as well as a functional description of the peripherals supported is also included.

SPRZ383 ***TMS320C5517 Fixed-Point Digital Signal Processor Silicon Errata.*** Describes the known exceptions to the functional specifications for this device.

SPRABP1 ***Using the TMS320C5517 Bootloader.*** Describes features of the on-chip ROM for this device, as well as descriptions of how to interface with possible boot devices and generating a boot image to store on an external device.

SWPU073 ***TMS320C55x DSP v3.x CPU Reference Guide.*** Describes more detailed information on the C55x CPU.

Wiki ***C5505/15/35 Schematic Checklist.*** Describes recommendations for the device applicable to unused pins, clocking, power, reset, and peripherals. Description also includes critical connections, DDR2 routing checklist, and debug considerations, and more.

7.3 社区资源

下列链接提供到 TI 社区资源的连接。 链接的内容由各个分销商“按照原样”提供。 这些内容并不构成 TI 技术规范和标准且不一定反映 TI 的观点；请见 TI 的使用条款。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

8 Mechanical Packaging and Orderable Information

The following packaging information and addendum reflect the most current data available for the designated device. This data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMS320C5517AZCH20	Active	Production	NFBGA (ZCH) | 196	184 | JEDEC TRAY (5+1)	Yes	Call TI	Level-3-260C-168 HR	-10 to 70	17AZCH20
TMS320C5517AZCH20.A	Active	Production	NFBGA (ZCH) | 196	184 | JEDEC TRAY (5+1)	Yes	Call TI	Level-3-260C-168 HR	-10 to 70	17AZCH20
TMS320C5517AZCHA20	Active	Production	NFBGA (ZCH) | 196	184 | JEDEC TRAY (5+1)	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	17AZCHA20
TMS320C5517AZCHA20.A	Active	Production	NFBGA (ZCH) | 196	184 | JEDEC TRAY (5+1)	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	17AZCHA20
TMS32C5517AZCHA20R	Active	Production	NFBGA (ZCH) | 196	1000 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	17AZCHA20
TMS32C5517AZCHA20R.A	Active	Production	NFBGA (ZCH) | 196	1000 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	17AZCHA20

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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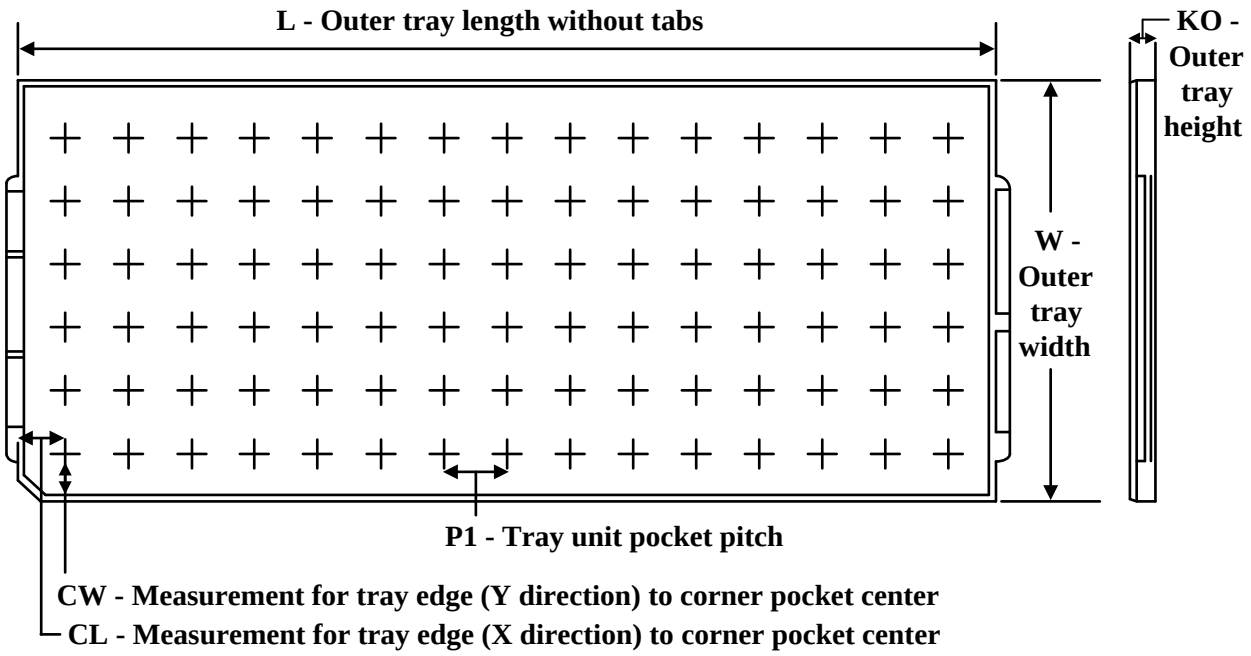
TRAY

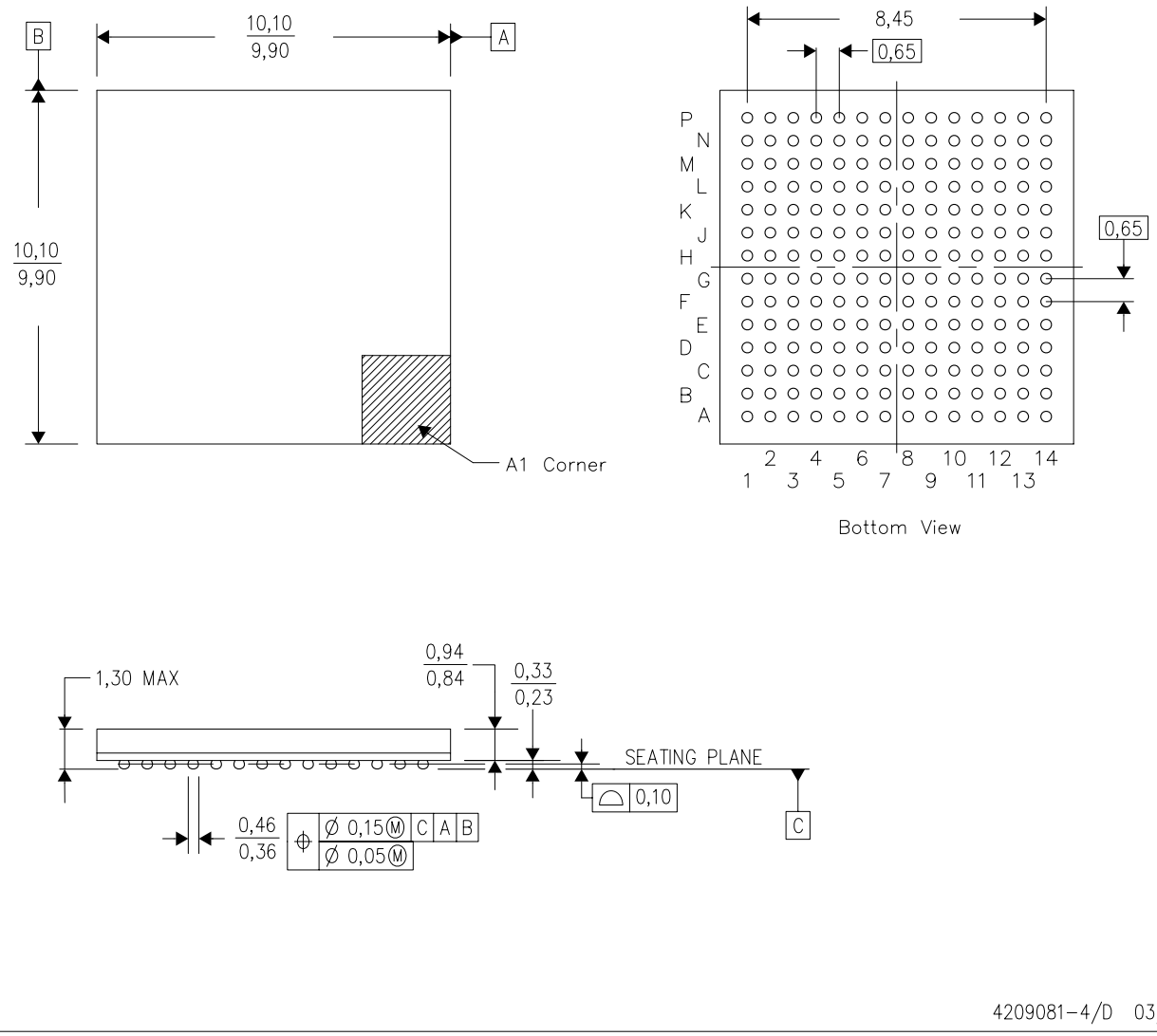


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TMS320C5517AZCH20	ZCH	NFBGA	196	184	8 x 23	150	315	135.9	7620	13.4	10.1	19.65
TMS320C5517AZCH20.A	ZCH	NFBGA	196	184	8 x 23	150	315	135.9	7620	13.4	10.1	19.65
TMS320C5517AZCHA20	ZCH	NFBGA	196	184	8 x 23	150	315	135.9	7620	13.4	10.1	19.65
TMS320C5517AZCHA20.A	ZCH	NFBGA	196	184	8 x 23	150	315	135.9	7620	13.4	10.1	19.65

ZCH (S–PBGA–N196) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. nFBGA configuration
D. This is a Pb–free solder ball design.

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