配备 I^{2}C 和 SMBus 接口并采用行业标准 LM75 外形尺寸和引脚排列的 TMP275-Q1 汽车级 ±0.75°C 温度传感器

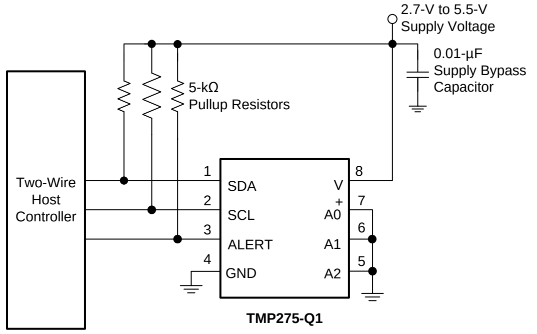
1 特性

- 具有符合 AEC-Q100 标准的以下结果：
  - 温度 1 级：-40°C 至 +125°C 的工作环境温度范围
  - 人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 组件充电模式 (CDM) ESD 分类等级 C6
- 高精度：
  - −10°C 至 +85°C 范围内为 ±0.75°C（最大值）
  - −40°C 至 +125°C 范围内为 ±1.5°C（最大值）
- 低静态电流：
  - 50µA（典型值）
  - 0.1µA（待机状态）
- 分辨率：9 至 12 位，用户可选
- 数字输出： SMBus™、两线制和 I^{2}C 接口兼容性
- 8 个 I^{2}C/系统管理总线 (SMBus) 地址
- 宽电源电压范围：2.7V 至 5.5V
- 小型 8 引脚超薄小外形尺寸 (VSSOP) 封装和 8 引脚小外形集成电路 (SOIC) 封装
- 无需指定加电序列，可在 V+ 之前使能双线制总线上拉

2 应用

- 汽车空调
- 信息娱乐处理器管理
- 空气流量传感器
- 电池控制单元
- 引擎控制单元
- UREA 传感器
- 抽水机
- HID 灯
- 安全气囊控制单元

简化电路原理图



3 说明

TMP275-Q1 是一款具有 12 位模数转换器 (ADC) 的 ±0.75°C 精密集成数字温度传感器，可在低至 2.7V 的电源电压下运行，并且与德州仪器 (TI) LM75、TMP75、TMP75B 和 TMP175 器件的引脚和寄存器兼容。TMP275-Q1 器件提供 8 引脚 SOIC 和 VSSOP 两种封装，不需要外部元件便可测温。该器件能够以最高 0.0625°C（12 位），最低 0.5°C（9 位）的分辨率读取温度，从而允许用户编程更高的分辨率或更短的转换时间来最大限度地提升效率。该器件的额定运行温度范围为 -40°C 至 +125°C。

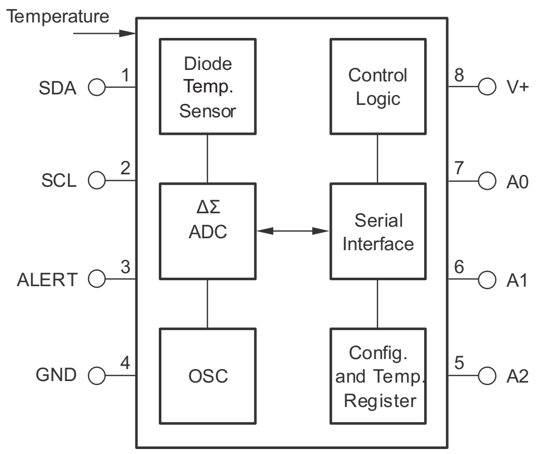
TMP275-Q1 器件 具有 SMBus 和两线制接口兼容性，并且可在同一总线上借助 SMBus 过热报警功能支持多达 8 个器件。厂家校准的温度精度和抗扰数字接口使得 TMP275-Q1 成为其他传感器和电子元器件温度补偿的首选解决方案，而且无需针对分布式温度感测进行额外的系统级校准或复杂的电路板布局布线。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
TMP275-Q1	SOIC (8)	4.90mm x 3.91mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

内部框图



目录

4 修订历史记录

Changes from Revision A (January 2016) to Revision B **Page**

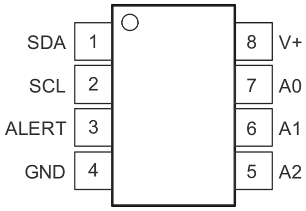
- 已更改 将*特性* 和*说明* 标题中的温度（最大值）从“±0.5°C”更改为“±0.75°C”；在“高精度”行下将 ±0.75°C 精度的温度范围从“–20°C 至 100°C”更改为“–10°C 至 85°C” 1
- Changed first test condition temperature range in "Accuracy" row from "–20°C to 100°C" to "–10°C to 85°C"; change MAX value in same row from "±0.5°C" to "±0.75°C" 5

Changes from Original (November 2015) to Revision A **Page**

- Changed *Thermal Information* table specifications 4

5 Pin Configuration and Functions

D, DGK Packages
8-Pin SOIC, VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SDA	I/O	Serial data. Open-drain output; requires a pullup resistor.
2	SCL	I	Serial clock. Open-drain output; requires a pullup resistor.
3	ALERT	O	Overtemperature alert. Open-drain output; requires a pullup resistor.
4	GND	—	Ground
5	A2	I	Address select. Connect to GND or V+.
6	A1	I	
7	A0	I	
8	V+	I	Supply voltage, 2.7 V to 5.5 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply, V+		7	V
Input voltage(2)	–0.5	7	V
Input current		10	mA
Operating temperature	–55	127	°C
Junction temperature, T_J max		150	°C
Storage temperature, T_{stg}	–60	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input voltage rating applies to all TMP275-Q1 input voltages.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	2.7		5.5	V
Operating free-air temperature, T_A	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP275-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.6	185	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.5	76.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	106.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23	14.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.5	104.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = –40°C to +125°C and V+ = 2.7 V to 5.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT							
	Range			–40		125	°C
	Accuracy (temperature error)		–10°C to 85°C, V+ = 3.3 V		±0.125	±0.75	°C
			0°C to 100°C, V+ = 3 V to 3.6 V		±0.125	±1	
			–40°C to 125°C, V+ = 3 V to 3.6 V		±0.125	±1.5	
			25°C to 100°C, V+ = 3.3 V to 5.5 V		±0.2	±2	
	Resolution(1)		Selectable		0.0625		°C
DIGITAL INPUT/OUTPUT							
	Input capacitance				3		pF
V_{IH}	High-level input logic			0.7 (V+)		6	V
V_{IL}	Low-level input logic			–0.5		0.3 (V+)	V
I_{IN}	Leakage input current		0 V ≤ V_{IN} ≤ 6 V			1	µA
	Input voltage hysteresis		SCL and SDA pins		500		mV
V_{OL}	Low-level output logic	SDA	I_{OL} = 3 mA	0	0.15	0.4	V
		ALERT	I_{OL} = 4 mA	0	0.15	0.4	
	Resolution		Selectable		9 to 12		Bits
	Conversion time		9 bits		27.5	37.5	ms
			10 bits		55	75	
			11 bits		110	150	
			12 bits		220	300	
	Time-out time			25	54	74	ms
POWER SUPPLY							
	Operating range			2.7		5.5	V
I_Q	Quiescent current		Serial bus inactive		50	85	µA
			Serial bus active, SCL frequency = 400 kHz		100		
			Serial bus active, SCL frequency = 3.4 MHz		410		
I_{SD}	Shutdown current		Serial bus inactive		0.1	3	µA
			Serial bus active, SCL frequency = 400 kHz		60		
			Serial bus active, SCL frequency = 3.4 MHz		380		
TEMPERATURE RANGE							
	Specified range			–40		125	°C
	Operating range			–55		127	°C

(1) Specified for 12-bit resolution.

6.6 Timing Requirements

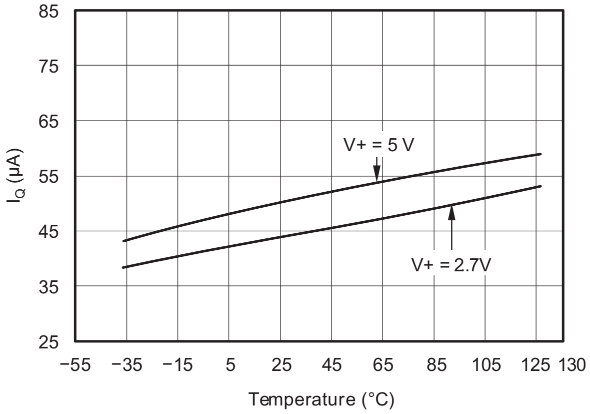
see the *Timing Diagrams* section for timing diagrams(1)

			FAST MODE		HIGH-SPEED MODE		UNIT
			MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	V+	0.001	0.4	0.001	2.38	MHz
$t_{(BUF)}$	Bus-free time between STOP and START condition	See the *Timing Diagrams* section	1300		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.		600		160		ns
$t_{(SUSTA)}$	repeated start condition setup time		600		160		ns
$t_{(SUSTO)}$	STOP condition setup time		600		160		ns
$t_{(HDDAT)}$	Data hold time		4	900	4	120	ns
$t_{(SUDAT)}$	Data setup time		100		10		ns
$t_{(LOW)}$	SCL-clock low period	V+ , see the *Timing Diagrams* section	1300		280		ns
$t_{(HIGH)}$	SCL-clock high period	See the *Timing Diagrams* section	600		60		ns
t_FD	Data fall time	See the *Timing Diagrams* section		300		150	ns
t_RC	Clock rise time	See the *Two-Wire Timing Diagrams* section		300		40	ns
		SCLK ≤ 100 kHz, see the *Timing Diagrams* section		1000			ns
t_FC	Clock fall time	See the *Two-Wire Timing Diagrams* section		300		40	ns

(1) Values are based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not specified and are not production tested.

6.7 Typical Characteristics

at T_A = 25°C and V+ = 5 V (unless otherwise noted)



Serial bus inactive

Figure 1. Quiescent Current vs Temperature

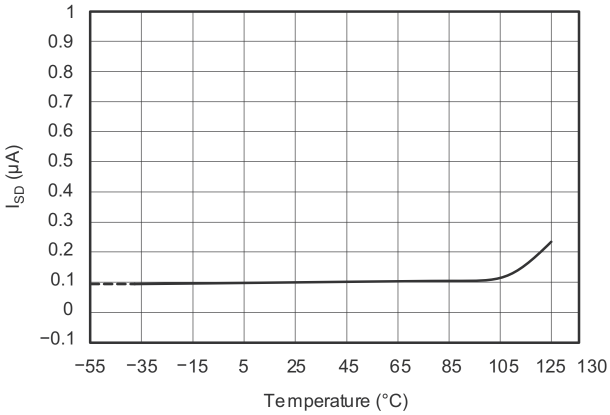
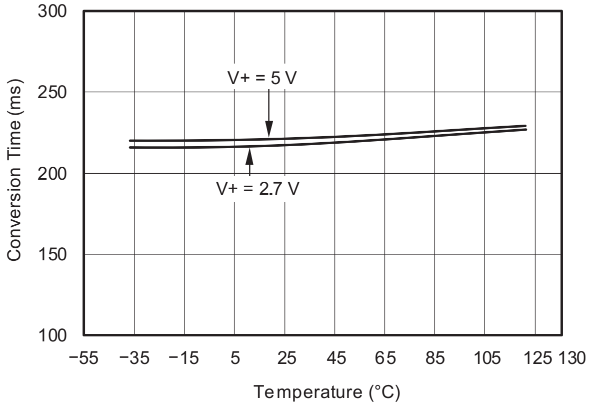


Figure 2. Shutdown Current vs Temperature



12-bit resolution

Figure 3. Conversion Time vs Temperature

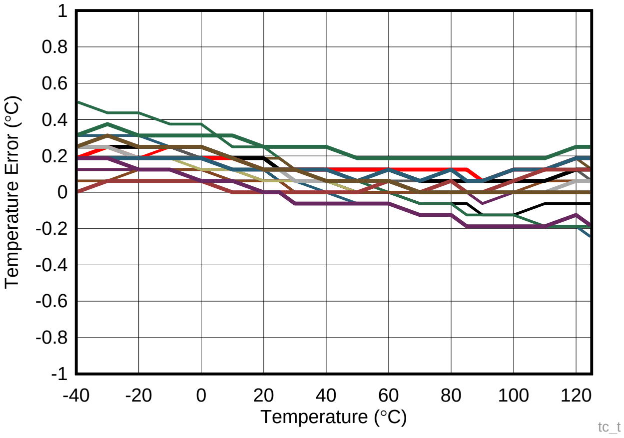


Figure 4. Temperature Error vs Temperature

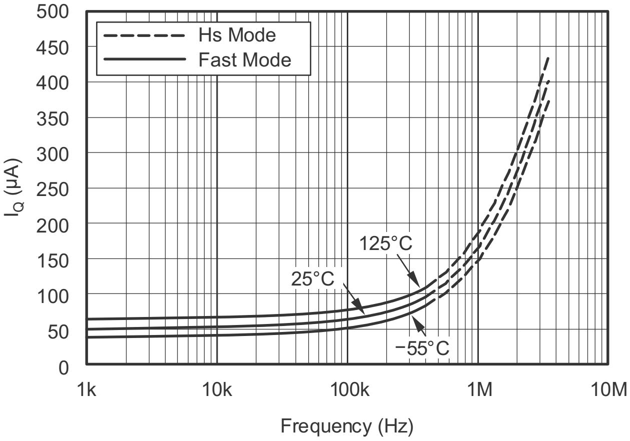


Figure 5. Quiescent Current with Bus Activity vs Temperature

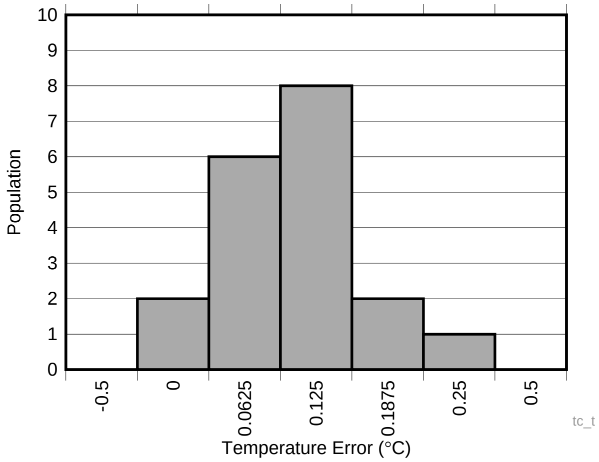


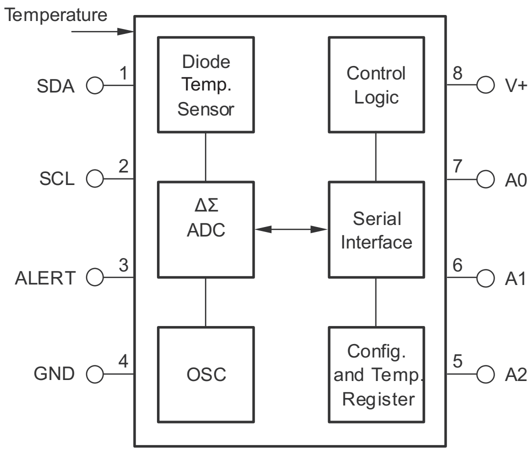
Figure 6. Temperature Error at 25°C

7 Detailed Description

7.1 Overview

The TMP275-Q1 is a digital temperature sensor that is optimal for thermal management and thermal protection applications. The TMP275-Q1 is two-wire, SMBus, and I^{2}C interface compatible, and is specified over the temperature range of –40°C to +125°C. The temperature sensor in the TMP275-Q1 is the device itself. Thermal paths run through the package leads as well as the plastic package. The package leads provide the primary thermal path because of the lower thermal resistance of the metal; see the *Functional Block Diagram* section for the internal block diagram of the TMP275-Q1 device.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital Temperature Output

The temperature register of the TMP275-Q1 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Table 5 and Table 6. Note that byte 1 is the most significant byte and is followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. The data format for temperature is summarized in Table 1. Following power-up or reset, the Temperature register reads 0°C until the first conversion is complete. The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits (MSBs) in the Temperature register are used with the unused least significant bits (LSBs) set to zero.

Table 1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

7.3.2 Serial Interface

The TMP275-Q1 operates only as a slave device on the SMBus, two-wire, and I^2C interface-compatible bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP275-Q1 supports the transmission protocol for fast (up to 400 kHz) and high-speed (up to 2.38 MHz) modes. All data bytes are transmitted most significant bit (MSB) first.

7.3.3 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device a START condition is initiated, indicated by pulling the data line (SDA) from a high to a low logic level when SCL is high. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer, SDA must remain stable when SCL is high because any change in SDA when SCL is high is interpreted as a control signal.

When all data are transferred, the master generates a STOP condition indicated by pulling SDA from low to high when SCL is high.

7.3.4 Serial Bus Address

To communicate with the TMP275-Q1, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation.

The TMP275-Q1 features three address pins, allowing up to eight devices to be connected per bus. Pin logic levels are described in Table 2. The address pins of the TMP275-Q1 are read after reset, at the start of communication, or in response to a two-wire address acquire request. Following reading the state of the pins, the address is latched to minimize power dissipation associated with detection.

Table 2. Address Pins and Slave Addresses for the TMP275-Q1

A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111

7.3.4.1 Writing and Reading to the TMP275-Q1

Accessing a particular register on the TMP275-Q1 is accomplished by writing the appropriate value to the Pointer register. The value for the Pointer register is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the TMP275-Q1 requires a value for the Pointer register; see Figure 8.

When reading from the TMP275-Q1, the last value stored in the Pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer register. This action is accomplished by issuing a slave address byte with the R/W bit low, followed by the Pointer register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/W bit high to initiate the read command; see Figure 9 for details of this sequence. If repeated reads from the same register are desired, the Pointer register bytes do not have to be continually sent because the TMP275-Q1 remembers the Pointer register value until it is changed by the next write operation.

Note that register bytes are sent most-significant byte first, followed by the least significant byte.

7.3.4.2 Slave Mode Operations

The TMP275-Q1 can operate as a slave receiver or slave transmitter.

7.3.4.2.1 Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit low. The TMP275-Q1 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer register. The TMP275-Q1 then acknowledges reception of the Pointer register byte. The next byte or bytes are written to the register addressed by the Pointer register. The TMP275-Q1 acknowledges reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

7.3.4.2.2 Slave Transmitter Mode

The first byte is transmitted by the master and is the slave address, with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a Not-Acknowledge bit on reception of any data byte, or by generating a START or STOP condition.

7.3.4.3 SMBus Alert Function

The TMP275-Q1 supports the SMBus alert function. When the TMP275-Q1 is operating in interrupt mode (TM = 1), the ALERT pin of the TMP275-Q1 can be connected as an SMBus alert signal. When a master senses that an Alert condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP275-Q1 is active, the device acknowledges the SMBus Alert command and responds by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the Alert condition. This bit is high if the temperature is greater than or equal to T_{HIGH}. This bit is low if the temperature is less than T_{LOW}; see Figure 10 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command determines which device clears its Alert status. If the TMP275-Q1 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP275-Q1 loses the arbitration, its ALERT pin remains active.

7.3.4.4 General Call

The TMP275-Q1 responds to a two-wire, general-call address (0000000) if the eighth bit is 0. The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 00000100, the TMP275-Q1 latches the status of its address pins but does not reset. If the second byte is 00000110, the TMP275-Q1 latches the status of its address pins and resets its internal registers to their power-up values.

7.3.4.5 High-Speed Mode

For the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP1275 device does not acknowledge this byte, but does switch its input filters on SDA and SCL and its output filters on SDA to operate in Hs-mode, thus allowing transfers at up to 2.38 MHz. After the Hs-mode master code is issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP275-Q1 switches the input and output filter back to fast-mode operation.

7.3.4.6 Time-Out Function

The TMP275-Q1 resets the serial interface if either SCL or SDA is held low for 54 ms (typical) between a START and STOP condition. The TMP275-Q1 releases the bus if it is pulled low and waits for a START condition. To avoid activating the time-out function, a communication speed of at least 1 kHz must be maintained for the SCL operating frequency.

7.3.5 Timing Diagrams

The TMP275-Q1 is two-wire, SMBus, and I^2C interface compatible. Figure 7 to Figure 10 describe the various operations on the TMP275-Q1. The following list provides bus definitions. Parameters for Figure 7 are defined in the *Timing Requirements* table.

Bus Idle: Both the SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line, from high to low when the SCL line is high defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a Not-Acknowledge bit on the last byte that is transmitted by the slave.

7.3.5.1 Two-Wire Timing Diagrams

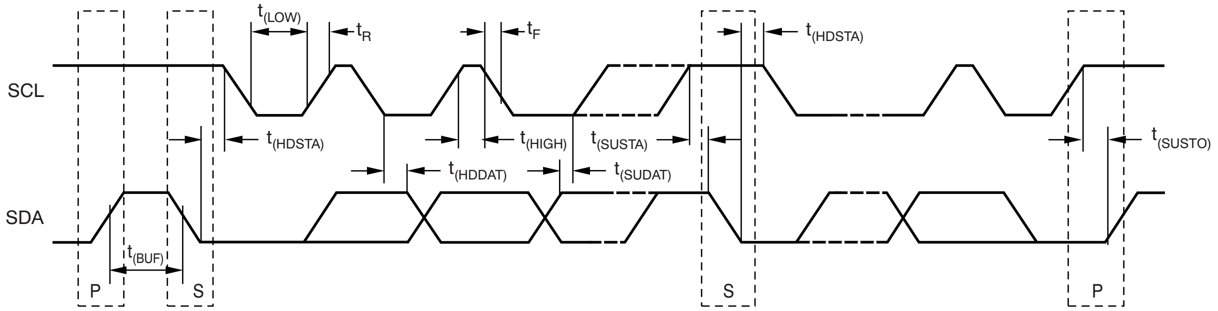


Figure 7. Two-Wire Timing Diagram

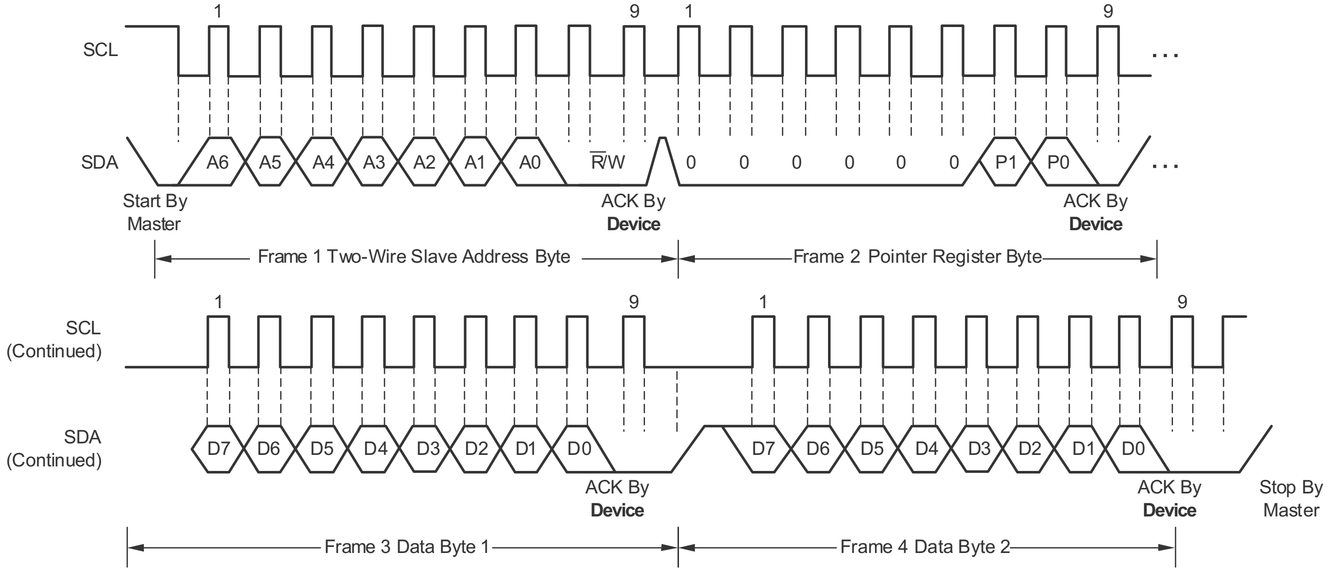
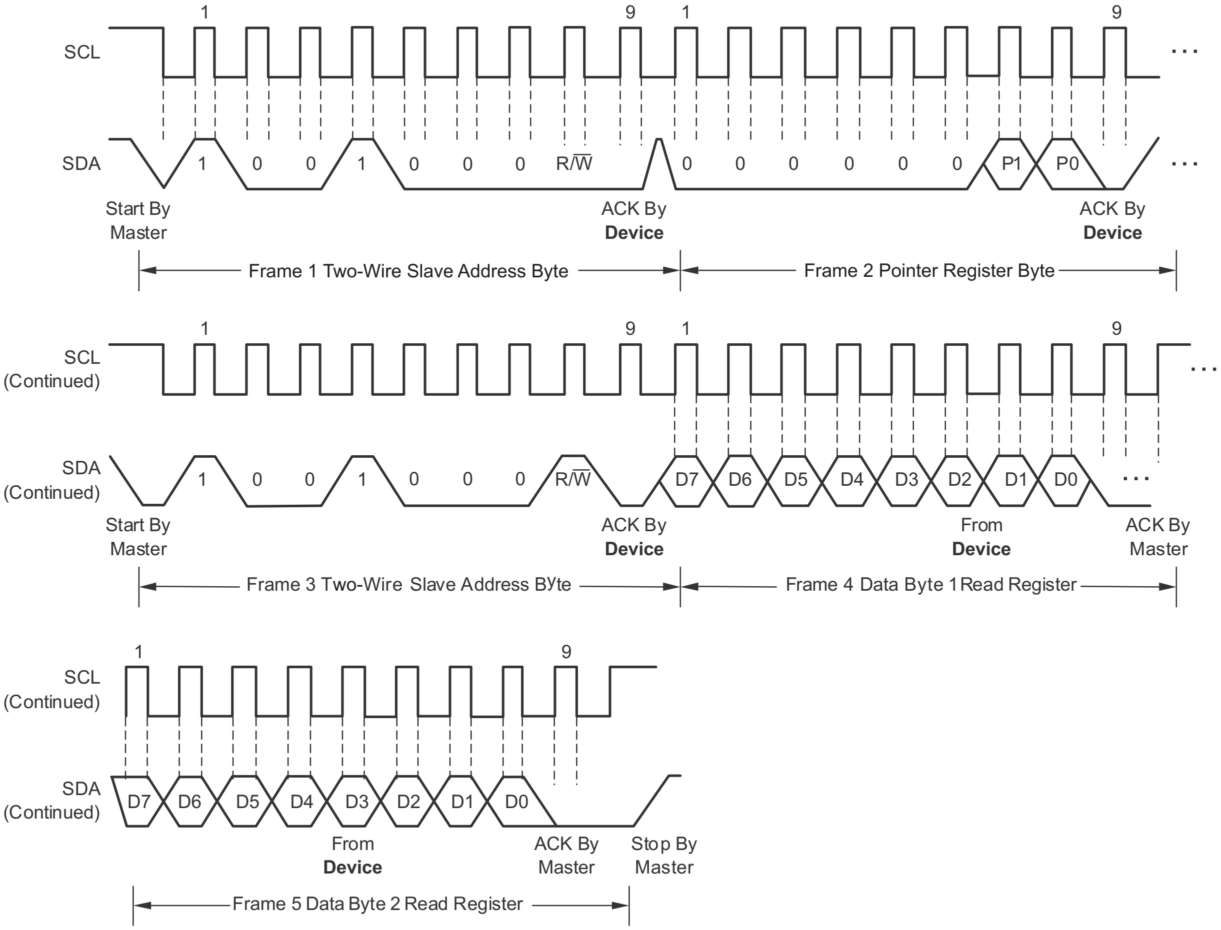
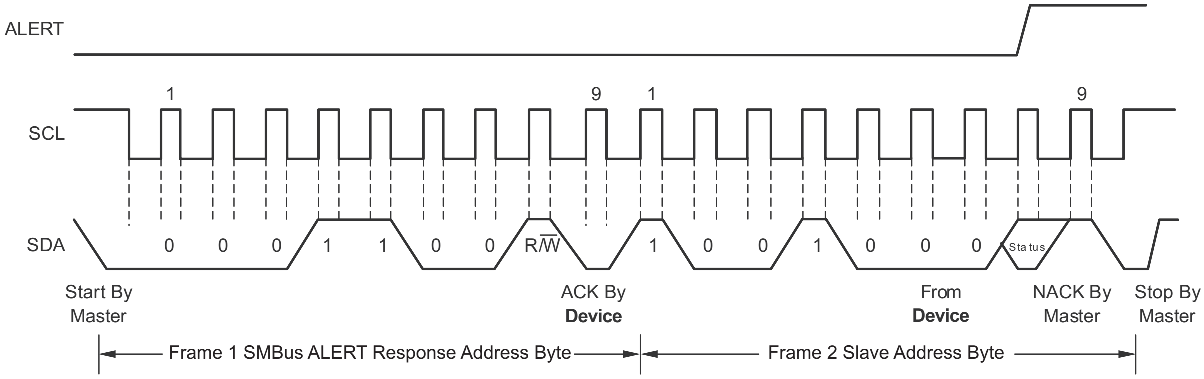


Figure 8. Two-Wire Timing Diagram for TMP275-Q1 Write Word Format



NOTE: Address pins A0, A1, and A2 = 0.

Figure 9. Two-Wire Timing Diagram for Read Word Format



NOTE: Address pins A0, A1, and A2 = 0.

Figure 10. Timing Diagram for SMBus ALERT

7.4 Device Functional Modes

7.4.1 Shutdown Mode (SD)

The shutdown mode of the TMP275-Q1 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, thus reducing current consumption to typically less than 0.1 μA. Shutdown mode is enabled when the SD bit is 1; the device shuts down when the current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

7.4.2 Thermostat Mode (TM)

The thermostat mode bit of the TMP275-Q1 indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the *High- and Low-Limit Registers* section.

7.4.2.1 Comparator Mode (TM = 0)

In comparator mode (TM = 0), the ALERT pin is activated when the temperature equals or exceeds the value in the T_{HIGH} register and remains active until the temperature falls below the value in the T_{LOW} register. For more information on the comparator mode, see the *High- and Low-Limit Registers* section.

7.4.2.2 Interrupt Mode (TM = 1)

In interrupt mode (TM = 1), the ALERT pin is activated when the temperature exceeds T_{HIGH} or goes below the T_{LOW} register. The ALERT pin is cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the *High- and Low-Limit Registers* section.

7.4.3 One-Shot (OS)

The TMP275-Q1 features a one-shot temperature measurement mode. When the device is in shutdown mode, writing a 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful for reducing power consumption in the TMP275-Q1 when continuous temperature monitoring is not required. When the configuration register is read, OS always reads zero.

7.5 Programming

7.5.1 Pointer Register

Figure 11 shows the internal register structure of the TMP275-Q1. The 8-bit Pointer register of the device is used to address a given data register. The Pointer register uses the two LSBs to identify which of the data registers must respond to a read or write command. Table 3 identifies the bits of the Pointer register byte. Table 4 describes the pointer address of the registers available in the TMP275-Q1. The power-up reset value of P1/P0 is 00.

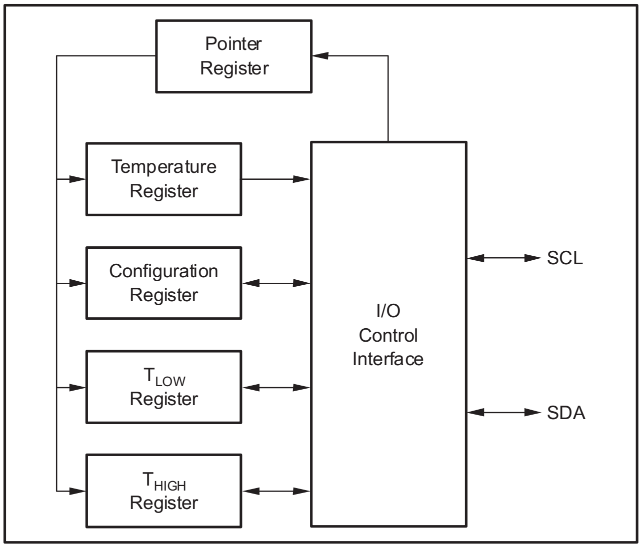


Figure 11. Internal Register Structure of the TMP275-Q1

Table 3. Pointer Register Byte (pointer = N/A) [reset = 00h]

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

Table 4. Pointer Addresses of the TMP275-Q1

P1	P0	TYPE	REGISTER
0	0	R only, default	Temperature register
0	1	R/W	Configuration register
1	0	R/W	T_{LOW} register
1	1	R/W	T_{HIGH} register

7.5.2 Temperature Register

The Temperature register of the TMP275-Q1 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data and are described in Table 5 and Table 6. Note that byte 1 is the most significant byte and is followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. The data format for temperature is summarized in Table 1. Following power-up or reset, the Temperature register reads 0°C until the first conversion is complete.

Table 5. Byte 1 of the Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

Table 6. Byte 2 of the Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

7.5.3 Configuration Register

The Configuration register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. The format of the Configuration register for the TMP275-Q1 is shown in Table 7, followed by a breakdown of the register bits. The power-up or reset value of the Configuration register is all bits equal to 0.

Table 7. Configuration Register Format

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD

7.5.4 Polarity (POL)

The Polarity bit of the TMP275-Q1 allows the user to adjust the polarity of the ALERT pin output. If POL = 0, the ALERT pin is active low, as shown in Figure 12. For POL = 1, the ALERT pin is active high and the state of the ALERT pin is inverted.

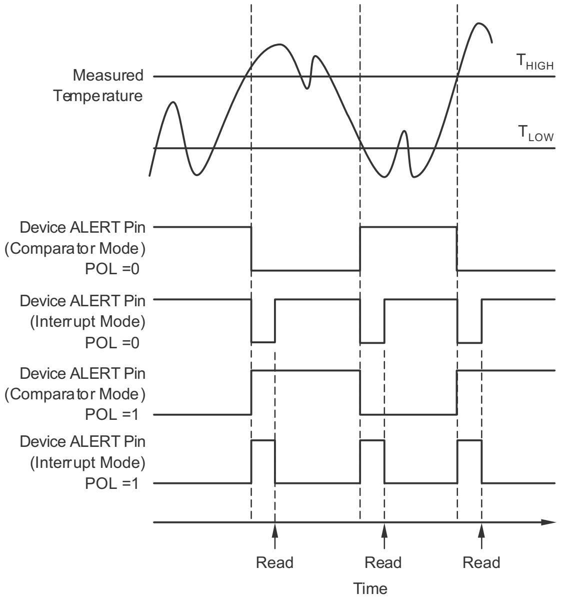


Figure 12. Output Transfer Function Diagrams

7.5.5 Fault Queue (F1/F0)

A fault condition is defined as when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} registers. Additionally, the number of fault conditions required to generate an alert can be programmed using the fault queue. The fault queue is provided to prevent a false alert resulting from environmental noise. The fault queue requires consecutive fault measurements to trigger the Alert function. Table 8 defines the number of measured faults that can be programmed to trigger an Alert condition in the device. For the T_{HIGH} and T_{LOW} register format and byte order, see the *High- and Low-Limit Registers* section.

Table 8. Fault Settings

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

7.5.6 Converter Resolution (R1/R0)

The converter resolution bits control the resolution of the internal analog-to-digital converter (ADC). This control allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table 9 identifies the resolution bits and the relationship between resolution and conversion time.

Table 9. Resolution of the TMP275-Q1

R1	R0	RESOLUTION	CONVERSION TIME (Typical)
0	0	9 bits (0.5°C)	27.5 ms
0	1	10 bits (0.25°C)	55 ms
1	0	11 bits (0.125°C)	110 ms
1	1	12 bits (0.0625°C)	220 ms

7.5.7 High- and Low-Limit Registers

In comparator mode (TM = 0), the ALERT pin of the TMP275-Q1 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus alert response address. The ALERT pin is also cleared if the device is placed in shutdown mode. When cleared, the ALERT pin only becomes active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin becomes active and remains active until cleared by a read operation of any register or a successful response to the SMBus alert response address. When the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the General-Call Reset command. This action also clears the state of the internal registers in the device, returning the device to comparator mode (TM = 0).

Both operational modes are represented in Figure 12. Table 10, Table 11, Table 12, and Table 13 describe the format for the T_{HIGH} and T_{LOW} registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and $_{TLOW}$ are:

T_{HIGH} = 80°C and T_{LOW} = 75°C

The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature register.

Table 10. Byte 1 the T_{HIGH} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4

Table 11. Byte 2 of the T_{HIGH} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	H3	H2	H1	H0	0	0	0	0

Table 12. Byte 1 the T_{LOW} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4

Table 13. Byte 2 of the T_{LOW} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	L3	L2	L1	L0	0	0	0	0

All 12 bits for the Temperature, T_{HIGH}, and, T_{LOW} registers are used in the comparisons for the Alert function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the Alert output even if the converter is configured for 9-bit resolution.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP275-Q1 is a digital output temperature sensor with SMBus, two-wire, and I^{2}C compatible interfaces. The device features three address pins (A0, A1, A2), allowing up to eight devices to be connected per bus. The TMP275-Q1 requires no external components for operation except for pullup resistors on SCL, SDA, and ALERT, although a 0.1-µF bypass capacitor is recommended. The TMP275-Q1 measures the printed circuit board (PCB) temperature of where the device is mounted. The sensing device of the TMP275-Q1 is the device itself. Thermal paths run through the package leads as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path.

8.2 Typical Applications

8.2.1 Typical Connections of the TMP275-Q1

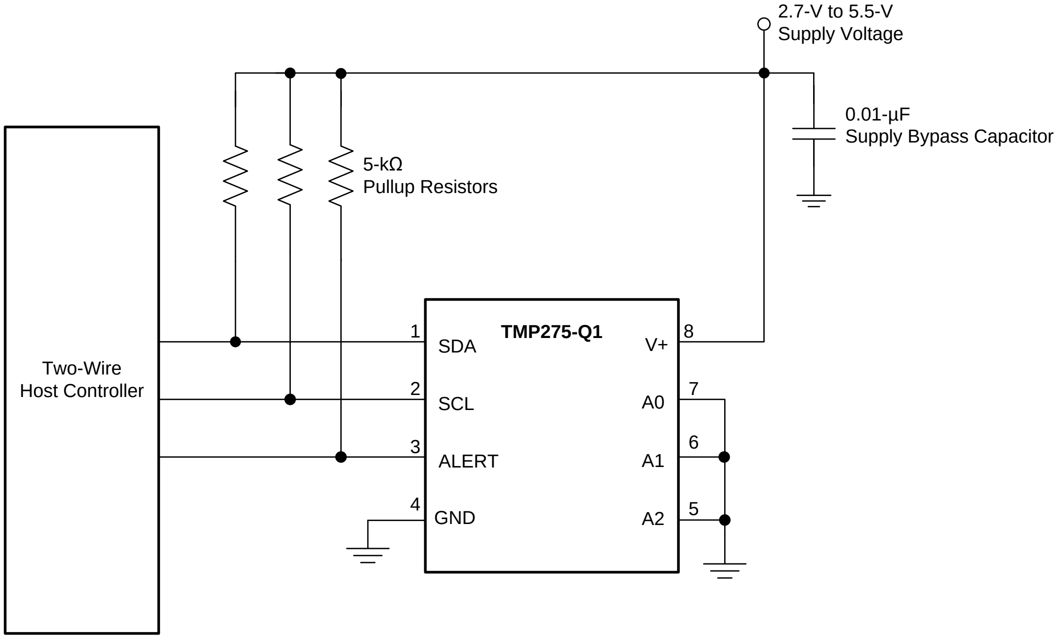


Figure 13. Typical Connections of the TMP275-Q1 Schematic

8.2.1.1 Design Requirements

Figure 13 shows the TMP275-Q1 typical connections. The TMP275-Q1 device requires pullup resistors on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistor is 5 kΩ. In some applications the pullup resistor can be lower or higher than 5 kΩ, but must not exceed 3 mA of current on the SCL and SDA pins and must not exceed 4 mA on the ALERT pin. If the resistors are missing, the SCL and SDA lines are always low (nearly 0 V) and the I^{2}C bus does not work. A 0.1-µF bypass capacitor is recommended, as shown in Figure 13. The SCL, SDA, and ALERT lines can be pulled up to a supply that is equal to or higher than V+ through the pullup resistors.

Typical Applications (continued)

The ALERT pin can be configured to respond to one of the two Alert functions available: *comparator mode* and *interrupt mode*. To configure one of eight different addresses on the bus, connect A0, A1, and A2 to either the GND or V+ pin. In the circuit shown in Figure 13, the comparator mode is selected and the address pins (A0, A1, A2) are connected to ground.

8.2.1.2 Detailed Design Procedure

Place the TMP275-Q1 device in close proximity to the heat source that must be monitored with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

8.2.1.3 Application Curve

Figure 14 shows the step response of the TMP275-Q1 device to a submersion in an oil bath of 100ºC from room temperature (27ºC). The time-constant, or the time for the output to reach 63% of the input step, is 1.5 s. The time-constant result depends on the PCB where the TMP275-Q1 devices are mounted. For this test, the TMP275-Q1 device was soldered to a two-layer PCB that measured 0.375 inches × 0.437 inches.

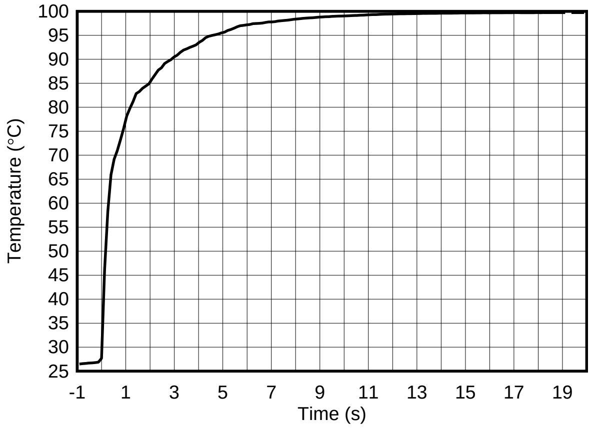


Figure 14. Temperature Step Response

Typical Applications (continued)

8.2.2 Connecting Multiple Devices on a Single Bus

The TMP275-Q1 features three address pins, allowing up to eight devices to be connected per bus. When the TMP275-Q1 is operating in interrupt mode (TM = 1) , the ALERT pin of the TMP275-Q1 can be connected as an SMBus Alert signal. Figure 15 shows eight TMP275-Q1 devices connected to an MCU (master) using one single bus. Each device that exists as a slave on the SMBus has one unique 7-bit address; see Table 2 for the TMP275-Q1 address options. When a master senses that an Alert condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP275-Q1 is active, the device acknowledges the SMBus Alert command and responds by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the temperature exceeding T_{HIGH} or falling below $_{TLOW}$ caused the ALERT condition. This bit is high if the temperature is greater than or equal to T_{HIGH}. This bit is low if the temperature is less than T_{LOW}.

This application has eight devices connected to the bus. If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command determines which device clears its ALERT status. If the TMP275-Q1 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP275-Q1 loses the arbitration, its ALERT pin remains active.

NOTE

Make sure you device is configured to operate in interrupt mode to enable the SMBus feature.

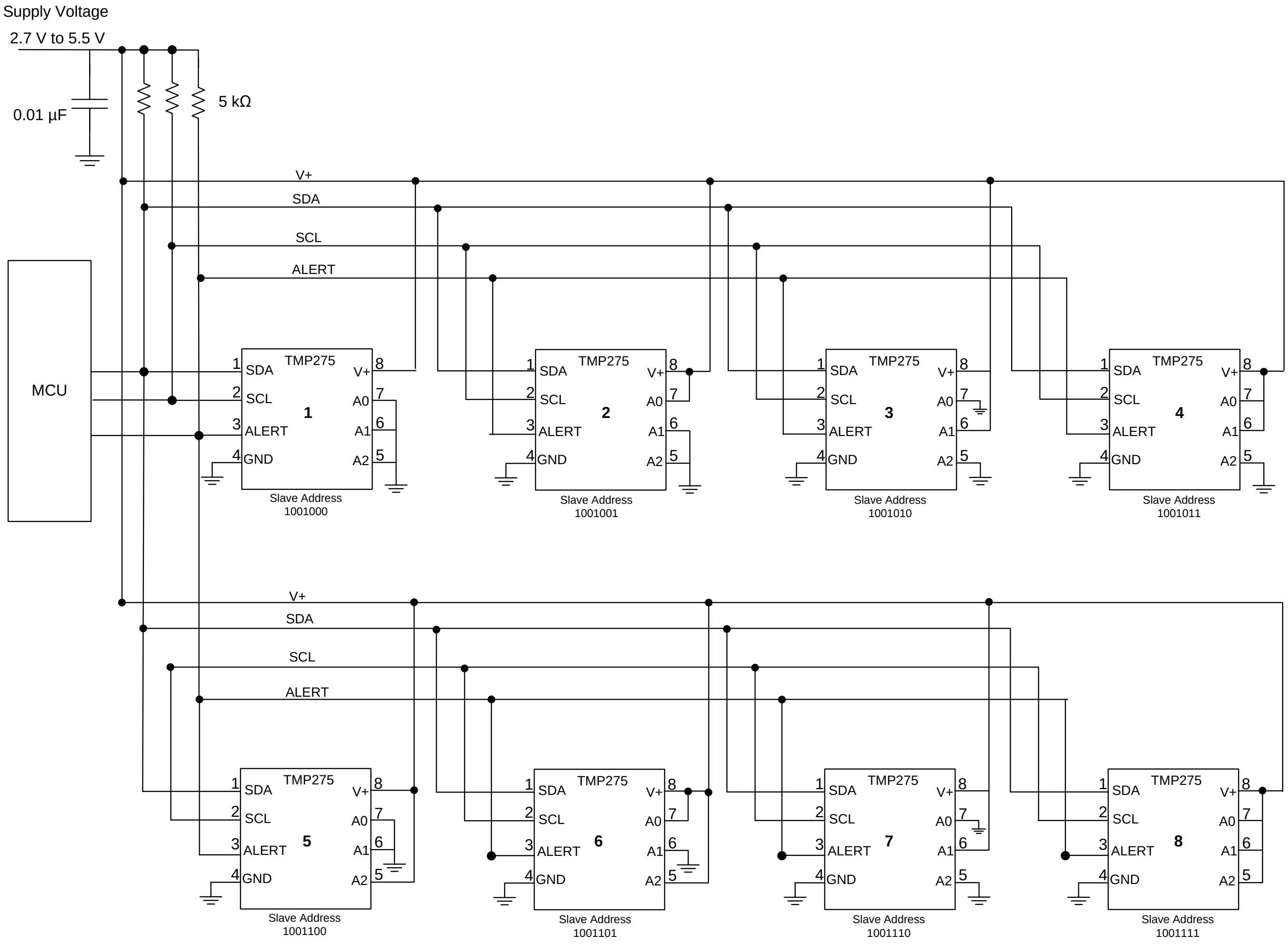


Figure 15. Connecting Multiple Devices on a Single Bus

Typical Applications (continued)

8.2.3 Temperature Data Logger for Cold Chain Management Applications

Cold chain management includes all of the means used to ensure a constant temperature for a product that is not heat stable from the time it is manufactured or farmed until the time it is used. This cold chain management includes industries such as food, retail, medical, and pharmaceutical. Figure 16 implements a cold chain monitoring system that measures temperature, then logs the sensor data to nonvolatile (FRAM) memory in the MCU. Figure 16 uses a near field communication (NFC) interface for wireless communication and is powered from a CR2032 coin cell battery with a focus on low power to maximize the battery lifetime.

The microcontroller communicates with all of the sensor devices through an I^2C compatible interface. The MCU also communicates with the NFC transponder through this interface. An NFC-enabled smartphone can be used to send configurations to the application board. For a detailed design procedure and requirements of this application, see *Ultralow Power Multi-sensor Data Logger with NFC Interface Reference Design*.

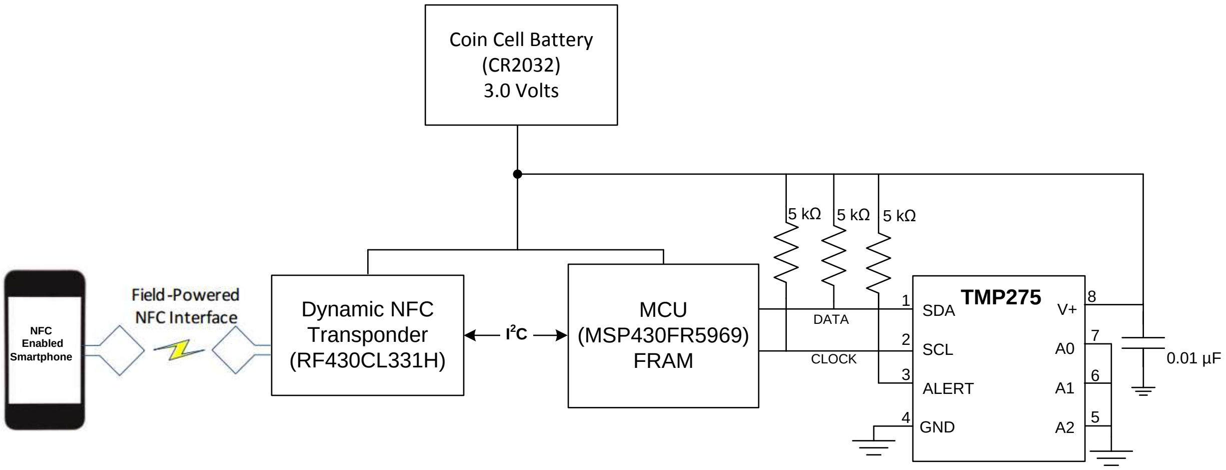


Figure 16. Temperature Data Logger

9 Power Supply Recommendations

The TMP275-Q1 device operates with power supplies in the range of 2.7 V to 5.5 V. A power-supply bypass capacitor is required for stability; place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 μF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

Mount the TMP275-Q1 to a PCB as shown in Figure 17. For this example the A0, A1, and A2 address pins are connected directly to ground. Connecting these pins to ground configures the device for slave address 1001000b.

- Bypass the V+ pin to ground with a low-ESR ceramic bypass capacitor. The typical recommended bypass capacitance is a 0.1-μF ceramic capacitor with a X5R or X7R dielectric. The optimum placement is closest to the V+ and GND pins of the device. Take care in minimizing the loop area formed by the bypass-capacitor connection, the V+ pin, and the GND pin of the device. Additional bypass capacitance can be added to compensate for noisy or high-impedance power supplies.
- Pull up the open-drain output pins SDA, SCL, and ALERT through 5-kΩ pullup resistors.

10.2 Layout Example

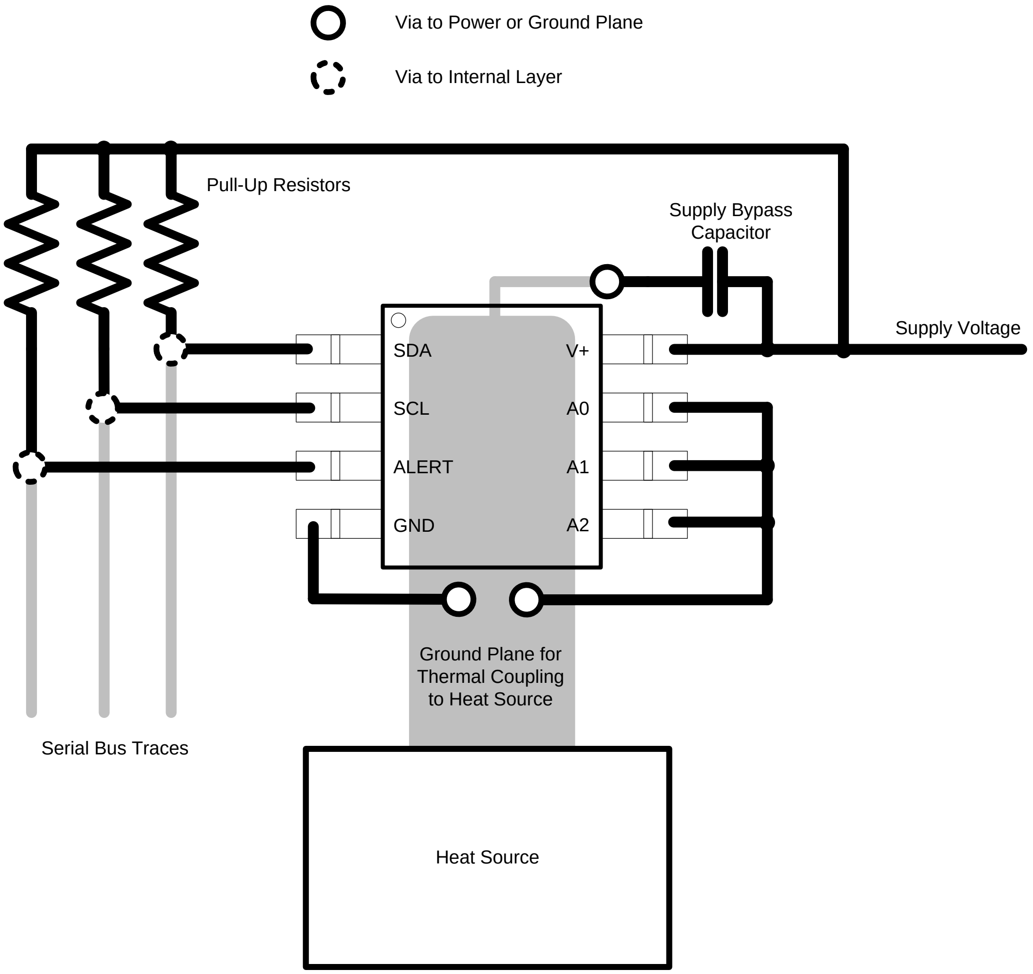


Figure 17. TMP275-Q1 Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 《LM75 数据表》
- 《TMP75、TMP175 数据表》
- 《TMP75B 数据表》
- *《具有 NFC 接口的超低功耗多传感器数据记录器参考设计》*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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设计支持	***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

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11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP275AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	275Q
TMP275AQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	275Q
TMP275AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T275Q1
TMP275AQDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T275Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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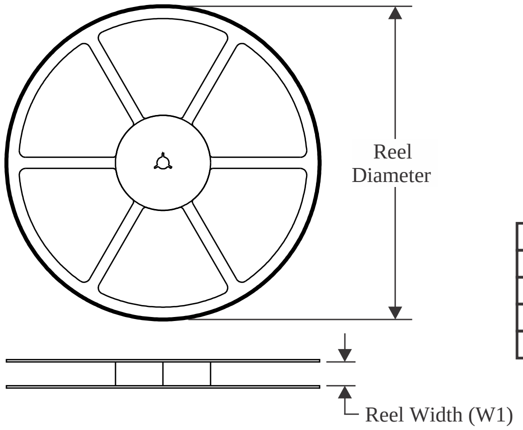
OTHER QUALIFIED VERSIONS OF TMP275-Q1 :

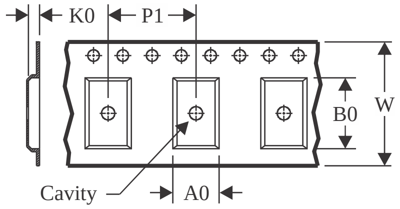
- Catalog : TMP275

NOTE: Qualified Version Definitions:

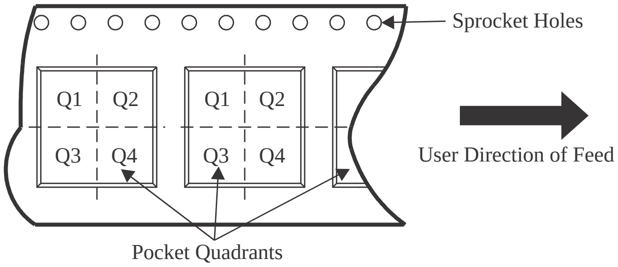
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


REEL DIMENSIONS


TAPE DIMENSIONS

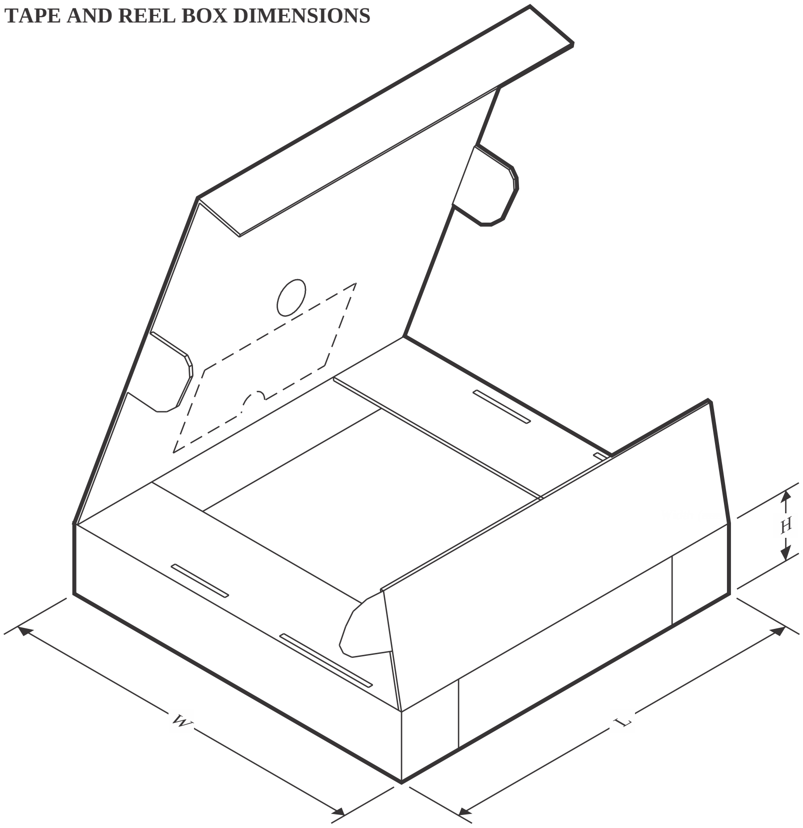
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

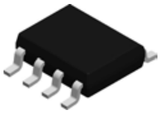
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP275AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP275AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP275AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP275AQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

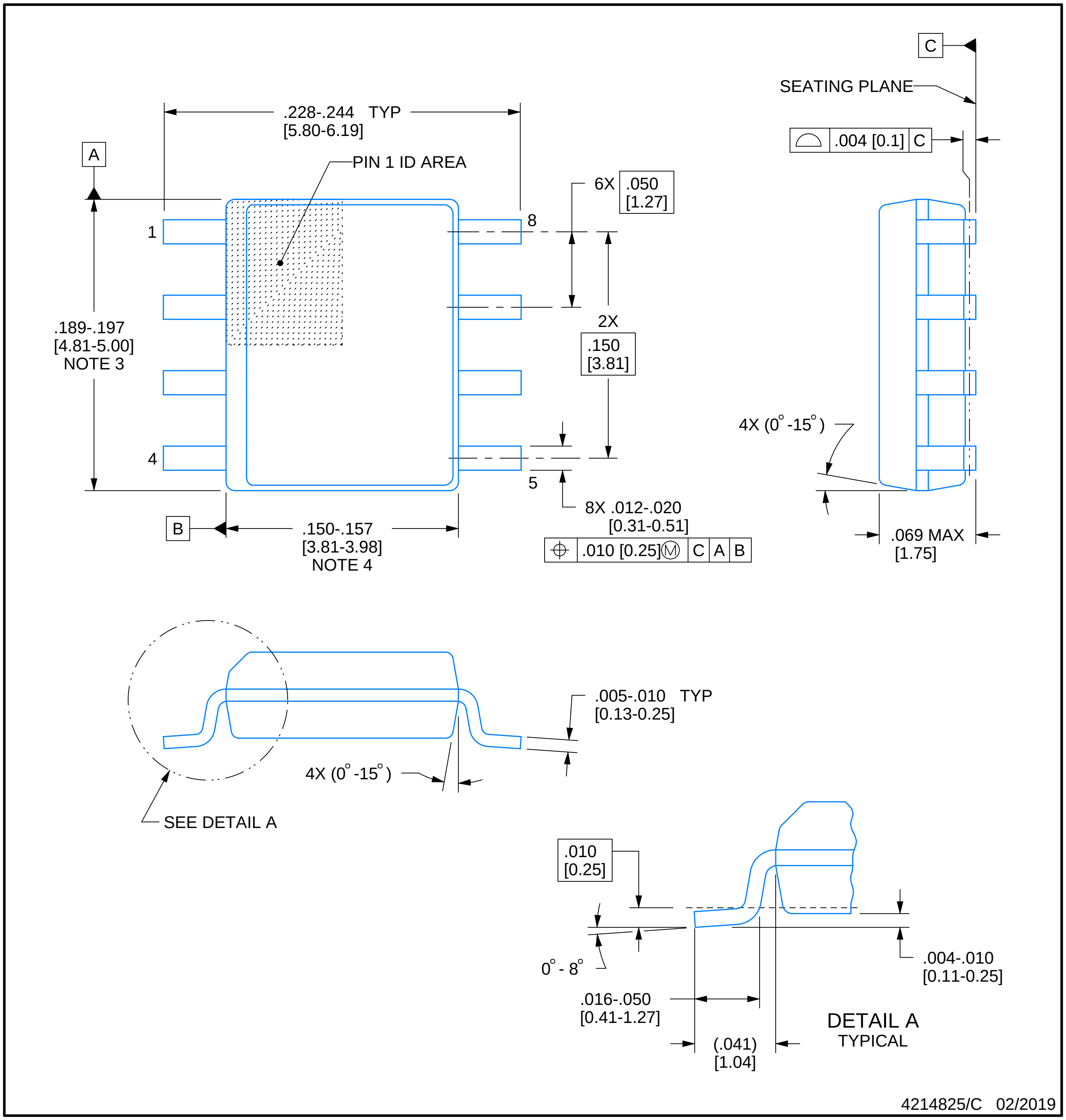


PACKAGE OUTLINE

D0008A

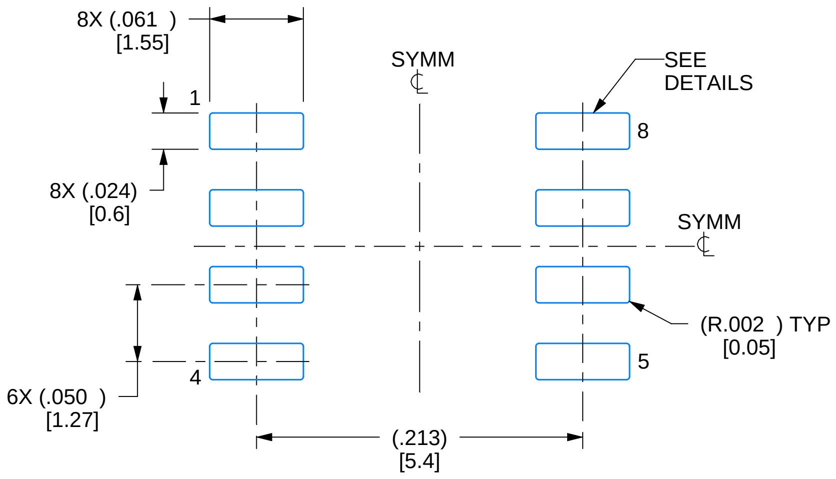
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

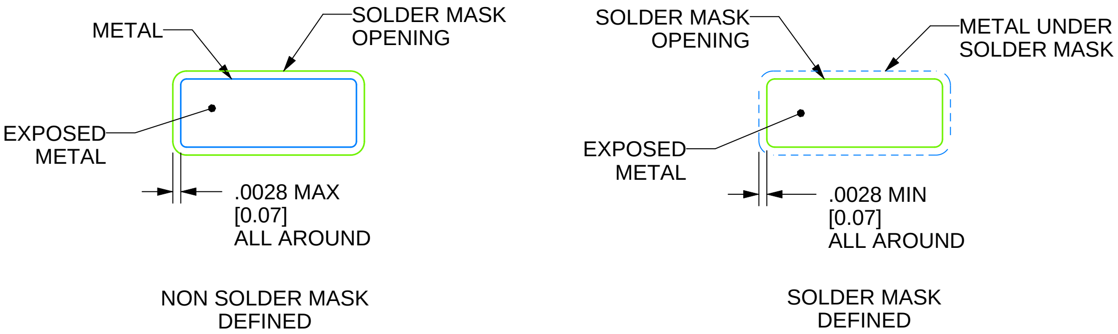


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

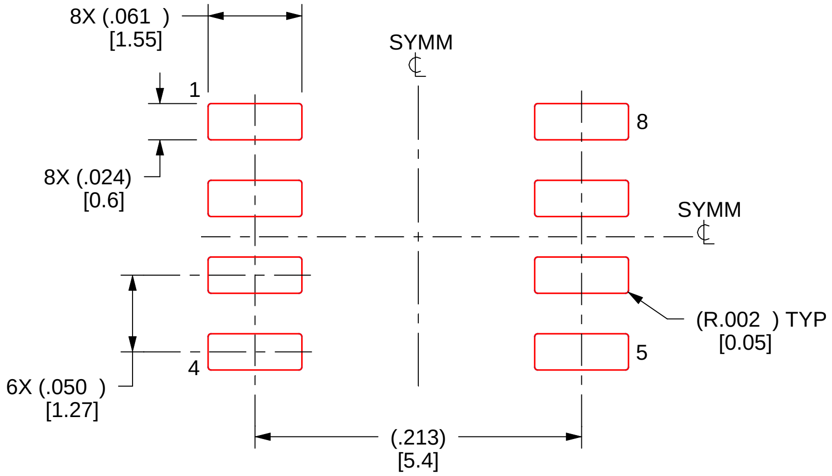


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

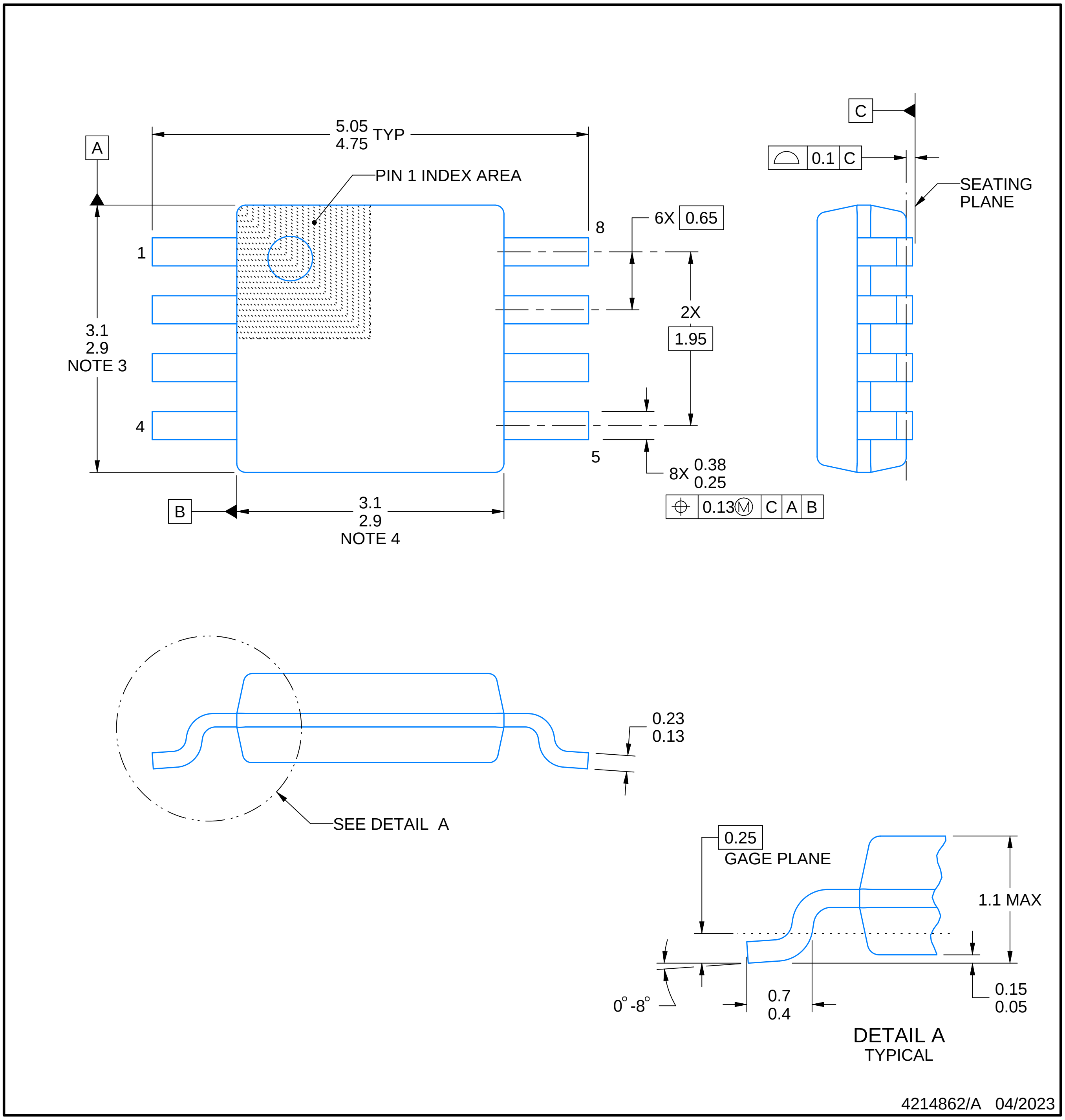


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

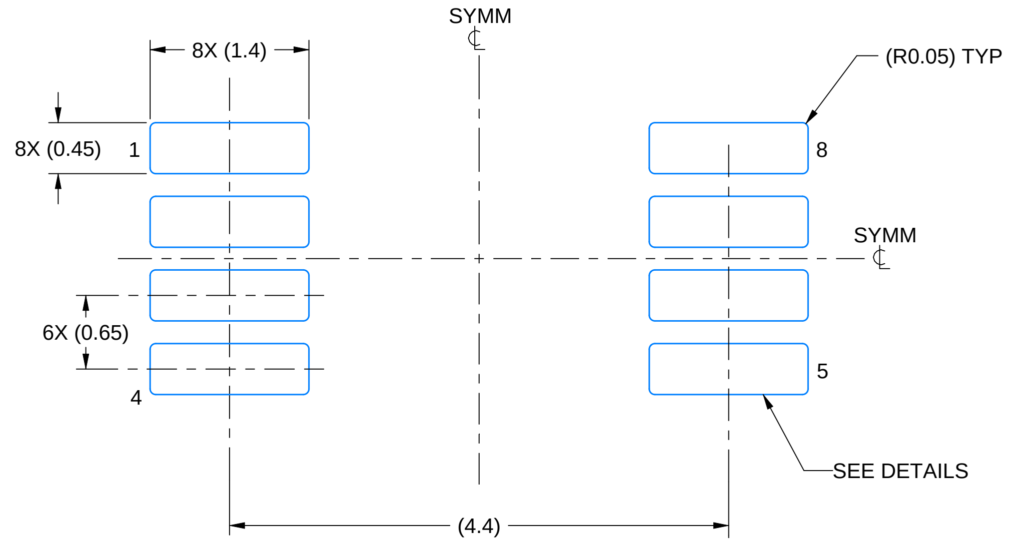


4214862/A 04/2023

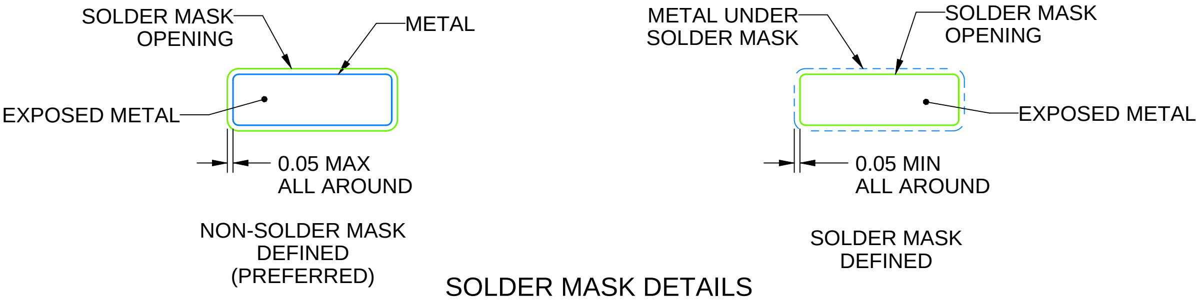
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

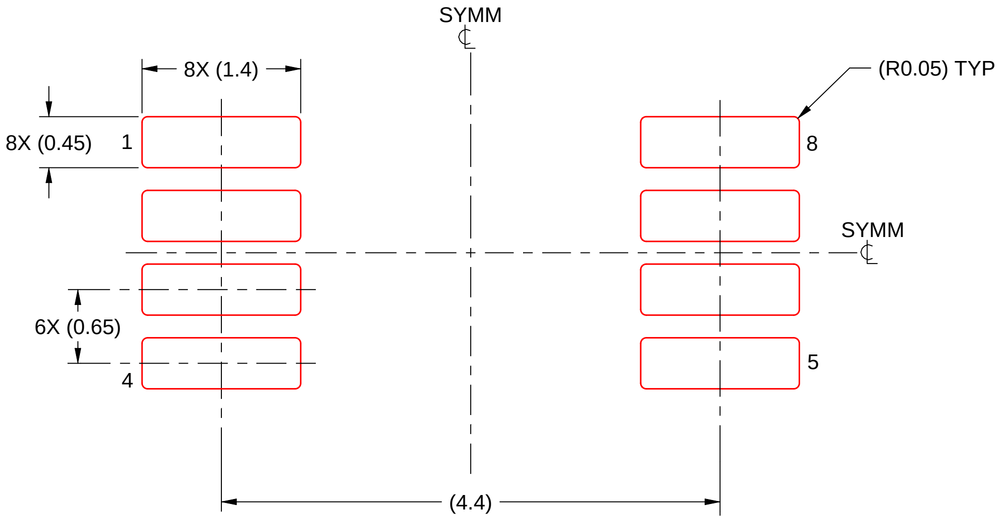


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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