TEXAS INSTRUMENTS
TLV9361-Q1, TLV9362-Q1, TLV9364-Q1
ZHCSRX5B – APRIL 2023 – REVISED AUGUST 2024

TLV936x-Q1 适用于成本敏感型系统的汽车级 10MHz、40V、轨至轨输出运算放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：-40°C 至 +125°C
  - 人体放电模型 (HBM) 静电放电 (ESD) 分级等级：2A
  - 充电器件模型 (CDM) ESD 分级等级：C6
- 低失调电压：±400µV
- 低失调电压漂移：±1.25µV/°C
- 低噪声：1kHz 时为 8.5nV/√Hz，6nV/√Hz 宽带
- 高共模抑制：110dB
- 低偏置电流：±10pA
- 轨到轨输出
- 高带宽：10.6MHz GBW，单位增益稳定
- 高压摆率：25V/µs
- 低静态电流：每个放大器 2.6mA
- 宽电源电压：±2.25V 至 ±20V，4.5V 至 40V
- 强大的 EMIRR 性能

2 应用

- 汽车音响主机
- 数字驾驶舱处理单元
- 远程信息处理控制单元
- 紧急呼叫 (eCall)
- 汽车有源噪声消除
- 汽车外部放大器

3 说明

TLV936x-Q1 系列（TLV9361-Q1、TLV9362-Q1 和 TLV9364-Q1）是一个符合 AEC-Q100 汽车标准的 40V 成本优化型运算放大器系列。

这些器件具有出色的直流和交流规格，包括轨至轨输出、低输入电压噪声密度 (6nV/√Hz)、低失调电压（典型值为 ±400µV）、低温漂（典型值为 ±1.25µV/°C）和 10.6MHz 带宽。

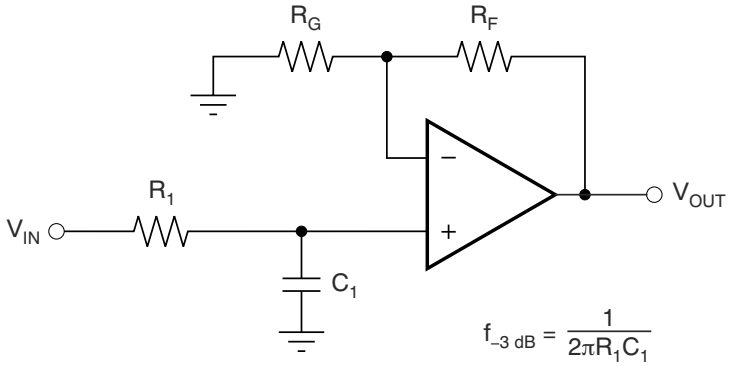
TLV936x-Q1 的特性（例如 EMIRR 滤波、大输出电流 (±60mA) 以及高压摆率 (25V/µs)）使其成为了一款可靠的运算放大器，适用于高电压成本敏感型应用。

TLV936x-Q1 系列运算放大器采用标准封装，额定工作温度范围为 -40°C 至 125°C。

封装信息

器件型号(1)	封装	封装尺寸(2)
TLV9361-Q1	DBV（SOT-23，5）	2.9mm × 2.8mm
	DCK（SC70，5）	2mm × 2.1mm
TLV9362-Q1	D（SOIC，8）	4.9mm × 6mm
	DGK（VSSOP，8）	3mm × 4.9mm
	PW（TSSOP，8）	3mm × 6.4mm
TLV9364-Q1	D（SOIC，14）	8.65mm × 6mm
	PW（TSSOP，14）	5mm × 6.4mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



TLV936x-Q1 应用于单极低通滤波器

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Table of Contents

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4 Pin Configuration and Functions

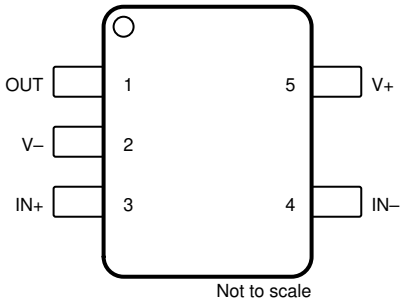

图 4-1. TLV9361-Q1 DBV Package
5-Pin SOT-23
(Top View)

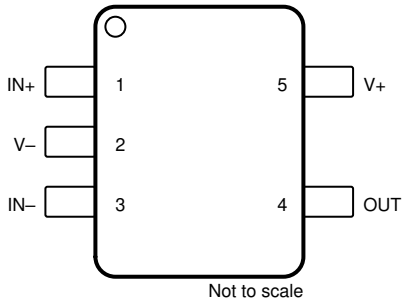

图 4-2. TLV9361-Q1 DCK Package
5-Pin SC70
(Top View)

表 4-1. Pin Functions: TLV9361-Q1

PIN			TYPE(1)	DESCRIPTION
NAME	SOT-23	SC70		
IN+	3	1	I	Non-inverting input
IN –	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V –	2	2	—	Negative (lowest) power supply

(1) I = input, O = output

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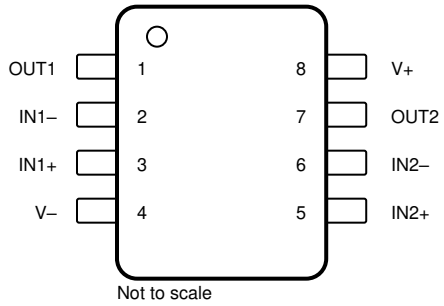

图 4-3. TLV9362-Q1 D, DGK, and PW Package 8-Pin SOIC, VSSOP, and TSSOP (Top View)

表 4-2. Pin Functions: TLV9362-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1+	3	I	Non-inverting input, channel 1
IN1 –	2	I	Inverting input, channel 1
IN2+	5	I	Non-inverting input, channel 2
IN2 –	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V –	4	—	Negative (lowest) power supply

(1) I = input, O = output

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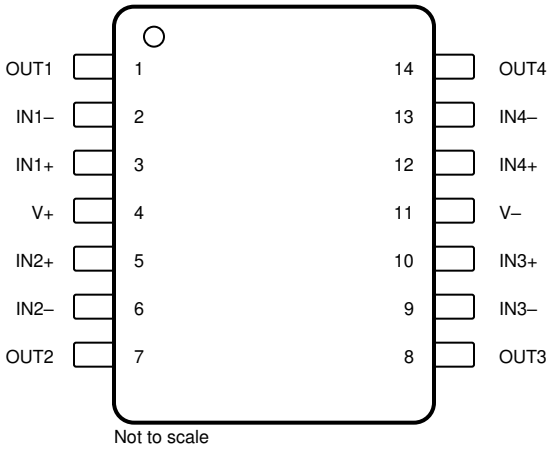

图 4-4. TLV9364-Q1 D and PW Package, SOIC and TSSOP (Top View)

表 4-3. Pin Functions: TLV9364-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1+	3	I	Non-inverting input, channel 1
IN1 –	2	I	Inverting input, channel 1
IN2+	5	I	Non-inverting input, channel 2
IN2 –	6	I	Inverting input, channel 2
IN3+	10	I	Non-inverting input, channel 3
IN3 –	9	I	Inverting input, channel 3
IN4+	12	I	Non-inverting input, channel 4
IN4 –	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V –	11	—	Negative (lowest) power supply

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	42	V
Signal input pins	Common-mode voltage(3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(3)		V_S + 0.2	V
	Current(3)	–10	10	mA
Output short-circuit(2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* causes permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, can affect device reliability and performance.
(2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
TLV9361-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	
TLV9362-Q1 and TLV9364-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	4.5	40	V
V_I	Common mode voltage range	(V–)	(V+) – 2	V
T_A	Specified temperature	–40	125	°C

5.4 Thermal Information for Single Channel

THERMAL METRIC(1)		TLV9361-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.3	202.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.8	111.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.9	51.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.6	25.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.5	51.4	°C/W

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THERMAL METRIC(1)		TLV9361-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Thermal Information for Dual Channel

THERMAL METRIC(1)		TLV9362-Q1			Unit
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130.8	173.9	159.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.0	65.7	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.3	95.6	98.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.8	10.9	9.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.5	94.1	96.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.6 Thermal Information for Quad Channel

THERMAL METRIC(1)		TLV9364-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.9	120.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.1	50.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.4	63.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.3	8.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.0	62.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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5.7 Electrical Characteristics

For V_S = (V+) – (V–) = 4.5 V to 40 V (±2.25 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.4	±1.7	mV
			T_A = –40°C to 125°C			±2	
dV_{OS}/dT	Input offset voltage drift	V_{CM} = V–	T_A = –40°C to 125°C		±1.25		µV/℃
PSRR	Input offset voltage versus power supply	V_{CM} = V–, V_S = 5 V to 40 V(1)	T_A = –40°C to 125°C		±1.5	±7.5	µV/V
	DC channel separation				1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		pA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			6		μV_{PP}
					1		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz			8.5		nV/√Hz
		f = 10 kHz			6		
i_N	Input current noise density	f = 1 kHz			100		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–)		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = 40 V, V– < V_{CM} < (V+) – 2 V	T_A = –40°C to 125°C	95	110		dB
		V_S = 5 V, V– < V_{CM} < (V+) – 2 V(1)		75	85		
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 9		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, V_{CM} = V_S / 2, (V–) + 0.1 V < V_O < (V+) – 0.1 V		115	130		dB
		V_S = 40 V, V_{CM} = V_S / 2, (V–) + 0.12 V < V_O < (V+) – 0.12 V	T_A = –40°C to 125°C		130		
		V_S = 5 V, V_{CM} = V_S / 2, (V–) + 0.1 V < V_O < (V+) – 0.1 V(1)		100	120		
			T_A = –40°C to 125°C		120		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				10.6		MHz
SR	Slew rate	V_S = 40 V, G = +1, V_{STEP} = 10 V, C_L = 20 pF(3)			25		V/µs
t_S	Settling time	To 0.1%, V_S = 40 V, V_{STEP} = 10 V, G = +1, C_L = 20 pF			0.65		µs
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V, G = +1, C_L = 20 pF			0.3		
		To 0.01%, V_S = 40 V, V_{STEP} = 10 V, G = +1, C_L = 20 pF			0.86		
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V, G = +1, C_L = 20 pF			0.44		
	Phase margin	G = +1, R_L = 10 kΩ, C_L = 20 pF			64		°
	Overload recovery time	V_{IN} × gain > V_S			170		ns

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For V_S = (V+) – (V –) = 4.5 V to 40 V (±2.25 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD+N	Total harmonic distortion + noise	V_S = 40 V, V_O = 3 V_{RMS}, G = 1, f = 1 kHz, R_L = 10 kΩ		0.0001%		
				120		dB
		V_S = 10 V, V_O = 3 V_{RMS}, G = 1, f = 1 kHz, R_L = 128 Ω		0.0056%		
				85		dB
		V_S = 10 V, V_O = 0.4 V_{RMS}, G = 1, f = 1 kHz, R_L = 32 Ω		0.00056%		
				105		dB

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For V_S = (V+) – (V–) = 4.5 V to 40 V (±2.25 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 40 V, R_L = no load		10		mV
			V_S = 40 V, R_L = 10 kΩ		60	100	
			V_S = 40 V, R_L = 2 kΩ		250	400	
I_{SC}	Short-circuit current				±60(2)		mA
C_{LOAD}	Capacitive Load Drive				See 图 5-28		pF
Z_O	Open-loop output impedance	I_O = 0 A			See 图 5-25		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			2.6	3	mA
			T_A = –40°C to 125°C			3.2	

(1) Specified by characterization only.
(2) At high supply voltage, placing the TLV936x in a sudden short to mid-supply or ground will lead to rapid thermal shutdown. Output current greater than I_{SC} can be achieved if rapid thermal shutdown is avoided as per 图 5-12.
(3) See 图 5-11 for more information.

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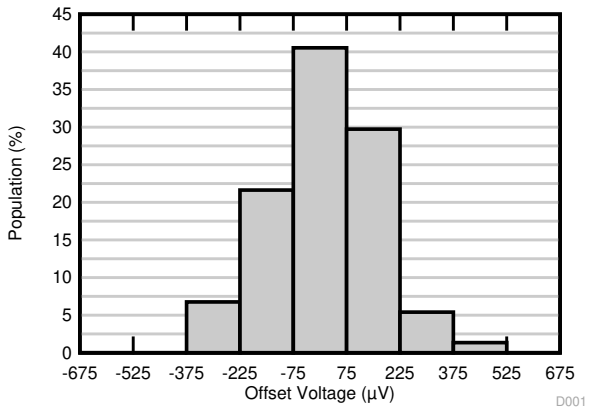
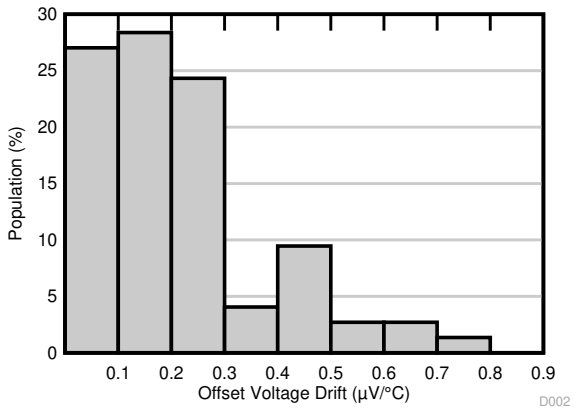
5.8 Typical Characteristics

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



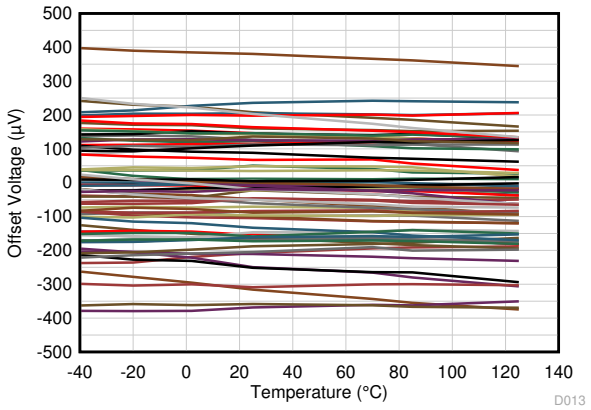
Distribution from 74 amplifiers, T_A = 25°C

图 5-1. Offset Voltage Production Distribution



Distribution from 74 amplifiers

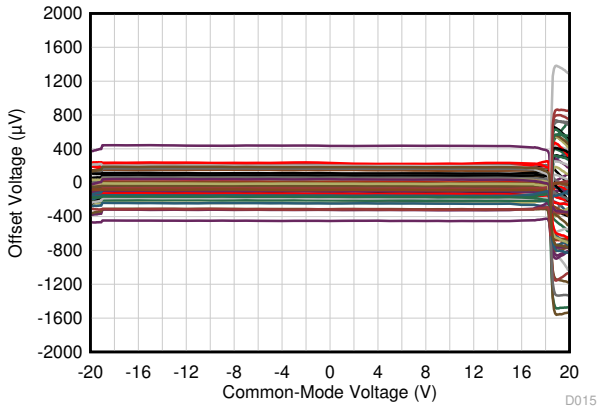
图 5-2. Offset Voltage Drift Distribution



V_{CM} = V-

Data from 74 amplifiers

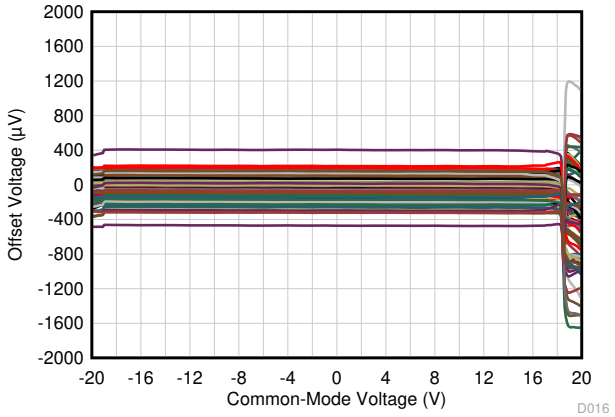
图 5-3. Offset Voltage vs Temperature



T_A = 25°C

Data from 74 amplifiers

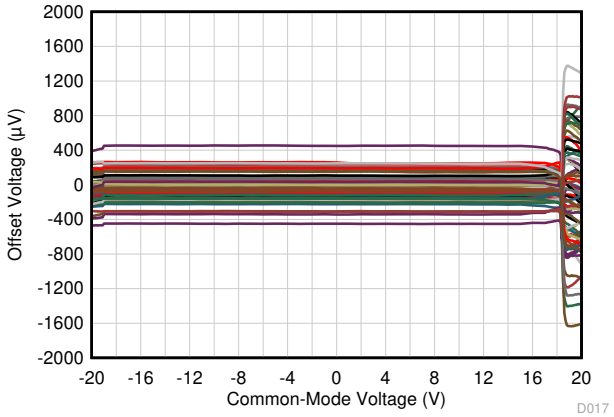
图 5-4. Offset Voltage vs Common-Mode Voltage



T_A = 125°C

Data from 74 amplifiers

图 5-5. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

Data from 74 amplifiers

图 5-6. Offset Voltage vs Common-Mode Voltage

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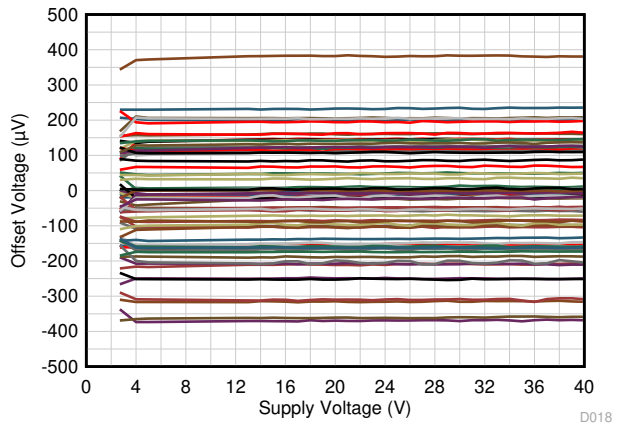
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



V_{CM} = V –
Data from 74 amplifiers

图 5-7. Offset Voltage vs Power Supply

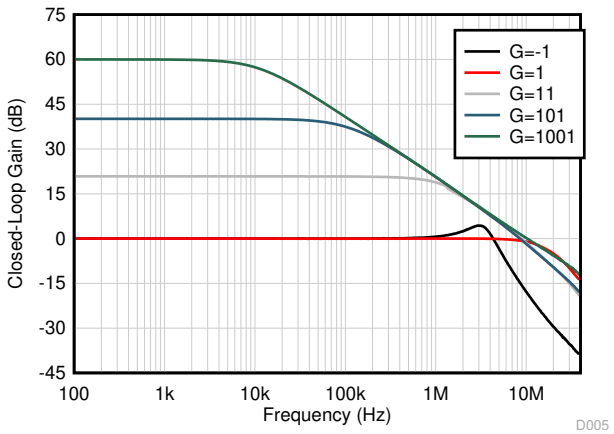


图 5-8. Closed-Loop Gain vs Frequency

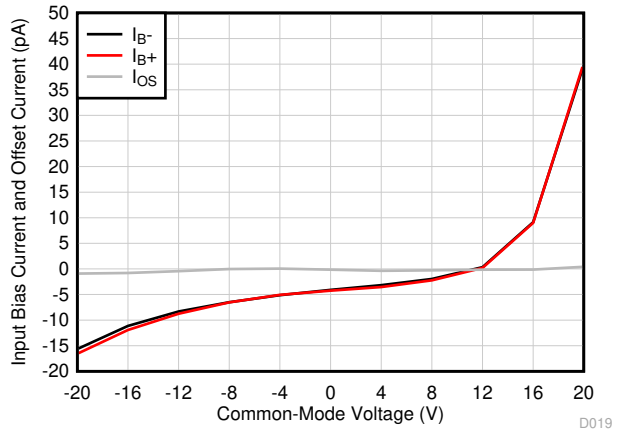


图 5-9. Input Bias Current and Offset Current vs Common-Mode Voltage

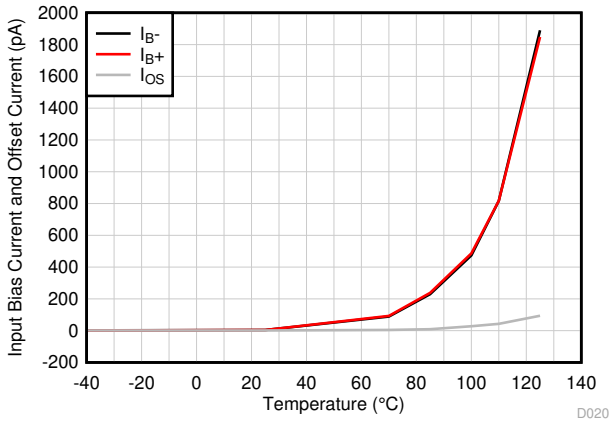


图 5-10. Input Bias Current and Offset Current vs Temperature

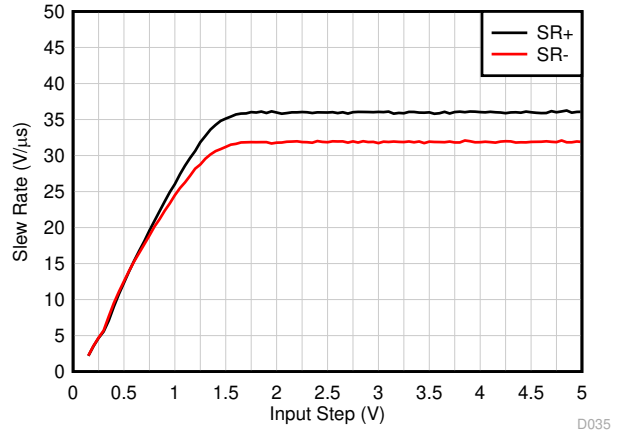
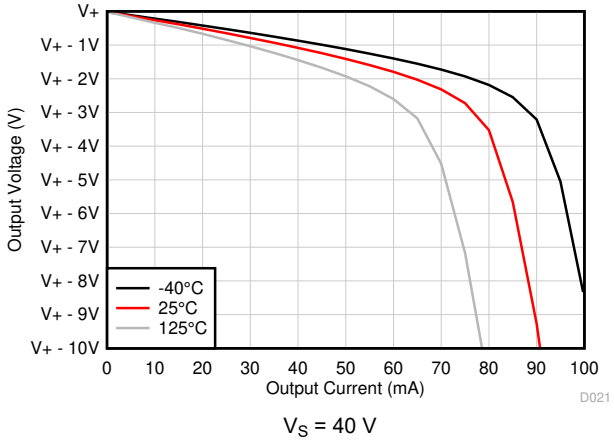


图 5-11. Slew Rate vs Input Step Voltage



V_S = 40 V

图 5-12. Output Voltage Swing vs Output Current (Sourcing)

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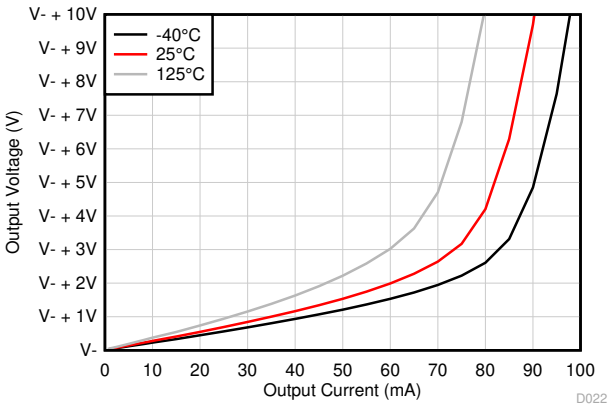
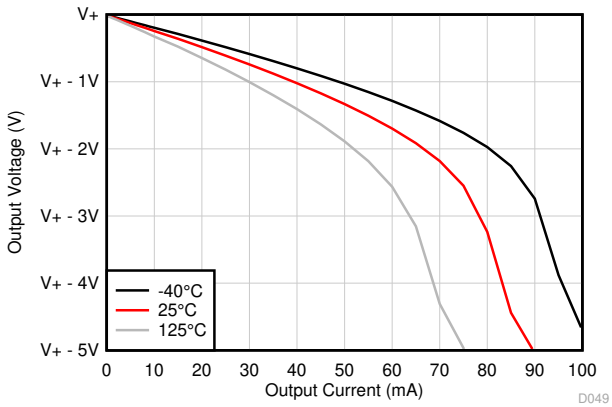
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



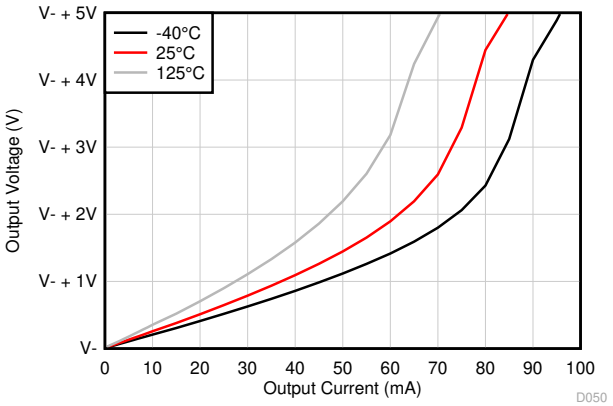
V_S = 40V

图 5-13. Output Voltage Swing vs Output Current (Sinking)



V_S = 5V

图 5-14. Output Voltage Swing vs Output Current (Sourcing)



V_S = 5V

图 5-15. Output Voltage Swing vs Output Current (Sinking)

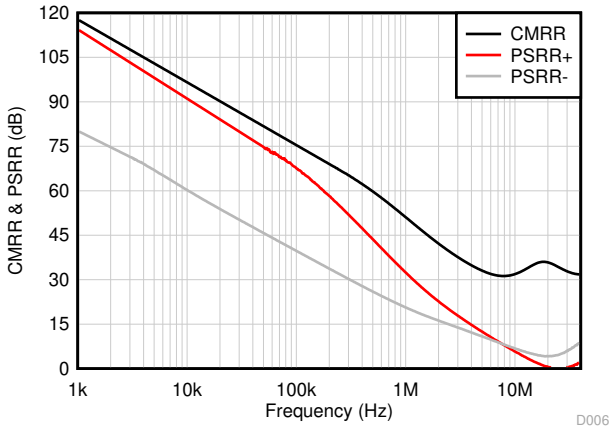
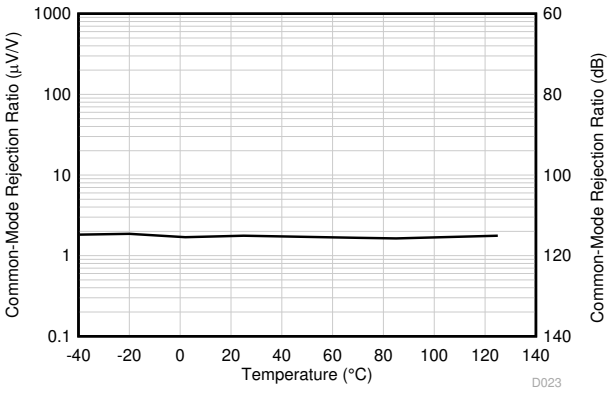
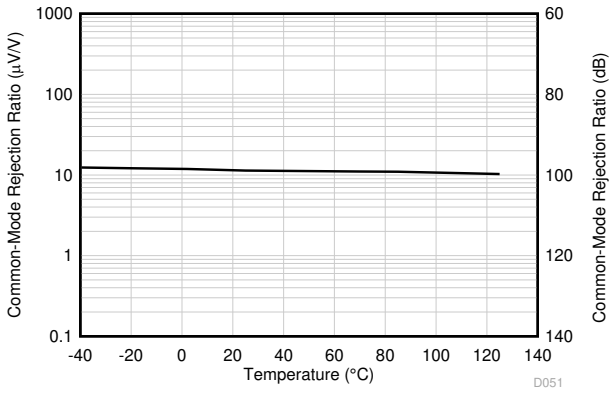


图 5-16. CMRR and PSRR vs Frequency



V_S = 40V

图 5-17. CMRR vs Temperature



V_S = 5V

图 5-18. CMRR vs Temperature

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

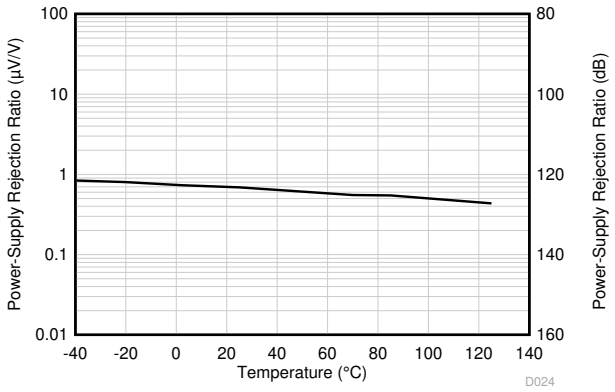


图 5-19. PSRR vs Temperature

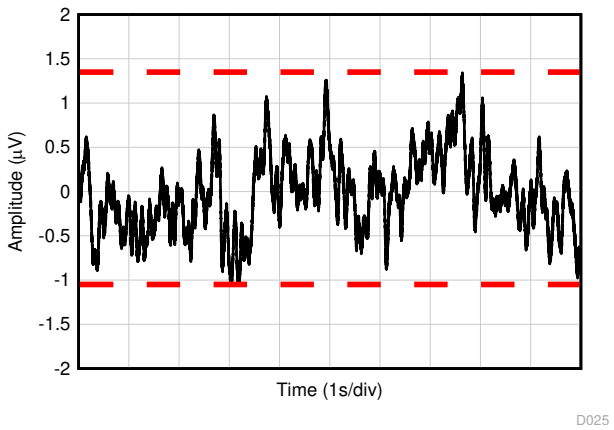


图 5-20. 0.1Hz to 10-Hz Noise

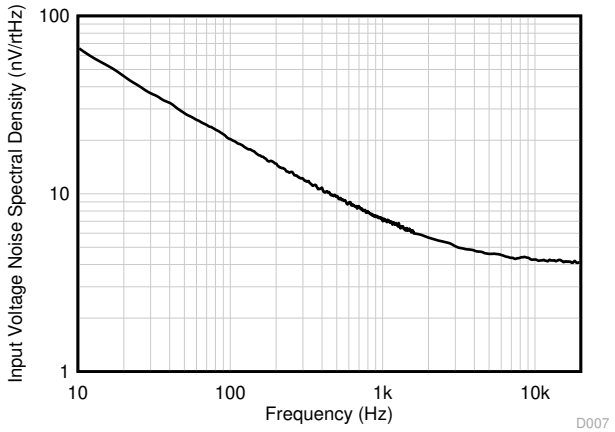
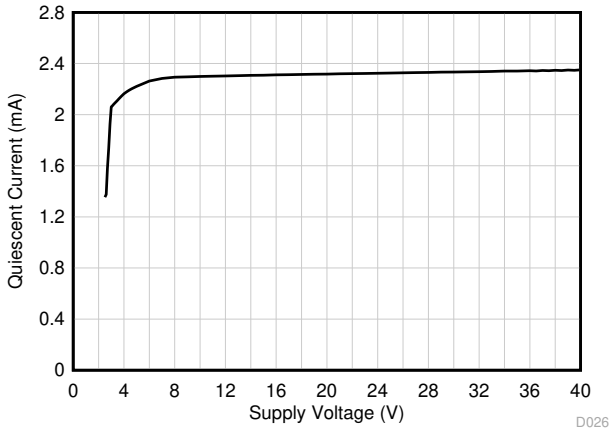
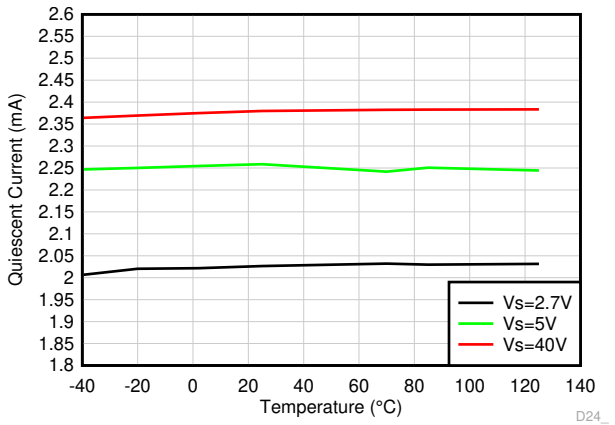


图 5-21. Input Voltage Noise Spectral Density vs Frequency



V_{CM} = V –

图 5-22. Quiescent Current vs Supply Voltage



V_{CM} = V –

图 5-23. Quiescent Current vs Temperature

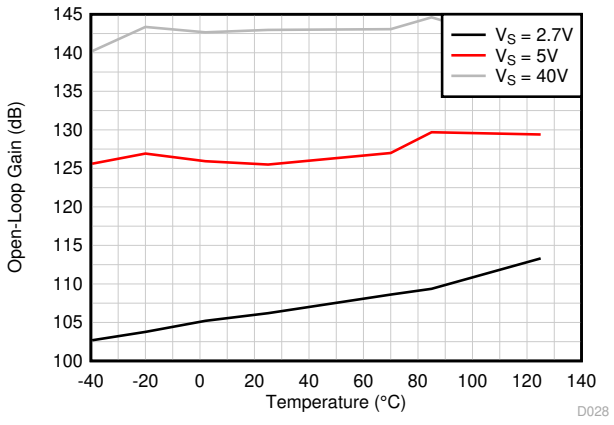


图 5-24. Open-Loop Voltage Gain vs Temperature (dB)

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

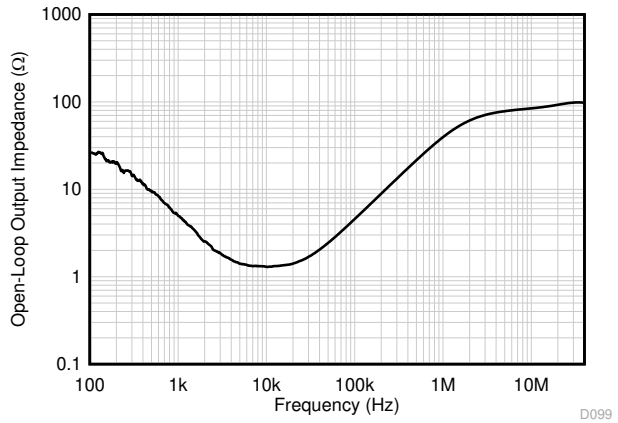
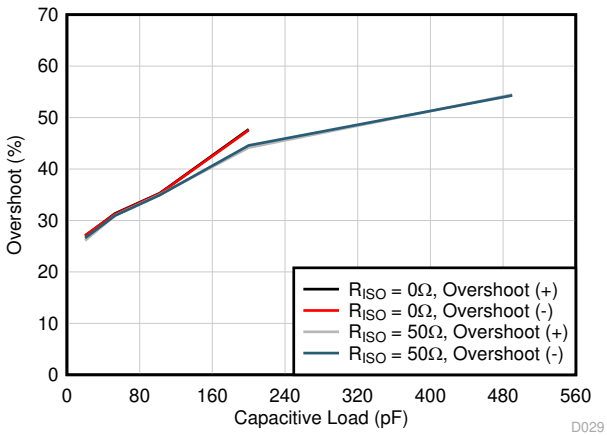
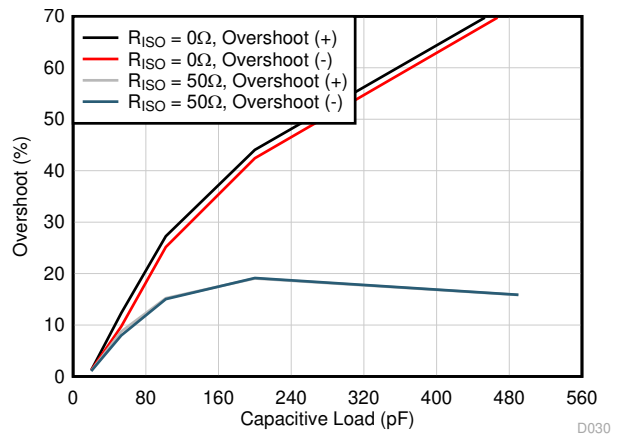


图 5-25. Open-Loop Output Impedance vs Frequency



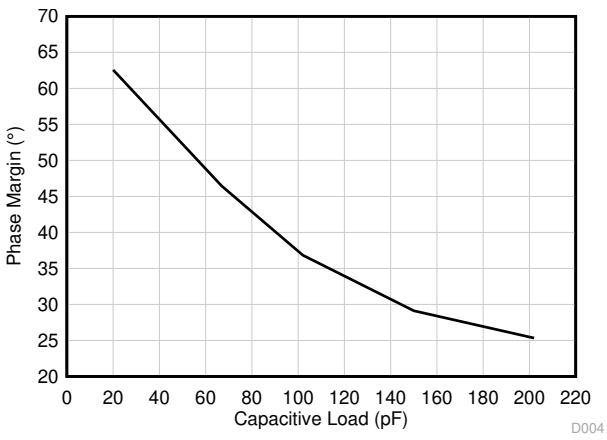
20mV$_{pp}$ Output Step, G = -1

图 5-26. Small-Signal Overshoot vs Capacitive Load



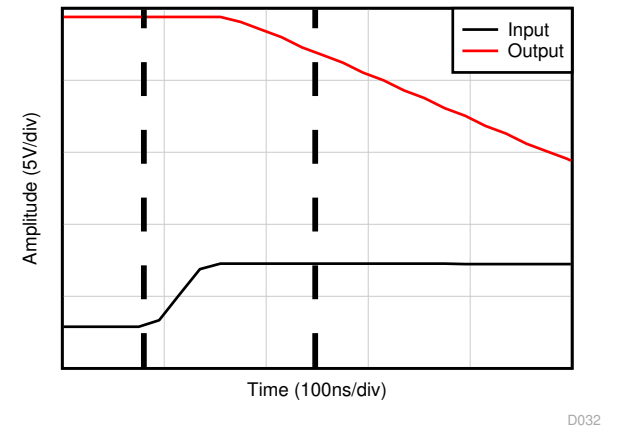
20mV$_{pp}$ Output Step, G = +1

图 5-27. Small-Signal Overshoot vs Capacitive Load



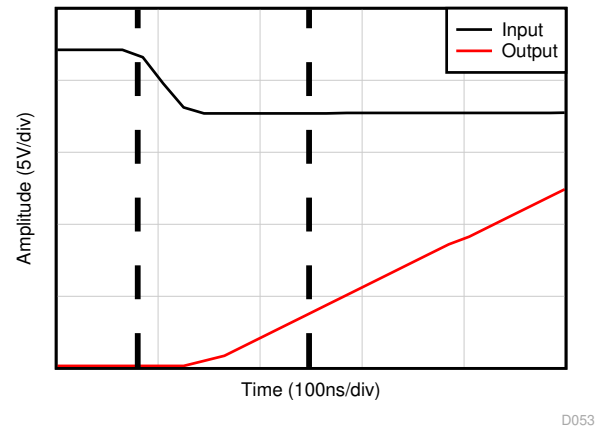
G = +1

图 5-28. Phase Margin vs Capacitive Load



G = –10

图 5-29. Positive Overload Recovery



G = –10

图 5-30. Negative Overload Recovery

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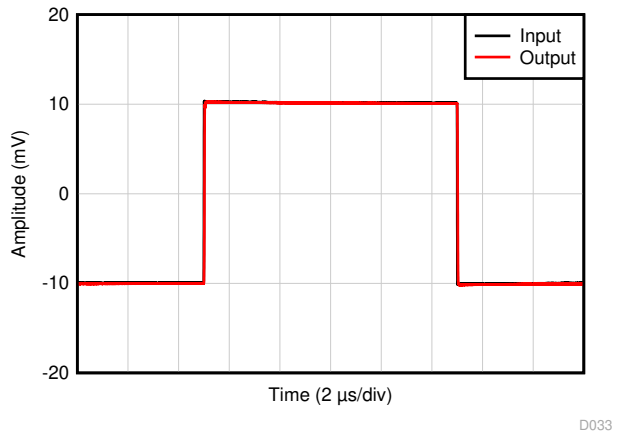
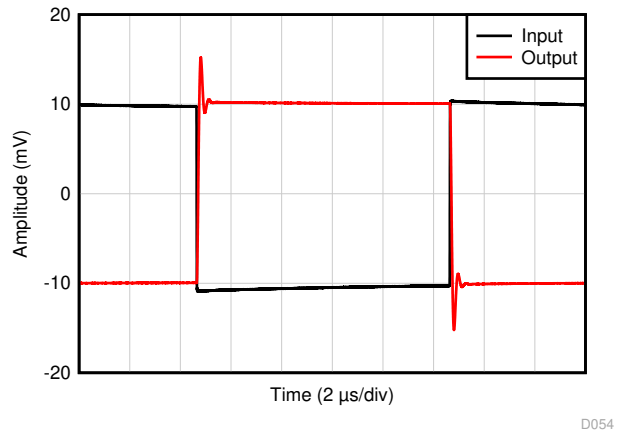
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



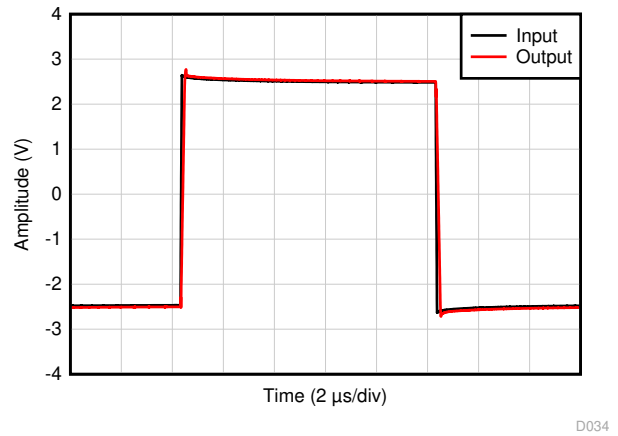
C_L = 20pF, G = 1, 20mV_{pp} step response

图 5-31. Small-Signal Step Response



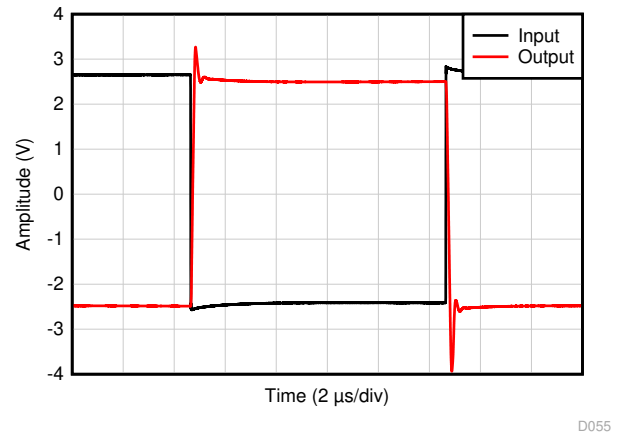
C_L = 20pF, G = -1, 20mV_{pp} step response

图 5-32. Small-Signal Step Response



C_L = 20pF, G = 1, 5V_{pp} step response

图 5-33. Large-Signal Step Response



C_L = 20pF, G = -1, 5V_{pp} step response

图 5-34. Large-Signal Step Response

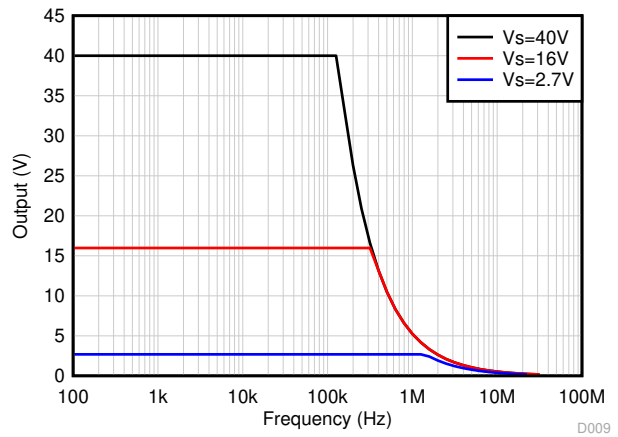


图 5-35. Maximum Output Voltage vs Frequency

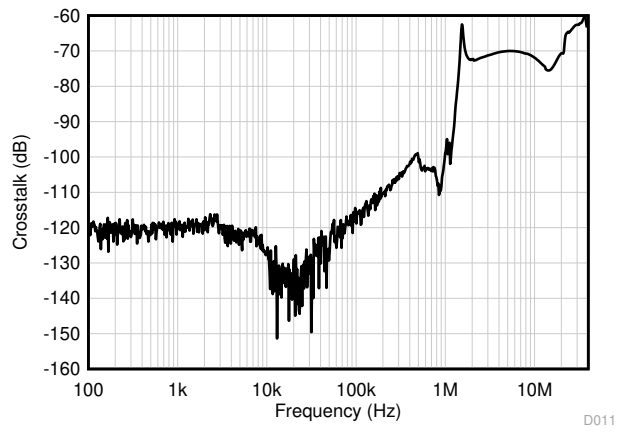


图 5-36. Channel Separation vs Frequency

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

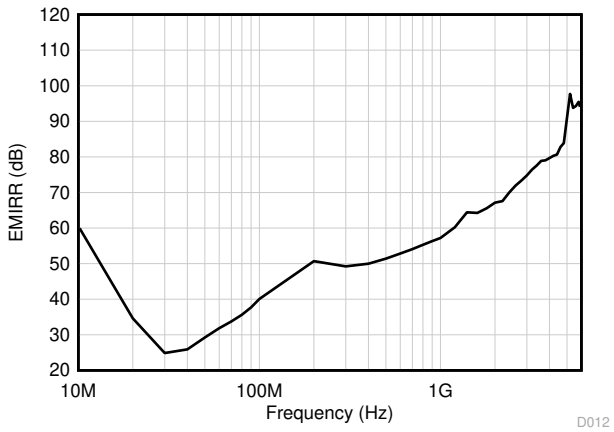


图 5-37. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6 Detailed Description

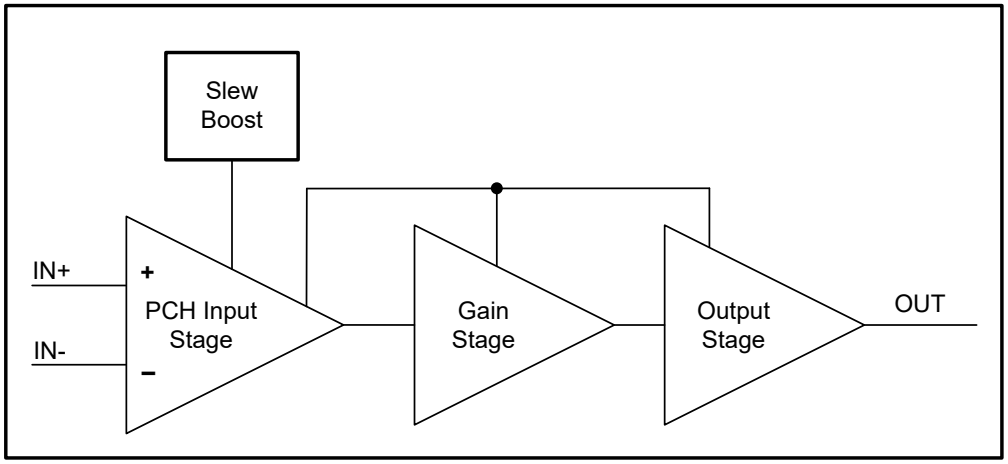
6.1 Overview

The TLV936x-Q1 family (TLV9361-Q1, TLV9362-Q1, and TLV9364-Q1) is a family of 40V, cost-optimized operational amplifiers. These devices offer strong general-purpose DC and AC specifications, including rail-to-rail output, low offset (±400µV, typical), low offset drift (±1.25µV/°C, typical), and 10.6MHz bandwidth.

Convenient features such as wide differential input-voltage range, high output current (±60mA), and high slew rate (25V/µs) make the TLV936x-Q1 a robust operational amplifier for high-voltage, cost-sensitive applications.

The TLV936x-Q1 family of op amps is available in standard packages and is specified from –40°C to 125°C.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 EMI Rejection

The TLV936x-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV936x-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. 图 6-1 shows the results of this testing on the TLV936x-Q1. 表 6-1 lists the EMIRR IN+ values for the TLV936x-Q1 at particular frequencies commonly encountered in real-world applications. 表 6-1 lists applications that can be centered on or operated near the particular frequency shown. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as relates to op amps and is available for download from www.ti.com.

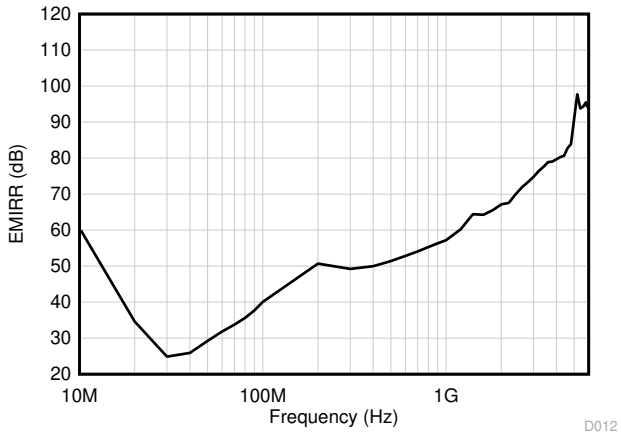

图 6-1. EMIRR Testing

表 6-1. TLV936x-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	50.0dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	56.3dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	65.6dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	70.0dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	78.9dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	91.0dB

6.3.2 Thermal Protection

The internal power dissipation of any amplifier causes the internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the TLV936x-Q1 is 150°C. Exceeding this temperature causes damage to the device. The TLV936x-Q1 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. 图 6-2 shows an application example for the TLV9362-Q1 that has significant self heating because of the power dissipation (0.954W). In this example, both channels have a quiescent power dissipation while one of the channels has a significant load. Thermal calculations indicate that for an ambient temperature of 55°C, the device junction temperature reaches 180°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. 图 6-2

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shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3V.

When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L. If the condition that caused excessive power dissipation is not removed, the amplifier oscillates between a shutdown and enabled state until the output fault is corrected. Please note that thermal performance can vary greatly depending on the package selected and the PCB layout design. This example uses the thermal performance of the SOIC (8) package.

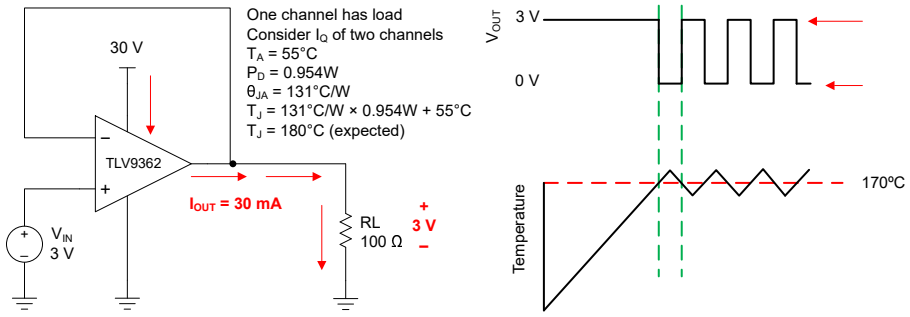

图 6-2. Thermal Protection

6.3.3 Capacitive Load and Stability

The TLV936x-Q1 features an output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to driver large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 图 6-3 and 图 6-4. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

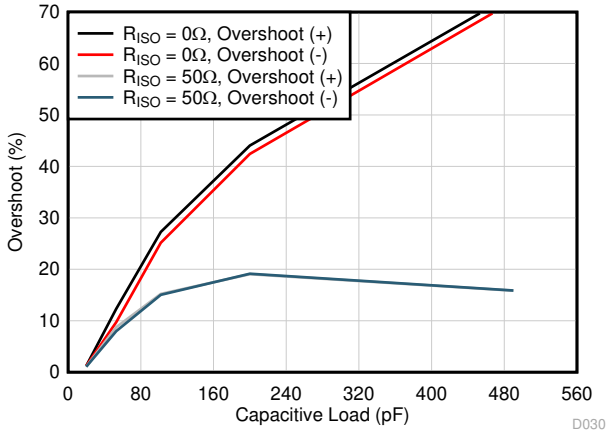

图 6-3. Small-Signal Overshoot vs Capacitive Load ($20mV_{pp}$ Output Step, G = +1)

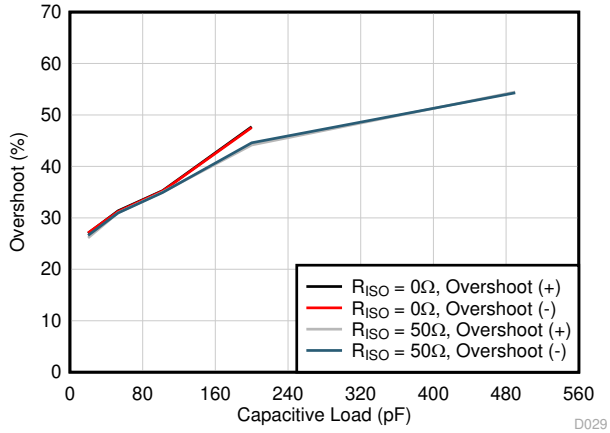

图 6-4. Small-Signal Overshoot vs Capacitive Load ($20mV_{pp}$ Output Step, G = -1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO}, in series with the output, as shown in 图 6-5. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the TLV936x-Q1 an excellent choice for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 图 6-5 uses an isolation

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resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

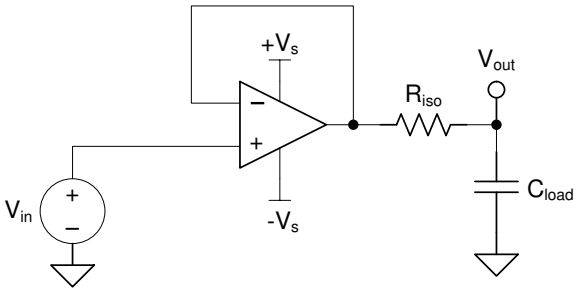

图 6-5. Extending Capacitive Load Drive With the TLV9361-Q1

6.3.4 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and relevance to an electrical overstress event is helpful. 图 6-6 shows an illustration of the ESD circuits contained in the TLV936x-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

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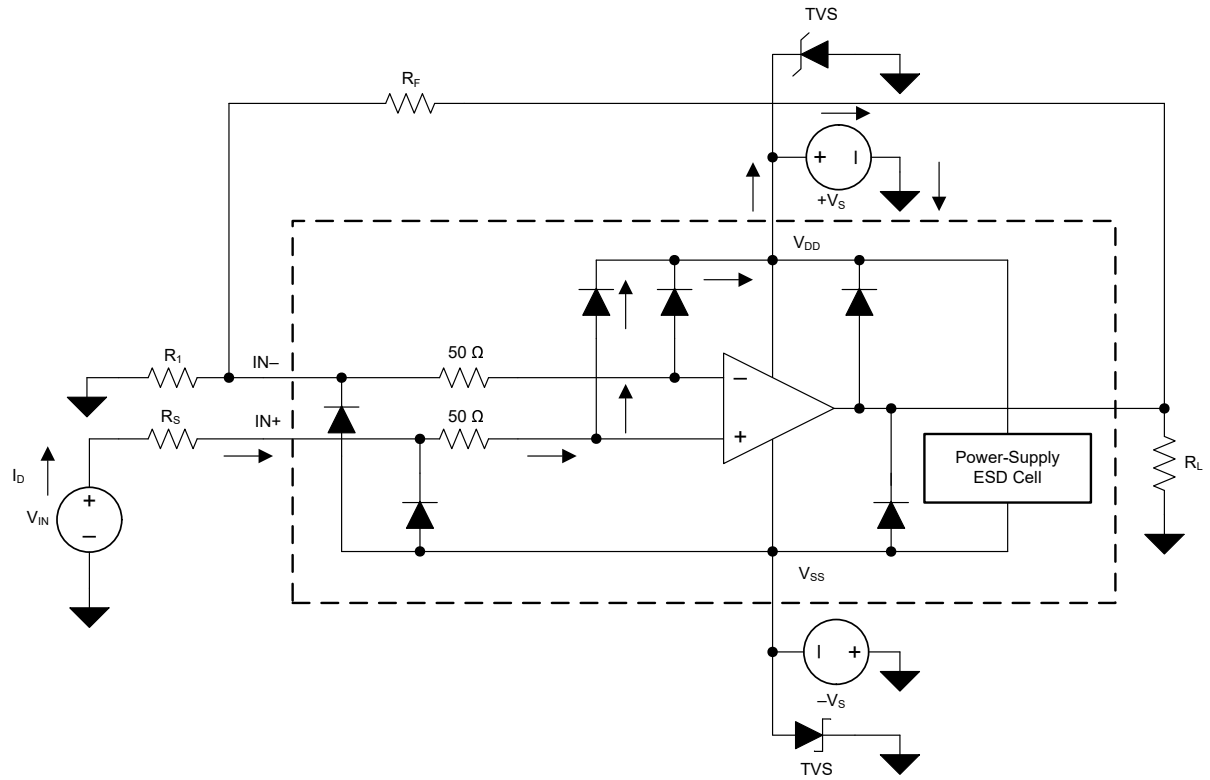

图 6-6. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1kV, 100ns), whereas an EOS event is long duration and lower voltage (for example; 50V, 100ms). The ESD diodes are designed for out-of-circuit ESD protection (that is; during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

6.3.5 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV936x-Q1 is approximately 170ns.

6.3.6 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the ideal value, like the input offset voltage of an amplifier. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers leverage this information to guard band systems, even when there are no minimum or maximum specifications in the *Electrical Characteristics* table.

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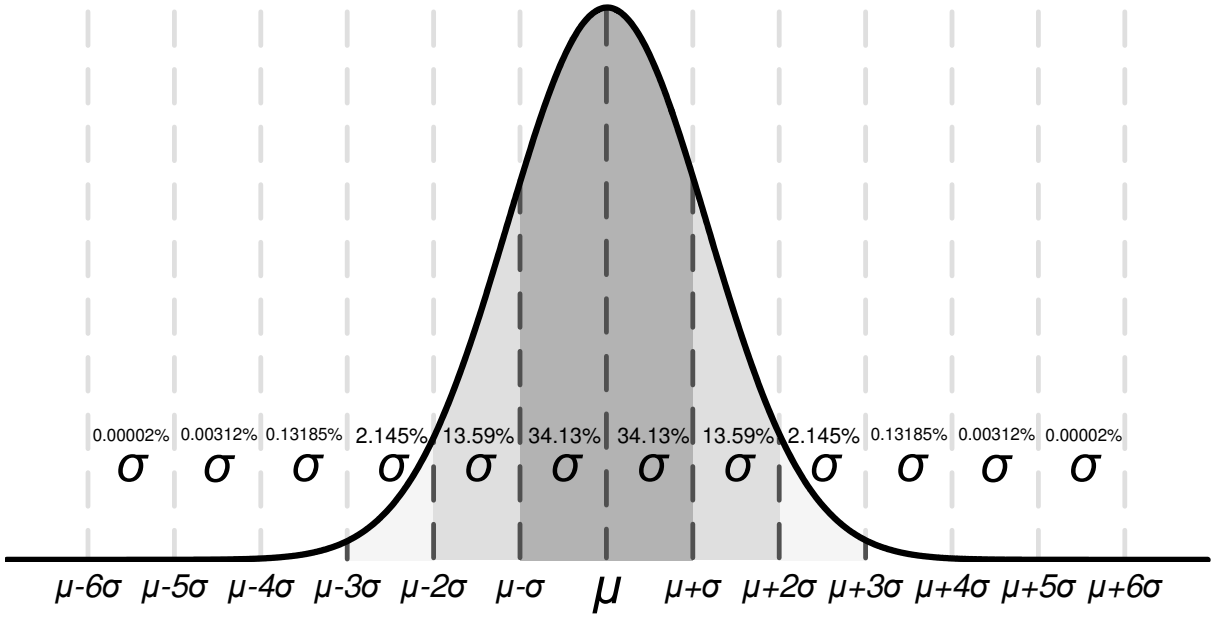

图 6-7. Ideal Gaussian Distribution

图 6-7 shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from *μ* – σ to *μ* + σ).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

Use this chart to calculate approximate probability of a specification in a unit; for example, for TLV936x-Q1, the typical input voltage offset is 400μV, so 68.2% of all TLV936x-Q1 devices are expected to have an offset from –400μV to 400μV. At 4 σ (±1600μV), 99.9937% of the distribution has an offset voltage less than ±1600μV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are specified by TI, and units outside these limits are removed from production material. For example, the TLV936x-Q1 family has a maximum offset voltage of 1.7mV at 125°C, and even though this corresponds to about 4.25 σ (≈2 in 100,000 units), which is unlikely, TI verifies that any unit with larger offset than 1.7mV is removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6 σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and can be an option as a wide guardband to design a system around. In this case, the TLV936x-Q1 family does not have a maximum or minimum for offset voltage drift, but based on the typical value of 1.25μV/°C in the *Electrical Characteristics* table, the 6 σ value is calculated for offset voltage drift is about 7.5μV/°C. When designing for worst-case system conditions, use this value to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot verify the performance of a device. This information must be used only to estimate the performance of a device.

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6.4 Device Functional Modes

The TLV936x-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 4.5V (±2.25V). The maximum power supply voltage for the TLV936x-Q1 is 40V (±20V).

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7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV936x-Q1 family offers excellent DC precision and DC performance. These devices operate up to 40V supply rails and offer true rail-to-rail output, low offset voltage and offset voltage drift, as well as 10.6MHz bandwidth and high output drive. These features make the TLV936x-Q1 a robust, high-performance operational amplifier for high-voltage cost-sensitive applications.

7.2 Typical Applications

7.2.1 Low-Side Current Measurement

图 7-1 shows the TLV936x-Q1 configured in a low-side current sensing application. For a full analysis of the circuit shown in 图 7-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0A to 1A Single-Supply Low-Side Current-Sensing Solution* .

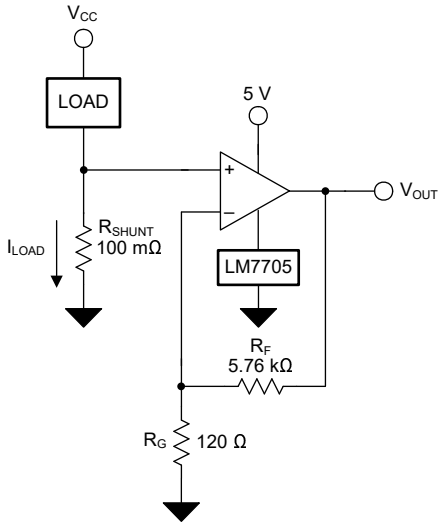

图 7-1. TLV936x-Q1 in a Low-Side, Current-Sensing Application

7.2.2 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Max output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.3 Detailed Design Procedure

The transfer function of the circuit in 图 7-1 is given in 方程式 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using 方程式 2:

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

Using 方程式 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV936x-Q1 to produce an output voltage of 0V to 4.9V. The gain needed by the TLV936x-Q1 to produce the necessary output voltage is calculated using 方程式 3:

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

Using 方程式 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. 方程式 4 is used to size the resistors, R_F and R_G, to set the gain of the TLV936x-Q1 to 49V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing R_F as 5.76kΩ, R_G is calculated to be 120Ω. R_F and R_G were chosen as 5.76kΩ and 120Ω because the values are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. However, excessively large resistors generate thermal noise that exceeds the intrinsic noise of the op amp. 图 7-2 shows the measured transfer function of the circuit shown in 图 7-1.

7.2.4 Application Curves

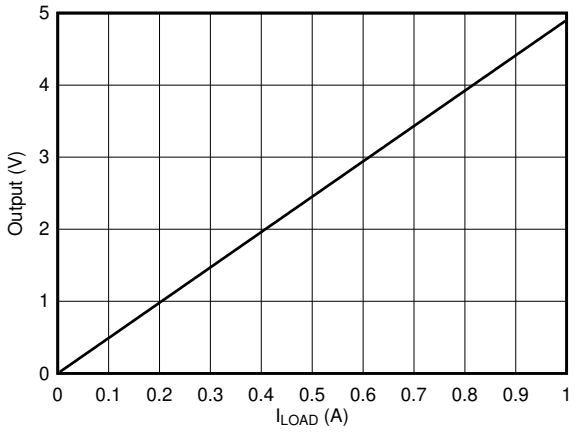

图 7-2. Low-Side, Current-Sense, Transfer Function

7.3 Power Supply Recommendations

The TLV936x-Q1 is specified for operation from 4.5V to 40V (±2.25V to ±20V); many specifications apply from –40°C to 125°C.

小心

Supply voltages larger than 40V can permanently damage the device; see the *Absolute Maximum Ratings* table.

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Place 0.1 μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 图 7-4, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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7.4.2 Layout Example

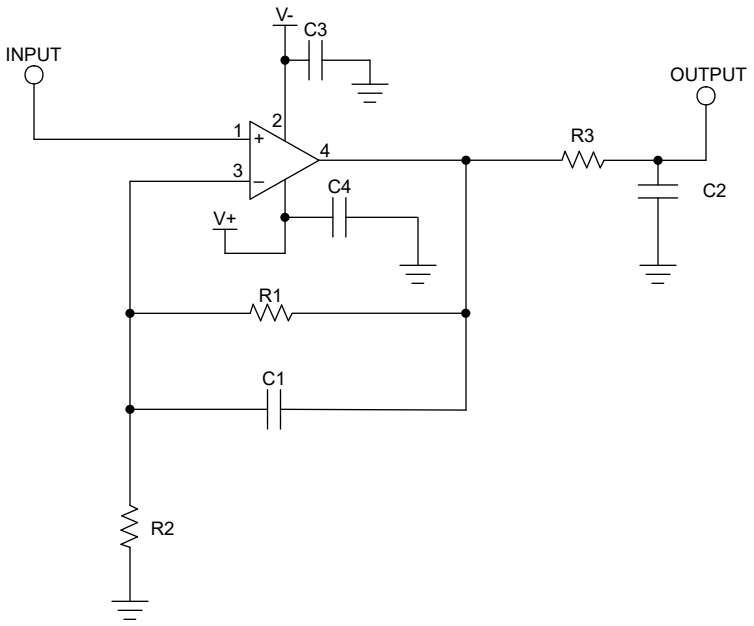

图 7-3. Schematic for Non-inverting Configuration Layout Example

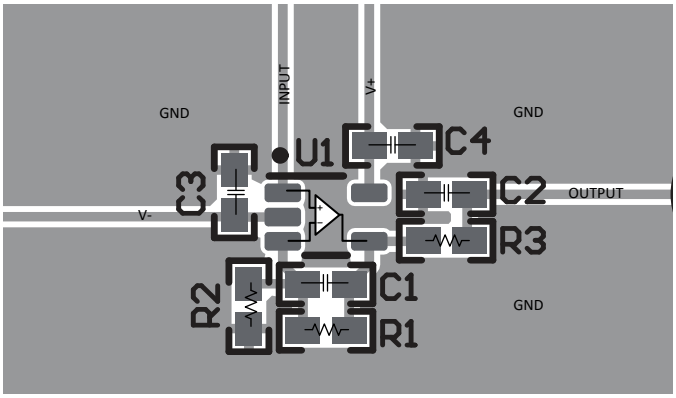

图 7-4. Operational Amplifier Board Layout for Non-inverting Configuration - SC70 (DCK) Package

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

备注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.1.1.2 TI Precision Designs

The TLV936x-Q1 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Analog Engineer's Circuit Cookbook: Amplifiers*
- Texas Instruments, *AN31 amplifier circuit collection* application report
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
- Texas Instruments, *Capacitive Load Drive Solution using an Isolation Resistor* reference design

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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8.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (May 2023) to Revision B (August 2024)	Page
• 向*封装信息*表中添加了 TLV9362-Q1 PW 封装	1
• 将*封装信息*测量值从*本体尺寸（标称值）*更改为*封装尺寸*	1
• Added the TLV9362-Q1 PW package to *Pin Configuration and Functions*	3
• Added 8-pin TSSOP (PW) package to *Thermal Information for Dual Channel table*	7

Changes from Revision * (April 2023) to Revision A (May 2023)	Page
• 将 D 和 DGK 封装状态从*预发布*更改为*正在供货*	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9361QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2W1H
TLV9361QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2W1H
TLV9361QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NL
TLV9361QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NL
TLV9362QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2S6T
TLV9362QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2S6T
TLV9362QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9362D
TLV9362QDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9362D
TLV9362QPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9362PW
TLV9362QPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9362PW
TLV9364QDRQ1	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9364QD
TLV9364QDRQ1.A	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9364QD
TLV9364QPWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9364PW
TLV9364QPWRQ1.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9364PW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV9361-Q1, TLV9362-Q1, TLV9364-Q1 :

- Catalog : TLV9361, TLV9362, TLV9364

NOTE: Qualified Version Definitions:

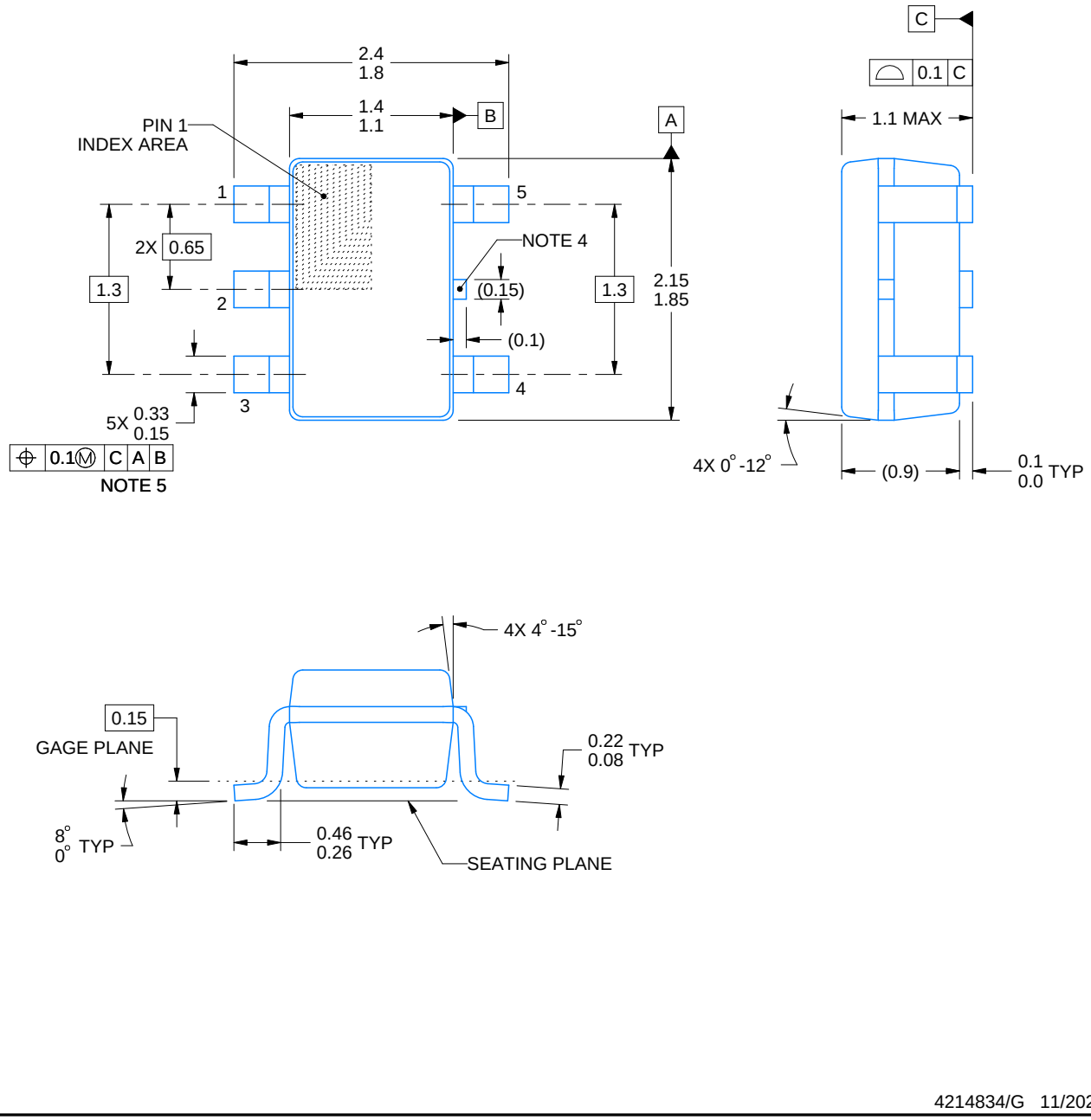
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

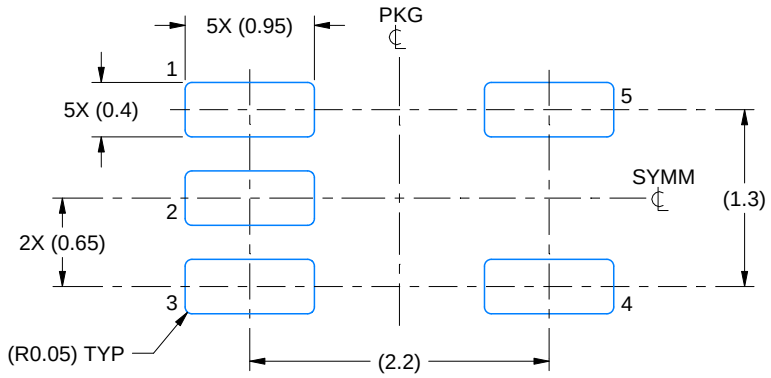
SMALL OUTLINE TRANSISTOR



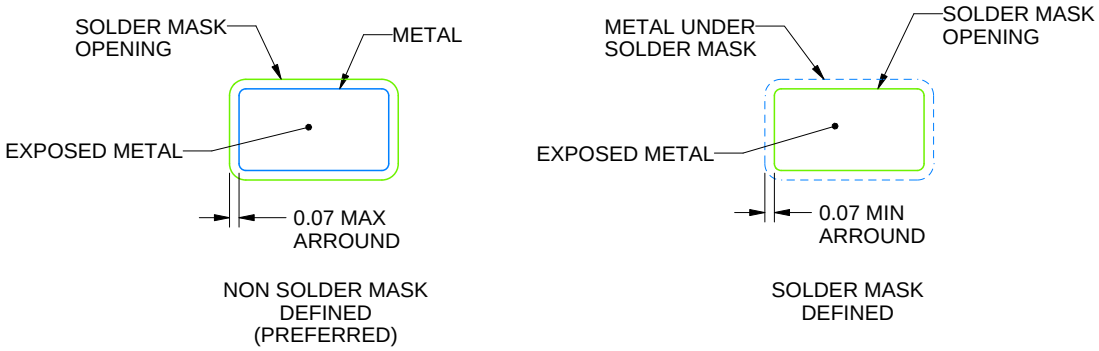
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

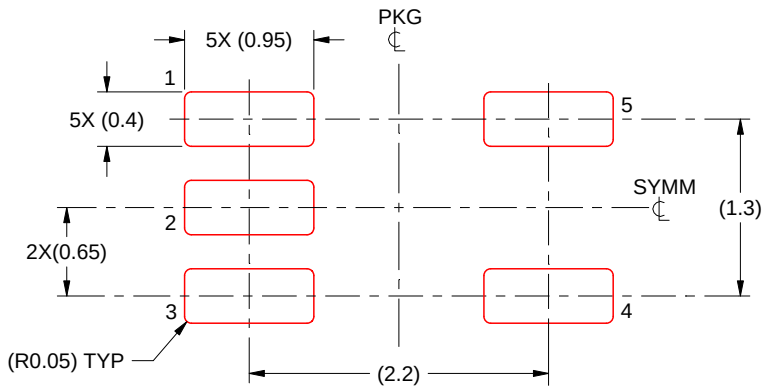


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

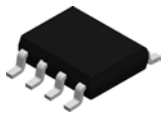


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

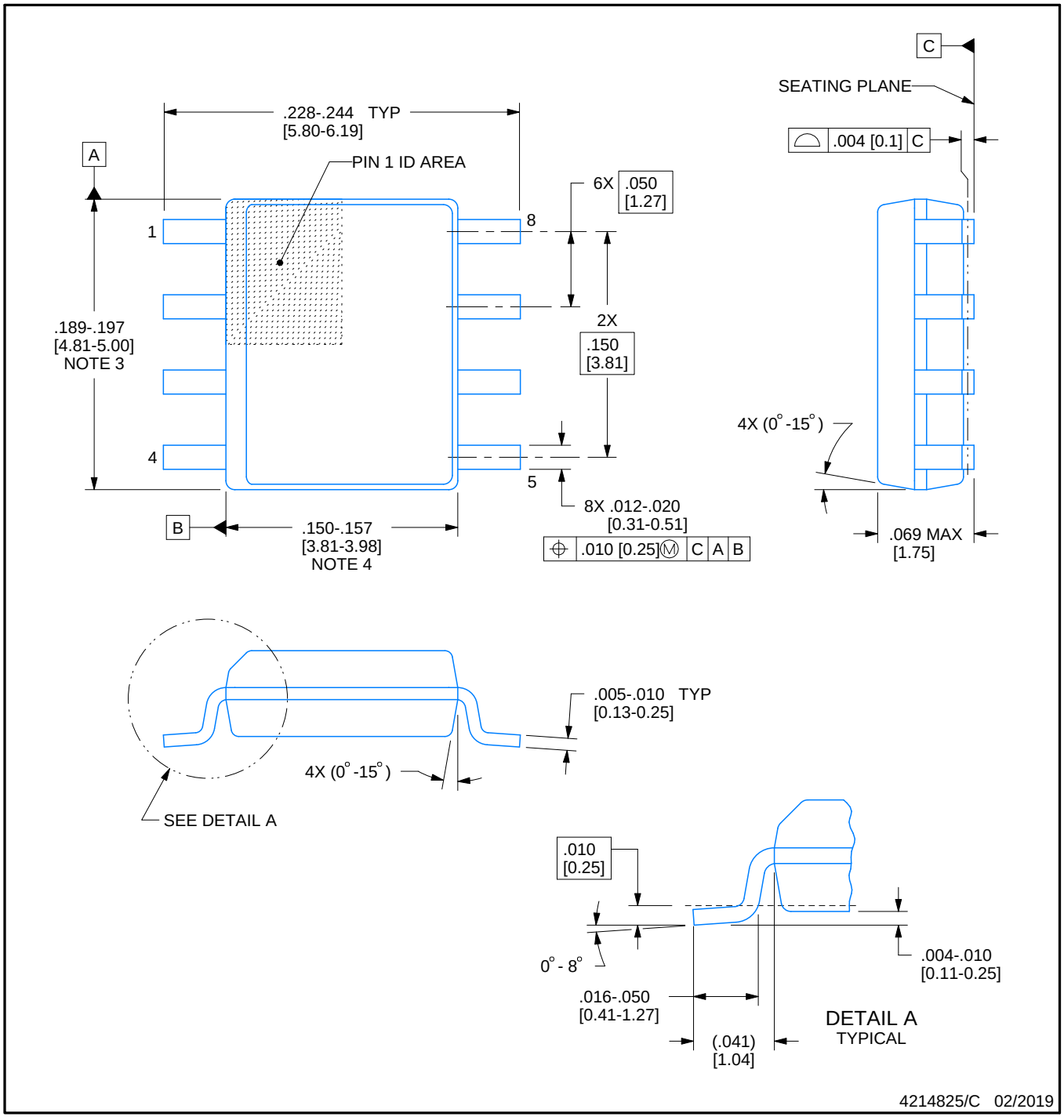


PACKAGE OUTLINE

D0008A

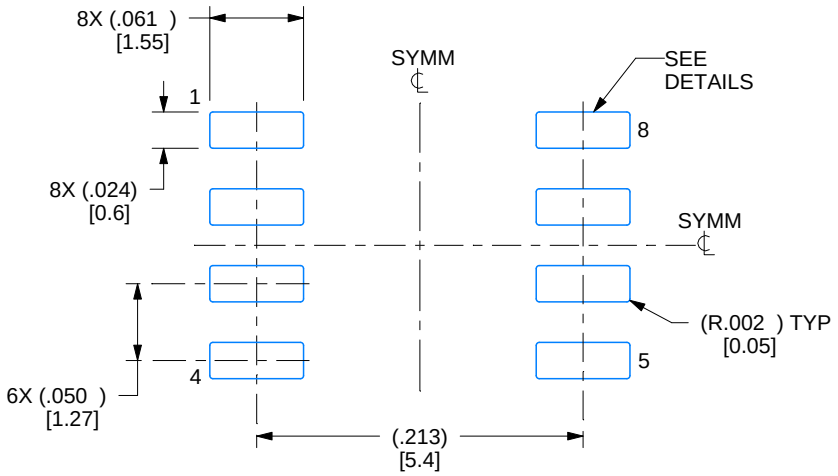
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

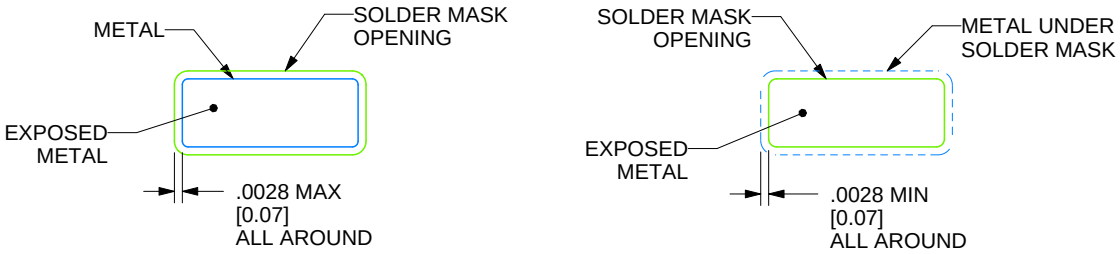


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

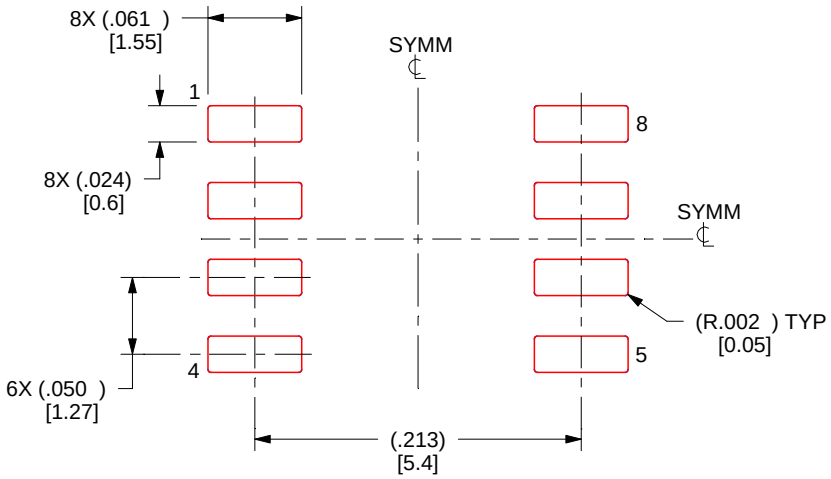
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

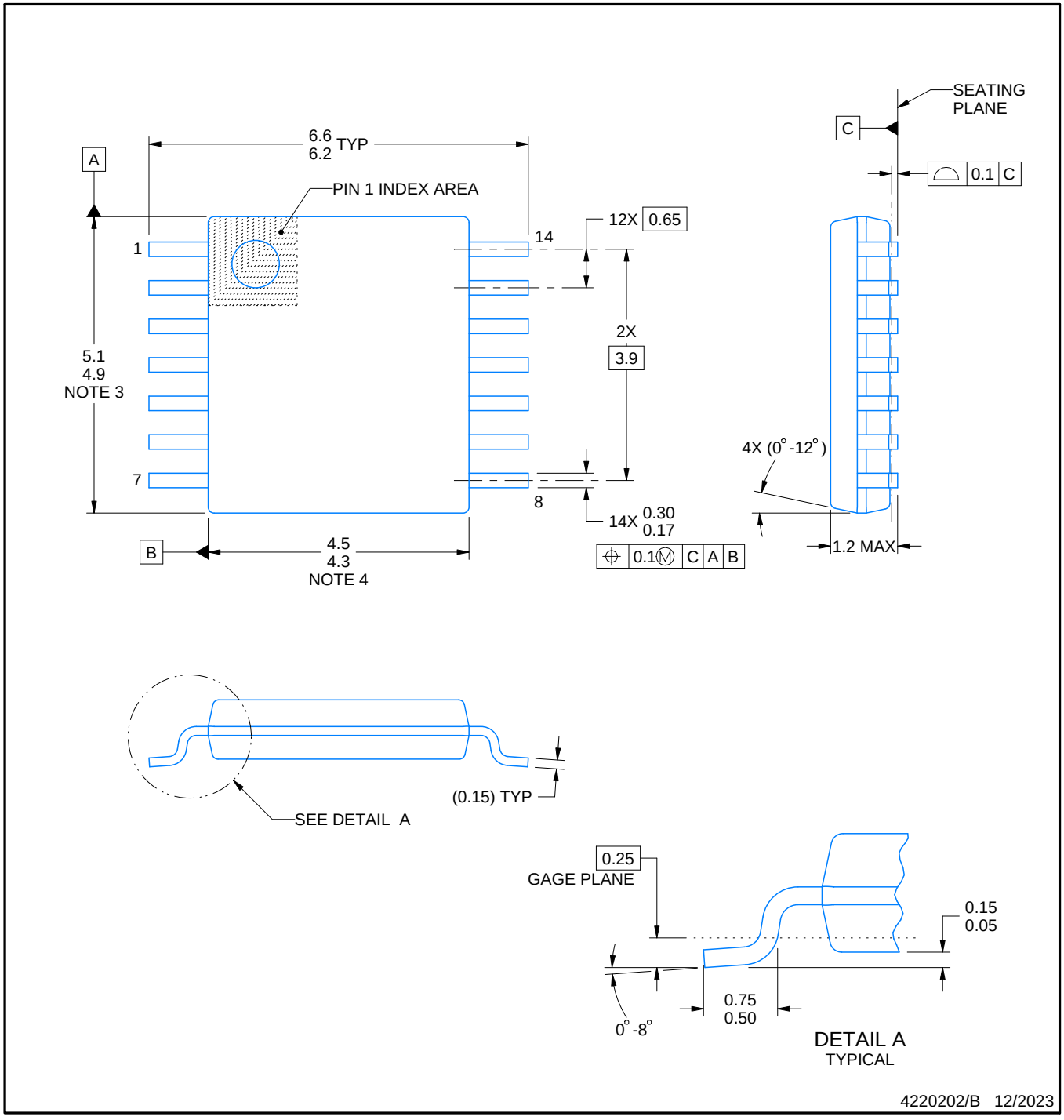
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

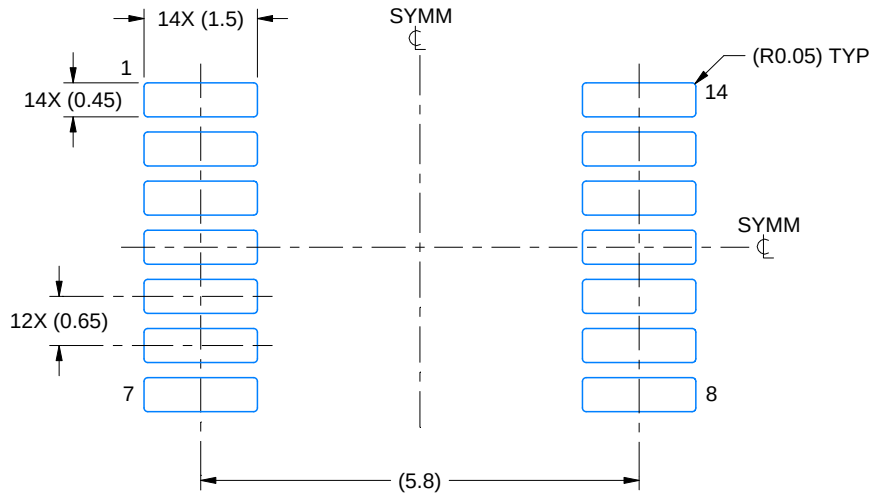
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

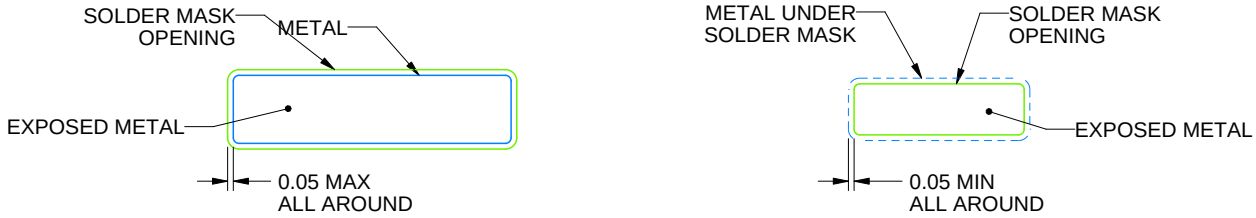


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

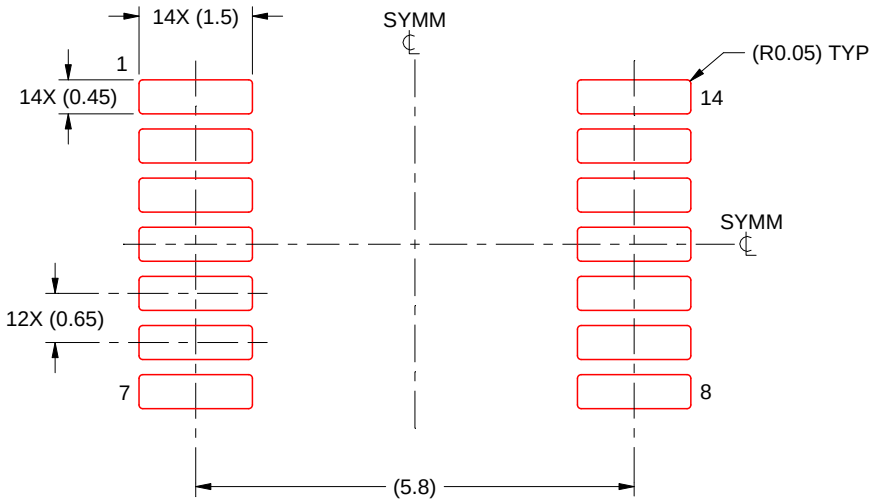


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

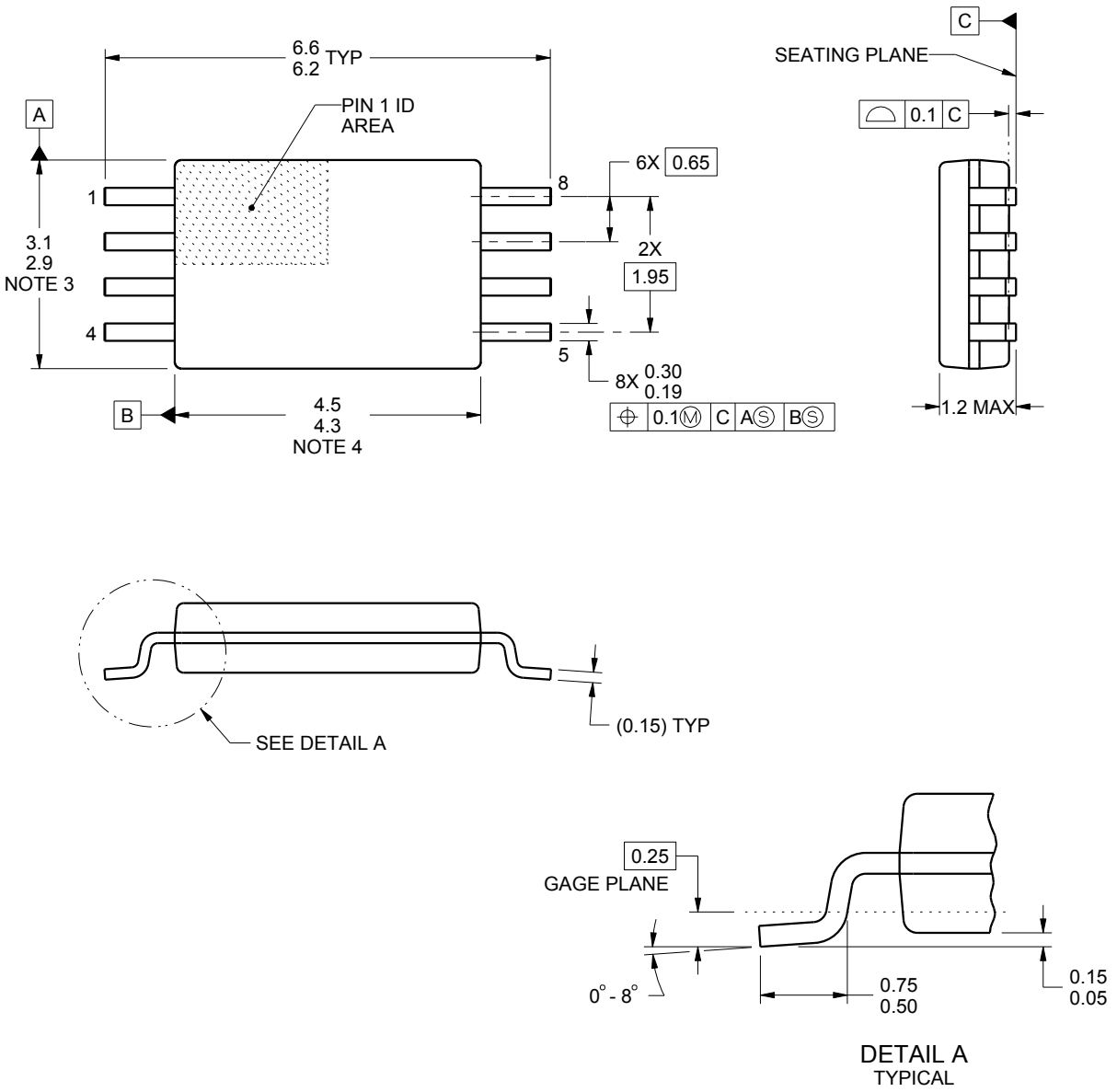
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

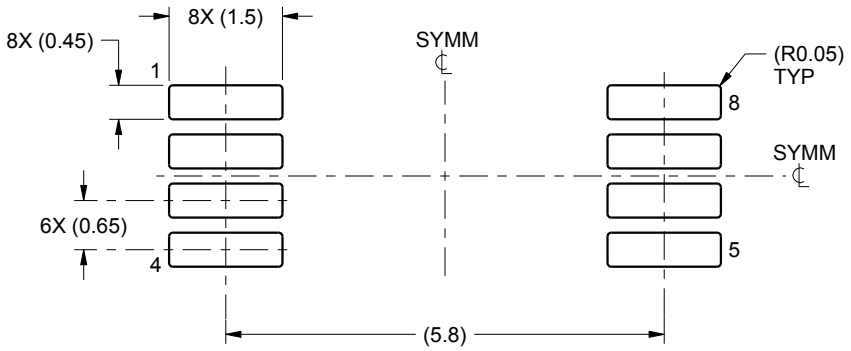
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

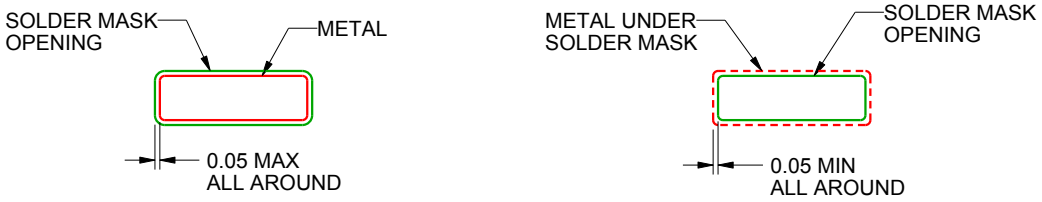


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

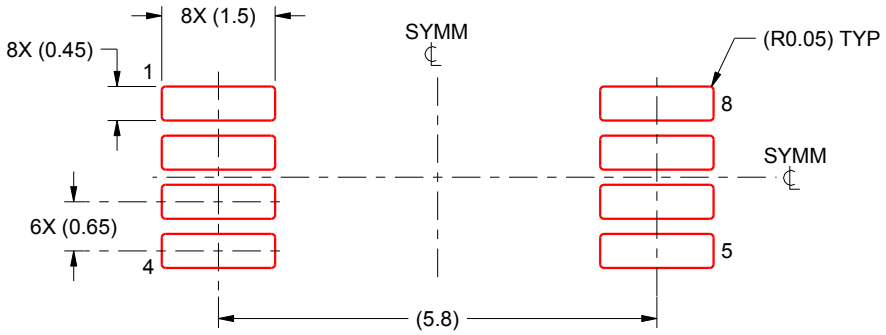


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

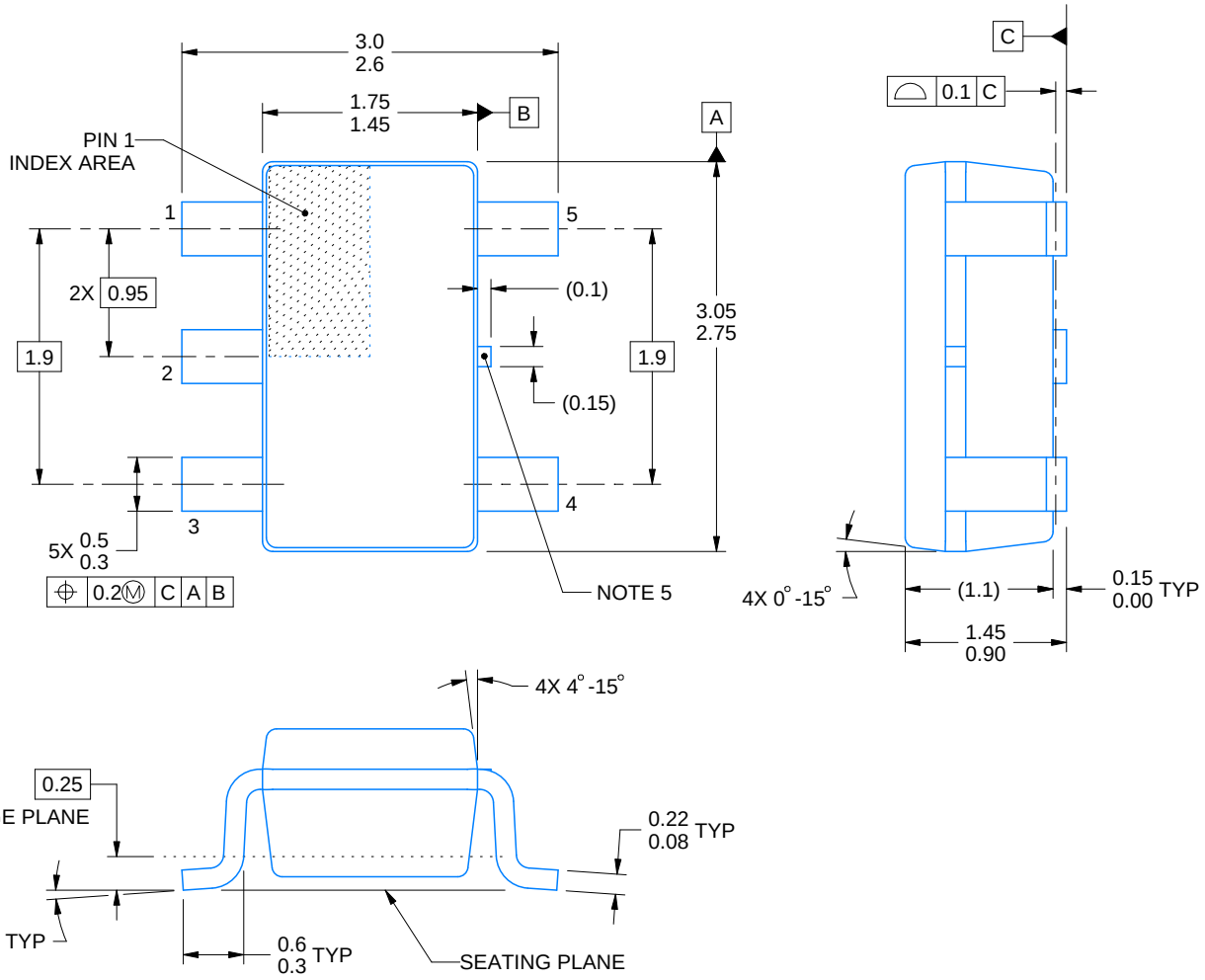
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

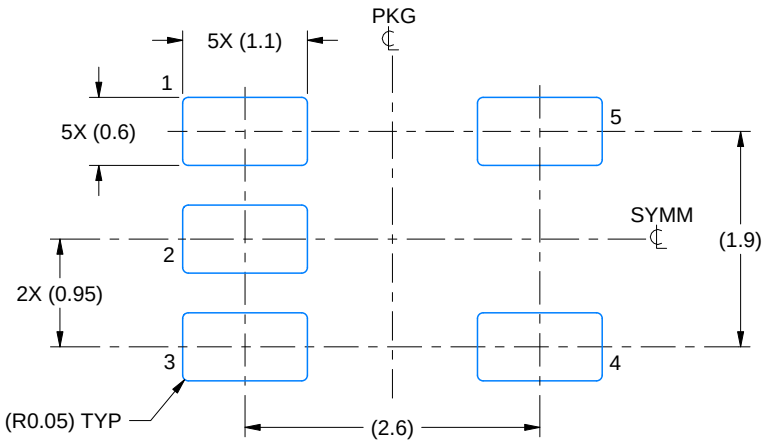
SMALL OUTLINE TRANSISTOR



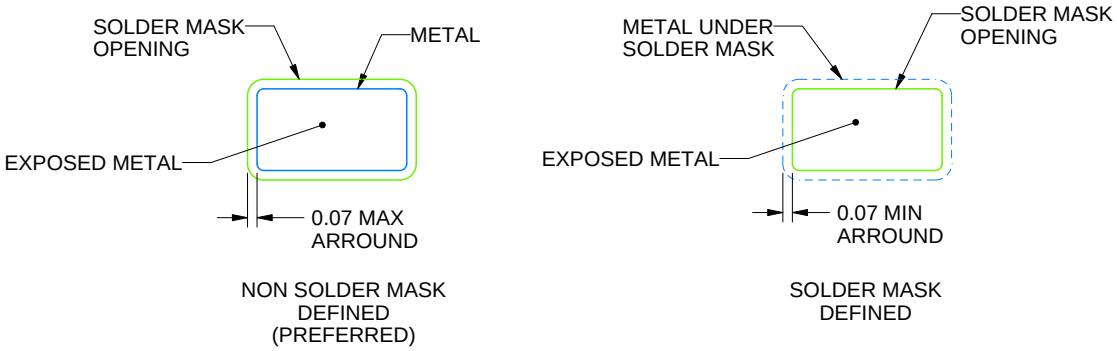
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

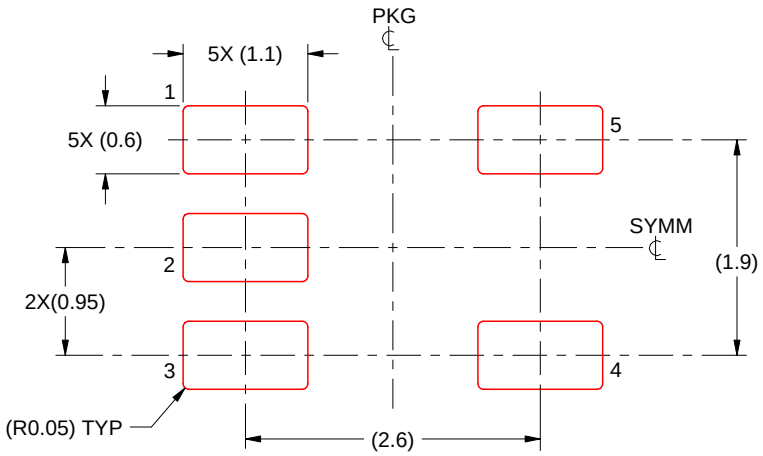


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

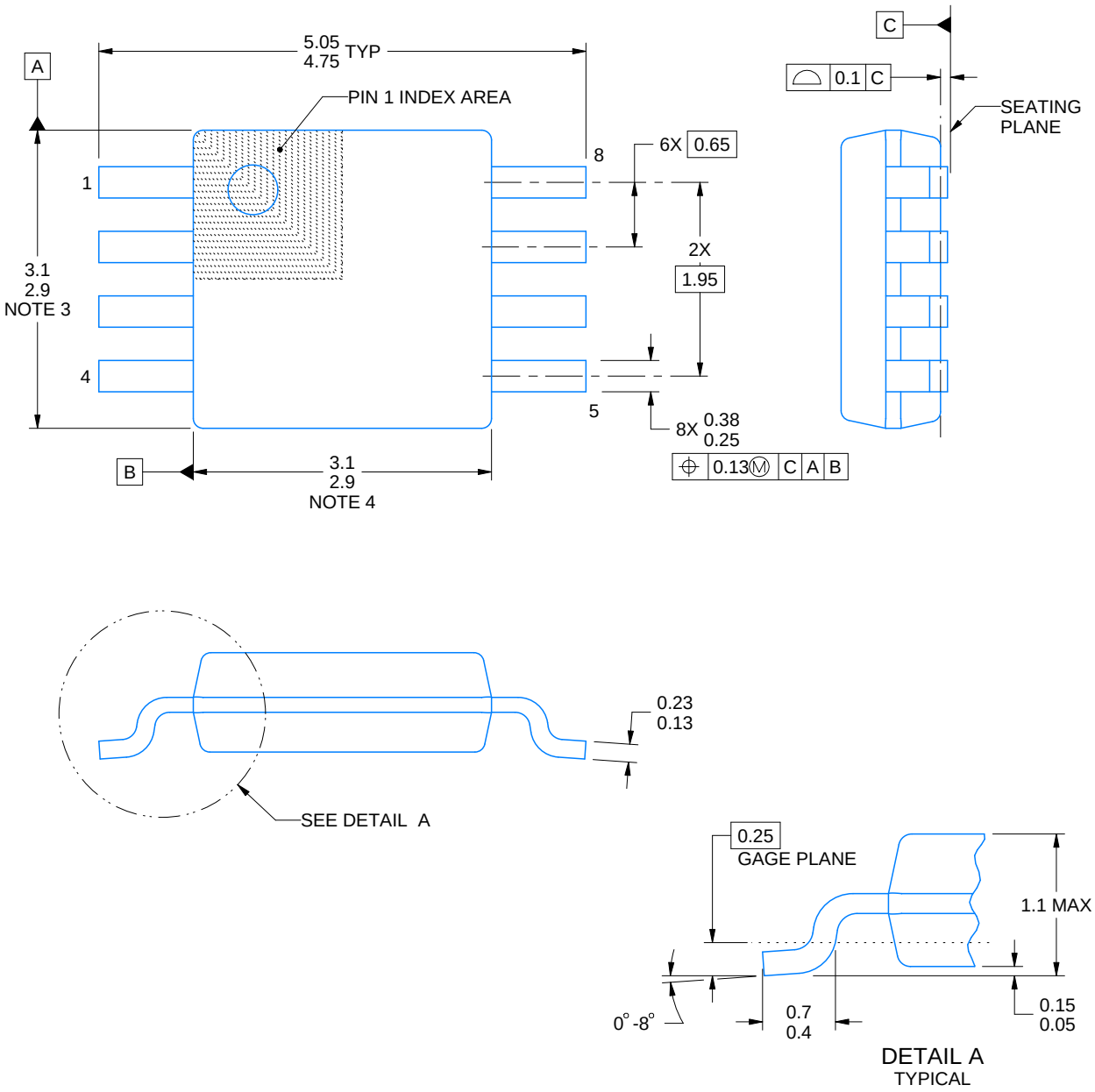
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

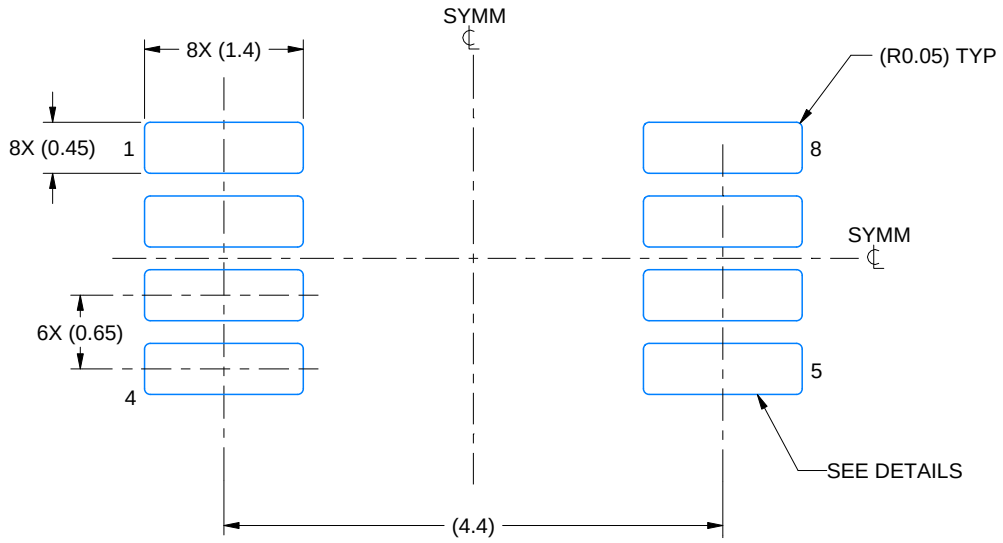
SMALL OUTLINE PACKAGE



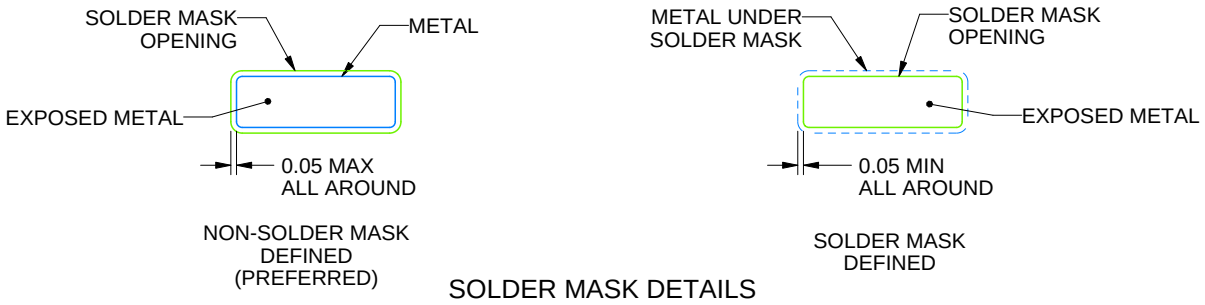
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

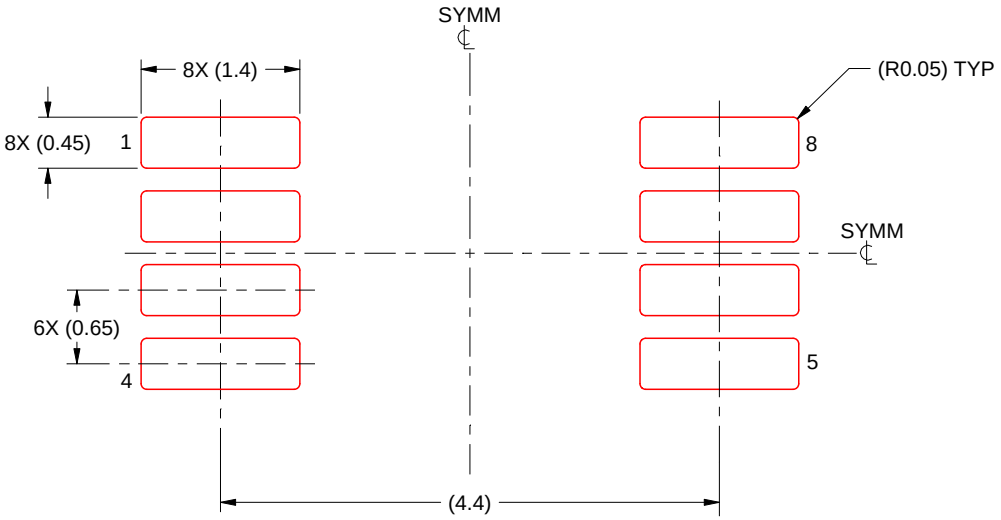


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

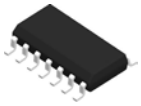


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

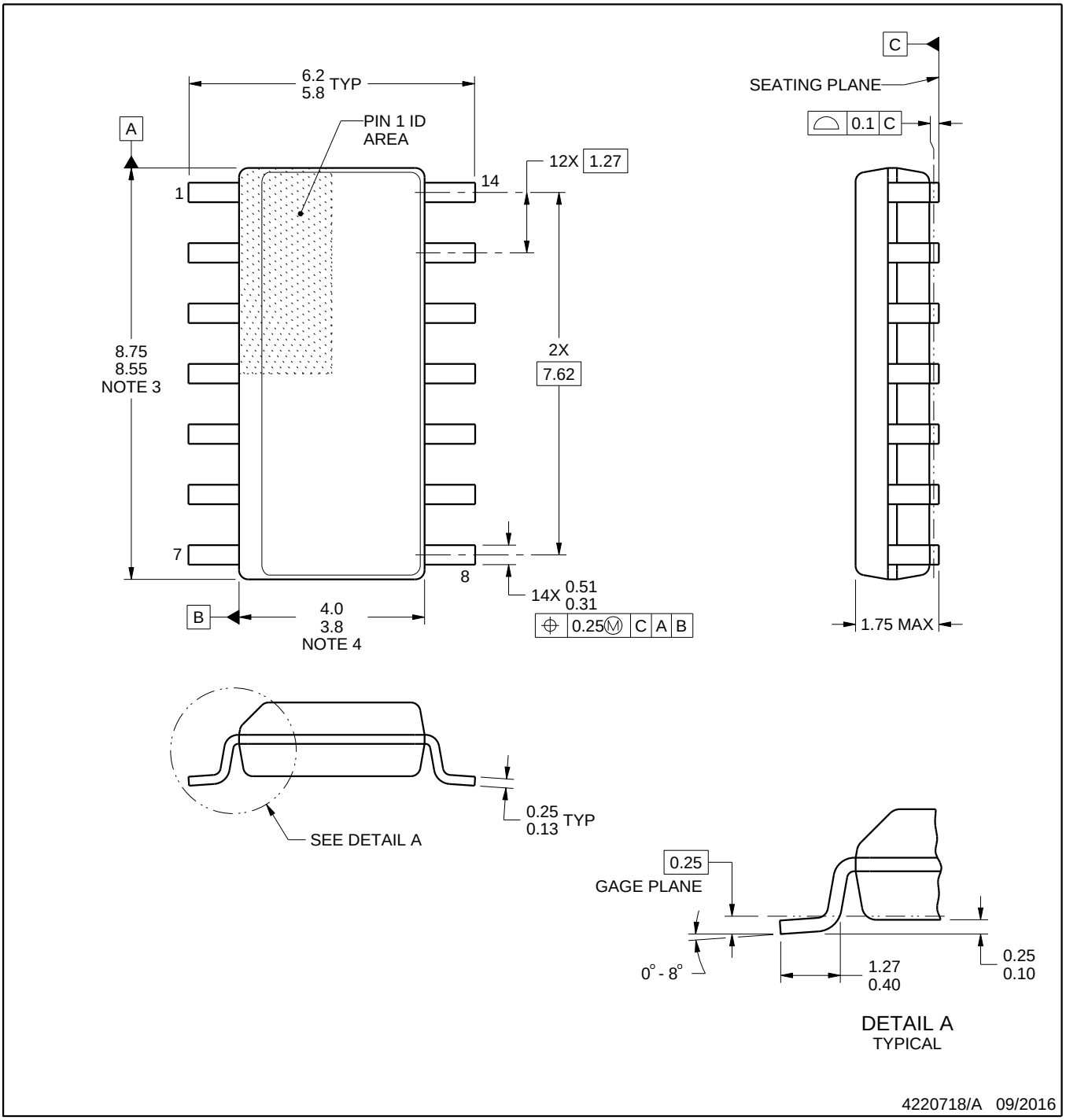


PACKAGE OUTLINE

D0014A

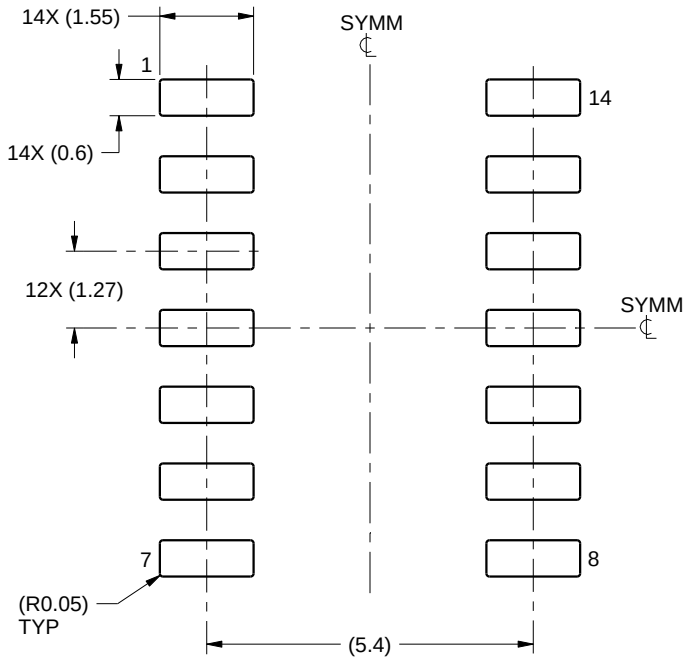
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

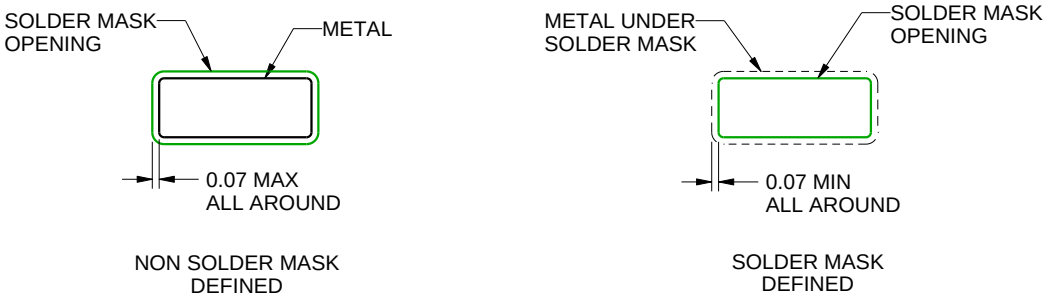


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

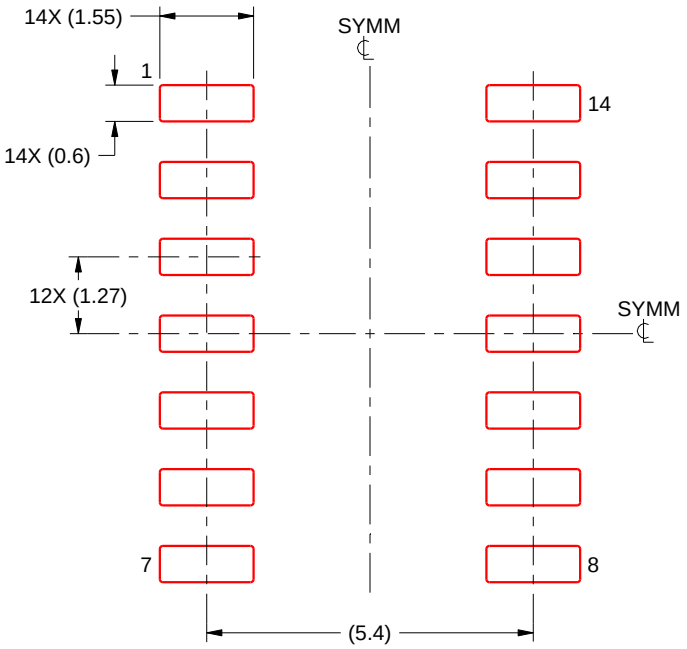
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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