TLV761 18V、1A、固定输出线性稳压器

1 特性

- 与采用选定封装的业界通用 LM1117 和 TLV1117 (x1117) 器件引脚对引脚兼容
- 输入电压范围 V_{IN}：2.5V 至 18V（20V 绝对最大额定值）
- 输出电压范围 V_{OUT}：
  - 0.8V 至 13V（固定值，100mV 阶跃）
- 输出电流：高达 1A
- 低静态电流 I_Q：
  - 60µA（典型值，关断时约 1.5µA）
- 在线路和负载范围内 ±1% 的输出精度
- 高 PSRR：1kHz 频率下为 60dB，1MHz 频率下为 40dB
- 内部软启动时间：500µs（典型值）
- 折返电流限制和热保护
- 与 1µF 的陶瓷输出电容器搭配使用时可保持稳定
- 温度范围：-40°C 至 +125°C
- 封装：
  - 4 引脚 6.5mm x 7mm SOT-223
  - 3 引脚 6.6mm x 10.11mm TO-252

2 应用

- 电器
- 家庭影院和娱乐系统
- 电机驱动器
- HVAC 和楼宇安全系统
- 智能电表

3 说明

TLV761 是一款线性稳压器，在传统 x1117 稳压器（TLV1117 或 LM1117）的基础上改进了功能，具有更严格的输出精度和低静态电流 (I_Q)，可降低待机功耗。TLV761 与其他采用 SOT-223、TO-252 封装且具有固定输出的稳压器引脚对引脚兼容。

TLV761 输入电压范围为 2.5V 至 18V，提供的输出电压范围为 0.8V 至 13V，可支持各种应用。

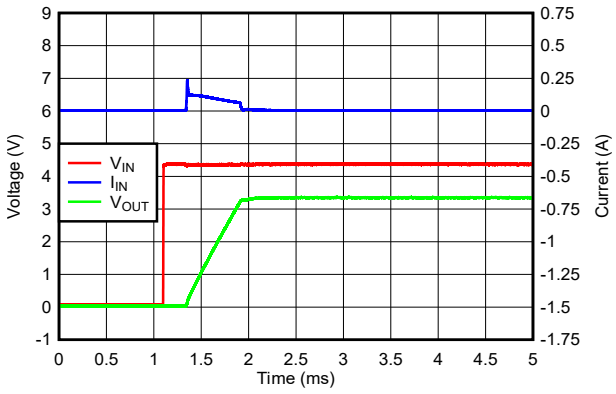
TLV761 的宽带宽 PSRR 性能通常在 1kHz 时大于 60dB，在 1MHz 时大于 40dB，因此有助于减小上游直流/直流转换器的开关频率，并更大限度地减少后置稳压器滤波。

此外，TLV761 还具有内部软启动功能，可减少启动期间的浪涌电流，这有助于通过尽可能减少输入电容来节省设计空间和成本。TLV761 具有折返电流限制，可在高负载电流故障或短路事件期间限制器件的功率耗散。

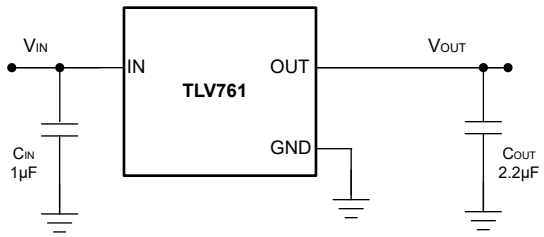
封装信息

器件型号	封装(1)	封装尺寸(2)
TLV761	DCY（SOT-223，4）	6.5mm × 7mm
	KVU（TO-252，3）	6.6mm × 10.11mm

(1) 如需更多信息，请参阅*机械、封装和可订购信息*。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



C_{OUT} 为 22µF 时的浪涌电流



典型应用电路

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4 Pin Configuration and Functions

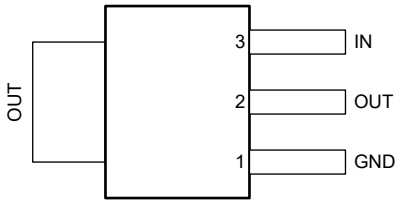


图 4-1. DCY Package, 4-Pin SOT-223 (Top View)

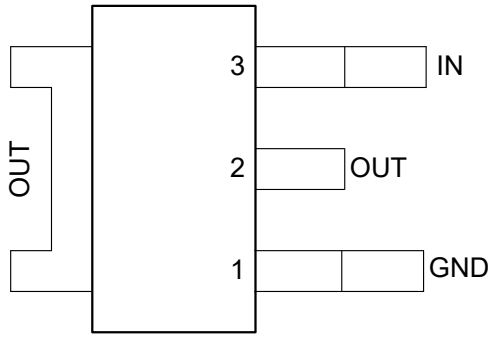


图 4-2. KVU Package, 3-Pin TO-252 (Top View)

表 4-1. Pin Functions

PIN				DESCRIPTION
NAME	DCY	KVU	FUNCTION	
GND	1	1	—	Ground pin
OUT	2, Tab	2, Tab	O	Output pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible.
IN	3	3	I	Input pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage (2)	V_{IN}	–0.3	20	V
	V_{OUT} (3)	–0.3	V_{IN} + 0.3	
Current	Maximum output current	Internally limited		A
Power	Power dissipation	Package limited (4)		W
Temperature	Operating junction (T_J)	–50	150	°C
	Storage (T_{STG})	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.
(3) V_{IN} + 0.3 V or 18 V (whichever is smaller).
(4) See thermal information for further details.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		18	V
V_{OUT}	Output voltage	0.8		13.5	
I_{OUT}	Output current (2.5 V ≤ V_{IN} < 3 V)	0		0.8	A
I_{OUT}	Output current (V_{IN} ≥ 3 V)	0		1	
C_{OUT} ESR	Output capacitor ESR	2		500	mΩ
C_{OUT}	Output capacitor(1)	1	2.2	220	µF
C_{IN}	Input capacitor(2)		1		
T_J	Junction temperature	–40		125	°C

(1) Effective output capacitance of 0.47 µF minimum required for stability.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47 µF minimum is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of systemlevel instability such as ringing or oscillation, especially in the presence of load transients

5.4 Thermal Information

THERMAL METRIC[1]		TLV761		UNIT
		DCY (SOT – 223)	KVU (TO – 252)	
		4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95.4	67.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.6	71.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.7	45.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.9	31.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	33.4	45.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	40.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

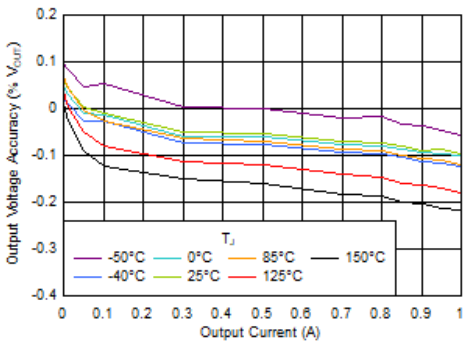
specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.5V or V_{IN} = 2.5V (whichever is greater), I_{OUT} = 10mA, C_{IN} = 1.0µF and C_{OUT} = 1.0µF (unless otherwise noted); typical values are at T_J= 25ºC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Nominal output accuracy	T_J = 25°C	–1		1	%
V_{OUT}	Output accuracy over temperature	VIN ≥ 3.0V, $V_{OUT(NOM)}$ ≤ 9.0V, 1mA ≤ I_{OUT} ≤ 1A	–1.75		1.75	%
		$V_{OUT(NOM)}$ > 9.0V, 1mA ≤ I_{OUT} ≤ 1A	–1.5		1.5	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation[1]	$V_{OUT(NOM)}$ ≤ 9.0V, $V_{OUT(NOM)}$ + 1.5V ≤ V_{IN} ≤ 18V, I_{OUT} = 10mA			0.02	%/V
		$V_{OUT(NOM)}$ > 9.0V, $V_{OUT(NOM)}$ + 1.5V ≤ V_{IN} ≤ 18V, I_{OUT} = 10mA			9.9	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1mA ≤ I_{OUT} ≤ 1A, V_{IN} ≥ 3.0V		0.1	0.75	%/A
V_{DO}	Dropout voltage[2]	V_{IN} ≥ 3.0V, I_{OUT} = 1A		0.9	1.6	V
I_{CL}	Output current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} ≥ 3.0V	1.1		1.6	A
I_{SC}	Short-circuit current limit	V_{OUT} = 0V	150	250	350	mA
I_Q	Quiescent current	I_{OUT} = 0mA		65	100	µA
$I_{PULLDOWN}$	Output pulldown current[3]	V_{IN} = 1.8V, V_{OUT} = 2.5V	0.7		1.1	mA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 300mA, f = 120Hz		70		dB
V_n	Output noise voltage	BW = 10Hz to 100kHz, V_{IN} = 3.3V, V_{OUT} = 0.8V, I_{OUT} = 100mA		60		μV_{RMS}
V_{UVLO+}	UVLO threshold rising	V_{IN} rising		2.2	2.4	V
$V_{UVLO(HYS)}$	UVLO hysteresis			130		mV
V_{UVLO-}	UVLO threshold falling	V_{IN} falling	1.9			V
$T_{SD(shutdown)}$	Thermal shutdown temperature	Temperature increasing		180		ºC
$T_{SD(reset)}$	Thermal shutdown reset temperature	Temperature falling		160		ºC

(1) Line regulation is measured with V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater).
(2) V_{DO} is measured with V_{IN} = 95% x $V_{OUT(nom)}$ for fixed output devices. V_{DO} is not measured for fixed output devices when V_{OUT} < 2.5 V.
(3) $I_{PULLDOWN}$ is measured with V_{IN} = 1.8 V (lower than UVLO falling threshold, with LDO in disabled state) and 2.5 V applied on V_{OUT} externally.

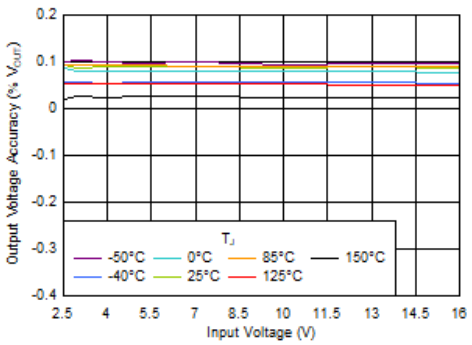
5.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



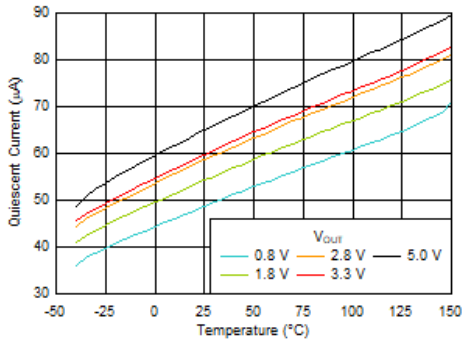
For V_{IN} ⩾ 3.0 V

图 5-1. V_{OUT} Accuracy vs I_{OUT}



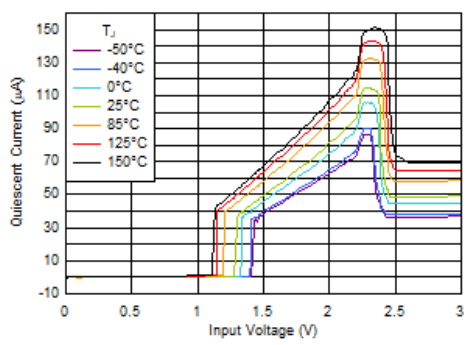
I_{OUT} = 10 mA

图 5-2. V_{OUT} Accuracy vs V_{IN}



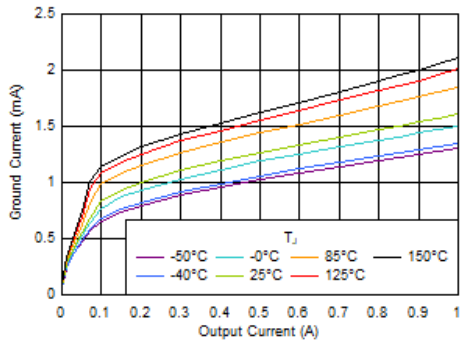
I_{OUT} = 0 mA

图 5-3. I_Q vs Temperature



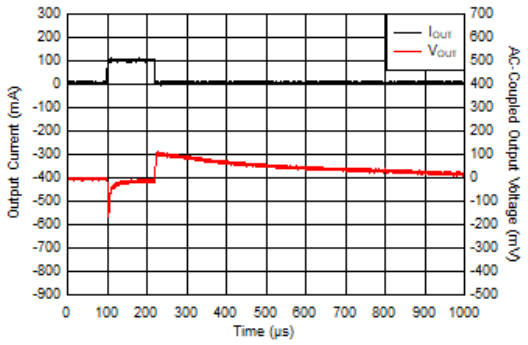
I_{OUT} = 0 mA

图 5-4. I_Q Increase Below Minimum V_{IN}



For V_{IN} ⩾ 3.0 V

图 5-5. I_{GND} vs I_{OUT}

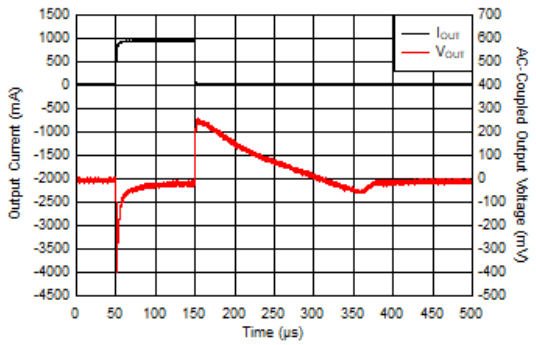


V_{IN} = 5 V, V_{OUT} = 3.3 V, ramp rate = 0.4 A/µs

图 5-6. I_{OUT} Transient From 0 mA to 100 mA

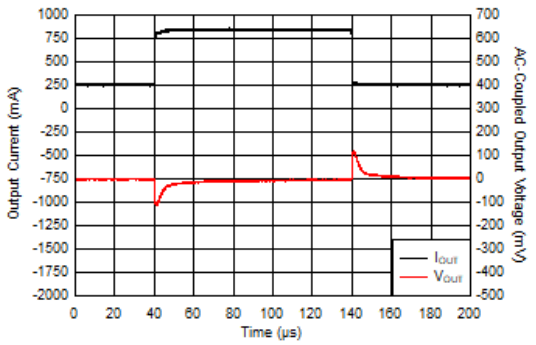
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



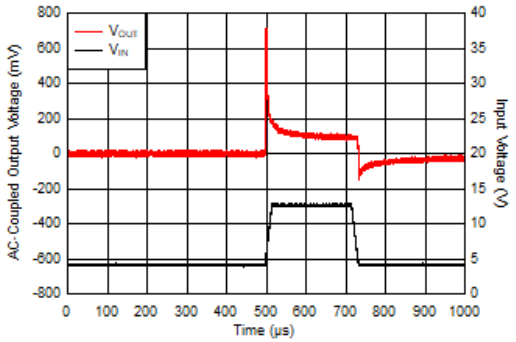
V_{IN} = 5 V, V_{OUT} = 3.3 V, ramp rate = 0.5 A/µs

图 5-7. I_{OUT} Transient From 1 mA to 1 A



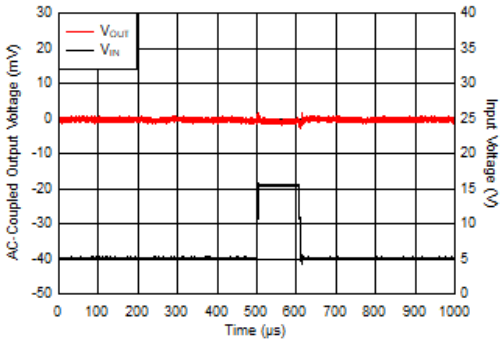
V_{IN} = 5 V, V_{OUT} = 3.3 V, ramp rate = 0.8 A/µs

图 5-8. I_{OUT} Transient From 250 mA to 850 mA



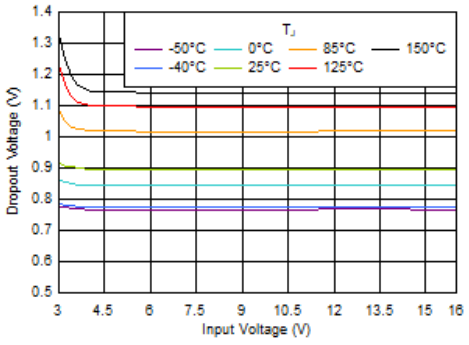
V_{IN} = 5 V V_{OUT} = 3.3 V, I_{OUT} = 1 A, V_{IN} ramp rate = 0.6 V/µs

图 5-9. V_{IN} Transient in Dropout From 4 V to 13 V



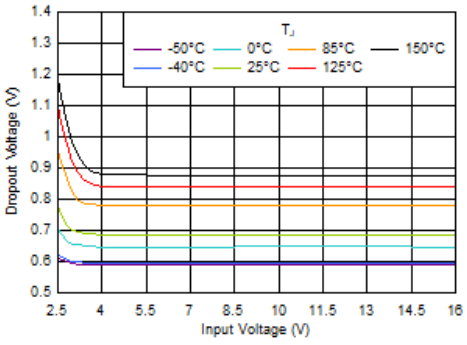
V_{OUT} = 3.3 V, I_{OUT} = 33 µA, V_{IN} ramp rate = 1.6 V/µs

图 5-10. V_{IN} Transient From 5 V to 16 V



I_{OUT} = 1.0 A

图 5-11. V_{DO} vs V_{IN}



I_{OUT} = 0.8 A

图 5-12. V_{DO} vs V_{IN}

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)

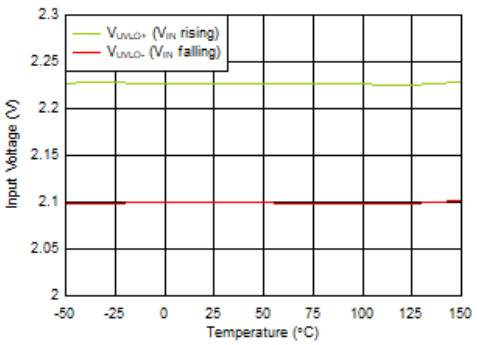
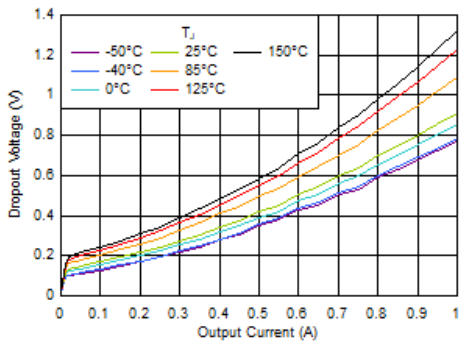
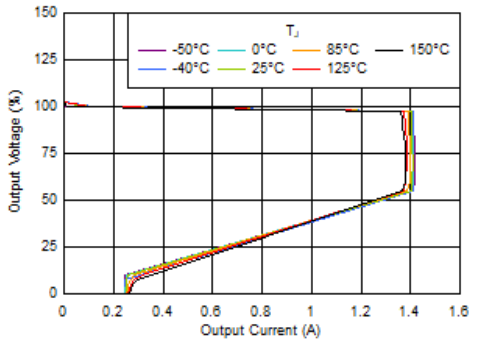


图 5-13. UVLO Thresholds vs Temperature



For V_{IN} ⩾ 3.0 V

图 5-14. V_{DO} vs I_{OUT}



For V_{IN} ⩾ 3.0 V

图 5-15. Foldback Current Limit vs Temperature

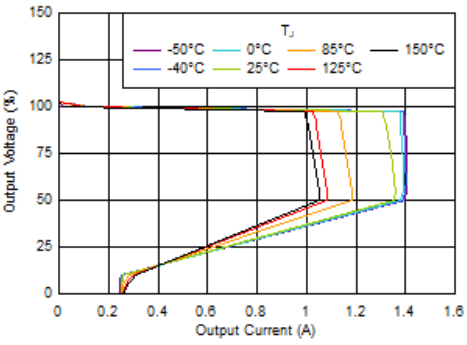
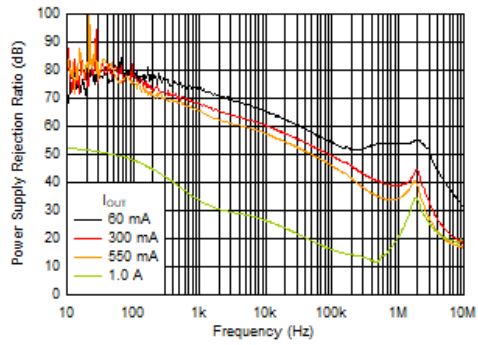
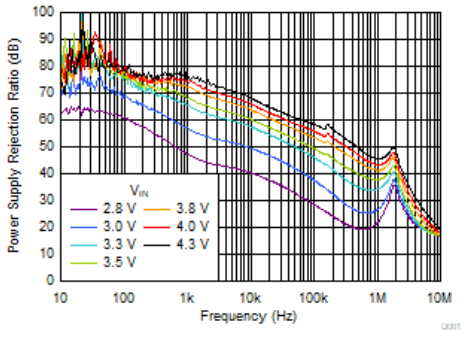


图 5-16. Foldback Current Limit vs Temperature



V_{OUT} = 1.8 V, V_{IN} = 3.3 V

图 5-17. PSRR vs I_{OUT}

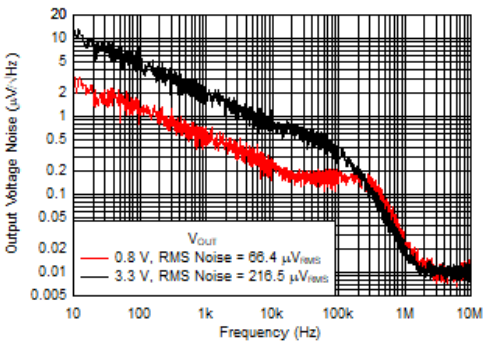


V_{OUT} = 1.8 V, I_{OUT} = 0.55 A

图 5-18. PSRR vs V_{IN}

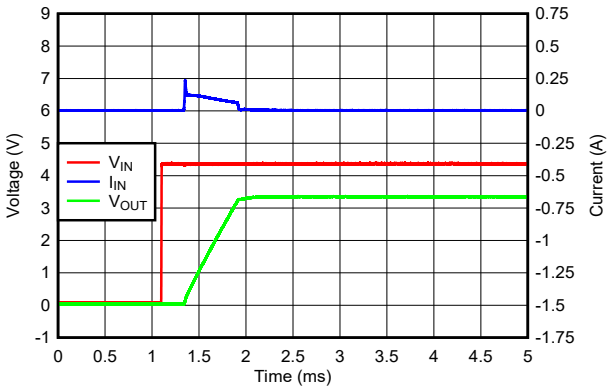
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



I_{OUT} = 0.1 A, RMS noise BW = 10 Hz to 100 kHz

图 5-19. Output Noise (V_n) vs V_{OUT}



I_{OUT} = 0.1 A, C_{OUT} = 22 µF

图 5-20. Inrush Current With 22 µF at C_{OUT}

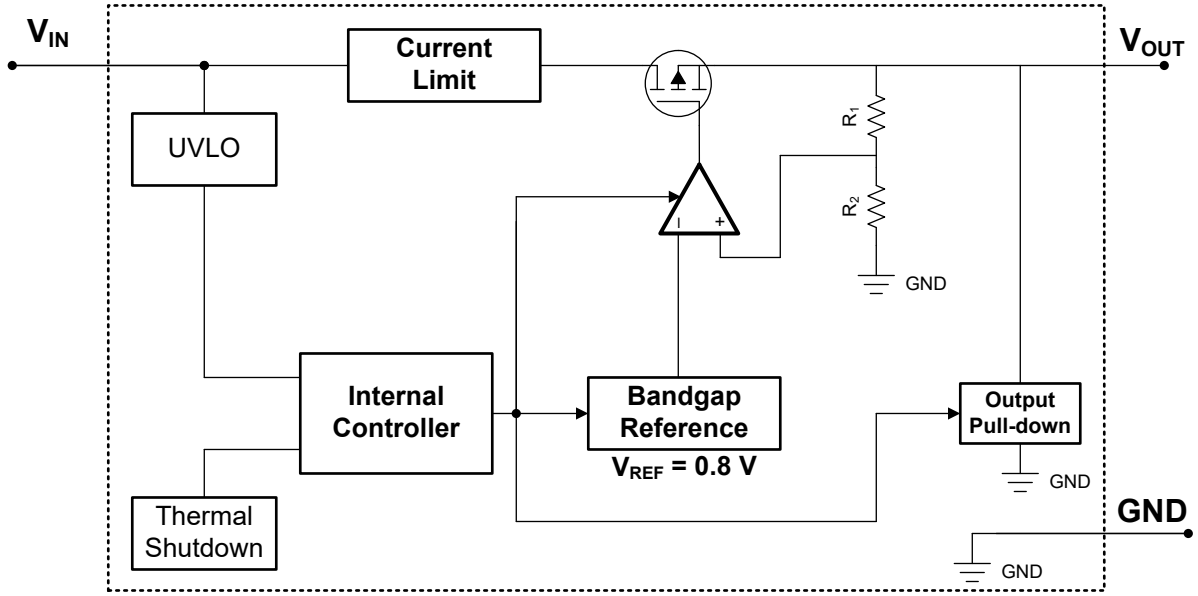
6 Detailed Description

6.1 Overview

The TLV761 is a low quiescent current, high PSRR linear regulator capable of sourcing load current up to 1 A. This device is designed for high current applications such as appliances where there are increasingly stringent requirements for standby and active power consumption.

This device features integrated foldback current limit, thermal shutdown, internal output pulldown, and undervoltage lockout (UVLO). This device delivers excellent line and load transient performance. The TLV761 is low noise and exhibits very good PSRR. The operating ambient temperature range of the device is –40°C to +125°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.2 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 50% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

图 6-1 shows a diagram of the foldback current limit.

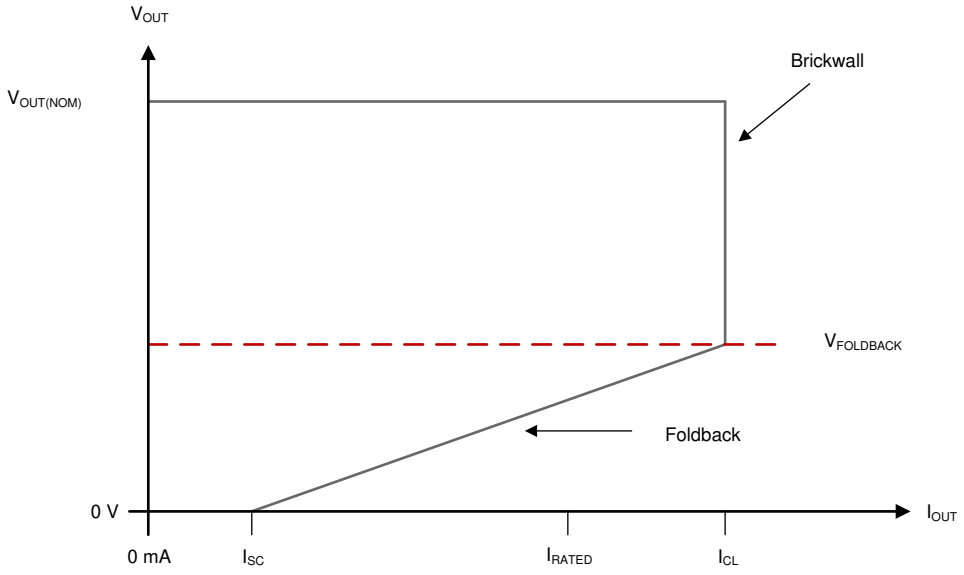


图 6-1. Foldback Current Limit

6.3.3 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

6.3.4 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

表 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER		
	V_{IN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start-up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

7.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.1.3 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leqslant V_{IN}$ + 0.3 V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

图 7-1 shows one approach for protecting the device.

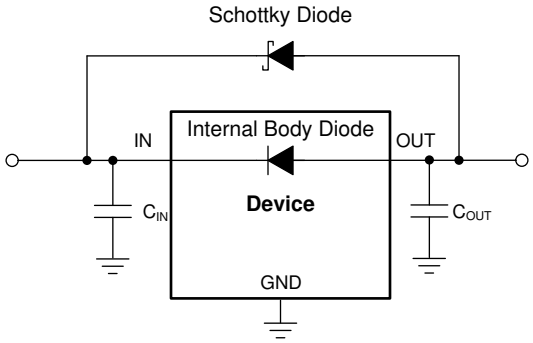


图 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

备注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.1.5 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J). As described in the following equations, use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (4)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (5)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.2 Typical Application

The TLV761 is a low quiescent current linear regulator designed for high current applications. Unlike most typical high current linear regulators, the TLV761 consumes significantly less quiescent current. This device delivers excellent line and load transient performance. The device is low noise and exhibits a very good PSRR. As a result, the TLV761 is designed for high current applications that require very sensitive power-supply rails.

This regulator offers both current limit and thermal protection. The operating ambient temperature range of the device is –40°C to +125°C.

图 7-2 shows a typical application circuit for this device.

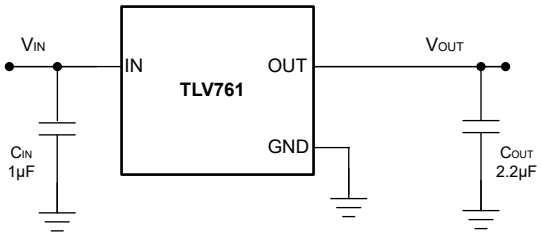


图 7-2. Typical Application Circuit

7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-1 as the input parameters.

表 7-1. Design Parameters

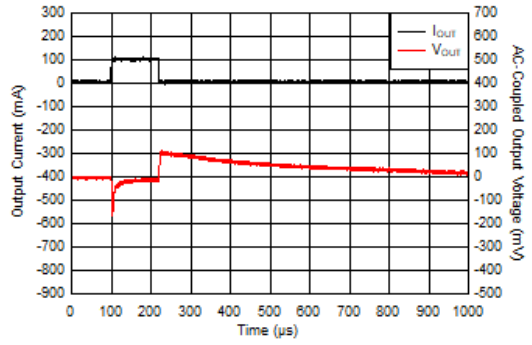
PARAMETER	DESIGN REQUIREMENT
Input voltage	12 V
Output voltage	3.3 V
Output current	50 mA

7.2.2 Detailed Design Procedure

For this design example, the 3.3-V, fixed-version TLV76133 is selected and is powered by a standard 12-V input supply. The dropout voltage (V_{DO}) is kept within the TLV761 dropout voltage specification for the 3.3-V output voltage option to keep the device in regulation under all load and temperature conditions for this design. A 1.0-µF output capacitor is recommended for excellent load transient response. The input capacitor is optional and is used to reduce the input impedance of the circuit and improve the transient response.

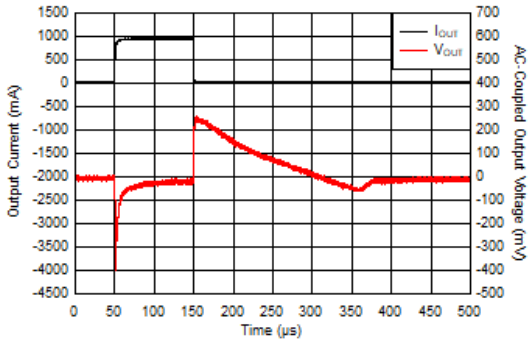
As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude.

7.2.3 Application Curves



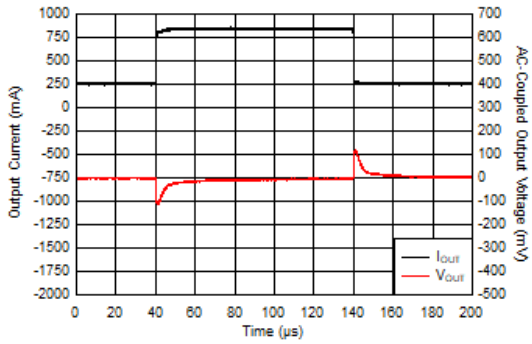
V_{IN} = 5 V, V_{OUT} = 3.3 V, ramp rate = 0.4 A/µs

图 7-3. I_{OUT} Transient From 0 mA to 100 mA



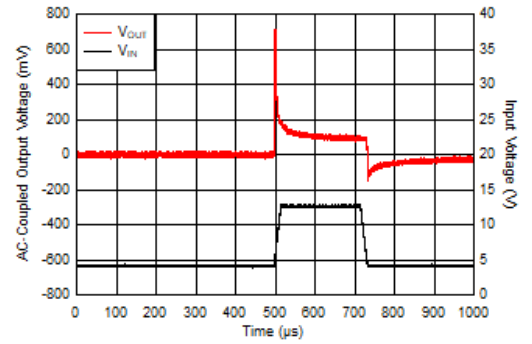
V_{IN} = 5 V, V_{OUT} = 3.3 V, ramp rate = 0.5 A/µs

图 7-4. I_{OUT} Transient From 1 mA to 1 A



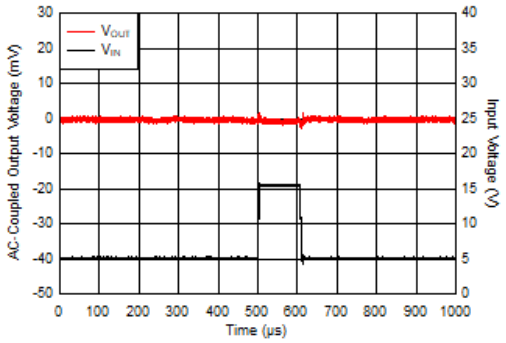
V_{IN} = 5 V, V_{OUT} = 3.3 V, ramp rate = 0.8 A/µs

图 7-5. I_{OUT} Transient From 250 mA to 850 mA



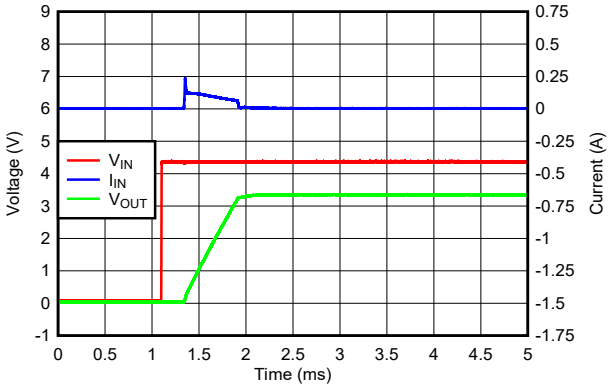
V_{IN} = 5 V V_{OUT} = 3.3 V, I_{OUT} = 1 A, V_{IN} ramp rate = 0.6 V/µs

图 7-6. V_{IN} Transient in Dropout From 4 V to 13 V



V_{OUT} = 3.3 V, I_{OUT} = 33 µA, V_{IN} ramp rate = 1.6 V/µs

图 7-7. V_{IN} Transient From 5 V to 16 V



I_{OUT} = 0.1 A, C_{OUT} = 22 µF

图 7-8. Inrush Current With 22 µF at C_{OUT}

7.3 Best Design Practices

Place input and output capacitors as close to the device as possible.

Use a ceramic output capacitor.

Do not exceed the device absolute maximum ratings.

7.4 Power Supply Recommendations

Connect a low output impedance power supply directly to the INPUT pin of the device . Inductive impedances between the input supply and the INPUT pin can create significant voltage excursions at the INPUT pin during start-up or load transient events.

7.5 Layout

7.5.1 Layout Guidelines

Place input and output capacitors as close to the device pins as possible. To improve characteristic AC performance such as PSRR, output noise, and transient response, design the board with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must be connected directly to the GND pin of the device. Higher value ESR capacitors can degrade PSRR performance.

7.5.2 Layout Examples

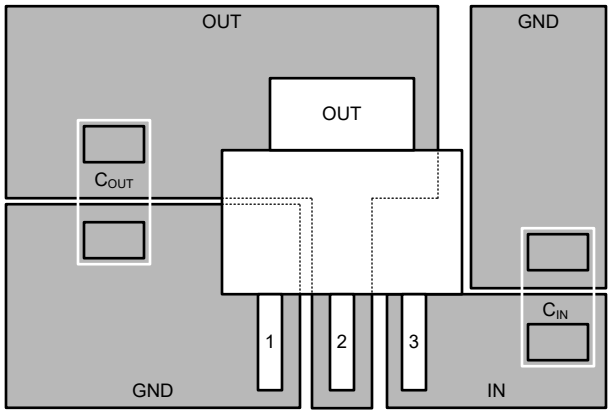


图 7-9. Layout Example for DCY (SOT-223) Package

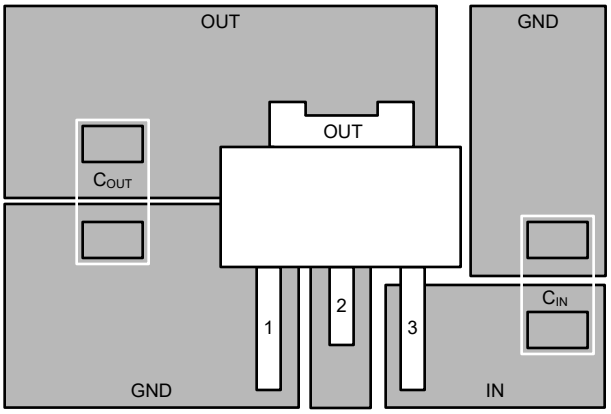


图 7-10. Layout Example for KVU (TO-252) Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Available Options

PRODUCT(1) (2)	DESCRIPTION
TLV761 ***ab*xxxy**	***ab*** is the nominal output voltage, hexadecimal coding is used. • ***a*** is used for the unit level of the output voltage. • ***b*** is used for the tenth level of the output voltage. For example, use 33 for 3.3V, A0 for 10.0V, C0 for 12.0V, and D0 for 13.0V. **xxx** is the package designator. **y** is the package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) The device is available in factory-programmable fixed output voltage increments of 50mV upon request.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TLV1117 Adjustable and Fixed Low-Dropout Voltage Regulator* data sheet
- Texas Instruments, *LM1117 800-mA Low-Dropout Linear Regulator* data sheet

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

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8.6 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (April 2024) to Revision D (May 2025)	Page
• 将 KVU 状态从*预发布*更改为*量产数据*	1
• 将最大输入电压范围 (V_{IN}) 从 *16V* 改为 *18V*	1
• 更改了*特性*中的*输出精度*要点	1
• Added *Application Curves* section	16
• Changed *Available Options* table	19

Changes from Revision B (February 2023) to Revision C (April 2024)	Page
• 向文档中添加了 KVU (TO-252) 封装作为*预告信息*	1
• Added KVU package information to *Pin Configuration and Functions* section	3
• Increased absolute maximum ratings to 20V for Input pin	4
• Added thermal numbers for KVU (TO-252) package	5
• Changed output voltage value from *5 V* to *3.3 V* in *Design Parameters* table	16
• Added *Layout Example for KVU (TO-252) Package* image to *Layout Examples* section	18

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTLV76118DCYR	Obsolete	Preproduction	SOT-223 (DCY) | 4	-	-	Call TI	Call TI	-40 to 125	
TLV76112DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76112C
TLV76112DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76112C
TLV76118DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76118C
TLV76118DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76118C
TLV76125DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76125C
TLV76125DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76125C
TLV76130DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76130C
TLV76130DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76130C
TLV76133DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76133C
TLV76133DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76133C
TLV76133KVUR	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TLV76133
TLV76133KVUR.A	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TLV76133
TLV76136DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76136C
TLV76136DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76136C
TLV76150DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76150C
TLV76150DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76150C
TLV76150KVUR	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TLV76150
TLV76150KVUR.A	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TLV76150
TLV76180DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76180C
TLV76180DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	76180C
TLV761C0DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	761C0C
TLV761C0DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	761C0C
TLV761C0KVUR	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TLV761C0
TLV761C0KVUR.A	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TLV761C0

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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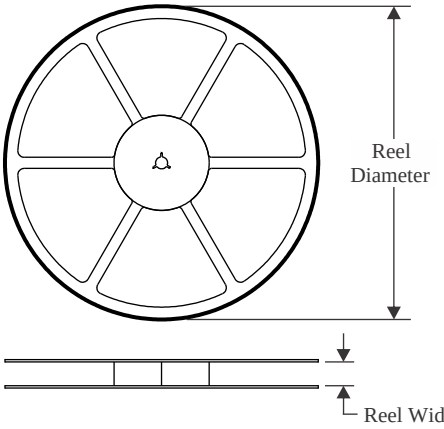
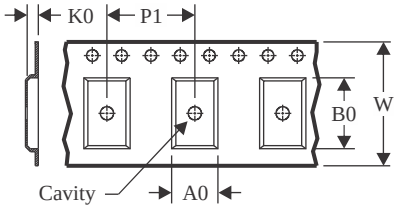
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

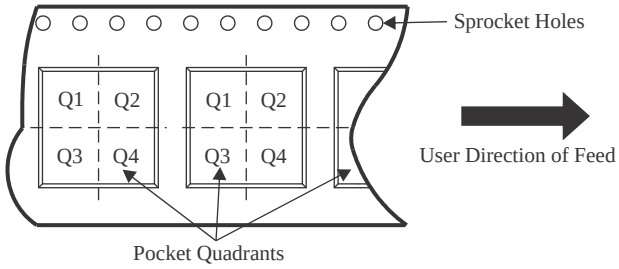


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

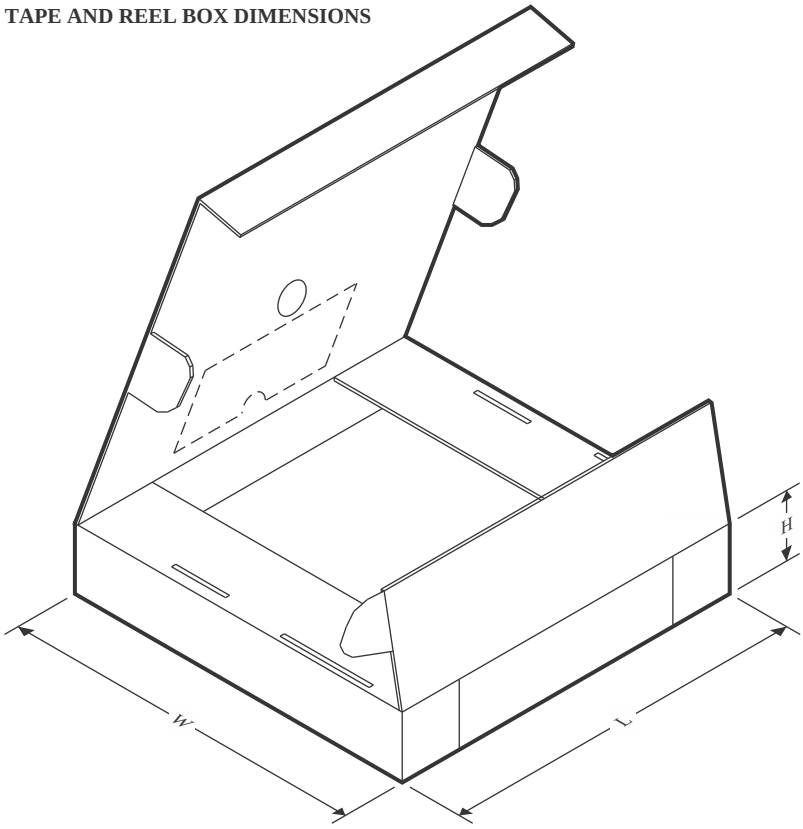
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV76112DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76118DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76125DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76130DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76133DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76133KVUR	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV76136DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76150DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76150KVUR	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV76180DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV761C0DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV761C0KVUR	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

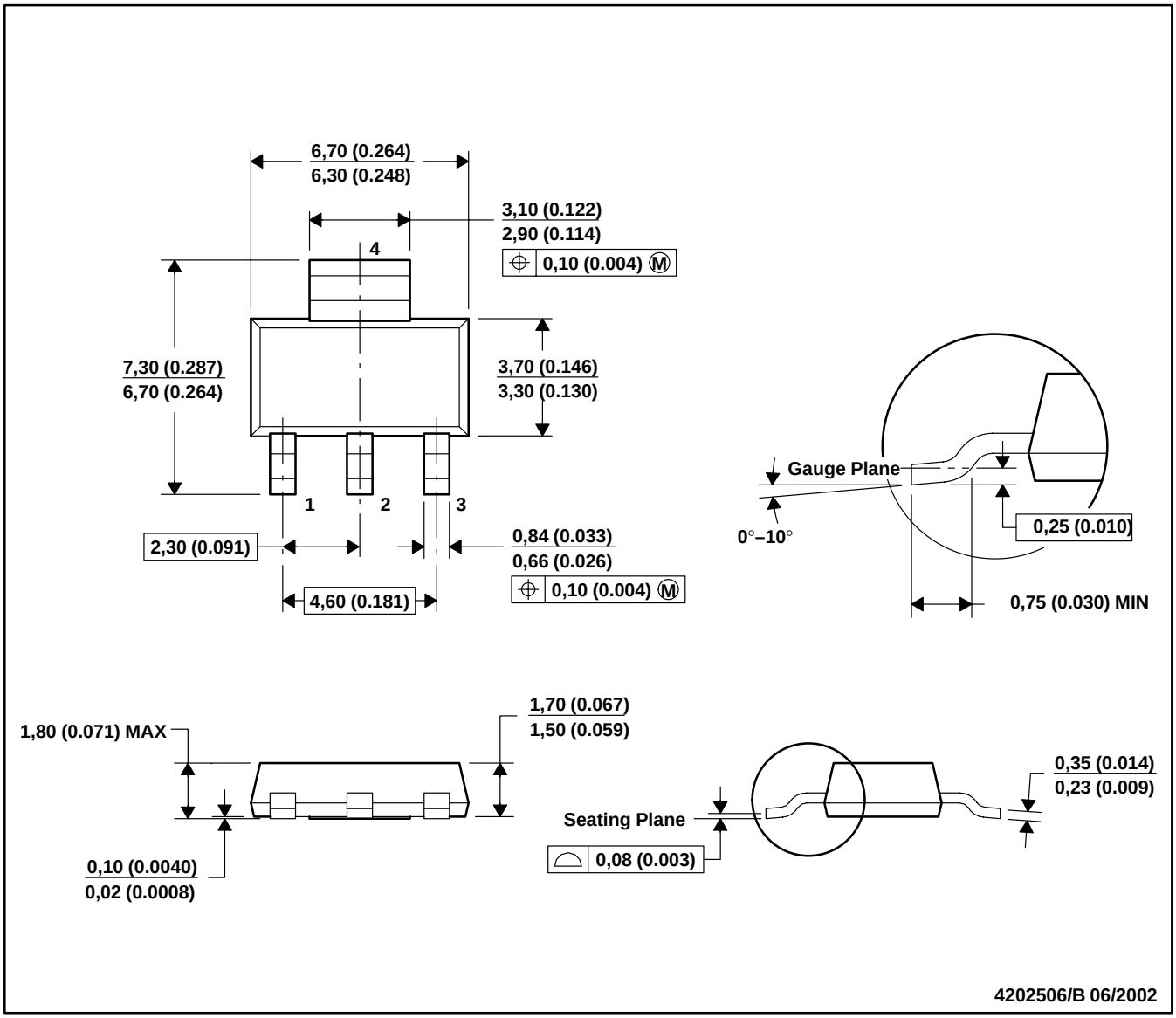


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV76112DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76118DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76125DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76130DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76133DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76133KVUR	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV76136DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76150DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76150KVUR	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV76180DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV761C0DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV761C0KVUR	TO-252	KVU	3	2500	340.0	340.0	38.0

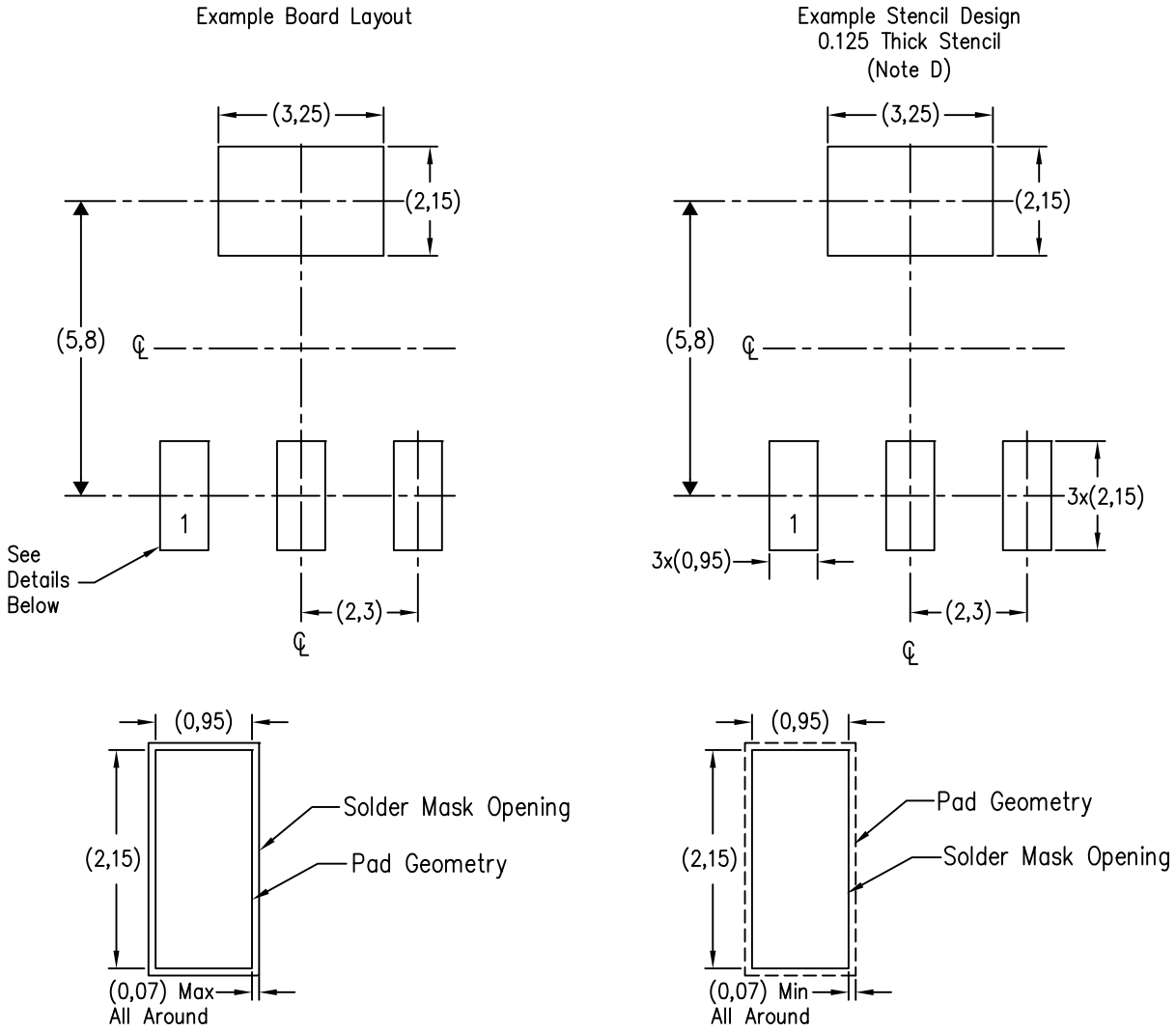
MPDS094A – APRIL 2001 – REVISED JUNE 2002

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



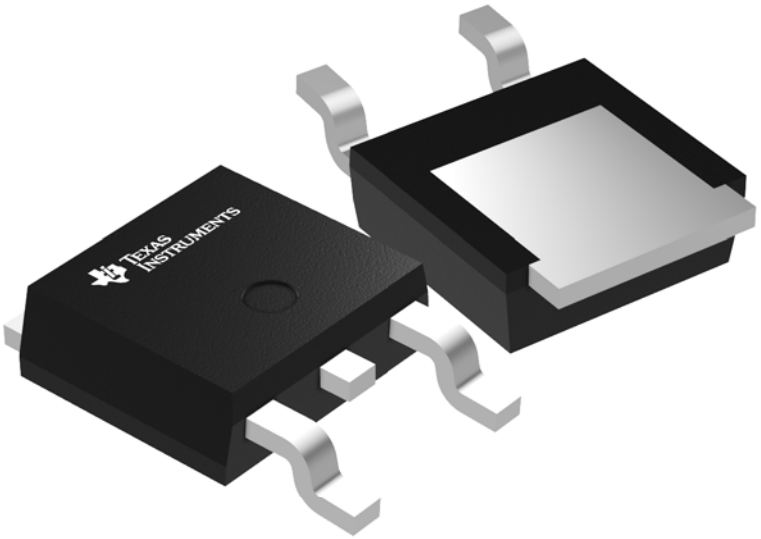
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

KVU 3

TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



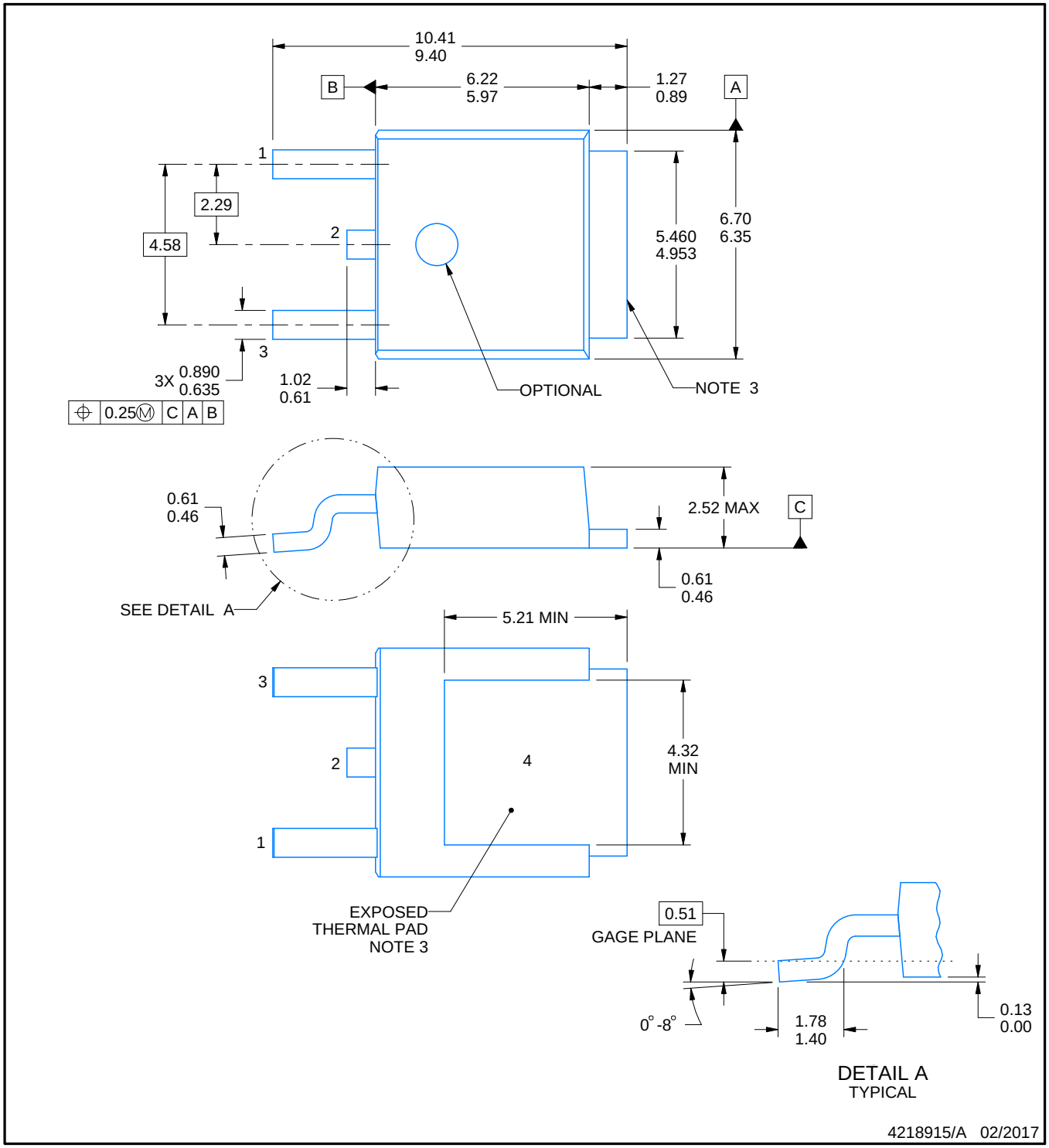
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

KVU0003A

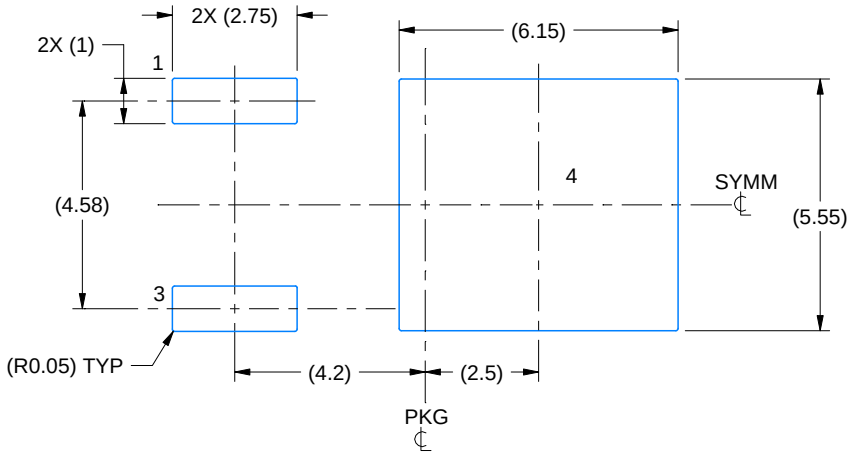
TO-252 - 2.52 mm max height

TO-252

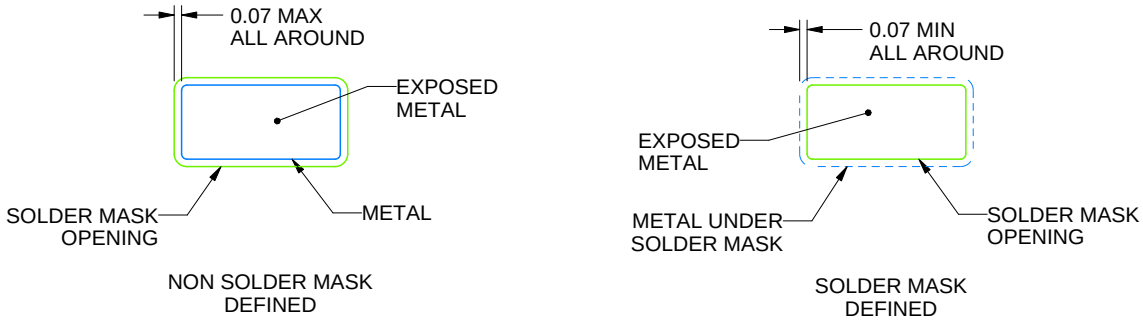


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

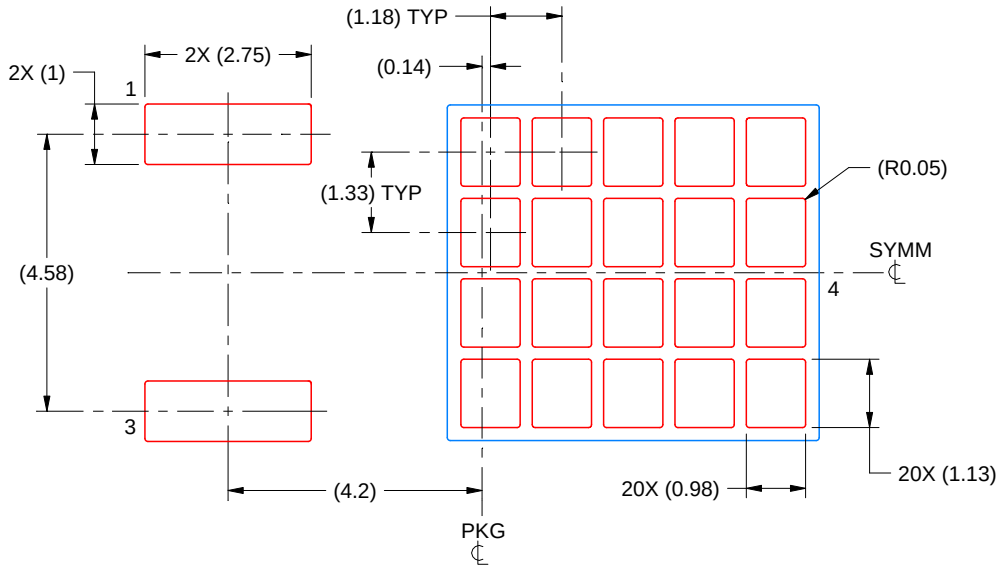
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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