TLV700xx-Q1 汽车类，300mA，低 I_Q，低压降稳压器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 器件温度等级 1：–40°C 至 125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 H2
  - 器件 CDM ESD 分类等级 C3B
- 2% 的精度
- 低 I_Q：35 µA
- 固定输出电压：1.2V 和 1.8V
- 高 PSRR：1kHz 时为 68dB
- 可在采用 0.1 µF 的有效电容时保持稳定(1)
- 如要了解热关断和过流保护功能，[1]

2 应用

- 汽车主机单元
- 摄像头传感器和模块
- 抬头显示屏 (HUD)
- 远程信息处理控制单元

3 说明

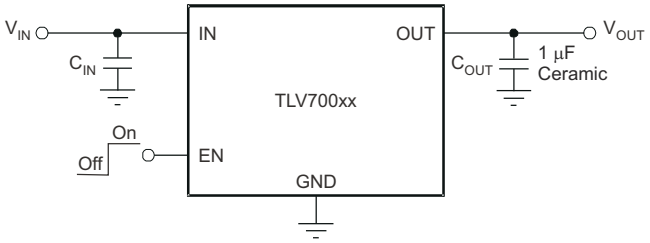
TLV70018-Q1 和 TLV70012-Q1 低压降 (LDO) 线性稳压器是具有出色线路和负载瞬态性能的低静态电流器件。高精度带隙与误差放大器支持 2% 的总精度。低输出噪声、高电源抑制比 (PSRR) 和低压降电压使得该系列器件成为为功耗敏感型负载供电的理想选择。所有器件版本均具有热关断和电流限制功能，用于检测故障情况。

此外，即使有效输出电容仅为 0.1 µF，这些器件也可稳定运行。凭借这一特性，可以使用具有更高偏置电压和温度降额的经济实惠的电容器。这些器件在没有负载的情况下可调节至指定的精度。

封装信息

器件型号	封装(1)	封装尺寸(2)
TLV70018-Q1	DDC（SOT，5）	2.9mm × 2.8mm
TLV70012-Q1		

(1) 如需更多信息，请参阅*机械、封装和可订购信息*。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



典型应用

[1] 请参阅*输入和输出电容器要求*。

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4 Pin Configuration and Functions

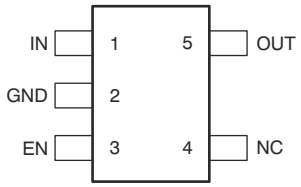


图 4-1. DDC Package, 5-Pin SOT (Top View)

表 4-1. Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	IN	Input pin. A small 1 µF ceramic capacitor is recommended from this pin to ground to provide stability and good transient performance.(1)
2	GND	Ground pin
3	EN	Enable pin. Driving EN over 0.9V turns on the regulator. Driving EN below 0.4V puts the regulator into shutdown mode and reduces operating current to 1 µA, nominal.
4	NC	No connection. This pin can be tied to ground to improve thermal dissipation.
5	OUT	Regulated output voltage pin. A small 1 µF ceramic capacitor is needed from this pin to ground to provide stability.(1)

(1) See the *Input and Output Capacitor Requirements* section for more details.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	6.0	V
	EN	–0.3	6.0	V
	OUT	–0.3	6.0	V
Current (source)	OUT	Internally limited		
Output short-circuit duration		Indefinite		
Operating virtual junction, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	2000	V
		Charged-device model (CDM), per AEC Q100-011	750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range, unless otherwise noted.

			MIN	MAX	UNIT
V_{IN}	Input voltage	IN	2	5.5	V
V_{EN}	Enable voltage	EN	0	5.5	V
V_{OUT}	Output voltage	OUT	0	1.8	V
I_{OUT}	Current output		0	300	mA
T_J	Operating junction temperature		–40	150	°C

5.4 Thermal Information

THERMAL METRIC(1)		TLV70018-Q1, TLV70012-Q1	UNIT
		DDC (SOT)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	262.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

at V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 2V (whichever is greater); I_{OUT} = 10mA, V_{EN} = 0.9V, C_{OUT} = 1.0 μF, and T_A = –40°C to 125°C (unless otherwise noted); typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2		5.5	V
V_{OUT}	DC output accuracy	–40°C ≤ T_A ≤ 125°C	–2%	0.5%	2%	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 10mA		1	5	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0mA ≤ I_{OUT} ≤ 300mA, TLV70018-Q1		1	15	mV
		0mA ≤ I_{OUT} ≤ 300mA, TLV70012-Q1		1	20	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	320	500	860	mA
I_{GND}	Ground pin current	I_{OUT} = 0mA		35	55	μA
		I_{OUT} = 300mA, V_{IN} = V_{OUT} + 0.5V		370		μA
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4V, V_{IN} = 2.0V		400		nA
		V_{EN} ≤ 0.4V, 2.0V ≤ V_{IN} ≤ 4.5V, T_A = –40°C to 85°C		1	2	μA
		V_{EN} ≤ 0.4V, 2.0V ≤ V_{IN} ≤ 4.5V, T_A = 85°C to 125°C		1	2.5	μA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3V, V_{OUT} = 1.8V, I_{OUT} = 10mA, f = 1kHz		68		dB
V_n	Output noise voltage	BW = 100Hz to 100kHz, V_{IN} = 2.3V, V_{OUT} = 1.8V, I_{OUT} = 10mA		48		μV_{RMS}
t_{STR}	Startup time(1)	C_{OUT} = 1.0 μF, I_{OUT} = 300mA		100		μs
$V_{EN(HI)}$	Enable pin high (enabled)		0.9		V_{IN}	V
$V_{EN(LO)}$	Enable pin low (disabled)		0		0.4	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 5.5V		0.04		μA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		145		°C
T_A	Operating temperature		–40		125	°C

(1) Startup time = time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

5.6 Typical Characteristics

over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 2V, whichever is greater; I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF (unless otherwise noted); typical values are at T_J = 25°C

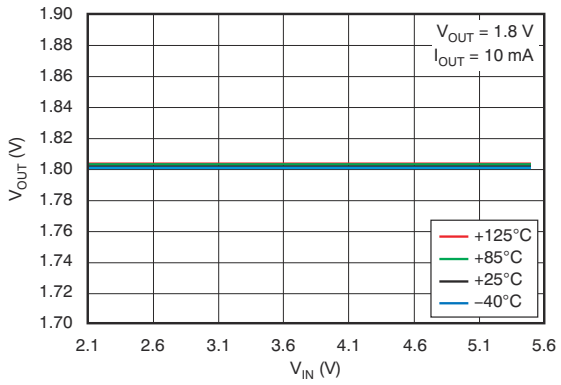


图 5-1. Line Regulation 10mA

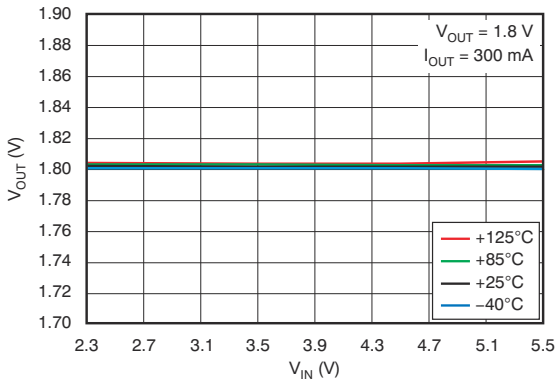


图 5-2. Line Regulation 300mA

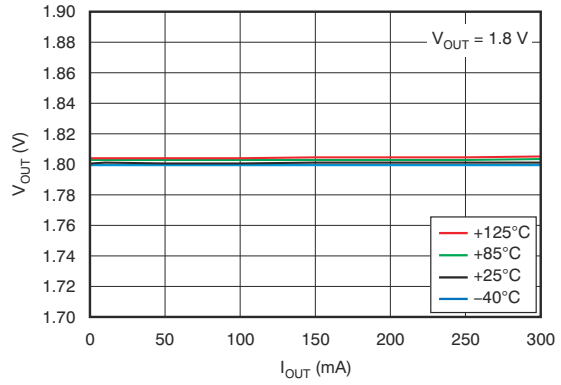


图 5-3. Load Regulation

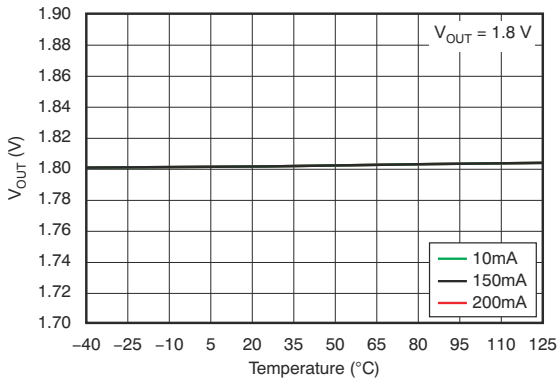


图 5-4. Output Voltage vs Temperature

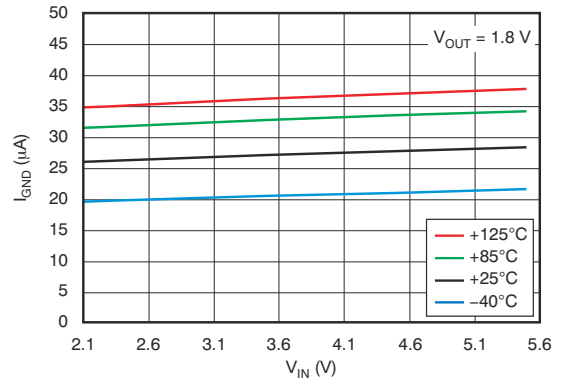


图 5-5. Ground Pin Current vs Input Voltage

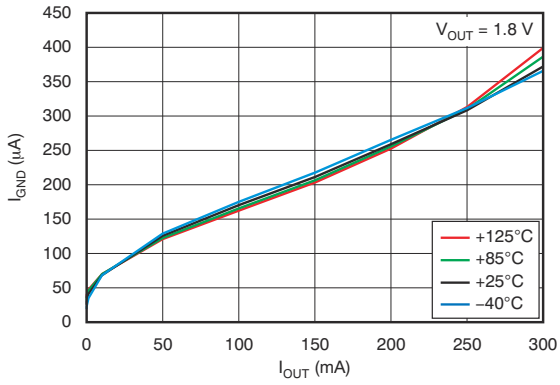


图 5-6. Ground Pin Current vs Load

5.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 2V, whichever is greater; I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 μF (unless otherwise noted); typical values are at T_J = 25°C

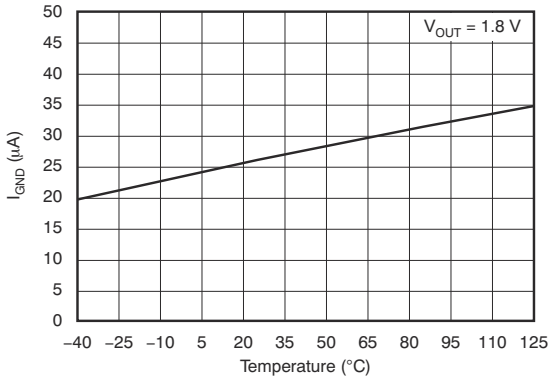


图 5-7. Ground Pin Current vs Temperature

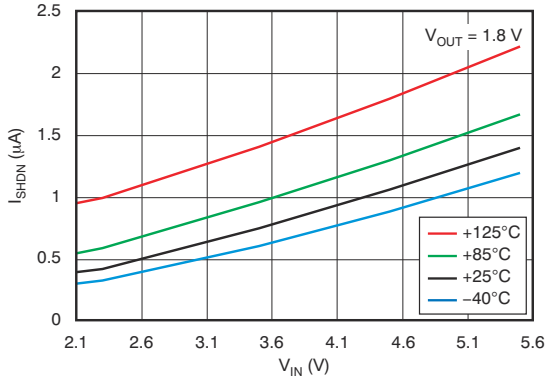


图 5-8. Shutdown Current vs Input Voltage

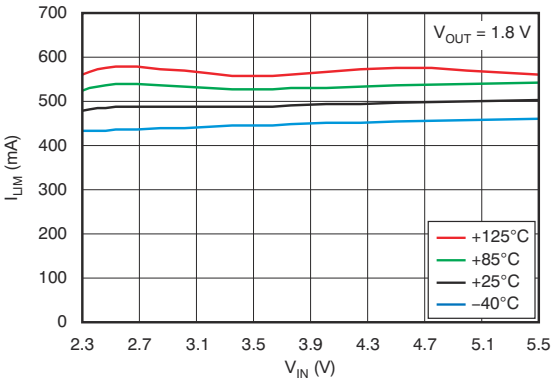


图 5-9. Current Limit vs Input Voltage

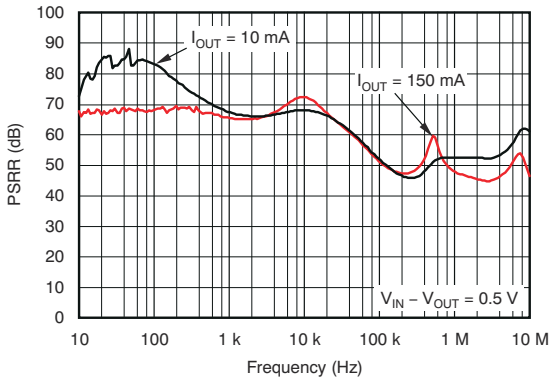


图 5-10. Power-Supply Ripple Rejection vs Frequency

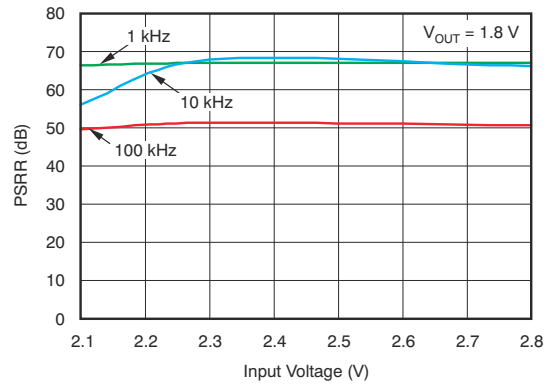


图 5-11. Power-Supply Ripple Rejection vs Input Voltage

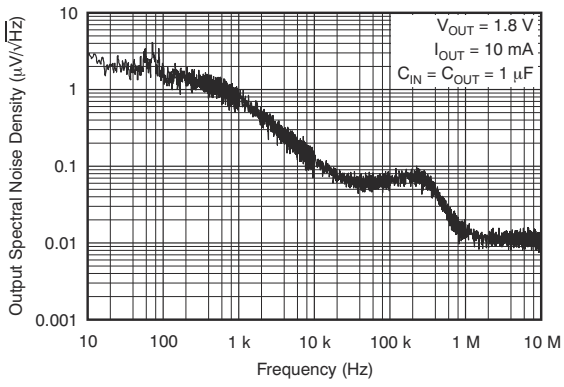


图 5-12. Output Spectral Noise Density vs Frequency

5.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 2V, whichever is greater; I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF (unless otherwise noted); typical values are at T_J = 25°C

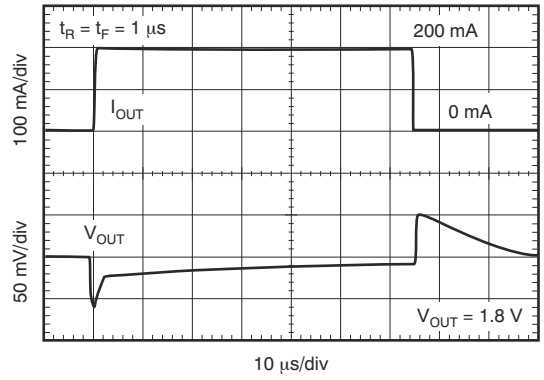


图 5-13. Load Transient Response

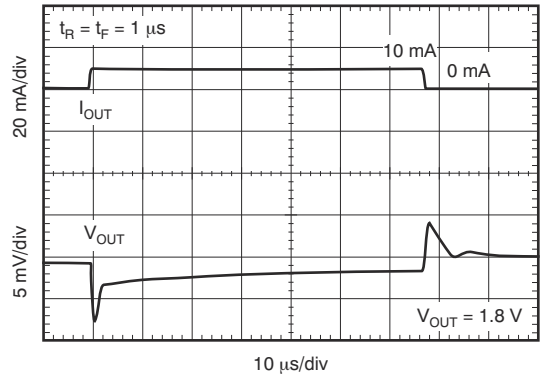


图 5-14. Load Transient Response

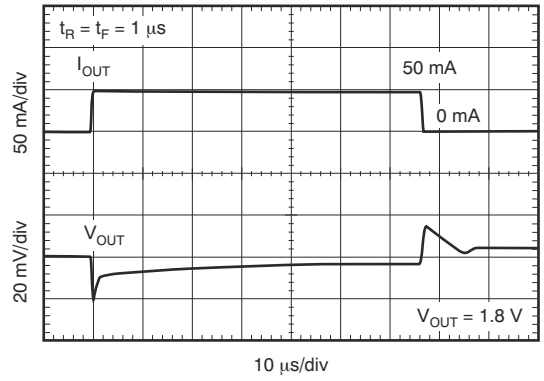


图 5-15. Load Transient Response

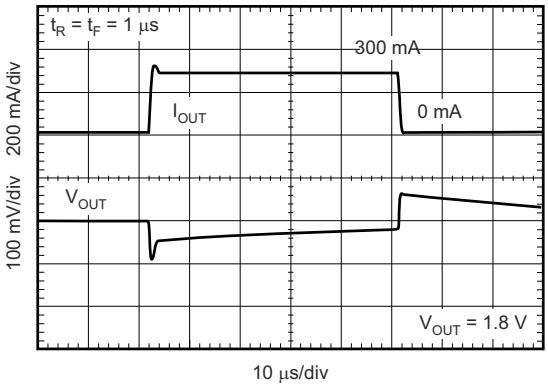


图 5-16. Load Transient Response

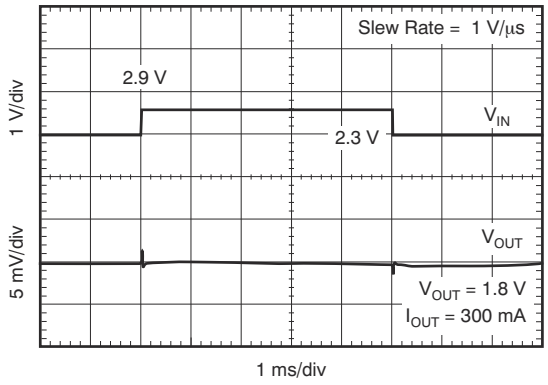


图 5-17. Line Transient Response

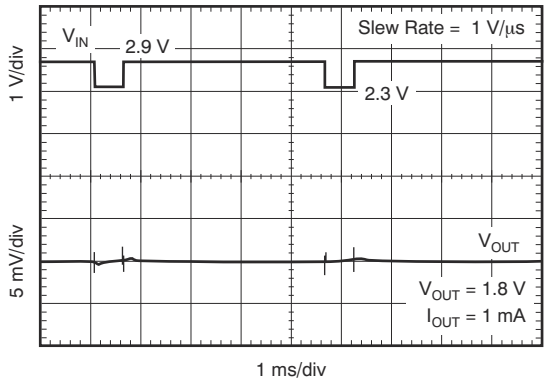


图 5-18. Line Transient Response

5.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 2V, whichever is greater; I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF (unless otherwise noted); typical values are at T_J = 25°C

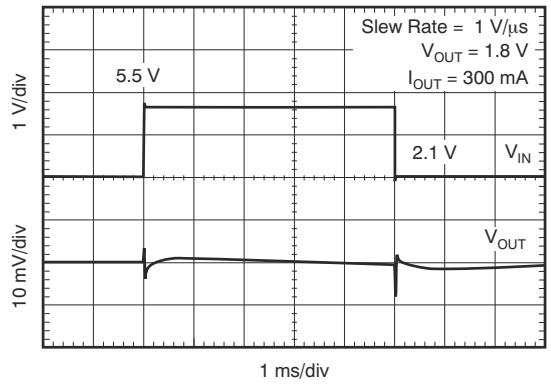


图 5-19. Line Transient Response

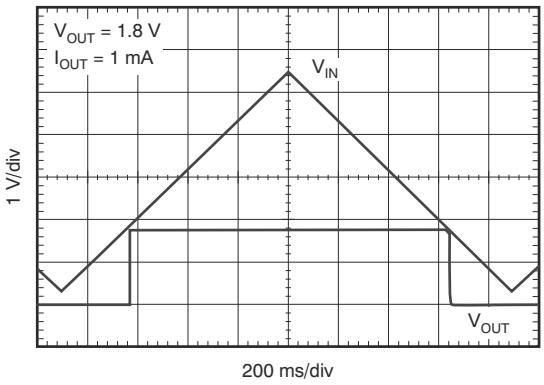


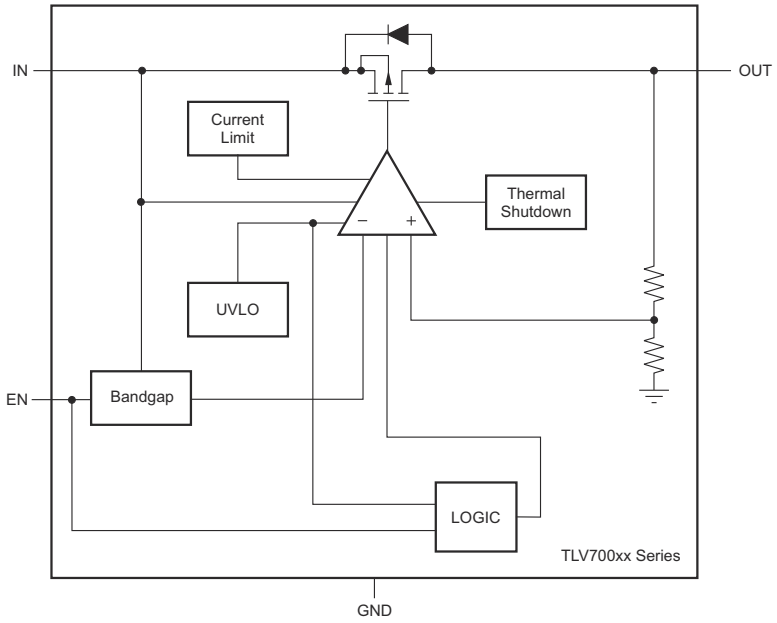
图 5-20. V_{IN} Ramp-Up, Ramp-Down Response

6 Detailed Description

6.1 Overview

The TLV70018-Q1 and TLV70012-Q1 low-dropout (LDO) linear regulators are low-quiescent-current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy together with low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Internal Current Limit

The TLV70018-Q1 and TLV70012-Q1 internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} - V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device turns off. As the device cools, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Considerations* section for more details.

The PMOS pass transistor in the TLV70018-Q1 and TLV70012-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

6.3.2 Dropout Voltage

The TLV70018-Q1 and TLV70012-Q1 use a PMOS pass transistor to achieve low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass transistor. V_{DO} scales approximately with output current because the PMOS transistor behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as $(V_{IN} - V_{OUT})$ approaches dropout. 图 5-11 illustrates this effect.

6.3.3 Undervoltage Lockout (UVLO)

The TLV70018-Q1 and TLV70012-Q1 use an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly.

6.3.4 Thermal Shutdown

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 40°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV70018-Q1 and TLV70012-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV70018-Q1 or TLV70012-Q1 into thermal shutdown degrades device reliability.

6.4 Device Functional Modes

6.4.1 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at EN pin goes above 0.9V. This relatively lower value of voltage required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO logic 1 voltage level is lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4V. When shutdown capability is not required, EN can be connected to the IN pin.

6.4.2 Operation with V_{IN} Less than 2V

The TLV70018-Q1 and TLV70012-Q1 devices operate with input voltages above 2V. The typical UVLO voltage is 1.9V and the device operates at an input voltage above 2V. When input voltage falls below UVLO voltage, the device will shutdown.

6.4.3 Operation with V_{IN} Greater than 2V

When V_{IN} is greater than 2V, if input voltage is higher than desired output voltage plus dropout voltage, the output voltage is equal to the desired value. Otherwise, output voltage will be V_{IN} minus dropout voltage.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The TLV70018-Q1 and TLV70012-Q1 consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for portable RF applications. This family of regulators offers current limit and thermal protection, and is specified from –40°C to 125°C.

7.2 Typical Application

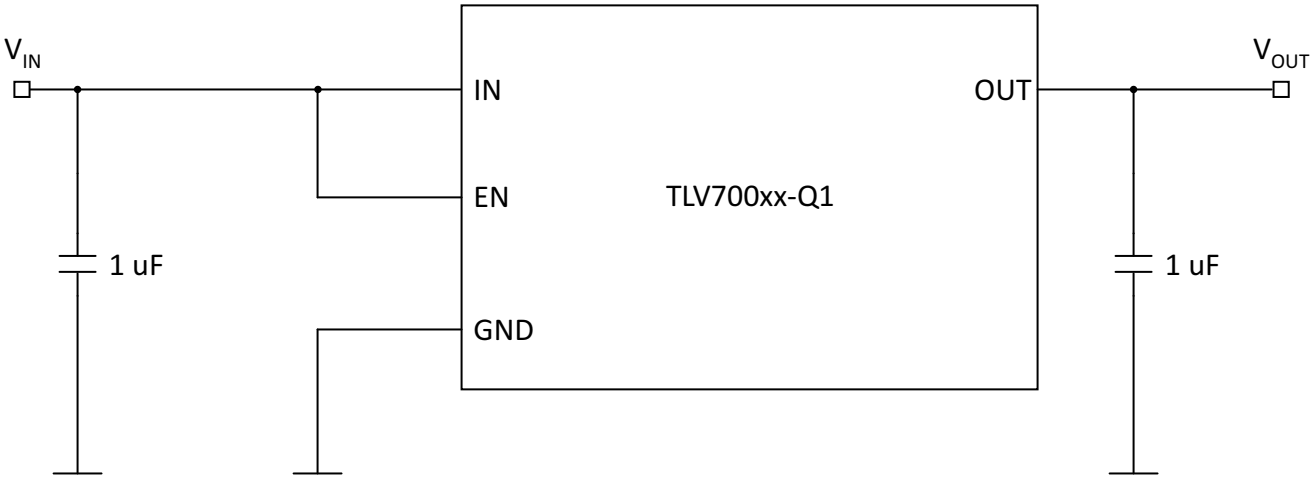


图 7-1. Simplified Schematic

7.2.1 Design Requirements

For this design example use, the parameters listed in 表 7-1 as the input parameters.

表 7-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	2V to 5.5V
Output voltage	1.2V, 1.8V
Output current rating	300mA
Effective output capacitor range	>0.1μF
Maximum output capacitor ESR range	<200mΩ

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Requirements

1.0 µF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV70018-Q1 and TLV70012-Q1 are designed to be stable with an *effective capacitance* of 0.1 µF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of lower-cost dielectrics, this capability of being stable with 0.1 µF effective capacitance also enables the use of smaller-footprint capacitors that have higher derating in size- and space-constrained applications.

备注

Using a 0.1 µF rated capacitor at the output of the LDO does not provide stability because the effective capacitance under the specified operating conditions would be less than 0.1 µF. Maximum ESR should be less than 200mΩ.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1 µF to 1.0 µF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2Ω, a 0.1 µF input capacitor may be necessary to ensure stability.

7.2.2.2 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot or undershoot magnitude but increases the duration of the transient response.

7.2.3 Application Curve

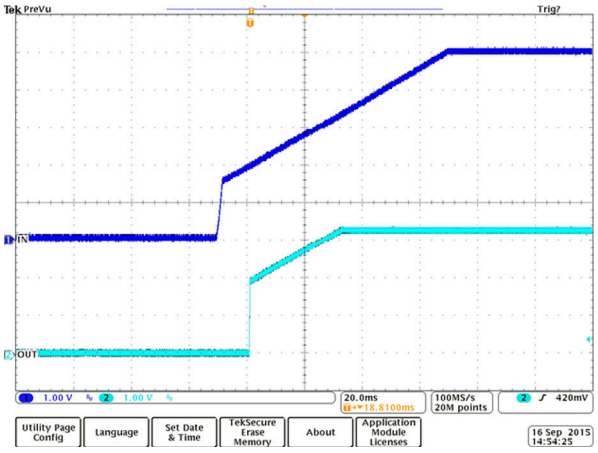


图 7-2. Power-Up

7.3 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 2V and 5.5V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, TI recommends adding a capacitor with a value of 0.1µF and a ceramic bypass capacitor at the input.

7.4 Layout

7.4.1 Layout Guidelines

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, the board is recommended to be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

7.4.1.1 Thermal Considerations

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum.

To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

7.4.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Thermal performance data for TLV70018-Q1 and TLV70012-Q1 were gathered using the TLV700 evaluation module (EVM), a 2-layer board with two ounces of copper per side. Corresponding thermal performance data are given in *Thermal Information*. Note that this board has provision for soldering not only the SOT23-5 package on the bottom layer, but also the SC-70 package on the top layer. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

7.4.1.2.1 Thermal Calculations

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass transistor, as shown in 方程式 1.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN} \quad (1)$$

where

- P_D is continuous power dissipation
- I_{OUT} is output current
- V_{IN} is input voltage
- V_{OUT} is output voltage

Because I_Q << I_{OUT}, the term $I_Q \times V_{IN}$ is always ignored.

For a device under operation at a given ambient air temperature (T_A), use 方程式 2 to calculate the junction temperature (T_J).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (2)$$

where:

- $Z_{\theta JA}$ is the junction-to-ambient air temperature thermal impedance

Use 方程式 3 to calculate the rise in junction temperature due to power dissipation.

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (3)$$

For a given maximum junction temperature ($T_{J(MAX)}$), use 方程式 4 to calculate the maximum ambient air temperature ($T_{A(MAX)}$) at which the device can operate.

$$T_{Amax} = T_{Jmax} - (R_{\theta JA} \times P_D) \quad (4)$$

7.4.2 Layout Example

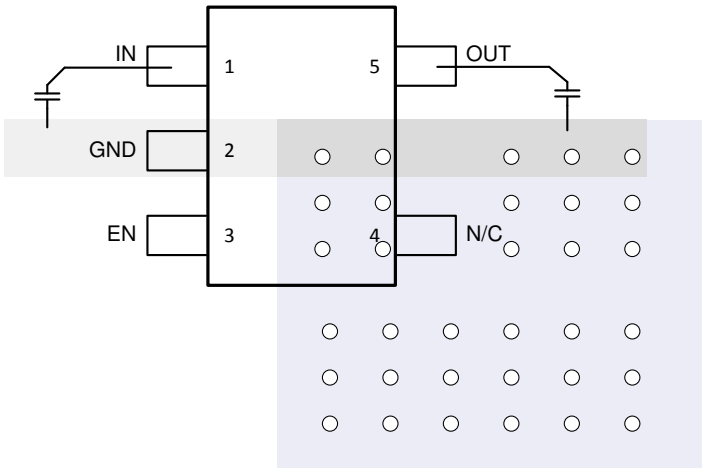


图 7-3. TLV700xx-Q1 Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT(1)	DESCRIPTION
TLV700**xxQyyyzQ1**	**xx** is the nominal output voltage (for example, 28 = 2.8V). **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **yyy** is the package designator. **z** is the tape and reel quantity (R = 3000, T = 250). **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

8.1.2 Package Mounting

Solder pad footprint recommendations for the TLV70018-Q1 are available from the Texas Instruments web site at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, TLV700 evaluation module

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.5 Trademarks

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8.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (June 2017) to Revision D (January 2025) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- Added *Device Nomenclature* table 15

Changes from Revision B (January 2016) to Revision C (June 2017) **Page**

- 将*固定输出电压*特性要点从*可能的固定输出电压组合为 1.2V 至 4.8V* 更改为*固定输出电压：1.2V 和 1.8V* 1
- 更改了*应用*部分 1
- 修改了“*说明*”部分的第一段：将“*TLV700xx-Q1 系列*”更改为“*TLV70018-Q1 和 TLV70012-Q1*”，删除了第二句，将“*多种电池供电的手持设备*”更改为“*为功耗敏感型负载供电*”，并将“*安全性*”更改为“*检测故障情况*” 1
- 从*典型应用*标题下删除了*固定电压*版本 1
- Changed *Input voltage* parameter: changed symbol from V_I to V_{IN}, moved EN and OUT rows to standalone parameters 3
- Changed maximum specification of *Output voltage* parameter from 5.5V to 1.8V 3
- Added I_{OUT} symbol to *Current output* parameter 3
- Deleted TLV70018-Q1 column from *Thermal Information* table 3
- Added TLV70018-Q1 to TLV70012-Q1 column in *Thermal Information* table; all thermal values for TLV70018-Q1 changed to the TLV70012-Q1 thermal values 3
- Changed $V_{OUT(TYP)}$ to $V_{OUT(NOM)}$ in conditions statement of *Electrical Characteristics* table 4
- Changed symbols for *Line regulation*, *Load regulation*, and *Output noise voltage* parameters from $\Delta V_O/\Delta V_{IN}$ to $\Delta V_{OUT}/\Delta V_{IN}$, $\Delta V_O/\Delta I_{OUT}$ to $\Delta V_{OUT}/\Delta I_{OUT}$, and V_N to V_n (respectively) in *Electrical Characteristics* table 4
- Changed $V_{OUT(TYP)}$ to $V_{OUT(NOM)}$ in *Typical Characteristics* conditions statement 5
- Deleted *Dropout Voltage vs Input Voltage* and *Dropout Voltage vs Output Current* curves 5
- Changed *TLV700xx-Q1* to *TLV70018-Q1 and TLV70012-Q1* in *Overview* section 9
- Added *TLV70012-Q1* to sub-sections of *Feature Description* and *Device Functional Modes* sections 9
- Changed 160°C to 165°C, 140°C to 145°C, and 35°C to 40°C in *Thermal Shutdown* section 10
- Changed *Application Information* section: changed first two sentences, deleted second paragraph 11
- Changed *Example Value* column values for 2nd and 3rd rows in Design Parameters table 11
- Added TLV70012-Q1 to *Input and Output Capacitor Requirements* section 12
- Deleted first and last paragraphs from *Thermal Considerations* section 13
- Deleted second sentence from second paragraph of *Power Dissipation* section 13
- Added TLV70012-Q1 to *Power Dissipation* section 13

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV70012QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDO
TLV70012QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDO
TLV70012QDDCRQ1.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDO
TLV70018QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAL
TLV70018QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAL
TLV70018QDDCRQ1.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

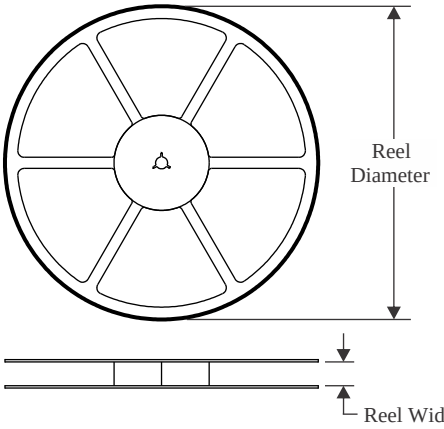
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

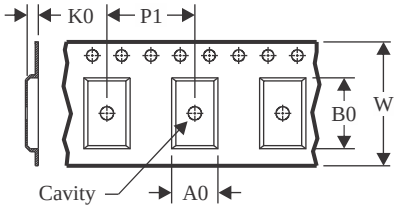
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

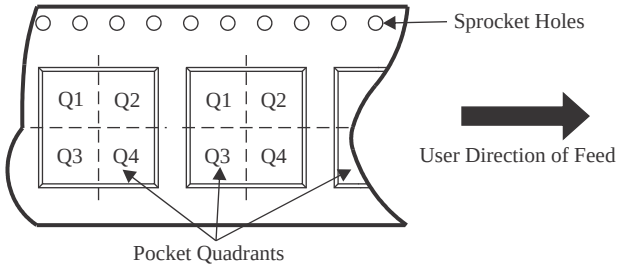


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

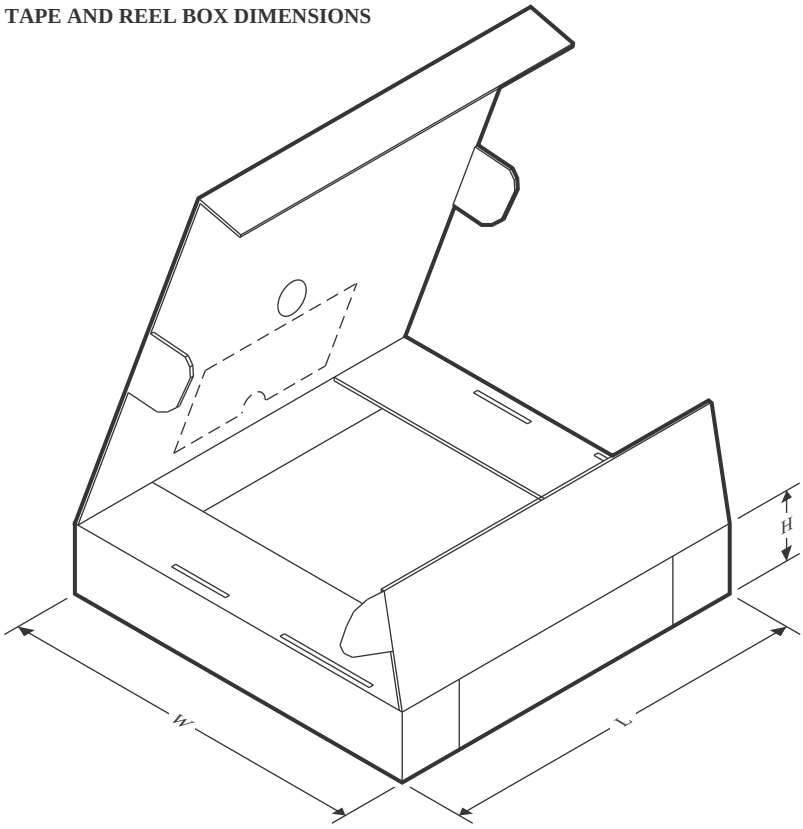
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70012QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70018QDDCRQ1	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

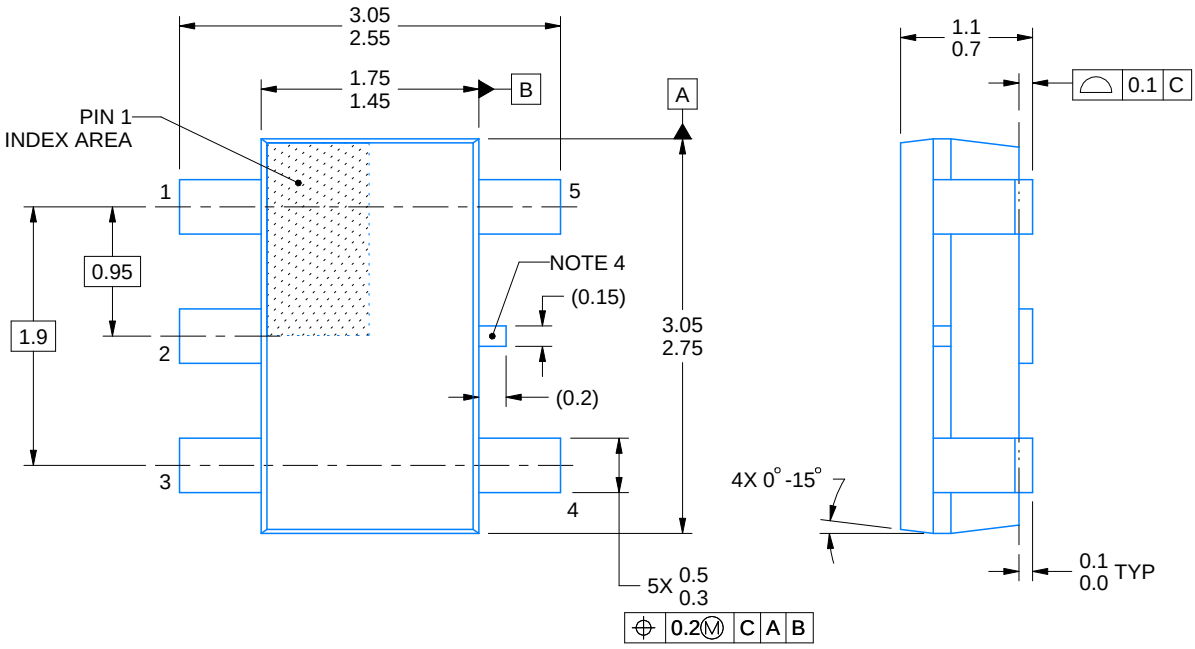
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70012QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TLV70018QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0

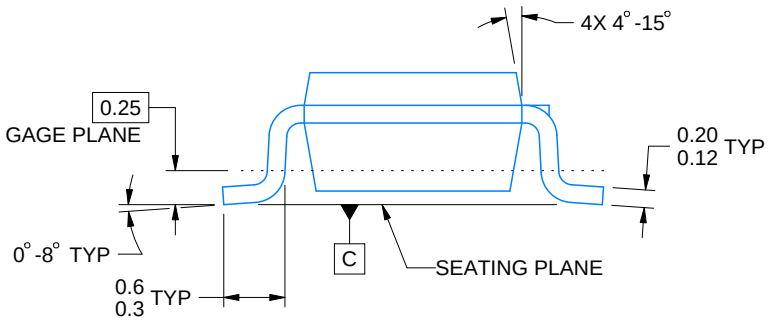
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR





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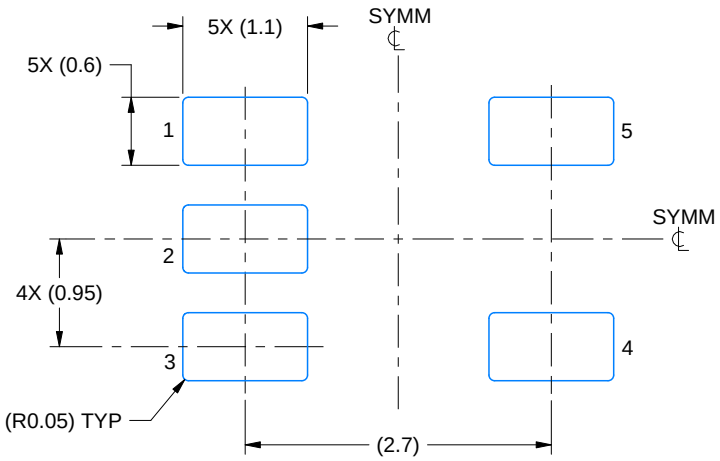
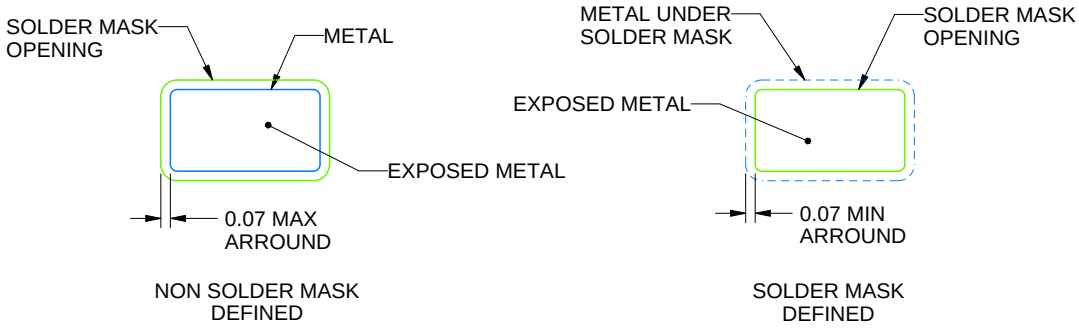
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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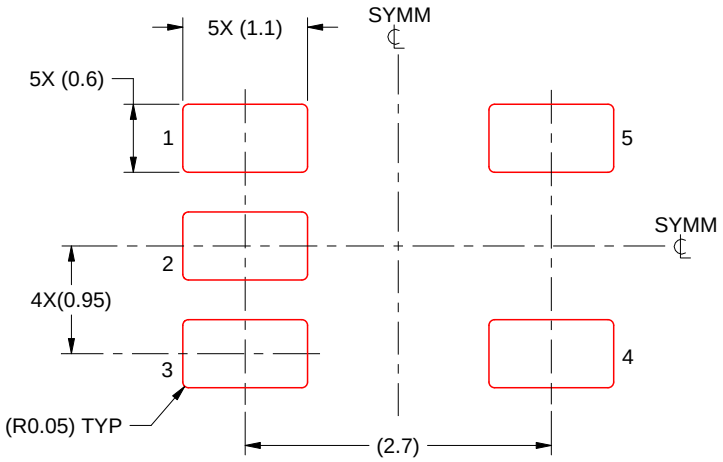
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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