具有 400mV 基准电压的 TLV6710 微功耗、36V 窗口比较器

1 特性

- 高电源电压范围：1.8V 至 36V
- 可调节阈值：低至 400mV
- 高阈值精度：
  - 0.25%（典型值）
  - 在工作温度范围内最大值为 0.75%
- 低静态电流：7μA（典型值）
- 漏极开路输出
- 内部滞后：5.5mV（典型值）
- 温度范围：-40°C 至 125°C
- 封装：超薄 SOT-23-6

2 应用

- 笔记本电脑和平板电脑
- 智能手机
- 数码相机
- 视频游戏控制器
- 中继器和断路器
- 便携式医疗设备
- 门窗传感器
- 便携式和电池供电类产品

3 说明

TLV6710 是一款高电压窗口比较器，工作电压范围为 1.8V 至 36V。此器件具有两个内部基准电压为 400mV 的高精度比较器和两个额定电压为 25V 的开漏输出 TLV6710 可以作为一个窗口比较器使用，也可以作为两个独立的比较器使用。可以使用外部电阻器设定监控电压。

当 INA+ 上的电压下降至低于 (V_{ITP} - V_{HYS})时，OUTA 被驱动至低电平，当电压返回到相应阈值 (V_{ITP}) 之上时，OUTA 变为高电平。当 INB- 上的电压上升至高于 V_{ITP}时，OUTB 被驱动至低电平，当电压下降至低于相应阈值 (V_{ITP} - V_{HYS}) 时，OUTB 变为高电平。TLV6710 中的两个比较器都具有内置迟滞来抑制短时毛刺脉冲，确保稳定的输出运行，不会引起误触发。

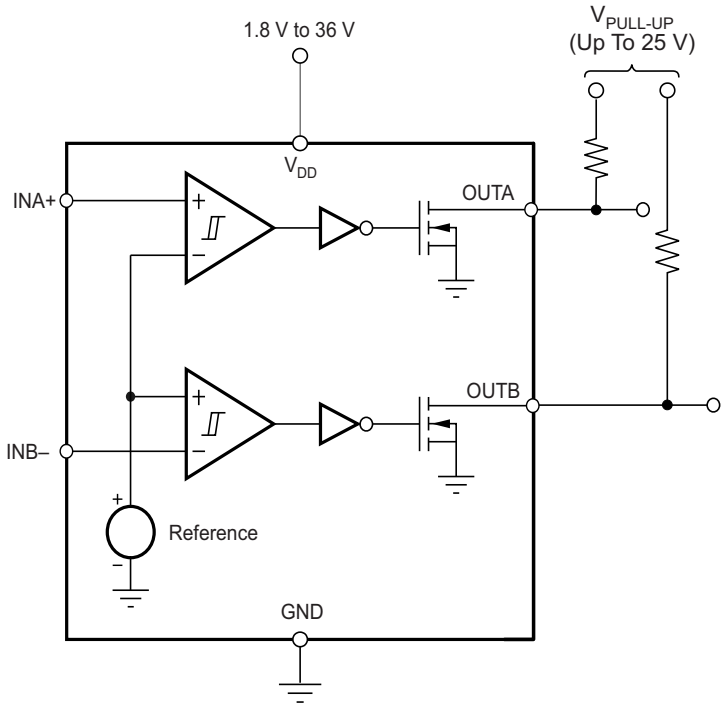
TLV6710 采用薄型 SOT-23-6 封装，额定结温范围为 –40°C 至 125°C。

器件信息(1)

器件编号	封装	封装尺寸（标称值）
TLV6710	SOT-23 (6)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

简化框图



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4 修订历史记录

Changes from Revision A (April 2018) to Revision B **Page**

- 将首页上 简化方框图、说明和应用信息部分的 输出 说明文字 从 36V 更改为 25V。 ... 1

Changes from Original (January 2018) to Revision A **Page**

- 将“预告信息”更改为“生产数据” ... 1

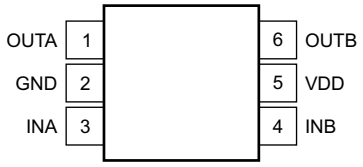
5 器件比较表

表 **1. TLV67xx** 集成比较器系列

器件编号	配置	工作电压范围	整个温度范围内的精度阈值
TLV6700	窗口	1.8V 至 18V	1%
TLV6703	同相单通道	1.8V 至 18V	1%
TLV6710	窗口	1.8V 至 36V	0.75%
TLV6713	同相单通道	1.8V 至 36V	0.75%

6 Pin Configuration and Functions

DDC Package
SOT-6
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Ground
INA	3	I	Comparator A input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage $V_{IT–(INA)}$, OUTA is driven low.
INB	4	I	Comparator B input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage $V_{IT+(INB)}$, OUTB is driven low.
OUTA	1	O	INA comparator open-drain output. OUTA is driven low when the voltage at this comparator is less than $V_{IT–(INA)}$. The output goes high when the sense voltage rises above $V_{IT+(INA)}$.
OUTB	6	O	INB comparator open-drain output. OUTB is driven low when the voltage at this comparator exceeds $V_{IT+(INB)}$. The output goes high when the sense voltage falls below $V_{IT–(INB)}$.
VDD	5	I	Supply voltage input. Connect a 1.8-V to 36-V supply to VDD to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating junction temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage(2)	V_{DD}	–0.3	+40	V
	V_{OUTA}, V_{OUTB}	–0.3	+28	V
	V_{INA}, V_{INB}	–0.3	+7	V
Current	Output pin current		40	mA
Temperature	Operating junction, T_J	–40	+125	°C
	Storage temperature, T_{stg}	–65	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.8		36	V
V_{INA}, V_{INB}	Input pin voltage	0		1.7	V
V_{OUTA}, V_{OUTB}	Output pin voltage	0		25	V
I_{OUTA}, I_{OUTB}	Output pin current	0		10	mA
T_J	Junction temperature	–40	+25	+125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TLV6710 DDC (SOT) 6 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	201.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to +125°C, 1.8 V ≤ V_{DD} < 36 V, and pullup resistors $RP_{1,2}$ = 100 kΩ, unless otherwise noted. Typical values are at T_J = 25°C and V_{DD} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		1.8		36	V
$V_{(POR)}$	Power-on reset voltage(1)	V_{OL} ≤ 0.2 V			0.8	V
$V_{IT–(INA)}$	INA pin negative input threshold voltage	V_{DD} = 1.8 V to 36 V	397	400	403	mV
$V_{IT+(INA)}$	INA pin positive input threshold voltage	V_{DD} = 1.8 V to 36 V	400	405.5	413	mV
$V_{HYS(INA)}$	INA pin hysteresis voltage ($HYS = V_{IT+(INA)} – V_{IT–(INA)}$)		2	5.5	12	mV
$V_{IT–(INB)}$	INB pin negative input threshold voltage	V_{DD} = 1.8 V to 36 V	387	394.5	400	mV
$V_{IT+(INB)}$	INB pin positive input threshold voltage	V_{DD} = 1.8 V to 36 V	397	400	403	mV
$V_{HYS(INB)}$	INB pin hysteresis voltage ($HYS = V_{IT+(INB)} – V_{IT–(INB)}$)		2	5.2	12	mV
V_{OL}	Low-level output voltage	V_{DD} = 1.8 V, I_{OUT} = 3 mA		130	250	mV
		V_{DD} = 5 V, I_{OUT} = 5 mA		150	250	mV
I_{IN}	Input current (at INA, INB pins)	V_{DD} = 1.8 V and 36 V, V_{INA}, V_{INB} = 6.5 V	–25	+1	+25	nA
		V_{DD} = 1.8 V and 36 V, V_{INA}, V_{INB} = 0.1 V	–15	+1	+15	nA
$I_{D(leak)}$	Open-drain output leakage current	V_{DD} = 1.8 V and 36 V, V_{OUT} = 25 V		10	300	nA
I_{DD}	Supply current	V_{DD} = 1.8 V – 36 V		8	11	µA
UVLO	Undervoltage lockout(2)	V_{DD} falling	1.3	1.5	1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)}$ > 15 µs/V. If less than $V_{(POR)}$, the output is undetermined.
(2) When V_{DD} falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined if less than $V_{(POR)}$.

7.6 Timing Requirements

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay(1)	V_{DD} = 24 V, ±10-mV input overdrive, R_L = 100 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250 mV		9.9		µs
$t_{pd(LH)}$	Low-to-high propagation delay(1)	V_{DD} = 24 V, ±10-mV input overdrive, R_L = 100 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250 mV		28.1		µs
$t_{d(start)}$(2)	Startup delay	V_{DD} = 5 V		155		µs
t_r	Output rise time	V_{DD} = 12 V, 10-mV input overdrive, R_L = 100 kΩ, C_L = 10 pF, V_O = (0.1 to 0.9) × V_{DD}		2.7		µs
t_f	Output fall time	V_{DD} = 12 V, 10-mV input overdrive, R_L = 100 kΩ, C_L = 10 pF, V_O = (0.9 to 0.1) × V_{DD}		0.12		µs

(1) High-to-low and low-to-high refers to the transition at the input pins (INA and INB).
(2) During power on, V_{DD} must exceed 1.8 V for at least 150 µs (typ) before the output state reflects the input condition.

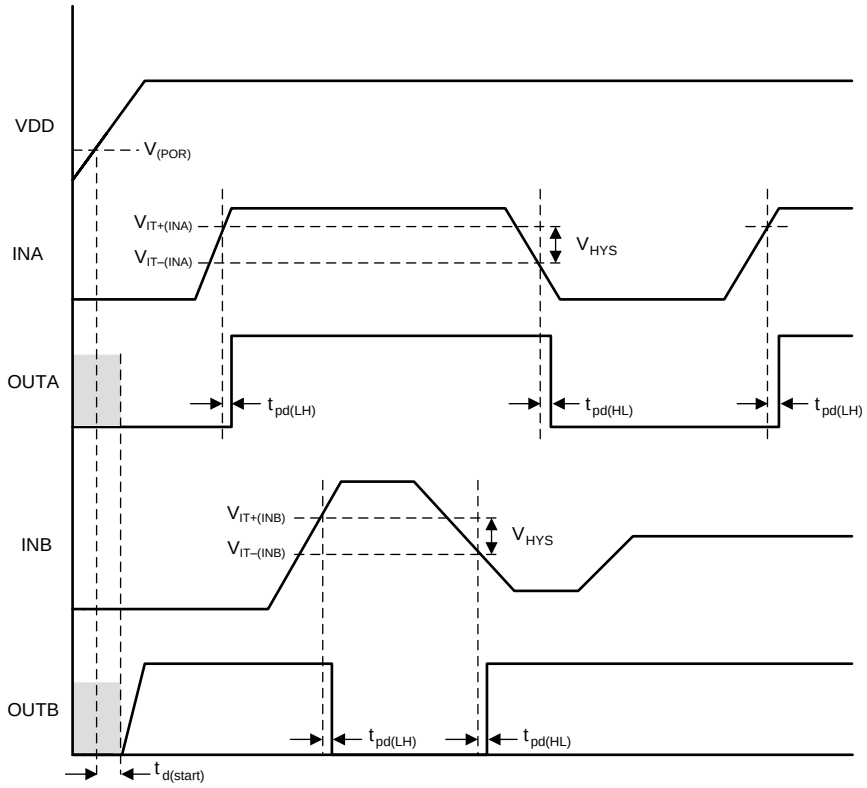


Figure 1. Timing Diagram

7.7 Typical Characteristics

At T_J = 25°C and V_{DD} = 12 V, unless otherwise noted.

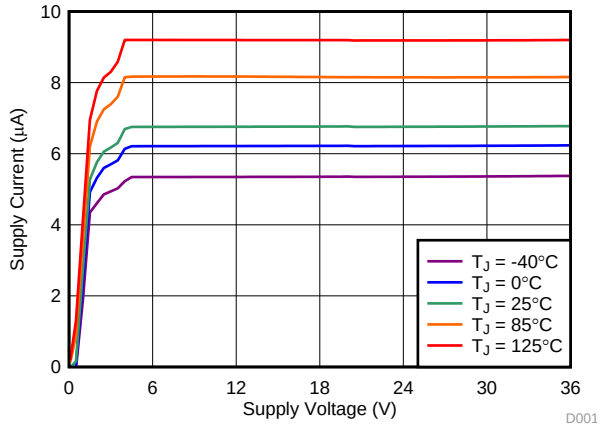
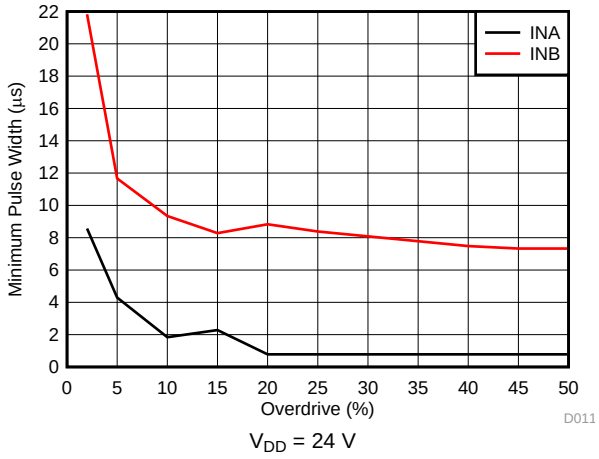


Figure 2. Supply Current vs Supply Voltage



V_{DD} = 24 V

Figure 3. Minimum Pulse Duration vs Threshold Overdrive Voltage(1) (1)

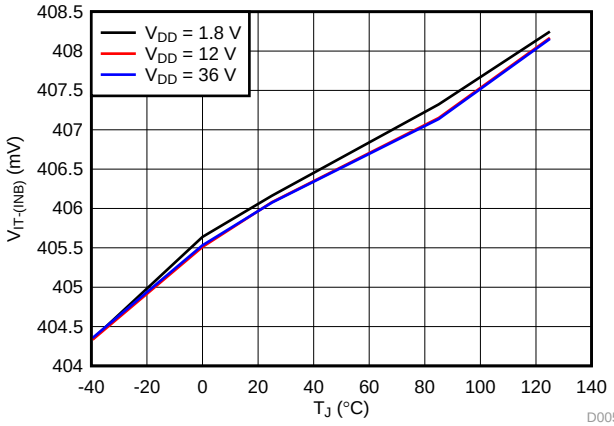


Figure 4. INA Positive Input Threshold Voltage ($V_{IT+(INA)}$) vs Temperature

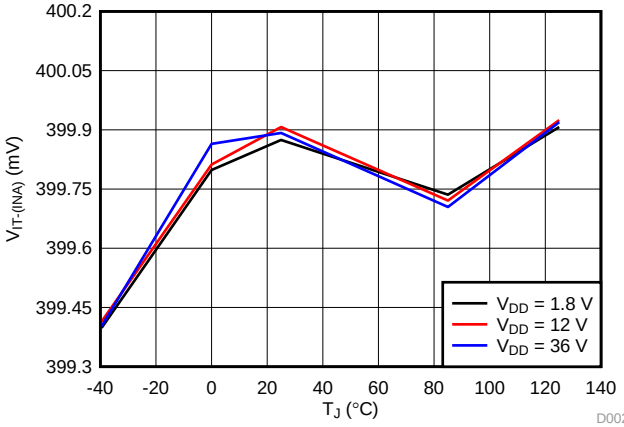


Figure 5. INA Negative Input Threshold Voltage ($V_{IT-(INA)}$) vs Temperature

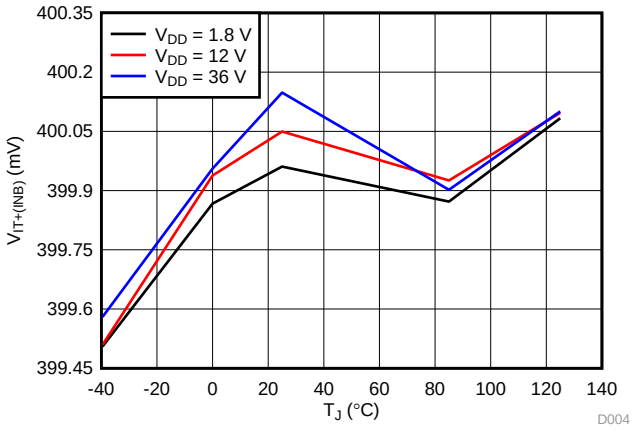


Figure 6. INB Positive Input Threshold Voltage ($V_{IT+(INB)}$) vs Temperature

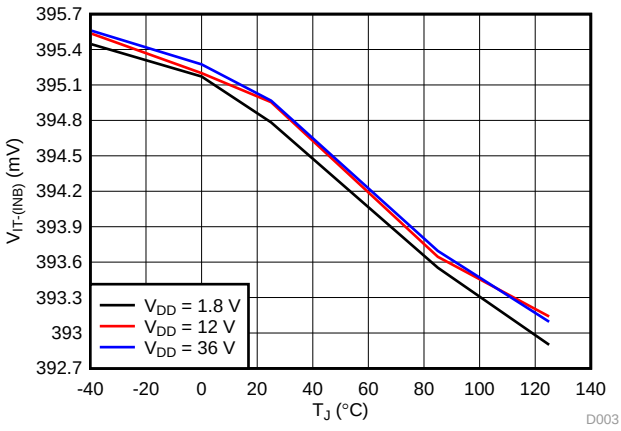


Figure 7. INB Negative Input Threshold Voltage ($V_{IT-(INB)}$) vs Temperature

(1) Minimum pulse duration required to trigger output high-to-low transition. INA = negative spike below V_{IT-} and INB = positive spike above V_{IT+}.

Typical Characteristics (continued)

At T_J = 25°C and V_{DD} = 12 V, unless otherwise noted.

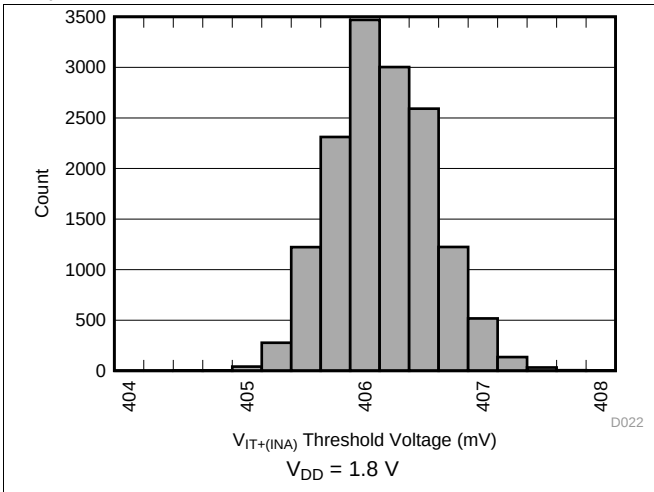


Figure 8. INA Positive Input Threshold Voltage ($V_{IT+(INA)}$) Distribution

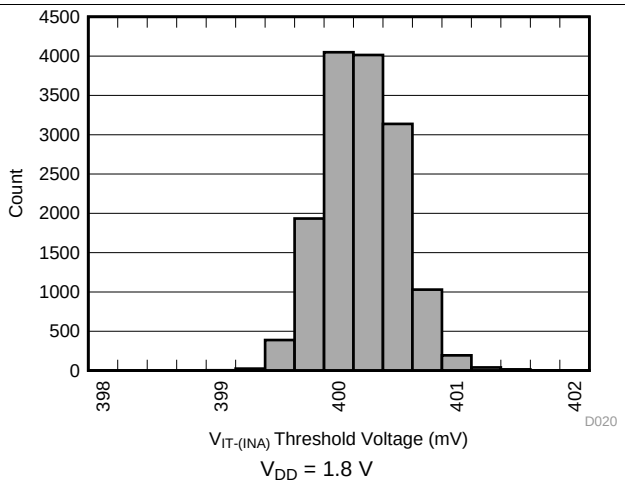


Figure 9. INA Negative Input Threshold Voltage ($V_{IT–(INA)}$) Distribution

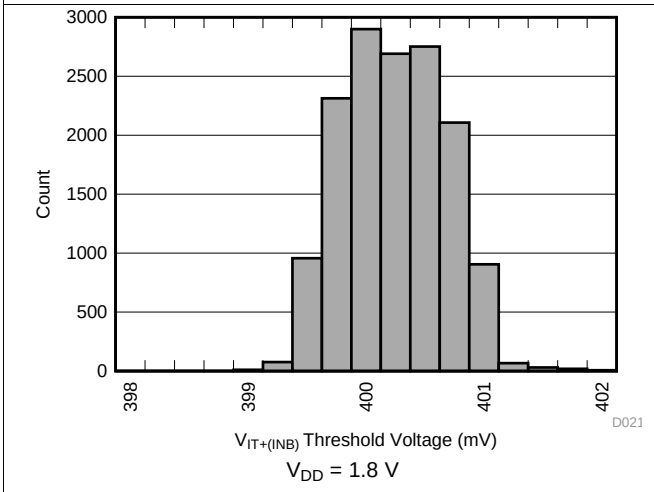


Figure 10. INB Positive Input Threshold Voltage ($V_{IT+(INB)}$) Distribution

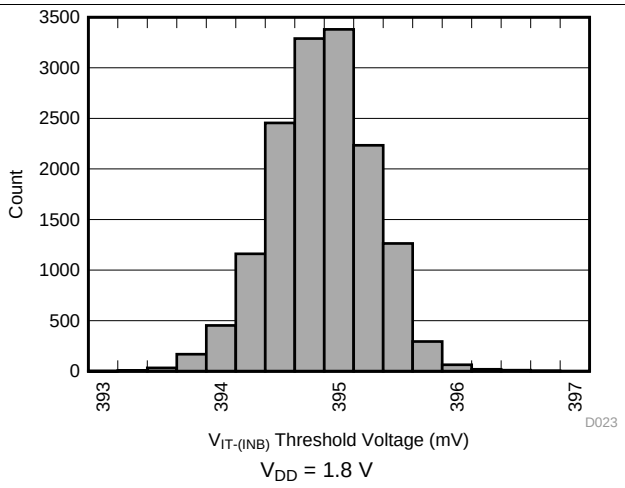


Figure 11. INB Negative Input Threshold Voltage ($V_{IT–(INB)}$) Distribution

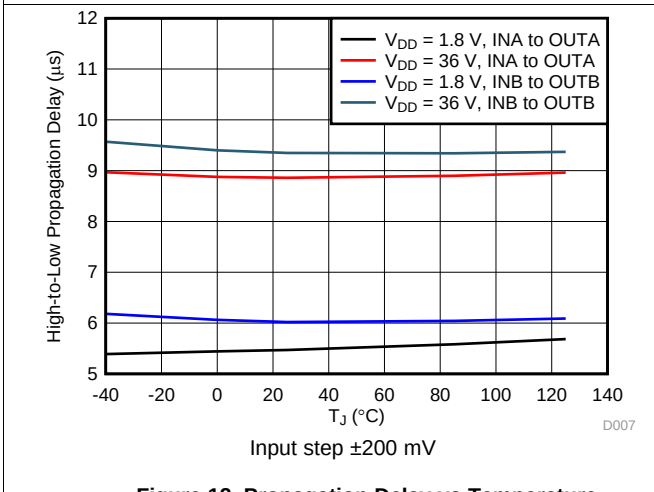


Figure 12. Propagation Delay vs Temperature (High-to-Low Transition at the Inputs)

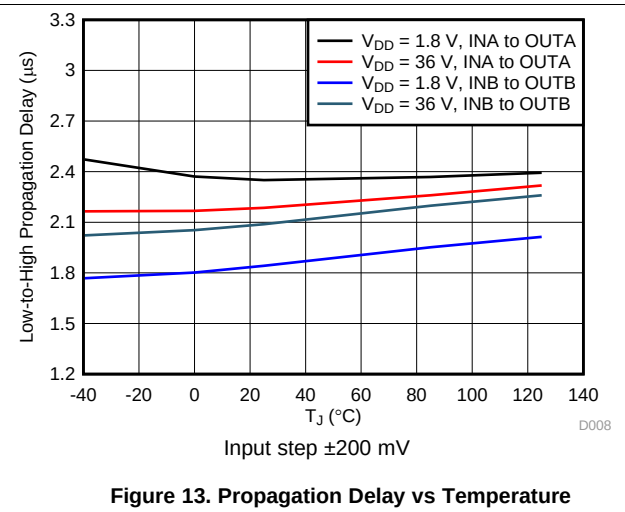


Figure 13. Propagation Delay vs Temperature (Low-to-High Transition at the Inputs)

Typical Characteristics (continued)

At T_J = 25°C and V_{DD} = 12 V, unless otherwise noted.

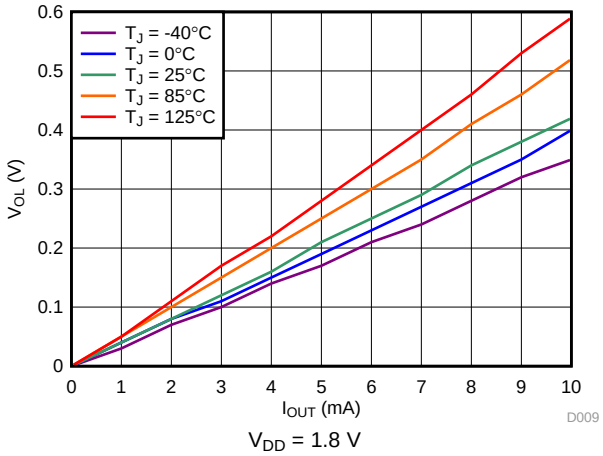


Figure 14. Output Voltage Low vs Output Sink Current

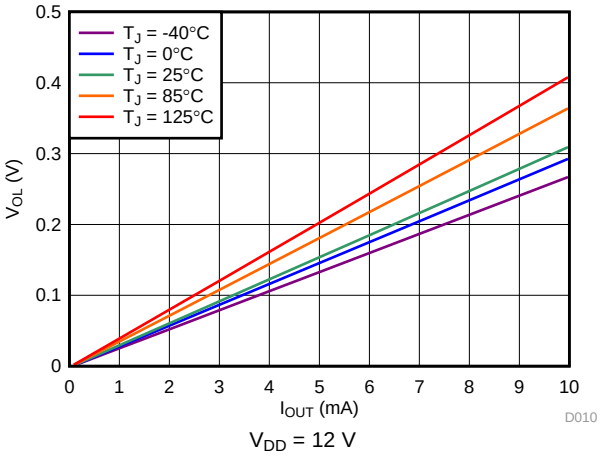


Figure 15. Output Voltage Low vs Output Sink Current

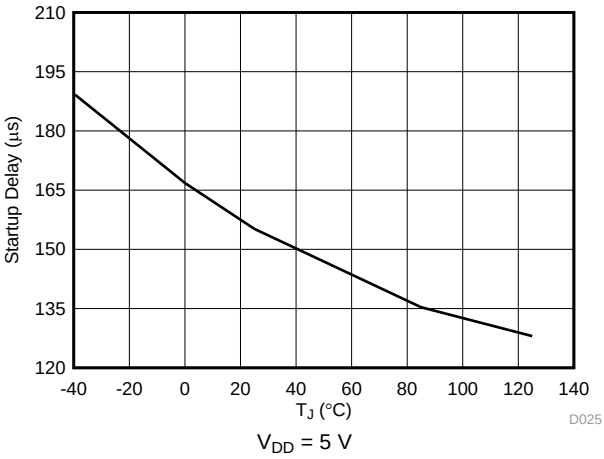


Figure 16. Start-Up Delay vs Temperature

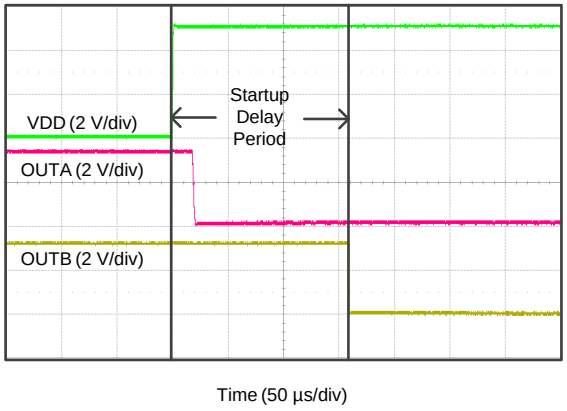


Figure 17. Start-Up Delay

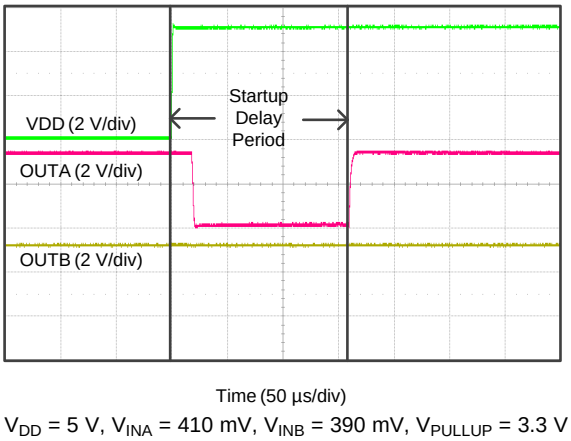


Figure 18. Start-Up Delay

8 Detailed Description

8.1 Overview

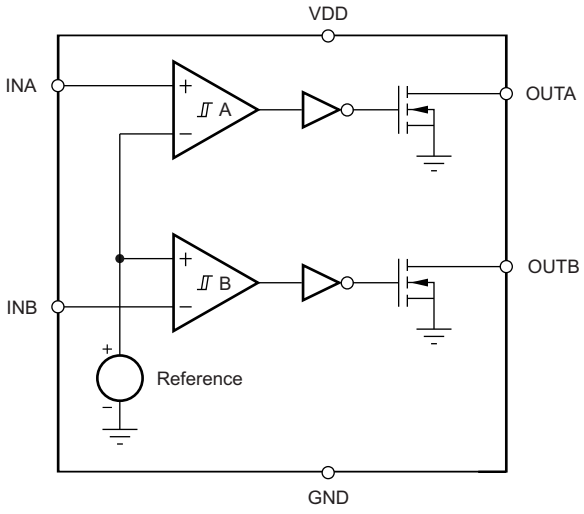
The TLV6710 combines two comparators (referred to as A and B) and a precision reference for overvoltage and undervoltage detection. The TLV6710 features a wide supply voltage range (1.8 V to 36 V) and high-accuracy window threshold voltages of 400 mV (0.75% over temperature) with built-in hysteresis. The outputs are rated to 25 V and can sink up to 10 mA.

Set each input pin (INA, INB) to monitor any voltage above 0.4 V by using an external resistor divider network. Each input pin has very low input leakage current, allowing the use of large resistor dividers without sacrificing system accuracy. To form a window comparator, use the two input pins and three resistors (see the *Window Comparator Considerations* section). In this configuration, the TLV6710 is designed to assert the output signals when the monitored voltage is within the window band. Each input can also be used independently. The relationship between the inputs and the outputs is shown in Table 2. Broad voltage thresholds are supported that enable the device to be used in a wide array of applications.

Table 2. Truth Table

CONDITION	OUTPUT	OUTPUT STATE
INA > $V_{IT+(INA)}$	OUTA high	Output A high impedance
INA < $V_{IT–(INA)}$	OUTA low	Output A sinking
INB > $V_{IT+(INB)}$	OUTB low	Output B sinking
INB < $V_{IT–(INB)}$	OUTB high	Output B high impedance

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Inputs (INA, INB)

The TLV6710 combines two comparators with a precision reference voltage. Each comparator has one external input; the other input is connected to the internal reference. The rising threshold on INB and the falling threshold on INA are designed and trimmed to be equal to the reference voltage (400 mV). This configuration optimizes the device accuracy when used as a window comparator. Both comparators also have built-in hysteresis that proves immunity to noise and ensures stable operation.

The comparator inputs swings from ground to 1.7 V (7.0 V absolute maximum), regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for noisy applications in order to reduce sensitivity to transient voltage changes on the monitored signal.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA voltage drops below $V_{IT-(INA)}$. When the voltage exceeds $V_{IT+(INA)}$, OUTA goes to a high-impedance state; see Figure 1.

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB exceeds $V_{IT+(INB)}$. When the voltage drops below $V_{IT-(INB)}$ OUTB goes to a high-impedance state; see Figure 1. Together, these two comparators form a window-detection function as described in the *Window Comparator Considerations* section.

8.3.2 Outputs (OUTA, OUTB)

In a typical TLV6710 application, the outputs are connected to a GPIO input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]).

The TLV6710 provides two open-drain outputs (OUTA and OUTB); use pullup resistors to hold these lines high when the output goes to a high-impedance state. Connect pullup resistors to the proper voltage rails to enable the outputs to be connected to other devices at correct interface voltage levels. The TLV6710 outputs can be pulled up to 25 V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by V_{OL}, output capacitive loading, and output leakage current ($I_{D(leak)}$). These values are specified in the *Electrical Characteristics* table. Use wired-OR logic to merge OUTA and OUTB into one logic signal.

Table 2 and the *Inputs (INA, INB)* section describe how the outputs are asserted or high impedance. See Figure 1 for a timing diagram that describes the relationship between threshold voltages and the respective output.

8.4 Device Functional Modes

8.4.1 Normal Operation (V_{DD} > UVLO)

When the voltage on VDD is greater than 1.8 V for at least 155 µs, the OUTA and OUTB signals correspond to the voltage on INA and INB as listed in Table 2.

8.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD} <$ UVLO)

When the voltage on VDD is less than the device UVLO voltage, and greater than the power-on reset voltage, $V_{(POR)}$, the OUTA and OUTB signals are asserted and high impedance, respectively, regardless of the voltage on INA and INB.

8.4.3 Power On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), both outputs are in a high-impedance state.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV6710 device is a wide-supply voltage window comparator that operates over a V_{DD} range of 1.8 V to 36 V. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 25 V for overvoltage and undervoltage detection. The device can be used either as a window comparator or as two independent voltage monitors. The monitored voltages are set with the use of external resistors.

9.1.1 Window Comparator Considerations

The inverting and noninverting configuration of the comparators forms a window-comparator detection circuit using a resistor divider network, as shown in Figure 19 and Figure 20. The input pins can monitor any system voltage above 400 mV with the use of a resistor divider network. INA and INB monitor for undervoltage and overvoltage conditions, respectively.

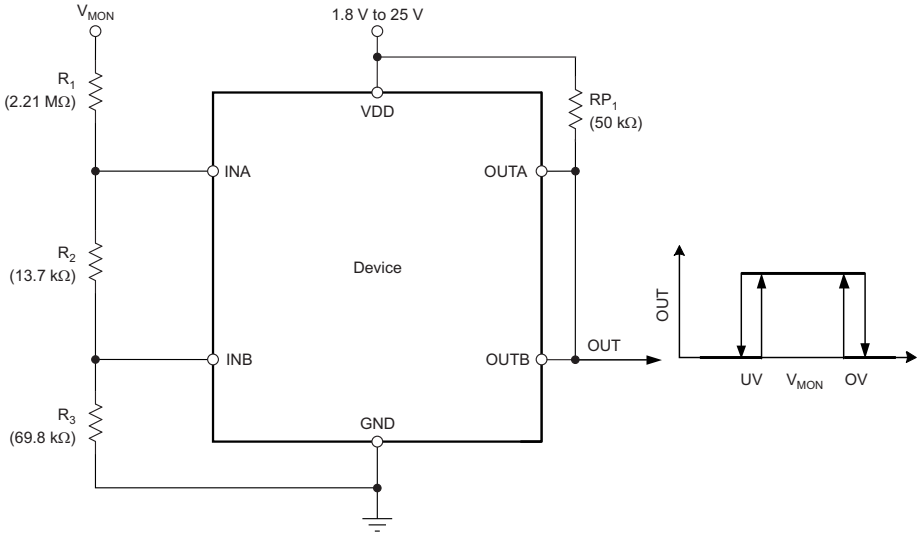


Figure 19. Window Comparator Block Diagram

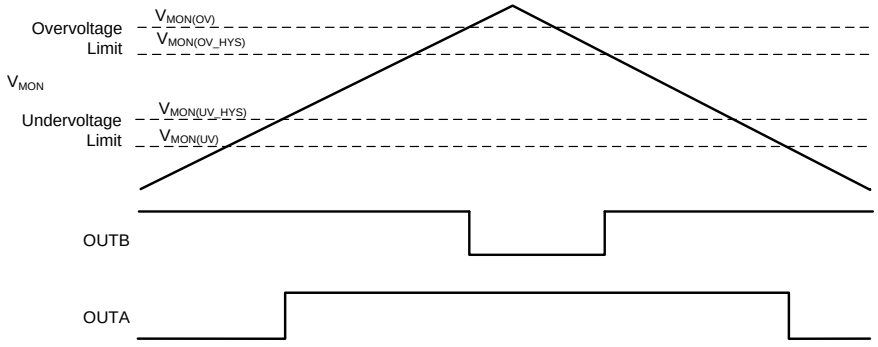


Figure 20. Window Comparator Timing Diagram

Application Information (continued)

The TLV6710 flags the overvoltage or undervoltage condition with the greatest accuracy. The highest accuracy threshold voltages are $V_{IT–(INA)}$ and $V_{IT+(INB)}$, and correspond with the falling undervoltage flag, and the rising overvoltage flag, respectively. These thresholds represent the accuracy when the monitored voltage is within the valid window (both OUTA and OUTB are in a high-impedance state), and correspond to the $V_{MON(UV)}$ and $V_{MON(OV)}$ trigger voltages, respectively. If the monitored voltage is outside of the valid window (V_{MON} is less than the undervoltage limit, $V_{MON(UV)}$, or greater than overvoltage limit, $V_{MON(OV)}$), then the input threshold voltages to re-enter the valid window are $V_{IT+(INA)}$ or $V_{IT–(INB)}$, and correspond with the $V_{MON(UV\_HYS)}$ and $V_{MON(OV\_HYS)}$ monitored voltages, respectively.

The resistor divider values and target threshold voltage can be calculated by using Equation 1 through Equation 4:

$$R_{TOTAL} = R_1 + R_2 + R_3 \quad (1)$$

Choose an R_{TOTAL} value so that the current through the divider is approximately 100 times higher than the input current at the INA and INB pins. Resistors with high values minimize current consumption; however, the input bias current degrades accuracy if the current through the resistors is too low. See application report *Optimizing Resistor Dividers at a Comparator Input* (SLVA450), for details on sizing input resistors.

R_3 is determined by Equation 2:

$$R_3 = \frac{R_{TOTAL}}{V_{MON(OV)}} \bullet V_{IT+(INB)} \quad (2)$$

where

- $V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected.

R_2 is determined by either Equation 3 or Equation 4:

$$R_2 = \left(\frac{R_{TOTAL}}{V_{MON(UV\_HYS)}} \bullet V_{IT+(INA)} \right) - R_3 \quad (3)$$

where

- $V_{MON(UV\_HYS)}$ is the target voltage at which an undervoltage condition is removed as V_{MON} rises.

$$R_2 = \left(\frac{R_{TOTAL}}{V_{MON(UV)}} \bullet V_{IT–(INA)} \right) - R_3 \quad (4)$$

where

- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected.

9.1.2 Input and Output Configurations

Figure 21 to Figure 23 show examples of the various input and output configurations.

Application Information (continued)

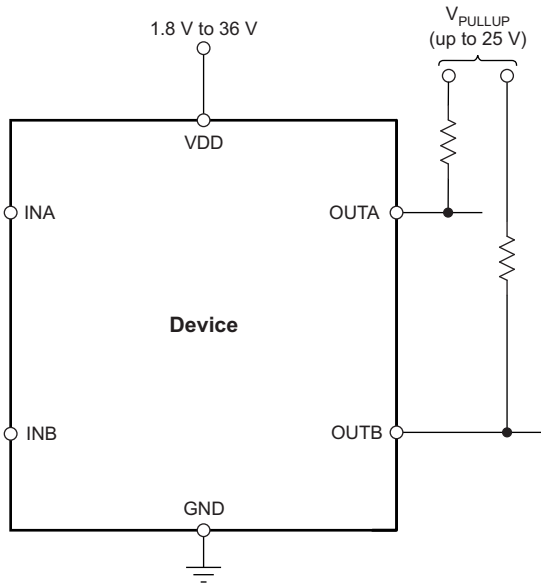


Figure 21. Interfacing to Voltages Other than V_{DD}

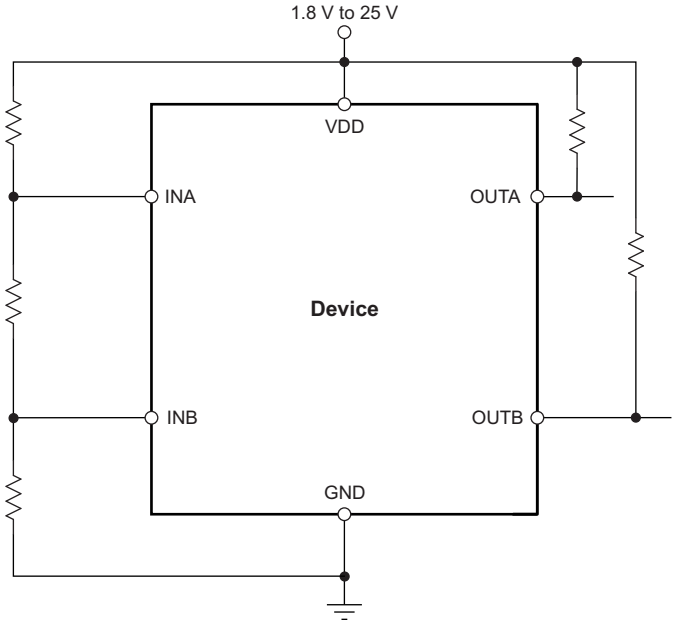
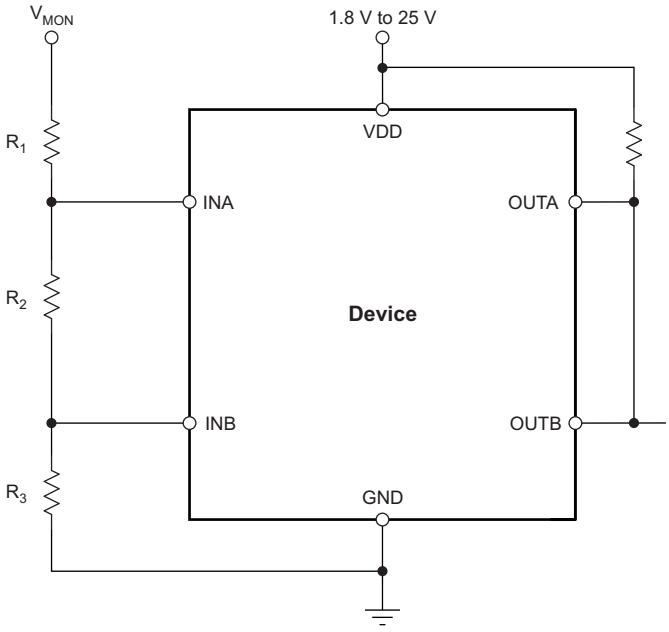


Figure 22. Monitoring the Same Voltage as V_{DD}

Application Information (continued)



NOTE: The inputs can monitor a voltage higher than V_{DD} (max) with the use of an external resistor divider network.

Figure 23. Monitoring a Voltage Other than V_{DD}

9.1.3 Immunity to Input Pin Voltage Transients

The TLV6710 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and amplitude; see Figure 3, *Minimum Pulse Duration vs Threshold Overdrive Voltage*.

9.2 Typical Application

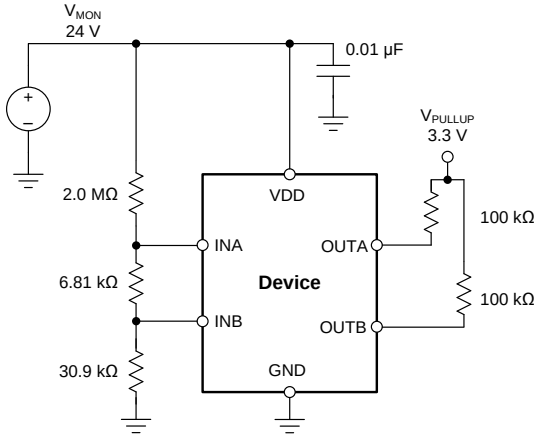


Figure 24. 24-V, 10% Window Comparator

Typical Application (continued)

9.2.1 Design Requirements

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	24-V nominal, rising ($V_{MON(OV)}$) and falling ($V_{MON(UV)}$) threshold ±10% nominal (26.4 V and 21.6 V, respectively)	$V_{MON(OV)}$ = 26.4 V ±2.7%, $V_{MON(UV)}$ = 21.6 V ±2.7%
Output logic voltage	3.3-V CMOS	3.3-V CMOS
Maximum current consumption	30 µA	24 µA

9.2.2 Detailed Design Procedure

1. Determine the minimum total resistance of the resistor network necessary to achieve the current consumption specification by using Equation 1. For this example, the current flow through the resistor network was chosen to be 13 µA; a lower current can be selected, however, care should be taken to avoid leakage currents that are artifacts of the manufacturing process. Leakage currents significantly impact the accuracy if they are greater than 1% of the resistor network current.

$$R_{TOTAL} = \frac{V_{MON(OV)}}{I} = \frac{26.4\ V}{13\ \mu A} = 2.03\ M\Omega \quad (5)$$

   where
   - $V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected as V_{MON} rises.
   - I is the current flowing through the resistor network.

2. After R_{TOTAL} is determined, R_3 can be calculated using Equation 6. Select the nearest 1% resistor value for R_3. In this case, 30.9 kΩ is the closest value.

$$R_3 = \frac{R_{TOTAL}}{V_{MON(OV)}} \bullet V_{IT+(INB)} = \frac{2.03\ M\Omega}{26.4\ V} \bullet 0.4\ V = 30.7\ k\Omega \quad (6)$$

3. Use Equation 7 to calculate R2. Select the nearest 1% resistor value for R_2. In this case, 6.81 kΩ is the closest value.

$$R_2 = \frac{R_{TOTAL}}{V_{MON(UV)}} \bullet V_{IT-(INA+)} - R_3 = \frac{2.03\ M\Omega}{21.6\ V} \bullet 0.4\ V - 30.9\ k\Omega = 6.69\ k\Omega \quad (7)$$

4. Use Equation 8 to calculate R1. Select the nearest 1% resistor value for R_1. In this case, 2 MΩ is the closest value.

$$R_1 = R_{TOTAL} - R_2 - R_3 = 2.03\ M\Omega - 6.81\ k\Omega - 30.9\ k\Omega = 1.99\ M\Omega \quad (8)$$

5. The worst-case tolerance can be calculated by referring to Equation 13 in application report *Optimizing Resistor Dividers at a Comparator Input* (SLVA450). An example of the rising threshold error, $V_{MON(OV)}$, is given in Equation 9:

$$\%\ ACC = \%\ TOL(V_{IT+(INB)}) + 2 \bullet \left(1 - \frac{V_{IT+(INB)}}{V_{MON(OV)}}\right) \bullet \%\ TOL_R = 0.75\ \% + 2 \bullet \left(1 - \frac{0.4}{26.4}\right) \bullet 1\% = 2.72\ \% \quad (9)$$

   where
   - % TOL($V_{IT+(INB)}$) is the tolerance of the INB positive threshold.
   - % ACC is the total tolerance of the $V_{MON(OV)}$ voltage.
   - % TOL_R is the tolerance of the resistors selected.

6. When the outputs switch to the high-Z state, the rise time of the OUTA or OUTB node depends on the pullup resistance and the capacitance on the node. Choose pullup resistors that satisfy the downstream timing requirements; 100-kΩ resistors are a good choice for low-capacitive loads.

9.2.3 Application Curve

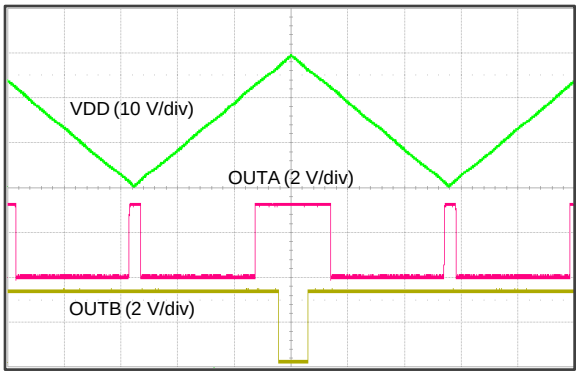


Figure 25. 24-V Window Monitor Output Response

9.3 Do's and Don'ts

It is good analog design practice to have a 0.1-µF decoupling capacitor from V_{DD} to GND.

If the monitored rail is noisy, connect decoupling capacitors from the comparator inputs to GND.

Do not use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparators without also accounting for the effect to the accuracy.

Do not use pullup resistors that are too small, because the larger current sunk by the output then exceeds the desired low-level output voltage (V_{OL}).

10 Power Supply Recommendations

The TLV6710 has a 40-V absolute maximum rating on the VDD pin, with a recommended operating condition of 36 V. If the voltage supply that is providing power to VDD is susceptible to any large voltage transient that may exceed 40 V, or if the supply exhibits high voltage slew rates greater than 1 V/µs, take additional precautions. Place an RC filter between the supply and VDD to filter any high-frequency transient surges on the VDD pin. A 100-Ω resistor and 0.01-µF capacitor is required in these cases, as shown in Figure 26.

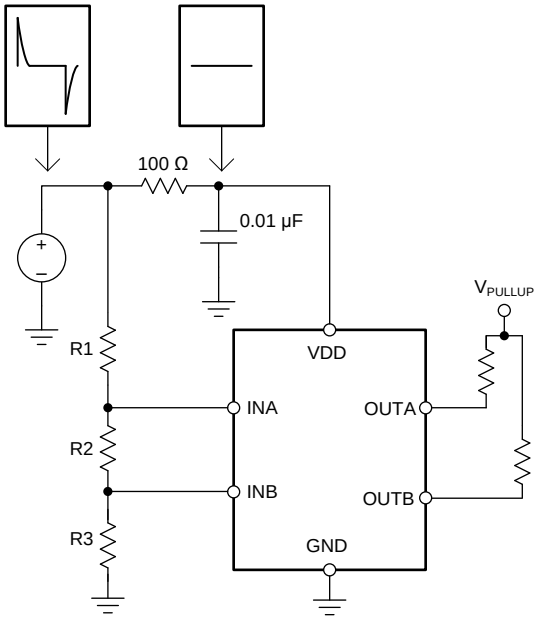


Figure 26. Using an RC Filter to Remove High-Frequency Disturbances on VDD

11 Layout

11.1 Layout Guidelines

- Place R_1, R_2, and R_3 close to the device to minimize noise coupling into the INA and INB nodes.
- Place the VDD decoupling capacitor close to the device.
- Avoid using long traces for the VDD supply node. The VDD capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, may form an LC tank and create ringing with peak voltages above the maximum VDD voltage. If this is unavoidable, see Figure 26 for an example of filtering VDD.

11.2 Layout Example

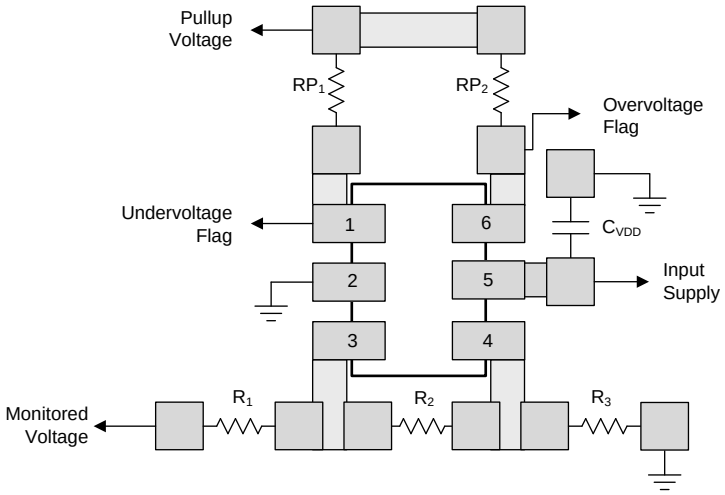


Figure 27. Recommended Layout

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

*DIP 适配器评估模块*可以将 SOT-23-6 封装转换为标准 DIP-6 引脚排列以便轻松构建原型和进行工作台评估。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

《优化比较器输入上的电阻分压器》(SLVA450)

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.5 商标

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV6710DDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1I61
TLV6710DDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1I61
TLV6710DDCRG4	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1I61
TLV6710DDCRG4.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1I61
TLV6710DDCT	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1I61
TLV6710DDCT.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1I61

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

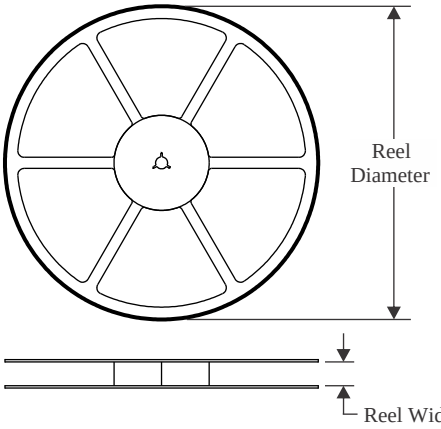
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

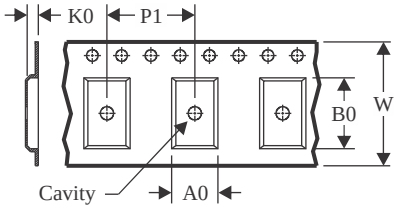
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

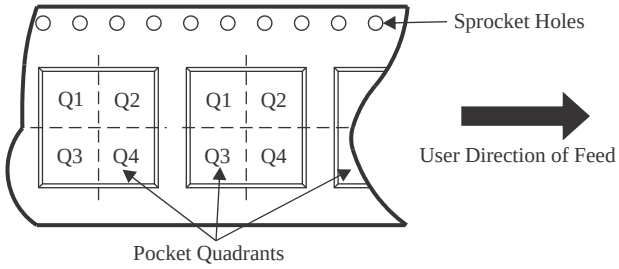


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

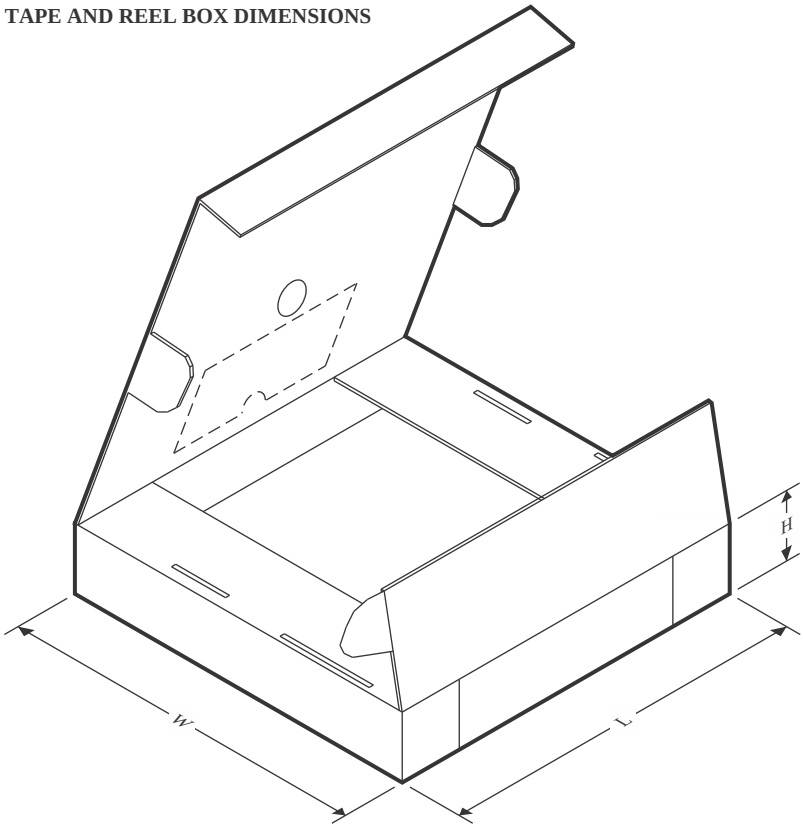
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV6710DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6710DDCRG4	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6710DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

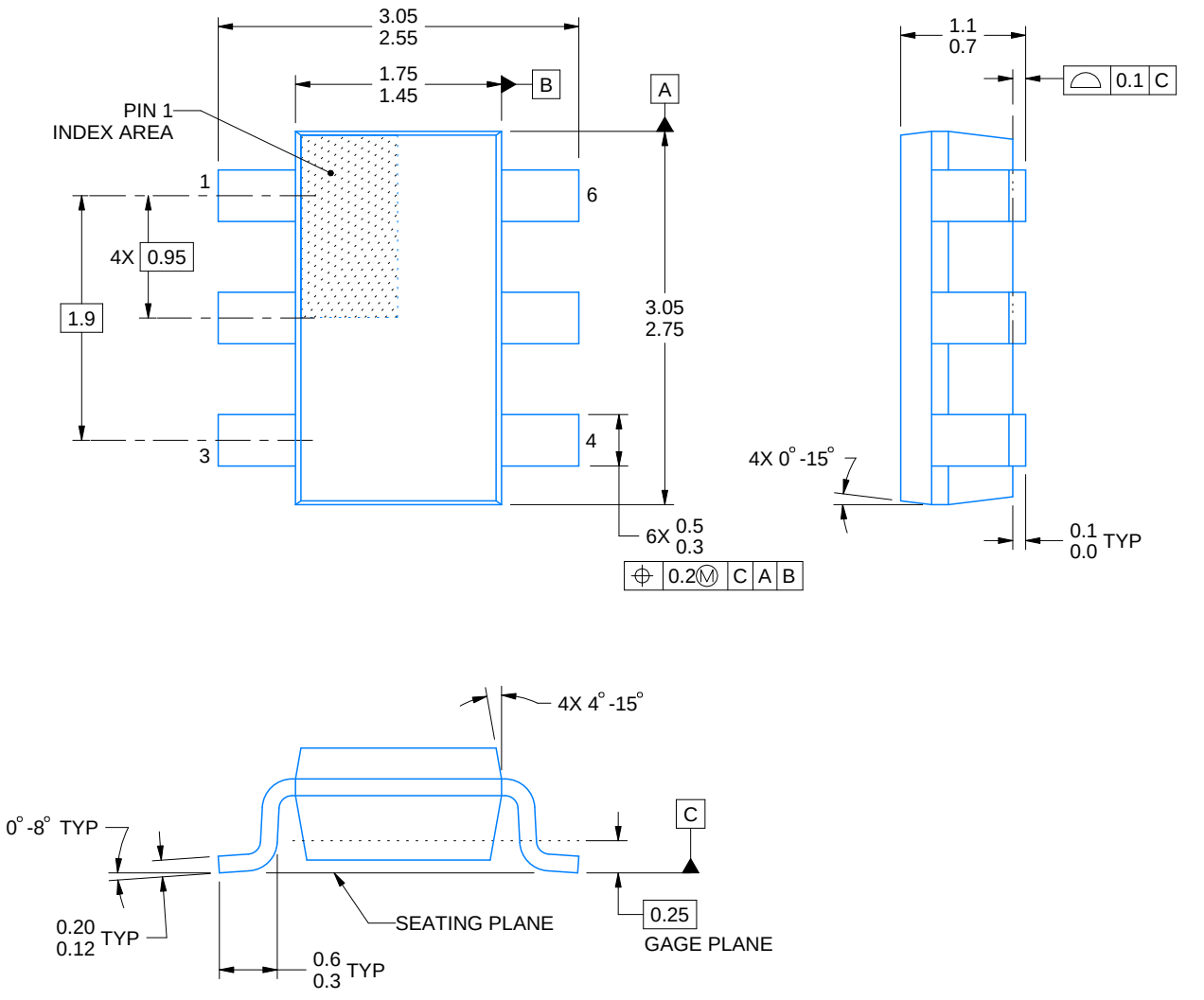
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV6710DDCR	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TLV6710DDCRG4	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TLV6710DDCT	SOT-23-THIN	DDC	6	250	213.0	191.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



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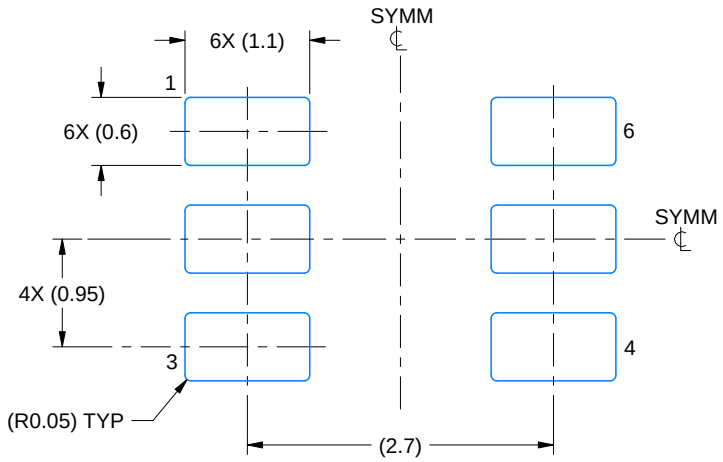
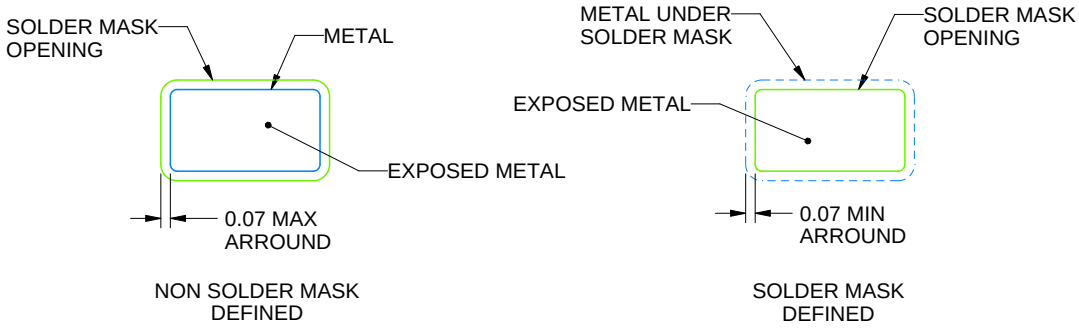
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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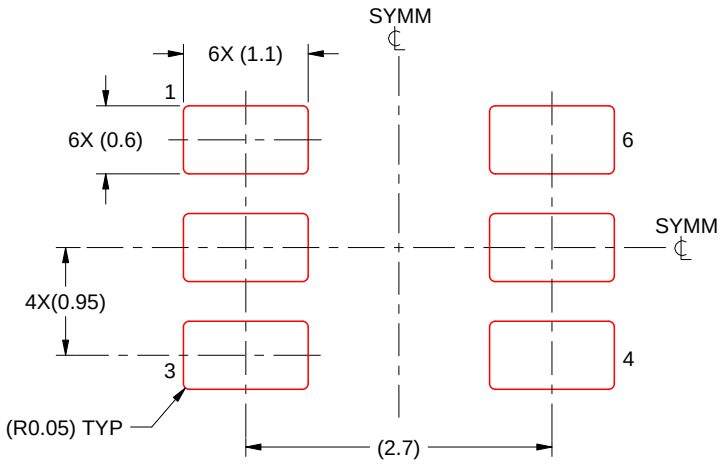
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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